



Mercedes's IPR Hearing Demonstratives for *Mercedes vs. Daedalus*

IPR2023-01345

U.S. Patent No. 10,705,588

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

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Mercedes EX1014
Mercedes-Benz USA, LLC
v. Daedalus Prime LLC
IPR2023-01345

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Grounds



Ground	References	Claims	Basis
1.	White (Ex. 1005)	Claims 1-4, 7-11, and 14-20	102 / 103
2.	White in view of Shakkarwar (Ex. 1006)	Claims 5-6 and 12-13	103
3.	Nussbaum (Ex. 1007)	Claims 1-4, 7-11, and 14-20	102 / 103
4.	Nussbaum in view of Shakkarwar	Claims 5-6 and 12-13	103

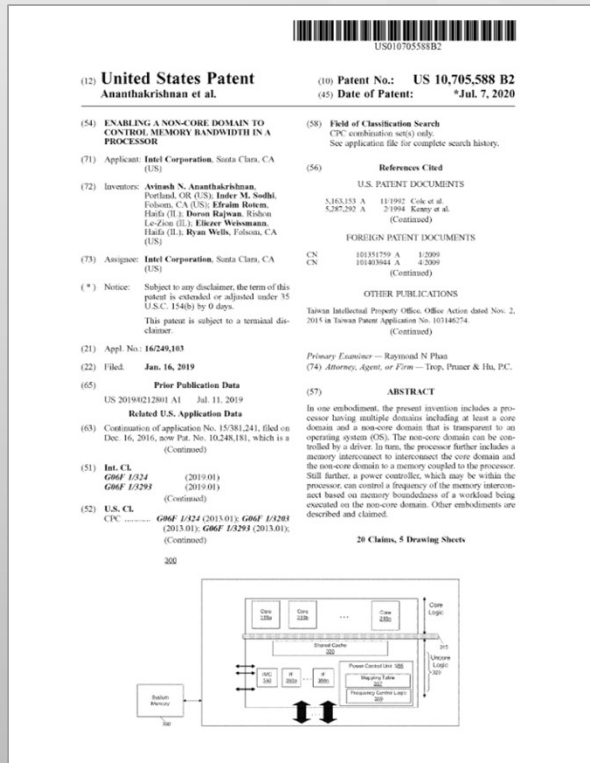
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Overview of the '588 Patent



- The '588 Patent discloses a system containing:
 - at least two processing cores,
 - a graphics engine, and
 - an interconnect.
- The cores, graphics engine, and interconnect can be dynamically controlled to operate at different frequencies.

'588 at 6:11-24, 30-44; Horst Decl. ¶¶ 42-47.

Overview of the '588 Patent



1. A processor comprising:

a plurality of cores including a first core operable at a first voltage and at a first frequency, and a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and

an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.

Claim 1 is representative and generally recites an integrated circuit including:

- a first core operable at a first voltage and first frequency
- a second core operable at a second voltage and frequency
- graphics processing circuitry operable at a third frequency
- an interconnect, operable at a fourth frequency, coupling the graphics processing circuitry to a memory

Overview of the '588 Patent



2. The processor of claim 1, further comprising: first power management circuitry and/or logic to cause the first core to operate at the first frequency and to cause the second core to independently operate at the second frequency.

4. The processor of claim 2, further comprising: second power management circuitry and/or logic to cause the graphics processing circuitry to operate at the third frequency.

5. The processor of claim 4, wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.

Claim 5 depends from claims 1, 2, and 4 and requires:

- first power management circuitry to cause the first and second cores to operate at the first and second frequencies,
- second power management circuitry to cause the graphics processing circuitry to operate at the third frequency, and
- a mapping of selectable frequencies of the graphics processing circuitry to those of the interconnect

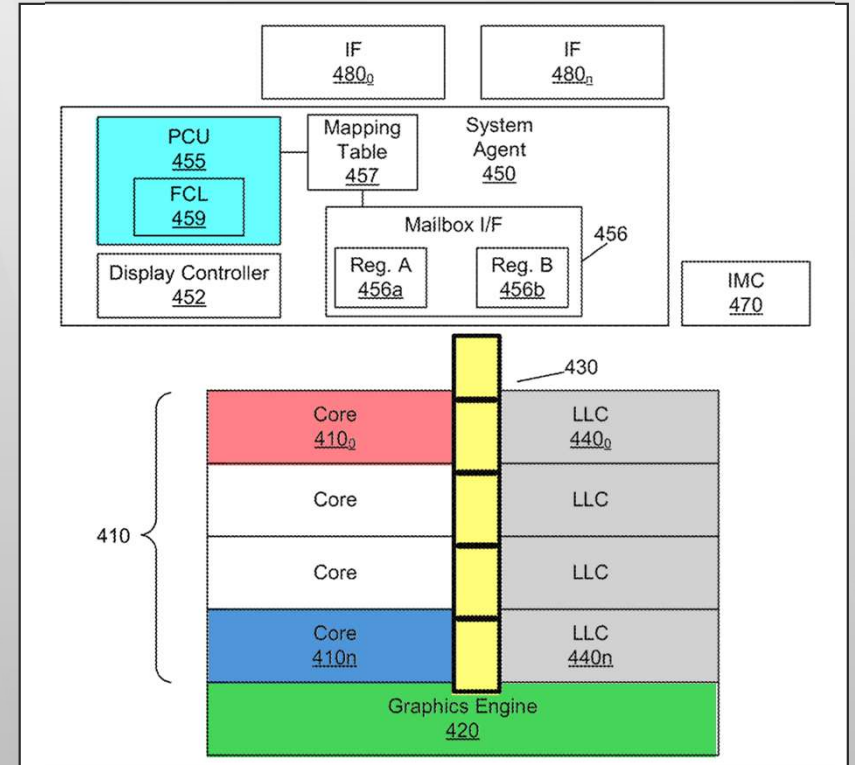
Overview of the '588 Patent



Fig. 4 depicts a system having:

- Graphics Engine **420**
- CPU cores **410_a** and **410_n**
- Interconnect **430**
- Power Control Unit (PCU) **455** can cause such components to dynamically operate at different frequencies.

'588 Patent at 6:11-24, 30-44; Horst Decl. ¶¶ 42-47.



'588 Patent at Fig. 4 (annotated)

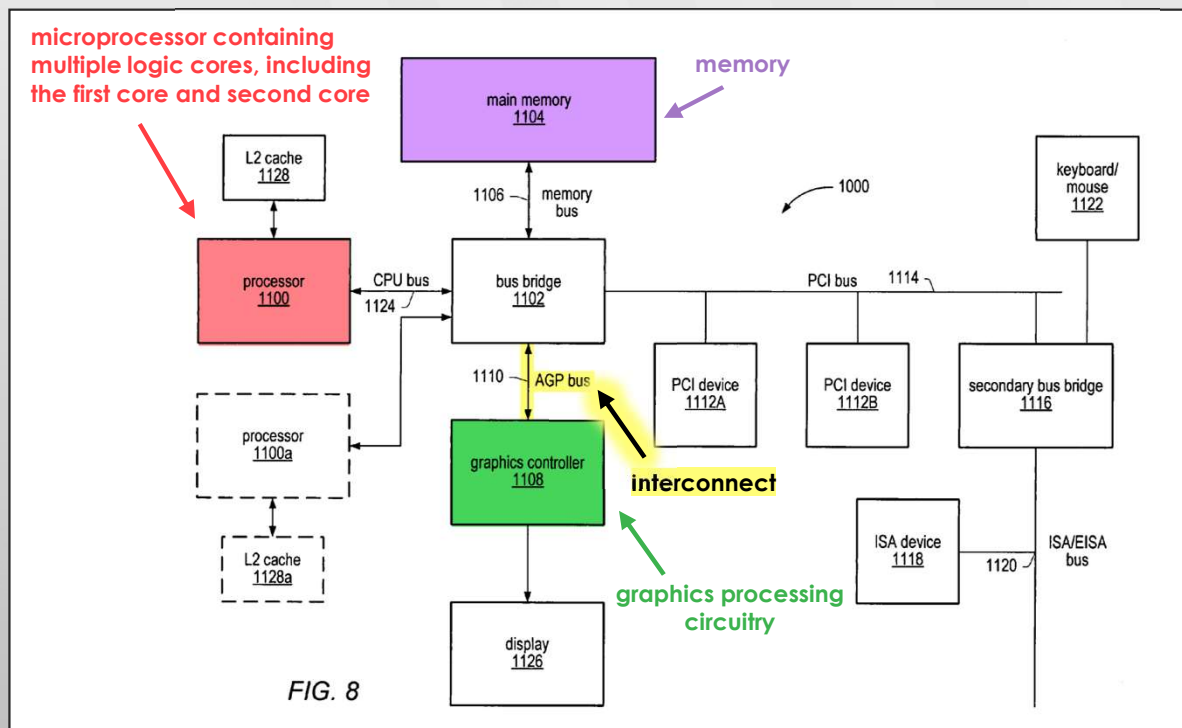
Prior Art References

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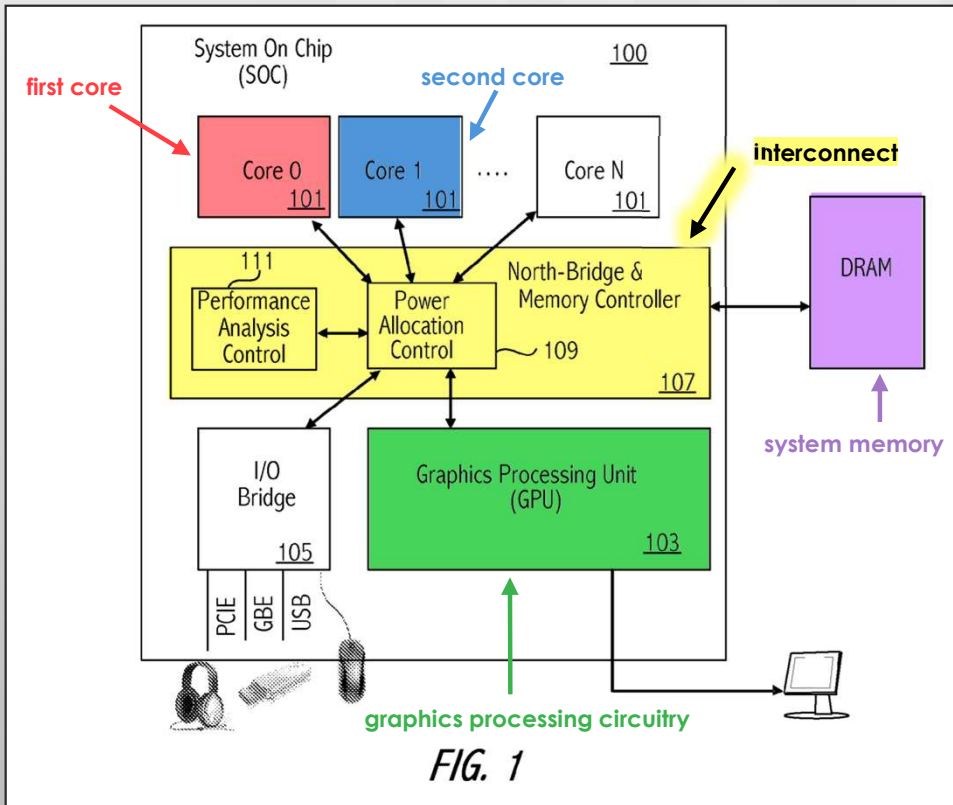
Overview of White



White at Fig. 8 (annotated).

- White discloses independently controlling frequencies and/or voltages of:
 - logic cores
 - a graphics controller
 - common bridge / AGP bus (i.e., interconnects) coupling the graphics controller to a memory

Overview of Nussbaum



Nussbaum at Fig. 1 (annotated).

- Nussbaum discloses power allocation control circuitry that independently adjusts the frequency and/or voltage of:
 - multiple processing cores
 - a graphics processing unit (GPU)
 - a North-Bridge (i.e., interconnect) coupling the GPU to a memory

Overview of Shakkarwar

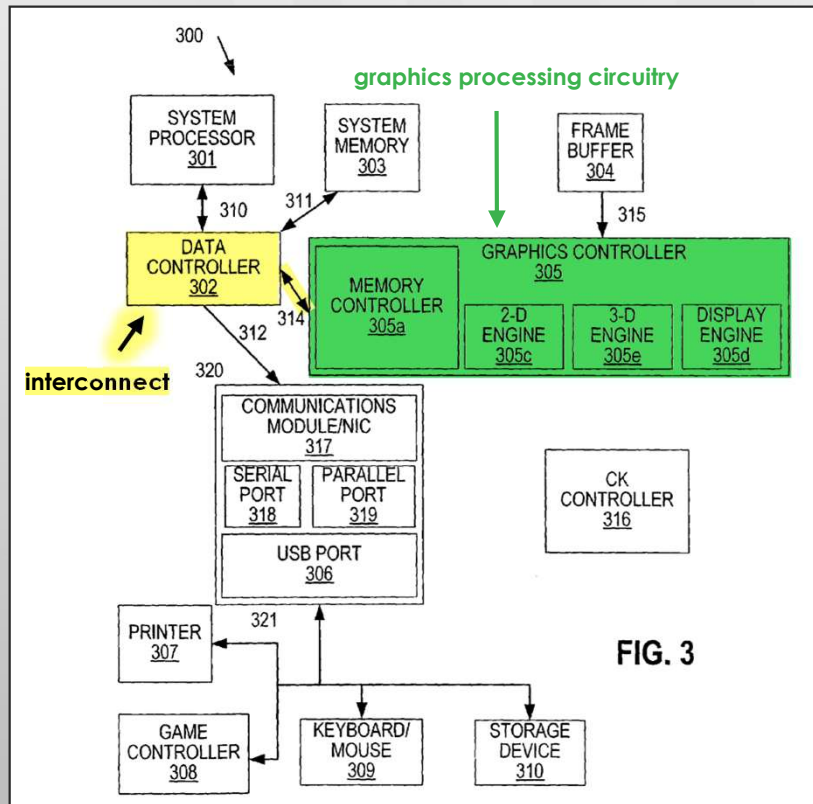


FIG. 3

Shakkarwar at Fig. 3 (annotated).

Shakkarwar discloses:

- a graphics controller
- a data controller/bus (i.e., interconnect) coupling the graphics controller to a memory
- adjusting the bus rate (i.e., frequency) of the interconnect based on the bandwidth requirements of the graphics controller.

Shakkarwar at 6:49-52.

Overview of Shakkarwar

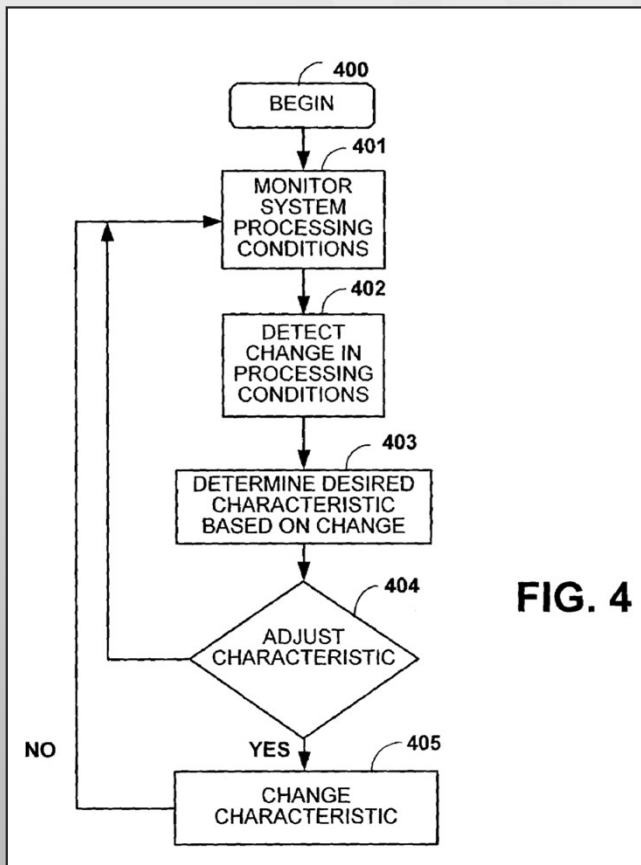


FIG. 4

- Fig. 4 depicts a method for managing power consumption:
 - **401** – monitor bandwidth of a component (e.g., graphics circuitry) for increasing or decreasing requirements
 - **402** – detect a change in the graphics circuitry's required bandwidth, such as when a 3-D graphics applications is started
 - **403** – determine the new bandwidth required for the graphics circuitry's data connection (i.e., interconnect) based on a look-up table containing clock speeds (i.e., frequencies)
 - **404** – determine whether the bandwidth of the interconnect should be modified
 - **405** – adjust the data rate of the interconnect, such as by increasing its frequency

Shakkarwar at 6:41-43, 49-52, 6:59-7:10, 7:26-29, Fig. 4.

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Dispute – Whether Shakkarwar discloses or renders obvious the “mapping of selectable frequencies . . .” limitation

The “Mapping of Selectable Frequencies . . .” Limitation



Claims 5 and 12 each recite “a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect”

Shakkarwar Discloses the Claimed “Selectable Frequencies”



- Shakkarwar describes selecting “clock...levels” (i.e., frequencies) of “graphics controller 305”:

and/or modules. Clock/voltage control 316 provides operating characteristics for each of system processor 301, data controller 302, IO device 320, and graphics controller 305. Clock and voltage levels of each processor, device, and or controller are alterable based on bandwidth requirements for communicating and processing information.

Shakkarwar at 5:25-30, 2:51-58;
Horst Decl. ¶ 140 n.4.

- Shakkarwar describes a selectable “clock rates” (i.e., frequencies) of a “communication bus” (i.e., interconnect):

bus having multiple operating voltage levels. The clock generator and communication bus are operated at variable clock rates and voltage levels to ensure bandwidth requirements are satisfied for communicating and processing information. In

Shakkarwar at Abstract, 2:51-58;
Horst Decl. ¶ 140 n.4.

Shakkarwar Discloses When “Mapping” is Performed



- Shakkarwar illustrates an association between graphics controller and interconnect frequencies:

For example, when an application that is known to use 3-D graphics is opened, system software can determine if the bus rate between the data controller and the graphics controller is high enough to support the graphics requirements. Likewise,

Shakkarwar at 6:49-52.

- Selecting to open a 3-D graphics program increases graphics controller frequency and bandwidth requirements, causing an associated increase in interconnect bus rate (i.e., frequency).
- Thus, when graphics circuitry frequency increases, Shakkarwar indicates that a determination of a required interconnect bus rate (i.e., frequency) is also made.

Horst Decl. ¶ 140 n.4

Shakkarwar Discloses a “Mapping”



- Shakkarwar describes using a look-up table listing devices' / components' clock speeds (i.e., frequencies) required to process a given amount of information.

Upon detecting a change in processing, the method determines bandwidth **403** for an associated data connection based on the **active components**. For example, a **look-up table** may include a list of clock speeds, and/or voltage levels required to process information for **specific devices and/or groups of devices**. Additionally, bandwidth requirements associated

Shakkarwar at 7:5-10.

- Such “components” and “devices” include the graphics controller 305 and data controller 302 (i.e., interconnect).

Shakkarwar at Abstract, 2:24-39, 6:41-43, 49-52; Horst Decl. ¶¶ 137-138, 140, 145.

Shakkarwar Discloses a “Mapping”



- Shakkarwar thus teaches the claimed mapping association between the frequencies of the data controller 302 interconnect and graphics controller 305.

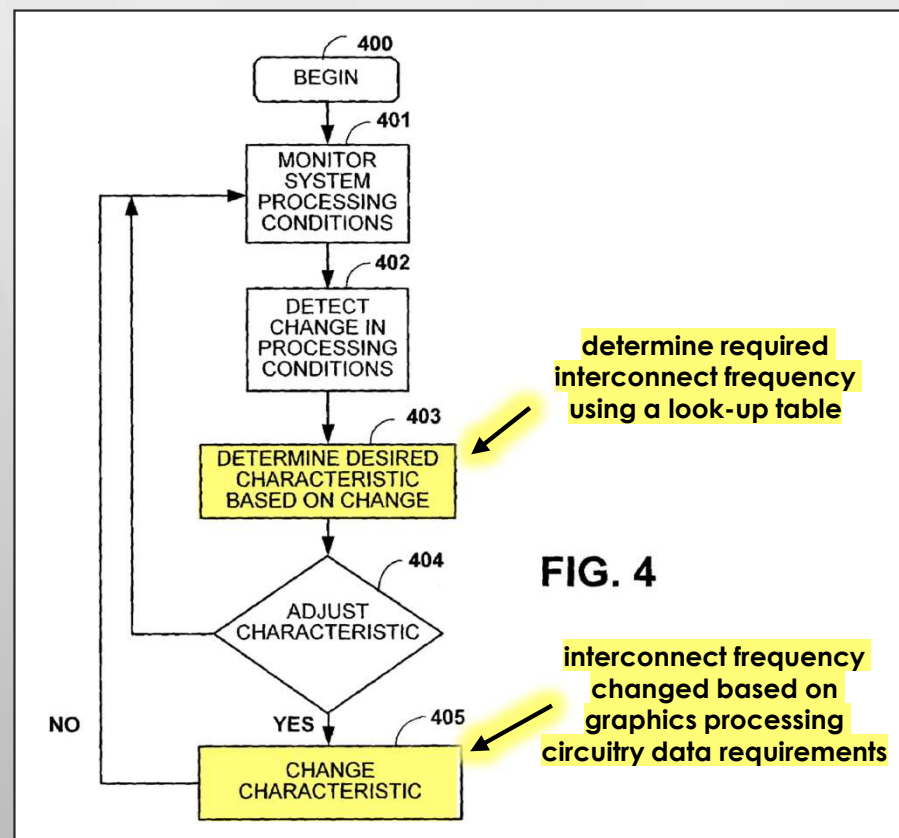
140. Shakkarwar thus teaches determining the appropriate bandwidth for a data connection to a module (e.g., graphics controller 305), utilizing a look-up table that includes a list of appropriate clock speeds⁴. (*Id.*, 7:5-10) It also considers other active components, such as the data controller 302 (e.g., the “interconnect”) and its clock speeds. (White, 7:5-10) As such, a POSITA would have understood that Shakkarwar teaches to map selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect using look-up tables.

Horst Decl. ¶ 140.

Shakkarwar Discloses a “Mapping”

- Bandwidth is a function of frequency.
- Shakkarwar describes determining the interconnect frequency based on graphics circuitry bandwidth needs.
- Shakkarwar's graphics circuitry frequency is therefore associated with a selectable interconnect frequency.

Horst Decl. ¶¶ 138-42 & n.4.



Shakkarwar at Fig. 4 (annotated).

“Clock Speed” is Undisputedly “Frequency”



- Dr. Horst explains that “frequency” is synonymous with “clock speed.”
- Daedalus’s expert, Dr. Brogioli, agrees that “frequency” is tantamount to “clock speed.”

⁴ A POSITA would understand that Shakkarwar’s “clock speed” is another term for “clock frequency.” A subsystem, such as a processor core has a clock signal delivered to various components to control the speed of operation. In this context, “frequency,” “clock frequency” and “clock rate” are synonymous. Bandwidth is

Horst Decl. ¶ 140 n.4.

Stepping back from the '588 patent, what is the frequency of a processing core?

that's not necessarily always the case, but in a simple example it's kind of the clock speed the thing is running at.

Brogioli Tr. (Ex. 1013) 28:17-29:6,
see also 29:7-11 (same, for GPUs), 29:12-24 (same, for interconnects)

Daedalus' Expert's Testimony



- Dr. Brogioli admits that Shakkarwar's look-up table determines bus (i.e., interconnect) frequencies

41. Shakkarwar determines a frequency to change the bus to by using "a look-up table [that] may include a list of clock speeds ... required to process information for specific devices and/or groups of devices." *Id.* at 7:7-10.

Brogioli Decl. ¶ 41.

- Shakkarwar's look-up table thus contains such interconnect frequencies based on Dr. Brogioli's description of how such tables operate

Speaking more generally what is a look-up table?

A. I think a generic example would be if you had a table of three entries and I went to look at what's at Row 2 or something, there would be some values there in a generic sense.

Brogioli Tr. 24:2-15; see also 57:17-58:9.

Daedalus' Expert's Testimony



- Dr. Brogioli states Shakkarwar's look-up table contains clock speeds (i.e., frequencies) of "computational components."
- Daedalus itself states that the clock speeds of computational components include those of "graphics processing circuitry."

"A module can be removed when it becomes enabled or disabled, for example, not used for a specific amount of time, time-outs, et cetera."

So it looks like those devices are computational components, for example, for which the look-up table includes clock speeds and voltage levels for processing information.

Brogioli Tr. 52:15- 53:14.

While the look-up table² of Shakkarwar may provide a list of clock speeds for graphics processing circuitry, there is no teaching or suggestion that

Patent Owner's Sur-reply at 5.

Reply at 5-8.
PO Sur-reply at 5 & n.2.

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Shakkarwar Discloses a the Claimed “Mapping . . .”



Patent Owner argues:

Shakkarwar lacks the “mapping of frequencies-to-frequencies” required by the claims because it “describes only a table that includes clock speeds and/or voltage levels required to process information for specific devices”

But:

- **Shakkarwar’s look-up table contains the requisite “mapping” association**

- It contains frequencies for “devices” / “components” including interconnects and graphics circuitry

Horst Decl. ¶¶ 134-149, 212-227; Brogioli Decl. ¶ 41; Brogioli Tr. 52:15-53:14; Patent Owner’s Sur-reply at 5-7.

Upon detecting a change in processing, the method determines bandwidth **403** for an associated data connection based on the **active components**. For example, a **look-up table** may include a list of clock speeds, and/or voltage levels required to process information for **specific devices and/or groups of devices**. Additionally, bandwidth requirements associated

Shakkarwar at 7:5-10.

Shakkarwar Discloses a the Claimed “Mapping . . .”



Patent Owner argues:

Shakkarwar lacks the “mapping of frequencies-to-frequencies” because it “monitors bandwidth, not frequency”

But:

- Bandwidth is proportional to frequency:

⁴ A POSITA would understand that Shakkarwar’s “clock speed” is another term for “clock frequency.” A subsystem, such as a processor core has a clock signal delivered to various components to control the speed of operation. In this context, “frequency,” “clock frequency” and “clock rate” are synonymous. Bandwidth is the product of frequency and the width of the connection. Sending 16 bits (2 bytes) at a frequency of 1 MHz is a bandwidth of 2 MB/s (Mega-Bytes per Second). With a fixed width connection, bandwidth increases in direct proportion to frequency.

Horst Decl. ¶ 140 n.4