

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MERCEDES-BENZ USA, LLC,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-01345
Patent 10,705,588 B2

Before WILLIAM V. SAINDON, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

SAINDON, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Mercedes-Benz USA, LLC (“Petitioner”) filed a petition (Paper 2, “Pet.”) to institute *inter partes* review of claims 1–20 of U.S. Patent No. 10,705,588 B2 (Ex. 1001, “the ’588 patent”). We instituted *inter partes* review on February 29, 2024. Paper 8. Subsequent to institution, Daedalus Prime LLC (“Patent Owner”) filed a Response (Paper 10, “PO Resp.”), after which Petitioner filed a Reply (Paper 13, “Pet. Reply”) and Patent Owner filed a Sur-reply (Paper 14, “Sur-reply”). An oral argument was held on December 3, 2024, a transcript of which is found in Paper 21 (“Tr.”).

We have authority to enter this final written decision under 35 U.S.C. § 318(a). The standard for review is set forth in 35 U.S.C. § 316(e), which provides that “the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.” For the reasons provided below, we determine that Petitioner has met the burden of establishing unpatentability of some, but not all, challenged claims. In particular, we determine that Petitioner has established the unpatentability of claims 1–4, 7–11, and 14–20 but not of claims 5, 6, 12, and 13.

B. Real Parties in Interest

Petitioner states that its real parties in interest are Mercedes-Benz USA, LLC, Mercedes-Benz Intellectual Property GmbH & Co. KG, Mercedes-Benz Group AG, and Mercedes-Benz AG. Pet. 2. Patent Owner states that its real party in interest is Daedalus Prime LLC. Paper 5, 2 (Patent Owner’s Mandatory Notice).

C. Related Matters

The parties both identify the following related matters outside the USPTO: *Daedalus Prime LLC v. Mazda Motor Corp.*, Case No. 1-22-cv-01109 (D. Del.), filed August 23, 2022, and dismissed against certain defendants—including Mercedes-Benz Group AG, Mercedes-Benz AG, and Mercedes-Benz USA, LLC—on March 20, 2023; *In the Matter of Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (U.S. International Trade Commission), filed September 12, 2022; *Daedalus Prime LLC v. Arrow Electronics, Inc.*, Case No. 1-22-cv-01107 (D. Del.), filed August 23, 2022, and dismissed on March 1, 2023; *Daedalus Prime LLC v. Mazda Motor Corp.*, Case No. 1-22-cv-01108 (D. Del.), filed August 23, 2022, and dismissed on November 14, 2022; *In the Matter of Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (U.S. International Trade Commission), filed August 23, 2022, and terminated on February 27, 2023; and *Daedalus Prime LLC v. Samsung Electronics Co.*, Case No. 2:22-cv-352 (E.D. Tex.), filed September 12, 2022, and dismissed as to the '588 patent on June 6, 2023. Pet. 2–3; Paper 5, 2.

The parties both identify the following related matters within the USPTO: *Qualcomm Inc. v. Daedalus Prime LLC*, IPR2023-00547 (PTAB), filed on February 2, 2023 (hereinafter the “Qualcomm IPR,” previously captioned as “*Samsung Electronics Co., v. Daedalus Prime LLC*”) (terminated on January 12, 2024 due to settlement). Pet. 4; Paper 5, 3.

D. Prior Art and Asserted Grounds

Petitioner’s grounds rely on the following prior art references:

Name	Reference	Exhibit No.
White	U.S. Pat. No. 7,263,457 B2, iss. Aug. 28, 2007	1005
Shakkarwar	U.S. Pat. No. 7,392,411 B2, iss. June 24, 2008	1006
Nussbaum	U.S. Pat. App. Pub. 2011/0022356 A1, pub. Jan. 27, 2011	1007

Petitioner asserts that the challenged claims would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–4, 7–11, 14–20	102	White
1–4, 7–11, 14–20	103	White
5, 6, 12, 13	103	White, Shakkarwar
1–4, 7–11, 14–20	102	Nussbaum
1–4, 7–11, 14–20	103	Nussbaum
5, 6, 12, 13	103	Nussbaum, Shakkarwar

Petitioner relies on the testimony of Robert W. Horst, Ph.D (Ex. 1003). Patent Owner relies on the testimony of Michael C. Brogioli, Ph.D (Ex. 2002).

E. Technical Background and Overview of the '588 Patent

The '588 patent is directed to a processor having multiple domains. The core domain contains the processor cores, whereas the non-core domain contains other components such as a graphics engine. Ex. 1001, 2:19–21. The various core and non-core components are connected via an interconnect in order to communicate with each other and to have access to other system devices such as memory. *Id.* at 2:3–6; *see* Fig. 4 (noting cores 410, graphics engine 420, interconnect 430, memory controller 470). Each of these components can operate at different frequencies, and those frequencies can be controlled by the power management circuitry. *Id.* at 5:41–43, 5:51–60. In particular, the power management circuitry of the '588

patent references a mapping table that associates a domain's frequency with a minimum interconnect frequency required. *Id.* at 5:60–63. In this way, each domain can be assured that the interconnect is working fast enough to support that domain. *Id.* at 2:21–25.

The '588 patent assumes that the reader is familiar with several basic concepts not described in detail, and for which we attempt a brief primer. The '588 patent suggests that the frequency is a direct driver of performance, due to frequency's impact on bandwidth. *Id.* at 2:6–18. Thus, we review the concepts of frequency and bandwidth.

Roughly speaking, the frequency at which a digital device operates is controlled by the clock to which it is connected. In particular, a clock delivers a signal that drives the speed of a device's operation. Ex. 1003 ¶ 140 n.4; Ex. 1005, 2:49–54. The “clock speed,” “clock rate,” “clock frequency,” or simply, “frequency,” is a value measured in Hertz. Ex. 1003 ¶ 140 n.4; Ex. 1005, 2:53–54. The faster the device is clocked, the faster the device operates (up to some physical constraint such as a power or thermal limit). Ex. 1003 ¶ 140 n.4; *see* Ex. 1001, 2:8–10. For purposes of this Decision, we will consider clock speed, clock rate, clock frequency, and frequency to be interchangeable terms.

“Bandwidth” refers to the amount of data a device can process in a given amount of time. Ex. 1005, 2:54–64, 3:4–8. Bandwidth is proportional to the frequency of the device (and thus, clock speed) because it is calculated as the product of frequency and the data connection width. Ex. 1003 ¶ 140 n.4 (“Bandwidth is the product of frequency and the width of the connection.”); Ex. 1013, 28:17–29:6 (deposition of Patent Owner's expert, agreeing). In this way, there is a direct connection between the two, e.g.,

increasing frequency increases bandwidth. The terms *bandwidth* and *data rate* are also interrelated, with one reference using “bandwidth” to describe the *capability* to move data through a path and “data rate” to describe the *amount* of data moving through the path. *See* Ex. 1006, 7:5–39. Although bandwidth, data rate, and frequency are not necessarily equivalent, they are highly interrelated, as each generally refers to the data processing capability of the device. For purposes of this Decision, we will consider bandwidth, data rate, and frequency to be interchangeable terms.

F. Challenged Claims

Claims 1–20 are challenged. Claims 1, 8, and 20 are independent. Claims 1 and 5 are reproduced below. Although claim 5 does not directly depend from claim 1, the particular subject matter recited in intervening claims 2 and 4 does not need to be reproduced to understand the issues addressed in this Decision.

1. A processor comprising:

a plurality of cores including a first core operable at a first voltage and at a first frequency, and a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and

an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.

5. The processor of claim 4,

wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.

II. ANALYSIS

A. Legal Standards Used in the Merits Analysis

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious . . . to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that:

A person of ordinary skill in the art (“POSITA”) of the ’588 would have had a bachelor’s degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and additional experience substituting for formal education.

Pet. 13–14 (citing Ex. 1003 ¶¶ 26–30). Patent Owner applies the same definition, but modifies it to remove the words “at least” in the phrase, “at least two years of experience.” PO Resp. 7–8. Patent Owner argues that a person of ordinary skill in the art would have two years of experience, and argues that “at least two years of experience” means that they could have many more years of experience. *Id.* at 8.

As we understand it, Patent Owner is arguing that the phrase “at least [X] years of experience” creates a definition of the level of ordinary skill that has no upper bound, and that such unbounded definitions are improper. We believe an example of this would be that, because “20 years” is “at least 2 years,” then a person with 20 years of experience may be considered a person of ordinary skill, when perhaps in reality they have extraordinary skill.

We are not inclined to adopt Patent Owner’s proposal to require a specific number of years (or a fully bounded range) in the definition of the level of ordinary skill in the art. First, Patent Owner has not offered any legal authority supporting or explaining its position. Second, using the term

“at least [X] years” is common practice and generally understood to be an approximation regarding the minimum level of skill of a *hypothetical* person—in other words, no precision can truly be expected of the specific number of years in this context. *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (“The person of ordinary skill in the art is a hypothetical person.”). The point of the exercise is to provide context for a holistic obviousness analysis. *See id.* (setting out “various factors” used to analyze the level of ordinary skill); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991) (“The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.”); *Kimberly-Clark Corp. v. Johnson & Johnson*, 745 F.2d 1437, 1453 (Fed. Cir. 1984) (the hypothetical person is an “an imaginary being possessing ‘ordinary skill in the art’ created by Congress to provide a standard of patentability”). We are not persuaded of a need for strict precision in the number of years of experience of a hypothetical person used in our analysis in this case. Third, Patent Owner asks for no particular relief based upon its argument. That is, even if we agreed to remove “at least,” Patent Owner does not argue that the outcome of the Decision would be any different.¹

¹ For example, setting the level of skill to exactly two years of experience would not serve to automatically disqualify an expert having ten years. *Kyocera Senco Ind’l Tools v. Int’l Trade Com’n*, 22 F.4th 1369, 1377 (Fed. Cir. 2022) (requiring that “a witness must at least have ordinary skill in the art” and stating that “it would be improper to require an expert witness to possess ordinary skill in the art and *nothing more*”).

In conclusion, we apply Petitioner’s proposed level of ordinary skill because it is reasonably consistent with the level of skill implied in the disclosure of the ’588 patent and the cited prior art.

C. Claim Construction

Under 37 C.F.R. § 42.100(b), we apply the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). That is, “the words of a claim ‘are generally given their ordinary and customary meaning’ . . . that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1312–13.

Claims 5 and 12 recite “a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.” The chief dispute in this case involves whether the prior art teaches this “mapping” limitation. *See* PO Resp. 19–22, 26–29; Pet. Reply 2–8; Sur-reply 1–7. Petitioner offers no particular construction and relies on ordinary and customary meaning. *See* Pet. 12. Patent Owner asserts that “the Board should construe claims 5 and 12 as requiring a mapping of a *set of possible frequencies* of the graphics processing circuitry that can be selected to a *set of possible frequencies* of the interconnect that can be selected.” PO Resp. 9 (emphasis added). Patent Owner’s construction is based on Petitioner’s expert’s testimony. *Id.*; Ex. 2001, 21:19–22:2.² In its Reply, Petitioner does not dispute Patent Owner’s construction as much as dispute whether the

² [Counsel]: “What would the person of ordinary skill in the art understand is the plain and ordinary meaning of “selectable frequencies” in [claim 5]?”
[Witness]: “I interpret that to mean that there are a set of possible frequencies that can be selected.”

reference teaches the limitation. *See, e.g.*, Pet. Reply 5 (arguing, “[t]his association [in the prior art] between corresponding frequencies is a ‘mapping’”). Patent Owner’s Sur-reply argues along a similar path, but in the opposite direction, that the prior art has “no association—no *mapping*—of frequencies-to-frequencies as demanded by the challenged claims.” Sur-reply 1. Accordingly, resolving the dispute between the parties requires a detailed understanding of the “mapping” limitation.

The specification of the ’588 patent describes a situation where a non-core domain (e.g., a graphics domain) accesses memory through an interconnect. Ex. 1001, 2:3–6. The higher the frequency of the interconnect, the higher the bandwidth to the memory, allowing higher graphics performance. *Id.* at 2:10–13. Other designs set interconnect frequency (i.e., bandwidth) as a function of *core* domain demand (the core generally having a higher impact on power demands), but this can lead to reduced performance in non-core domains. *Id.* at 2:6–15. Thus, the ’588 patent seeks to provide the non-core domain with some degree of control over the interconnect. *Id.* at 1:67–2:3, 2:21–25. The solution is to provide a mapping of “non-core domain frequency to a corresponding interconnect frequency.” *Id.* at 2:28–30; *see also id.* at 2:44–46. The mapping allows a power control unit to use the non-core frequency value to lookup an interconnect frequency that supports that particular non-core frequency. *Id.* at 3:10–14. This can be done using a table. *Id.* at 3:5–16. Below is a partial reproduction of Table 1 of the ’588 patent, showing a mapping of non-core frequencies and their corresponding interconnect frequencies:

Table Entry	Non-Core Frequency	Minimum Interconnect Frequency
1	300	800

Table Entry	Non-Core Frequency	Minimum Interconnect Frequency
2	350	800
3	400	800
4	450	800
5	500	800
6	500	800
7	600	800
8	650	1500
9	700	1500
11 [sic]	750	1500
12	800	1500
13	850	1500
14	900	1800
15	950	1900
...	...	...
22	1300	2600

Ex. 1001, 5:15–35. Table 1 shows a set of selectable frequencies for the non-core domain, each of which is associated with (i.e., mapped to) one of the set of corresponding interconnect frequencies. For example, if the non-core device is to operate at a frequency of 650 MHz, then the minimum interconnect frequency must be at least 1500 MHz. In this way, “the embodiments described [in the ’588 patent] enable [the non-core domain] this ability [to control its memory/interconnect bandwidth] by a mechanism that maps non-core domain frequency to a *corresponding* interconnect frequency.” *Id.* at 2:19–39 (emphasis added).

The description of “mapping” in the ’588 patent makes clear to us that it is an *association of an input value* from a set of input values *to a corresponding output value* from a set of output values. *Id.* at 2:44–46 (describing “the mapping table that *associates* non-core domain operating frequencies and *corresponding* interconnect operating frequencies”)

(emphases added). The “association” described here in the ’588 patent is not merely describing the fact that both exist, but that knowing the value of the first causes you to know the value of the second. This is also how it is described in the claims, wherein the “mapping” is “*of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.*” *Id.* at 8:63–65 (emphasis added). Or more generally, the claim recites a mapping of a frequency *to* a frequency.

In sum, although we agree with the parties that “mapping” should be given its plain and ordinary meaning in light of the specification, we note that the parties appear to dispute whether the prior art teaches the claimed “mapping” based on differing understandings of the plain and ordinary meaning. Based on our analysis above, we determine that a person of ordinary skill in the art reviewing the ’588 patent would understand that the “mapping” limitation requires (1) frequencies mapped to frequencies and (2) that a mapping is an association of one value to a corresponding value such that knowing the graphics frequency means that you know the corresponding interconnect frequency. Further, given that the corresponding frequencies are “selectable,” we understand that to mean that there is a set of possible frequencies that are defined from which to select. Ex. 2001, 21:19–22:2. With this understanding, we can turn to the dispute over whether the prior art teaches the limitations set forth in claims 5 and 12, as no other terms require construction at this time. *Realtime, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms. . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

*D. Asserted Obviousness Over White and Shakkarwar
(Claims 5, 6, 12, and 13)*

Petitioner asserts that claims 5, 6, 12, and 13 would have been obvious in view of White and Shakkarwar. Pet. 49–61. The present dispute between the parties can be resolved by an analysis of claim 5; we focus our analysis on that claim. Claim 5 ultimately depends from independent claim 1, and adds that certain power management circuitry “includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.” Ex. 1001, 8:62–65.

1. The Parties’ Positions

Petitioner’s ground relies on White to teach the power management circuitry, the graphics processing circuitry, and the interconnect, then relies on Shakkarwar to teach the mapping limitation. Pet. 49–53. Petitioner cites to a passage in Shakkarwar that states, “a lookup table may include a list of clock speeds, and/or voltage levels required to process information for specific devices and/or groups of devices.” Ex. 1006, 7:7–10 (cited at Pet. 51). The look-up table provides the bandwidth requirements for each device, so that each active component’s bandwidth requirement is identified and added up to provide a total bandwidth requirement. *Id.* at 7:10–17. Petitioner asserts that this look-up table teaches the claimed mapping. Pet. 53 (citing Ex. 1003 ¶ 140). Petitioner asserts that including the look-up table of Shakkarwar in White would “improve responsiveness and increase the ability of the system to respond to dynamically changing conditions.” *Id.* (citing Ex. 1003 ¶ 141).

Patent Owner argues in its Response that “Shakkarwar does not associate, by way of a look-up table or otherwise, particular GPU

frequencies with particular bus frequencies.” PO Resp. 20. Patent Owner disputes that the look-up table in Shakkarwar has any mapping because, according to Patent Owner, it is just a list of clock speeds for specific devices. *Id.* (citing Ex. 2002 ¶ 43); *see also id.* at 19–22 (entire argument).

Petitioner argues in its reply that Shakkarwar teaches to increase the bus (interconnect) frequency as a consequence of increasing the graphic circuitry’s frequency, and that “[t]his association between corresponding frequencies is a ‘mapping.’” Pet. Reply 5; *see also id.* at 2–8 (entire argument).

Patent Owner’s Sur-reply largely mirrors its Response, arguing that Shakkarwar has “no association—no *mapping*—of frequencies-to-frequencies as demanded by the challenged claims.” Sur-reply 1; *see also id.* at 1–7 (entire argument).

2. Analysis

Reviewing the arguments and evidence presented to us, we determine that Petitioner has not shown sufficiently that Shakkarwar teaches the claimed mapping limitation, for the following reasons. The lookup table in Shakkarwar has a list of clock speeds (frequencies) for specific devices. Ex. 1006, 7:7–10. These clock speeds represent the bandwidth needs of each individual device. *Id.* at 7:10–13. By looking up the bandwidth needs of each individual device in use, the system can determine the total bandwidth need. *Id.* at 7:5–17. For example, if one device requires 20 Megabits of data and the second device requires 10 Megabits of data, then the data rate (bandwidth) required will be 30 Megabits of data. *Id.* at 7:13–17. If the required bandwidth is different from the current bandwidth, then the current bandwidth must be modified. *Id.* at 7:18–26.

Given this disclosure, we agree with the testimony of Patent Owner's expert that Shakkarwar's empirical calculation, by looking up the frequencies of various devices and summing them up, is not the claimed mapping of frequencies to frequencies. Ex. 2002 ¶ 44 (citing Ex. 1006, 6:8–16, 6:49–7:17). That is, rather than teaching the use of the graphics device frequency get a corresponding interconnect frequency, Shakkarwar calculates the interconnect frequency by adding up the frequencies of all of the devices using the interconnect. Ex. 1006, 6:63–7:30; Ex. 2002 ¶ 44 (“Considerations of the hardware are addressed through empirical calculation, by knowing the requested data bandwidth of each device.”). Based on the above, we find that Shakkarwar's table does not map a set of frequencies to a set of frequencies, and we find that the alleged mapping in Shakkarwar is not what is required by the claim because knowing the non-core device frequency in Shakkarwar is insufficient to know the required interconnect frequency. Thus, we credit the testimony of Patent Owner's expert that Shakkarwar does not teach the claimed mapping. Ex. 2002 ¶¶ 42–45. On the other hand, the testimony of Petitioner's expert is conclusory on this point, and fails to grapple with these differences between the claims and prior art. Ex. 1003 ¶ 140. Thus, we credit the testimony of Patent Owner's expert over Petitioner's expert as to the teachings of Shakkarwar.

We acknowledge Petitioner's position that in some way the non-core device frequency is associated with the interconnect frequency, in that the calculated interconnect frequency value is based at least in part on the non-core device frequency input value. *See, e.g.*, Pet. 50–53; Pet. Reply 2–6. However, as we discussed in our claim construction section, claim 5 requires

a mapping, i.e., an association of a value to a corresponding value, and specifically of a frequency to a frequency. *See, e.g.*, Ex. 1001, 2:46–47 (“the table can map non-core domain frequency to a minimum interconnect frequency”). Adding up frequencies does not *map* a set of frequencies *to* another set of frequencies; it is an empirical calculation. Ex. 2002 ¶ 44. The calculation means that there are no “selectable frequencies” of non-core devices being mapped to “selectable frequencies” of the interconnect. If one uses Shakkarwar’s table to look up a graphics processor frequency, one does not determine the appropriate interconnect frequency because one must also figure out all of the other devices that are operating and consider their frequencies. Because one cannot know the interconnect frequency based on a corresponding non-core device frequency, there is no mapping of non-core frequency to interconnect frequency. *See id.*; *see also* Ex. 1006, 7:10–13 (stating that “bandwidth requirements . . . may be empirically calculated by knowing the required data bandwidth of each device”); *but see* Ex. 1001, 5:2–5 (the device “can access the table based on a frequency at which the non-core domain is operating to obtain the corresponding target interconnect frequency”). In sum, that Shakkarwar uses one or more non-core frequencies *when calculating* an interconnect frequency does not mean it *maps* non-core frequencies to interconnect frequencies.

Similarly, we acknowledge Petitioner’s position that Shakkarwar uses a look-up table, and so does the example embodiment of the ’588 patent. *See, e.g.*, Pet. 51–52; Ex. 1001, 5:15–35 (Table 1, having the columns “Non-Core Frequency” and “Minimum Interconnect Frequency”); Ex. 1006, 7:7–10 (“a look-up table . . . of clock speeds . . . for specific devices”). However, the Shakkarwar look-up table provides a list of devices and their

corresponding frequencies. The look-up table is used by looking up each device in use to find its required frequency, and then summing the required frequencies for each device in use. Ex. 1006, 7:5–26. In this way, it maps a set of *devices* to a set of *frequencies*, and then requires a further summation operation because all devices must be considered in order to figure out an interconnect frequency. On the other hand, the '588 patent's look-up table provides a list of non-core frequencies and corresponding interconnect frequencies. The look-up table is used by looking up the non-core frequency to find the appropriate minimum interconnect frequency to support that non-core frequency. Ex. 1001, 4:57–61, 4:66–5:7. In this way, it maps a set of *frequencies* to a set of *frequencies*. No further calculation is required because the answer (interconnect frequency) is mapped to the input (non-core frequency). Thus, the fact that Shakkarwar has a look-up table does not mean that it teaches or suggests the table described in the '588 patent, let alone the claimed mapping of frequencies to frequencies. It is a different table used in a different way. Ex. 2002 ¶¶ 42–45.³

In conclusion, we are not persuaded that Shakkarwar discloses the mapping required by claim 5. Petitioner's position for claims 6, 12, and 13 relies on its position for claim 5 (*see* Pet. 49, 53), and thus is similarly unpersuasive. Accordingly, we determine that Petitioner has not shown by

³ This is one reason why Petitioner's attempts to characterize Patent Owner's expert's testimony as supporting Petitioner's position are unpersuasive. Reply 8 (citing Ex. 1013, 51:1–9, 52:15–53:14). Even if Shakkarwar's look-up table lists various device frequencies, the table does not associate frequencies of devices with frequencies of the interconnect as claimed. Ex. 1013, 54:8 (Patent Owner's expert concluding that "there's no mapping going on [in Shakkarwar's table]").

a preponderance of the evidence that the subject matter of claims 5, 6, 12, and 13 would have been obvious at the time of invention in view of White and Shakkarwar.

*E. Asserted Obviousness Over Nussbaum and Shakkarwar
(Claims 5, 6, 12, and 13)*

Petitioner's Nussbaum and Shakkarwar ground relies on the same position that we found unpersuasive regarding White and Shakkarwar. Pet. 85–89. Accordingly, for similar reasons, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claims 5, 6, 12, and 13 would have been obvious at the time of invention in view of Nussbaum and Shakkarwar.

F. Remaining Grounds

Patent Owner does not contest the grounds challenging claims 1–4, 7–11, and 14–20. Tr. 60:8–13 (Patent Owner's counsel acknowledging that they did not argue these claims and instead rely on Petitioner's burden to demonstrate unpatentability). Petitioner has addressed each limitation of claims 1–4, 7–11, and 14–20 challenged in the White anticipation/obviousness ground (Pet. 19–49) and the Nussbaum anticipation/obviousness ground (*id.* at 61–84). Both grounds are supported by unrebutted expert testimony. *See* Ex. 1003 ¶¶ 22–63 (White), ¶¶ 76–100 (Nussbaum). We deem any argument Patent Owner has not raised to challenge Petitioner's remaining grounds to have been forfeited, and every material fact not specifically denied to have been admitted. *See also* 37 C.F.R. § 42.23(a) (in a reply, “[a]ny material fact not specifically denied may be considered admitted”); Paper 8, 9 (Scheduling Order) (“Patent

Owner is cautioned that any arguments not raised in the response may be deemed waived”).

We have reviewed Petitioner’s positions and the evidence cited therein, and find them persuasive. Independent claim 1 requires a processor having at least two cores, a graphics processing circuitry, and an interconnect, each operating at a different frequency. As Petitioner explains, White teaches all four of these components operable at independent frequencies. Pet. 19–32 (citing, e.g., Ex. 1005, 6:42–46 (“logic cores 120A and 120B each of which may be configured to operate at an independent voltage and frequency”), 24:50–54 (“graphics controller 1108 may include one or more multi-core integrated circuits and each logic core within such an integrated circuit may be configured to operate at independent frequencies and/or voltages”), 2:65–67 (the bridge, or interconnect, can “operate at a frequency and voltage different from any particular voltage or frequency at which the individual logic cores may be currently operating”)). Independent claims 8 and 20 recite similar language as independent claim 1. Pet. 32 (“there are no substantive differences between Claim 1 and Claim 8”), 35 (“The ‘functions’ recited in Claim 20 are the same as those recited in Claim 1.”).

We turn briefly to the dependent claims. Dependent claims 2 and 9 state that power management circuitry or logic causes the cores to operate independently. Petitioner explains how White teaches this. Pet. 38 (citing, e.g., Ex. 1005, 24:41–46 (“power management logic and/or temperature control logic both of which may be configured to control or adjust the operating frequency and/or voltage for logic core(s) 120, and possible common bridge logic 110, according to various embodiments, and as

described herein”)); *see also id.* at 38–40 (entire argument). Dependent claims 3 and 10 state that there is a non-core power domain comprising a cache. Petitioner explains how White discloses an L2 cache. Pet. 40–41. Dependent claims 4 and 11 state that there is a second power management circuitry for the graphics processing circuitry. Petitioner explains how a person of ordinary skill in the art would understand that White’s power management and temperature control logic independently control the frequencies of the logic cores of the graphics controller. Pet. 42–44. Dependent claims 7 and 14 require power management circuitry to cause the non-core power domain to operate at a different frequency from the first and second cores. Petitioner explains how White discloses power management logic configured to supply higher frequencies to the common bridge (i.e., interconnect). Pet. 44–45. Dependent claims 15–19 involve interfaces to various I/O devices. Petitioner explains how White discloses a bus bridge to provide an interface to the PCI bus, and thus to various devices such as an audio card, the display, an input device, and the network communication device. Pet. 45–49.

Petitioner’s analysis involving Nussbaum is similarly complete. *See* Pet. 61–84.

We have reviewed both of these uncontested grounds and the admitted evidence cited therein, and adopt Petitioner’s analysis as our own. We determine that this uncontested analysis demonstrates that Petitioner has shown, by a preponderance of the evidence, that claims 1–4, 7–11, and 14–20 would have been obvious in view of, or anticipated by, White or Nussbaum.

III. CONCLUSION

For the reasons given above, we determine that Petitioner has established by a preponderance of the evidence that claims 1–4, 7–11, and 14–20 would have been obvious in view of, or anticipated by, White or Nussbaum, but has not established by a preponderance of the evidence that any of claims 5, 6, 12, and 13 would have been obvious in view of White in view of Shakkarwar or Nussbaum in view of Shakkarwar.

The following table summarizes the outcome of this proceeding:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–4, 7–11, 14–20	102	White	1–4, 7–11, 14–20	
1–4, 7–11, 14–20	103	White	1–4, 7–11, 14–20	
5, 6, 12, 13	103	White, Shakkarwar		5, 6, 12, 13
1–4, 7–11, 14–20	102	Nussbaum	1–4, 7–11, 14–20	
1–4, 7–11, 14–20	103	Nussbaum	1–4, 7–11, 14–20	
5, 6, 12, 13	103	Nussbaum, Shakkarwar		5, 6, 12, 13
Overall Outcome			1–4, 7–11, 14–20	5, 6, 12, 13

IV. ORDER⁴

In consideration of the foregoing, it is hereby

ORDERED that the record shows that Petitioner has *not* established the unpatentability of claims 5, 6, 12, and 13 over White and Shakkarwar or Nussbaum and Shakkarwar;

FURTHER ORDERED that the record shows that Petitioner has established the unpatentability of claims 1–4, 7–11, and 14–20 over White or Nussbaum; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

⁴ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding after the issuance of this Final Written Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), (b)(2).

IPR2023-01345
Patent 10,705,588 B2

FOR PETITIONER:

Celine Crowson
Joe Raffetto
Scott Hughes
Helen Trac
Ryan Stephenson
Nicholas Rotz
HOGAN LOVELLS US LLP
celine.crowson@hoganlovells.com
joseph.raffetto@hoganlovells.com
scott.hughes@hoganlovells.com
helen.trac@hoganlovells.com
ryan.stephenson@hoganlovells.com
nicholas.rotz@hoganlovells.com

FOR PATENT OWNER:

Tarek Fahmi
Jonathan Tsao
ASCENDA LAW GROUP, PC
tarek.fahmi@ascendalaw.com
jonathan.tsao@ascendalaw.com