

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Mercedes-Benz USA, LLC,  
Petitioner,

v.

Daedalus Prime LLC,  
Patent Owner.

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Case No. IPR2023-01345  
U.S. Patent No. 10,705,588

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**PETITIONER'S REQUEST FOR DIRECTOR REVIEW**

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Filed on behalf of Petitioner:  
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## **I. INTRODUCTION**

Pursuant to 37 C.F.R. § 42.75, Petitioner Mercedes-Benz USA, LLC respectfully requests Director Review regarding the finding in the Final Written Decision (“**FWD**”) that claims 5, 6, 12, and 13 of U.S. Patent No. 10,705,588 (the “**588**”) were not shown to be unpatentable. The Board’s decision is based on erroneous findings of material fact and conclusions of law. In particular, the Board erred in finding that Shakkarwar (EX1006) does not disclose a “mapping” of selectable frequencies of graphics processing circuitry to selectable frequencies of an interconnect, as recited in claims 5 and 12, by improperly narrowing the scope of this term in a way not supported by the specification or claims (FWD, 10-13), and by improperly discounting disclosures in Shakkarwar regarding the association, or mapping, of frequencies of components. (FWD, 15-19.) For these reasons, Petitioner respectfully requests Director Review or rehearing by a Delegated Review Panel, and that Board’s FWD be vacated, reversed, or remanded as appropriate.

## **II. ARGUMENT**

### **A. Legal Standard**

Under the USPTO’s procedures, the Director may review any Final Written Decision presenting “(a) an abuse of discretion, (b) important issues of law or

policy, (c) erroneous findings of material fact, or (d) erroneous conclusions of law. USPTO Website, Revised Interim Director Review Process. 37 C.F.R. §§ 42.71(d), 42.75(a).

**B. The Board Erroneously Found Shakkarwar Does Not Disclose a “Mapping” of Graphics Processing Circuitry Frequencies to Interconnect Frequencies, as Required by Claims 5 and 12**

In its FWD, the Board concluded that Petitioner failed to prove claim 5-6 and 12-13 are unpatentable over White and Shakkarwar because Shakkarwar allegedly does not teach a “mapping of selectable frequencies of the graphics processing circuitry to a selectable frequencies of the interconnect”. (FWD, 18-19.) For the same reason, the Board concluded that Petitioner failed to prove claims 5-6 and 12-13 were unpatentable over the reference Nussbaum in combination with Shakkarwar. (*Id.*, 19.) In reaching its decision, the Board took an unduly narrow understanding as to how a person of ordinary skill would have understood “mapping” as recited in the claims, appearing to require a one-to-one association of graphics processing circuitry frequency to interconnect frequency as presented in the Table 1 mapping table. (FWD, 10-13)

The Board construed “mapping” to require (1) “frequencies mapped to frequencies” and (2) “that a mapping is an association of one value to a corresponding value such that knowing the graphics frequency means that you know

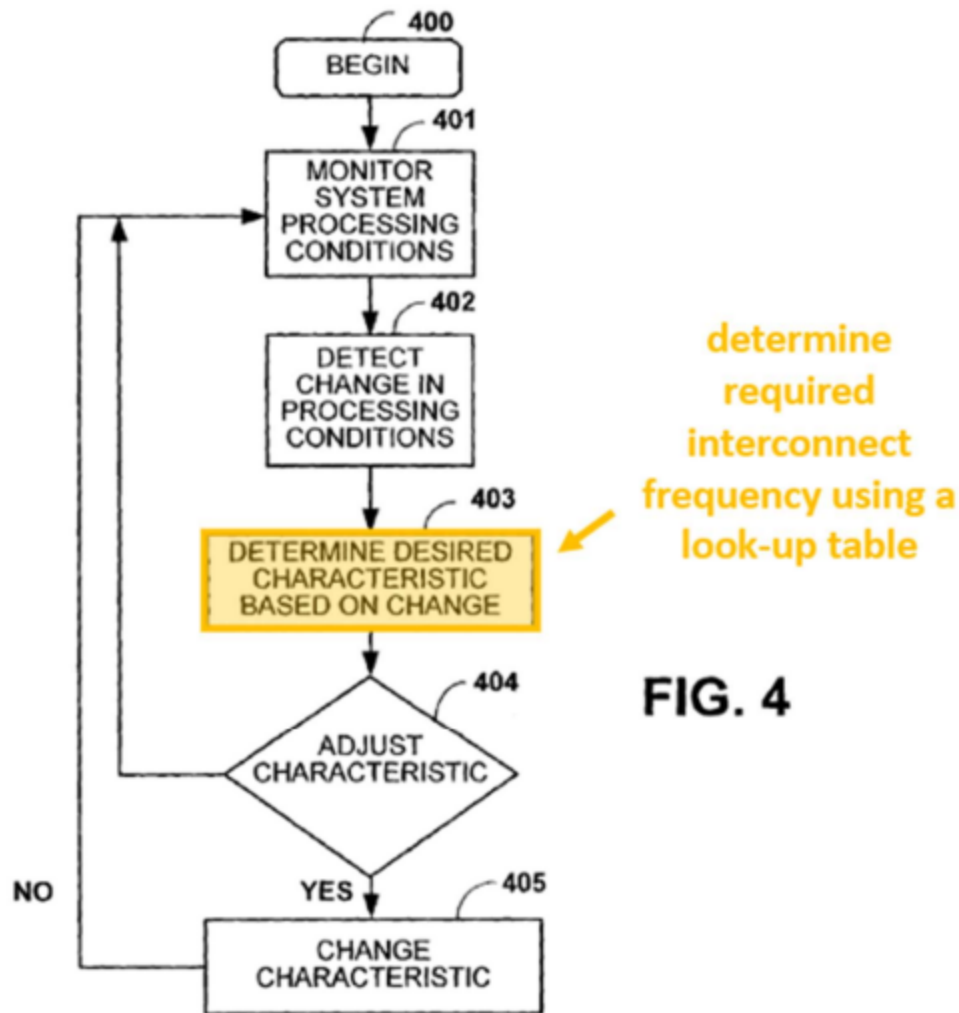
the corresponding interconnect frequency.” (FWD, 13.) The Board’s construction improperly limits the scope of this term to the specific, exemplary “mapping table” described in the ’588 Patent as just one way in which the “mapping” can be done, as it finds that the claimed “mapping” must have the same one-to-one association of a particular non-core frequency value to a specific interconnect frequency value as shown in Table 1 of the ’588 Patent. (FWD, 10-13; ’588 Patent 5:15-35.) However, the claims recite “mapping” generally—not a “mapping table”—and do not require an association of one frequency value of a component to one frequency of an interconnect. Instead, the claims broadly recite a “mapping” in general, something that the ’588 Patent describes as simply “a mechanism that maps non-core domain frequency to a corresponding interconnect frequency,” and that is an “association” of frequency values, but not specifically a one-to-one association of one specific value to another as the Board appears to require. (’588, 2:26-46, 4:57-61, 5:5-35; Pet. Reply, 4; Pet., 50-53; EX1003, ¶¶137-140.) The ’588 Patent even expressly states that the claimed mapping “*can* be maintained in a table, (’588, 2:30-32 (emphasis added), Pet. Reply, 4), and that Table 1 is just an “example” of how mapping can be performed. (’588, 2:26-46, 4:57-61, 5:5-35; Pet. Reply, 4; Pet., 50-53; EX1003, ¶¶137-140.) Further, the ’588 Patent notes that, when a table is used, the entries can “associate frequencies by ratios, offsets or so forth,” indicating the “mapping” does not need to be expressly one frequency to another as the Board

required. ('588 4:57-63.) Properly construed, “mapping” merely requires making any association between the frequencies. (Reply, 4; Pet., 50-53; EX1003, ¶¶137-140.) Shakkarwar teaches precisely this.

For example, Shakkarwar discloses selecting clock levels (*i.e.*, frequencies) for components including graphics controller 304 (*i.e.*, graphics processing circuitry) and a communication bus (*i.e.*, an interconnect). (Pet. at 49-59, 84-94; Pet. Reply, 5-6, n.2; Shakkarwar, Abstract, 2:51-58, 5:25-30.) Shakkarwar further discloses that, for example, “when an application that is known to use 3-D graphics is opened, system software can determine if the *bus rate between the data controller and the graphics controller* is high enough to support the graphics requirement.” (Shakkarwar, 6:49-52 (emphasis added).) In other words, when an application is opened, the graphics controller bandwidth requirements increase (*i.e.*, because it is operating at a higher frequency) and the bus frequency increases to accommodate the higher graphics controller bandwidth requirements. (Pet. Reply, 5; EX1003 ¶140.) Thus, when the graphics controller frequency increases, Shakkarwar teaches that the associated interconnect bus rate (frequency) is also determined based on the selected increased frequency of the graphics controller. (*Id.*)

Moreover, Shakkarwar discloses mapping selectable frequencies using a “look-up table” listing the clock speeds (*i.e.*, frequencies) required for devices to process a given amount of information. (Pet. Reply, 5-6; *see* Shakkarwar Abstract,

6:63-7:10; EX1003, ¶138.) These devices include the graphics controller 305 and data controller 302 (*i.e.*, an interconnect). (Pet. 51-53; Pet. Reply 4-6; Shakkarwar at Abstract, 2:24-39, 6:41-43, 49-52; EX1003, ¶¶137-138, 140, 145.) Shakkarwar specifically discloses determining bandwidth requirements for a data connection (*i.e.*, a bus or interconnect) based on the components active at a given time. (Pet. Reply, 5-6; *see* Shakkarwar 6:63-7:7; EX1003, ¶139.) The bandwidth requirements can depend on whether the graphics processing circuitry is being used (*i.e.*, has a nonzero bandwidth and frequency) or is inactive (*i.e.*, having an effective frequency of zero), and importantly any required bandwidth for the graphics processing circuitry is accounted for in the selected data connection bandwidth, making the two “associated with” or “mapped” to each other. (Pet. Reply, 6; *see* Shakkarwar, 6:59-62; *see also* 5:47-52.) That is, given the bandwidth (or frequency) requirements of graphics processing circuitry and other components, the look-up table is used to determine the associated interconnect frequency required. (Pet. Reply, 6; *see* EX1003, ¶139.) This process is shown in Figure 4 of Shakkarwar:



(Shakkarwar, Fig. 4 (annotated).) Stated differently, when graphics circuitry bandwidth (which is a function of frequency) changes, Shakkarwar uses a look-up table to determine the interconnect frequency required to accommodate this graphics circuitry bandwidth. (Reply, 4-6; EX1004, ¶¶138-42, n.4.) Thus, Shakkarwar teaches an association, or “mapping,” between the frequencies as claimed.

Using its improperly narrow interpretation of “mapping,” the Board incorrectly concludes that Shakkarwar cannot disclose this limitation because it determines the bandwidth of the data connection as a “sum” of the required frequencies or bandwidths of multiple components and thus is not simply an association of one frequency of the graphics processing circuitry to one frequency of an interconnect. (FWD, 15-19.) However, as noted above, the “association” of the claimed “mapping” is broader than this. And, Shakkarwar’s look-up table that associates the required interconnect frequency with at least the frequency required for the graphics processing circuitry meets the claim element, as the interconnect frequency selected is dependent upon, and therefore associated with, the frequency selected for the graphics circuitry. (Reply, 4-6; EX1004, ¶¶138-42, n.4.)

Further, even if Shakkarwar sums the required bandwidths for multiple active components using the look-up table and then calculates the interconnect bandwidth (or frequency) required, this is still an “association” of the frequency of the active graphics processing circuitry frequency to the interconnect bandwidth, even under the Board’s construction. This calculation expressly requires knowing the selected frequency for the graphics processing unit, and thus the frequency for the interconnect cannot be determined without it as the two are “associated.” (Pet.; 50-53, Pet. Reply, 2-6.) The Board even acknowledged this, stating that “[w]e acknowledge Petitioner’s position that in some way the non-core device frequency

is associated with the interconnect frequency, in that the calculated interconnect frequency value is based at least in part on the noncore device frequency input value.” (FWD, 16-17.) The direct association between the graphics processing circuitry frequency and the interconnect frequency is particularly apparent when that is the only active component whose required bandwidth changes – if the graphics circuitry frequency increases to require 10 more Megabits per second of interconnect bandwidth and no other component changes, then there is in fact a direct mapping as the interconnect bandwidth would need to increase by this exact 10 Megabits per second to account for the increased frequency of the graphics circuitry. (Shakkarwar, 7:5-17; Pet. 49-59, 84, Pet. Reply 4-8.) As Shakkarwar expressly discloses using a look-up table that directly correlates, or associates, the bandwidth of graphics circuitry with the bandwidth required for the interconnect, it discloses the claimed “mapping.”

### **III. CONCLUSION**

For the foregoing reasons, Petitioner respectfully requests Director Review or rehearing by the Delegated Review Panel to vacate the Board’s Decision and to reverse or remand as appropriate.

Dated: March 6, 2025

Respectfully submitted,

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**Certificate of Word Count**

The undersigned certifies, in accordance with 37 C.F.R. § 42.24(d), that the foregoing **PETITIONER’S REQUEST FOR DIRECTOR REVIEW** complies with the type-volume limitation of 15 pages, excluding the parts exempted by § 42.24(a)(1).

Dated: March 6, 2025

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**Certificate of Service**

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, the foregoing **PETITIONER’S REQUEST FOR DIRECTOR REVIEW** was served on March 6, 2025, electronically via e-mail upon the following parties:

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