UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/972,888	7356733	2113	9200

OC000000081543460

Correspondence Address/Fee Address Change

The following fields have been set to Customer Number 56436 on 03/18/2016

- **Correspondence Address**
- **Maintenance Fee Address**

The address of record for Customer Number 56436 is:

56436
Hewlett Packard Enterprise
3404 E. Harmony Road
Mail Stop 79
Fort Collins, CO 80528

PART 1 - ATTORNEY/APPLICANT COPY
page 1 of 1

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,356,733 B2
APPLICATION NO. : 10/972888
DATED : April 8, 2008
INVENTOR(S) : Scott L. Michaelis et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 11, line 45, delete "PAL_{13} MC_{13} RESUME" and insert -- PAL_MC_RESUME --, therefor.

In column 12, line 28, in Claim 1, insert -- , -- before "system".

Signed and Sealed this

Twenty-ninth Day of July, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	3392993
Application Number:	10972888
International Application Number:	
Confirmation Number:	1169
Title of Invention:	SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR
First Named Inventor/Applicant Name:	Scott L. Michaelis
Customer Number:	22879
Filer:	Kevin M. Hart/Marci Santillanes
Filer Authorized By:	Kevin M. Hart
Attorney Docket Number:	200404970-1
Receipt Date:	03-JUN-2008
Filing Date:	25-OCT-2004
Time Stamp:	09:52:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	200404970.pdf	472861 5d82442448d8e319068b8ed10371d3d5f9ed3df9	no	3

Warnings:

Information:

Total Files Size (in bytes):	472861

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: U.S. Patent No. 7,356,733

USPTO CONFIRMATION CODE: 1169

APPLICATION NO.: 10/972,888

FILED: Oct. 25, 2004

EXAMINER: Christopher McCarthy

GROUP ART UNIT: 2113

FOR: SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

ATTORNEY DOCKET NUMBER: 200404970-1

37 CFR 1.322 & 37 CFR 1.323 REQUEST FOR CERTIFICATE OF CORRECTION

HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS

Sir:

The following is a request for a certificate of correction in Serial Number 10/972,888, now Patent Number 7,356,733.

A certificate of correction under 35 USC 254 is respectfully requested in the above-identified patent.

☒ All errors were the fault of the USPTO, no fee required. In the event that a further fee is required, please charge the amount to Deposit Account No. 082025.

☐ All errors were the fault of the applicant and, accordingly, please charge **$100.00** to our Deposit Account No. 082025. In the event that a further fee is required, please charge the amount to the same Deposit Account.

☐ The errors were the fault of both the applicant and USPTO and, accordingly, please charge **$100.00** to our Deposit Account No. 082025. In the event that a further fee is required, please charge the amount to the same Deposit Account.

The exact locations where the errors appear in the patent and patent application are as follows:

In column 11, line 45, delete "PAL_{13} MC_{13} RESUME" and insert - - PAL_MC_RESUME - -, therefor.
(Amendment to specification filed on Oct. 11, 2007, page 4, line 14)

In column 12, line 28, in Claim 1, insert - - , - - before "system".
(Amendment to claims filed on Oct. 11, 2007, page 5, in Claim 19, line 3)

The requested corrections are attached on Form PTO 1050.

Respectfully Submitted

6/2/2008
DATE

Name:
Registration No.:

Attorney/Agent of Record

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,356,733

APPLICATION NO. : 10/972,888

ISSUE DATE : Apr. 08, 2008

INVENTOR(S) : Scott L. Michaelis, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 11, line 45, delete "PAL_{13} MC_{13} RESUME" and insert - - PAL_MC_RESUME - -, therefor.

In column 12, line 28, in Claim 1, insert - - , - - before "system".

MAILING ADDRESS OF SENDER (Please do not use customer number below):

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

This collection of information is required by 37 CFR 1.322, and 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Attention Certificate of Corrections Branch, Commissioner for Patent, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/972,888	04/08/2008	7356733	200404970-1	1169

22879 7590 03/19/2008
HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 570 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Scott L. Michaelis, Plano, TX;
Anurupa Rajkumari, Round Rock, TX;
Sylvia K. Myer, Fort Collins, CO;
Richard D. Powers, Highland Village, TX;

OIPE
FEB 13 2008

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22879 7590 11/14/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

02/14/2008 FMETEKI2 00000016 082025 10972888

01 FC:1501 1440.00 DA
02 FC:1504 300.00 DA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Marci Santillanes (Depositor's name)
Marci Santillanes (Signature)
02-13-08 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/972,888	10/25/2004	Scott L. Michaelis	200404970-1	1169

TITLE OF INVENTION: SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	02/14/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
MCCARTHY, CHRISTOPHER S	2113	714-011000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363)
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 ____
2 ____
3 ____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Hewlett-Packard Development Company, L.P.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Houston, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies ____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 08-2025 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature: [signature] Date: 2/13/2008

Typed or printed name: Steven L. Webb Registration No. 44,392

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PAGE 1/2 * RCVD AT 2/13/2008 3:54:45 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/1 * DNIS:2732885 * CSID:9708987247 * DURATION (mm-ss):01-14

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22879 7590 11/14/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
MCCARTHY, CHRISTOPHER S

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/14/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/972,888	10/25/2004	Scott L. Michaelis	200404970-1	1169

TITLE OF INVENTION: SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	02/14/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22879 7590 11/14/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/972,888	10/25/2004	Scott L. Michaelis	200404970-1	1169

TITLE OF INVENTION: SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	02/14/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
MCCARTHY, CHRISTOPHER S	2113	714-011000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/972,888	10/25/2004	Scott L. Michaelis	200404970-1	1169

22879 7590 11/14/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
MCCARTHY, CHRISTOPHER S

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/14/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 570 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 570 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/972,888	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/11/07*.

2. ☒ The allowed claim(s) is/are *19-25,27-28 renumbered as 1-9*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

Christopher McCarthy
Examiner AU 2113

Issue Classification	Application/Control No. 10/972,888	Applicant(s)/Patent under Reexamination MICHAELIS ET AL.
	Examiner Christopher S. McCarthy	Art Unit 2113

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
714	12	G	06	F	11	/00					/
CROSS REFERENCES						/					/
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
714	11					/					/
712	31					/					/
						/					/
						/					/
						/					/

(Assistant Examiner) (Date)	Christopher McCarthy 11/9/07	Total Claims Allowed: 9
(Legal Instruments Examiner) (Date)	(Primary Examiner) (Date)	O.G. Print Claim(s) 1 / O.G. Print Fig. 1

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
1	19		49		79		109		139		169		199
2	20		50		80		110		140		170		200
3	21		51		81		111		141		171		201
4	22		52		82		112		142		172		202
5	23		53		83		113		143		173		203
6	24		54		84		114		144		174		204
7	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
8	28		58		88		118		148		178		208
9	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/972,888	MICHAELIS ET AL.
	Examiner	Art Unit
	Christopher S. McCarthy	2113

SEARCHED			
Class	Subclass	Date	Examiner
714	11-13	11/9/2007	CM
712	31	11/9/2007	CM

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
PGPUB	txt srch	11/9/2007	CM

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Search Updated	11/9/2007	CM
Inventor Name Search	11/9/2007	CM

Interference Search

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	3	(lockstep with loss with idl$4 with firmware).clm.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/11/09 11:16

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1484	714/11,12,13.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/11/09 11:13
L2	94	712/31.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/11/09 11:15
L3	94	712/31.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/11/09 11:15
L4	3	(lockstep with loss with idl$4 with firmware).clm.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/11/09 11:16
S1	710	714/11.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/11/09 10:59
S2	0	("2006/0107107").URPN.	USPAT	AND	ON	2007/07/02 10:38
S3	0	("2006/0107106").URPN.	USPAT	AND	ON	2007/07/02 10:38
S4	323	714/12.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 16:14
S5	580	714/13.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/03 12:42
S6	460	714/13.ccls. and (not 714/11,12.ccls.)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/03 11:03
S7	94	712/31.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/03 12:42
S8	0	("2007/0043972").URPN.	USPAT	AND	ON	2007/07/03 13:59
S9	24	("20040019771" | "20040153731" | "20040153857" | "4589066" | "4750177" | "5369749" | "5732209" | "5748873" | "5913059" | "6065135" | "6141718" | "6148348" | "6263452" | "6330661" | "6378021" | "6567839" | "6615366" | "6625749" | "6625756" | "6640313" | "6751749" | "6772368" | "6976155" | "7003691").PN. OR ("7155721").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 20:59
S10	9	("4750177" | "4849979" | "5157780" | "5428768" | "5434997" | "6065135" | "6249856" | "6279119").PN. OR ("7003691").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:09

EAST Search History

S11	25	("4438494" | "4503535" | "4823256" | "4916704" | "5138708" | "5226152" | "5233615" | "5249187" | "5249188" | "5255367" | "5313575" | "5339408" | "5353436" | "5640521").PN. OR ("5915082").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:10
S12	21	("20020073357" | "20020144177" | "20020152418" | "20020152420" | "20030005380" | "4785453" | "5226152" | "5276823" | "5434997" | "5764660" | "5948111" | "6065135" | "6247144" | "6393582" | "6473869" | "6604177" | "6615366" | "6625749" | "6751698" | "6820213" | "7055060"). PN. OR ("7237144").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:13
S13	27	("4751639" | "5799022" | "5903717" | "5923830").PN. OR ("6141770").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:15
S14	1	("2004/0078650").URPN.	USPAT	AND	ON	2007/07/03 21:18
S15	1	("2004/0006722").URPN.	USPAT	AND	ON	2007/07/03 21:19
S16	3	("2003/0051190").URPN.	USPAT	AND	ON	2007/07/03 21:19
S17	32	("4438494" | "4503535" | "4823256" | "4916704" | "5138708" | "5226152" | "5233615" | "5249187" | "5249188" | "5313575" | "5353436" | "5915082"). PN. OR ("6065135").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:19
S18	0	("2006/0248384").URPN.	USPAT	AND	ON	2007/07/03 21:22
S19	1	("2005/0246581").URPN.	USPAT	AND	ON	2007/07/03 21:22
S20	1	("2005/0240811").URPN.	USPAT	AND	ON	2007/07/03 21:22
S21	15	("20020073357" | "20020144177" | "20030126498" | "20040019771" | "20040153731" | "20040153857" | "4589066" | "5732209" | "6065135" | "6148348" | "6263452" | "6378021" | "6615366" | "6751749" | "6772368"). PN. OR ("7085959").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:22
S22	14	("5522029" | "5884019" | "5892898" | "5919266" | "6065078" | "6141770" | "6173386" | "6199179" | "6308285" | "6360333").PN. OR ("6675324").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:24
S23	39	("4181940" | "4634110" | "5155731" | "5247659" | "5408647" | "5418955"). PN. OR ("5491788").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:26
S24	0	("2006/0010344").URPN.	USPAT	AND	ON	2007/07/03 21:29
S25	33	("3898621" | "4907228" | "4954942" | "4984234" | "5005174" | "5136204" | "5255367" | "5278962").PN. OR ("5748873").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:29

EAST Search History

S26	143	("3252149" | "3303474" | "3395396" | "3409879" | "3444528" | "3503048" | "3786433" | "3810119" | "3931505" | "4198678").PN. OR ("4358823").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:31
S27	29	("4453215" | "4912707" | "5475856" | "5504859" | "5530802" | "5664214" | "5748873" | "6279119" | "6393582"). PN. OR ("6625749").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:35
S28	17	("20030167389" | "20040006722" | "20040078650" | "20040078651" | "20050149776" | "20050240810" | "20050240811" | "4453215" | "4553215" | "4912707" | "5475856" | "5504859" | "5530802" | "5664214" | "5748873" | "6279119" | "6393582"). PN. OR ("7134047").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:38
S29	7	("5761518" | "5978923").PN. OR ("6308285").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:39
S30	22	("5465360" | "5491788" | "5497497" | "5535395" | "5568641" | "5611078" | "5627962" | "5659748" | "5724527" | "5729675" | "5737604" | "5737615" | "5761518" | "5870602" | "6058475" | "6122735" | "6308285").PN. OR ("6496881").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:39
S31	18	("4679166" | "5327548" | "5448716" | "5450576" | "5491788" | "5495569" | "5659748" | "5724527" | "5860002"). PN. OR ("6058475").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:41
S32	18	("4888683" | "5450576" | "5491788" | "5627962" | "5659748" | "5729675" | "5768585").PN. OR ("6009521").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:42
S33	14	reestablish$4 with lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:35
S34	6	(("5675794") or ("6438687") or ("6920581")).PN.	US-PGPUB; USPAT; DERWENT	OR	OFF	2007/07/04 11:37
S35	11	(("5226152") or ("5249188") or ("5751932") or ("5758058") or ("5764660") or ("6065135") or ("6148348") or ("6473869") or ("6560682") or ("6604177") or ("6615366")).PN.	USPAT	OR	OFF	2007/07/04 11:42
S36	8	(("6625749") or ("6687851") or ("6754787") or ("20020144177") or ("20030070050") or ("20040006722") or ("20040019771") or ("20040153857")).PN.	US-PGPUB; USPAT	OR	OFF	2007/07/04 11:50

EAST Search History

S37	15	resynch$7 with lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:38
S38	13	lockstep with (reset$4 or resynch$8 or reestablish$5) with (operating adj system)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:41
S39	55	recover$4 with lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:47
S40	62	recover$4 with (lock adj step)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:48
S41	54	S40 and (not S39)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:48
S42	19	(lockstep or (lock adj step)) with boot	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:54
S43	24	(lockstep or (lock adj step)) with boot$4	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:55
S44	30	(lockstep or (lock adj step)) with idle$4	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:03
S45	225	(lockstep or (lock adj step)) and (boot with processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:03
S46	22	(lockstep or (lock adj step)) and (boot adj2 processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:05
S47	19	(lockstep or (lock adj step)) and (boot adj processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:05
S48	19	(lockstep or (lock adj step)) and (boot$4 adj processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:06
S49	2	("20050172164").PN.	US-PGPUB; USPAT; DERWENT	OR	OFF	2007/07/04 14:17
S50	20	lockstep with spare	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 14:18
S51	23	lockstep and (spare with (switch$4 or failover))	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:12

EAST Search History

S52	27	lockstep and (spare with (switch$4 or failover or replac$4))	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:13
S53	23	("4015246" | "4799140" | "4926281" | "4967347" | "5276823" | "5423024" | "5572620" | "5596756" | "5666483" | "5799198").PN. OR ("5923830").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/04 15:18
S54	373	(boot adj processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:25
S55	0	(boot adj processor) with failover	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:25
S56	7	(boot adj processor) with replac$4	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:32
S57	17	(boot adj processor) and lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:32
S58	139	714/11,12.ccls. and boot	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 16:14

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404970-1

Inventor(s): Scott L. Michaelis et al.

Confirmation No.: 1169

Application No.: 10/972,888

Examiner: C.S. McCarthy

Filing Date: October 25, 2004

Group Art Unit: 2113

Title: SYSTEM AND METHOD FOR SYSTEM FIREWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

Mail Stop Amendment
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Transmitted herewith is/are the following in the above-identified application:

- [X] Response/Amendment
- [ ] New fee as calculated below
- [X] No additional fee
- [ ] Other _____ Fee$_____
- [ ] Petition to extend time to respond
- [ ] Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	9	MINUS	38	= 0	X $50	$ 0
INDEP. CLAIMS	1	MINUS	5	= 0	X $200	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $360	$ 0
EXTENSION FEE	[ ] 1st Month $120	[ ] 2nd Month $450	[ ] 3rd Month $1020	[ ] 4th Month $1590		$ 0
OTHER FEES						$
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this document is being transmitted to the Patent and Trademark Office via eletronic filing.

Date of Transmission: October 11, 2007

Respectfully submitted,

Scott L. Michaelis et al.

By: Jody C. Bishop

Attorney/Agent for Applicant(s)

Reg No. : 44,034

Date : October 11, 2007

Telephone : (214) 855-8007

Rev 10/06a (E-TransAmd)

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Docket No.: 200404970-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Scott L. Michaelis et al.

Application No.: 10/972,888

Confirmation No.: 1169

Filed: October 25, 2004

Art Unit: 2113

For: SYSTEM AND METHOD FOR SYSTEM FIRWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

Examiner: C. S. McCarthy

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated July 18, 2007, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

AMENDMENTS TO THE SPECIFICATION

[0001] The present application is related to the following concurrently filed and commonly assigned U.S. Patent Applications: Serial No. ~~[Attorney Docket No. 200404944-1]~~ 10/973,077 titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. ~~[Attorney Docket No. 200404943-1]~~ 10/973,004 titled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"; Serial No. ~~[Attorney Docket No. 200404941-1]~~ 10/973,076 titled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION"; Serial No. ~~[Attorney Docket No. 200404973-1~~ 10/972,588 titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. ~~[Attorney Docket No. 200404971-1]~~ 10/973,003 titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"; Serial No. ~~[Attorney Docket No. 200404946-1]~~ 10/972,835 titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION"; Serial No. ~~[Attorney Docket No. 200404972-1]~~ 10/973,075 titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"; and Serial No. ~~[Attorney Docket No. 200404974-1]~~ 10/972,796 titled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR", the disclosures of which are hereby incorporated herein by reference.

[0019] As described further herein and in concurrently filed and commonly assigned U.S. Patent Application Serial No. ~~[Attorney Docket No. 200404941-1]~~ 10/973,076 titled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION," the disclosure of which is incorporated herein by reference,

certain techniques are provided for recovering from LOL detected for a processor module in a multi-processor system. In using these exemplary techniques, system firmware instructs the system's OS to idle the processor module for which LOL was detected. Control of the processor module is then returned to the system firmware so that the system firmware can take actions to attempt to recover the lockstep. If lockstep is successfully recovered, in certain implementations, the firmware triggers the OS to again recognize the processor module and begin scheduling instructions for it.

[0031] Exemplary techniques for recovering from a detected LOL that may be employed are described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. ~~[Attorney Docket No. 200404941-1]~~ 10/973,076 titled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION," the disclosure of which is incorporated herein by reference. Embodiments provided herein further discuss techniques for instructing a system's OS to idle a processor module for which LOL is detected. Embodiments provided herein do not require that the OS be implemented with processor-specific information to receive an instruction to idle the processor responsive to LOL being detected for the processor. That is, the OS is not required to be developed specifically for a certain processor architecture in order to receive an instruction from the system firmware to idle the processor. For instance, in certain embodiments, standard OS methods, such as ACPI methods, are used for instructing the OS to idle the processor. Thus, in certain embodiments, any ACPI-compatible OS can receive an instruction to idle the processor module in the manner described herein. Thus, in accordance with certain embodiments, an OS that is fully ACPI compliant can receive notification that a processor should have its use discontinued, responsive to detected LOL. Further, in certain implementations, the OS can keep using the disabled processor until it is convenient to eject the processor and return it to firmware control.

[0042] In operational block 303, SAL asserts a General Purpose Event Interrupt (GPE) by writing to the appropriate GPE register in the ACPI register space. This causes the OS to execute its interrupt handler, which will run an ACPI Machine Language (AML) Method associated with this particular interrupt. In this example, this AML method that is executed

responsive to the interrupt generated by the GPE includes an AML instruction called "Notify". This "Notify" operation indicates the CPU object that has lost lockstep (i.e., identifies which processor module lost its lockstep) and that an Eject is being requested as arguments. The AML instruction notifies the OS that action is being requested on this CPU. The AML method then returns and the OS can take action asynchronously to satisfy the notify request. Exemplary actions that can be taken to idle the processor module responsive to this request and then attempt to reestablish lockstep for the processor module are described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ ~~[Attorney Docket No. 200404971-1]~~ 10/973,003 titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED", the disclosure of which is hereby incorporated herein by reference.

[0044] The processor module, returns to normal execution without lockstep protection in operational block 305. That is, the processor module executes normally until the OS idles/ejects it. Before restoring the execution state and calling PAL_MC_RESUME, firmware evaluates the error that occurred. If there is any chance of data corruption propagating throughout the system, then the exemplary process of FIGURE 3 is not followed. For instance, if determined in block 101 of FIGURE 1 that the lockstep is not recoverable, then the system crashes in block 102. The exemplary operational flow of FIGURE 3 is performed in operational block 103 (of FIGURE 1) of this embodiment. Exemplary techniques for deciding whether to attempt to reestablish lockstep for the processor module (and thus whether to request that the OS idle the processor and in the meantime resume operation of the processor) are described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ ~~[Attorney Docket No. 200404946-1]~~ 10/972,835 titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION" and concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ ~~[Attorney Docket No. 200404971-1]~~ 10/973,003 titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED", the disclosures of which are hereby incorporated herein by reference.

AMENDMENTS TO THE CLAIMS

1-18. (Canceled)

19. (Currently Amended) A method comprising:

detecting loss of lockstep (LOL) for a processor module in a system; ~~and~~

responsive to said detecting LOL for the processor module, system firmware instructing the system's operating system to idle the processor module and return control over the processor module to the system firmware; and

continuing operation of the processor module without lockstep protection, while awaiting for the operating system to idle the processor module and return control over the processor module to the system firmware.

20. (Original) The method of claim 19 further comprising:

determining if the LOL is immediately fatal.

21. (Original) The method of claim 20 further comprising:

performing said continuing operation if determined that the LOL is not immediately fatal.

22. (Original) The method of claim 21 further comprising:

if determined that the LOL is immediately fatal, ceasing operation of the processor module.

23. (Original) The method of claim 19 further comprising:

determining if lockstep can be recovered for the processor module without shutting down the system's operating system.

24. (Original) The method of claim 23 further comprising:

performing said continuing operation if determined that lockstep can be recovered for the processor module without shutting down the system's operating system.

25. (Original) The method of claim 24 further comprising:

ceasing operation of the processor module if determined that lockstep cannot be recovered for the processor module without shutting down the system's operating system.

26. (Canceled)

27. (Canceled)

28. (Currently Amended) The method of ~~claim 27~~ claim 19 further comprising:

said operating system idling the processor module and returning control over the processor module to the system firmware.

29. (Original) The method of claim 28 further comprising:

said system firmware reestablishing lockstep for the processor module, wherein said operating system is not shut down for said reestablishing.

30-38. (Canceled)

REMARKS

Claims 1-38 were pending in the present application. Claims 1-26 and 30-38 are rejected and claims 27-29 are objected to in the current Office Action (mailed July 18, 2007). Claims 27-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Claims 1-18 and 30-38 are canceled herein, and thus the rejections raised for those claims are now moot.

Claim 19 is amended to include the elements of claims 26 and 27. Claim 26 originally depended from claim 19, and claim 27 depended from claim 26. Thus, claim 19 is amended to effectively re-write claim 27 in independent form. As such, claims 26 and 27 are canceled without prejudice herein. Claim 28 is amended to change its dependency from canceled claim 27 to claim 19.

Because claim 27 was indicated in the present Office Action as being allowable if rewritten in independent (which Applicant has done by this amendment), Applicant respectfully submits that the present application should be passed to allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 200404970-1 from which the undersigned is authorized to draw.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: October 11, 2007

Signature: Donna Forbit
(Donna Forbit)

Respectfully submitted,

By _____
Jody C. Bishop
Attorney/Agent for Applicant(s)
Reg. No. 44,034
Date: October 11, 2007
Telephone No. (214) 855-8007

Electronic Acknowledgement Receipt

EFS ID:	2309902
Application Number:	10972888
International Application Number:	
Confirmation Number:	1169
Title of Invention:	System and method for system firmware causing an operating system to idle a processor
First Named Inventor/Applicant Name:	Scott L. Michaelis
Customer Number:	22879
Filer:	David H. Tannenbaum/Donna Forbit
Filer Authorized By:	David H. Tannenbaum
Attorney Docket Number:	200404970-1
Receipt Date:	11-OCT-2007
Filing Date:	25-OCT-2004
Time Stamp:	17:41:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		P899.pdf	452055 96f5584364e35f8ebc38a65e5e193245c6d08b4a	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment - After Non-Final Rejection	1	2
	Specification	3	5
	Claims	6	7
	Applicant Arguments/Remarks Made in an Amendment	8	8

Warnings:	
Information:	
Total Files Size (in bytes):	452055

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/972,888	10/25/2004	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/11/2007	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 9	Minus	** 38	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***5	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Dorian P. Evans/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

MN

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/972,888	10/25/2004	Scott L. Michaelis	200404970-1	1169

22879 7590 07/18/2007
HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
MCCARTHY, CHRISTOPHER S

ART UNIT	PAPER NUMBER
2113	

MAIL DATE	DELIVERY MODE
07/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/972,888	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 October 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 and 30-38 is/are rejected.

7)☒ Claim(s) 27-29 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 October 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/25/04.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 14 and 24 of U.S. Patent Application 10/973,003 contains every element of claims 1, 8 and 1, 2, respectively of the instant application and as such anticipates claims 1, 2, 8 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-18, 30-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Bigbee et al. U.S. Patent 6,920,581.

As per claim 1, Bigbee teaches a method comprising: system firmware instructing a system's operating system to idle a processor; and responsive to said instructing, said operating system idling the processor and returning control over the processor to the system firmware (column 4, lines 39-65).

As per claim 2, Bigbee teaches the method of claim 1 wherein said instructing comprises: using an Advanced Configuration and Power Interface (ACPI) method to instruct the operating system to idle the processor (column 3, lines 17-30).

As per claim 3, Bigbee teaches the method of claim 2 wherein said ACPI method is an ACPI eject method (column 8, lines 5-11).

As per claim 4, Bigbee teaches the method of claim 1 wherein said instructing comprises: generating an interrupt (column 4, lines 14-20).

As per claim 5, Bigbee teaches the method of claim 4 wherein said generating said interrupt comprises: said system firmware writing to a general purpose execution (GPE) register (column 3, lines 30-34).

As per claim 6, Bigbee teaches the method of claim 4 further comprising: executing an Advanced Configuration and Power Interface Machine Language (AML) method associated with the generated interrupt (column 3, lines 27-30).

As per claim 7, Bigbee teaches the method of claim 6 wherein said executing said AML method comprises: requesting said operating system to eject said processor module (column 4, lines 55-65).

As per claim 8, Bigbee teaches the method of claim 1 wherein said system firmware instructs the system's operating system to idle the processor responsive to detection of loss of lockstep for the processor (column 1, lines 25-35).

As per claim 9, Bigbee teaches he method of claim 8 further comprising: responsive to said operating system returning control over the processor to the system firmware, the system firmware reestablishing lockstep for the processor (column 4, line 65 – column 5, line 12).

As per claim 10, Bigbee teaches the method of claim 9 wherein said system firmware reestablishes lockstep for the processor without shutting down the operating system (column 4, line 65 – column 5, line 12).

As per claim 11, Bigbee teaches a method comprising: detecting loss of lockstep (LOL) for a processor module in a system; and responsive to said detecting LOL for the processor module, system firmware instructing an operating system to idle the processor module (column 1, lines 16-34; column 4, lines 39-65).

As per claim 12, Bigbee teaches the method of claim 11 further comprising: responsive to said instructing, said operating system idling the processor module (column 4, lines 55-65).

As per claim 13, Bigbee teaches the method of claim 12 further comprising: the operating system returning control over the idled processor module to the system firmware (column 4, line 66- column 5, line 12).

As per claim 14, Bigbee teaches the method of claim 13 further comprising: the system firmware reestablishing lockstep for the processor module without shutting down the operating system (column 4, lines 66 – column 5, line 12).

As per claim 15, Bigbee teaches the method of claim 11 wherein said instructing comprises: generating an interrupt (column 3, lines 27-30).

As per claim 16, Bigbee teaches the method of claim 15 wherein said generating said interrupt comprises: writing to a general purpose execution (GPE) register (column 3, lines 30-34).

As per claim 17, Bigbee teaches the method of claim 15 wherein said operating system is Advanced Configuration and Power Interface (ACPI) compatible, further comprising: executing an ACPI Machine Language (AML) method associated with the generated interrupt (column 3, lines 27-30).

As per claim 18, Bigbee teaches the method of claim 17 wherein said executing said AML method comprises: requesting said operating system to eject said processor module (column 4, liens 55-65).

As per claim 30, Bigbee teaches system comprising: a processor; an operating system for scheduling operations for the processor; and system firmware operable to request that said operating system idle the processor (column 3, lines 66-67, 17-30, 3-17).

As per claim 31, Bigbee teaches the system of claim 30 wherein said operating system is operable, responsive to said system firmware requesting that said operating system idle the processor, to idle the processor and return control over the processor to the system firmware (column 4, lines 39-65).

As per claim 32, Bigbee teaches the system of claim 31 wherein said system firmware is operable, responsive to detection of loss of lockstep (LOL) for the processor, to request that said operating system idle the processor (column 4, lines 39-.65)

As per claim 33, Bigbee teaches the system of claim 32 wherein said system firmware is operable, responsive to receiving said control over the processor, to reestablish lockstep for the processor (column 4, line 65 – column 5, line 12).

As per claim 34, Bigbee teaches the system of claim 30 wherein said system firmware is operable, responsive to detection of loss of lockstep (LOL) for the processor, to request that said operating system idle the processor (column 4, lines 39-65).

As per claim 35, Bigbee teaches the system of claim 30 wherein said processor is an Itanium Processor Family (IPF) processor (column 7, lines 24-25).

As per claim 36, Bigbee teaches the system of claim 30 wherein said system firmware uses an Advanced Configuration and Power Interface (ACPI) method to request that said operating system idle the processor (column 3, lines 17-30).

As per claim 37, Bigbee teaches a system comprising: means for detecting loss of lockstep (LOL) for a processor module in a system; and system firmware including means, responsive to said detecting LOL for the processor module, for instructing an operating system to idle the processor module (column 4, lines 39-65).

As per claim 38, Bigbee teaches the system of claim 37 wherein responsive to the instructing means instructing the operating system to idle the processor module, the operating system idling the processor module and returning control over the processor module to the system firmware (column 4, lines 39-67).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 10-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Marshall et al U.S. Patent 5,915,082.

As per claim 19, Marshall teaches a method comprising: detecting loss of lockstep (LOL) for a processor module in a system; and continuing operation of the processor module without lockstep protection (column 5, lines 46-50).

As per claim 20, Marshall teaches he method of claim 19 further comprising: determining if the LOL is immediately fatal (column 5, line 66 – column 6, line 3).

As per claim 21, Marshall teaches the method of claim 20 further comprising: performing said continuing operation if determined that the LOL is not immediately fatal (column 5, lines 28-67).

As per claim 22, Marshall teaches the method of claim 21 further comprising: if determined that the LOL is immediately fatal, ceasing operation of the processor module (column 5, line 65 – column 6, line 28).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 23 –25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marshall in view of Quach U.S. Patent 6,625,749.

As per claim 23, Marshall teaches the method of claim 19. Marshall does not teach further comprising: determining if lockstep can be recovered for the processor module without shutting down the system's operating system. Quach does teach the recovery to comprise determining whether to attempt to reestablish lockstep for the processor module (column 9, lines 15-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the recovery process of Quach to the recovery process of Marshall. One of ordinary skill in the art would have been motivated to combine the recovery process of Quach to the recovery process of Marshall because Quach teaches the recovery of a discrepancy of parity

between two redundant processors (column 1, lines 33-48); an explicit desire of Marshall (column 4, lines 41-58).

As per claim 24, Marshall in view of Quach teaches the method of claim 23. Quach teaches further comprising: performing said continuing operation if determined that lockstep can be recovered for the processor module without shutting down the system's operating system (column 9, lines 15-21).

As per claim 24, Marshall in view of Quach teaches the method of claim 24. Marshall teaches further comprising: ceasing operation of the processor module if determined that lockstep cannot be recovered for the processor module without shutting down the system's operating system (column 5, line 65 – column 6, line 28).

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marshall in view of Bigbee.

As per claim 26, Marshall teaches the method of claim 19. Marshall does not teach further comprising: responsive to said detecting LOL for the processor module, system firmware instructing the system's operating system to idle the processor module and return control over the processor module to the system firmware. Bigbee does teach responsive to said detecting LOL for the processor module, system firmware instructing the system's operating system to idle the processor module and return control over the processor module to the system firmware (column 4, lines 39-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the process of Bigbee to the process of Marshall. One of ordinary skill in the art would have been motivated to combine the process of Bigbee to the

process of Marshall because Bigbee teaches the recovery in a system when lockstep is lost (column 4, lines 1-14); an explicit desire of Marshall (column 1, lines 10-19).

Allowable Subject Matter

9. Claims 27-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher S. McCarthy
Examiner
Art Unit 2113

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404970-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
/CM/	1A	5,226,152	07/06/1993	Klug et al.	
	1B	5,249,188	09/28/1993	McDonald	
	1C	5,751,932	05/12/1998	Horst et al.	
	1D	5,758,058	05/26/1998	Milburn	
	1E	5,764,660	06/09/1998	Mohat	
	1F	6,065,135	05/16/2000	Marshall et al.	
	1G	6,148,348	11/14/2000	Garnett et al.	
	1H	6,473,869	10/29/2002	Bissett et al.	
	1I	6,560,682	05/06/2003	Miller et al.	
	1J	6,604,177	08/05/2003	Kondo et al.	
	1K	6,615,366	09/02/2003	Grochowski et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

/CM/	1Q	Attorney Docket No. 200404974-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR"
/CM/	1R	Attorney Docket No. 200404944-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
/CM/	1S	Attorney Docket No. 200404946-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION"

EXAMINER	DATE CONSIDERED
/Christopher Mccarthy/	07/11/2007

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200404970-1	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Scott L. Michaelis et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
/CM/	2A	6,625,749	09/23/2003	Quach	
	2B	6,687,851	02/03/2004	Somers et al.	
	2C	6,754,787	06/22/2004	Miller et al.	
	2D	2002/0144177	10/03/2002	Kondo et al.	
	2E	2003/0070050	04/10/2003	Miller et al.	
	2F	2004/0006722	01/08/2004	Safford	
	2G	2004/0019771	01/29/2004	Quach	
	2H	2004/0153857	08/05/2004	Yamazaki et al.	
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

/CM/	2Q	Attorney Docket No. 200404941-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION"
/CM/	2R	Attorney Docket No. 200404943-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PRCESSOR MODULE"
/CM/	2S	Attorney Docket No. 200404971-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"

EXAMINER	DATE CONSIDERED
/Christopher Mccarthy/	07/11/2007

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200404970-1	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Scott L. Michaelis et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

/CM/	3Q	Attorney Docket No. 200404972-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"
/CM/	3R	Attorney Docket No. 200404973-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
	3S	

EXAMINER	DATE CONSIDERED
/Christopher Mccarthy/	07/11/2007

Rev 05/04 (PTO1449)

Notice of References Cited	Application/Control No. 10/972,888	Applicant(s)/Patent Under Reexamination MICHAELIS ET AL.	
	Examiner Christopher S. McCarthy	Art Unit 2113	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,915,082 A	06-1999	Marshall et al.	714/11
*	B	US-2002/0152420 A1	10-2002	Chaudhry et al.	714/11
*	C	US-2003/0051190 A1	03-2003	MARISETTY et al.	714/11
*	D	US-2003/0126498 A1	07-2003	Bigbee et al.	714/10
*	E	US-6,604,177 B1	08-2003	Kondo et al.	711/150
*	F	US-6,625,749 B1	09-2003	Quach, Nhon	714/10
*	G	US-2004/0006722 A1	01-2004	Safford, Kevin David	714/11
*	H	US-2004/0078650 A1	04-2004	Safford et al.	714/011
*	I	US-2004/0078651 A1	04-2004	Safford et al.	714/011
*	J	US-6,920,581 B2	07-2005	Bigbee et al.	714/10
*	K	US-7,003,691 B2	02-2006	Safford et al.	714/11
*	L	US-7,085,959 B2	08-2006	Safford, Kevin David	714/11
*	M	US-7,155,721 B2	12-2006	Safford et al.	718/104

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/972,888	Applicant(s)/Patent Under Reexamination MICHAELIS ET AL.	
	Examiner Christopher S. McCarthy	Art Unit 2113	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,675,324 B2	01-2004	Marisetty et al.	714/30
*	B	US-2004/0019771 A1	01-2004	Quach, Nhon	712/229
*	C	US-7,134,047 B2	11-2006	Quach, Nhon	714/11
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/972,888	MICHAELIS ET AL.
	Examiner	Art Unit
	Christopher S. McCarthy	2113

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	7/11/07								
	1	v								
	2	v								
	3	v								
	4	v								
	5	v								
	6	v								
	7	v								
	8	v								
	9	v								
	10	v								
	11	v								
	12	v								
	13	v								
	14	v								
	15	v								
	16	v								
	17	v								
	18	v								
	19	v								
	20	v								
	21	v								
	22	v								
	23	v								
	24	v								
	25	v								
	26	v								
	27	o								
	28	o								
	29	o								
	30	v								
	31	v								
	32	v								
	33	v								
	34	v								
	35	v								
	36	v								
	37	v								
	38	v								
	39									
	40									
	41									
	42									
	43									
	44									
	45									
	46									
	47									
	48									
	49									
	50									

Claim		Date								
Final	Original									
	51									
	52									
	53									
	54									
	55									
	56									
	57									
	58									
	59									
	60									
	61									
	62									
	63									
	64									
	65									
	66									
	67									
	68									
	69									
	70									
	71									
	72									
	73									
	74									
	75									
	76									
	77									
	78									
	79									
	80									
	81									
	82									
	83									
	84									
	85									
	86									
	87									
	88									
	89									
	90									
	91									
	92									
	93									
	94									
	95									
	96									
	97									
	98									
	99									
	100									

Claim		Date								
Final	Original									
	101									
	102									
	103									
	104									
	105									
	106									
	107									
	108									
	109									
	110									
	111									
	112									
	113									
	114									
	115									
	116									
	117									
	118									
	119									
	120									
	121									
	122									
	123									
	124									
	125									
	126									
	127									
	128									
	129									
	130									
	131									
	132									
	133									
	134									
	135									
	136									
	137									
	138									
	139									
	140									
	141									
	142									
	143									
	144									
	145									
	146									
	147									
	148									
	149									
	150									

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/972,888	MICHAELIS ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

SEARCHED			
Class	Subclass	Date	Examiner
714	11-13	7/5/2007	CM
712	31	7/5/2007	CM

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Search History Enclosed	7/5/2007	CM
Inventor Name Search	7/5/2007	CM

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 1169

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/972,888	10/25/2004 RULE	714	2113	200404970-1

APPLICANTS

Scott L. Michaelis, Plano, TX;
Anurupa Rajkumari, Round Rock, TX; CM
Sylvia K. Myer, Fort Collins, CO;
Richard D. Powers, Highland Village, TX;

**** CONTINUING DATA ****************************

**** FOREIGN APPLICATIONS ***********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 01/12/2005

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☒ no	TX	3	38	5
35 USC 119 (a-d) conditions met	☐ yes ☒ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature Initials				

ADDRESS
22879

TITLE
System and method for system firmware causing an operating system to idle a processor

FILING FEE RECEIVED		
1290	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	710	714/11.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/02 15:02
S2	0	("2006/0107107").URPN.	USPAT	AND	ON	2007/07/02 10:38
S3	0	("2006/0107106").URPN.	USPAT	AND	ON	2007/07/02 10:38
S4	323	714/12.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 16:14
S5	580	714/13.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/03 12:42
S6	460	714/13.ccls. and (not 714/11,12.ccls.)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/03 11:03
S7	94	712/31.ccls.	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/03 12:42
S8	0	("2007/0043972").URPN.	USPAT	AND	ON	2007/07/03 13:59
S9	24	("20040019771" | "20040153731" | "20040153857" | "4589066" | "4750177" | "5369749" | "5732209" | "5748873" | "5913059" | "6065135" | "6141718" | "6148348" | "6263452" | "6330661" | "6378021" | "6567839" | "6615366" | "6625749" | "6625756" | "6640313" | "6751749" | "6772368" | "6976155" | "7003691").PN. OR ("7155721").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 20:59
S10	9	("4750177" | "4849979" | "5157780" | "5428768" | "5434997" | "6065135" | "6249856" | "6279119").PN. OR ("7003691").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:09
S11	25	("4438494" | "4503535" | "4823256" | "4916704" | "5138708" | "5226152" | "5233615" | "5249187" | "5249188" | "5255367" | "5313575" | "5339408" | "5353436" | "5640521").PN. OR ("5915082").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:10
S12	21	("20020073357" | "20020144177" | "20020152418" | "20020152420" | "20030005380" | "4785453" | "5226152" | "5276823" | "5434997" | "5764660" | "5948111" | "6065135" | "6247144" | "6393582" | "6473869" | "6604177" | "6615366" | "6625749" | "6751698" | "6820213" | "7055060"). PN. OR ("7237144").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:13

EAST Search History

S13	27	("4751639" | "5799022" | "5903717" | "5923830").PN. OR ("6141770").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:15
S14	1	("2004/0078650").URPN.	USPAT	AND	ON	2007/07/03 21:18
S15	1	("2004/0006722").URPN.	USPAT	AND	ON	2007/07/03 21:19
S16	3	("2003/0051190").URPN.	USPAT	AND	ON	2007/07/03 21:19
S17	32	("4438494" | "4503535" | "4823256" | "4916704" | "5138708" | "5226152" | "5233615" | "5249187" | "5249188" | "5313575" | "5353436" | "5915082"). PN. OR ("6065135").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:19
S18	0	("2006/0248384").URPN.	USPAT	AND	ON	2007/07/03 21:22
S19	1	("2005/0246581").URPN.	USPAT	AND	ON	2007/07/03 21:22
S20	1	("2005/0240811").URPN.	USPAT	AND	ON	2007/07/03 21:22
S21	15	("20020073357" | "20020144177" | "20030126498" | "20040019771" | "20040153731" | "20040153857" | "4589066" | "5732209" | "6065135" | "6148348" | "6263452" | "6378021" | "6615366" | "6751749" | "6772368"). PN. OR ("7085959").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:22
S22	14	("5522029" | "5884019" | "5892898" | "5919266" | "6065078" | "6141770" | "6173386" | "6199179" | "6308285" | "6360333").PN. OR ("6675324").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:24
S23	39	("4181940" | "4634110" | "5155731" | "5247659" | "5408647" | "5418955"). PN. OR ("5491788").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:26
S24	0	("2006/0010344").URPN.	USPAT	AND	ON	2007/07/03 21:29
S25	33	("3898621" | "4907228" | "4954942" | "4984234" | "5005174" | "5136204" | "5255367" | "5278962").PN. OR ("5748873").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:29
S26	143	("3252149" | "3303474" | "3395396" | "3409879" | "3444528" | "3503048" | "3786433" | "3810119" | "3931505" | "4198678").PN. OR ("4358823").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:31
S27	29	("4453215" | "4912707" | "5475856" | "5504859" | "5530802" | "5664214" | "5748873" | "6279119" | "6393582"). PN. OR ("6625749").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:35

EAST Search History

S28	17	("20030167389" | "20040006722" | "20040078650" | "20040078651" | "20050149776" | "20050240810" | "20050240811" | "4453215" | "4553215" | "4912707" | "5475856" | "5504859" | "5530802" | "5664214" | "5748873" | "6279119" | "6393582"). PN. OR ("7134047").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:38
S29	7	("5761518" | "5978923").PN. OR ("6308285").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:39
S30	22	("5465360" | "5491788" | "5497497" | "5535395" | "5568641" | "5611078" | "5627962" | "5659748" | "5724527" | "5729675" | "5737604" | "5737615" | "5761518" | "5870602" | "6058475" | "6122735" | "6308285").PN. OR ("6496881").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:39
S31	18	("4679166" | "5327548" | "5448716" | "5450576" | "5491788" | "5495569" | "5659748" | "5724527" | "5860002"). PN. OR ("6058475").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:41
S32	18	("4888683" | "5450576" | "5491788" | "5627962" | "5659748" | "5729675" | "5768585").PN. OR ("6009521").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/03 21:42
S33	14	reestablish$4 with lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:35
S34	6	(("5675794") or ("6438687") or ("6920581")).PN.	US-PGPUB; USPAT; DERWENT	OR	OFF	2007/07/04 11:37
S35	11	(("5226152") or ("5249188") or ("5751932") or ("5758058") or ("5764660") or ("6065135") or ("6148348") or ("6473869") or ("6560682") or ("6604177") or ("6615366")).PN.	USPAT	OR	OFF	2007/07/04 11:42
S36	8	(("6625749") or ("6687851") or ("6754787") or ("20020144177") or ("20030070050") or ("20040006722") or ("20040019771") or ("20040153857")).PN.	US-PGPUB; USPAT	OR	OFF	2007/07/04 11:50
S37	15	resynch$7 with lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:38
S38	13	lockstep with (reset$4 or resynch$8 or reestablish$5) with (operating adj system)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:41

EAST Search History

S39	55	recover$4 with lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:47
S40	62	recover$4 with (lock adj step)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:48
S41	54	S40 and (not S39)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:48
S42	19	(lockstep or (lock adj step)) with boot	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:54
S43	24	(lockstep or (lock adj step)) with boot$4	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 12:55
S44	30	(lockstep or (lock adj step)) with idle$4	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:03
S45	225	(lockstep or (lock adj step)) and (boot with processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:03
S46	22	(lockstep or (lock adj step)) and (boot adj2 processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:05
S47	19	(lockstep or (lock adj step)) and (boot adj processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:05
S48	19	(lockstep or (lock adj step)) and (boot$4 adj processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 13:06
S49	2	("20050172164").PN.	US-PGPUB; USPAT; DERWENT	OR	OFF	2007/07/04 14:17
S50	20	lockstep with spare	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 14:18
S51	23	lockstep and (spare with (switch$4 or failover))	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:12
S52	27	lockstep and (spare with (switch$4 or failover or replac$4))	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:13
S53	23	("4015246" | "4799140" | "4926281" | "4967347" | "5276823" | "5423024" | "5572620" | "5596756" | "5666483" | "5799198").PN. OR ("5923830").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2007/07/04 15:18

EAST Search History

S54	373	(boot adj processor)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:25
S55	0	(boot adj processor) with failover	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:25
S56	7	(boot adj processor) with replac$4	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:32
S57	17	(boot adj processor) and lockstep	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 15:32
S58	139	714/11,12.ccls. and boot	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 16:55
S59	29	ACPI with eject	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/04 16:55
S60	3	grochowski.in. and spare	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/05 11:58
S61	0	quach.in. and spare	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/05 11:58
S62	4	safford.in. and spare	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/05 11:58
S63	9	safford.in. and boot	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/05 11:58
S64	2	("6920581").PN.	US-PGPUB; USPAT; DERWENT	OR	OFF	2007/07/11 12:47
S65	147	(lockstep or (lock adj step)) and fatal	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/11 12:48
S66	14	(lockstep or (lock adj step)) same fatal	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/11 12:58
S67	3	(lockstep or (lock adj step)) same severity	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/11 12:58
S68	297	(lockstep or (lock adj step)) same level	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/11 12:58

EAST Search History

S69	49	(lockstep or (lock adj step)) same ((error or fault) with level)	US-PGPUB; USPAT; DERWENT	AND	ON	2007/07/11 12:59

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404970-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): **Scott L. Michaelis et al.**

TITLE: **SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR**

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 3 sheets of drawings (one set) ( ) Associate Power of Attorney

( ) Form PTO-1449 (X) Information Disclosure Statement and Form PTO-1449

( ) Priority document(s) ( ) (Other) _____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	38 — 20	18	X $18	$ 324
INDEPENDENT CLAIMS	5 — 3	2	X $88	$ 176
ANY MULTIPLE DEPENDENT CLAIMS	0		$300	$ 0
BASIC FEE: Design ($350.00); Utility ($790.00)				$ 790
TOTAL FILING FEE				$ 1,290
OTHER FEES				$
TOTAL CHARGES TO DEPOSIT ACCOUNT				$ 1,290

Charge $ 1,290 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EV 375342713US

Date of Deposit Oct. 25, 2004

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450

By _____

Typed Name: Phyllis Ewing

Respectfully submitted,

Scott L. Michaelis et al.

By _____

Jody C. Bishop

Attorney/Agent for Applicant(s)
Reg. No. 44,034
Date: Oct. 25, 2004

Telephone No.: (214) 855-8007

- Attach as First Page to Transmitted Papers -

Certificate of Express Mailing Under 37 CFR 1.10

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Airbill No. EV 375342713US in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on October 25, 2004
Date

Signature

Phyllis Ewing
Typed or printed name of person signing Certificate

Registration Number, if applicable

(214) 855-8000
Telephone Number

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

Assignment (copy) 2 pages
Assignment Recordation Cover Sheet - 2 pages (1 orig. + 1 copy)
Certificate of Express Mail - 1 page

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

Inventors:

Scott L. Michaelis
1524 Bamburgh Drive
Plano, TX 75075
Citizenship: U.S.A.

Anurupa Rajkumari
2511 Echo Wood Place
Round Rock, TX 78681
Citizenship: India

Sylvia K. Myer
836 Terra View Circle
Fort Collins, CO 80525
Citizenship: U.S.A.

Richard D. Powers
2985 Hillside Drive
Highland Village, TX 75077
Citizenship: U.S.A.

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is related to the following concurrently filed and commonly assigned U.S. Patent Applications: Serial No. _____ [Attorney Docket No. 200404944-1] titled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. _____ [Attorney Docket No. 200404943-1] titled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PROCESSOR MODULE"; Serial No. _____ [Attorney Docket No. 200404941-1] titled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION"; Serial No. _____ [Attorney Docket No. 200404973-1 titled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR"; Serial No. _____ [Attorney Docket No. 200404971-1] titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"; Serial No. _____ [Attorney Docket No. 200404946-1] titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION"; Serial No. _____ [Attorney Docket No. 200404972-1] titled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"; and Serial No. _____ [Attorney Docket No. 200404974-1] titled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR", the disclosures of which are hereby incorporated herein by reference.

DESCRIPTION OF RELATED ART

[0002] Silent Data Corruption ("SDC") is a difficult problem in the computing industry. In general, SDC refers to data that is corrupt, but which the system does not detect as being corrupt. SDCs primarily occur due to one of two factors: a) a broken hardware unit or b) a "cosmic" event that causes values to change somewhere in the system. Broken hardware means

unit in a processor is instructed to add 1+1 and it returns the incorrect answer 3 instead of the correct answer 2. An example of a cosmic event is when a charged particle (e.g., alpha particle or cosmic ray) strikes a region of a computing system and causes some bits to change value (e.g., from a 0 to a 1 or from a 1 to a 0).

[0003] Numerous techniques have been developed for detecting SDC to prevent the SDC from remaining "silent" or "undetected" within a system, as well as preventing such SDC from propagating through the system. Examples of these techniques include parity-based mechanisms and error correcting codes (ECCs) on buses and memory locations, as well as checksums and/or cyclic redundancy checks (CRC) over regions of memory. Parity-based mechanisms are often employed in processors, wherein a parity bit is associated with each block of data when it is stored. The parity bit is set to one or zero according to whether there is an odd or even number of ones in the data block. When the data block is read out of its storage location, the number of ones in the block is compared with the parity bit. A discrepancy between the values indicates that the data block has been corrupted. ECCs are parity-based mechanisms that track additional information for each data block. The additional information allows the corrupted bit(s) to be identified and corrected.

[0004] Parity/ECC mechanisms have been employed extensively for caches, memories, and similar data storage arrays. In the remaining circuitry on a processor, such as data paths, control logic, execution logic, and registers (the "execution core"), it is more difficult to apply parity/ECC mechanisms for SDC detection. Thus, there is typically some unprotected area on a processor in which data corruption may occur and the parity/ECC mechanisms do not prevent the corrupted data from actually making it out onto the system bus. One approach to SDC detection in an execution core (or other unprotected area of the processor chip) is to employ "lockstep processing." Generally, in lockstep processing two processors are paired together, and the two processors perform exactly the same operations and the results are compared (e.g., with an XOR gate). If there is ever a discrepancy between the results of the lockstep processors, an error is signaled. The odds of two processors experiencing the exact same error at the exact same moment (e.g., due to a cosmic event occurring in both processors at exactly the same time or due to a mechanical failure occurring in each processor at exactly the same time) is nearly zero.

[0005] A pair of lockstep processors may, from time to time, lose their lockstep. "Loss of lockstep" (or "LOL") is used broadly herein to refer to any error in the pair of lockstep processors. One example of LOL is detection of data corruption (e.g., data cache error) in one of the processors by a parity-based mechanism and/or ECC mechanism. Another example of LOL is detection of the output of the paired processors not matching, which is referred to herein as a "lockstep mismatch." It should be recognized that in some cases the data in the cache of a processor may become corrupt (e.g., due to a cosmic event), which once detected (e.g., by a parity-based mechanism or ECC mechanism of the processor) results in LOL. Of course, unless such corrupt data is acted upon by the processor, the output of that processor will not fail to match the output of its paired processor and thus a "lockstep mismatch" will not occur. For example, suppose that a value of "1" is stored to first location of cache in each of a pair of lockstep processors and a value of "1" is also stored to a second location of cache in each of the pair of lockstep processors. Further suppose that a cosmic event occurs for a first one of the processors, resulting in the first location of its cache being changed from "1" to "0", and thus corrupted. This data corruption in the first processor is a LOL for the pair. An error detection mechanism of this first processor may detect the data corruption, thus detecting the LOL. If the processors are instructed to act on the data of their first cache locations, then a lockstep mismatch will occur as the output of each of the processors will not match. For instance, if the processors each add the data stored to the first location of their respective cache with the data stored to the second location of their respective cache, the first processor (having the corrupt data) will output a result of "1" (0+1=1) while the second processor outputs a result of "2" (1+1=2), and thus their respective outputs will not match.

[0006] By employing such techniques as parity-based error detection mechanisms and output comparisons for lockstep paired processors, SDC detection can be enhanced such that practically no SDC occurring in a processor goes undetected (and thus such SDC does not remain "silent") but instead results in detection of LOL. However, the issue then becomes how best for the system to respond to detected LOL. The traditional response to detected LOL has been to crash the system to ensure that the detected error is not propagated through the system. That is, LOL in one pair of lockstep processors in a system halts processing of the system even if other processors that have not encountered an error are present in the system. However, with the increased desire for many systems to maintain high availability, crashing the system each time LOL is detected is not an attractive proposition. This is particularly unattractive for large

systems having many processors because cosmic events typically occur more frequently as the processor count goes up, which would result in much more frequent system crashes in those large systems. High availability is a major desire for many customers having large, multi-processor systems, and thus having their system crash every few weeks is not an attractive option. Of course, permitting corrupt data to propagate through the system is also not a viable option.

[0007] Prior solutions attempting to resolve at least some detected SDCs without requiring the system to be crashed have been Operating System ("OS") centric. That is, in certain solutions the OS has been implemented in a manner to recover from a detected LOL without necessarily crashing the system. This OS-centric type of solution requires a lot of processor and platform specific knowledge to be embedded in the OS, and thus requires that the OS provider maintain the OS up-to-date as changes occur in later versions of the processors and platforms in which the OS is to be used. This is such a large burden that most commonly used OSs do not support lockstep recovery.

[0008] Certain solutions have attempted to recover from a LOL without involving the OS in such recovery procedure. For instance, in one technique upon LOL being detected, firmware is used to save the state of one of the processors in a lockstep pair (the processor that is considered "good") to memory, and then both processors of the pair are reset and reinitialized. Thereafter, the state is copied from the memory to each of the processors in the lockstep pair. This technique makes the processors unavailable for an amount of time without the OS having any knowledge regarding this unavailability, and if the amount of time required for recovery is too long, the system may crash. That is, typically, if a processor is unresponsive for X amount of time, the OS will assume that the processor is hung and will crashdump the system so that the problem can be diagnosed. Further, in the event that a processor in the pair cannot be reset and reinitialized (e.g., the processor has a physical problem and fails to pass its self-test), this technique results in crashing the system.

BRIEF SUMMARY OF THE INVENTION

[0009] According to one embodiment, a method comprises system firmware instructing a system's operating system to idle a processor, and responsive to the instructing, the operating system idling the processor and returning control over the processor to the system firmware.

[0010] According to one embodiment, a method comprises detecting loss of lockstep (LOL) for a processor module in a system, and responsive to the detecting LOL for the processor module, system firmware instructing an operating system to idle the processor module.

[0011] According to one embodiment, a method comprises detecting loss of lockstep (LOL) for a processor module in a system. The method further comprises, responsive to the detecting LOL, generating an interrupt, by system firmware, and, responsive to the interrupt, an operating system idling the processor module.

[0012] According to one embodiment, a method comprises detecting loss of lockstep (LOL) for a processor module in a system, and continuing operation of the processor module without lockstep protection.

[0013] According to one embodiment, a system comprises a processor, and an operating system for scheduling operations for the processor. The system further comprises system firmware operable to request that the operating system idle the processor.

[0014] According to one embodiment, a system comprises means for detecting loss of lockstep (LOL) for a processor module in a system. The system further comprises system firmware including means, responsive to the detecting LOL for the processor module, for instructing an operating system to idle the processor module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIGURE 1 shows an example embodiment of a system that uses firmware for instructing an operating system to idle a processor module responsive to detecting a loss of lockstep (LOL) for the processor module;

[0016] FIGURE 2 shows a block diagram of one embodiment implemented for the IA-64 processor architecture; and

[0017] FIGURE 3 shows an exemplary operational flow diagram of system firmware according to one embodiment for instructing the operating system to idle a processor module responsive to detection of LOL for the processor module.

DETAILED DESCRIPTION OF THE INVENTION

[0018] Embodiments are described herein in which system firmware requests that an operating system (OS) idle a processor. Specific examples are described in which the system firmware requests that the OS idle a processor module responsive to detection of LOL for the processor module. Control over the processor module is returned from the OS to the system firmware, and the system firmware can take actions to attempt to recover lockstep for the processor module. However, the embodiments hereof for using system firmware for requesting that the OS idle a processor and return control over such processor to the system firmware are not limited to instances in which LOL is detected for the processor. Rather, the embodiments for using system firmware for requesting that the OS idle a processor and return control over such processor to the system firmware may be utilized for a variety of reasons, including responsive to any processor errors that are not immediately fatal (such as the LOL errors discussed further below), maintenance of the processor, physically moving the processor module to a different system, power failures, etc. Thus, while exemplary embodiments are described herein specifically for instances in which LOL is detected for a processor module, the concept of utilizing the system firmware for causing the OS to idle a processor module and return control thereof to the system firmware is not limited to instances in which LOL is detected for the processor module.

[0019] As described further herein and in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404941-1] titled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION," the disclosure of which is incorporated herein by reference, certain techniques are provided for recovering from LOL detected for a processor module in a multi-processor system. In using these exemplary techniques, system firmware instructs the system's OS to idle the processor module for which LOL was detected. Control of the processor module is then returned to the system firmware so that the system firmware can take actions to attempt to recover the lockstep. If lockstep is successfully recovered, in certain implementations, the firmware triggers the OS to again recognize the processor module and begin scheduling instructions for it.

[0020] Embodiments disclosed herein provide a system and method for instructing an OS to idle the processor module for which a LOL is detected. In certain embodiments,

responsive to detecting LOL for a processor module, system firmware uses an ACPI method for instructing the OS to idle (or "eject") the processor module. Thus, the OS is aware that the processor module is not to be used, and the firmware can resume control of the processor module and attempt to recover its lockstep. In certain embodiments, the processor module can continue its operation without lockstep protection, at least until the OS is capable of idling/ejecting the processor module in response to the firmware's ACPI instruction.

[0021] Turning to FIGURE 1, an example embodiment of a system 10 that includes system firmware 15 that instructs the system's OS 11 to idle a processor module 12 responsive to detection of LOL for such processor module 12. System 10 includes OS 11, as well as master processor 12A and slave processor 12B (collectively referred to as a lockstep processor pair 12). In certain implementations the lockstep processor pair 12 may be implemented on a single silicon chip, which is referred to as a "dual core processor" in which master processor 12A is a first core and slave processor 12B is a second core. Further, lockstep processor pair 12 may be referred to as a processor or CPU "module" because it includes a plurality of processors (12A and 12B) in such module. Master processor 12A includes cache 14A, and slave processor 12B includes cache 14B. OS 11 and lockstep processor pair 12 are communicatively coupled to bus 16. Typically, master processor 12A and slave processor 12B are coupled to bus 16 via an interface that allows each of such processors to receive the same instructions to process, but such interface only communicates the output of master processor 12A back onto bus 16. The output of slave processor 12B is used solely for checking the output of mater processor 12A. While only one lockstep processor pair 12 is shown for simplicity in the example of FIGURE 1, system 10 may include any number of such lockstep processor pairs. As one specific example, system 10 may have 64 lockstep processor pairs, wherein the master processors of the pairs may perform parallel processing for the system.

[0022] In this example, master processor 12A includes error detect logic 13A, and slave processor 12B includes error detect logic 13B.. While shown as included in each of the processors 12A and 12B in this example, in certain embodiments the error detect logic 13A and 13B may be implemented external to processors 12A and 12B. Error detect logic 13A and 13B include logic for detecting errors, such as data cache errors, present in their respective processors 12A and 12B. Examples of error detect logic 13A and 13B include known parity-based mechanisms and ECC mechanisms. Error detect logic 13C is also included, which may include an XOR (exclusive OR) gate, for detecting a lockstep mismatch between master processor 12A

and slave processor 12B. As mentioned above, a lockstep mismatch refers to the output of master processor 12A and slave processor 12B failing to match. While shown as external to the lockstep processor pair 12 in this example, in certain embodiments error detect logic 13C may be implemented on a common silicon chip with processors 12A and 12B.

[0023] Lockstep mismatch is one way of detecting a LOL between the master processor 12A and slave processor 12B. A detection of an error by either of error detect logic 13A and 13B also provides detection of LOL in the processors 12A and 12B. Because the detection of LOL by error detect logic 13A and 13B may occur before an actual lockstep mismatch occurs, the detection of LOL by error detect logic 13A and 13B may be referred to as a detection of a "precursor to lockstep mismatch". In other words, once an error (e.g., corrupt data) is detected by error detect logic 13A or 13B, such error may eventually propagate to a lockstep mismatch error that is detectable by error detect logic 13C.

[0024] Firmware 15 is also included in system 10, which in this embodiment is invoked upon an error being detected by any of the error detect logics 13A, 13B, and 13C. In certain embodiments, processors 12A and 12B are processors from the Itanium Processor Family (IPF). IPF is a 64-bit processor architecture co-developed by Hewlett-Packard Company and Intel Corporation, which is based on Explicitly Parallel Instruction Computing (EPIC). IPF is a well-known family of processors. IPF includes processors such as those having the code names of MERCED, MCKINLEY, and MADISON. In addition to supporting a 64-bit processor bus and a set of 128 registers, the 64-bit design of IPF allows access to a very large memory (VLM) and exploits features in EPIC. While a specific example implementation of one embodiment is described below for the IPF architecture, embodiments of firmware for notifying the system's OS of a detected LOL as described herein are not limited in application to an IPF architecture, but may be applied as well to other architectures (e.g., 32-bit processor architectures, etc.).

[0025] Processor architecture generally comprises corresponding supporting firmware, such as firmware 15 of system 10. For example, as described further below in conjunction with the specific example of FIGURE 2, the IPF processor architecture comprises such supporting firmware as Processor Abstraction Layer (PAL), System Abstraction Layer (SAL), and Extended Firmware Interface (EFI). Such supporting firmware may enable, for example, the OS to access a particular function implemented for the processor. For instance, the OS may query the PAL as to the size of the cache implemented for the processor, etc. Other

well-known functions provided by the supporting firmware (SAL, EFI) include, for example: (a) performing I/O configuration accesses to discover and program the I/O Hardware (SAL_PCI_CONFIG_READ and SAL_PCI_CONFIG_WRITE); (b) retrieving error log data from the platform following a Machine Check Abort (MCA) event (SAL_GET_STATE_INFO); (c) accessing persistent store configuration data stored in non-volatile memory (EFI variable services: GetNextVariableName, GetVariable and SetVariable); and accessing the battery-backed real-time clock/calendar (EFI GetTime and SetTime). Accordingly, the supporting firmware, such as the PAL, is implemented to provide an interface to the processor(s) for accessing the functionality provided by such processor(s). Each of those interfaces provide standard, published procedure calls that are supported. While shown as external to the lockstep processor pair 12 in this example, in certain embodiments all or a portion of firmware 15 may be implemented on a common silicon chip with processors 12A and 12B.

[0026] In the example embodiment of FIGURE 1, upon firmware 15 being invoked responsive to detection of LOL for processor module 12 (by any of error detect logics 13A, 13B, and 13C), firmware 15 instructs OS 11 to idle the processor module 12 and return control over such processor module 12 to the firmware 15. In the specific example of FIGURE 1, upon firmware 15 being invoked responsive to detection of LOL for processor module 12, firmware 15 determines, in operational block 101, whether the detected LOL is a recoverable LOL. That is, firmware 15 determines in block 101 whether the detected LOL is of a type from which the firmware can recover lockstep for the lockstep processor pair 12 without crashing the system. If the lockstep is not recoverable from the detected LOL, then in the example of FIGURE 1 firmware 15 crashes the system in block 102.

[0027] In this example, firmware 15 is implemented in a manner that allows for recovery from certain detected errors without requiring that OS 11 be implemented with specific knowledge for handling such recovery. However, if the lockstep is determined to be recoverable, firmware 15 cooperates with OS 11 via standard OS methods to recover the lockstep. For instance, in the example embodiment of FIGURE 1, Advanced Configuration and Power Interface (ACPI) methods are used by firmware 15 to cooperate with OS 11. Accordingly, no processor or platform specific knowledge is required to be embedded in OS 11, but instead any ACPI-compatible OS may be used, including without limitation HP-UX and Open VMS operating systems.

[0028] In the example embodiment of FIGURE 1, if lockstep is determined to be recoverable in block 101, then firmware 15 triggers OS 11 to idle the master processor 12A in block 103. In this embodiment, firmware 15 utilizes an ACPI method 104 to "eject" master processor 12A, thereby triggering OS 11 to idle the master processor 12A (i.e., stop scheduling tasks for the processor). Of course, by idling master processor 12A, slave processor 12B will in turn be idled. Thus, idling master processor 12A results in idling the lockstep processor pair 12. In this example embodiment, OS 11 is not aware of the presence of slave processor 12B, but is instead aware of master processor 12A. The interface of lockstep processor pair 12 to bus 16 manages copying to slave processor 12B the instructions that are directed by OS 11 to master processor 12A. Thus, firmware 15 need not direct OS 11 to eject slave processor 12B, as OS 11 is not aware of such slave processor 12B in this example implementation. Again, by idling master processor 12A, slave processor 12B is also idled as it merely receives copies of the instructions directed to master processor 12A. Of course, if in a given implementation OS 11 is aware of slave 12B, firmware 15 may be implemented to also direct OS 11 to idle such slave processor 12B in a manner similar to that described for idling master processor 12A.

[0029] Firmware 15 then attempts to recover lockstep for the lockstep processor pair 12 in block 105. For instance, firmware 15 resets the processor pair 12. During such reset of processor pair 12, system 10 can continue to operate on its remaining available processors (not shown in FIGURE 1).

[0030] Once the processor pair 12 is reset and lockstep is recovered, firmware 15 reintroduces master processor 12A to OS 11 in operational block 106. In this embodiment, firmware 15 updates the ACPI device table information for master processor 12A to indicate that such master processor 12A is "present, functioning and enabled." As discussed in the ACPI 2.0 specification for the _STA status method of a device, the _STA (status) object returns the status of a device, which can be one of the following: enabled, disabled, or removed. In this respect, in the result code (bitmap) bit 0 is set if the device is present; bit 1 is set if the device is enabled and decoding its resources; bit 2 is set if the device should be shown in the UI; bit 3 is set if the device is functioning properly (cleared if the device failed its diagnostics); bit 4 is set if the battery is present; and bits 5-31 are reserved. A device can only decode its hardware resources if both bits 0 and 1 are set. If the device is not present (bit 0 cleared) or not enabled (bit 1 cleared), then the device must not decode its resources. Bits 0, 1 and 3 are the "present, enabled and functioning" bits mentioned above. Firmware 15 utilizes an ACPI method 107 to trigger OS 11

to "check for" master processor 12A, thereby reintroducing the master processor 12A to OS 11. As a result of checking for master processor 12A, OS 11 will recognize that such master processor 12A is again available and will thus begin scheduling tasks for master processor 12A once again.

[0031] Exemplary techniques for recovering from a detected LOL that may be employed are described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404941-1] titled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION," the disclosure of which is incorporated herein by reference. Embodiments provided herein further discuss techniques for instructing a system's OS to idle a processor module for which LOL is detected. Embodiments provided herein do not require that the OS be implemented with processor-specific information to receive an instruction to idle the processor responsive to LOL being detected for the processor. That is, the OS is not required to be developed specifically for a certain processor architecture in order to receive an instruction from the system firmware to idle the processor. For instance, in certain embodiments, standard OS methods, such as ACPI methods, are used for instructing the OS to idle the processor. Thus, in certain embodiments, any ACPI-compatible OS can receive an instruction to idle the processor module in the manner described herein. Thus, in accordance with certain embodiments, an OS that is fully ACPI compliant can receive notification that a processor should have its use discontinued, responsive to detected LOL. Further, in certain implementations, the OS can keep using the disabled processor until it is convenient to eject the processor and return it to firmware control.

[0032] FIGURE 2 shows a block diagram of one embodiment of the above system 10, which is implemented for the IPF processor architecture and is labeled as system 10_A. The quintessential model of the traditional IPF architecture is given in the Intel IA-64 Architecture Software Developer's Manual, Volume 2: IA-64 System Architecture, in section 11.1 *Firmware Model*, the disclosure of which is hereby incorporated herein by reference. Accordingly, in this example embodiment of system 10_A, firmware 15, labeled as firmware 15_A, includes processor abstraction layer (PAL) 201 and platform/system abstraction layer (SAL) 202. In general, PAL 201 is firmware provided by Intel for its processors, and SAL 202 is developed by an original equipment manufacturer (OEM) for the specific system/platform in which the processors are to be employed. PAL 201, SAL 202, as well as an extended firmware interface (EFI) layer (not

shown), together provide, among other things, the processor and system initialization for an OS boot in an IPF system.

[0033] It should be noted that while the above description of PAL and SAL is specific to the IPF architecture, other architectures may include a "PAL" and "SAL" even though such firmware layers may not be so named or specifically identified as separate layers. In general, such a PAL layer may be included in a given system architecture to provide an interface to the processor hardware. The interface provided by the PAL layer is generally dictated by the processor manufacturer. Similarly, a SAL layer may be included in a given system architecture to provide an interface from the operating system to the hardware. That is, the SAL may be a system-specific interface for enabling the remainder of the system (e.g., OS, etc.) to interact with the non-processor hardware on the system and in some cases be an intermediary for the PAL interface.

[0034] The boot-up process of a traditional IPF system, for example, proceeds as follows: When the system is first powered on, there are some sanity checks (e.g., power on self-test) that are performed by microprocessors included in the system platform, which are not the main system processors that run applications. After those checks have passed, power and clocks are given to a boot processor (which may, for example, be master processor 12A). The boot processor begins executing code out of the system's Read-Only Memory (ROM) (not specifically shown in FIGURE 2). The code that executes is the PAL 201, which gets control of system 10. PAL 201 executes to acquire all of the processors in system 10_A (recall that there may be many lockstep processor pairs 12) such that the processors begin executing concurrently through the same firmware.

[0035] After it has performed its duty of initializing the processor(s), PAL 201 passes control of system 10_A to SAL 202. It is the responsibility of SAL 202 to discover what hardware is present on the system platform, and initialize it to make it available for the OS 11. When main memory is initialized and functional, the firmware 15_A is copied into the main memory. Then, control is passed to EFI (not shown), which is responsible for activating boot devices, which typically includes the disk. The EFI reads the disk to load a program into memory, typically referred to as an operating system loader. The EFI loads the OS loader into memory, and then passes it control of system 10_A by branching the boot processor into the entry point of such OS loader program.

[0036] The OS loader program then uses the standard firmware interfaces to discover and initialize system 10_A further for control. One of the things that the OS loader typically has to do in a multi-processor system is to retrieve control of the other processors (those processors other than the boot processor). For instance, at this point in a multi-processor system, the other processors may be executing in do-nothing loops. In an ACPI-compatible system, OS 11 makes ACPI calls to parse the ACPI tables to discover the other processors of a multi-processor system in a manner as is well-known in the art. Then OS 11 uses the firmware interfaces to cause those discovered processors to branch into the operating system code. At that point, OS 11 controls all of the processors and the firmware 15_A is no longer in control of system 10_A.

[0037] As OS 11 is initializing, it has to discover from the firmware 15_A what hardware is present at boot time. And in the ACPI standards, it also discovers what hardware is present or added or removed at run-time. Further, the supporting firmware (PAL, SAL, and EFI) are also used during system runtime to support the processor. For example, OS 11 may access a particular function of master processor 12A via the supporting firmware 15_A, such as querying PAL 201 for the number, size, etc., of the processor's cache 14A. Some other well-known firmware functions that OS 11 may employ during runtime include: (a) PAL 201 may be invoked to configure or change processor features such as disabling transaction queuing (PAL_BUS_SET_FEATURES); (b) PAL 201 may be invoked to flush processor caches (PAL_CACHE_FLUSH); (c) SAL 202 may be invoked to retrieve error logs following a system error (SAL_GET_STATE_INFO, SAL_CLEAR_STATE_INFO); (d) SAL 202 may be invoked as part of hot-plug sequences in which new I/O cards are installed into the hardware (SAL_PCI_CONFIG_READ, SAL_PCI_CONFIG_WRIT); (e) EFI may be invoked to change the boot device path for the next time the system reboots (SetVariable); (f) EFI may be invoked to change the clock/calendar hardware settings; and (g) EFI may be invoked to shutdown the system (ResetSystem).

[0038] A "device tree" is provided, which is shown as device tree 203 in this example. Device tree 203 is stored in SRAM (Scratch RAM) on the cell, which is RAM that is reinitialized. Firmware 15A builds the device tree 203 as it discovers what hardware is installed in the system. Firmware then converts this information to the ACPI tables format and presents it to OS 11 so that OS 11 can know what is installed in the system. The ACPI device tables (not shown) are only consumed by OS 11 at boot time, so they are never updated as things change.

For OS 11 to find the current status, it calls an ACPI "method" to discover the "current status". The _STA method described above is an example of such an ACPI method. When _STA is called, the AML can look for properties on the device specified in the firmware device tree and convert that into the Result Code bitmap described above. So, if lockstep has been lost on a processor, firmware 15A will set the device tree property that indicates loss of lockstep, then when OS 11 calls _STA for that device, the "lockstep lost" property directs the AML code to return to "0" in the "functioning properly" bit so that OS 11 can know there is a problem with that processor.

[0039] A simple example of device tree 203 is shown below in Table 1:

Device	Status	Lockstep Enabled
Processor A	Present, Enabled, and Functioning	Yes

Table 1

[0040] As mentioned above, once LOL is detected for a processor module, it becomes desirable to notify the system's OS that the processor module is running without lockstep. This notification will allow the OS to stop using the processor, release any resources that may be associated with the processor, and return the processor to firmware control so that there is no further opportunity for silent data corruption problems to occur on the processor module that no longer has lockstep protection. Exemplary embodiments are provided herein in which system firmware (e.g., SAL) notifies the OS that lockstep has been lost and the processor should be returned to firmware control. More specifically, exemplary embodiments are provided herein in which system firmware, responsive to detection of LOL for a processor module, instructs the OS to idle the processor module and return control of the processor module to the system firmware.

[0041] FIGURE 3 shows an exemplary operational flow diagram of system firmware according to one embodiment for instructing the OS to idle a processor module for which LOL is detected. This may be thought of as notifying the OS of the LOL detected for the processor module, but in certain embodiments the LOL is not actually notified of the LOL but is instead instructed to idle the processor module and return control over the processor module to the system firmware (without the OS knowing the reason for doing so). As shown, the "Notify OS" procedure of the system firmware is entered in block 301 responsive to detection of LOL for

a processor module, such as processor module 12 of FIGURES 1-2. In operational block 302, SAL sets a property in the firmware device tree indicating that lockstep has been lost and an eject is being requested. In this manner, the system firmware leaves itself a "clue" that the processor has lost lockstep so that when the processor is returned to firmware control (after instructing the OS to idle the processor), the system firmware knows why it has control of the processor. So, in block 302, a property is set in the firmware device tree that indicates lockstep has been lost for this processor module and firmware is requesting that the CPU be ejected and returned to firmware control.

[0042] In operational block 303, SAL asserts a General Purpose Event Interrupt (GPE) by writing to the appropriate GPE register in the ACPI register space. This causes the OS to execute its interrupt handler, which will run an ACPI Machine Language (AML) Method associated with this particular interrupt. In this example, this AML method that is executed responsive to the interrupt generated by the GPE includes an AML instruction called "Notify". This "Notify" operation indicates the CPU object that has lost lockstep (i.e., identifies which processor module lost its lockstep) and that an Eject is being requested as arguments. The AML instruction notifies the OS that action is being requested on this CPU. The AML method then returns and the OS can take action asynchronously to satisfy the notify request. Exemplary actions that can be taken to idle the processor module responsive to this request and then attempt to reestablish lockstep for the processor module are described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404971-1] titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED", the disclosure of which is hereby incorporated herein by reference.

[0043] In operational block 304, the system firmware restores the saved state and resumes the previous context. When an LOL is detected, an MCA (Machine Check Abort) is generated. As soon as the MCA is generated, the "state" of the processor is saved. That means all of the control registers, stack and RSE pointers are moved to a storage area (both memory and extra registers in the processor) so that the application that was running on the processor can be resumed later on. The MCA is processed and then all of the stored pointers and registers are reloaded to exactly what their values were when the MCA occurred. The system firmware calls PAL_MC_RESUME, which triggers PAL to correct the internal state of the processor. That is,

PAL_MC_RESUME then instructs the processor to return to the exact instruction that was executing when the MCA occurred and begin executing again.

[0044] The processor module, returns to normal execution without lockstep protection in operational block 305. That is, the processor module executes normally until the OS idles/ejects it. Before restoring the execution state and calling PAL_MC_RESUME, firmware evaluates the error that occurred. If there is any chance of data corruption propagating throughout the system, then the exemplary process of FIGURE 3 is not followed. For instance, if determined in block 101 of FIGURE 1 that the lockstep is not recoverable, then the system crashes in block 102. The exemplary operational flow of FIGURE 3 is performed in operational block 103 (of FIGURE 1) of this embodiment. Exemplary techniques for deciding whether to attempt to reestablish lockstep for the processor module (and thus whether to request that the OS idle the processor and in the meantime resume operation of the processor) are described further in concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404946-1] titled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION" and concurrently filed and commonly assigned U.S. Patent Application Serial No. _____ [Attorney Docket No. 200404971-1] titled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED", the disclosures of which are hereby incorporated herein by reference.

[0045] In view of the above, embodiments are provided in which system firmware requests that an OS idle a processor and return control over the processor to the system firmware. While specific examples are described above in which the system firmware requests that the OS idle a processor module responsive to detection of LOL for the processor module, embodiments hereof are not limited in application to instances in which LOL is detected for a processor. Rather, Rather, the embodiments described above for using system firmware for requesting that the OS idle a processor and return control over such processor to the system firmware may be utilized for a variety of different applications, including responsive to any processor errors that are not immediately fatal (such as the LOL errors discussed further below), maintenance of the processor, physically moving the processor module to a different system, power failures, etc. Thus, while idling a processor module responsive to detection of LOL is an application of particular advantage, the concept of utilizing the system firmware for causing the OS to idle a

processor module and return control thereof to the system firmware is not intended to be limited to instances in which LOL is detected for the processor module, but may equally be applied in any other desired applications.

CLAIMS

What is claimed is:

1. A method comprising:

system firmware instructing a system's operating system to idle a processor; and

responsive to said instructing, said operating system idling the processor and returning control over the processor to the system firmware.

2. The method of claim 1 wherein said instructing comprises:

using an Advanced Configuration and Power Interface (ACPI) method to instruct the operating system to idle the processor.

3. The method of claim 2 wherein said ACPI method is an ACPI eject method.

4. The method of claim 1 wherein said instructing comprises:

generating an interrupt.

5. The method of claim 4 wherein said generating said interrupt comprises:

said system firmware writing to a general purpose execution (GPE) register.

6. The method of claim 4 further comprising:

executing an Advanced Configuration and Power Interface Machine Language (AML) method associated with the generated interrupt.

7. The method of claim 6 wherein said executing said AML method comprises:

requesting said operating system to eject said processor module.

8. The method of claim 1 wherein said system firmware instructs the system's operating system to idle the processor responsive to detection of loss of lockstep for the processor.

9. The method of claim 8 further comprising:

responsive to said operating system returning control over the processor to the system firmware, the system firmware reestablishing lockstep for the processor.

10. The method of claim 9 wherein said system firmware reestablishes lockstep for the processor without shutting down the operating system.

11. A method comprising:

detecting loss of lockstep (LOL) for a processor module in a system; and

responsive to said detecting LOL for the processor module, system firmware instructing an operating system to idle the processor module.

12. The method of claim 11 further comprising:

responsive to said instructing, said operating system idling the processor module.

13. The method of claim 12 further comprising:

the operating system returning control over the idled processor module to the system firmware.

14. The method of claim 13 further comprising:

the system firmware reestablishing lockstep for the processor module without shutting down the operating system.

15. The method of claim 11 wherein said instructing comprises:

generating an interrupt.

16. The method of claim 15 wherein said generating said interrupt comprises:

writing to a general purpose execution (GPE) register.

17. The method of claim 15 wherein said operating system is Advanced Configuration and Power Interface (ACPI) compatible, further comprising:

executing an ACPI Machine Language (AML) method associated with the generated interrupt.

18. The method of claim 17 wherein said executing said AML method comprises:

requesting said operating system to eject said processor module.

19. A method comprising:

detecting loss of lockstep (LOL) for a processor module in a system; and

continuing operation of the processor module without lockstep protection.

20. The method of claim 19 further comprising:

determining if the LOL is immediately fatal.

21. The method of claim 20 further comprising:

performing said continuing operation if determined that the LOL is not immediately fatal.

22. The method of claim 21 further comprising:

if determined that the LOL is immediately fatal, ceasing operation of the processor module.

23. The method of claim 19 further comprising:

determining if lockstep can be recovered for the processor module without shutting down the system's operating system.

24. The method of claim 23 further comprising:

performing said continuing operation if determined that lockstep can be recovered for the processor module without shutting down the system's operating system.

25. The method of claim 24 further comprising:

ceasing operation of the processor module if determined that lockstep cannot be recovered for the processor module without shutting down the system's operating system.

26. The method of claim 19 further comprising:

responsive to said detecting LOL for the processor module, system firmware instructing the system's operating system to idle the processor module and return control over the processor module to the system firmware.

27. The method of claim 26 further comprising:

while awaiting for the operating system to idle the processor module and return control over the processor module to the system firmware, performing said continuing operation.

28. The method of claim 27 further comprising:

said operating system idling the processor module and returning control over the processor module to the system firmware.

29. The method of claim 28 further comprising:

said system firmware reestablishing lockstep for the processor module, wherein said operating system is not shut down for said reestablishing.

30. A system comprising:

a processor;

an operating system for scheduling operations for the processor; and

system firmware operable to request that said operating system idle the processor.

31. The system of claim 30 wherein said operating system is operable, responsive to said system firmware requesting that said operating system idle the processor, to idle the processor and return control over the processor to the system firmware.

32. The system of claim 31 wherein said system firmware is operable, responsive to detection of loss of lockstep (LOL) for the processor, to request that said operating system idle the processor.

33. The system of claim 32 wherein said system firmware is operable, responsive to receiving said control over the processor, to reestablish lockstep for the processor.

34. The system of claim 30 wherein said system firmware is operable, responsive to detection of loss of lockstep (LOL) for the processor, to request that said operating system idle the processor.

35. The system of claim 30 wherein said processor is an Itanium Processor Family (IPF) processor.

36. The system of claim 30 wherein said system firmware uses an Advanced Configuration and Power Interface (ACPI) method to request that said operating system idle the processor.

37. A system comprising:

means for detecting loss of lockstep (LOL) for a processor module in a system; and

system firmware including means, responsive to said detecting LOL for the processor module, for instructing an operating system to idle the processor module.

38. The system of claim 37 wherein responsive to the instructing means instructing the operating system to idle the processor module, the operating system idling the processor module and returning control over the processor module to the system firmware.

ABSTRACT

According to one embodiment, a method comprises system firmware instructing a system's operating system to idle a processor, and responsive to the instructing, the operating system idling the processor and returning control over the processor to the system firmware. According to one embodiment, a method comprises detecting loss of lockstep (LOL) for a processor module in a system, and responsive to the detecting LOL for the processor module, system firmware instructing an operating system to idle the processor module.

FIG. 1

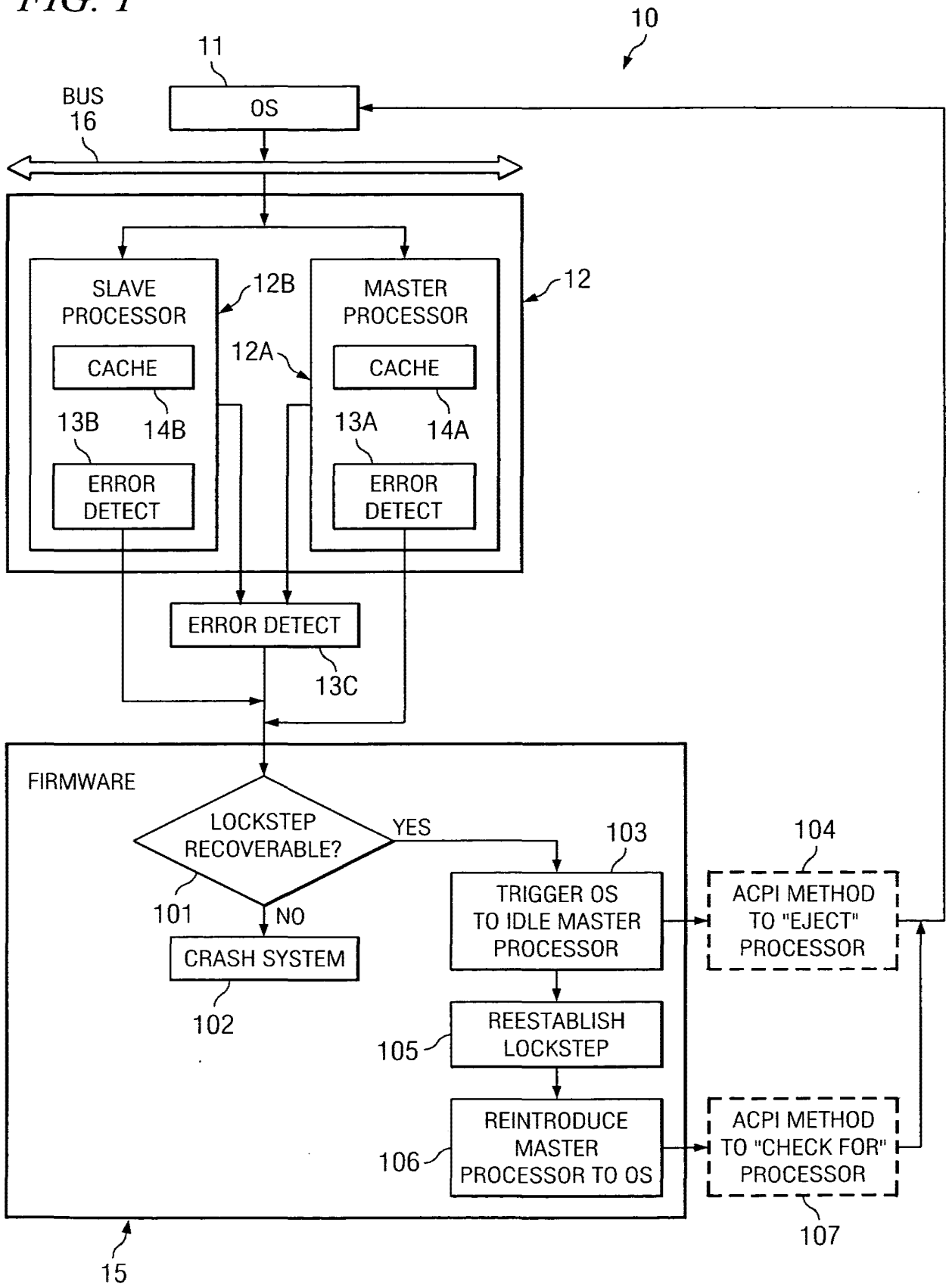

10
11
OS
BUS
16
SLAVE
PROCESSOR
12B
MASTER
PROCESSOR
12
CACHE
12A
CACHE
13B
14B
13A
14A
ERROR
DETECT
ERROR
DETECT
ERROR DETECT
13C
FIRMWARE
LOCKSTEP
RECOVERABLE?
YES
103
104
101
NO
TRIGGER OS
TO IDLE MASTER
PROCESSOR
ACPI METHOD
TO "EJECT"
PROCESSOR
CRASH SYSTEM
102
REESTABLISH
LOCKSTEP
105
REINTRODUCE
MASTER
PROCESSOR TO OS
106
ACPI METHOD
TO "CHECK FOR"
PROCESSOR
107
15

FIG. 2

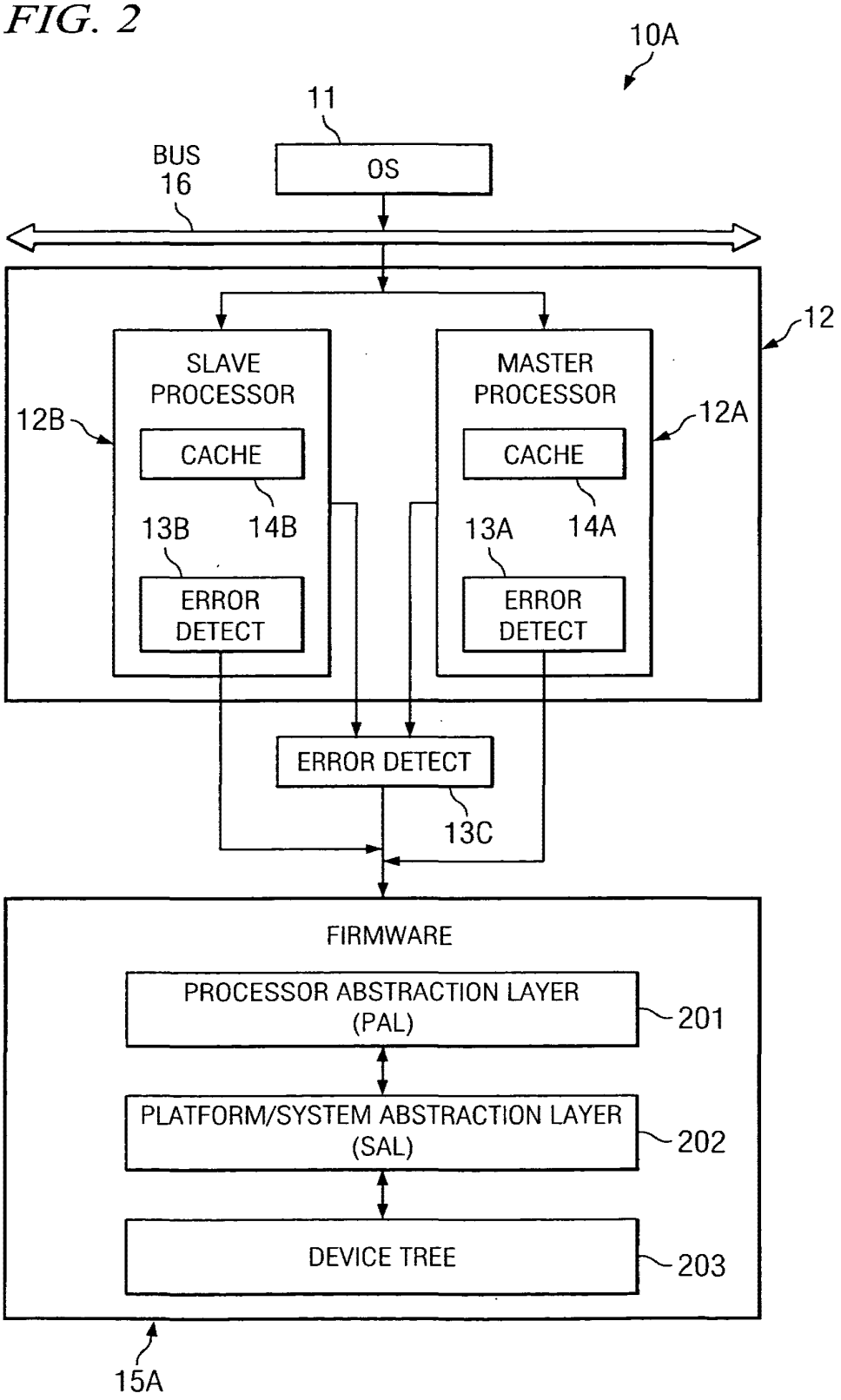
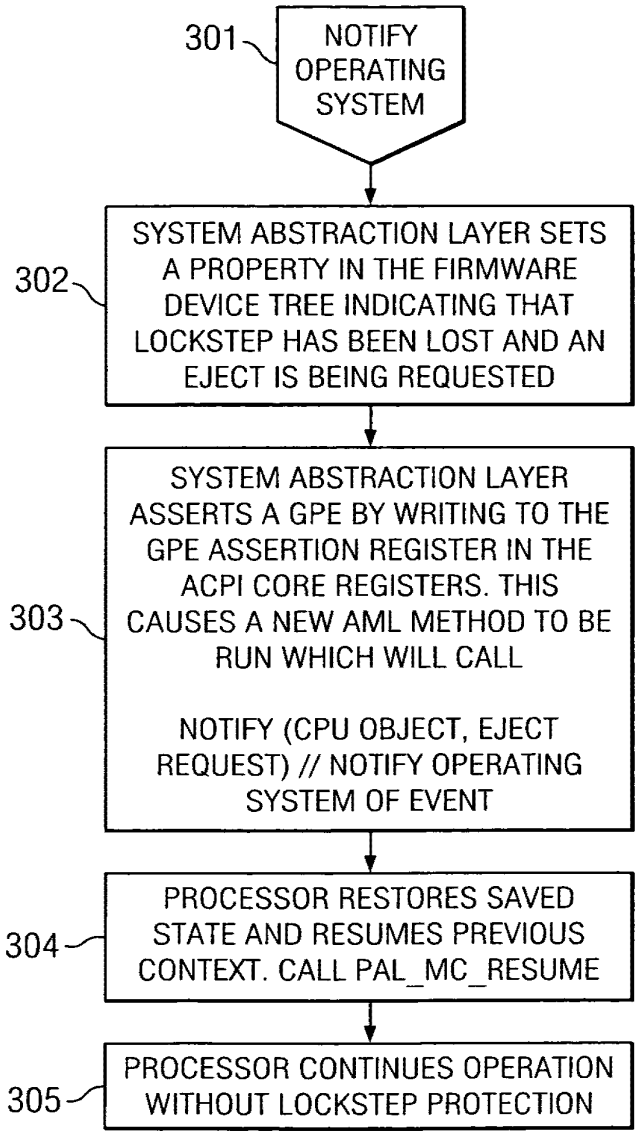

10A
11
OS
BUS
16
12
SLAVE
PROCESSOR
CACHE
14B
13B
ERROR
DETECT
12B
MASTER
PROCESSOR
CACHE
14A
13A
ERROR
DETECT
12A
ERROR DETECT
13C
FIRMWARE
PROCESSOR ABSTRACTION LAYER
(PAL)
201
PLATFORM/SYSTEM ABSTRACTION LAYER
(SAL)
202
DEVICE TREE
203
15A

FIG. 3


301
NOTIFY OPERATING SYSTEM
302
SYSTEM ABSTRACTION LAYER SETS A PROPERTY IN THE FIRMWARE DEVICE TREE INDICATING THAT LOCKSTEP HAS BEEN LOST AND AN EJECT IS BEING REQUESTED
303
SYSTEM ABSTRACTION LAYER ASSERTS A GPE BY WRITING TO THE GPE ASSERTION REGISTER IN THE ACPI CORE REGISTERS. THIS CAUSES A NEW AML METHOD TO BE RUN WHICH WILL CALL
NOTIFY (CPU OBJECT, EJECT REQUEST) // NOTIFY OPERATING SYSTEM OF EVENT
304
PROCESSOR RESTORES SAVED STATE AND RESUMES PREVIOUS CONTEXT. CALL PAL_MC_RESUME
305
PROCESSOR CONTINUES OPERATION WITHOUT LOCKSTEP PROTECTION

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 200404970-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

the specification of which is attached hereto unless the following box is checked:

( ) was filed on _____ as US Application No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO: ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Send Correspondence to:

Customer Number 022879

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Direct Telephone Calls to:

Richard Stokey

(281) 518-3184

Even though the attorney is listed, please associate HP's Customer Number 022879 with this case.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Scott L. Michaelis **Citizenship:** U.S.A.

Residence: 1524 Bamburgh Drive, Plano, TX 75075

Post Office Address: 1524 Bamburgh Drive, Plano, TX 75075

Scott L Michaelis 10/20/2004

Inventor's Signature **Date**

Rev 10/04 (DecPwr)

(Use Page Two For Additional Inventor(s) Signature(s))

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 200404970-1

Full Name of # 2 joint inventor: Anurupa Rajkumari Citizenship: India

Residence: 2511 Echo Wood Place, Round rock, TX 78681

Post Office Address: 2511 Echo Wood Place, Round rock, TX 78681

Anurupa Rajkumari
Inventor's Signature

10/20/04
Date

Full Name of # 3 joint inventor: Sylvia K. Myer Citizenship: U.S.A.

Residence: 836 Terra View Circle, Fort Collins, CO 80525

Post Office Address: 836 Terra View Circle, Fort Collins, CO 80525

Sylvia K. Myer
Inventor's Signature

10/19/04
Date

Full Name of # 4 joint inventor: Richard D. Powers Citizenship: U.S.A.

Residence: 2985 Hillside Drive, Highland Village, TX 75077

Post Office Address: 2985 Hillside Drive, Highland Village, TX 75077

Inventor's Signature

10/20/04
Date

Full Name of # 5 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

Full Name of # 6 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

Full Name of # 7 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

Full Name of # 8 joint inventor: Citizenship:

Residence:

Post Office Address:

Inventor's Signature

Date

(Use Page Two For Additional Inventor(s) Signature(s))

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

10/27/2004 ZJUHAR1 00000066 082025 10972888

01 FC:1001	790.00	DA
02 FC:1202	324.00	DA
03 FC:1201	176.00	DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2004

Application or Docket Number: 10972888

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	38	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	38 minus 20=	* 18
INDEPENDENT CLAIMS	5 minus 3 =	* 2
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	395.00	OR	BASIC FEE	790.00
X$ 9=		OR	X$18=	324
X44=		OR	X88=	176
+150=		OR	+300=	
TOTAL		OR	TOTAL	1290

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

11,19,136137

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X44=		OR	X88=	
+150=		OR	+300=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200404970-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Scott L. Michaelis et al. **Confirmation No.:**

Application No.: **Examiner:**

Filing Date: **Group Art Unit:**

Title: SYSTEM AND METHOD FOR SYSTEM FIRMWARE CAUSING AN OPERATING SYSTEM TO IDLE A PROCESSOR

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EV 375342713US**

Date of Deposit **Oct. 25, 2004**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By

Typed Name: **Phyllis Ewing**

Respectfully submitted,

Scott L. Michaelis et al.

By

Jody C. Bishop

Attorney/Agent for Applicant(s)
Reg. No. **44,034**

Date: **Oct. 25, 2004**

Telephone No.: **(214) 855-8007**

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404970-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,226,152	07/06/1993	Klug et al.	
	1B	5,249,188	09/28/1993	McDonald	
	1C	5,751,932	05/12/1998	Horst et al.	
	1D	5,758,058	05/26/1998	Milburn	
	1E	5,764,660	06/09/1998	Mohat	
	1F	6,065,135	05/16/2000	Marshall et al.	
	1G	6,148,348	11/14/2000	Garnett et al.	
	1H	6,473,869	10/29/2002	Bissett et al.	
	1I	6,560,682	05/06/2003	Miller et al.	
	1J	6,604,177	08/05/2003	Kondo et al.	
	1K	6,615,366	09/02/2003	Grochowski et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Attorney Docket No. 200404974-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR MAINTAINING IN A MULTI-PROCESSOR SYSTEM A SPARE PROCESSOR THAT IS IN LOCKSTEP FOR USE IN RECOVERING FROM LOSS OF LOCKSTEP FOR ANOTHER PROCESSOR"
	1R	Attorney Docket No. 200404944-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR ESTABLISHING A SPARE PROCESSOR FOR RECOVERING FROM LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
	1S	Attorney Docket No. 200404946-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR USING INFORMATION RELATING TO A DETECTED LOSS OF LOCKSTEP FOR DETERMINING A RESPONSIVE ACTION"

EXAMINER	DATE CONSIDERED

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404970-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A	6,625,749	09/23/2003	Quach	
	2B	6,687,851	02/03/2004	Somers et al.	
	2C	6,754,787	06/22/2004	Miller et al.	
	2D	2002/0144177	10/03/2002	Kondo et al.	
	2E	2003/0070050	04/10/2003	Miller et al.	
	2F	2004/0006722	01/08/2004	Safford	
	2G	2004/0019771	01/29/2004	Quach	
	2H	2004/0153857	08/05/2004	Yamazaki et al.	
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	Attorney Docket No. 200404941-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR PROVIDING FIRMWARE RECOVERABLE LOCKSTEP PROTECTION"
	2R	Attorney Docket No. 200404943-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR CONFIGURING LOCKSTEP MODE OF A PRCESSOR MODULE"
	2S	Attorney Docket No. 200404971-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REESTABLISHING LOCKSTEP FOR A PROCESSOR MODULE FOR WHICH LOSS OF LOCKSTEP IS DETECTED"

EXAMINER	DATE CONSIDERED

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. **200404970-1**	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT **Scott L. Michaelis et al.**		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	3Q	Attorney Docket No. 200404972-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR REINTRODUCING A PROCESSOR MODULE TO AN OPERATING SYSTEM AFTER LOCKSTEP RECOVERY"
	3R	Attorney Docket No. 200404973-1, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR SWITCHING THE ROLE OF BOOT PROCESSOR TO A SPARE PROCESSOR RESPONSIVE TO DETECTION OF LOSS OF LOCKSTEP IN A BOOT PROCESSOR"
	3S	

EXAMINER	DATE CONSIDERED