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Hewlett Packard Enterprise			SORRELL, ERON J	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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***EX PARTE* REEXAMINATION COMMUNICATION TRANSMITTAL FORM**

REEXAMINATION CONTROL NO. 90/019,245 .

PATENT UNDER REEXAMINATION 7502958 .

ART UNIT 3992 .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting Request For Ex Parte Reexamination	Control No. 90/019,245	Patent Under Reexamination 7502958	
	Examiner ERON J SORRELL	Art Unit 3992	AIA (FITF) Status No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed 09/01/2023 has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a) ☐ PTO-892, b) ☒ PTO/SB/08, c) ☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

/ERON J SORRELL/
Primary Examiner, Art Unit 3992

cc:Requester (if third party requester)

Decision

A Third-Party Requester, Unified Patents, LLC, ("Requester") has requested *Ex Parte* Reexamination of Claims 1-25 of U.S. Patent No. 7,502,958 to Michaelis et al. ("the '958 Patent"). The Request for *Ex Parte* Reexamination ("the Request") was granted a filing date of September 1, 2023.

MPEP 2240 recites in part,

37 C.F.R. 1.515 Determination of the request for ex parte reexamination.

(a) Within three months following the filing date of a request for an *ex parte* reexamination, an examiner will consider the request and determine whether or not a substantial new question of patentability affecting any claim of the patent is raised by the request and the prior art cited therein, with or without consideration of other patents or printed publications. A statement and any accompanying information submitted pursuant to § 1.501(a)(2) will not be considered by the examiner when making a determination on the request. The examiner's determination will be based on the claims in effect at the time of the determination, will become a part of the official file of the patent, and will be given or mailed to the patent owner at the address provided for in § 1.33(c) and to the person requesting reexamination.

The Request is found to raise at least one substantial new question of patentability ("SNQ") with respect to at least one claim of the '958 Patent thus the Request is **GRANTED**.

Prior/concurrent litigation or Office Proceedings

Reviewing any post grant challenges, the Examiner finds the '958 Patent is subject to the following:

Litigation:

Foras Technologies Ltd. V. Bayerische Motoren Werke Ag et al. (6:23cv386);

Foras Technologies Ltd. V. Kia Corporation et al. (2:23cv219);

Foras Technologies Ltd. V. Nissan Motor Company, Ltd. et al. (1:23cv640);

Foras Technologies Ltd. V. Toyota Motor North America, Inc. et al. (2:23cv150);

Foras Technologies Ltd. V. Volkswagen Ag et al. (2:23cv314);

Office proceedings:

IPR2023-01373 filed September 8, 2023

Listing of Prior Art

The Request alleges the existence of at least one SNQ based on the following patents/printed publications:

- i. U.S. Patent Application Publication No. 2003/0126498 to Bigbee et al. ("Bigbee");
- ii. U.S. Patent No. 7,085,959 to Safford ("Safford");

- iii. U.S. Patent Application Publication No. 2003/0051190 to Marisetty et al. ("Marisetty");
- iv. U.S. Patent No. 5,491,788 to Cepulis et al. ("Cepulis").

Of the four (4) references listed above, only Cepulis is newly cited with respect to the '958 Patent. The other references were all cited during the patent's original prosecution. Safford was used in prior art rejections in the original prosecution and is thus "old art". Marisetty and Bigbee were cited in information disclosure statements filed with Requests for Continued Examination on June 6, 2008 and October 16, 2008, respectively, after the initial Notice of Allowance was mailed on June 3, 2008. Neither Bigbee or Marisetty were specifically addressed by the Examiner of record at the time.

The '958 Patent

The '958 Patent issued on March 10, 2009 having claims 1-25 with claims 1, 13, 19, and 23 being independent. The '958 Patent matured from U.S. Patent Application No. 10/973,076 ("the '076 Application"), filed October 25, 2004.

The '958 Patent discloses a method for providing firmware recoverable lockstep protection in a system comprising at least two processors operating in lockstep by executing the same

instructions and comparing the results to check for errors. If one of the processors becomes faulty, a loss of lockstep is detected and the system triggers, using firmware, the operating system to idle the processors, and attempts to recover lockstep between the processors. If lockstep is recovered, the firmware triggers the operating system to recognize the processors as being available. (See '958 Patent, lines 51-58 of column 3).

Independent claims 1, 13, 19, and 23 are reproduced below for discussion purposes.

*1. A method comprising:
detecting loss of lockstep for a lockstep pair of
processors;
using firmware to trigger an operating system to idle the
lockstep pair of processors, recover lockstep for the
lockstep pair of processors, and trigger the operating
system to recognize the lockstep pair of processors
having recovered lockstep; and
responsive to said detecting loss of lockstep, using said
firmware to determine if lockstep is recoverable for
the lockstep pair of processors, wherein said using
said firmware to determine if lockstep is recoverable
further comprises determining if a lockstep mismatch
has occurred between the lockstep pair of processors.*

*13. A system comprising:
an Advanced Configuration and Power Interface (ACPI)-
compatible operating system;
master processor operable to process instructions scheduled
by said ACPI-compatible operating system;
slave processor lockstepped with the master processor
operable to perform redundant processing of said
instructions scheduled for the master processor; and*

firmware operable, responsive to detection of loss of lockstep between the master and slave processors, to use an ACPI method to trigger the operating system to idle the master processor, attempt to recover lockstep between the master and slave processors, and if recovery of lockstep is successful then use an ACPI method to reintroduce the master processor to the operating system.

19. A system comprising a pair of lockstep processors and computer-executable firmware code stored to a computer-readable medium, the computer-executable firmware code comprising:

firmware code, responsive to detection of loss of lockstep between the pair of lockstep processors, for determining if the lockstep is recoverable for the pair of lockstep processors, wherein said firmware code for determining if the lockstep is recoverable further comprises firmware code for determining if a lockstep mismatch has occurred between the pair of lockstep processors; and

firmware code, responsive to determining that the lockstep is recoverable, for triggering an operating system to idle the processors, attempting to recover lockstep between the pair of processors, and if lockstep is successfully recovered between the pair of processors, triggering said operating system to recognize the processors as being available for receiving instructions.

23. A method comprising:

establishing, in a multi-processor system, a hot spare processor for a system boot processor;

detecting loss of lockstep for a lockstep pair of processors in said multi-processor system;

determining if said lockstep pair of processors for which the loss of lockstep is detected is the system boot processor;

if determined that said lockstep pair of processors for which the loss of lockstep is the system boot processor, copying a state of the system boot processor to the hot spare processor; and

if determined that said lockstep pair of processors for which the loss of lockstep is not the system boot

processor, then triggering an operating system to a) idle the lockstep pair of processors, b) attempt to recover lockstep between the lockstep pair of processors, and c) if lockstep is successfully recovered between the lockstep pair of processors, trigger said operating system to recognize the processors as being available for receiving instructions.

Third Party Requester's Position

The Requester's alleged SNQs have been grouped/reorganized for discussion purposes.

SNQ 1: Bigbee to raise a SNQ over claims 1-8 and 13-22.

This group is based on proposed rejections of claims 1-8 and 13-22 under 35 USC § 102 as being anticipated by Bigbee, or alternatively under 35 USC § 103 as being obvious over Bigbee.

SNQ 2: Safford in view of Marisetty to raise a SNQ over claims 1-8 and 13-22. This group is based on proposed rejections of claims 1-8 and 13-22 under 35 USC § 103 as being obvious over Safford in view of Marisetty.

SNQ 3: Safford in view of Cepulis and further in view if Marisetty to raise a SNQ over claims 9-12 and 23-25. This group is based on proposed rejections of claims 9-12 and 23-25 under

35 USC § 103 as being obvious over Safford in view of Marisetty, and Cepulis.

Review of Prosecution History

Reviewing the prosecution history of the '958 Patent, the Examiner finds the '076 Application was originally filed with claims 1-35 with claims 1, 15, 21, 26, and 29 being independent claims.

On September 12, 2007, a Non-final Office action was mailed in which, among other findings, claims 1-35 were rejected under 35 USC § 103(a) as being obvious over U.S. Patent No. 5,915,082 to Marshall et al. in view of Safford.

On November 27, 2007, the Applicant filed a response to the then outstanding Office action. Aside from changing the dependency of claim 31, the claims were unamended. With respect to the prior art rejections, the Applicant argued that the applied prior art failed to teach triggering an operating system to idle a lockstep pair of processors for which a loss of lockstep has been detected. The Applicant argued that Safford discloses a processor signaling a node controller that a processor pair should be taken offline, which could lead the system to crash. The Applicant argued that Safford's method is distinct from the claimed invention which idles the lock step pair of processors for which lock step has been detected prior

to taking them offline. (See Remarks filed 11/27/07, pages at 17-19).

On February 27, 2008, a Final Office action was mailed in which the Examiner found that claims 15-20 and 26-28 were allowable over the prior art, and objected to claims 8-10, 14, and 33 for being dependent on a rejected base claim, but otherwise allowable. (See Final Rejection mailed 2/27/08, page 7). The Examiner did not provide any specific reasons for identifying the allowable subject matter. The Final Office action maintained the rejections of claims 1-7, 11-13, 21-25, 29-32, 34, and 35.

On April 10, 2008, the Applicant filed a Response after Final Rejection which included claim amendments that put the application in condition for allowance. Specifically, claim 1 was amended to include the limitations from claim 8 (and intervening claim 7) that were found allowable. Independent claim 21 was amended in a similar fashion. Claims 29-35 were canceled.

On June 3, 2008, a Notice of Allowance was mailed in which claims 1-6, 9-22, and 24-28 were allowed and subsequently renumbered as claims 1-25 with claims 1, 13, 19, and 23 being independent. The Notice of Allowance included an Examiner's amendment to claim 21 (renumbered as claim 19) to ensure

statutory compliance with 35 USC § 101, however no specific reasons for allowance were provided.

In light of the foregoing, if a new prior art reference or combination of references teaches,

triggering an operating system to idle a lockstep pair of processors for which loss of lockstep has been detected,

which was the limitation argued as not taught by the prior art just prior to the allowance of claims 13 and 23, then that prior art reference or combination of references would raise a SNQ.

Additionally, if a new prior art reference or combination of references teaches,

using firmware, in response to detecting loss of lockstep between two processors, to determine if lockstep is recoverable for the lockstep pair of processors, wherein using said firmware to determine if lockstep is recoverable further comprises determining if lockstep mismatch has occurred between the lockstep pair of processors,

which were the limitations added to claims 1 and 19 to obtain allowance of those claims, then that prior art reference or combination of references would raise a SNQ.

Substantial New Questions of Patentability

SNQ 1

The Request alleges that Bigbee raises a SNQ over claims 1-8 and 13-22. For the specific reasons below, the Examiner agrees in part. Bigbee raises a SNQ over claims 1-8 and 19-22, however

the Examiner does not find Bigbee to raise a SNQ with respect to claims 13-18.

Bigbee

Bigbee qualifies as prior art at least under pre-AIA 35 USC § 102(b).

Bigbee teaches a method and apparatus for functional redundancy check (FRC) mode recovery in a system comprising a plurality of processors. Bigbee's invention includes data processing hardware, firmware, and software. (See Bigbee, ¶ 12). Bigbee's system is ACPI-compliant and the Operating System (OS) comprises OSPM program code and the firmware comprises an ACPI BIOS. (See *Id.*, ¶ 16). In a particular embodiment, the hardware includes two or more processor packages, each package comprising two or more processor cores operating in lockstep in an FRC mode as a single processor from the point of view of the OS. The hardware also comprises FRC logic which detects errors within individual processor cores which causes the hardware to break lockstep between at least two processor cores within the package. The hardware disables any of the error containing cores and generates a recoverable machine check exception which in turn triggers execution of a processor error handler routine within one of the packages error free cores. (See *Id.*, ¶ 19). Bigbee teaches the FRC logic monitors processor cores operations

involving a shared cache to detect inconsistencies in generated results which indicate an FRC mismatch error. (See *Id.*, ¶ 33).

Bigbee teaches the processor error handler causes the firmware to initiate a platform independent device removal sequence for a processor associated with the processor package. (See *Id.*, ¶ 20). Bigbee further teaches the firmware saves processor related information and attempts to correct processor related errors where possible. Bigbee states that processors may be taken offline and then reset or reinitialized to a state needed for it to be subsequently activated by the operating system (See *Id.*, ¶ 23).

As shown above, Bigbee, which is cited on the cover of the '958 Patent but never specifically discussed on the record, can reasonably be interpreted as teaching

using firmware, in response to detecting loss of lockstep between two processors, to determine if lockstep is recoverable for the lockstep pair of processors (see Bigbee, ¶ 21), *wherein using said firmware to determine if lockstep is recoverable further comprises determining if lockstep mismatch has occurred between the lockstep pair of processors* (see *Id.*, ¶ 33).

These teachings are significant because they include the limitations in independent claims 1 and 19 found patentable during the original prosecution of the '958 Patent. Moreover, there is a substantial likelihood that a reasonable Examiner would consider these teachings important in deciding the

patentability of the '958 Patent. For those reasons, Bigbee is found to raise a SNQ over independent claims 1 and 19.

Additionally, since dependent claims carry with them each of the limitations of the claim(s) from which it depends, it follows that Bigbee also raises a SNQ over claims 2-13 and 19-22.

Regarding independent claim 13, however, Bigbee is not seen as teaching triggering an operating system to idle a lockstep pair of processors for which loss of lockstep has been detected. Instead, Bigbee teaches "Hardware 102 then disables any of the package's error containing cores, placing them in a 'zombie' state, and generates a recoverable machine check exception." (See Bigbee, ¶ 19). Additionally, Bigbee teaches, "...hardware (FRC logic) detects an error within a first processor core of a plurality of processor cores..." (See *Id.*, ¶ 35). Bigbee discloses the OS may virtually eject a processor, however ejecting a processor is distinct from idling or disabling the processor. (See *Id.*, ¶ 23).

With that, Bigbee is not found to raise a SNQ over claims 13-18.

SNQ 2

The Request alleges that Safford in view of Marisetty raises a SNQ over claims 1-8 and 13-22. Upon review and for the reasons discussed below, the Examiner agrees. Safford in view of Marisetty raises a SNQ over claims 1-8 and 13-22.

Safford

Safford qualifies as prior art under pre-AIA 35 USC § 102(a).

Safford teaches a method and apparatus for recovery from a loss of lockstep in a computer system comprising a plurality of processor units, wherein each processor unit comprises at least two processor units operating in lockstep (arranged as a master/checker pair) and an idle processor unit also operating in lockstep. The system further comprises a controller coupled to the at least two processors and the idle processor comprising means for copying an architected state of each of the at least two processors to the idle processor unit. Safford's method comprises receiving loss of lockstep signal from a processor unit, receiving a notice from the processor unit experiencing loss of lockstep to take it offline; moving the architected state of the processor unit experiencing loss of lockstep to a spare unit, wherein the spare unit becomes an active processor. (See Safford, lines 13-57 of column 2).

Safford discloses that at some future time, the processor may recover from the loss of lockstep, and lockstep operation of the processors may be restored. (See *Id.*, lines 41-51 of column 3).

Marisetty

Marisetty qualifies as prior art under pre-AIA 35 USC § 102(b).

Marisetty teaches a multiprocessor system comprising a non-volatile memory that stores an error handling routine which each of the processors may access when detecting an error. The processor detecting the error may signal other processors in the system to enter a "rendezvous state". (See Marisetty, ¶ 15). Marisetty discloses certain system errors can be handled by different software layers comprising a processor abstraction layer (PAL), a system abstraction layer (SAL), and the operating system (OS), wherein the PAL and SAL together are known as firmware. (See *Id.*, ¶¶ 24 and 26). The processor detecting the error may perform error handling then release the other processors from the rendezvous state. (See *Id.*, ¶ 25). The processor performing the error handling may be referred to as a monarch processor which is assigned by the system or determined

each time the system needs to enter the rendezvous state. (See *Id.*, ¶ 43).

As shown above, the combination of Safford and Marisetty can reasonably be interpreted as teaching,

in response to detecting loss of lockstep between two processors, determining if lockstep is recoverable for the lockstep pair of processors (See Safford, line 55 of column 2 to line 52 of column 3), *wherein determining if lockstep is recoverable further comprises determining if lockstep mismatch has occurred between the lockstep pair of processors* (See *Id.*, line 55 of column 2 to line 52 of column 3).

using firmware to detect errors and recover from errors in a processor unit (See Marisetty, ¶ 27).

These teachings are significant because they include the limitations in independent claims 1 and 19 found patentable during the original prosecution of the '958 Patent.

The combination of Safford and Marrietty can also be reasonably interpreted as teaching

idling a lockstep pair of processors for which loss of lockstep has been detected (see Safford, lines 55-67 of column 2).

triggering an operating system to idle processors in a multiprocessor system when errors in the system are detected (see Marisetty, ¶¶ 37, 38, and 42).

These teachings are significant because they include the limitations in independent claim 13 specifically argued by the Applicant as missing from the applied prior art just prior to the claim being found allowable during the original prosecution of the '958 Patent.

Safford was considered during the original prosecution of the '958 Patent, however Safford was never viewed in combination with Marisetty, therefore Safford in view of Marisetty is a new combination of references. Moreover, there is a substantial likelihood that a reasonable Examiner would consider these teachings important in deciding the patentability of the '958 Patent. For those reasons, Safford in view of Marisetty is found to raise a SNQ over independent claims 1, 13, and 19. Additionally, since dependent claims carry with them each of the limitations of the claim(s) from which it depends, it follows that Safford in view of Marisetty also raises a SNQ over claims 2-12 and 14-18, and 20-22.

SNQ 3: The Request alleges Safford in view of Cepulis and further in view if Marisetty raises SNQs over claims 9-12 and 23-25. Upon review, and for the reason discussed below, the Examiner agrees, Safford in view of Cepulis and further in view if Marisetty raises SNQs over claims 9-12 and 23-25.

Safford

Safford qualifies as prior art under pre-AIA 35 USC § 102(a).

Safford teaches a method and apparatus for recovery from a loss of lockstep in a computer system comprising a plurality of processor units, wherein each processor unit comprises at least two processor units operating in lockstep (arranged as a master/checker pair) and an idle processor unit also operating in lockstep. The system further comprises a controller coupled to the at least two processors and the idle processor comprising means for copying an architected state of each of the at least two processors to the idle processor unit. Safford's method comprises receiving loss of lockstep signal from a processor unit, receiving a notice from the processor unit experiencing loss of lockstep to take it offline; moving the architected state of the processor unit experiencing loss of lockstep to a spare unit, wherein the spare unit becomes an active processor. (See Safford, lines 13-57 of column 2).

Safford discloses that at some future time, the processor may recover from the loss of lockstep, and lockstep operation of the processors may be restored. (See *Id.*, lines 41-51 of column 3).

Marisetty

Marisetty qualifies as prior art under pre-AIA 35 USC § 102(b).

Marisetty teaches a multiprocessor system comprising a non-volatile memory that stores an error handling routine which each of the processors may access when detecting an error. The processor detecting the error may signal other processors in the system to enter a "rendezvous state". (See Marisetty, ¶ 15). Marisetty discloses certain system errors can be handled by different software layers comprising a processor abstraction layer (PAL), a system abstraction layer (SAL), and the operating system (OS), wherein the PAL and SAL together are known as firmware. (See *Id.*, ¶¶ 24 and 26). The processor detecting the error may perform error handling then release the other processors from the rendezvous state. (See *Id.*, ¶ 25). The processor performing the error handling may be referred to as a monarch processor which is assigned by the system or determined each time the system needs to enter the rendezvous state. (See *Id.*, ¶ 43).

Cepulis

Cepulis qualifies as prior art under pre-AIA 35 USC
§ 102(b).

Cepulis teaches a method for booting a multiprocessor system. Cepulis's method assigns logical CPU designations among the multiple CPUs with a booting CPU being assigned/re-assigned based on prior errors on that CPU. (See Cepulis, lines 13-17 of column 1). When a multiprocessor system is powered up, all of the CPUs except for the CPU in physical slot 0 (CPU P0) are initially put into a sleep mode while CPU P0 performs its power on self-test (POST) procedures. The POST procedures include reviewing error logs and testing the other processors and associated caches. If there were no prior errors and the CPU functions properly, it is designated as CPU L0 and the other processors are then awakened. If there was a prior error or the CPU P0 does not function properly, it is designated as inoperative and CPU P1 is awakened and the testing procedures are repeated. If CPU P1 functions properly, it is designated as CPU L0. If CPU P1 does not function properly it is also designated as inoperative and CPU P2 is awakened and the process continues. If at least one CPU functions properly the system boots and operates. (See *Id.*, lines 30-64 of column 2).

As shown above in SNQ 2, Safford in view of Marisetty is seen as raising a SNQ over dependent claims 9-12, so it follows that Safford in view of Marisetty and further in view of Cepulis would also raise a SNQ over claims 9-12.

Furthermore, as shown above, the combination of Safford and Marrietty can also be reasonably interpreted as teaching

idling a lockstep pair of processors for which loss of lockstep has been detected (see Safford, lines 55-67 of column 2).

triggering an operating system to idle processors in a multiprocessor system when errors in the system are detected (see Marisetty, ¶¶ 37, 38, and 42).

These teachings are significant because they include the limitations in independent claim 23 specifically argued by the Applicant as missing from the applied prior art just prior to the claim being found allowable during the original prosecution of the '958 Patent.

Safford was considered during the original prosecution of the '958 Patent, however Safford was never viewed in combination with Marisetty and/or Cepulis, therefore Safford in view of Marisetty and further in view of Cepulis is a new combination of references. Moreover, there is a substantial likelihood that a reasonable Examiner would consider these teachings important in deciding the patentability of the '958 Patent. For those

reasons, Safford in view of Marisetty and further in view of Cepulis is found to raise a SNQ over independent claim 23. Additionally, since dependent claims carry with them each of the limitations of the claim(s) from which it depends, it follows that Safford in view of Marisetty and further in view of Cepulis also raises a SNQ over claims 24 and 25.

35 U.S.C. 325(d)

35 USC 325(d) states in part that "[i]n determining whether to institute or order a proceeding under this chapter, chapter 30, or chapter 31, the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.". Thus, in order for the Director to exercise discretion as to whether to Order a reexamination proceeding under chapter, 30, the request must first be determined to be based on the same or substantially the same prior art or arguments that previously were presented to the Office.

A review of the post grant history of the '198 patent indicates that the patent is the subject of a single Office post grant challenge filed after the filing of the instant *ex parte* reexamination request (90/019,245).

On September 8, 2023 (after the filing of this *ex parte* reexamination request), Petitioner BMW of North America, LLC., filed a petition (IPR2023-01373) for *inter partes* review of claims 1-8 and 13-22 of the '198 patent which asserted the following grounds as raising a reasonable likelihood in prevailing (RLP):

RLP Ground	Claims	Basis	References
#1	1-8 and 13-22	35 USC 103(a)	Bigbee and Nguyen

As of the mailing date of this Order, there has been no decision on institution of the petition, issued by the Patent Trial and Appeal Board (PTAB).

A comparison between the prior art and arguments presented in the instant reexamination request and the later filed IPR petition indicates that at least ground presented in the reexam request is based on substantially the same prior art that was presented in the IPR petition. For instance, SNQ Ground #1 is substantially the same as that presented in the later filed IPR petition for ground #1. Presented SNQ Ground #1 in the reexamination request is over Bigbee alone, while RLP Ground #1 in the IPR petition is over Bigbee in combination with Nguyen. Because SNQ ground #1 is a subset of RLP ground #1, it is based on the substantially same prior art. However, because the request for reexam was filed before the petition for IPR, the

prior art and arguments were not "previously" presented to the Office relative to the art and arguments presented in the reexamination request, and thus the threshold under 325(d) for the Director to exercise discretion to reject the request is not met.

However, even if the 325(d) threshold was met, the Director would decline to exercise such discretion to reject the instant reexamination request in view of the following facts:

- 1.) The is no evidence that petitioner and third-party requester are the same real party-in-interest.
- 2.) The PTAB has yet to make any decision on institution with respect the prior art prior art presented in the pending IPR petition.
- 3.) There has been no finding of serial abusive Office challenges to the '958 patent.
- 4.) The instant reexamination request presents different arguments with respect to the assertions of unpatentability of the requested claims. As stated above, the third party requester asserts the Bigbee reference discloses all the limitations of the challenged claims, while in the pending IPR, petitioner presents arguments that a secondary reference, Nguyen, discloses some of the limitations.

In view of these facts, to the extent the threshold for exercising discretion under 325(d) is met, the Director declines to exercise discretion to reject this request.

Accordingly, *ex parte* reexamination is ordered in view of the determination that the request raises a substantial new question of patentability to the claims of the '198 patent.

Extensions of Time

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

Conclusion

ALL correspondence relating to this *ex parte* reexamination proceeding should be directed as follows:

Please mail any communications to:

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Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

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/ERON J SORRELL/
Primary Examiner, Art Unit 3992

Conferees:

/DEANDRA M HUGHES/
Reexamination Specialist, Art Unit 3992

/MICHAEL FUELLING/
Supervisory Patent Examiner, Art Unit 3992