UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

BMW OF NORTH AMERICA, LLC AND
ROBERT BOSCH LLC,

Petitioner

v.

FORAS TECHNOLOGIES LIMITED

Patent Owner

_____

Case IPR2023-01373

U.S. Patent No. 7,502,958 B2

_____

REMOTE ORAL DEPOSITION OF

MICHAEL C. BROGIOLI

WEDNESDAY, JULY 10, 2024

REPORTED BY:

DEBRA A. DIBBLE, FAPR, RDR, CRR, CRC, Notary Public

JOB NO.: 9433

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Exhibit 2009 - Page 1

1

2 REMOTE ORAL DEPOSITION OF MICHAEL C. BROGIOLI,
3 produced as a witness at the instance of the Patent
4 Owner and duly sworn, was taken in the above-styled
5 and numbered cause on the above-referenced date,
6 from 9:58 a.m. to 1:25 p.m. EDT, before Debra A.
7 Dibble, CSR, CCR, RDR, CRR, Fellow of the Academy of
8 Professional Reporters, Notary Public, reported
9 remotely by realtime stenographic means at the
10 location of the witness, Finnegan, Henderson,
11 Farabow, Garrett & Dunner LLP, 1875 Explorer Street,
12 Suite 800, Reston, Virginia.
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Exhibit 2009 - Page 2

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Exhibit 2009 - Page 3

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Foras Technologies Ltd.
Exhibit 2009 - Page 4

1 INDEX

2

3 APPEARANCES 3

4 PROCEEDINGS 7

5

6 EXAMINATION OF MICHAEL C. BROGIOLI:

7 BY MR. PETRSORIC 7

8

9 CERTIFICATE 92

10

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edb0f9b5-7d9f-4eb0-98be-e9cd13090142
Foras Technologies Ltd.
Exhibit 2009 - Page 5

1 DEPOSITION EXHIBITS

NUMBER	DESCRIPTION	PAGE
Exhibit 1001	United States Patent No. US 7,502,958 B2	16
Exhibit 1002	Declaration of Dr. Michael C. Brogioli	11
Exhibit 1005	United States Patent Application Publication US 2003/0126498 A1 (Bigbee)	28

edb0f9b5-7d9f-4eb0-98be-e9cd13090142
Foras Technologies Ltd.
Exhibit 2009 - Page 6

1 ----------

2 P R O C E E D I N G S

3 July 10, 2024, 9:58 a.m. EDT

4 ----------

5 COURT REPORTER: Due to the nature of

6 remote reporting, please pause briefly before

7 speaking to ensure all parties are heard

8 completely.

9 All parties to this deposition are

10 appearing remotely and have agreed to the

11 witness being sworn in remotely, which I will

12 do now if there are no objections to my doing

13 so.

14 ----------

15 MICHAEL C. BROGIOLI,

16 having been duly sworn,

17 testified as follows:

18 ----------

19 EXAMINATION

20 ----------

21 BY MR. PETRSORIC:

22 Q. Good morning, Mr. Brogioli.

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Exhibit 2009 - Page 7

1 A. Morning.
2 Q. Would you please state your full name for
3 the record.
4 A. Yes. It's Michael Charles Brogioli.
5 Q. And how many times approximately have you
6 been deposed before?
7 A. In the 50 range, maybe 55, something like
8 that.
9 Q. And do you understand during this
10 deposition that the court reporter is here to record
11 both the questions I ask and your answers to those
12 questions?
13 A. Yes, I do.
14 Q. Do you understand that your answers
15 should be given out loud and in words so that the
16 court reporter can take them down?
17 A. Yes.
18 Q. Where are you presently?
19 A. In Finnegan's office in Reston, Virginia.
20 Q. Is anybody with you?
21 A. Yes. Three of the attorneys are.
22 Q. And who are those attorneys?

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Exhibit 2009 - Page 8

1 A. Kara Specht, I believe is her last name;
2 Xirui Zhang is her last name; and Lionel --
3 THE WITNESS: I'm forgetting your
4 last name, sorry.
5 MR. LAVENUE: Lavenue.
6 THE WITNESS: Lavenue. Thank you.
7 BY MR. PETRSORIC:
8 Q. What type of device are you running for
9 this deposition?
10 A. It's -- looks like -- so it was set up by
11 IT. It looks like a Dell laptop with an external
12 monitor and a webcam, and then there's a microphone
13 to my right.
14 Q. Are there any communication programs
15 running besides Zoom?
16 A. Not that I'm aware of, no.
17 Q. Do you have any notes or documents with
18 you today?
19 A. No notes. I have documents that are just
20 clean hard copies of my declaration, and then the
21 exhibits that went along with it.
22 Q. Can you tell me which exhibits?

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Exhibit 2009 - Page 9

1 A. Sure. It's -- I'll show you a picture of
2 it here. It's a -- it should be all of the
3 references that are in my -- I think it's in my
4 materials considered, it would be.
5 So the prior art references, ACPI
6 references, things like that.
7 Q. Are there any notes, annotations or other
8 markings on any of those documents?
9 A. No, there are not.
10 Q. Do you understand you are expected to
11 tell the truth today?
12 A. Yes, I do.
13 Q. Along these lines, is there any reason
14 today, medical or otherwise, that would prevent you
15 from being able to tell the truth?
16 A. No.
17 Q. Dr. Brogioli, since you have paper
18 copies, I'll let you decide as to how you'd like to
19 refer to the various exhibits, but I will upload
20 them in the chat for at least the court reporter to
21 have an electronic copy. And you can retrieve them
22 from the chat as well.

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Foras Technologies Ltd.
Exhibit 2009 - Page 10

1 I'd like to introduce first Exhibit 1002,
2 which is entitled the Declaration of Dr. Michael C.
3 Brogioli. I'm going to place that in the chat now
4 so that everybody has access to it.
5 A. So in this first one, I'll probably --
6 I'm not sure where it's going to download them to on
7 this computer, so it might take me a second.
8 Q. Understandable. I'll let you know when I
9 have got it up there so you can start to look.
10 (Brogioli Deposition Exhibit 1002
11 marked.)
12 BY MR. PETRSORIC:
13 Q. Okay, I've just sent it. Can you let me
14 know when you're able to see it?
15 A. Okay, yep, I've got it up here on this
16 computer.
17 Q. Okay. And again, if you'd like to refer
18 to the hard copy, please feel free.
19 If you would turn to section Roman
20 numeral IX.B of your declaration. And that starts
21 at page 47 of 96.
22 A. Okay.

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Exhibit 2009 - Page 11

1 Q. And in paragraph 80, in the first
2 sentence you state that: At the time of the '958
3 patent, a known problem in the art was addressing
4 errors, causing loss of lockstep in a lockstep pair
5 of processors that were both recoverable and
6 non-recoverable.
7 Correct?
8 A. That's correct, yes.
9 Q. Can you tell me what a recoverable error
10 is?
11 A. There's a number of examples in prior art
12 that I mention in my declaration, but it may be
13 something that, for example, an example would be if
14 you're loading data from a cache that may have had a
15 bit error, they can be corrected maybe via ECC bits
16 or things like that, and then the system can
17 continue computing without suffering data corruption
18 or things like that.
19 Q. Can you tell me what a non-recoverable
20 error is?
21 A. I would say at a high level, just as a
22 number of the prior art references talked about,

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Exhibit 2009 - Page 12

1 cases where things, various of the processors are
2 out of lockstep, and lockstep can't be resumed and
3 actions need to be taken before things are corrupted
4 in the system.
5 Q. And when you say actions need to be
6 taken, what do you mean?
7 A. Just the general idea that if -- if the
8 computer's allowed to continue operating, this -- an
9 example is perhaps bad data might end up elsewhere
10 in the system causing further problems or data
11 corruption issues, availability issues and so forth.
12 Q. What would the -- what would be an
13 example of the actions that would be taken?
14 MS. ZHANG: Objection, form.
15 A. What -- you're asking what actions would
16 be taken in which scenario?
17 BY MR. PETRSORIC:
18 Q. In the non-recoverable error scenario.
19 A. I guess I would point us back to the
20 Nguyen reference that talks about detecting --
21 detecting a scenario like that, and then, as I
22 believe Nguyen says, the restarting of the system.

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Exhibit 2009 - Page 13

1 Or resetting, rather.
2 Q. So the resetting of the system would be
3 the action that would be taken in the example you
4 just gave?
5 A. That's, as I recall, one of the scenarios
6 that the Nguyen reference talks about.
7 Q. In the second sentence of paragraph 80 of
8 the declaration, you state that: A person of
9 ordinary skill in the art would have understood that
10 a complete and robust system would be able to handle
11 both recoverable (e.g., soft errors) and
12 non-recoverable errors (e.g., mismatch errors).
13 Correct?
14 A. That's correct.
15 Q. And as an example of a recoverable error,
16 you identify soft errors, correct?
17 A. That's an example I give, that's right.
18 Q. What's a soft error?
19 A. So I -- I would consider that something
20 like -- and what the patent talks about, if I go
21 back to, I guess, columns 1 and 2 of the patent.
22 [Document review.]

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Exhibit 2009 - Page 14

1 A. I'm going back through, I guess, columns
2 2 to 3 to see if it's in the patent that the
3 language "soft error" is used.
4 But an example of that would be, I would
5 say, similar to what I was mentioning earlier, where
6 there may be a bit -- a digital bit within a
7 processor that has -- is the wrong value, but that
8 can be corrected, perhaps internally, using parity
9 bits or things like that. And execution can
10 continue.
11 BY MR. PETRSORIC:
12 Q. And just for purposes of logistics, when
13 you're referring to the patent, are you referring to
14 the '958 patent?
15 A. Yes, that's correct.
16 Q. And that's Exhibit 1001, correct?
17 A. That is correct.
18 Q. For complete purposes, let me upload
19 Exhibit 1001 into the chat so both you and the
20 reporter have an electronic copy.
21 Okay, it's on its way.
22 A. Okay.

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Exhibit 2009 - Page 15

1 (Brogioli Deposition Exhibit 1001
2 marked.)
3 BY MR. PETRSORIC:
4 Q. Could you let me know that you've
5 received it?
6 A. I have it, yes.
7 Q. Referring back to the soft errors we were
8 just discussing, how would a soft error in the
9 example that you gave be detected?
10 A. I think we'd need to be a bit more
11 specific about a specific scenario, but an example
12 being a cache line that has a bit that's -- that has
13 been flipped to the incorrect value, let's say a 0
14 to a 1, and something that can be corrected by an --
15 error correction codes or ECC codes that are part of
16 the cache, they can correct that in a passive
17 manner, so to speak.
18 Q. What do you mean by a passive manner?
19 MS. ZHANG: Objection, foundation.
20 A. Just generally speaking, you -- the bits
21 that are sort of added on to the data bits in this
22 cache line example can be used to figure out if a

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Exhibit 2009 - Page 16

1 bit needs to be switched and corrected.
2 BY MR. PETRSORIC:
3 Q. And when you say the data bits that are
4 added -- strike that.
5 When you say the bits that are added on
6 to the data bits, are you referring to the parity
7 bits you also referenced earlier?
8 A. In this, yeah, high-level scenario, yes,
9 you've got an extra set of bits that aren't data
10 that, let's say, your program is using, but they're
11 there and added on to correct errors that might be
12 present in the cache data.
13 Q. And the error correction, is that
14 considered a recoverable error scenario?
15 MS. ZHANG: Objection, form.
16 A. I guess I would say just generically
17 speaking, if someone was considering a bad bit in an
18 L1 cache line as an error and some parity
19 information is used to correct that, that would be a
20 way of correcting the bad bit.
21 BY MR. PETRSORIC:
22 Q. Let me circle back to my previous

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Exhibit 2009 - Page 17

1 question. In the example of the soft error that you
2 gave, how would the soft error be detected?
3 MS. ZHANG: Objection, asked and
4 answered.
5 A. I would say we'd need to probably look at
6 a specific solution or implementation, but typically
7 that extra parity information is used to either
8 detect the issue in this cache line example or
9 correct it. There's -- that type of concept is used
10 in many areas of computing.
11 Just like the patent talks about, there's
12 places where you can use it and then it's -- the
13 '958 also talks about you can't ECC protect
14 everything either. But it's used in
15 telecommunications and other areas as well. It
16 would depend on the system as to how you or how a
17 designer wanted to go about doing that.
18 BY MR. PETRSORIC:
19 Q. And that would be -- would that include
20 using the parity bits to determine if there was an
21 error in the data bits?
22 MS. ZHANG: Objection, form.

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Exhibit 2009 - Page 18

1 A. I would say sort of in this generic
2 example, yes, you can use parity information to see
3 if there's -- if there's some bits that are
4 erroneously set.
5 BY MR. PETRSORIC:
6 Q. And do I understand from your testimony
7 that using the parity bits to see if there are some
8 data bits that are erroneously set, some of -- in
9 certain instances, those erroneously set bits may be
10 corrected?
11 A. It sounds like you're asking about just
12 what the patent -- the '958 patent talks about in --
13 in, I guess, starting around the top of column 2 at
14 5, where it says: Parity/ECC mechanisms have been
15 employed extensively for caches, memory, and similar
16 data storage arrays -- or just, you know, arrays in
17 a computer where we keep bits and bytes of
18 information.
19 Q. I don't think that was exactly my
20 question. I'm just trying to determine if there are
21 parity -- if parity bits indicate an error in the
22 data bits, is that error correct -- always

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Exhibit 2009 - Page 19

1 correctable?
2 A. I guess it would -- it depends on how
3 you're using parity bits. You may have a system
4 that uses them to detect an error or perhaps detect
5 and correct, or depending on how you designed your
6 system or the number of bits or correction bits,
7 maybe there's too much corruption to correct, so it
8 would -- there's, I guess, some variability there in
9 terms of how a system designer or implementer would
10 want to use them.
11 Q. So with respect to lockstep errors, would
12 a soft error include a scenario where the parity
13 bits cannot be used to correct the data bit errors?
14 MS. ZHANG: Objection, form.
15 A. Let me hear your question one more time?
16 BY MR. PETRSORIC:
17 Q. Sure.
18 With respect to lockstep errors, and
19 specifically with respect to a soft error, would
20 that include a scenario where the parity bits cannot
21 be used to correct the data bit errors?
22 A. I mean, this sounds like somewhat of a

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Exhibit 2009 - Page 20

1 hypothetical that I -- I haven't addressed in my
2 declaration, but if we had a cache for a processor,
3 the uppermost layer 1, let's say, and there are --
4 it's a -- let's say a 64-bit cache line, and eight
5 bits of parity or something, and there was some sort
6 of catastrophic soft error that corrupted a large
7 number of bits in the cache line, it -- you know,
8 depending on how your algorithms are set up, that
9 might result in something that can't be corrected by
10 parity bits. It would depend on the system or
11 implementation.
12 Q. In the second sentence of paragraph 80 of
13 your declaration you also give an example of
14 non-recoverable errors as a mismatch error, correct?
15 A. That's correct.
16 Q. What is a mismatch error?
17 A. So just as I discuss in my declaration,
18 if we have two CPUs that are operating in lockstep,
19 as I talked about, and they start to -- so in
20 lockstep, producing the same instruction stream, and
21 then there -- you observe that they start to produce
22 different results for, let's say, the same

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Exhibit 2009 - Page 21

1 arithmetic add instruction, there's a mismatch going
2 on between the two processors because they should be
3 producing the same result.
4 And that can be an example of a
5 non-recoverable error here that if you let this
6 machine keep going on computing, it would result in
7 a lot of undesirable behavior, corruption, things
8 like that. Data corruption, things like that.
9 Q. Are all mismatch errors non-recoverable
10 errors?
11 MS. ZHANG: Objection, form.
12 A. I think even the prior art references and
13 perhaps Nguyen talk about various ways of handling
14 non-recoverable errors.
15 I'm done with my answer. I'm just
16 flipping through my declaration.
17 BY MR. PETRSORIC:
18 Q. Okay. So is a mismatch error always a
19 non-recoverable error?
20 A. So I'm going back to, I guess,
21 paragraph 47 of my declaration, just revisiting.
22 [Document review.]

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Exhibit 2009 - Page 22

1 A. So here, I guess in 48, we can start.
2 And I talk about the Safford reference. And Safford
3 talks about a scenario where, as is shown in the
4 Figure 2 here on page 27, there's two CPUs, and an
5 error is detected in one of these processors. And
6 the lockstep can be recovered here in this scenario.
7 And in that scenario, that's before the mismatch
8 gets detected and signaled by the mismatch detection
9 logic.
10 BY MR. PETRSORIC:
11 Q. Were you done with your answer,
12 Dr. Brogioli?
13 A. I was, yes.
14 Q. Okay. Then what about the instance where
15 the -- a mismatch is detected before an error is
16 detected in one of the two processors?
17 A. Can I hear you one more time? Just
18 before I continue reading?
19 Q. Sure.
20 In the instance where a mismatch is
21 detected before an error is detected in one of the
22 two processors, is that a non-recoverable error?

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Exhibit 2009 - Page 23

1 A. I'm not sure I'm fully understanding your
2 question. It sounded like you're asking if a
3 mismatch is detected before an error is detected.
4 Q. In your previous answer you mention that
5 where there's two CPUs and an error is detected in
6 one of those processors, lockstep can be recovered
7 if, in that scenario, it happens before the mismatch
8 gets detected, correct?
9 A. That sounds like what I have said, yes.
10 Q. And I'm asking if a mismatch gets
11 detected before an error in one of the two
12 processors gets detected, whether that would be a
13 non-recoverable error.
14 MS. ZHANG: Objection, form.
15 A. It sounds like you're asking if -- I
16 guess I'm -- I'll stick sort of within this page 27
17 of my declaration. If there is a mismatch error --
18 so if I'm understanding your question or para- --
19 sort of echoing it back, you're asking about a
20 mismatch error detected, or the signal being
21 generated and detected before an error is detected
22 in an individual processor. That sounds like a

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Exhibit 2009 - Page 24

1 scenario -- I'm not sure that's a scenario I talk
2 about in my declaration. Or feel free to point me
3 to it if I do.
4 BY MR. PETRSORIC:
5 Q. I'm just trying to determine,
6 Dr. Brogioli, if it's your opinion that a mismatch
7 error is always a non-recoverable error.
8 A. I guess we'd need to go back and look at
9 a specific reference. But there are mismatch --
10 there are errors that can occur within one of the
11 processors, and then an error that can be generated
12 as a mismatch error or mismatch detected error, and
13 then handling in various ways.
14 If you're asking about something that may
15 detect that and try and do something like unwinding
16 instruction streams or something, I don't recall
17 discussing that in my declaration.
18 Q. If you look ahead to paragraph 81 of your
19 declaration, which is on page 47 of 96.
20 A. Okay.
21 Q. The first sentence -- in the first
22 sentence you say: Bigbee discloses detecting errors

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Exhibit 2009 - Page 25

1 within a lockstep pair of processors using FRC logic
2 including detecting both recoverable (e.g., soft
3 errors) and non-recoverable errors (e.g., mismatch
4 errors when the processor causing the error cannot
5 be determined).
6 Do you see that?
7 A. Yes.
8 Q. So what do you mean by "mismatch errors
9 when the processor causing the error cannot be
10 determined"?
11 A. So I'll go back to this paragraph in
12 Bigbee for us, if -- or I can wait for you to
13 introduce it, however you prefer to do it.
14 Q. I can -- I can introduce Bigbee, but I'm
15 also -- I'm also trying to understand what you mean
16 by this particular example of non-recoverable errors
17 in the first sentence of paragraph 81 of your
18 declaration where you state that: A
19 non-recoverable -- an example of a non-recoverable
20 error is a mismatch error when the processor causing
21 the error cannot be determined.
22 A. Sure. So I'm just going to jump back to

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Exhibit 2009 - Page 26

1 this paragraph in my hard copy.
2 [Document review.]
3 A. Right. So there's -- so the last
4 sentence on that -- in paragraph 33 on the leftmost
5 column where it says: FRC logic 308 monitors
6 processor core store operations or "writes" to
7 shared cache 306 to detect inconsistencies in the
8 generated results which indicate an FRC mismatch
9 error.
10 And so going back to this sentence you
11 were asking about in my declaration, in which I
12 state: Mismatch errors when the processor causing
13 the error cannot be determined -- this is a scenario
14 where there's the two processor cores, or two
15 processors, they're mismatching. I don't know
16 who -- or I being the FRC checker logic, doesn't
17 know -- it knows the two of them are different, but
18 it doesn't know who is right or wrong. And so that
19 results in the non-recoverable error I'm talking
20 about here.
21 BY MR. PETRSORIC:
22 Q. If the FRC logic was able to determine

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Exhibit 2009 - Page 27

1 which of the processors was right or wrong, would
2 that result in a non-recoverable error?
3 A. I don't recall analyzing that scenario in
4 my declaration. That doesn't sound to me like
5 something that Bigbee was contemplating.
6 I would say -- I'll add on to that.
7 Given the way that, for instance, Bigbee and Nguyen
8 talked about the Itanium processors and, I guess,
9 how those systems were designed to operate in FRC
10 scenarios.
11 Q. For logistics purposes, let me upload
12 Bigbee, which is Exhibit 1005, into the chat.
13 (Brogioli Deposition Exhibit 1005
14 marked.)
15 BY MR. PETRSORIC:
16 Q. Okay, I have sent it. Can you let me
17 know if you have received it?
18 A. Okay.
19 Q. And if you would turn to page 8 of this
20 exhibit, 1005, in paragraph 19.
21 A. Okay.
22 Q. The third sentence of paragraph 19 reads:

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Exhibit 2009 - Page 28

1 FRC logic detects errors within individual processor
2 cores of the described embodiment which causes
3 hardware 102 to break lockstep between at least two
4 processor cores within a processor package,
5 disabling FRC mode operation.
6 Do you see that?
7 A. I see that sentence, yes.
8 Q. A moment ago you stated that Bigbee
9 doesn't teach that the FRC logic detects errors
10 within individual processor cores, correct?
11 MS. ZHANG: Objection, form.
12 A. I'm just revisiting this paragraph.
13 [Document review.]
14 A. Right. That's what I was saying earlier
15 when we were referring to that sentence in my
16 declaration and I was, I think, reading from that
17 paragraph 33.
18 BY MR. PETRSORIC:
19 Q. Paragraph 33 indicates that the FRC logic
20 detects inconsistencies in the generated results
21 which indicate an FRC mismatch error. Correct?
22 A. Is that the FR -- this is in

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Exhibit 2009 - Page 29

1 paragraph 33. That the FRC logic is monitoring the
2 writes to a shared cache in this description, and
3 checking for inconsistencies in those generated
4 writes to see if there's an FRC mismatch error.
5 Q. Does the FRC logic also check to see
6 which processor was in -- which processor might be
7 in error?
8 MS. ZHANG: Objection, form.
9 A. I don't see that in paragraph 33 of
10 Bigbee, which is what I was referring to in my
11 declaration. I don't see that that's described.
12 BY MR. PETRSORIC:
13 Q. Is that described in paragraph 19 of
14 Bigbee?
15 A. So I'm reviewing 19 and a bit of the
16 surrounding language right now.
17 [Document review.]
18 A. So it -- just as paragraph 19 states, it
19 looks like it's saying within this embodiment, the
20 hardware 102, I guess at Figure 1, includes FRC
21 logic, and that FRC detects errors within individual
22 processor cores of this embodiment, which causes

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Exhibit 2009 - Page 30

1 hardware 102 in Figure 1 to break lockstep between
2 at least two processor cores within a processor
3 package, and disables that FRC mode operation.
4 And then it looks like it's saying that
5 same hardware 102, it disables the package's
6 error-containing core and puts it into what Bigbee
7 refers to as a zombie state, and then generates a
8 machine check exception, which then that machine
9 check exception goes off and causes execution of
10 some processor error handler within the PAL or
11 processor extraction layer of the error-free core.
12 BY MR. PETRSORIC:
13 Q. So just to be clear, the FRC logic
14 described in paragraph 19 does detect which
15 processor might be in error, correct?
16 A. I'm just revisiting paragraph 20 as well,
17 and then I'll answer.
18 [Document review.]
19 A. So I'll start my answer going back to 19,
20 and then jump to 20.
21 So the paragraph 19 says: FRC logic
22 detects errors, and here within an individual core,

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Exhibit 2009 - Page 31

1 and breaks lockstep, and then, as I said, disables
2 the erroneous or the error-containing cores, goes
3 into zombie state, executes the PAL functionality.
4 And then in 20, it's saying that there's
5 error handling code in the system extraction layer
6 that runs, and that initiates a platform-independent
7 removal sequence to just pull these processors. And
8 so this whole just removal scenario starts in 19
9 with the FRC logic that seems to be describing
10 detecting some sort of fault in one -- one of the
11 processor cores.
12 BY MR. PETRSORIC:
13 Q. And is this description in paragraph 19,
14 in your opinion -- strike that.
15 In your opinion, is the description in
16 paragraph 19 relating to a recoverable error?
17 MS. ZHANG: Objection, form.
18 A. It looks like 19, when -- when we follow
19 through the whole process described here into at
20 least paragraph 20, is just seeing an error and then
21 disabling hardware and removing it from the system.
22 * * *

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Exhibit 2009 - Page 32

1 BY MR. PETRSORIC:
2 Q. Is that a recoverable -- do you consider
3 that a recoverable error or non-recoverable error?
4 A. In the context that a CPU or logical
5 processor is just being removed, that seems to be
6 something that's not really handled one way or the
7 other. Things are just disabled and left inoperable
8 within the box that's the larger computer.
9 Q. Regardless of how Bigbee reacts to the
10 error, is that error that's described and detected
11 by the FRC logic in paragraph 19, do you consider
12 that a recoverable error or a non-recoverable error?
13 MS. ZHANG: Objection, foundation.
14 A. I would say that, in this scenario, the
15 FRC of 19 detects an error that's occurred, and then
16 proceeds to kick off the SAL and PAL -- I guess the
17 PAL and then SAL logic -- to remove the, not just
18 the core but the overall processor package from the
19 computer itself. So both physical cores, or
20 whatever physical cores are in the logical package,
21 and then that's just not a -- that functionality, or
22 that logical processor is just no longer available.

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Exhibit 2009 - Page 33

1 BY MR. PETRSORIC:
2 Q. So do you consider that a non-recoverable
3 error?
4 MS. ZHANG: Objection, form.
5 A. I'm not sure -- so I talk -- in my
6 declaration I talk about recoverable and
7 non-recoverable errors in the confines of the Bigbee
8 and Nguyen references. Here is more of a scenario
9 of something is in error, just remove it and leave
10 it nonfunctional. Or as Bigbee says, just put it in
11 a zombie state. You're not getting any availability
12 from that hardware. It's not coming back for use to
13 run threads or things like that.
14 BY MR. PETRSORIC:
15 Q. After that first sentence in paragraph 81
16 of your declaration, you cite paragraph 33 of
17 Bigbee, correct?
18 A. That's correct.
19 Q. And if we look at paragraph 33, which is
20 on page 10 of Bigbee --
21 Can you let me know when you're there?
22 A. I'm there.

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Exhibit 2009 - Page 34

1 Q. In the first sentence it states: In one
2 embodiment, the first and second processor cores
3 302a-b within the depicted processor package 204a
4 may be bound together to function as a single
5 logical processor from the point of view of
6 operating system software.
7 Do you see that?
8 A. Yes, I do.
9 Q. Now, this sentence references processor
10 cores 302a and 302b as well as the package 204a,
11 correct?
12 A. That's correct.
13 Q. And these processor cores in the package
14 are shown in Figure 3 of Bigbee, correct?
15 A. That's one example, yes. They're talked
16 about elsewhere.
17 Q. And as another example, they're described
18 with respect to Figure 3 in paragraph 32 of Bigbee,
19 correct?
20 A. That looks right, Figure -- paragraph 32
21 talks about 302a and b and 204a.
22 Q. And the first sentence of paragraph 32 of

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Exhibit 2009 - Page 35

1 Bigbee indicates that Figure 3 illustrates an
2 exemplary block diagram of processor package 204a of
3 Figure 2, according to one embodiment of the present
4 invention. Correct?
5 A. That's correct.
6 Q. And then the second sentence of
7 paragraph 32 of Bigbee recites: In the illustrated
8 embodiment, a processor package 204a may be coupled
9 to a shared "front side" bus 205a, and may include
10 functional redundancy check (FRC) logic 308, a
11 shared cache memory 306, and a first processor core
12 302a, and a second processor core 302b, each having
13 an associated private cache memory 304a and 304b
14 respectively.
15 Do you see that?
16 A. Yes.
17 Q. Can you tell me what the front side bus
18 205a is?
19 A. This is a bus -- let me start over. I
20 can answer it more concisely.
21 So referring back to Figure 3, there's
22 the two processor cores 302a and b. They each have

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Exhibit 2009 - Page 36

1 a private cache, which is a little, small, fast --
2 very fast memory that only they can talk to, I
3 guess, directly, and then there is a shared cache
4 below that. And all of this stuff is within the
5 package. Or the processor package.
6 And then the package itself, you know, if
7 it wanted to talk to, for -- or send something, for
8 example, to the network port on your computer or a
9 hard drive or something, has to go over that 205a
10 front side bus to send information or data, or
11 receive elsewhere in the system.
12 Q. You mentioned the two processor cores
13 each having a private cache. Just to confirm,
14 processor core 302a has private cache 304a and
15 processor core 302b has private cache 304b, correct?
16 A. In Figure 3, that's correct, yes.
17 Q. There's also the shared cache memory 306,
18 correct?
19 A. That's correct.
20 Q. What is the shared cache memory?
21 A. That is a memory that can contain data or
22 instructions or -- we'll just stick with data for

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Exhibit 2009 - Page 37

1 simplicity -- that's either used by one or perhaps
2 both of the processors. So it's kind of a bigger
3 bucket of memory, bigger in terms of storage size,
4 that can contain information for both cores kind of
5 thing.
6 Q. And then there's the functional
7 redundancy check FRC logic 308, correct?
8 A. That's correct.
9 Q. And the FRC logic is also discussed in
10 the second sentence of paragraph 33, correct?
11 A. That's correct, yes.
12 Well, I -- sorry, yes, that's correct,
13 FRC logic 308.
14 Q. And that second sentence reads: Both
15 cores 302a and 302b operate in an FRC mode in which
16 identical instructions may be provided to each core
17 and concurrently executed on identical data using
18 FRC logic 308. Correct?
19 A. I think you said using FRC logic, and it
20 says utilizing, but otherwise, yes, that's right.
21 Q. What is FRC mode?
22 A. I'm going to go back through Bigbee to

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Exhibit 2009 - Page 38

1 see where he states that, just so I'm not confusing
2 Bigbee with another prior art reference.
3 [Document review.]
4 A. I see -- I'm jumping back to Bigbee,
5 paragraph 27, and that third sentence starting at
6 the bottom of the left-hand column: In one
7 embodiment, each of the illustrated processor
8 packages includes a pair of processor cores operable
9 in an FRC mode as a single logical processor.
10 So I think -- and Bigbee may elaborate on
11 that a little earlier in its specification, but I
12 think Bigbee is talking about this is a mode of
13 operation where we have those two cores, for
14 example, and they're operating as one logical
15 processor to the operating system.
16 Bigbee also talks about the FRC mode, it
17 looks like, in paragraph 2.
18 Yeah, he also states, about halfway down
19 paragraph 2: Operated in a functional redundancy
20 check FRC mode in which identical instructions are
21 provided to each core and concurrently executed on
22 identical data...

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Exhibit 2009 - Page 39

1 BY MR. PETRSORIC:
2 Q. Is it fair to say that the FRC mode is
3 where the processor cores are considered running in
4 lockstep?
5 A. I would say that the intention of turning
6 FRC mode on is to have those two, I'll call them
7 physical cores, running in lockstep and presenting
8 themselves within that package as the one logical
9 core.
10 Q. And that would be as opposed to a
11 multiprocessing mode where each of the cores is
12 operating independently?
13 A. Yeah. So I was looking to see if Bigbee
14 actually states that. I think one of the other
15 prior art references does. But generally, that
16 sounds right. If you aren't in FRC mode, you could
17 use -- in a system, you might be able to use each of
18 the physical cores as its own non-FRC-checking
19 separate processor with its own stream of
20 computation on it.
21 Q. And just to check, back to paragraph 33
22 of Bigbee on page 10.

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Exhibit 2009 - Page 40

1 A. Mm-hmm.
2 Q. The fourth sentence reads: FRC logic 308
3 operates processor cores 302a-b as a single logical
4 processor by concurrently providing each with
5 identical data and instructions.
6 Is that consistent with your
7 understanding of lockstep operation?
8 A. That looks in line with the lockstep
9 operation we've been talking about, where each --
10 the -- in this scenario, the two processors get the
11 same instruction streams and operate as a -- one
12 logical processor.
13 Q. The fifth sentence refers to: Each
14 processor core 302a-b executing instructions and
15 processing data to generate results, which may then
16 be stored within an associated private, e.g.,
17 304a-b, and/or shared, e.g., 306 cache.
18 Do you see that?
19 A. Yes.
20 Q. Can generated results be stored in both
21 the private and shared caches?
22 A. Sorry, can the what results be stored?

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Exhibit 2009 - Page 41

1 Q. The generated results that Bigbee is
2 referring to in the fifth sentence, can they be
3 stored in both the private and shared caches?
4 A. So it probably depends on -- I guess to
5 back up, so Bigbee Figure 3 illustrates an aspect of
6 Bigbee, or Bigbee's embodiment, where there's the
7 shared cache 306 and an FRC logic. And it's really
8 just showing high-level components.
9 When we go over to Figure 4A, which talks
10 about the same embodiment, it also -- and I'll point
11 us to block 404. It talks about detecting the error
12 within the processor of this plurality of
13 processors.
14 And so I guess we'd need to be more
15 specific in terms of what's sorted in cache.
16 If, for instance, if we're in Figure 4
17 and hardware -- if in block 404, the hardware
18 detects an error within the first processor and
19 disables that first processor core, I don't know
20 that that resultant -- let's say the result of its
21 write operation is making it to the L1 -- I'm sorry,
22 the first private cache or a shared cache, either

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Exhibit 2009 - Page 42

1 way.
2 Q. In the sixth sentence of paragraph 33,
3 Bigbee recites that: The FRC logic 308 monitors
4 processor core store operations or "writes" to
5 shared cache 306 to detect inconsistencies in the
6 generated results which indicate an FRC mismatch
7 error. Correct?
8 A. That's correct, yes.
9 Q. So this sentence is indicating that the
10 FRC logic is operating on data in the shared cache,
11 correct?
12 A. For this portion of Bigbee -- I apologize
13 for scrolling so much. I'm not used to the mouse
14 yet -- it's describing where there's an FRC logic
15 looking at the shared cache here. It's all --
16 Bigbee also talks about FRC logic monitoring into
17 these cores as well. But this sentence in 33 you're
18 referring to is the FRC logic looking at writes to
19 the shared cache 306.
20 Q. Does Bigbee describe the FRC logic
21 operating on data within each of the processor
22 cores?

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Exhibit 2009 - Page 43

1 MS. ZHANG: Objection, form.
2 A. That's what Bigbee talks about, at least
3 one example being in paragraph 35, where -- I'll
4 start with the second sentence of Bigbee 35: The
5 illustrated process begins (block 402) and
6 thereafter hardware (e.g. FRC logic) detects an
7 error within a first processor core of a plurality
8 of processor cores operating in an FRC mode as that
9 single logical processor we talked about.
10 BY MR. PETRSORIC:
11 Q. And does that sentence indicate where --
12 what data the FRC logic is operating on?
13 A. So I -- in paragraph 35, anyway, it's
14 stating the FRC logic is detecting an error within
15 the first processor core. I don't see in this
16 sentence or these couple of sentences if your
17 question is sort of what -- where is the FRC logic
18 sampling from or something like that. I don't see
19 that described in this sentence, anyway.
20 Q. In paragraph 33, the sixth sentence
21 indicates that: The FRC logic monitors processor
22 core store operation or "writes" to the shared cache

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Exhibit 2009 - Page 44

1 306. Correct?
2 A. In that portion of Bigbee, that's what
3 it's describing in relation to the way things are
4 illustrated in that Figure 3.
5 Q. Does Bigbee at all indicate the FRC logic
6 monitoring a processor core store operation or
7 writes to the private caches?
8 MS. ZHANG: Objection, form.
9 A. In that -- I don't see private cache
10 mentioned in that sentence, but when Bigbee starts
11 describing Figure 4 and the monitoring -- or the FRC
12 logic monitoring errors within one or the other of
13 the processor cores, it's monitoring core-specific
14 information. And that's just what's described in
15 Figure 4. Similar to how the other, I think Safford
16 and the other prior art references illustrate the
17 FRC block, if you will, sampling from the cores
18 themselves.
19 BY MR. PETRSORIC:
20 Q. But Bigbee does not give an express
21 disclosure of what particular data or operations
22 it's monitoring with respect to the determination of

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Exhibit 2009 - Page 45

1 errors within the processor cores, does it?
2 MS. ZHANG: Objection, form.
3 A. I would say it does. It talks about, for
4 instance in -- this mouse -- in 33. And that's, I
5 think you said the sixth sentence, that second line
6 from the bottom: FRC logic monitors processor core
7 store operations or "writes." Here it's talking
8 about a shared cache. Perhaps you would want to
9 monitor those same writes in paragraph 35 where
10 Bigbee's already talked about the processor writes,
11 when you're monitoring by the FRC logic for an error
12 in that first processor core.
13 BY MR. PETRSORIC:
14 Q. So you're indicating that Bigbee would
15 want to monitor the writes to the shared cache to
16 detect an error in the -- in the first processor
17 core.
18 MS. ZHANG: Objection, form.
19 A. I would say when Bigbee is describing
20 Figure 4a, it is -- the FRC logic is looking at an
21 error within the first processor core to determine
22 if the rest of these, you know, machine check

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Exhibit 2009 - Page 46

1 exceptions and so forth need to happen.
2 BY MR. PETRSORIC:
3 Q. Could Bigbee monitor the data and parity
4 bits in the shared cache to determine if there is an
5 error in one of the processor cores?
6 A. I don't see that Bigbee is talking about
7 monitoring the parity bits within the private data
8 cache in this paragraph 35.
9 Q. And Bigbee isn't talk -- Bigbee isn't
10 talking about monitoring the parity bits within
11 the -- strike that.
12 Does Bigbee describe monitoring anything
13 other than the shared data cache for errors?
14 A. So you're kind of misinterpreting what I
15 was saying earlier. Bigbee is saying in
16 paragraph 33, it is in -- in this paragraph, FRC
17 logic monitors processor core store operations or
18 writes to the shared cache.
19 Q. And besides this disclosure, does Bigbee
20 disclose the FRC logic monitoring any other store
21 operations or caches?
22 A. I guess I'll need to go back through

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Exhibit 2009 - Page 47

1 parts of Bigbee's specification to see what else it
2 says about -- to the extent it describes things
3 explicitly that the FRC logic would monitor for, I
4 guess, the description in Figure 4a.
5 MR. PETRSORIC: We've been going
6 about an hour, a little over an hour. Would
7 you like to take a break?
8 THE WITNESS: Sure.
9 (Recess taken, 11:08 a.m. to
10 11:22 a.m. EDT)
11 BY MR. PETRSORIC:
12 Q. Before the break, Dr. Brogioli, I had
13 asked you does Bigbee disclose the FRC logic
14 monitoring any other store operations or caches
15 other than to the shared data cache 306.
16 Do you recall that?
17 A. I recall that discussion and talking
18 about the processor core write operations and so
19 forth, yes.
20 Q. And you said you would need to go back
21 through parts of Bigbee's specification to see what
22 else it says about the FRC logic monitoring,

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Exhibit 2009 - Page 48

1 correct?
2 A. That's right. We were, I think, talking
3 about paragraph 35 and 4a, and I didn't recall from
4 memory what else Bigbee may have said about things
5 the FRC was monitoring. Explicitly, anyway.
6 Q. And so could you look back through
7 Bigbee, then, to see if you can identify any --
8 anything other than the core store operations or
9 writes to the shared cache?
10 A. Okay.
11 [Document review.]
12 A. So one -- I guess one thing I'll mention
13 is paragraph 19, which we discussed earlier, talks
14 about FRC mode for the processors Bigbee talks
15 about, so there may be additional information in
16 that documentation.
17 [Document review.]
18 A. I'm just continuing on through the
19 descriptions of this Figure 2 and so forth.
20 Yeah.
21 [Document review.]
22 A. Yeah, then in 33 it mentions -- it gets

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Exhibit 2009 - Page 49

1 more specific about the Intel architecture in FRC
2 mode. It mentions Itanium, which we talked about
3 earlier, and as I recall, there's FRC mode,
4 et cetera, on flavors of the pentium, the 32-bit
5 pentium. Then that same bottom of 33 says the FRC
6 logic monitors processor core store operations or
7 writes to shared cache, stores being a store with
8 data going to an address somewhere in the computer
9 to stick the data.
10 34 mentions the FRC logic implemented as
11 executable firmware or dedicated hardware coupled
12 with or incorporated into one or more of the
13 package's components. That, to me, says if you
14 could be -- I'll use the word "sampling," but you
15 could be sampling or monitoring information at
16 various places within the processor package, if you
17 want.
18 35 starts -- still talking about the FRC
19 logic. Bigbee's already established you can use
20 this FRC logic at various places in the package as
21 you want, and here it starts talking about
22 monitoring -- or detecting errors within the first

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Exhibit 2009 - Page 50

1 processor core itself.
2 I'm just continuing on.
3 [Document review.]
4 A. And then, you know, Bigbee here also --
5 we're talking about the FRC mode and firmware, and
6 the firmware of Bigbee is ACPI, and even paragraphs
7 30 -- I guess 35 talks about the SAL and PAL, which
8 are -- one is a processor layer, one is a system
9 layer, that are all part of the ACPI universe, and
10 so there's a whole ton of data you can monitor and
11 sample at those different layers in the system, that
12 it would seem -- a person of skill in the art would
13 understand implementing the FRC logic in that
14 firmware. There's a lot of things you could
15 monitor.
16 So yeah, it seems like it's describing
17 quite a bit.
18 BY MR. PETRSORIC:
19 Q. So it's your understanding that a person
20 of ordinary skill in the art reading Bigbee would
21 understand that the FRC logic could monitor data
22 beyond what's in the shared cache.

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Exhibit 2009 - Page 51

1 A. I guess I would phrase that differently,
2 that going back to the bottom of paragraph 33 of
3 Bigbee, I think it's that sixth sentence, Bigbee
4 says -- here's an example: The FRC logic monitors
5 processor core store operations or writes to the
6 shared cache, and then goes on to describe the FRC
7 logic can go in various places in the processor
8 package, and it's firmware that can be in ACPI,
9 slash, SAL, slash, PAL, and there's a lot of data
10 moving around through ACPI. Part of the reason why
11 we developed ACPI.
12 And so that there's a lot of things you
13 could potentially monitor there as part of your
14 implementation.
15 Q. So are you suggesting a person of
16 ordinary skill in the art would understand that the
17 FRC logic could monitor data that's in the private
18 caches?
19 MS. ZHANG: Objection, form.
20 A. I guess if -- I guess what I'm saying is
21 a person of skill in the art would understand that
22 this FRC logic of Bigbee can be done in firmware,

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Exhibit 2009 - Page 52

1 which, if they wanted, sort of in this kind of
2 hypothetical universe they would have access to,
3 good, bad, or otherwise, could look at processor
4 layer information or system layer information and
5 other data.
6 BY MR. PETRSORIC:
7 Q. And could that processor layer
8 information be monitored through the shared cache?
9 A. I guess I would answer that differently,
10 that one thing Bigbee seems to talk about in 33 is
11 the FRC logic monitors, the processor core, each of
12 those two physical cores writes to that shared cache
13 and looking for inconsistencies.
14 And that that -- those potential
15 inconsistencies here indicate the FRC mismatch.
16 Q. Would a person of ordinary skill in the
17 art understand that the -- that the data in parity
18 bits in the shared cache could be monitored to
19 determine whether there were errors within a
20 particular processor core?
21 MS. ZHANG: Objection, form.
22 A. You're asking in the shared cache?

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Exhibit 2009 - Page 53

1 BY MR. PETRSORIC:
2 Q. Yes.
3 A. Okay. I don't see that Bigbee's talking
4 about that. To me, at least in this paragraph 33,
5 Bigbee is saying, I'm looking at write operations
6 coming from each of these respective cores that make
7 up the logical core and seeing if there's a
8 difference between the write operations to the
9 shared cache.
10 Q. But that's to detect inconsistencies in
11 the generated results, which might indicate a
12 mismatch error, correct?
13 A. That's correct.
14 Q. But I'm also asking you, would a person
15 of ordinary skill in the art understand that the
16 shared data cache would also include parity bits in
17 addition to data bits?
18 A. Yes. So for a -- I'm trying to answer
19 you without going off into the weeds.
20 So for a given piece or a strip of data
21 in that shared cache, there may be parity bits
22 associated with that strip of data.

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Exhibit 2009 - Page 54

1 Q. And would a person of ordinary skill in
2 the art understand that the -- those parity bits may
3 be used to indicate errors within that strip of
4 data?
5 MS. ZHANG: Objection, form.
6 A. I guess getting away from Bigbee and just
7 talking about a cache line sitting in a shared
8 cache, there's going to be some parity bits that get
9 generated based on data, possibly the data going
10 into the cache line itself, or that's stored in that
11 strip of memory in the shared cache.
12 BY MR. PETRSORIC:
13 Q. And that could also be data that may have
14 been stored in the private cache of the individual
15 processor as well, correct?
16 MS. ZHANG: Objection, form.
17 A. That, I would say generally in cache
18 architecture, you can have -- there's a lot of
19 flavors to how people design this, depending on what
20 decade we're in and what type of computer, but, yes,
21 you can have data that's sitting in the small, fast,
22 private cache that's also present in the bigger,

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Exhibit 2009 - Page 55

1 slower, shared cache.
2 BY MR. PETRSORIC:
3 Q. And the -- with the data that's sitting
4 in both the private cache and the shared cache,
5 would a person of ordinary skill in the art
6 understand that if there are parity bits used for
7 the private cache, the parity bits would also
8 accompany the data in the shared cache?
9 A. I guess I would say if -- you know, if I
10 went home and grabbed my computer architecture book,
11 it would talk about reasons why you might want to
12 use parity bits in an L1 -- or a private cache, or
13 you might want to use them in a shared cache, or
14 both, or things like that.
15 I think they would understand those
16 concepts.
17 Q. Back to -- just circling back to the
18 sixth sentence of paragraph 33 and the core store
19 operations, are you understanding this sentence to
20 be disclosing that the FRC logic is monitoring the
21 core store operations to the shared cache?
22 A. If -- it looks like it's saying, for this

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Exhibit 2009 - Page 56

1 paragraph, that FRC logic is looking at writes
2 coming from those two cores that are operating on
3 the same instruction string, or supposed to be. And
4 seeing that those writes, as they move through the
5 cache hierarchy to the shared, the bigger, slower,
6 shared cache, let's say, are -- is the same thing
7 showing up. And if it's not the same thing, the FRC
8 logic is going to say, this is indicating an FRC
9 mismatch error.
10 Q. But do you understand this sentence of
11 Bigbee to be disclosing that the FRC logic is
12 monitoring only the operations to the shared cache?
13 MS. ZHANG: Objection, form.
14 A. I think Bigbee doesn't -- at least in
15 talking about Figure 3, doesn't get into a huge
16 discussion of cache architecture and memory
17 architecture and things like that. I think the
18 sentence just sort of states what it states, if you
19 will, that FRC logic, in this sentence, is looking
20 at write operations from each of the two cores in
21 the package when they get out to that shared cache.
22 * * *

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Exhibit 2009 - Page 57

1 BY MR. PETRSORIC:
2 Q. So it's your understanding that in this
3 sentence the FRC logic is not looking at write
4 operations to the private caches?
5 A. I don't see that Bigbee is explicitly
6 saying that in this sentence. A write operation
7 would presumably go -- well, again, depending on how
8 you have the cache designed, but you would have
9 writes to those private caches, too.
10 Q. Would the FRC logic be able to identify
11 inconsistencies in the generated results if it was
12 looking at writes to the private caches?
13 A. Let me just hear your question one more
14 time before I answer.
15 Q. Okay. Would the FRC logic be able to
16 identify inconsistencies in the generated results
17 from the two processor cores if that FRC logic was
18 looking at writes to the private caches?
19 MS. ZHANG: Objection, form.
20 A. I would say in this system you're
21 describing, if I've got the FRC logic block, and
22 instead of, you know, collecting data here for two

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Exhibit 2009 - Page 58

1 streams going to the shared cache and I look at the
2 stream higher up at the two private caches, you
3 know, if each core submitted a write operation to
4 its respective private cache, and one was writing
5 the value A and one was writing the value B, or
6 maybe to different addresses or something, it
7 would -- I think an FRC block would detect that
8 difference similarly to it would detect at the L2 --
9 or sorry, the shared cache.
10 BY MR. PETRSORIC:
11 Q. But you don't understand that Bigbee is
12 expressly teaching the FRC logic monitoring the
13 private caches?
14 MS. ZHANG: Objection, form.
15 A. Well, I guess at this point in Bigbee, in
16 33, in discussing that first illustration in
17 Figure 3 or 3a -- Figure 3, it's talking about in
18 this sentence, looking at writes to that shared
19 cache level in that Figure 3.
20 BY MR. PETRSORIC:
21 Q. I'd like to look back at paragraph 19 of
22 Bigbee on page 8.

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Exhibit 2009 - Page 59

1 A. Okay.
2 Q. And the second sentence of paragraph 19
3 states that: Hardware 102 of the disclosed
4 embodiment further includes FRC logic. Correct?
5 A. That's right.
6 Q. Then the third sentence indicates -- and
7 we've seen this already -- that the: FRC logic
8 detects errors within individual processor cores of
9 the described embodiment which causes hardware 102
10 to break lockstep between at least two processor
11 cores within a processor package, comma, disabling
12 FRC mode operation.
13 Do you see that?
14 A. Yes.
15 Q. And is it your understanding that by
16 disabling FRC mode operation, Bigbee is referring to
17 disabling the processors from running in lockstep?
18 A. It looks like what -- well, let me go
19 back to my declaration.
20 [Document review.]
21 A. Okay. So it looks like in 19, where
22 Bigbee mentions -- I'm just refinding my place --

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Exhibit 2009 - Page 60

1 about halfway through -- to break lockstep between
2 the two processor cores within a processor package,
3 disabling FRC mode operation.
4 So here it turns off the mode, and then
5 the hardware disables any of the package level error
6 containing cores, those go into the zombie state,
7 and then goes into generating exceptions.
8 So it sounds like what -- that it's
9 disabling that lockstep mode as part of this -- like
10 a multistep process, if you will.
11 BY MR. PETRSORIC:
12 Q. The sentence we read recites a break in
13 lockstep. Is that break in lockstep as a result of
14 the mismatch or potential for mismatch between the
15 results from the two processor cores?
16 [Document review.]
17 A. So it's saying that -- this paragraph is
18 talking about within a processor package, a
19 physical -- sorry, a physical processor package,
20 that the operating system sees as logical processor.
21 There's two or more of these physical processor
22 cores in lockstep when the FRC mode is on, or when

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Exhibit 2009 - Page 61

1 they're in that FRC mode.
2 And the logic is detecting an error
3 within the actual singular physical processor core,
4 and that error causes the hardware to break lockstep
5 between the two physical cores in this scenario.
6 And so when the FRC logic detects that,
7 that's when the rest of these steps engage.
8 (Clarification by reporter.)
9 BY MR. PETRSORIC:
10 Q. You mentioned zombie state being
11 disclosed in one of the sentences of paragraph 19 of
12 Bigbee a few moments ago, correct?
13 A. That's correct.
14 Q. Can you tell me what the zombie state is
15 referring to?
16 A. I'm just reviewing the next couple of
17 paragraphs that describe some of this.
18 [Document review.]
19 A. So this process -- so Bigbee mentions the
20 zombie state in 19. And then following paragraph,
21 20, 21, 22, and onward, talks about things that the
22 ACPI-compliant system does. And it's a -- it's a

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Exhibit 2009 - Page 62

1 rather lengthy process of disabling things, using
2 ACPI functionality to ultimately remove this
3 processor from the system and let other
4 firmware-type layers in the system know that this
5 logical processor is not -- something happened to it
6 and it's removed from service, if you will. And
7 this kind of is described in 20, probably through
8 25 -- paragraph 25 or so.
9 BY MR. PETRSORIC:
10 Q. You mentioned removing the processors,
11 but with respect to the zombie state, the
12 paragraph 19 of Bigbee refers to placing the cores,
13 the error-containing cores into a zombie state.
14 So are -- is that something different in
15 terms of the process to remove the entire processor
16 from the system?
17 A. I would say there is the multistep
18 ACPI/SAL/PAL process for doing the ACPI total eject
19 and all of that -- all of what is entailed in that
20 by ACPI. It looks like at this stage, after the FRC
21 condition happens and lockstep breaks between those
22 processor cores in 19, Bigbee uses this language of

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Exhibit 2009 - Page 63

1 zombie state for that error-containing core at that
2 moment in time.
3 Q. I'm trying to understand what the zombie
4 state is in reference to particular aspects of the
5 multistep ACPI process. Is there a particular step
6 of the ACPI process where the error-containing core
7 is placed into a zombie state?
8 MS. ZHANG: Objection, form.
9 A. No, I think what the -- the error happens
10 on the error-containing core, and Bigbee uses this
11 word "zombie state" because, I think, just at a high
12 level or generally, something is wrong on that core
13 here.
14 And then Bigbee goes on to describe, in
15 the next six paragraphs or so, the higher level,
16 here's what ACPI -- or here's what I'm describing to
17 do to get not only this error-containing core but
18 the larger logical processor module out of the
19 system in a -- like an ordered instruction, an
20 instructor -- sorry. An ordered and structured
21 manner that -- like ACPI contemplates.
22 * * *

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Exhibit 2009 - Page 64

1 BY MR. PETRSORIC:
2 Q. The -- in paragraph 19, it states that a
3 hardware 102 disables any of the package's
4 error-containing cores, placing them into a zombie
5 state.
6 Is that an active operation separate and
7 apart from the discovery that there's something
8 wrong within the error-containing core?
9 MS. ZHANG: Objection, form.
10 A. I'm not sure that Bigbee gets into that
11 detail. He's saying that the FRC -- so I'm -- just
12 to be clear, I'm starting about seven lines down.
13 The FRC logic detects the error in this -- let's say
14 this core, and then that causes the hardware to
15 break lockstep between the two cores within this
16 package, and then turns off the FRC mode, the
17 hardware turns off -- or, yeah, that's what he says.
18 The hardware turns off the FRC mode. And then
19 hardware 102 disables the package's error-containing
20 core at this point and sticks it in the -- what
21 Bigbee calls the zombie state.
22 And then you still have the other core in

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Exhibit 2009 - Page 65

1 this processor package that didn't have an error,
2 and then Bigbee continues to describe what goes on.
3 BY MR. PETRSORIC:
4 Q. Is there a particular portion of the ACPI
5 description in Bigbee where -- (interruption).
6 Sorry about that. Let me re-ask that.
7 Is there a particular portion of the ACPI
8 description in Bigbee where a particular portion of
9 the ACPI is active in disabling the error-containing
10 cores?
11 MS. ZHANG: Objection, form.
12 A. So I guess I'm not sure what you mean by,
13 in your question, if I heard it correctly, quote,
14 disabling the error-containing cores.
15 As paragraph 19 discusses, the error
16 happens in one of the cores in the processor
17 package. FRC detects this condition, lockstep
18 breaks between the two -- the hardware 102 breaks
19 the lockstep, and then it disables FRC mode because
20 lockstep -- we're not in lockstep anymore, and we
21 know one of the physical cores has the error
22 condition, and then disables that error-containing

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Exhibit 2009 - Page 66

1 core within the package we're talking about, and
2 puts it into the zombie state.
3 And then generates a check exception from
4 within this processor module, and that check
5 exception is what goes off in -- kicks off things in
6 the PAL layer that then starts this whole process of
7 getting this processor module removed from the
8 system in ACPI world.
9 Q. Is it the generation of the machine check
10 exception that is indicative of the error-containing
11 core being placed into the zombie state?
12 MS. ZHANG: Objection, form.
13 A. What Bigbee says is the FRC logic detects
14 the error in the individual processor core, let's
15 say, here, and then that causes the hardware to
16 break the lockstep between the two and disable the
17 FRC mode. And then that hardware 102 also disables
18 the error-containing core, putting it in that zombie
19 state.
20 BY MR. PETRSORIC:
21 Q. Is there any particular disclosure within
22 Bigbee as to how the error-containing core is

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Exhibit 2009 - Page 67

1 disabled?

2 MS. ZHANG: Objection, form.

3 A. I would say Bigbee, just like Nguyen and

4 a number of the other references, talks about these

5 Intel Itanium systems, or systems that support this

6 FRC mode, and the overall ACPI process with the PAL

7 layer and the SAL layer as how to remove these

8 processor packages from the system.

9 BY MR. PETRSORIC:

10 Q. But there's a difference between

11 disabling the processor and removing the processor

12 package -- oh, strike that.

13 There's a difference between disabling an

14 error-containing processor core and removing the

15 processor package from the system, correct?

16 A. Yes, they're -- I would say they're --

17 one is part of the other, but yes, in this process,

18 there is the error happening on the error-containing

19 core and then there's the subsequent steps that are

20 described.

21 Q. And is there a particular ACPI command

22 that's issued to disable the error-containing

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Exhibit 2009 - Page 68

1 processing core?
2 A. There -- as I talk about in my
3 declaration, there's the various ACPI eject methods
4 that I discuss, and the firmware in my Bigbee and
5 Nguyen combination.
6 Q. Does the ACPI eject -- disable the
7 error-containing core or does it remove the
8 processor package from the system?
9 A. The ACPI-level functionality is removing
10 this package from the system. In your initial
11 question about Bigbee in 19, it's talking about
12 hardware 102 perceiving the error in the core, the
13 hardware breaking the lockstep between the two
14 processor cores and disabling that FRC mode
15 operation, and then putting the error-containing
16 core into the zombie state, and then that hardware
17 102 generating a machine check exception that then
18 causes functionality in the PAL firmware layer to
19 start performing its functionality.
20 Q. So there's no particular ACPI command
21 that disables the error-containing core, is there?
22 MS. ZHANG: Objection, asked and

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Exhibit 2009 - Page 69

1 answered.

2 A. I would say -- and we can go back to the

3 section in my declaration on the ACPI methods, and

4 particularly the _EJx method for ejecting, and I

5 talk about others of them.

6 But in terms of what Bigbee is talking

7 about here, that the hardware 102 in paragraph 19 is

8 being described as detecting the error condition and

9 breaking the lockstep and the zombie state for its

10 error-containing processor, and the generation of

11 the machine check exception, which then, as I said,

12 triggers the execution of the PAL layer

13 functionality on the core that's not -- the core

14 within the module that's not in the zombie state.

15 BY MR. PETRSORIC:

16 Q. The EJx method ejects the entire

17 processor package, including all its constituent

18 cores, correct?

19 A. I'm just doing a quick search through my

20 declaration for you.

21 [Document review.]

22 A. Right. So the EJx method is ACPI for

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Exhibit 2009 - Page 70

1 ejecting the processor in this scenario, like a hot
2 removal. And 36 of Bigbee talks about the operating
3 system modifies its internal data structures to
4 indicate the processor is offline, requests firmware
5 ejection. Firmware ejection is done by the EJx
6 control method.
7 And then 37, it talks about reenabling
8 FRC of the at least first and second cores,
9 et cetera, et cetera.
10 So we can go back to the ACPI
11 specification, but I believe the EJx is for, in this
12 case, this ejecting and idling the processors.
13 The -- I believe it's at the logical level of the
14 processor module.
15 BY MR. PETRSORIC:
16 Q. And that goes beyond just disabling the
17 error-containing core, correct?
18 A. I would say that, as Bigbee describes
19 back in paragraph 19 that we talked about a moment
20 ago, the hardware 102 detects this error-condition
21 and disables the lockstep, and then generates an
22 exception that then causes functionality at the ACPI

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Exhibit 2009 - Page 71

1 processor abstraction layer to start executing,
2 which then results in what we were just talk- -- is
3 part of the process we were just talking about, the
4 ACPI ejection and so forth.
5 Q. But again, I'm trying to see if there's
6 any express disclosure in Bigbee as to exactly what
7 occurs to disable the error-containing core in
8 response to the FRC logic detecting an error.
9 Is there a specific ACPI command that's
10 issued to the error-containing core to disable it?
11 MS. ZHANG: Objection, form.
12 A. Your question sounds like it's asking for
13 an answer that encompasses, I guess, multiple layers
14 in this complex multilayer system. But just as
15 Bigbee says in 19, there's a hardware 102 that
16 detects the error within this individual processor
17 core, and then that same hardware block, or hardware
18 102, has seen the error, disables the lockstep
19 between the -- in this case, let's say two processor
20 cores, turns off FRC mode, because lockstep is no
21 longer present, and then it says that same hardware
22 disables the package's error-containing cores.

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Exhibit 2009 - Page 72

1 I don't see the -- if you're asking does
2 Bigbee say which signal goes from low to high or
3 something like that, to which input signal on a core
4 or something like that, I don't see that he states
5 that at that level of detail, but he -- but he
6 describes that it goes into the zombie state and
7 then generates an exception, which results in the
8 firmware of ACPI performing its steps.
9 BY MR. PETRSORIC:
10 Q. Turning back to your declaration at
11 page 48 in the second half of paragraph 81, you
12 state that: Bigbee only discloses recovering from
13 recoverable lockstep errors; it does not disclose
14 performing a threshold determination of whether
15 detected errors are recoverable or non-recoverable.
16 Do you see that?
17 A. That's right, up through, I think, the
18 second-to-last sentence of 81. I was just catching
19 up to you there.
20 Q. Is -- and what do you mean by "a
21 threshold determination" in that sentence?
22 A. This would be, if we jump ahead, for

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Exhibit 2009 - Page 73

1 example, two pages to the figure -- the annotated
2 Bigbee figure I've prepared where there is a -- the
3 determining if the lockstep is recoverable, and if
4 not, performing the steps that I show in this
5 figure.
6 Q. And are you referring to the figure
7 before paragraph 86 in -- on page 50 of 96?
8 A. That's correct.
9 Q. And the -- it's paragraph 85 on page 49
10 of 96 that describes that figure, correct?
11 A. That's what -- that's what paragraph 85
12 is talking about, the Bigbee-Nguyen system, and my
13 illustration on the next page.
14 Q. The second sentence of paragraph 85
15 states: Taking step 404 of Bigbee's Figure 2, and
16 adding Nguyen's step of determining whether lockstep
17 is recoverable after Bigbee detects loss of
18 lockstep, would address both recoverable and
19 non-recoverable errors, as the following figure
20 shows. Correct?
21 A. That's correct.
22 Q. You reference Bigbee's Figure 2 there,

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Exhibit 2009 - Page 74

1 but doesn't that show the annotation -- the
2 annotated figure on page 50 actually shows
3 Figure 4a, correct?
4 A. That is correct. I didn't notice that.
5 Q. So there's -- that Figure 2 is in error
6 and should be referring to Figure 4a?
7 A. That sounds right. I believe I meant to
8 reference Bigbee 4a, which is what I use in the
9 subsequent figure I generated on the next page.
10 Q. Are you aware of any other typographical
11 or clerical errors in your declaration?
12 A. Not offhand. There might be one
13 similar -- I said a Figure 3 when I meant Figure 1
14 or something like that, but I don't remember
15 specifically.
16 Q. In this annotated figure on page 50 of 96
17 in the declaration you highlight step 404 of
18 Figure 4a, correct?
19 A. That's correct.
20 Q. And in Bigbee, is that where the loss of
21 lockstep is determined?
22 [Document review.]

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Exhibit 2009 - Page 75

1 A. So here in block 404 of Figure 4a of
2 Bigbee is where Bigbee's hardware detects an error
3 within the first processor core of the -- let's say
4 the two cores in that logical processor that were in
5 functional redundancy check mode. And this is the
6 step in which I incorporate the -- determining if
7 that lockstep is recoverable using the portion from
8 the Nguyen reference.
9 BY MR. PETRSORIC:
10 Q. And the rightmost portion of the figure
11 in the diamond-shaped box, you attribute -- that's
12 where you attribute the determining if lockstep is
13 recoverable to Nguyen, correct?
14 A. The Nguyen determination step, yes.
15 Q. And if the lockstep is recoverable, this
16 is where you indicate a return to Bigbee's teaching
17 to disable the first core and generate a machine
18 check exception?
19 A. Yes. And if I remember, I think you
20 asked if there were any other typographical errors.
21 I think this box in my red figure that you're
22 reading from, there's one -- I think two or three

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Exhibit 2009 - Page 76

1 more words that got cut off here. But yes, it
2 continues with the Bigbee flow that's described in
3 that block.
4 Q. And should that box at the bottom of the
5 right side of the figure read: Disables the first
6 processor core, and generates a machine check
7 exception?
8 A. Machine -- yeah, same as what we see in
9 that -- the -- I guess the original Bigbee block
10 404, generates a machine check exception -- or check
11 exception to firmware.
12 Q. And back to the diamond block, if
13 lockstep is not recoverable, that's when you're
14 indicating to reset the system as taught by Nguyen?
15 MS. ZHANG: Objection, form.
16 A. That's where I incorporate -- at least
17 part of the Nguyen reference or Nguyen's determining
18 and handling of that non-recoverable scenario.
19 BY MR. PETRSORIC:
20 Q. And the action taken or taught by Nguyen
21 is to reset the system?
22 MS. ZHANG: Objection, form.

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Exhibit 2009 - Page 77

1 A. So I cite to a few paragraphs in Nguyen
2 in this section, such as 56 and 57. And I'm just
3 revisiting my declaration point.
4 [Document review.]
5 A. And I also mention in paragraph 84,
6 Nguyen's paragraphs 8 and 9 talking about handling
7 otherwise -- talking about handling the
8 non-recoverable errors, and going back to what
9 Nguyen talks about in terms of recovering in this
10 scenario. Or handling this scenario, I should say.
11 Q. So is it fair to say that you're
12 inserting Nguyen's determination of recoverability
13 in -- as part of this process in block 404 of
14 Bigbee?
15 MS. ZHANG: Objection, form.
16 A. That I would say it's -- I'm
17 incorporating Nguyen's determination of whether
18 these Bigbee error -- errors detected by Bigbee are
19 recoverable or non-recoverable and to properly
20 handle the detected errors and the benefits that
21 come with them.
22 * * *

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Exhibit 2009 - Page 78

1 BY MR. PETRSORIC:
2 Q. And is that your determining -- using
3 Nguyen to determine/properly handle the detected
4 errors after you -- after Bigbee first detects an
5 error in the first processor core?
6 A. I would phrase it that it is using
7 Bigbee's detection functionality, and then -- the
8 Nguyen determining of recoverable or
9 non-recoverable.
10 MS. ZHANG: We've been going on for
11 an hour.
12 Mike, would you like to take a break?
13 THE WITNESS: Sure.
14 MS. ZHANG: Counsel, would you like
15 to take a lunch break at this time?
16 MR. PETRSORIC: It's up to
17 Dr. Brogioli. I probably have less than one
18 session left, so if you'd like to take lunch,
19 that's fine. If you'd like to finish after a
20 short break, that's fine as well.
21 MS. ZHANG: Okay. Let's go off the
22 record for now and take a break.

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Exhibit 2009 - Page 79

1 THE WITNESS: Okay.
2 (Recess taken, 12:26 p.m. to
3 12:53 p.m. EDT)
4 BY MR. PETRSORIC:
5 Q. Dr. Brogioli, I'd like to turn in your
6 declaration now to paragraph 113 at -- begins at
7 page 63 of 96.
8 A. Okay.
9 Q. And in paragraph 113, you indicate a --
10 that a person of ordinary skill in the art would
11 have incorporated Nguyen's determining if the
12 lockstep is recoverable into Bigbee to take an
13 appropriate action responsive to the recoverability
14 of the error detected in the lockstep processor
15 pair.
16 Do you see that?
17 A. Yes, I do.
18 Q. And can you tell me what you mean here by
19 an appropriate action responsive to the
20 recoverability of the error?
21 A. I'm just revisiting the couple prior
22 paragraphs.

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Exhibit 2009 - Page 80

1 [Document review.]
2 A. So this would be a person of skill
3 performing the Nguyen determining step in firmware,
4 and as I discuss in the couple prior paragraphs,
5 there's the -- Nguyen's notion of this timeout
6 interval that I talk about on page 62. And if the
7 error detector detects an error after that timeout
8 interval, i.e., the non-recoverable, one thing that
9 Nguyen talks about is -- I'll have to go back.
10 The -- I think it's the resetting or
11 restarting language that Nguyen uses. One second.
12 [Document review.]
13 A. I'm just jumping back to the Nguyen
14 reference.
15 [Document review.]
16 A. As I mention in my declaration here, I
17 guess in paragraphs 110 and 111, would be
18 implementing -- or invoking the Nguyen recovery
19 routine described in these -- I guess paragraphs 56
20 and 57 of Nguyen.
21 BY MR. PETRSORIC:
22 Q. And that -- with respect to paragraphs 56

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Exhibit 2009 - Page 81

1 and 57 of Nguyen, that is -- what you're saying is
2 responsive to determining if the lockstep is
3 recoverable is when paragraphs 56 and 57 of Nguyen
4 indicate recoverability versus non-recoverability;
5 is that correct?
6 MS. ZHANG: Objection, form.
7 A. That I am incorporating the Nguyen
8 determining if that -- the lockstep scenario is
9 recoverable, and taking that appropriate action to
10 perform the recoverability that I talk about in 113.
11 BY MR. PETRSORIC:
12 Q. In paragraph 114 on the next page, which
13 is page 64 of 96, you indicate that Bigbee discloses
14 firmware code... for triggering an operating system
15 to idle the processors. Correct?
16 A. That's correct.
17 Q. And I just want to understand it further.
18 So with respect to Figure 4a of Bigbee,
19 in response to the loss of lockstep determination,
20 the firmware, specifically the SAL, the S-A-L,
21 program code generates a system control interrupt,
22 SCI, to the operating system, correct?

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Exhibit 2009 - Page 82

1 A. The -- yes, Bigbee talks about ACPI and
2 the SAL layer as part of that process generating
3 these interrupts to perform, as we were talking
4 about earlier, this ejection process.
5 Q. And that in response to the SCI, the
6 operating system queries the ACPI firmware to
7 determine the source of the SCI, correct?
8 A. That the -- yes, the operating system
9 queries or inquires into this ACPI firmware, which
10 then responds to the query and notifies that this
11 request for the processor hot removal using the ACPI
12 Notify command.
13 Q. So the ACPI Notify will indicate --
14 strike that.
15 So the firmware will, using the ACPI
16 Notify, identify the processor that is -- for which
17 hot removal is required to the operating system.
18 MS. ZHANG: Objection, form.
19 A. That the firmware here is determining the
20 source of the SCI we talked about, and tells -- or
21 responds to this query notifying the operating
22 system, or OS, that there's a processor hot removal

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Exhibit 2009 - Page 83

1 request happening, and then the operating system
2 goes and modifies its data structures or
3 bookkeeping. And then the firmware is ejecting the
4 processor using the EJx command that's idling the
5 processors in this flow.
6 And I think these are similar paragraphs
7 we were talking about before the break in Bigbee.
8 BY MR. PETRSORIC:
9 Q. After that sentence, that third sentence
10 in paragraph 114, there's a cite to paragraph 36 of
11 Bigbee and Figure 4a at blocks 408 to 410, correct?
12 A. That's correct.
13 Q. And then there's a parenthetical of
14 triggering an operating system, correct?
15 A. Yes.
16 Q. What is the source of that parenthetical?
17 A. That is the language of the claim element
18 19c that this section is talking about.
19 Q. And similarly, the last sentence of
20 paragraph 114 reads that: The operating system then
21 modifies its internal data structures to indicate
22 that the processor is offline and requests firmware

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Exhibit 2009 - Page 84

1 ejection of the processor, e.g., by executing an
2 _EJx control method.
3 Correct?
4 A. That's correct.
5 Q. And are you indicating that -- here that
6 the -- by executing an EJx control method, that this
7 satisfies the claim language of "to idle the
8 processors"?
9 A. Yes, that the EJx method, as part of
10 ACPI, is the idling of the processors. And that's
11 referenced in Bigbee and similarly, the same ACPI in
12 Nguyen as well. And the '958 patent as well.
13 Q. And with respect to the '958 patent,
14 you're -- is it in paragraph 116 that you're
15 equating the ejection of the processors with idling
16 of the processor?
17 MS. ZHANG: Objection to form.
18 A. So you are asking in the patent itself,
19 correct?
20 BY MR. PETRSORIC:
21 Q. Or within -- both within the '958 patent
22 itself and with respect to your opinion in

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Exhibit 2009 - Page 85

1 paragraph 116 on page 66 of 96 of your declaration.
2 A. So let me start -- I'm not sure I'm
3 totally following you. So where in the patent were
4 you asking about?
5 Q. I was more primarily asking in
6 paragraph 116 of your declaration.
7 A. Okay. That the operating system is using
8 this EJx control method to perform the idling of the
9 processors here.
10 Q. And then are you saying -- are you saying
11 that that's also taught -- what's taught by the '958
12 patent in reference to your citations to the '958
13 patent at column 8, lines 9 through 17; column 6,
14 lines 40 through 42; and column 6, from line 55 to
15 57?
16 A. So I apologize. I hear you reading cites
17 that sound like they're from my declaration to the
18 patent specification, but I don't -- I'm not
19 following where that is in paragraph 114. Maybe
20 I --
21 Q. Paragraph 116.
22 A. Probably why I'm not following.

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Exhibit 2009 - Page 86

1 [Document review.]
2 A. Yes, that's right, that I'm talking about
3 the '958 and the idling of the processors and the
4 use of the ACPI eject method here, and then I've got
5 the various cites to the patent.
6 BY MR. PETRSORIC:
7 Q. If you'd pull up Exhibit 1001, which is
8 the patent, the '958 patent.
9 A. All right.
10 Q. At the -- the first citation at
11 paragraph 116 is to column 8, lines 9 through 17,
12 correct?
13 A. That is correct.
14 Q. Can you explain to me how column 8 at
15 lines 9 through 17 of the '958 patent uses an ACPI
16 method to eject the processors?
17 A. 9 to 17.
18 [Document review.]
19 A. Okay. So the first portion, I guess,
20 roughly from 9 through 14 is talking about the
21 ACPI-compatible OS and there are -- in ACPI, there's
22 tables that are used to discover what's present in

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Exhibit 2009 - Page 87

1 the system or the computer.
2 And so then the OS is using the firmware
3 interfaces here to perform this functionality on the
4 processors that are discovered. And so now the
5 OS -- I'm at line 13 or so -- has control here of
6 processors and firmware -- is no longer in control,
7 it says, so the OS has gone out and kind of figured
8 out the world.
9 And then at 15, it discovers from
10 firmware the hardware that was present at boot time,
11 and it also has knowledge of hardware that's present
12 or added or removed and stating how it uses --
13 there's a supporting firmware that we talked about,
14 PAL/SAL, as an example. And those are used at
15 run-time to support the processor in this
16 functionality we've been talking about.
17 Q. Does this particular portion of the '958
18 patent at column 8, lines 9 through 17, discuss
19 ejection of the processors at all?
20 A. It's describing the relationship between
21 OS, ACPI, and firmware, which, as the patent itself
22 states, is well-known in the art, and how at this

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Exhibit 2009 - Page 88

1 point in, for example, the system coming online, how
2 these things interrelate for what's present in the
3 system or can be added and removed. And it's
4 explaining, at least in part, how this all works in
5 ACPI, and because it's ACPI in these different
6 layers, you know that the eject method is present,
7 because it's part of the ACPI specification.
8 Q. Similarly, column 6 at lines 40 through
9 42 of the '958 patent, it reads: Firmware 15 then
10 attempts to recover lockstep for the lockstep
11 processor pair 12 in block 105. For instance,
12 firmware 15 resets the processor pair 12.
13 Do you see that?
14 A. I do.
15 Q. How does resetting the processor pair
16 relate to ejecting the processors?
17 MS. ZHANG: Objection, form.
18 A. Just reading the surrounding text before
19 I answer.
20 [Document review.]
21 A. So the language starting at 40 of
22 firmware 15 then attempts to recover lockstep for

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Exhibit 2009 - Page 89

1 the lockstep processor pair in block 105, but then
2 is following onto the language of the prior
3 paragraph, and here it's all talking about ACPI,
4 specifically utilization of the ACPI method eject at
5 lines 12, 13, 14, and that relationship with the OS,
6 and the stopping and scheduling tasks for the
7 processor and so forth.
8 BY MR. PETRSORIC:
9 Q. Then similarly, the cite at column 6 from
10 line 55 through 57 cites -- recites: Once the
11 processor pair 12 is reset and lockstep is
12 recovered, firmware 15 reintroduces master processor
13 12A to OS 11 in operational block 106.
14 Correct?
15 A. Yes, that's correct.
16 Q. Does that have anything to do with
17 ejecting the processors or basically reintroducing
18 the processors to the operating system after
19 lockstep has been recovered?
20 A. This is -- this paragraph starting at 55
21 is, again, talking about in the same flow, at least
22 starting in line 9 of this column 6, where once this

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Exhibit 2009 - Page 90

1 processor pair is reset and lockstep is recovered,
2 the firmware reintroduces master processor 12A to
3 the OS in operational block 106, and then talks
4 about updating of the ACPI device tables that we
5 talked about a moment ago.
6 MR. PETRSORIC: I have no further
7 questions.
8 MS. ZHANG: Mike, can we take a
9 break?
10 (Recess taken, 1:16 p.m. to
11 1:24 p.m. EDT)
12 MS. ZHANG: Thank you. We have no
13 further questions.
14 (Time noted: 1:25 p.m. EDT)
15 --o0o--
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Exhibit 2009 - Page 91

1 C E R T I F I C A T E

2

3 I, DEBRA A. DIBBLE, RDR, CRR, CRC, Notary

4 Public, do hereby certify:

5 That MICHAEL C. BROGIOLI, the witness

6 whose deposition is hereinbefore set forth, was duly

7 sworn by me and that such deposition is a true

8 record of the testimony given by such witness;

9 That pursuant to FRCP Rule 30, signature of

10 the witness was not requested by the witness or

11 other party before the conclusion of the deposition;

12 I further certify that I am not related to any

13 of the parties to this action by blood or marriage,

14 and that I am in no way interested in the outcome of

15 this matter.

16 IN WITNESS WHEREOF, I have hereunto set my

17 hand on this 10th day of July, 2024.

18

19 _____
Debra A. Dibble
20 Fellow of the Academy of Professional Reporters
Registered Diplomate Reporter
21 Certified Realtime Reporter

22

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Exhibit 2009 - Page 92

1 I HEREBY CERTIFY that I have read
2 this transcript of my deposition, and that
3 this transcript accurately states the testimony
4 given by me, with the changes or corrections, if
5 any, as noted.
6
7
8 X _____
9 MICHAEL C. BROGIOLI
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Exhibit 2009 - Page 93

1 ERRATA SHEET FOR THE TRANSCRIPT OF:

2 CASE NAME: BMW/Bosch v Foras Technologies

3 DEP DATE: July 10, 2024

4 DEPONENT: MICHAEL C. BROGIOLI

	Pg.	Ln.	Now Reads	Should Read	Reason
6	__	__	_____	_____	_____
7	__	__	_____	_____	_____
8	__	__	_____	_____	_____
9	__	__	_____	_____	_____
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20

21 X _____

22 MICHAEL C. BROGIOLI

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Exhibit 2009 - Page 94

A

a.m 2:6 7:3 48:9,10
A1 6:9
able 10:15 11:14 14:10 27:22 40:17 58:10,15
above-referenced 2:5
above-styled 2:4
abstraction 72:1
Academy 2:7 92:20
access 11:4 53:2
accompany 56:8
accurately 93:3
ACPI 10:5 51:6,9 52:8,10,11 63:2 63:18,20 64:5,6 64:16,21 66:4,7,9 67:8 68:6,21 69:3 69:6,20 70:3,22 71:10,22 72:4,9 73:8 83:1,6,9,11 83:13,15 85:10,11 87:4,15,21 88:21 89:5,5,7 90:3,4 91:4
ACPI-compatible 87:21
ACPI-compliant 62:22
ACPI-level 69:9
ACPI/SAL/PAL 63:18
action 14:3 77:20 80:13,19 82:9 92:13
actions 13:3,5,13 13:15
active 65:6 66:9
actual 62:3
add 22:1 28:6
added 16:21 17:4,5 17:11 88:12 89:3
adding 74:16
addition 54:17
additional 49:15
address 50:8 74:18
addressed 21:1
addresses 59:6
addressing 12:3
ago 29:8 62:12 71:20 91:5
agreed 7:10
ahead 25:18 73:22
algorithms 21:8
allowed 13:8
AMERICA 1:5
analyzing 28:3
and/or 41:17
annotated 74:1 75:2,16
annotation 75:1
annotations 10:7
answer 22:15 23:11 24:4 31:17,19 36:20 53:9 54:18 58:14 72:13 89:19
answered 18:4 70:1
answers 8:11,14
anybody 8:20
anymore 66:20
anyway 44:13,19 49:5
apart 65:7
apologize 43:12 86:16
APPEAL 1:3
APPEARANCES 3:1 5:3
appearing 7:10
Application 6:8
appropriate 80:13 80:19 82:9
approximately 8:5
aratycz@bclgpc.... 3:4
architecture 50:1 55:18 56:10 57:16 57:17
areas 18:10,15
arithmetic 22:1
arrays 19:16,16
art 10:5 12:3,11,22 14:9 22:12 39:2 40:15 45:16 51:12 51:20 52:16,21 53:17 54:15 55:2 56:5 80:10 88:22
ASHLEY 3:3
asked 18:3 48:13 69:22 76:20
asking 13:15 19:11 24:2,10,15,19 25:14 27:11 53:22 54:14 72:12 73:1 85:18 86:4,5
aspect 42:5
aspects 64:4
associated 36:13 41:16 54:22
Atlanta 4:4
attempts 89:10,22
attorneys 8:21,22
attribute 76:11,12
availability 13:11 34:11
available 33:22
Avenue 3:4
aware 9:16 75:10

B

b 35:21 36:22 59:5
B2 1:12 6:4
back 13:19 14:21 15:1 16:7 17:22 22:20 24:19 25:8 26:11,22 27:10 31:19 34:12 36:21 38:22 39:4 40:21 42:5 47:22 48:20 49:6 52:2 56:17 56:17 59:21 60:19 70:2 71:10,19 73:10 77:12 78:8 81:9,13
bad 13:9 17:17,20 53:3
based 55:9
basically 90:17
BC 3:2
begins 44:5 80:6
behavior 22:7
believe 9:1 13:22 71:11,13 75:7
benefits 78:20
beyond 51:22 71:16
Bigbee 6:9 25:22 26:12,14 28:5,7 28:12 29:8 30:10 30:14 31:6 33:9 34:7,10,17,20 35:14,18 36:1,7 38:22 39:2,4,10 39:12,16 40:13,22 42:1,5,6 43:3,12 43:16,20 44:2,4 45:2,5,10,20 46:14,19 47:3,6,9 47:9,12,15,19 48:13 49:4,7,14 51:4,6,20 52:3,3 52:22 53:10 54:5 55:6 57:11,14 58:5 59:11,15,22 60:16,22 62:12,19 63:12,22 64:10,14 65:10,21 66:2,5,8 67:13,22 68:3 69:4,11 70:6 71:2 71:18 72:6,15 73:2,12 74:2,17 75:8,20 76:2 77:2 77:9 78:14,18,18 79:4 80:12 82:13 82:18 83:1 84:7 84:11 85:11
Bigbee's 42:6 46:10 48:1,21 50:19 54:3 74:15,22 76:2,16 79:7
Bigbee-Nguyen 74:12
bigger 38:2,3 55:22 57:5
bit 12:15 15:6,6 16:10,12 17:1,17 17:20 20:13,21 30:15 51:17
bits 12:15 15:9 16:20,21 17:3,5,6 17:7,9 18:20,21 19:3,7,8,9,17,21 19:22 20:3,6,6,13 20:20 21:5,7,10 47:4,7,10 53:18 54:16,17,21 55:2 55:8 56:6,7,12
block 36:2 42:11,17 44:5 45:17 58:21 59:7 72:17 76:1 77:3,9,12 78:13 89:11 90:1,13 91:3
blocks 84:11
blood 92:13
BMW 1:5
BMW/Bosch 94:2
BOARD 1:3
book 56:10
bookkeeping 84:3
boot 88:10
BOSCH 1:5
Boston 3:11
bottom 39:6 46:6 50:5 52:2 77:4
bound 35:4
box 33:8 76:11,21 77:4
break 29:3 31:1 48:7,12 60:10 61:1,12,13 62:4 65:15 67:16 79:12 79:15,20,22 84:7 91:9
breaking 69:13 70:9
breaks 32:1 63:21 66:18,18
briefly 7:6
Brogioli 1:16 2:2 5:6 6:6 7:15,22 8:4 10:17 11:3,10 16:1 23:12 25:6 28:13 48:12 79:17

80:5 92:5 93:9 94:4,22
bucket 38:3
bus 36:9,17,19 37:10
bytes 19:17

C

C 1:16 2:2 5:6 6:6 7:2,15 11:2 92:1,1 92:5 93:9 94:4,22
cache 12:14 16:12 16:16,22 17:12,18 18:8 21:2,4,7 27:7 30:2 36:11,13 37:1,3,13,14,15 37:17,20 41:17 42:7,15,22,22 43:5,10,15,19 44:22 45:9 46:8 46:15 47:4,8,13 47:18 48:15 49:9 50:7 51:22 52:6 53:8,12,18,22 54:9,16,21 55:7,8 55:10,11,14,17,22 56:1,4,4,7,8,12,13 56:21 57:5,6,12 57:16,21 58:8 59:1,4,9,19
caches 19:15 41:21 42:3 45:7 47:21 48:14 52:18 58:4 58:9,12,18 59:2 59:13
call 40:6
calls 65:21
case 1:11 71:12 72:19 94:2
cases 13:1
catastrophic 21:6
catching 73:18
cause 2:5
causes 29:2 30:22 31:9 60:9 62:4 65:14 67:15 69:18 71:22
causing 12:4 13:10 26:4,9,20 27:12
CCR 2:7
certain 19:9
CERTIFICATE 5:9
Certified 92:21
certify 92:4,12 93:1
cetera 50:4 71:9,9
changes 93:4
Charles 8:4
chat 10:20,22 11:3 15:19 28:12
check 30:5 31:8,9 36:10 38:7 39:20 40:21 46:22 67:3 67:4,9 69:17 70:11 76:5,18 77:6,10,10
checker 27:16
checking 30:3
circle 17:22
circling 56:17
citation 87:10
citations 86:12
cite 34:16 78:1 84:10 90:9
cites 86:16 87:5 90:10
claim 84:17 85:7
Clarification 62:8
clean 9:20
clear 31:13 65:12
clerical 75:11
code 32:5 82:14,21
codes 16:15,15
collecting 58:22
column 19:13 27:5 39:6 86:13,13,14 87:11,14 88:18 89:8 90:9,22
columns 14:21 15:1
combination 69:5
come 78:21
coming 34:12 54:6 57:2 89:1
comma 60:11
command 68:21 69:20 72:9 83:12 84:4
communication 9:14
complete 14:10 15:18
completely 7:8
complex 72:14
components 42:8 50:13
computation 40:20
computer 11:7,16 19:17 33:8,19 37:8 50:8 55:20 56:10 88:1
computer's 13:8
computing 12:17 18:10 22:6
concept 18:9
concepts 56:16
concisely 36:20
conclusion 92:11
concurrently 38:17 39:21 41:4
condition 63:21 66:17,22 70:8
confines 34:7
confirm 37:13
confusing 39:1
consider 14:19 33:2 33:11 34:2
considered 10:4 17:14 40:3
considering 17:17
consistent 41:6
constituent 70:17
contain 37:21 38:4
containing 61:6
contemplates 64:21
contemplating 28:5
context 33:4
continue 12:17 13:8 15:10 23:18
continues 66:2 77:2
continuing 49:18 51:2
control 71:6 82:21 85:2,6 86:8 88:5,6
copies 9:20 10:18
copy 10:21 11:18 15:20 27:1
core 27:6 31:6,11 31:22 33:18 36:11 36:12 37:14,15 38:16 39:21 40:9 41:14 42:19 43:4 44:7,15,22 45:6 46:6,12,17,21 47:17 48:18 49:8 50:6 51:1 52:5 53:11,20 54:7 56:18,21 59:3 62:3 64:1,6,10,12 64:17 65:8,14,20 65:22 67:1,11,14 67:18,22 68:14,19 69:1,7,12,16,21 70:13,13 71:17 72:7,10,17 73:3 76:3,17 77:6 79:5
core-specific 45:13
cores 27:14 29:2,4 29:10 30:22 31:2 32:2,11 33:19,20 35:2,10,13 36:22 37:12 38:4,15 39:8,13 40:3,7,11 40:18 41:3 43:17 43:22 44:8 45:13 45:17 46:1 47:5 53:12 54:6 57:2 57:20 58:17 60:8 60:11 61:2,6,15 61:22 62:5 63:12 63:13,22 65:4,15 66:10,14,16,21 69:14 70:18 71:8 72:20,22 76:4
correct 12:7,8 14:13,14,16 15:15 15:16,17 16:16 17:11,19 18:9 19:22 20:5,7,13 20:21 21:14,15 24:8 29:10,21 31:15 34:17,18 35:11,12,14,19 36:4,5 37:15,16 37:18,19 38:7,8 38:10,11,12,18 43:7,8,11 45:1 49:1 54:12,13 55:15 60:4 62:12 62:13 68:15 70:18 71:17 74:8,10,20 74:21 75:3,4,18 75:19 76:13 82:5 82:15,16,22 83:7 84:11,12,14 85:3 85:4,19 87:12,13 90:14,15
correctable 20:1
corrected 12:15 15:8 16:14 17:1 19:10 21:9
correcting 17:20
correction 16:15 17:13 20:6
corrections 93:4
correctly 66:13
corrupted 13:3 21:6
corruption 12:17 13:11 20:7 22:7,8
Counsel 3:8,12,18 4:5 79:14
couple 44:16 62:16 80:21 81:4
coupled 36:8 50:11
court 7:5 8:10,16 10:20
CPU 33:4
CPUs 21:18 23:4 24:5
CRC 1:21 92:3
CRR 1:21 2:7 92:3
CSR 2:7
cut 77:1

D

D 7:2
data 12:14,17 13:9 13:10 16:21 17:3 17:6,9,12 18:21 19:8,16,22 20:13 20:21 22:8 37:10 37:21,22 38:17 39:22 41:5,15 43:10,21 44:12 45:21 47:3,7,13 48:15 50:8,9 51:10,21 52:9,17 53:5,17 54:16,17 54:20,22 55:4,9,9 55:13,21 56:3,8 58:22 71:3 84:2 84:21
date 2:5 94:3
day 92:17
Debra 1:21 2:6 92:3,19
decade 55:20
decide 10:18
declaration 6:5 9:20 11:2,20 12:12 14:8 21:2 21:13,17 22:16,21 24:17 25:2,17,19 26:18 27:11 28:4 29:16 30:11 34:6 34:16 60:19 69:3 70:3,20 73:10 75:11,17 78:3 80:6 81:16 86:1,6 86:17
dedicated 50:11
Dell 9:11
DEP 94:3
depend 18:16 21:10
depending 20:5 21:8 55:19 58:7
depends 20:2 42:4
depicted 35:3
DEPONENT 94:4
deposed 8:6
deposition 1:15 2:2 6:1 7:9 8:10 9:9 11:10 16:1 28:13 92:6,7,11 93:2
describe 43:20 47:12 52:6 62:17 64:14 66:2
described 29:2 30:11,13 31:14 32:19 33:10 35:17 44:19 45:14 60:9 63:7 68:20 70:8 77:2 81:19
describes 48:2 71:18 73:6 74:10
describing 32:9 43:14 45:3,11 46:19 51:16 58:21 64:16 88:20
description 6:2 30:2 32:13,15 48:4 66:5,8
descriptions 49:19
design 55:19
designed 20:5 28:9 58:8
designer 18:17 20:9
detail 65:11 73:5
detect 18:8 20:4,4 25:15 27:7 31:14 43:5 46:16 54:10 59:7,8
detected 16:9 18:2 23:5,8,15,16,21 23:21 24:3,3,5,8 24:11,12,20,21,21 25:12 33:10 73:15 78:18,20 79:3 80:14
detecting 13:20,21 25:22 26:2 32:10 42:11 44:14 50:22 62:2 70:8 72:8
detection 23:8 79:7
detector 81:7
detects 29:1,9,20 30:21 31:22 33:15 42:18 44:6 60:8 62:6 65:13 66:17 67:13 71:20 72:16 74:17 76:2 79:4 81:7
determination 45:22 73:14,21 76:14 78:12,17 82:19
determine 18:20 19:20 25:5 27:22 46:21 47:4 53:19 83:7
determine/prope... 79:3
determined 26:5,10 26:21 27:13 75:21
determining 74:3 74:16 76:6,12 77:17 79:2,8 80:11 81:3 82:2,8 83:19
developed 52:11
device 9:8 91:4
diagram 36:2
diamond 77:12
diamond-shaped 76:11
Dibble 1:21 2:7 92:3,19
difference 54:8 59:8 68:10,13
different 21:22 27:17 51:11 59:6 63:14 89:5
differently 52:1 53:9
digital 15:6
Diplomate 92:20
directly 37:3
disable 67:16 68:22 69:6 72:7,10 76:17
disabled 33:7 68:1
disables 31:3,5 32:1 42:19 61:5 65:3,19 66:19,22 67:17 69:21 71:21 72:18,22 77:5
disabling 29:5 32:21 60:11,16,17 61:3,9 63:1 66:9 66:14 68:11,13 69:14 71:16
disclose 47:20 48:13 73:13
disclosed 60:3 62:11
discloses 25:22 73:12 82:13
disclosing 56:20 57:11
disclosure 45:21 47:19 67:21 72:6
discover 87:22
discovered 88:4
discovers 88:9
discovery 65:7
discuss 21:17 69:4 81:4 88:18
discussed 38:9 49:13
discusses 66:15
discussing 16:8 25:17 59:16
discussion 48:17 57:16
Document 14:22 22:22 27:2 29:13 30:17 31:18 39:3 49:11,17,21 51:3 60:20 61:16 62:18 70:21 75:22 78:4 81:1,12,15 87:1 87:18 89:20
documentation 49:16
documents 9:17,19 10:8
doing 7:12 18:17 63:18 70:19
download 11:6
Dr 6:5 10:17 11:2 23:12 25:6 48:12 79:17 80:5
drive 37:9
Due 7:5
duly 2:4 7:16 92:6
Dunner 2:11 3:8,14 4:1

E

E 7:2,2 92:1,1
e.g 14:11,12 26:2,3 41:16,17 44:6 85:1
earlier 15:5 17:7 29:14 39:11 47:15 49:13 50:3 83:4
ECC 12:15 16:15 18:13
echoing 24:19
EDT 2:6 7:3 48:10 80:3 91:11,14
eight 21:4
either 18:7,14 38:1 42:22
eject 63:18 69:3,6 87:4,16 89:6 90:4
ejecting 70:4 71:1 71:12 84:3 89:16 90:17
ejection 71:5,5 72:4 83:4 85:1,15 88:19
ejects 70:16
EJx 70:4,16,22 71:5,11 84:4 85:2 85:6,9 86:8
elaborate 39:10
electronic 10:21 15:20
element 84:17
embodiment 29:2 30:19,22 35:2 36:3,8 39:7 42:6 42:10 60:4,9
employed 19:15
encompasses 72:13
engage 62:7
ensure 7:7
entailed 63:19
entire 63:15 70:16

entitled 11:2
equating 85:15
ERRATA 94:1
erroneous 32:2
erroneously 19:4,8 19:9
error 12:9,15,20 13:18 14:15,18 15:3 16:8,15 17:13,14,18 18:1 18:2,21 19:21,22 20:4,12,19 21:6 21:14,16 22:5,18 22:19 23:5,15,21 23:22 24:3,5,11 24:13,17,20,21 25:7,7,11,12,12 26:4,9,20,20,21 27:9,13,19 28:2 29:21 30:4,7 31:10,15 32:5,16 32:20 33:3,3,10 33:10,12,12,15 34:3,9 42:11,18 43:7 44:7,14 46:11,16,21 47:5 54:12 57:9 61:5 62:2,4 64:9 65:13 66:1,15,21 67:14 68:18 69:12 70:8 72:8,16,18 75:5 76:2 78:18 79:5 80:14,20 81:7,7
error-condition 71:20
error-containing 31:6 32:2 63:13 64:1,6,10,17 65:4 65:8,19 66:9,14 66:22 67:10,18,22 68:14,18,22 69:7 69:15,21 70:10 71:17 72:7,10,22
error-free 31:11
errors 12:4 14:11 14:12,12,16 16:7 17:11 20:11,13,18 20:21 21:14 22:9 22:10,14 25:10,22 26:3,3,4,8,16 27:12 29:1,9 30:21 31:22 34:7 45:12 46:1 47:13 50:22 53:19 55:3 60:8 73:13,15 74:19 75:11 76:20 78:8,18,20 79:4
ESQUIRE 3:2,3,9 3:15 4:2
established 50:19
et 50:4 71:9,9
everybody 11:4
exactly 19:19 72:6
EXAMINATION 5:6 7:19
example 12:13,13 13:9,13 14:3,15 14:17 15:4 16:9 16:11,22 18:1,8 19:2 21:13 22:4 26:16,19 35:15,17 37:8 39:14 44:3 52:4 74:1 88:14 89:1
examples 12:11
exception 31:8,9 67:3,5,10 69:17 70:11 71:22 73:7 76:18 77:7,10,11
exceptions 47:1 61:7
executable 50:11
executed 38:17 39:21
executes 32:3
executing 41:14 72:1 85:1,6
execution 15:9 31:9 70:12
exemplary 36:2
exhibit 6:3,5,7 11:1 11:10 15:16,19 16:1 28:12,13,20 87:7
exhibits 6:1 9:21,22 10:19
expected 10:10
explain 87:14
explaining 89:4
explicitly 48:3 49:5 58:5
Explorer 2:11 3:16
express 45:20 72:6
expressly 59:12
extensively 19:15
extent 48:2
external 9:11
extra 17:9 18:7
extraction 31:11 32:5

F

F 92:1
fair 40:2 78:11
FAPR 1:21
Farabow 2:11 3:8 3:14 4:1
fast 37:1,2 55:21
fault 32:10
feel 11:18 25:2
Fellow 2:7 92:20
fifth 41:13 42:2
figure 16:22 23:4 30:20 31:1 35:14 35:18,20 36:1,3 36:21 37:16 42:5 42:9,16 45:4,11 45:15 46:20 48:4 49:19 57:15 59:17 59:17,19 74:1,2,5 74:6,10,15,19,22 75:2,3,5,6,9,13,13 75:16,18 76:1,10 76:21 77:5 82:18 84:11
figured 88:7
fine 79:19,20
finish 79:19
Finnegan 2:10 3:8 3:14 4:1
Finnegan's 8:19
firmware 50:11 51:5,6,14 52:8,22 69:4,18 71:4,5 73:8 77:11 81:3 82:14,20 83:6,9 83:15,19 84:3,22 88:2,6,10,13,21 89:9,12,22 90:12 91:2
firmware-type 63:4
first 11:1,5 12:1 25:21,21 26:17 34:15 35:1,2,22 36:11 42:18,19,22 44:7,15 46:12,16 46:21 50:22 59:16 71:8 76:3,17 77:5 79:4,5 87:10,19
flavors 50:4 55:19
flipped 16:13
flipping 22:16
Floor 3:5
flow 77:2 84:5 90:21
follow 32:18
following 62:20 74:19 86:3,19,22 90:2
follows 7:17
Foras 1:8 94:2
forgetting 9:3
form 13:14 17:15 18:22 20:14 22:11 24:14 29:11 30:8 32:17 34:4 44:1 45:8 46:2,18 52:19 53:21 55:5 55:16 57:13 58:19 59:14 64:8 65:9 66:11 67:12 68:2 72:11 77:15,22 78:15 82:6 83:18 85:17 89:17
forth 13:11 47:1 48:19 49:19 72:4 90:7 92:6
foundation 16:19 33:13
fourth 41:2
FR 29:22
FRC 26:1 27:5,8,16 27:22 28:9 29:1,5 29:9,19,21 30:1,4 30:5,20,21 31:3 31:13,21 32:9 33:11,15 36:10 38:7,9,13,15,18 38:19,21 39:9,16 39:20 40:2,6,16 41:2 42:7 43:3,6 43:10,14,16,18,20 44:6,8,12,14,17 44:21 45:5,11,17 46:6,11,20 47:16 47:20 48:3,13,22 49:5,14 50:1,3,5 50:10,18,20 51:5 51:13,21 52:4,6 52:17,22 53:11,15 56:20 57:1,7,8,11 57:19 58:3,10,15 58:17,21 59:7,12 60:4,7,12,16 61:3 61:22 62:1,6 63:20 65:11,13,16 65:18 66:17,19 67:13,17 68:6 69:14 71:8 72:8 72:20
FRCP 92:9
free 11:18 25:2
front 36:9,17 37:10
full 8:2
fully 24:1
function 35:4
functional 36:10 38:6 39:19 76:5
functionality 32:3 33:21 63:2 69:9 69:18,19 70:13 71:22 79:7 88:3 88:16
further 13:10 60:4 82:17 91:6,13

92:12

G

G 7:2
Garrett 2:11 3:8,14 4:1
general 13:7
generally 16:20 40:15 55:17 64:12
generate 41:15 76:17
generated 24:21 25:11 27:8 29:20 30:3 41:20 42:1 43:6 54:11 55:9 58:11,16 75:9
generates 31:7 67:3 71:21 73:7 77:6 77:10 82:21
generating 61:7 69:17 83:2
generation 67:9 70:10
generic 19:1
generically 17:16
Georgia 4:4
getting 34:11 55:6 67:7
give 14:17 21:13 45:20
given 8:15 28:7 54:20 92:8 93:4
go 14:20 18:17 25:8 26:11 37:9 38:22 42:9 47:22 48:20 52:7 58:7 60:18 61:6 70:2 71:10 79:21 81:9
goes 31:9 32:2 52:6 61:7 64:14 66:2 67:5 71:16 73:2,6 84:2
going 11:3,6 15:1 22:1,6,20 26:22 27:10 31:19 38:22 48:5 50:8 52:2 54:19 55:8,9 57:8 59:1 78:8 79:10
good 7:22 53:3
grabbed 56:10
GROUP 3:2
guess 13:19 14:21 15:1 17:16 19:13 20:2,8 22:20 23:1 24:16 25:8 28:8 30:20 33:16 37:3 42:4,14 47:22 48:4 49:12 51:7 52:1,20,20 53:9 55:6 56:9 59:15 66:12 72:13 77:9 81:17,19 87:19

H

half 73:11
halfway 39:18 61:1
hand 92:17
handle 14:10 78:20 79:3
handled 33:6
handler 31:10
handling 22:13 25:13 32:5 77:18 78:6,7,10
happen 47:1
happened 63:5
happening 68:18 84:1
happens 24:7 63:21 64:9 66:16
hard 9:20 11:18 27:1 37:9
hardware 29:3 30:20 31:1,5 32:21 34:12 42:17 42:17 44:6 50:11 60:3,9 61:5 62:4 65:3,14,17,18,19 66:18 67:15,17 69:12,13,16 70:7 71:20 72:15,17,17 72:21 76:2 88:10 88:11
hear 20:15 23:17 58:13 86:16
heard 7:7 66:13
Henderson 2:10 3:8,14 4:1
hereinbefore 92:6
hereunto 92:16
hierarchy 57:5
high 12:21 64:11 73:2
high-level 17:8 42:8
higher 59:2 64:15
highlight 75:17
home 56:10
hot 71:1 83:11,17 83:22
hour 48:6,6 79:11
huge 57:15
hypothetical 21:1 53:2

I

i.e 81:8
idea 13:7
identical 38:16,17 39:20,22 41:5
identify 14:16 49:7 58:10,16 83:16
idle 82:15 85:7
idling 71:12 84:4 85:10,15 86:8 87:3
illustrate 45:16
illustrated 36:7 39:7 44:5 45:4
illustrates 36:1 42:5
illustration 59:16 74:13
implementation 18:6 21:11 52:14
implemented 50:10
implementer 20:9
implementing 51:13 81:18
include 18:19 20:12 20:20 36:9 54:16
includes 30:20 39:8 60:4
including 26:2 70:17
inconsistencies 27:7 29:20 30:3 43:5 53:13,15 54:10 58:11,16
incorporate 76:6 77:16
incorporated 50:12 80:11
incorporating 78:17 82:7
incorrect 16:13
independently 40:12
INDEX 5:1
indicate 19:21 27:8 29:21 43:6 44:11 45:5 53:15 54:11 55:3 71:4 76:16 80:9 82:4,13 83:13 84:21
indicates 29:19 36:1 44:21 60:6
indicating 43:9 46:14 57:8 77:14 85:5
indicative 67:10
individual 24:22 29:1,10 30:21 31:22 55:14 60:8 67:14 72:16
information 17:19 18:7 19:2,18 37:10 38:4 45:14 49:15 50:15 53:4 53:4,8
initial 69:10
initiates 32:6
inoperable 33:7
input 73:3
inquires 83:9
inserting 78:12
instance 2:3 23:14 23:20 28:7 42:16 46:4 89:11
instances 19:9
instruction 21:20 22:1 25:16 41:11 57:3 64:19
instructions 37:22 38:16 39:20 41:5 41:14
instructor 64:20
Intel 50:1 68:5
intention 40:5
interested 92:14
interfaces 88:3
internal 71:3 84:21
internally 15:8
interrelate 89:2
interrupt 82:21
interruption 66:5
interrupts 83:3
interval 81:6,8
introduce 11:1 26:13,14
invention 36:4
invoking 81:18
IPR2023-01373 1:11
issue 18:8
issued 68:22 72:10
issues 13:11,11
Itanium 28:8 50:2 68:5
IX.B 11:20

J

JOB 1:22
JOHN 3:2
jpetrsoric@bclg... 3:3
July 1:17 7:3 92:17 94:3
jump 26:22 31:20 73:22
jumping 39:4 81:13

K

Kara 4:2 9:1
kara.specht@fin...

4:2
keep 19:17 22:6
kick 33:16
kicks 67:5
kind 38:2,4 47:14 53:1 63:7 88:7
know 11:8,14 16:4 19:16 21:7 27:15 27:17,18 28:17 34:21 37:6 42:19 46:22 51:4 56:9 58:22 59:3 63:4 66:21 89:6
knowledge 88:11
known 12:3
knows 27:17

L

L1 17:18 42:21 56:12
L2 59:8
Lane 3:10
language 15:3 30:16 63:22 81:11 84:17 85:7 89:21 90:2
laptop 9:11
large 21:6
larger 33:8 64:18
Lavenue 3:15 9:5,5 9:6
LAW 3:2
layer 21:3 31:11 32:5 51:8,9 53:4,4 53:7 67:6 68:7,7 69:18 70:12 72:1 83:2
layers 51:11 63:4 72:13 89:6
leave 34:9
left 33:7 79:18
left-hand 39:6
leftmost 27:4
lengthy 63:1
let's 16:13 17:10 21:3,4,22 42:20 57:6 65:13 67:14 72:19 76:3 79:21
level 12:21 59:19 61:5 64:12,15 71:13 73:5
LIMITED 1:8
line 16:12,22 17:18 18:8 21:4,7 41:8 46:5 55:7,10 86:14 88:5 90:10 90:22
lines 10:13 65:12 86:13,14 87:11,15 88:18 89:8 90:5
Lionel 3:15 9:2
lionel.lavenue@f... 3:15
little 37:1 39:11 48:6
LLC 1:5,5
LLP 2:11 3:8,14 4:1
Ln 94:5
loading 12:14
location 2:10
lockstep 12:4,4 13:2,2 20:11,18 21:18,20 23:6 24:6 26:1 29:3 31:1 32:1 40:4,7 41:7,8 60:10,17 61:1,9,13,13,22 62:4 63:21 65:15 66:17,19,20,20 67:16 69:13 70:9 71:21 72:18,20 73:13 74:3,16,18 75:21 76:7,12,15 77:13 80:12,14 82:2,8,19 89:10 89:10,22 90:1,11 90:19 91:1
logic 23:9 26:1 27:5 27:16,22 29:1,9 29:19 30:1,5,21 31:13,21 32:9 33:11,17 36:10 38:7,9,13,18,19 41:2 42:7 43:3,10 43:14,16,18,20 44:6,12,14,17,21 45:5,12 46:6,11 46:20 47:17,20 48:3,13,22 50:6 50:10,19,20 51:13 51:21 52:4,7,17 52:22 53:11 56:20 57:1,8,11,19 58:3 58:10,15,17,21 59:12 60:4,7 62:2 62:6 65:13 67:13 72:8
logical 33:4,20,22 35:5 39:9,14 40:8 41:3,12 44:9 54:7 61:20 63:5 64:18 71:13 76:4
logistics 15:12 28:11
longer 33:22 72:21 88:6
look 11:9 18:5 25:8 25:18 34:19 49:6 53:3 59:1,21
looking 40:13 43:15,18 46:20 53:13 54:5 57:1 57:19 58:3,12,18 59:18
looks 9:10,11 30:19 31:4 32:18 35:20 39:17 41:8 56:22 60:18,21 63:20
loss 12:4 74:17 75:20 82:19
lot 22:7 51:14 52:9 52:12 55:18
loud 8:15
low 73:2
lunch 79:15,18

M

M 3:15
machine 22:6 31:8 31:8 46:22 67:9 69:17 70:11 76:17 77:6,8,10
Madison 3:4
making 42:21
manner 16:17,18 64:21
marked 11:11 16:2 28:14
markings 10:8
marriage 92:13
Massachusetts 3:11
master 90:12 91:2
materials 10:4
matter 92:15
mean 13:6 16:18 20:22 26:8,15 66:12 73:20 80:18
means 2:9
meant 75:7,13
mechanisms 19:14
medical 10:14
memory 19:15 36:11,13 37:2,17 37:20,21 38:3 49:4 55:11 57:16
mention 12:12 24:4 49:12 78:5 81:16
mentioned 37:12 45:10 62:10 63:10
mentioning 15:5
mentions 49:22 50:2,10 60:22 62:19
method 70:4,16,22 71:6 85:2,6,9 86:8 87:4,16 89:6 90:4
methods 69:3 70:3
Michael 1:16 2:2 5:6 6:5 7:15 8:4 11:2 92:5 93:9 94:4,22
microphone 9:12
Mike 79:12 91:8
misinterpreting 47:14
mismatch 14:12 21:14,16 22:1,9 22:18 23:7,8,15 23:20 24:3,7,10 24:17,20 25:6,9 25:12,12 26:3,8 26:20 27:8,12 29:21 30:4 43:6 53:15 54:12 57:9 61:14,14
mismatching 27:15
Mm-hmm 41:1
mode 29:5 31:3 38:15,21 39:9,12 39:16,20 40:2,6 40:11,16 44:8 49:14 50:2,3 51:5 60:12,16 61:3,4,9 61:22 62:1 65:16 65:18 66:19 67:17 68:6 69:14 72:20 76:5
modifies 71:3 84:2 84:21
module 64:18 67:4 67:7 70:14 71:14
moment 29:8 64:2 71:19 91:5
moments 62:12
monitor 9:12 46:9 46:15 47:3 48:3 51:10,15,21 52:13 52:17
monitored 53:8,18
monitoring 30:1 43:16 45:6,11,12 45:13,22 46:11 47:7,10,12,20 48:14,22 49:5 50:15,22 56:20 57:12 59:12
monitors 27:5 43:3 44:21 46:6 47:17 50:6 52:4 53:11
morning 7:22 8:1
mouse 43:13 46:4
move 57:4
moving 52:10

multilayer 72:14
multiple 72:13
multiprocessing 40:11
multistep 61:10 63:17 64:5

N

N 7:2
name 8:2 9:1,2,4 94:2
nature 7:5
need 13:3,5 16:10 18:5 25:8 42:14 47:1,22 48:20
needs 17:1
network 37:8
New 3:5,5
Nguyen 13:20,22 14:6 22:13 28:7 34:8 68:3 69:5 76:8,13,14 77:14 77:17,20 78:1,9 79:3,8 81:3,9,11 81:13,18,20 82:1 82:3,7 85:12
Nguyen's 74:16 77:17 78:6,12,17 80:11 81:5
non-FRC-checking 40:18
non-recoverability 82:4
non-recoverable 12:6,19 13:18 14:12 21:14 22:5 22:9,14,19 23:22 24:13 25:7 26:3 26:16,19,19 27:19 28:2 33:3,12 34:2 34:7 73:15 74:19 77:18 78:8,19 79:9 81:8
nonfunctional 34:10
NORTH 1:5
Notary 1:21 2:8 92:3
noted 91:14 93:5
notes 9:17,19 10:7
notice 75:4
notifies 83:10
Notify 83:12,13,16
notifying 83:21
notion 81:5
number 6:2 12:11 12:22 20:6 21:7 68:4
numbered 2:5
numeral 11:20
NW 4:3

O

O 7:2
o0o-- 91:15
Objection 13:14 16:19 17:15 18:3 18:22 20:14 22:11 24:14 29:11 30:8 32:17 33:13 34:4 44:1 45:8 46:2,18 52:19 53:21 55:5 55:16 57:13 58:19 59:14 64:8 65:9 66:11 67:12 68:2 69:22 72:11 77:15 77:22 78:15 82:6 83:18 85:17 89:17
objections 7:12
observe 21:21
occur 25:10
occurred 33:15
occurs 72:7
offhand 75:12
office 1:1 8:19
offline 71:4 84:22
oh 68:12
Okay 11:13,15,17 11:22 15:21,22 22:18 23:14 25:20 28:16,18,21 49:10 54:3 58:15 60:1 60:21 79:21 80:1 80:8 86:7 87:19
once 90:10,22
online 89:1
onward 62:21
operable 39:8
operate 28:9 38:15 41:11
Operated 39:19
operates 41:3
operating 13:8 21:18 35:6 39:14 39:15 40:12 43:10 43:21 44:8,12 57:2 61:20 71:2 82:14,22 83:6,8 83:17,21 84:1,14 84:20 86:7 90:18
operation 29:5 31:3 39:13 41:7,9 42:21 44:22 45:6 58:6 59:3 60:12 60:16 61:3 65:6 69:15
operational 90:13 91:3
operations 27:6 43:4 45:21 46:7 47:17,21 48:14,18 49:8 50:6 52:5 54:5,8 56:19,21 57:12,20 58:4
opinion 25:6 32:14 32:15 85:22
opposed 40:10
ORAL 1:15 2:2
ordered 64:19,20
ordinary 14:9 51:20 52:16 53:16 54:15 55:1 56:5 80:10
original 77:9
OS 83:22 87:21 88:2,5,7,21 90:5 90:13 91:3
outcome 92:14
overall 33:18 68:6
Owner 1:9 2:4 3:8

P

P 7:2
p.m 2:6 80:2,3 91:10,11,14
package 29:4 31:3 33:18,20 35:3,10 35:13 36:2,8 37:5 37:5,6 40:8 50:16 50:20 52:8 57:21 60:11 61:2,5,18 61:19 65:16 66:1 66:17 67:1 68:12 68:15 69:8,10 70:17
package's 31:5 50:13 65:3,19 72:22
packages 39:8 68:8
page 6:2 11:21 23:4 24:16 25:19 28:19 34:20 40:22 59:22 73:11 74:7,9,13 75:2,9,16 80:7 81:6 82:12,13 86:1
pages 74:1
pair 12:4 26:1 39:8 80:15 89:11,12,15 90:1,11 91:1
PAL 31:10 32:3 33:16,17 51:7 52:9 67:6 68:6 69:18 70:12
PAL/SAL 88:14
paper 10:17
para- 24:18
paragraph 12:1 14:7 21:12 22:21 25:18 26:11,17 27:1,4 28:20,22 29:12,17,19 30:1 30:9,13,18 31:14 31:16,21 32:13,16 32:20 33:11 34:15 34:16,19 35:18,20 35:22 36:7 38:10 39:5,17,19 40:21 43:2 44:3,13,20 46:9 47:8,16,16 49:3,13 52:2 54:4 56:18 57:1 59:21 60:2 61:17 62:11 62:20 63:8,12 65:2 66:15 70:7 71:19 73:11 74:7 74:9,11,14 78:5 80:6,9 82:12 84:10,10,20 85:14 86:1,6,19,21 87:11 90:3,20
paragraphs 51:6 62:17 64:15 78:1 78:6 80:22 81:4 81:17,19,22 82:3 84:6
parenthetical 84:13,16
parity 15:8 17:6,18 18:7,20 19:2,7,21 19:21 20:3,12,20 21:5,10 47:3,7,10 53:17 54:16,21 55:2,8 56:6,7,12
Parity/ECC 19:14
part 16:15 51:9 52:10,13 61:9 68:17 72:3 77:17 78:13 83:2 85:9 89:4,7
particular 26:16 45:21 53:20 64:4 64:5 66:4,7,8 67:21 68:21 69:20 88:17
particularly 70:4
parties 7:7,9 92:13
parts 48:1,21
party 92:11
passive 16:16,18
patent 1:1,3,9,12 2:3 3:8 6:3,7 12:3 14:20,21 15:2,13 15:14 18:11 19:12

19:12 85:12,13,18 85:21 86:3,12,13 86:18 87:5,8,8,15 88:18,21 89:9
pause 7:6
PC 3:2
pentium 50:4,5
people 55:19
perceiving 69:12
perform 82:10 83:3 86:8 88:3
performing 69:19 73:8,14 74:4 81:3
person 14:8 51:12 51:19 52:15,21 53:16 54:14 55:1 56:5 80:10 81:2
Petitioner 1:6 3:12 3:18 4:5
PETRSORIC 3:2 5:7 7:21 9:7 11:12 13:17 15:11 16:3 17:2,21 18:18 19:5 20:16 22:17 23:10 25:4 27:21 28:15 29:18 30:12 31:12 32:12 33:1 34:1,14 40:1 44:10 45:19 46:13 47:2 48:5,11 51:18 53:6 54:1 55:12 56:2 58:1 59:10,20 61:11 62:9 63:9 65:1 66:3 67:20 68:9 70:15 71:15 73:9 76:9 77:19 79:1 79:16 80:4 81:21 82:11 84:8 85:20 87:6 90:8 91:6
Pg 94:5
PH.D 3:9
phrase 52:1 79:6
physical 33:19,20 40:7,18 53:12 61:19,19,21 62:3 62:5 66:21
picture 10:1
piece 54:20
place 11:3 60:22
placed 64:7 67:11
places 18:12 50:16 50:20 52:7
placing 63:12 65:4
platform-indepe... 32:6
please 7:6 8:2 11:18
plurality 42:12 44:7
point 13:19 25:2 35:5 42:10 59:15 65:20 78:3 89:1
port 37:8
portion 43:12 45:2 66:4,7,8 76:7,10 87:19 88:17
possibly 55:9
potential 53:14 61:14
potentially 52:13
prefer 26:13
prepared 74:2
present 3:9,16 4:3 17:12 36:3 55:22 72:21 87:22 88:10 88:11 89:2,6
presenting 40:7
presently 8:18
presumably 58:7
prevent 10:14
previous 17:22 24:4
primarily 86:5
prior 10:5 12:11,22 22:12 39:2 40:15 45:16 80:21 81:4 90:2
private 36:13 37:1 37:13,14,15 41:16 41:21 42:3,22 45:7,9 47:7 52:17 55:14,22 56:4,7 56:12 58:4,9,12 58:18 59:2,4,13
probably 11:5 18:5 42:4 63:7 79:17 86:22
problem 12:3
problems 13:10
PROCEEDINGS 5:4
proceeds 33:16
process 32:19 44:5 61:10 62:19 63:1 63:15,18 64:5,6 67:6 68:6,17 72:3 78:13 83:2,4
processing 41:15 69:1
processor 15:7 21:2 24:22 26:4,9,20 27:6,12,14 29:1,4 29:4,10 30:6,6,22 31:2,2,10,11,15 32:11 33:5,18,22 35:2,3,5,9,13 36:2 36:8,11,12,22 37:5,12,14,15 39:7,8,9,15 40:3 40:19 41:3,4,12 41:14 42:12,18,19 43:4,21 44:7,8,9 44:15,21 45:6,13 46:1,6,10,12,16 46:21 47:5,17 48:18 50:6,16 51:1,8 52:5,7 53:3 53:7,11,20 55:15 58:17 60:8,10,11 61:2,2,15,18,19 61:20,21 62:3 63:3,5,15,22 64:18 66:1,16 67:4,7,14 68:8,11 68:11,14,15 69:8 69:14 70:10,17 71:1,4,14 72:1,16 72:19 76:3,4 77:6 79:5 80:14 83:11 83:16,22 84:4,22 85:1,16 88:15 89:11,12,15 90:1 90:7,11,12 91:1,2
processors 12:5 13:1 22:2 23:5,16 23:22 24:6,12 25:11 26:1 27:15 28:1,8 32:7 38:2 41:10 42:13 49:14 60:17 63:10 71:12 82:15 84:5 85:8 85:10,15 86:9 87:3,16 88:4,6,19 89:16 90:17,18
produce 21:21
produced 2:3
producing 21:20 22:3
Professional 2:8 92:20
program 17:10 82:21
programs 9:14
properly 78:19
protect 18:13
provided 38:16 39:21
providing 41:4
Public 1:21 2:8 92:4
Publication 6:8
pull 32:7 87:7
purposes 15:12,18 28:11
pursuant 92:9
put 34:10
puts 31:6 67:2
putting 67:18 69:15

Q

queries 83:6,9
query 83:10,21
question 18:1 19:20 20:15 24:2,18 44:17 58:13 66:13 69:11 72:12
questions 8:11,12 91:7,13
quick 70:19
quite 51:17
quote 66:13

R

R 7:2 92:1
range 8:7
RATYCZ 3:3
RDR 1:21 2:7 92:3
re-ask 66:6
reacts 33:9
read 61:12 77:5 93:1 94:5
reading 23:18 29:16 51:20 76:22 86:16 89:18
reads 28:22 38:14 41:2 84:20 89:9 94:5
really 33:6 42:7
realtime 2:9 92:21
reason 10:13 52:10 94:5
reasons 56:11
recall 14:5 25:16 28:3 48:16,17 49:3 50:3
receive 37:11
received 16:5 28:17
Recess 48:9 80:2 91:10
recites 36:7 43:3 61:12 90:10
record 8:3,10 79:22 92:8
recover 89:10,22
recoverability 78:12 80:13,20 82:4,10
recoverable 12:5,9 14:11,15 17:14 26:2 32:16 33:2,3 33:12 34:6 73:13 73:15 74:3,17,18 76:7,13,15 77:13 78:19 79:8 80:12

82:3,9
recovered 23:6 24:6 90:12,19 91:1
recovering 73:12 78:9
recovery 81:18
red 76:21
redundancy 36:10 38:7 39:19 76:5
reenabling 71:7
refer 10:19 11:17
reference 13:20 14:6 23:2 25:9 39:2 64:4 74:22 75:8 76:8 77:17 81:14 86:12
referenced 17:7 85:11
references 10:3,5,6 12:22 22:12 34:8 35:9 40:15 45:16 68:4
referring 15:13,13 16:7 17:6 29:15 30:10 36:21 42:2 43:18 60:16 62:15 74:6 75:6
refers 31:7 41:13 63:12
refinding 60:22
Regardless 33:9
Registered 92:20
reintroduces 90:12 91:2
reintroducing 90:17
relate 89:16
related 92:12
relating 32:16
relation 45:3
relationship 88:20 90:5
remember 75:14 76:19
remote 1:15 2:2 3:1 7:6
remotely 2:9 7:10 7:11
removal 32:7,8 71:2 83:11,17,22
remove 33:17 34:9 63:2,15 68:7 69:7
removed 33:5 63:6 67:7 88:12 89:3
removing 32:21 63:10 68:11,14 69:9
reported 1:20 2:8
reporter 7:5 8:10 8:16 10:20 15:20 62:8 92:20,21
Reporters 2:8 92:20
reporting 7:6
request 83:11 84:1
requested 92:10
requests 71:4 84:22
required 83:17
reset 77:14,21 90:11 91:1
resets 89:12
resetting 14:1,2 81:10 89:15
respect 20:11,18,19 35:18 45:22 63:11 81:22 82:18 85:13 85:22
respective 54:6 59:4
respectively 36:14
responds 83:10,21
response 72:8 82:19 83:5
responsive 80:13 80:19 82:2
rest 46:22 62:7
restarting 13:22 81:11
Reston 2:12 3:17 8:19
result 21:9 22:3,6 28:2 42:20 61:13
resultant 42:20
results 21:22 27:8 27:19 29:20 41:15 41:20,22 42:1 43:6 54:11 58:11 58:16 61:15 72:2 73:7
resumed 13:2
retrieve 10:21
return 76:16
review 14:22 22:22 27:2 29:13 30:17 31:18 39:3 49:11 49:17,21 51:3 60:20 61:16 62:18 70:21 75:22 78:4 81:1,12,15 87:1 87:18 89:20
reviewing 30:15 62:16
revisiting 22:21 29:12 31:16 78:3 80:21
right 9:13 14:17 27:3,18 28:1 29:14 30:16 35:20 38:20 40:16 49:2 60:5 70:22 73:17 75:7 77:5 87:2,9
rightmost 76:10
ROBERT 1:5
robust 14:10
Roman 11:19
roughly 87:20
routine 81:19
Rule 92:9
run 34:13
run-time 88:15
running 9:8,15 40:3,7 60:17
runs 32:6

S

S 7:2
S-A-L 82:20
Safford 23:2,2 45:15
SAL 33:16,17 51:7 52:9 68:7 82:20 83:2
sample 51:11
sampling 44:18 45:17 50:14,15
satisfies 85:7
saying 29:14 30:19 31:4 32:4 47:15 47:15 52:20 54:5 56:22 58:6 61:17 65:11 82:1 86:10 86:10
says 13:22 19:14 27:5 31:21 34:10 38:20 48:2,22 50:5,13 52:4 65:17 67:13 72:15 72:21 88:7
scenario 13:16,18 13:21 16:11 17:8 17:14 20:12,20 23:3,6,7 24:7 25:1 25:1 27:13 28:3 32:8 33:14 34:8 41:10 62:5 71:1 77:18 78:10,10 82:8
scenarios 14:5 28:10
scheduling 90:6
SCI 82:22 83:5,7 83:20
scrolling 43:13
Seaport 3:10
search 70:19
second 11:7 14:7 21:12 35:2 36:6 36:12 38:10,14 44:4 46:5 60:2 71:8 73:11 74:14 81:11
second-to-last 73:18
section 11:19 70:3 78:2 84:18
see 11:14 15:2 19:2 19:7 26:6 29:6,7 30:4,5,9,11 35:7 36:15 39:1,4 40:13 41:18 44:15 44:18 45:9 47:6 48:1,21 49:7 54:3 58:5 60:13 72:5 73:1,4,16 77:8 80:16 89:13
seeing 32:20 54:7 57:4
seen 60:7 72:18
sees 61:20
send 37:7,10
sent 11:13 28:16
sentence 12:2 14:7 21:12 25:21,22 26:17 27:4,10 28:22 29:7,15 34:15 35:1,9,22 36:6 38:10,14 39:5 41:2,13 42:2 43:2,9,17 44:4,11 44:16,19,20 45:10 46:5 52:3 56:18 56:19 57:10,18,19 58:3,6 59:18 60:2 60:6 61:12 73:18 73:21 74:14 84:9 84:9,19
sentences 44:16 62:11
separate 40:19 65:6
sequence 32:7
service 63:6
session 79:18
set 9:10 17:9 19:4,8 19:9 21:8 92:6,16
seven 65:12
shared 27:7 30:2 36:9,11 37:3,17 37:20 41:17,21 42:3,7,22 43:5,10 43:15,19 44:22 46:8,15 47:4,13 47:18 48:15 49:9 50:7 51:22 52:6 53:8,12,18,22

54:9,16,21 55:7 55:11 56:1,4,8,13 56:21 57:5,6,12 57:21 59:1,9,18
SHEET 94:1
short 79:20
show 10:1 74:4 75:1
showing 42:8 57:7
shown 23:3 35:14
shows 74:20 75:2
side 36:9,17 37:10 77:5
signal 24:20 73:2,3
signaled 23:8
signature 92:9
similar 15:5 19:15 45:15 75:13 84:6
similarly 59:8 84:19 85:11 89:8 90:9
simplicity 38:1
single 35:4 39:9 41:3 44:9
singular 62:3
sitting 55:7,21 56:3
six 64:15
sixth 43:2 44:20 46:5 52:3 56:18
size 38:3
skill 14:9 51:12,20 52:16,21 53:16 54:15 55:1 56:5 80:10 81:2
slash 52:9,9
slower 56:1 57:5
small 37:1 55:21
soft 14:11,16,18 15:3 16:7,8 18:1,2 20:12,19 21:6 26:2
software 35:6
solution 18:6
somewhat 20:22
sorry 9:4 38:12 41:22 42:21 59:9 61:19 64:20 66:6
sort 16:21 19:1 21:5 24:16,19 32:10 44:17 53:1 57:18
sorted 42:15
sound 28:4 86:17
sounded 24:2
sounds 19:11 20:22 24:9,15,22 40:16 61:8 72:12 75:7
source 83:7,20 84:16
speak 16:17
speaking 7:7 16:20 17:17
Specht 4:2 9:1
specific 16:11,11 18:6 25:9 42:15 50:1 72:9
specifically 20:19 75:15 82:20 90:4
specification 39:11 48:1,21 71:11 86:18 89:7
stage 63:20
start 11:9 21:19,21 23:1 31:19 36:19 44:4 69:19 72:1 86:2
starting 19:13 39:5 65:12 89:21 90:20 90:22
starts 11:20 32:8 45:10 50:18,21 67:6
state 8:2 12:2 14:8 26:18 27:12 31:7 32:3 34:11 61:6 62:10,14,20 63:11 63:13 64:1,4,7,11 65:5,21 67:2,11 67:19 69:16 70:9 70:14 73:6,12
stated 29:8
states 1:1 6:3,7 30:18 35:1 39:1 39:18 40:14 57:18 57:18 60:3 65:2 73:4 74:15 88:22 93:3
stating 44:14 88:12
stenographic 2:9
step 64:5 74:15,16 75:17 76:6,14 81:3
steps 62:7 68:19 73:8 74:4
stick 24:16 37:22 50:9
sticks 65:20
stopping 90:6
storage 19:16 38:3
store 27:6 43:4 44:22 45:6 46:7 47:17,20 48:14 49:8 50:6,7 52:5 56:18,21
stored 41:16,20,22 42:3 55:10,14
stores 50:7
stream 21:20 40:19 59:2
streams 25:16 41:11 59:1
Street 2:11 3:16 4:3
strike 17:4 32:14 47:11 68:12 83:14
string 57:3
strip 54:20,22 55:3 55:11
structured 64:20
structures 71:3 84:2,21
stuff 37:4
submitted 59:3
subsequent 68:19 75:9
suffering 12:17
suggesting 52:15
Suite 2:12 3:17 4:4
support 68:5 88:15
supporting 88:13
supposed 57:3
sure 10:1 11:6 20:17 23:19 24:1 25:1 26:22 34:5 48:8 65:10 66:12 79:13 86:2
surrounding 30:16 89:18
switched 17:1
sworn 2:4 7:11,16 92:7
system 12:16 13:4 13:10,22 14:2,10 18:16 20:3,6,9 21:10 32:5,21 35:6 37:11 39:15 40:17 51:8,11 53:4 58:20 61:20 62:22 63:3,4,16 64:19 67:8 68:8 68:15 69:8,10 71:3 72:14 74:12 77:14,21 82:14,21 82:22 83:6,8,17 83:22 84:1,14,20 86:7 88:1 89:1,3 90:18
systems 28:9 68:5,5

T

T 92:1,1
tables 87:22 91:4
take 8:16 11:7 48:7 79:12,15,18,22 80:12 91:8
taken 2:4 13:3,6,13 13:16 14:3 48:9 77:20 80:2 91:10
talk 22:13 23:2 25:1 34:5,6 37:2,7 47:9 53:10 56:11 69:2 70:5 81:6 82:10
talk- 72:2
talked 12:22 21:19 28:8 35:15 44:9 46:10 50:2 71:19 83:20 88:13 91:5
talking 27:19 39:12 41:9 46:7 47:6,10 48:17 49:2 50:18 50:21 51:5 54:3 55:7 57:15 59:17 61:18 67:1 69:11 70:6 72:3 74:12 78:6,7 83:3 84:7 84:18 87:2,20 88:16 90:3,21
talks 13:20 14:6,20 18:11,13 19:12 23:3 35:21 39:16 42:9,11 43:16 44:2 46:3 49:13 49:14 51:7 62:21 68:4 71:2,7 78:9 81:9 83:1 91:3
tasks 90:6
taught 77:14,20 86:11,11
teach 29:9
teaching 59:12 76:16
Technologies 1:8 94:2
telecommunicati... 18:15
tell 9:22 10:11,15 12:9,19 36:17 62:14 80:18
tells 83:20
terms 20:9 38:3 42:15 63:15 70:6 78:9
testified 7:17
testimony 19:6 92:8 93:3
text 89:18
Thank 9:6 91:12
thing 38:5 49:12 53:10 57:6,7 81:8
things 10:6 12:16 12:18 13:1,3 15:9 22:7,8 33:7 34:13 45:3 48:2 49:4 51:14 52:12 56:14 57:17 62:21 63:1

67:5 89:2
think 10:3 16:10 19:19 22:12 29:16 38:19 39:10,12 40:14 45:15 46:5 49:2 52:3 56:15 57:14,17 59:7 64:9,11 73:17 76:19,21,22 81:10 84:6
third 28:22 39:5 60:6 84:9
threads 34:13
three 8:21 76:22
threshold 73:14,21
time 12:2 20:15 23:17 58:14 64:2 79:15 88:10 91:14
timeout 81:5,7
times 8:5
today 9:18 10:11 10:14
ton 51:10
top 19:13
total 63:18
totally 86:3
TRADEMARK 1:1
transcript 93:2,3 94:1
TRIAL 1:3
triggering 82:14 84:14
triggers 70:12
true 92:7
truth 10:11,15
try 25:15
trying 19:20 25:5 26:15 54:18 64:3 72:5
turn 11:19 28:19 80:5
turning 40:5 73:10
turns 61:4 65:16,17 65:18 72:20
two 3:10 21:18 22:2 23:4,16,22 24:5 24:11 27:14,14,17 29:3 31:2 36:22 37:12 39:13 40:6 41:10 53:12 57:2 57:20 58:17,22 59:2 60:10 61:2 61:15,21 62:5 65:15 66:18 67:16 69:13 72:19 74:1 76:4,22
type 9:8 18:9 55:20
typically 18:6
typographical 75:10 76:20

U

U.S 1:12
ultimately 63:2
understand 8:9,14 10:10 19:6 26:15 51:13,21 52:16,21 53:17 54:15 55:2 56:6,15 57:10 59:11 64:3 82:17
Understandable 11:8
understanding 24:1,18 41:7 51:19 56:19 58:2 60:15
understood 14:9
undesirable 22:7
United 1:1 6:3,7
universe 51:9 53:2
unwinding 25:15
updating 91:4
upload 10:19 15:18 28:11
uppermost 21:3
use 18:12 19:2 20:10 34:12 40:17 40:17 50:14,19 56:12,13 75:8 87:4
uses 20:4 63:22 64:10 81:11 87:15 88:12
utilization 90:4
utilizing 38:20

V

v 1:7 94:2
value 15:7 16:13 59:5,5
variability 20:8
various 10:19 13:1 22:13 25:13 50:16 50:20 52:7 69:3 87:5
versus 82:4
view 35:5
Virginia 2:12 3:17 8:19

W

wait 26:12
want 20:10 46:8,15 50:17,21 56:11,13 82:17
wanted 18:17 37:7 53:1
way 15:21 17:20 28:7 33:6 43:1 45:3 92:14
ways 22:13 25:13
we'll 37:22
we're 42:16 51:5 55:20 66:20 67:1
we've 41:9 48:5 60:7 79:10 88:16
webcam 9:12
WEDNESDAY 1:17
weeds 54:19
well-known 88:22
went 9:21 56:10
WHEREOF 92:16
witness 2:3,10 3:9 3:16 4:3 7:11 9:3 9:6 48:8 79:13 80:1 92:5,8,10,10 92:16
word 50:14 64:11
words 8:15 77:1
works 89:4
world 67:8 88:8
write 42:21 48:18 54:5,8 57:20 58:3 58:6 59:3
writes 27:6 30:2,4 43:4,18 44:22 45:7 46:7,9,10,15 47:18 49:9 50:7 52:5 53:12 57:1,4 58:9,12,18 59:18
writing 59:4,5
wrong 15:7 27:18 28:1 64:12 65:8

X

X 93:8 94:21
Xirui 3:9 9:2
xirui.zhang@fin... 3:10

Y

yeah 17:8 39:18 40:13 49:20,22 51:16 65:17 77:8
yep 11:15
York 3:5,5

Z

Zhang 3:9 9:2 13:14 16:19 17:15 18:3,22 20:14 22:11 24:14 29:11 30:8 32:17 33:13 34:4 44:1 45:8 46:2,18 52:19 53:21 55:5,16 57:13 58:19 59:14 64:8 65:9 66:11 67:12 68:2 69:22 72:11 77:15,22 78:15 79:10,14,21 82:6 83:18 85:17 89:17 91:8,12
zombie 31:7 32:3 34:11 61:6 62:10 62:14,20 63:11,13 64:1,3,7,11 65:4 65:21 67:2,11,18 69:16 70:9,14 73:6
Zoom 9:15

0

0 16:13
02210-2001 3:11

1

1 14:21 16:14 21:3 30:20 31:1 75:13
1:16 91:10
1:24 91:11
1:25 2:6 91:14
10 1:17 7:3 34:20 40:22 94:3
1001 6:3 15:16,19 16:1 87:7
10016 3:5
1002 6:5 11:1,10
1005 6:7 28:12,13 28:20
102 29:3 30:20 31:1 31:5 60:3,9 65:3 65:19 66:18 67:17 69:12,17 70:7 71:20 72:15,18
105 89:11 90:1
106 90:13 91:3
10th 92:17
11 6:5 90:13
11:08 48:9
11:22 48:10
110 81:17
111 81:17
113 80:6,9 82:10
114 82:12 84:10,20 86:19
116 85:14 86:1,6,21 87:11
12 89:11,12 90:5,11
12:26 80:2
12:53 80:3
12A 90:13 91:2
13 88:5 90:5
14 87:20 90:5

Foras Technologies Ltd.
Exhibit 2009 - Page 105

1400 4:4
15 88:9 89:9,12,22 90:12
16 6:3
17 86:13 87:11,15 87:17 88:18
17th 4:3
1875 2:11 3:16
19 28:20,22 30:13 30:15,18 31:14,19 31:21 32:8,13,16 32:18 33:11,15 49:13 59:21 60:2 60:21 62:11,20 63:12,22 65:2 66:15 69:11 70:7 71:19 72:15
19c 84:18

2

2 14:21 15:2 19:13 23:4 36:3 39:17 39:19 49:19 74:15 74:22 75:5
20 31:16,20 32:4,20 62:21 63:7
200 3:4
2003/0126498 6:9
20190-6023 3:17
2024 1:17 7:3 92:17 94:3
203-2750 3:18
204a 35:3,10,21 36:2,8
205a 36:9,18 37:9
21 62:21
212 3:6
22 62:21
24th 3:5
25 63:8,8
27 23:4 24:16 39:5
271 4:3
28 6:7

3

3 5:3 15:2 35:14,18 36:1,21 37:16 42:5 45:4 57:15 59:17,17,19 75:13
30 51:7 92:9
302a 35:10,21 36:12,22 37:14 38:15
302a-b 35:3 41:3 41:14
302b 35:10 36:12 37:15 38:15
30363-6209 4:4
304a 36:13 37:14
304a-b 41:17
304b 36:13 37:15
306 27:7 36:11 37:17 41:17 42:7 43:5,19 45:1 48:15
308 27:5 36:10 38:7 38:13,18 41:2 43:3
32 35:18,20,22 36:7
32-bit 50:4
33 27:4 29:17,19 30:1,9 34:16,19 38:10 40:21 43:2 43:17 44:20 46:4 47:16 49:22 50:5 52:2 53:10 54:4 56:18 59:16
34 50:10
35 44:3,4,13 46:9 47:8 49:3 50:18 51:7
36 71:2 84:10
37 71:7
3a 59:17

4

4 42:16 45:11,15
40 86:14 89:8,21
402 44:5
404 4:5 42:11,17 74:15 75:17 76:1 77:10 78:13
408 84:11
410 84:11
42 86:14 89:9
47 11:21 22:21 25:19
48 23:1 73:11
49 74:9
4a 42:9 46:20 48:4 49:3 75:3,6,8,18 76:1 82:18 84:11

5

5 19:14
50 8:7 74:7 75:2,16
55 8:7 86:14 90:10 90:20
56 78:2 81:19,22 82:3
57 78:2 81:20 82:1 82:3 86:15 90:10
571 3:18

6

6 86:13,14 89:8 90:9,22
617 3:11
62 81:6
63 80:7
64 82:13
64-bit 21:4
646-1626 3:11
653-6481 4:5
66 86:1

7

7 5:4,7
7,502,958 1:12 6:4

8

8 28:19 59:22 78:6 86:13 87:11,14 88:18
80 12:1 14:7 21:12
800 2:12 3:17
81 25:18 26:17 34:15 73:11,18
84 78:5
85 74:9,11,14
86 74:7

9

9 78:6 86:13 87:11 87:15,17,20 88:18 90:22
9:58 2:6 7:3
92 5:9
9433 1:22
951-0100 3:6
958 12:2 15:14 18:13 19:12 85:12 85:13,21 86:11,12 87:3,8,15 88:17 89:9
96 11:21 25:19 74:7 74:10 75:16 80:7 82:13 86:1