

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
U.S. Patent 8,350,294

PETITION FOR *INTER PARTES* REVIEW

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Ex. 1001	U.S. Patent No. 8,350,294 B2 (“the ’294 patent”)
Ex. 1002	Prosecution History of the ’294 Patent (“ <i>Prosecution History</i> ”)
Ex. 1003	Declaration of Dr. James Richard Shealy (“ <i>Shealy</i> ”)
Ex. 1004	Curriculum Vitae of Dr. James Richard Shealy
Ex. 1005	U.S. Patent Application Publication No. US 2007/0164315 A1 to Smith (“ <i>Smith</i> ”)
Ex. 1006	U.S. Patent Application Publication No. US 2008/0087915 A1 to Uemoto (“ <i>Uemoto</i> ”)
Ex. 1007	Japanese Patent Publication No. JP2006-253224 A to Kigami.
Ex. 1008	Certified English Translation of Japanese Patent Publication No. JP2006-253224 A (“ <i>Kigami</i> ”)
Ex. 1009	Translator’s Declaration for Certified English Translation of JP 2006-253224 A.
Ex. 1010	Umesh K. Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, vol. 90, no. 6 (June 2002), pp. 1022-1031 (“ <i>Mishra</i> ”).
Ex. 1011	Excerpts of Rüdiger Quay, <i>Gallium Nitride Electronics</i> , vol. 96, Springer Science & Business Media (2008) (“ <i>Quay</i> ”).
Ex. 1012	Excerpts of Stephen J. Pearton et al., <i>Gallium Nitride Processing for Electronics, Sensors and Spintronics</i> , Springer Science & Business Media (2006) (“ <i>Pearton</i> ”).
Ex. 1013	U.S. Patent Application Publication No. US 2004/0012015 A1 to Saxler (“ <i>Saxler015</i> ”)

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Ex. 1014	X. Hu et al., <i>Enhancement mode AlGaIn/GaN HFET with selectively grown pn junction gate</i> , Electronics Letters, vol. 36, no. 8 (2000), pp. 753-754 (“Hu”).
Ex. 1015	Excerpts of Chang Soo Suh, Enhancement-Mode GaN-Based HEMTs for High-Voltage Switching Applications (Dec. 2008) (Ph.D. dissertation, University of California, Santa Barbara) (“Suh”).
Ex. 1016	U.S. Patent Application Publication No. US 2005/0145874 A1 to Saxler (“Saxler874”)
Ex. 1017	Chris G. Van de Walle et al., “Hydrogen in III-V Nitrides,” <i>Semiconductors and Semimetals</i> , vol. 57 (1998), pp. 157-184 (“Van de Walle”).
Ex. 1018	Shuji Nakamura et al., <i>Hole Compensation Mechanism of P-Type GaN Films</i> ,” Japanese Journal of Applied Physics, vol. 31 (1992), pp. 1258-1266 (“Nakamura”).
Ex. 1019	Complainant’s Proposed Constructions & Respondents’ Proposed Constructions in related International Trade Commission investigation: <i>In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same</i> , Inv. No. 337-TA-1366, dated September 5, 2023 (“ITC Constructions”).
Ex. 1020	U.S. Patent No. 5,985,687 (“Bowers”)
Ex. 1021	U.S. Patent Application Publication No. 2002/0167023 A1 to Chavarkar (“Chavarkar”)
Ex. 1022	U.S. Patent Application Publication No. 2003/0102482 A1 to Saxler (“Saxler482”)

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Ex. 1023	Shuji Nakamura – Biographical, NobelPrize.org, Nobel Prize Outreach AB 2023, www.nobelprize.org/prizes/physics/2014/nakamura/biographical/ (last visited Aug. 28, 2023) (“ <i>Biographical Nakamura</i> ”)
Ex. 1024	Excerpts of Vasco Matias, Defect characterization of Europium implanted Gallium Nitride (2008) (Ph.D. dissertation, KU University, Belgium) (“ <i>Matias</i> ”).

I. PRELIMINARY STATEMENT

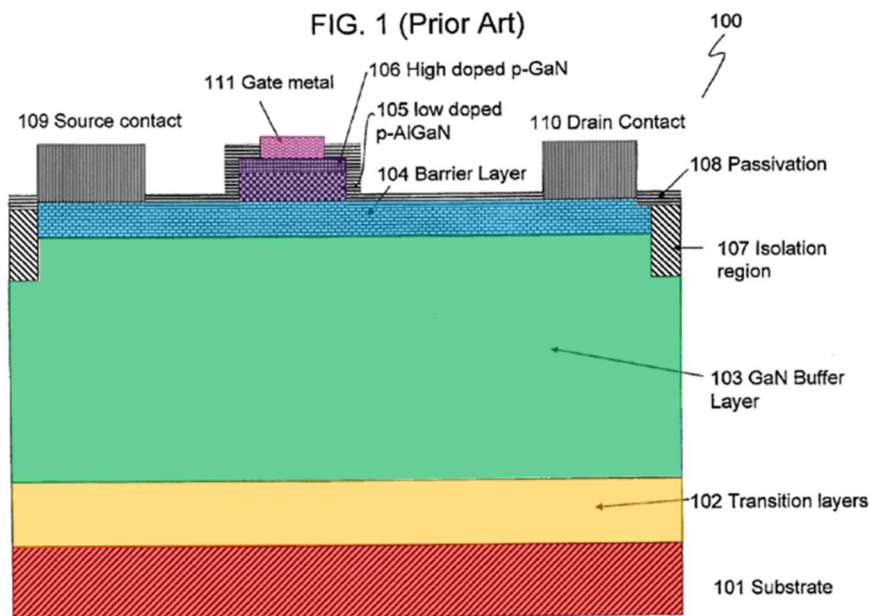
Petitioner requests *inter partes* review of U.S. Patent 8,350,294 and cancellation of claims 1-12.

The challenged claims are directed to III-nitride transistors. '294 patent, 5:12-6:27. III-nitride transistors are fabricated with semiconductors that combine a group III element (e.g., indium or gallium) with nitrogen. III-nitride transistors were admittedly known and “conventional.” *Id.*, 1:55-2:2, Fig. 1. The '294 patent purports to improve a single region—the “cap” underneath the gate of the well-known transistor structure. According to the '294 patent, incorporating a “compensated GaN layer or a semi-insulating GaN layer below the gate contact and above the barrier layer” resolved performance issues, such that either the “compensated” or “semi-insulating” layers reduced leakage. *Id.*, 1:14-17, 3:17-19, 3:63-67.

But forming “compensated” or “semi-insulating” cap layers was far from new. Others—like *Smith*, *Uemoto*, and *Kigami*—had already disclosed III-nitride transistors with “compensated” or “semi-insulating” layers below their gates. Because these references render claims 1-12 obvious, the Board should institute and cancel all challenged claims. *Shealy*, [06]-[07], [089], [0103].

II. THE '294 PATENT

The '294 patent relates to a “transistor with a compensated GaN layer or a semi-insulating GaN layer below the gate contact and above the barrier layer.” '294 patent, 1:14-17. It admits GaN transistors were “conventional” and known in the “Prior Art.” *Id.*, 1:55-2:2, Fig. 1. Figure 1 shows the “conventional enhancement mode GaN transistor,” formed with a **substrate**, **transition layers**, **buffer layer**, **barrier layer**, **p-type layers**, and contacts for **gate** and **source/drain**.¹ *Id.*



'294 patent, Fig. 1.

The '294 patent purports to address leakage issues in the conventional transistor. *Id.*, 2:3-9. It contends forming “compensated GaN” and/or “semi-

¹ All figures in this Petition containing color are annotated.

insulating” layers “below the gate contact” reduces leakage. *Id.*, 2:14-19. The ’294 patent describes the steps to form the conventional transistor layers. *Id.*, 3:22-42, Figs. 2-9. But then pinpoints its “invention” as the formation of the compensated or semi-insulating layer, emphasizing that “[t]he critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen.” *Id.*, 3:43-45. According to the ’294 patent, this “critical step” of passivation leads to “compensated semi-insulating material” below the gate. *Id.*, 3:43-52, 4:20-29.

The ’294 patent presents four transistor embodiments using the “compensated” or “semi-insulating” layers. The first embodiment, shown in Figure 2, has the same **substrate**, **transition**, **buffer**, **barrier**, and **gate** of the “conventional” transistor, but substitutes the **p-type layers** with a “[c]ompensated semiconductor layer 38 [that] preferably comprises AlGa_N or Ga_N with a deep level passivated p-type impurity.” *Id.*, 2:56-3:13:

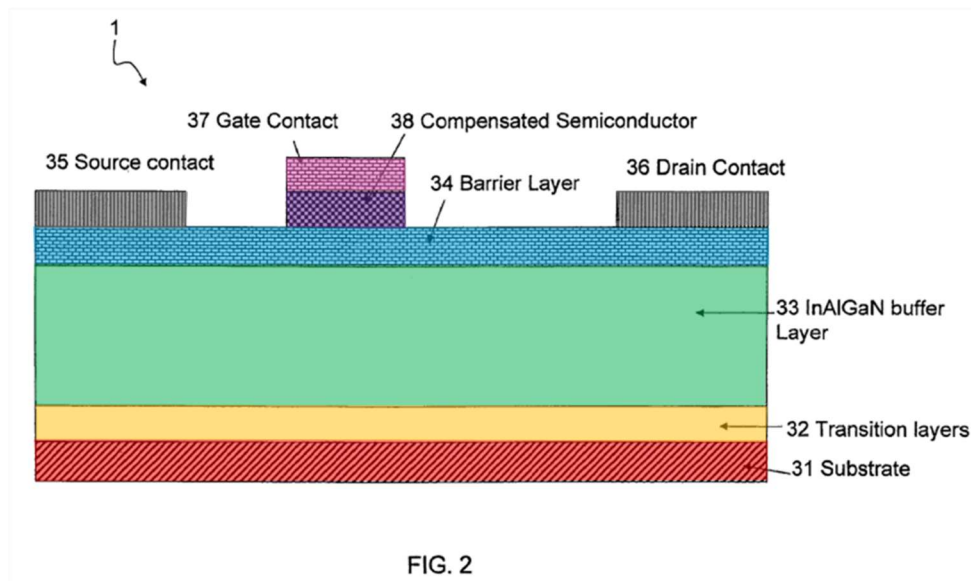


FIG. 2

'294 patent, Fig. 2.

The **only** difference from the admitted prior art is the purported use of a “compensated semiconductor” layer under the gate:²

² While Figure 2 labels the buffer layer as composed of “InAlGa_N,” this is just a preferred embodiment. Ex. 1001, Fig. 2. The '294 patent is clear the buffer layer is “made of a III Nitride material,” which “can be composed of In_xAl_yGa_{1-x-y}N where x+y≤1,”—including simply GaN. *Id.*, 3:12-15.

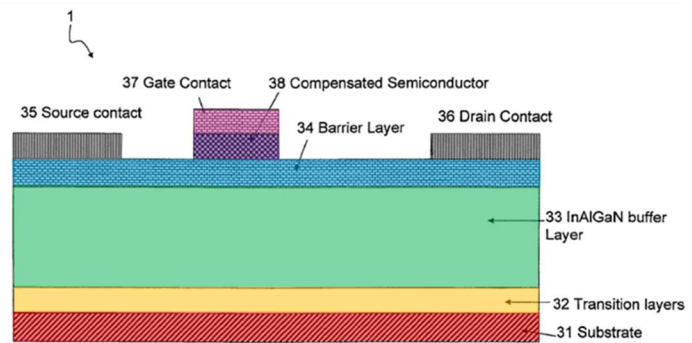
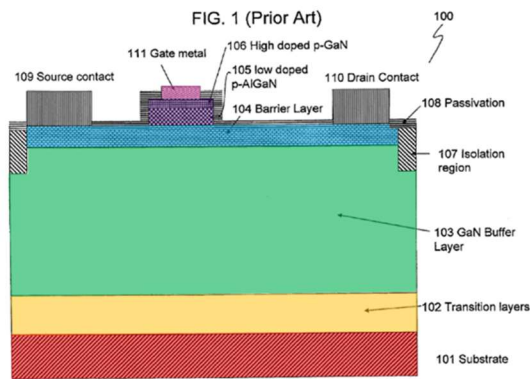


FIG. 2

'294 patent, Figs. 1, 2.

The second embodiment uses “a semi-insulating layer 39 in place of the compensated semiconductor layer 38,” where the “[s]emi-insulating layer 39 may comprise, for example, AlGaIn or GaN, with deep level impurity atoms;” further, the transistor could “have both a semi-insulating layer and a compensated semiconductor layer.” *Id.*, 3:54-61. The remaining embodiments add layers: “a confinement layer ... above the semi-insulating layer” (*id.*, 4:31-34), and “a spacer layer 49 beneath [the] semi-insulating layer” (*id.*, 4:64-66). All embodiments are related solely to variations of the layers between the gate and barrier layer. *Shealy*, [044]-[051].

III. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) with respect to the '294 patent would have possessed at least a four-year degree in electrical engineering, chemical engineering, physics, or material science, or a closely related field, and at

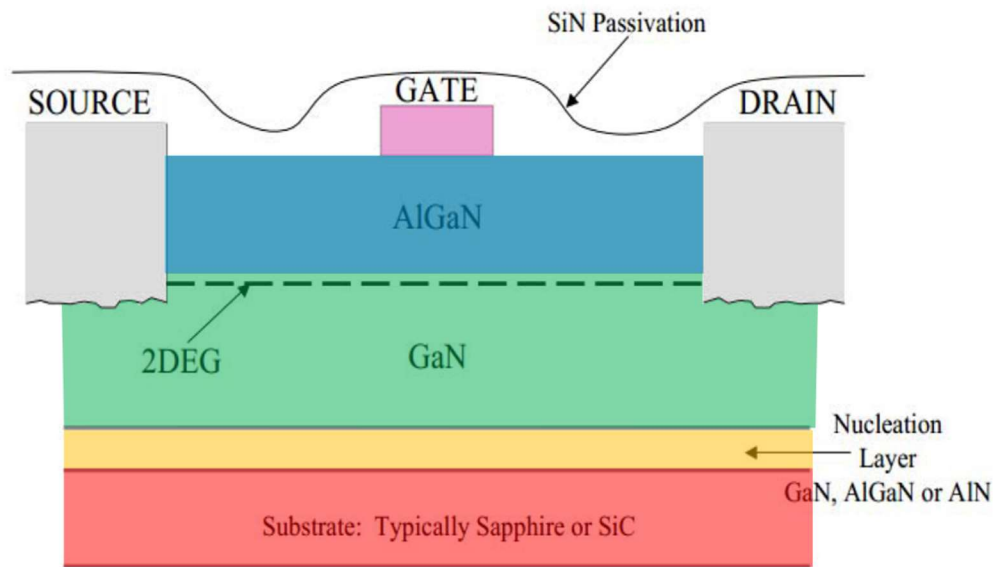
least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. *Shealy*, [052]-[054]. Additional education could substitute for professional experience and vice versa. *Id.*

IV. TECHNOLOGY BACKGROUND

A. III-Nitride Transistors

III-nitride transistor technology dates back to the mid-1990s—by 2009, it was over a decade old. *Shealy*, [055] (citing *Mishra*, Fig. 1; *Quay*, §2.5.5; *Pearson*, §6.2). A POSITA knew well the transistors’ structures, characteristics, operation, and fabrication. *Id.*

A POSITA would have known that the transistors could be fabricated by layering III-nitride materials with different band gaps. *Id.*, [056] (citing *Mishra*, §II). A POSITA was intimately familiar with the structure of the high-electron mobility transistor (HEMT)—a type of III-nitride transistor—and understood the structure consisting of nucleation, channel, barrier, and gate layers stacked on a substrate, as exemplified in the “Basic HEMT structure” below.



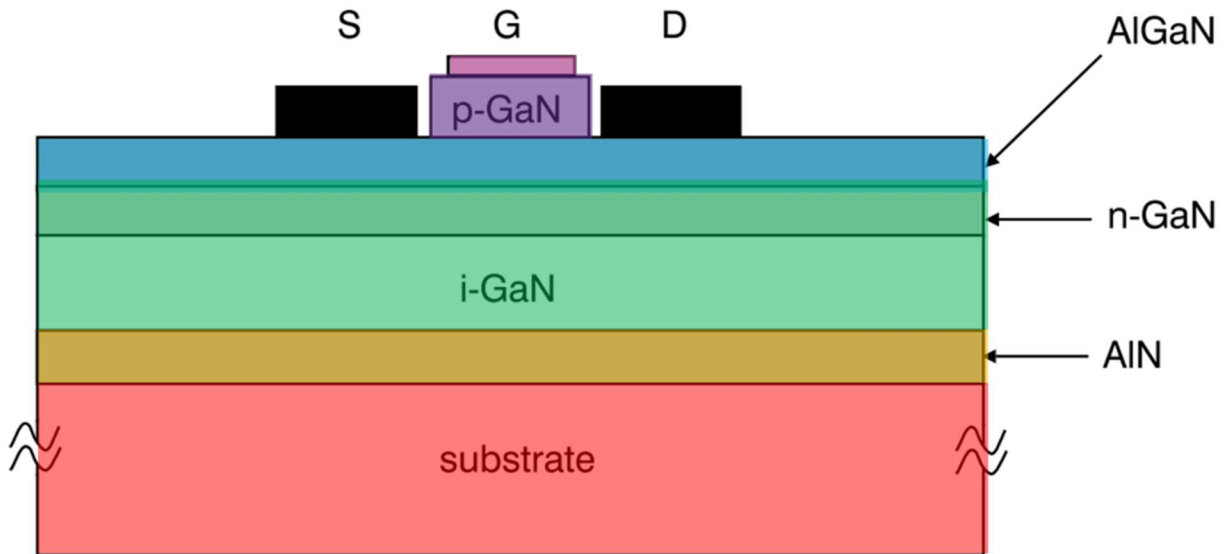
Mishra, Fig. 4.

A POSITA would have known about the transistor's operation and design considerations. *Shealy*, [057]. A POSITA would have known, for example, that transition or buffers between the different layers could be used to balance lattice and thermal mismatch between the substrate and the GaN layers. *Id.* (citing *Quay*, §3.1.1; *Pearton*, §1.2; *Saxler015*, Abstract, [0002]). A POSITA also would have known that aluminum in the barrier induced a two-dimensional electron gas (2DEG), forming a channel. *Id.*, (citing *Mishra*, Fig. 6; *Quay*, §2.2.3).

B. Cap Layers

In the early 2000s, the basic structure was updated to include a “**cap layer**” between the **barrier** and the **gate**. *Shealy*, [058] (citing *Hu*; *Suh*, §4.1; *Quay*, §3.4.2). Cap layers were added to, among other things, control the transistor's threshold

voltage and enable enhancement (i.e., normally off) operation. *Shealy*, [058] (citing *Suh*, §4.1). The **cap layer** is shown in the Figure below.



Hu, Fig. 1.

By 2009, the effect of cap layers had been thoroughly studied. *Shealy*, [059]. Many had experimented with different cap layers and investigated how cap layer thickness and/or composition impacted performance. *Id.* (citing *Quay*, §3.4.2; *Suh*, §4.4). A POSITA understood how cap layer characteristics (e.g., thickness or composition) could be used in a “design space,” and how different cap layer combinations tailored transistor’s performance. *Id.*, (citing *Suh*, §4.2; *Hu*, 1-2; *Smith*, [0008]-[0017]).

C. Acceptor Doping and Hydrogen Passivation

Doping of III-nitride materials had also been thoroughly studied by 2009. *Shealy*, [060]. A POSITA understood how doping defined optoelectronic

characteristics of nitride semiconductor layers. *Id.* (citing *Quay*, §2.2.5; *Pearton*, §1.2; *Saxler874*, [0004]). A POSITA would have known about the doping processes and elements. *Shealy*, [061] (citing *Quay*, §2.2.5, 3.3.1; *Saxler874*, [0006]). A POSITA understood, for example, that beryllium, magnesium, or carbon were all elements that could be used as acceptor dopants and used to form p-type III-nitride layers. *Id.*, (citing *Quay*, §§2.2.5, 3.3.1; *Smith*, [0014]; *Saxler874*, [0006], [0023]; *Pearton*, §1.4).

Among the various dopants, magnesium received special attention. *Shealy*, [062]. Magnesium was identified as a suitable acceptor dopant in the 1970s. *Id.* (citing *Pearton*, §1.3.1). By 2009, magnesium doping was well-understood. *Id.*, [062]. It was well-known, for example, that magnesium dopants tended to naturally interact with hydrogen during the epitaxial growth processes (e.g., during Metal-Organic Chemical Vapour Deposition, or MOCVD), and that even “as-grown” (i.e., materials without modifications) MOCVD materials included innate hydrogen concentration. *Id.*, (citing *Quay*, §3.3.1; *Pearton*, §§ 1.2, 1.3.1.3; *Van de Walle*, §I.1.c). A POSITA knew that hydrogen played an important role in magnesium passivation and that hydrogenation (incorporation of hydrogen) influenced the layer’s resistivity. *Id.* (citing *Quay*, §3.3.1; *Pearton*, §1.2; *Uemoto*, [0049]; *Kigami*, [0007]).

The hydrogenation process and its effects on resistivity were well-known in 2009. *Shealy*, [063]-[064]. Hydrogenation in doped GaN had been reported in the early 1990s by Nobel Prize winner Dr. Shuji Nakamura, who explained that hydrogenation “naturally occurs” in GaN materials.³ *Nakamura*, 1265. Dr. Nakamura explained that “as-grown GaN films are hydrogen passivated” and demonstrated how hydrogen passivation affected resistivity. *Id.*, 1266. By 2009, a POSITA was well versed on the mechanisms of hydrogen passivation and understood that, as Dr. Nakamura found, hydrogen would be “naturally” present in as-grown layers. *Shealy*,[064].

V. STATEMENT OF RELIEF REQUESTED

A. Prior Art

Exhibit	Prior Art
1005	<i>Smith</i> , U.S. Patent Publication No. 2007/0164315, published July 19, 2007; prior art under 35 U.S.C. § 102(b). ⁴

³ Indeed, Dr. Nakamura won the Nobel Prize in part for this work. *Biographical Nakamura*, 12 (“Shuji also clarified the mechanism of hole compensation ... Atomic hydrogen produced from the dissociation of ammonia gas forms Mg-H complexes. This formation prevents magnesium acceptors from behaving as acceptors.”).

⁴ Pre-AIA law applies.

Exhibit	Prior Art
1006	<i>Uemoto</i> , U.S. Patent Publication No. 2008/0087915, filed July 24, 2007, and published April 17, 2008; prior art under 35 U.S.C. § 102(a) and (e).
1007 (Translation 1008)	<i>Kigami</i> , Japanese Patent Publication No. JP2006-253224, published September 21, 2006; prior art under 35 U.S.C. § 102(b).

B. Challenges

Grounds	Challenged Claims	Basis	Prior Art
1A	1-12	§ 103	<i>Smith</i>
1B	1-12	§ 103	<i>Smith</i> and <i>Kigami</i>
1C	1-12	§ 103	<i>Smith</i> and <i>Uemoto</i>
2	1-12	§ 103	<i>Uemoto</i> and <i>Smith</i>

Shealy, [0102]-[0103].

VI. STATEMENT OF FACTS

Pursuant to 37 C.F.R. § 42.22(c), Petitioner submits the following statement of facts that set forth the state of III-nitride transistor technology at the time of the '294 patent claimed priority date:

1. P-type dopants are acceptor impurities.
2. Before April 8, 2009, the following were known:
 - a. III-nitride transistors.

- b. Using a substrate in a III-nitride transistor.
- c. Using III-nitride transition layers above a substrate.
- d. Using a III-nitride buffer layer above transition layers.
- e. Using a III-nitride barrier layer above a buffer layer.
- f. Using a doped GaN layer above the barrier layer.
- g. Using a gate contact above a doped GaN layer.
- h. Using source and drain contacts in a III-nitride transistor.
- i. Creating p-type doped GaN using Mg, Zn, Be, or Ca as dopant.
- j. Creating doped and semi-insulating GaN using C, Fe, Mn, Cr, or V as deep-level dopants.
- k. Hydrogen passivates acceptor dopants in GaN layers.
- l. As-grown acceptor doped GaN layers include hydrogen.

VII. CLAIM CONSTRUCTION

In a related matter, Patent Owner and Petitioner have agreed that the term “compensated GaN layer” in claim 1 should be construed as follows:

Petitioner's	Patent Owner's
“Doped GaN layer formed with a step to passivate its impurities” which is a “product-by-process” limitation	“A semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor).”

ITC Constructions, 1, 9. The challenged claims are unpatentable under both constructions. *Shealy*, [065]-[071], [087]-[088]. But should the Board construe the term, Petitioner's is correct.

“In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006). Here, the claim language, the written description, and the prosecution history all support Petitioner's construction. *Shealy*, [072].

The claim language itself supports the Petitioner’s construction because while the claim uses “compensated” as an adjective, that adjective derives from a past-tense verb. The past-tense form of “compensated” suggests that the step of compensating had occurred. *Donghee Am., Inc. v. Plastic Omnium Advanced Innovation & Rsch.*, 812 F. App’x 988, 991 (Fed. Cir. 2020) (nonprecedential) (affirming PTAB finding that claim term “stake-fasten” described “an accessory that has already been fastened”); *Modavox, Inc. v. Tacoda, Inc.*, 607 F. Supp. 2d 530, 534-35 (S.D.N.Y. 2009) (finding the past tense of “embedded” suggests the act of embedding had occurred); *Shealy*, [073].

The written description agrees, emphasizing the “critical step” of “passivation of a p-type impurity using hydrogen” is the purported improvement distinguishing from the prior art. ’294 patent, 3:43-45. This “critical step” of passivation leads to a “highly compensated” material. *Id.*, 3:43-49. The ’294 patent also describes the “compensated” layer as a layer “with a deep level passivated p-type impurity” and discloses the passivation “can be performed by exposing the device to ammonia or hydrogen.” *Id.*, 3:10-39. The ’294 patent, thus, defines that a layer is “compensated” when it is formed with the “critical step” to passivate its impurities. *Shealy*, [074].

The Applicant also advanced this meaning during prosecution. The Examiner initially rejected the “compensated GaN layer” limitation as obvious over *Bowers*, because *Bowers* disclosed that it was “known that hydrogen passivates [or

compensates] the p-type dopants in Mg doped GaN.” *Prosecution History*, 87-89; *Bowers*, 8:31-35. In response the Applicant argued that, while *Bowers* disclosed knowledge about hydrogen passivation, it failed to disclose “**forming** a ‘compensated GaN layer.’” *Prosecution History*, 106 (emphasis added). The Applicant’s remarks clarify that the claimed “compensated GaN layer” requires “*forming*” the compensated layer, not mere presence of hydrogen in as-grown layers. *Shealy*, [075].

Moreover, extrinsic evidence supports Petitioner’s construction. *Shealy*, [076]. Hydrogenation in as-grown III-nitride materials had been well-known for over a decade by 2009. *Supra* §IV.C. *Shealy*,[060]-[064]. Thus, “compensated,” defined in the ’294 patent as the “critical step” (and often *only* step) distinguishing from the prior art, cannot be interpreted as mere hydrogen presence in as-grown material, a well-known property of doped GaN. *Hubbell v. United States*, 179 U.S. 77, 80 (1900) (“[I]t is well settled that the claim as allowed must be read and interpreted with reference to the rejected claim and to the prior state of the art, and cannot be so construed as to cover either what was rejected by the Patent Office or disclosed by prior devices.”).

However, “compensated GaN layer” *also* recites product-by-process steps in a device claim, which lend no patentable weight. “The patentability of a product does not depend on its method of production. If the product in a product-by-process

claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” *In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985); *Kamstrup A/S v. Axioma Metering UAB*, 43 F.4th 1374, 1381-83 (Fed. Cir. 2022) (finding “cast in one piece” in claim to flow meter, a product-by-process element that gives no patentable weight); *United Therapeutics Corp. v. Liquidia Techs., Inc.*, 74 F.4th 1360, 1373 (Fed. Cir. 2023) (“As these claims are product claims, they are anticipated by a disclosure of the same product irrespective of the processes by which they are made.”). Thus, under Petitioner’s construction, the prior art only need show a material with passivated impurities to show unpatentability, not the step to achieve it.

Patent Owner’s proposed construction should be rejected. Patent Owner’s construction is divorced from the specification and introduces ambiguities. Patent Owner’s proposed construction would also render the claim ambiguous and indefinite because it introduces undefined relative terms that are never used or defined in the specification or the prosecution history. *Shealy*, [077]. Particularly, Patent Owner’s proposed construction introduces “imperfection,” “partially cancels,” and “electrical effects” in the claim; terms that are not used in the claims or disclosed in the specification, and these undefined terms introduce ambiguities. *Id.*, [078]-[081]. Patent Owner’s proposed construction cannot apply because it is so vague that it permits an interpretation to cover **any** GaN material, even the materials

the '294 patent admitted as prior art and that the Applicant specifically distinguished from during prosecution. *Id.*, [082]-[086]; '294 patent, 3:43-45; *Matias*, §3.1 (“in a real crystal, the structure is always disturbed by some irregularities. Crystalline imperfections, or defects, will always be present”).

VIII. GROUNDS 1A-1C: *SMITH*, EITHER ALONE (1A), IN VIEW OF *KIGAMI* (1B), OR IN VIEW OF *UEMOTO* (1C)

A. Overview of Asserted Prior Art

1. *Smith*

Like the '294 patent, *Smith* discloses transistors formed with III-nitride materials—specifically GaN-based. *Smith*, [0002], [0008]; *Shealy*, [090]-[091]. *Smith* discloses several III-nitride transistor embodiments including the well-known layers, fabricated with the well-known technique of stacking semiconductor layers on a substrate. *Smith*, [0069]-[0077], Figs. 1A-9; *Shealy*, [092]. As shown in Figures 1A-9, *Smith* discloses the use of different cap layers and gate contacts to adjust the transistor's electrical characteristics. *Smith*, [0068]-[0069]; *Shealy*, [092]. One of *Smith*'s transistors is shown below.

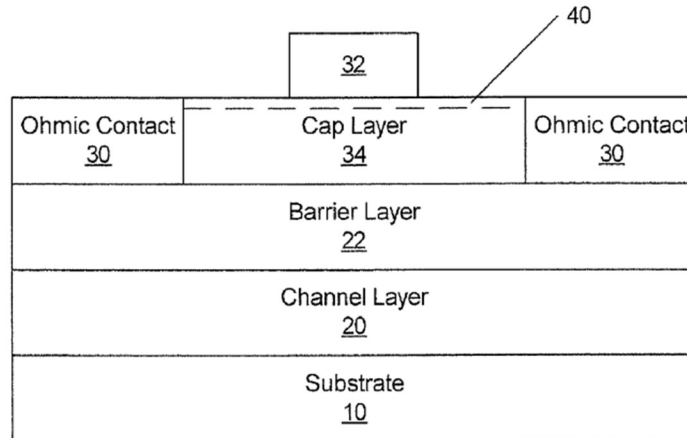


Figure 2A

Smith, Fig. 2A.

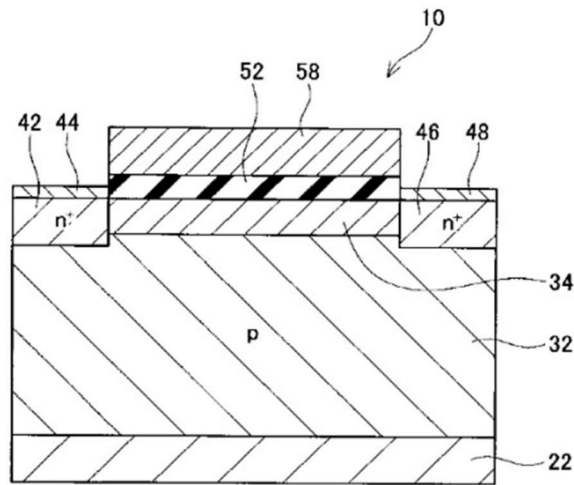
Smith discloses transistors with cap layers of different composition, thickness, and doping, explaining that cap layers can be selected to adjust transistor variables like leakage current, threshold voltage, and frequency performance. *Id.*, [0077]-[0097], *Shealy*, [093]. *Smith* discloses further adjustments to the transistor characteristics using multilayers and protective layers in the cap region. *Id.*, [0092], [0100], [0108], Figs. 3A-8. *Smith* discloses multiple structures and fabrication methods for III-nitride transistors, describing how different features (in particular cap layers) adjust electrical characteristics. *Shealy*, [094].

2. *Kigami*

Kigami, like the '294 patent, discloses III-V semiconductor devices, particularly normally-off GaN transistors. *Kigami*, [0001]-[0005]; *Shealy*,

[099]-[0100]. In *Kigami*, a doped GaN layer is formed on a substrate. *Kigami*, [0024], Fig. 2. *Kigami* discloses forming the transistor with a MIS (Metal-Insulator-Semiconductor) structure. *Id.*, [0024], Fig. 4. *Kigami*'s transistor is shown in Figure 1.

FIG. 1



Kigami, Fig. 1.

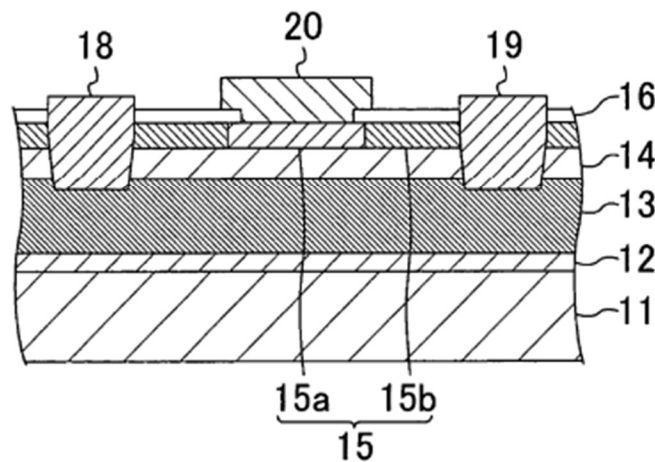
Kigami discloses that GaN transistors can be improved by hydrogenating (introducing hydrogen) the GaN layer to locally passivate impurities. *Id.*, [0007], [0022]; *Shealy*, [0101]. *Kigami* discloses that hydrogen can be introduced by exposing the transistor to an ionized gas. *Id.*, [0026], Fig. 5. *Kigami* discloses that introduced hydrogen atoms form a composite with magnesium, inactivating the impurities and making the layer more resistive. *Id.*, [0026]. *Kigami* explains the hydrogenation improves performance by reducing and stabilizing threshold voltage

while keeping a high withstand (or breakdown) voltage. *Id.*, [0006], [0023], [0029]; *Shealy*, [0101].

3. *Uemoto*

Uemoto, like the '294 patent, discloses III-nitride transistors formed by stacking nitride layers on a substrate. *Uemoto*, [0031]-[0035]; *Shealy*, [095]-[096]. In Figure 1, *Uemoto* illustrates one of its embodiments, showing semiconductor nitride layers (13, 14, 15) stacked on a substrate (11) with an intervening buffer layer (12).

FIG. 1



Uemoto, Fig. 1.

Uemoto discloses that, as shown in Figure 1, the nitride layer 15 has two regions: a control region 15a (with active impurities) and a resistive region 15b (where hydrogen inactivates or passivates impurities). *Uemoto*, [0015], [0033]; *Shealy*, [097]. *Uemoto* discloses that the formation of the highly resistive region 15b

is beneficial because it reduces gate-drain leakage and improves temperature stability. *Id.*, [0059], [0063], Fig. 8.

Uemoto discloses different methods to form the highly resistive region 15b. *Shealy*, [098]. One method uses a “hydrogen diffusion barrier film 16” that prevents hydrogen desorption from layer 15. *Uemoto*, [0047]-[0048]. Another method uses a “hydrogen diffusion film 17” that promotes hydrogen diffusion into layer 15. *Id.*, [0063]. *Uemoto* teaches to selectively diffuse hydrogen in regions of layer 15 by forming one of the diffusion films and performing a thermal treatment. *Id.*, [0050], [0063], Fig. 8. *Uemoto* explains how the diffused hydrogen passivates impurities, resulting in higher (and more stable) resistivity. *Id.*, [0049], [0063], [0064]; *Shealy*, [098].

B. Overview of the *Smith* Grounds (1A-1C).

1. Ground 1A

Smith discloses all the “conventional” layers the ’294 patent admits as prior art (e.g., **substrate**, **transition**, **buffer**, **barrier**, and **gate**). *Smith*, [0068], Fig. 1A; *Shealy*, [0104]-[0105]. *Smith* also discloses transistors with **cap layers**, and describes how to select or combine different **cap layers** to adjust the transistor’s characteristics. *Smith*, Figs. 1A-9, [0068]. *Smith* also discloses the allegedly inventive elements, including the “semi-insulating,” “confinement,” and “spacer”

layers—and *Smith* discloses “a compensated GaN layer,” regardless of how the term is construed. *Shealy*, [0105]; *Smith*, [0087], [0090], [0120].

Petitioner’s Construction

Under Petitioner’s construction the “compensated GaN layer” limitation means “doped GaN layer formed with a step to passivate its impurities” and should be interpreted as product-by-process. *ITC Constructions*, 9. The limitation is, thus, anticipated by any prior art that discloses the resulting structure. *United Therapeutics*, 74 F.4th at 1373. So prior art disclosing a GaN layer with passivated impurities, regardless of the passivation method, meets the “compensated GaN layer” limitation. *In re Thorpe*, 777 F.2d at 697. And *Smith* discloses this. *Shealy*, [0106]-[0108].

Smith discloses its cap layers being formed with different materials, dopants, and thicknesses. *Smith*, [0085]-[0089]. Additionally, it was well-known that “as-grown GaN films are hydrogen passivated.” *Nakamura*, 1266; *supra* §IV.C; *Shealy*, [0109]. A POSITA would have recognized that *Smith*’s doped cap layer is a GaN layer with passivated impurities.

But even if the “compensated GaN layer” limitation of claim 1 is not interpreted as product-by-process, *Smith* would still render the limitation obvious. While *Smith* does not explicitly disclose a “doped GaN layer formed with a step to passivate its impurities,” *Smith*’s disclosure makes such layer obvious. *Shealy*,

[0110]. *Smith* discloses that cap layers can be doped with acceptors and that the level of doping should be adjusted, specifying that “[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths.” *Smith*, [0014], [0085], [0087]. A POSITA would have understood that *Smith*’s “level of doping” was related to the level of active (non-passivated) impurities. *Shealy*, [0110]. A POSITA also knew that well-known processing steps, like hydrogenation, would passivate dopants, affecting the doping level. *Id.*; *supra* §IV.C. Because it was well-known that passivation affected the level of doping, and *Smith* identifies the level of doping as a variable altering the device characteristics, a POSITA would have been motivated to control the doping of cap layers with a hydrogenation processes as a result-effective variable. *Shealy*, [0111]. Even if the limitation of “compensated GaN layer” is interpreted to require the process, *Smith* itself still renders the limitation obvious because a POSITA would have known that the result effective variable of level of doping could be controlled with hydrogenation.

Patent Owner’s Construction

If “compensated GaN layer” is construed as proposed by the Patent Owner (as “A semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other

type of dopant, impurity, or imperfection (for example, acceptor)’’), *Smith* also discloses it, for similar reasons. *Shealy*, [0112].

By 2009 it was well established that ‘‘hydrogen passivation occurs in as-grown GaN films.’’ *Nakamura*, 1265; *supra* §IV.C. If ‘‘compensated GaN layer’’ is interpreted with Patent Owner’s proposal, a POSITA would have recognized that *Smith*’s cap layer was a ‘‘compensated GaN layer.’’ *Shealy*, [0113]-[0115]. A POSITA would have recognized *Smith* discloses that its cap layer is ‘‘GaN gate material,’’ including ‘‘one type of dopant, impurity, or imperfection’’ (the innate or naturally occurring hydrogen) that ‘‘partially cancels the electrical effects of the other type of dopant, impurity, or imperfection’’ (the magnesium). *Id.*; *Smith*, [0085], *supra* §IV.C.

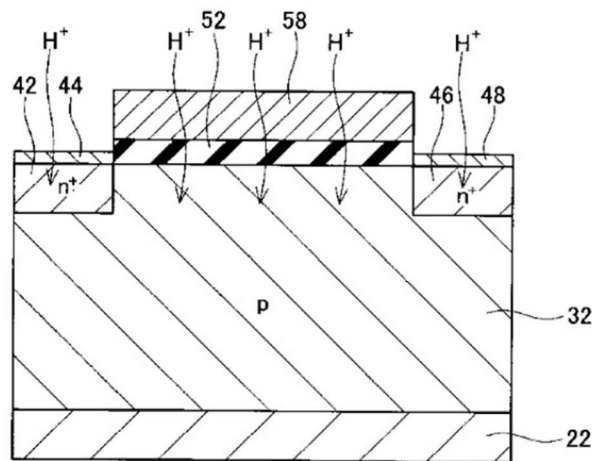
2. Grounds 1B and 1C

Looking beyond a POSITA’s knowledge, incorporating the ‘‘compensated GaN layer’’ in *Smith*’s device would have also been obvious. Each of *Kigami* (Ground 1B) and *Uemoto* (Ground 1C) discloses the ‘‘compensated GaN layer’’ under both proposed constructions; *Shealy*, [0116].

Ground 1B: A POSITA would have applied *Kigami*’s method of passivating impurities to improve *Smith*’s transistor. *Shealy*, [0117]. *Kigami* discloses that introducing hydrogen in the GaN layer opposing the gate improves performance. *Kigami*, [0007], [0022]. Specifically, *Kigami* discloses that passivating the GaN

layer with a hydrogenation step, shown below in Figure 5, improves the transistor's performance by reducing and stabilizing the threshold voltage I_d , [0006], [0023], [0026], [0029]; *Shealy*, [0118]-[0119].

FIG. 5



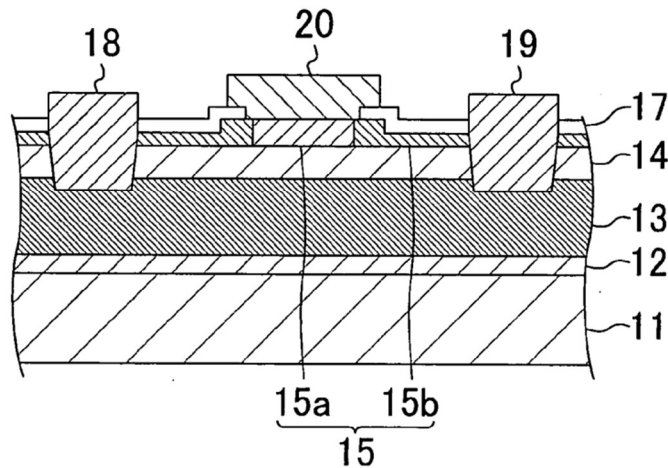
Kigami, Fig. 5.

Using *Kigami*'s hydrogenation process in *Smith* would “compensate” *Smith*'s cap layer resulting in the “compensated GaN layer above the barrier” under both parties' constructions.

Ground 1C: A POSITA would have employed *Uemoto*'s method of passivating impurities with a hydrogen diffusion layer to *Smith* seeking to, for example, reduce leakage current. *Shealy*, [0120]. *Uemoto* teaches forming a resistive region 15b through a hydrogen diffusion step. *Uemoto*, [0063], Fig. 7; *supra* §VIII.A.3. *Uemoto* also discloses that forming the high resistive region improves

transistor performance, reducing leakage. *Uemoto*, [0071]. *Uemoto*'s Figure 7 shows region 15b being formed beneath gate electrode 20.

FIG. 7



Uemoto, Fig. 7.

Using *Uemoto*'s hydrogen diffusion in *Smith* would “compensate” *Smith*'s cap layer resulting in the “compensated GaN layer above the barrier” under both parties' constructions. *Shealy*, [0121]-[0122].

C. Obviousness Rationales

1. (GROUND 1A) Motivation to adjust the level of doping in *Smith*'s cap layer using hydrogen passivation

A POSITA would have been motivated to adjust *Smith*'s doping by using hydrogen passivation because *Smith* recognizes level of doping as a result-effective variable controlling transistor characteristics, and a POSITA would have known that hydrogen passivation adjusted the doping level. *Shealy*, [0123]-[0127].

Smith discloses that the level of doping in cap layers is a result-effective variable to control leakage, explaining that “[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths.” *Smith*, [0087]; *E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1006 (Fed. Cir. 2018) (“[R]ecognition in the prior art that a property is affected by the variable is sufficient to find the variable result-effective.”). By 2009, a POSITA was intimately familiar with acceptor doping and hydrogen passivation. *Supra* §IV.C. A POSITA would have known that incorporating hydrogen in GaN layers would passivate acceptor dopants affecting the level of doping. *Id.*; *Shealy*, [0124]-[0125].

Because a POSITA would have known that hydrogenation can affect the “level of doping” in GaN layers and *Smith* identifies the level of doping as a result effective variable, a POSITA would have been motivated to adjust doping in cap layers to control leakage. *Shealy*, [0126]-[0127]. To a POSITA, it would have been obvious to adjust the level of doping as a result-effective variable to, as disclosed by *Smith*, improve leakage. *Id.*; *E.I. DuPont*, 904 F.3d at 1011 (“[M]otivation was sufficient for a skilled artisan to adjust result-effective parameters.”).

2. (GROUND 1B) Motivation to incorporate *Kigami's* hydrogenation in *Smith*

A POSITA would have been motivated to apply *Kigami's* hydrogenation processing step(s) to passivate impurities in *Smith's* cap layers. *Shealy*, [0128]-[0133]. A POSITA would have been motivated to use *Kigami's* hydrogen incorporation techniques to form a region with passivated impurities in *Smith's* cap layer. *Id.* To a POSITA it would have been obvious to employ *Kigami's* ionized gas hydrogenation (*Kigami*, [0026]) to passivate impurities in *Smith's* doped cap layer (*Smith*, [0085]). *Shealy*, [0128]. Multiple rationales support the combination shown below (modifying *Smith's* Figure 2A based on *Kigami's* Figure 5):

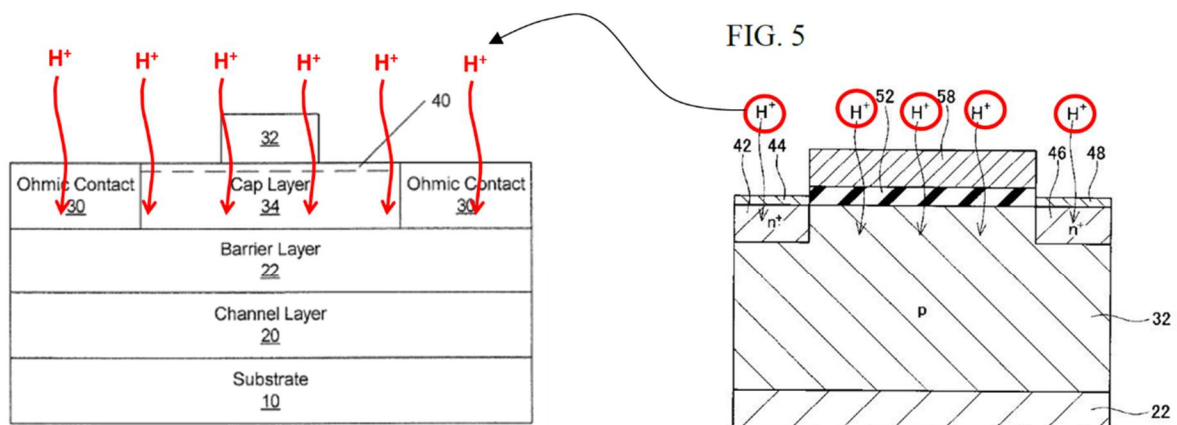


Figure 2A

Smith, Fig. 2A; *Kigami*, Fig. 5 (showing their combination).

First, *Smith* and *Kigami* are directed to the same field and techniques. Both relate to nitride-based transistors. *Smith*, Abstract; *Kigami*, Abstract. Both

specifically describe techniques for fabricating HEMTs. *Smith*, [0031]; *Kigami*, [0010]. Both describe structures and techniques that seek to improve HEMTs' robustness and operation. *Smith*, [0064]; *Kigami*, [0010]; *Shealy*, [0129]-[0130]. *Smith* and *Kigami* are, thus, analogous art and a POSITA would have considered their teachings relevant and combinable. *Shealy*, [0130].

Second, *Kigami* suggests and motivates the combination. *Kigami* teaches that introducing hydrogen into GaN transistor layers, like those of *Smith*, improves performance. *Shealy*, [0131]; *Kigami*, [0007]. *Kigami* states that "utilizing the phenomenon in which the p-type impurity is inactivated by hydrogen atoms" permits "having a low threshold voltage and a high withstand voltage." *Kigami*, [0007]. *Kigami* further touts the benefits of using its intentional hydrogen passivation, explaining it has "effects of stabilized threshold voltage, increased switching speed, and the like." *Id.*, [0029]. A POSITA would have considered these effects advantageous to *Smith*'s device because *Smith* was also concerned with improving the transistor's operation. *Smith*, [0003]-[0007] (seeking to use transistors for "high frequency applications"), [0081] (seeking to adjust characteristics "such as threshold voltage, frequency performance, etc."), [0089] (controlling the level of doping to reduce leakage current) ; *Shealy*, [0131]. Indeed, *Kigami* directly suggests applying its techniques to transistors that, like *Smith*'s, use magnesium dopants stating that its

“invention is particularly useful in situations in which magnesium is used as a p-type impurity.” *Kigami*, [0012].

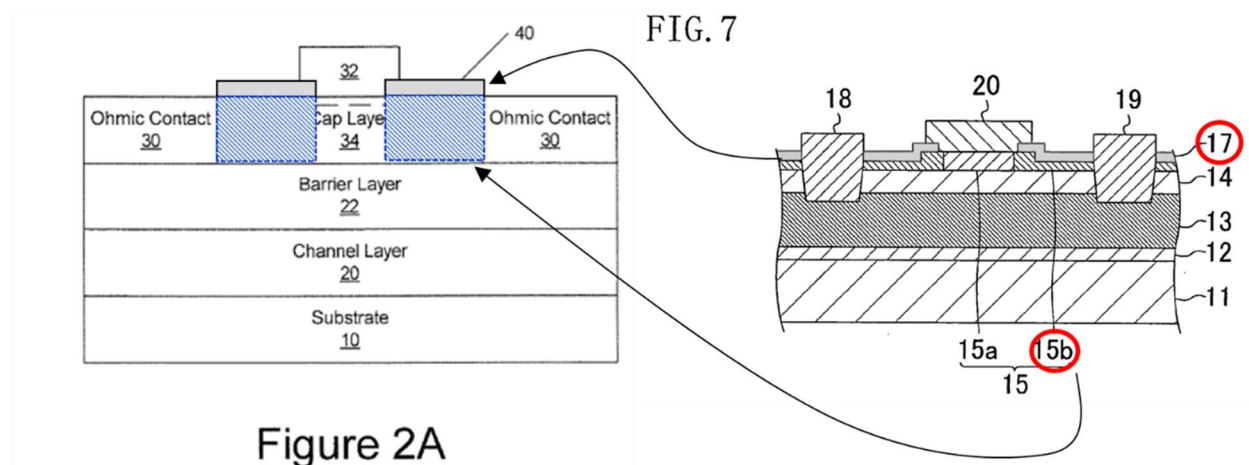
Third, the combination of *Kigami* and *Smith* would also be the use of a known technique to improve similar devices. *Kigami*’s discloses a known technique, the hydrogen incorporation to inactivate impurities. *Id.* *Kigami* explains that incorporating hydrogen reduces the transistor’s threshold voltage, maintains a high withstand voltage, and increases switching speed. *Id.*, [0007]-[0008], [0029]; *Shealy*, [0101], [0132]. A POSITA would have been motivated to use *Kigami*’s technique to improve *Smith*’s transistor in the same way because *Smith* also sought to control the transistor’s threshold voltage, having high breakdown strength, operating at high frequencies, and controlling the level of doping. *Smith*, [0003]-[0007], [0081]-[0087]; *Shealy*, [0132]. A POSITA, thus, would have understood *Smith*’s transistor as a base device that would be improved with *Kigami*’s hydrogenation technique. *Shealy*, [0132]. Because *Smith*’s and *Kigami*’s devices are comparable, a POSITA would have applied *Kigami*’s technique to *Smith* in the same way.

Fourth, a POSITA would have expected success implementing *Kigami*’s suggested incorporation of hydrogen in *Smith*’s transistor. *Shealy*, [0133]. By the earliest ’294 priority date, it was well-known that hydrogen passivated impurities in GaN layers and affected the layer’s conductivity. *Prosecution History*, 87; *supra* §IV.C. *Kigami* provides experimental data showing the effect of introducing

hydrogen atoms in transistor performance. *Kigami*, [0028], Fig. 6. *Kigami* explains mechanisms for hydrogen diffusion and impurity passivation, detailing how the hydrogen diffusion would be performed. *Id.*, [0022]-[0026], Fig. 5.

3. (GROUND 1C) Motivation to modify *Smith* by diffusing hydrogen in AlGaN layers, as taught by *Uemoto*

A POSITA would also have been motivated to apply *Uemoto*'s hydrogen diffusion technique to selectively increase the resistivity of *Smith*'s cap layers. *Shealy*, [0134]-[0140]. A POSITA would have been motivated to use *Uemoto*'s "hydrogen diffusion film 17" in *Smith* to form the "high resistive region 15b," which *Uemoto* teaches reduce leakage, to similarly inactive impurities in *Smith*'s cap layer, generate the highly resistive regions, and reduce leakage. *Id.*, [0134]-[0135]; *Uemoto*, [0059], [0063]. Multiple rationales support the combination shown below (modifying *Smith*'s Figure 2A based on *Uemoto*'s Figure 7):



Smith, Fig. 2A; *Uemoto*, Fig. 7 (showing their combination).

First, *Smith* and *Uemoto* are directed to the same field and the same techniques. Both relate to III-nitride transistors. *Shealy*, [0137]; *Smith*, Abstract; *Uemoto*, [0003]. Both describe techniques for fabricating transistors with gallium nitride. *Smith*, [0031]; *Uemoto*, [0005]. And both describe structures and techniques that seek to improve transistor operation by, for example, reducing leakage currents. *Smith*, [0064], [0087]-[0089]; *Uemoto*, [0059]. *Smith* and *Uemoto* are thus analogous art to the '294 patent, and a POSITA would have considered their teachings relevant and combinable. *Shealy*, [0137].

Second, *Uemoto* suggests and motivates the modification. *Id.*, [0138]. *Uemoto* suggests using a hydrogen diffusion film to selectively inactivate impurities in a GaN layer, explaining that inactivating impurities increases resistivity and reduces leakage. *Uemoto*, [0059], [0063]; *Shealy*, [0138]. *Uemoto* teaches that the diffusion film releases hydrogen during a thermal treatment, selectively inactivating impurities and enhancing resistivity. *Uemoto*, [0063]-[0068], Fig. 8. *Uemoto* also teaches that with its hydrogen diffusion technique, “a greater amount of leakage current between the gate and the drain can be reduced.” *Id.*, [0059]. *Smith* was also concerned with fabrication methods that reduce transistor leakage. *Smith*, [0087], [0089] (describing level of doping considerations “to reduce leakage currents”). Indeed, *Uemoto* directly suggests applying its techniques to fabrication of nitride semiconductor transistors—like *Smith*’s—stating that his invention “is useful for a

nitride semiconductor transistor such as a power transistor with a high breakdown voltage.” *Uemoto*, [0079].

Third, the combination of *Uemoto* and *Smith* would have been the application of a known technique to improve similar devices. A POSITA would have recognized that *Uemoto*’s method to selectively increase resistivity would improve *Smith*. *Shealy*, [0139]. *Uemoto* discloses that its hydrogen diffusion technique reduces leakage current. *Uemoto*, [0071]. A POSITA would have been motivated to use *Uemoto*’s technique to improve *Smith*’s transistor in the same way. *Smith* was also concerned with reducing the leakage current in its transistors and used the same materials, dopants, and structures as *Uemoto*. *Smith*, [0064], Fig. 2A; *Uemoto*, [0054], Fig. 7. Because *Smith* and *Uemoto*’s devices are similar, a POSITA would have been motivated to take *Smith*’s transistor as a base device and improve it with *Uemoto*’s teachings. *Shealy*, [0139].

Fourth, a POSITA would have expected success incorporating *Uemoto*’s hydrogen diffusion film into *Smith*. *Shealy*, [0140]. The mechanisms and effects of hydrogen incorporation into doped GaN layers had been well-established by 2009. *Prosecution History*, 87; *supra* §IV.C. *Uemoto* provides both experimental data and theoretical analyses that support the use of a hydrogen diffusion film to selectively increase resistivity and improve transistor characteristics. *Uemoto*, [0038], [0049], Figs. 4-8; *Shealy*, [0140].

D. Claim 1

1. [1p] A column III Nitride transistor comprising:

Smith discloses [1p]. *Shealy*, [0141]-[0142]. *Smith* specifies its invention relates to “transistors that incorporate nitride-based active layers” and discloses a “Group III-nitride high electron mobility transistor (HEMT).” *Smith*, [0002], [0008]. *Smith* also explains its invention can be used for “nitride-based devices such as Group III-nitride based HEMTs.” *Id.*, [0060]. In the figures, such as Figure 2A, *Smith* illustrates cross-sectional schematics of the transistors.

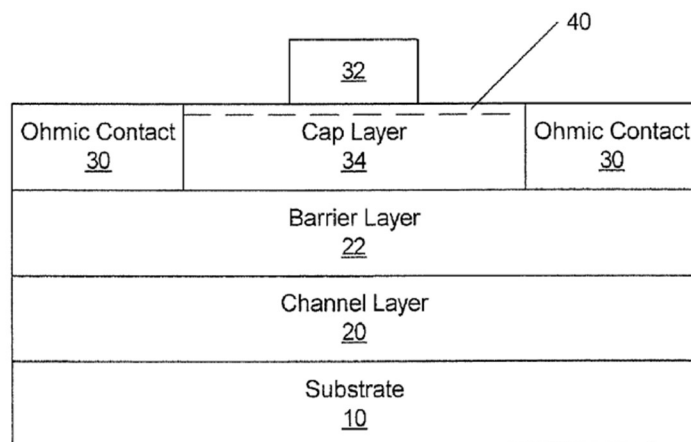


Figure 2A

Smith, Fig. 2A.

2. [1a] a substrate,

Smith discloses [1a]. *Shealy*, [0143]. Specifically, *Smith* discloses a “substrate 10 ... on which nitride based devices may be formed.” *Smith*, [0069]. Like

the '294 patent, *Smith* discloses the substrate can be formed with silicon carbide. *Id.*; '294 patent, 2:57-59. Figure 2A shows *Smith*'s **substrate 10**.

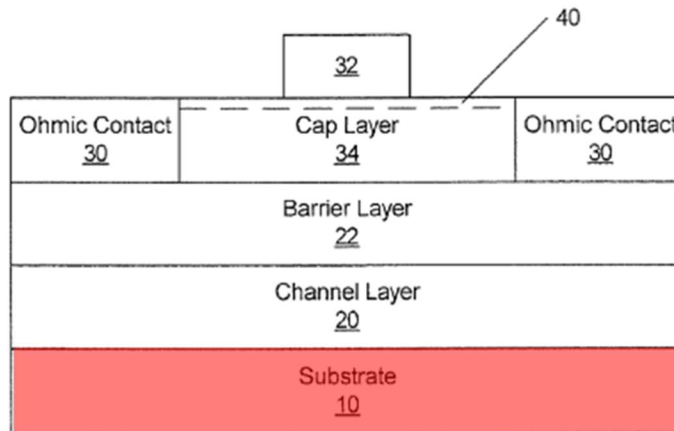


Figure 2A

Smith, Fig. 2A.

3. [1b] a set of III-N transition layers above the substrate,

Smith discloses [1b]. *Shealy*, [0144]-[0145]. *Smith* discloses the transistor includes “transition layers” that “may be provided on the **substrate 10**.” *Smith*, [0070]. *Smith* discloses the transition layers are formed with a III-nitride material, AlN specifically. *Id.*; *Shealy*, [0144]. This is the same material specified in the '294 patent. *Compare Smith*, [0070] (describing AlN transition layers), with '294 patent, 1:56-2:2 (same). Modified Figure 2A below shows *Smith*'s **transition layers**, which *Smith* describes but does not show, above **substrate 10**. *Smith*, [0070] (“**transition layers** (not shown) may be provided on the **substrate 10**”).

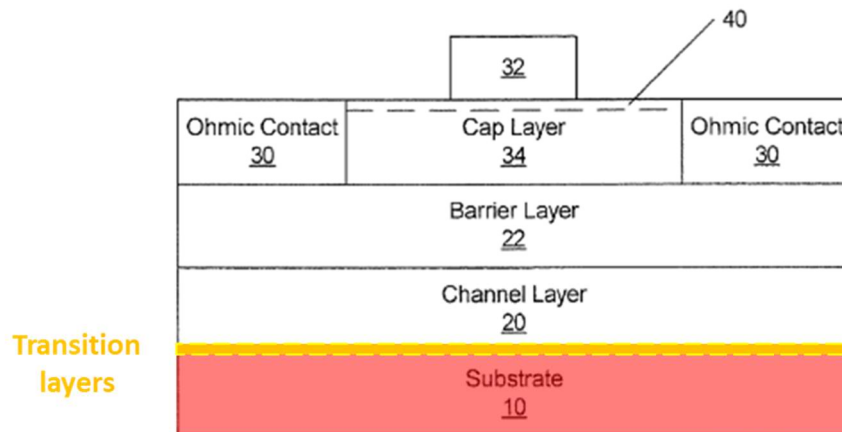


Figure 2A

Smith, Fig. 2A (modified).

4. [1c] a III-N buffer layer above the set of transition layers,

Smith discloses [1c] by disclosing a “channel layer 20 [that] may be deposited on the **substrate 10** using buffer layers, **transition layers**, and/or nucleation layers.” *Id.*, [0073]; *Shealy*, [0146]-[0149]. *Smith* discloses the “channel layer 20 is a Group III-nitride, such as $\text{Al}_x\text{Ga}_{1-x}\text{N}$ where $0 \leq x < 1$ ” (*Smith*, [0074]), describing overlapping formulations to the ones the ’294 patent associates with the buffer layer. ’294 patent, 2:63-66 (describing the buffer as “InAlGaN with any concentration of In and Al (including 0% In and/or Al)”). *Smith*’s channel layer serves the same function of “separat[ing] the transition layers 32 from a barrier layer 34” (*id.*, 2:62-63) as the buffer layer in the ’294 patent. *Smith*, [0070]-[0073]; *Shealy*, [0147]. Therefore, despite the difference in nomenclature, *Smith* discloses the “III-N buffer layer” of [1c] by describing the “channel layer 20.” *Id.*, [0074]; *Adasa Inc. v. Avery Dennison*

Corp., 55 F.4th 900, 913 (Fed. Cir. 2022) (“[A] prior art inventor need not ‘conceive of its invention using the same words as the patentee would later use to claim it.’”); MPEP §2131 (“identity of terminology is not required” (citing *In re Bond*, 910 F.2d 831 (Fed. Cir. 1990))). Figure 2A shows *Smith*’s **channel layer 20** above the **transition layers**.

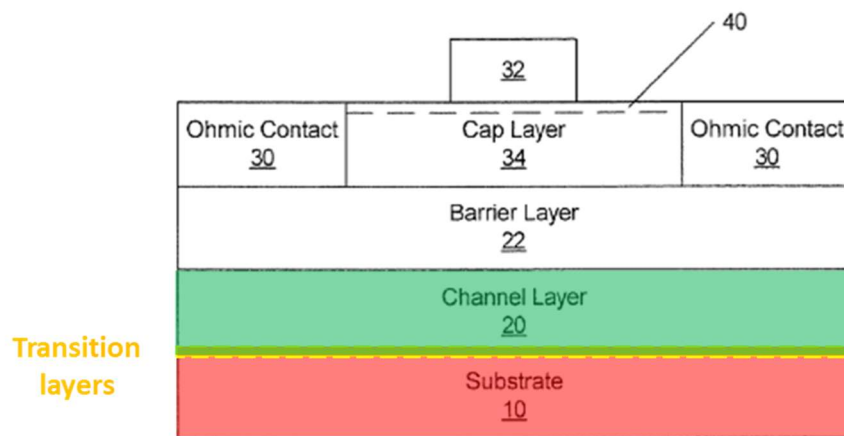


Figure 2A

Smith, Fig. 2A (modified).

5. [1d] a III-N barrier layer above the buffer layer,

Smith discloses [1d]. *Shealy*, [0150]. *Smith* discloses a “barrier layer 22 [that] is provided on the channel layer 20.” *Smith*, [0075]. *Smith* discloses “[t]he barrier layer 22 may be a Group III-nitride.” *Id.* Like the ’294 patent, *Smith* discloses the barrier layer is formed with AlGa_N. *Compare id.* (“barrier layer 22 is AlN, AlInN, AlGa_N or AlInGa_N”), with ’294 patent, 2:66-7:1 (“barrier layer 34 is formed of AlGa_N”). Figure 2A shows *Smith*’s **barrier layer 22** above **channel layer 20**.

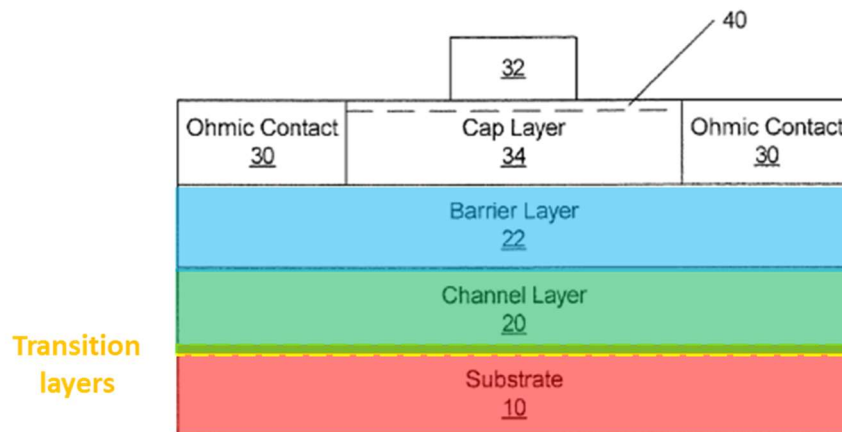


Figure 2A

Smith, Fig. 2A (modified).

6. [1e] a compensated GaN layer above the barrier layer, and

Smith, alone or in view of *Kigami* or *Uemoto*, renders obvious [1e] under both proposed constructions of “a compensated GaN layer.” *Shealy*, [0151]-[0163].

Smith teaches a “GaN layer above the barrier layer” by disclosing a “cap layer 34.” *Smith*, [0085]; *Shealy*, [0152]. *Smith* specifies “cap layer 34, 34’ may be a GaN based cap layer, such as a GaN layer.” *Smith*, [0085]. *Smith* further discloses the cap layer being doped, with “a dopant incorporated throughout the cap layer 34” and a “doped region 40 [that] may be provided by a region of increased dopant concentration.” *Id.* *Smith* teaches that the level of doping should be controlled to be high enough to reduce leakage current, but low enough to not act as a conductive layer. *Id.*, [0087]. Figure 2A shows *Smith*’s **cap layer 34** above the **barrier layer 22**.

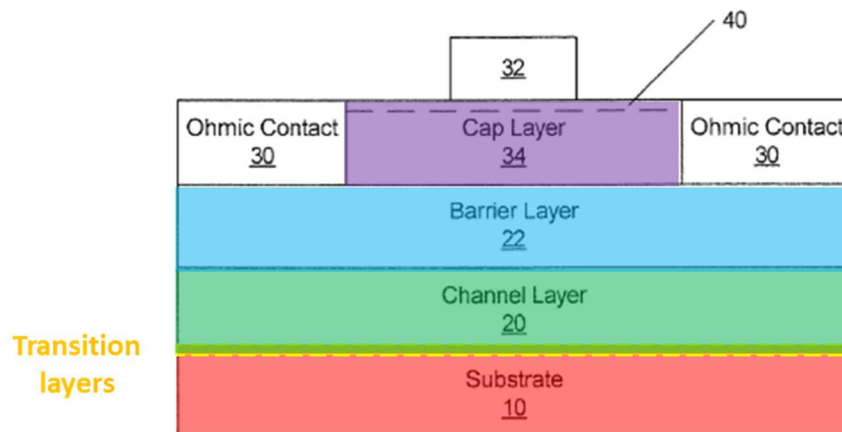


Figure 2A

Smith, Fig. 2A (modified).

Petitioner's Construction

If “compensated GaN layer” is properly construed as “*doped GaN layer formed with a step to passivate its impurities*,” Petitioner’s construction, *Smith*, alone or in combination with *Kigami* or *Uemoto*, renders obvious [1e]. *Shealy*, [0153]-[0157]

Ground 1A: Under Petitioner’s construction, element [1e] should be interpreted as product-by-process. *Supra* §§VII, VIII.B.1. *Smith* discloses a GaN layer passivated with acceptor impurities. *Smith*, [0087]. And because it was well-known that as-grown GaN films are naturally hydrogen passivated (*supra* §IV.C) a POSITA would have recognized that *Smith*’s cap layer 34 has passivated impurities meeting the product-by-process limitation of a “doped GaN layer formed with a step

to passivate its impurities,” regardless of the specific compensation process. *Shealy*, [0154].

To the extent it is argued the “compensated GaN layer” limitation should not be interpreted as product-by-process, *Smith* still renders element [1e] obvious. *Smith* identifies the level of doping as a result effective variable to control leakage and a POSITA knew that hydrogenation affected the level of doping. *Supra* §VIII.B.1. Because a POSITA knew that hydrogenation affected the “level of doping” in a GaN layer, a POSITA would have found it obvious to adjust doping in **cap layer 34** “with a step to passivate its impurities,” as required by [1e] under Petitioner’s construction. *Shealy*, [0155]; *E.I. DuPont*, 904 F.3d at 1011.

Ground 1B: The combination of *Smith* and *Kigami* also renders obvious [1e] under Petitioner’s construction because applying *Kigami*’s hydrogenation to *Smith* “compensates” (as the term is used in the ’294 patent) **cap layer 34**. Applying *Kigami*’s hydrogenation to *Smith* makes **cap layer 34** a “doped GaN layer formed with a step to passivate its impurities.” A POSITA would have been motivated to apply *Kigami*’s hydrogenation to *Smith*. *Supra* §VIII.C.2. Such modification would introduce hydrogen into *Smith*’s **cap layer 34**, passivating its acceptor impurities. *Shealy*, [0156]. As modified by *Kigami*, *Smith*’s **cap layer 34** would be a “doped GaN layer formed with a step to passivate its impurities.” *ITC Constructions*, 9.

Ground 1C: The combination of *Smith* and *Uemoto* also renders obvious [1e] under Petitioner’s construction because applying *Uemoto*’s technique to diffuse hydrogen would result in **cap layer 34** being “compensated,” as the term is used in the ’294 patent. *Shealy*, [0157]. Incorporating *Uemoto*’s hydrogen diffusion technique, using a hydrogen diffusion film and a thermal diffusion, to *Smith* makes **cap layer 34** a “doped GaN layer formed with a step to passivate its impurities.” A POSITA would have found it obvious to use *Uemoto*’s technique to diffuse hydrogen into *Smith*’s **cap layer 34**. *Supra* §VIII.C.3. Such a modification introduces hydrogen in cap layer 34 and passivates impurities to form high resistive regions that reduce leakage. *Id.*; *Shealy*, [0157]. When combined with *Uemoto*, *Smith*’s **cap layer 34** is a “doped GaN layer formed with a step to passivate its impurities.”

Patent Owner’s Construction

Patent Owner’s construction is vague and overly broad. *Supra* §VII. It encompasses the admitted prior art and also Petitioner’s construction. *Shealy*, [0158]-[0159]. Therefore, the same prior art disclosure showing “a compensated GaN layer” under Petitioner’s construction, shows it under Patent Owner’s. *Id.*, [0159]. But additionally, **Grounds 1A-1C** also explicitly disclose “a compensated GaN layer” under Patent Owner’s construction.

Ground 1A: If “compensated GaN layer” is construed as Patent Owner proposes (as “semiconductor GaN gate material in which one type of dopant,

impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor).”), *Smith* discloses [1e]. *Smith* specifies that **cap layer 34** is a GaN layer doped with a “p-type dopant, such as Mg.” *Smith*, [0085]. As explained previously, by 2009 it was well-known that hydrogen would be naturally present in such layers. *Supra* §IV.C. It was known that hydrogen would be present even in as-grown GaN materials, forming acceptor-H neutral complexes that passivate the impurity. *Id.* (citing *Nakamura*, 1266; *Quay*, §3.3.1). Therefore, if “compensated GaN layer” is construed as the Patent Owner proposes, *Smith* discloses [1e] by disclosing the acceptor-doped **cap layer 34** because it is a “GaN gate material,” including “one type of dopant, impurity, or imperfection” (the innate hydrogen) that “partially cancels the electrical effects of the other type of dopant, impurity, or imperfection” (the acceptor dopant). *Shealy*, [0160].

Grounds 1B/1C: The *Smith/Kigami* and *Smith/Uemoto* combinations also each render obvious [1e] under the Patent Owner’s proposed construction. *Smith* discloses a **cap layer 34** is doped with magnesium. *Smith*, [0087]. And under each combination with *Kigami* or *Uemoto*, *Smith*’s **cap layer 34** would be “GaN gate material,” with “one type of dopant, impurity, or imperfection” (the introduced or diffused hydrogen disclosed in *Kigami* or *Uemoto*) that “partially cancels the electrical effects of the other type of dopant, impurity, or imperfection” (the acceptor

dopant Smith disclose). *Shealy*, [0161]-[0163]. In each combination, *Smith*'s **cap layer 34** would include hydrogen—resulting either from *Kigami*'s ionized gas hydrogenation (*Kigami*, [0027]) or *Uemoto*'s hydrogen diffusion (*Uemoto*, [0063])—that inactivates or passivates the dopants in the layer. *Id.* Both combinations, thus, make *Smith*'s **cap layer 34** a “semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor).” *ITC Construction*, 1.

7. [1f] a gate contact above the compensated GaN layer.

Smith discloses [1f]. *Shealy*, [0164]. *Smith*'s transistor comprises a “gate contact 32 may also be formed on the cap layer.” *Smith*, [0082], [0085]. Further, *Smith* discloses the gate contact being formed with “conventional materials ... such as Ni, Pt, NiSix, Cu, Pd, Cr, W and/or WSiN.” *Id.*, [0082]. These are the materials the '294 patent specifies for the gate contact. '294 patent, 3:4-7 (“gate contact 37, formed of[,] for example, Ta, Ti, TiN, W, or WSi2”). Figure 2A shows *Smith*'s **gate contact 32** above **cap layer 14**.

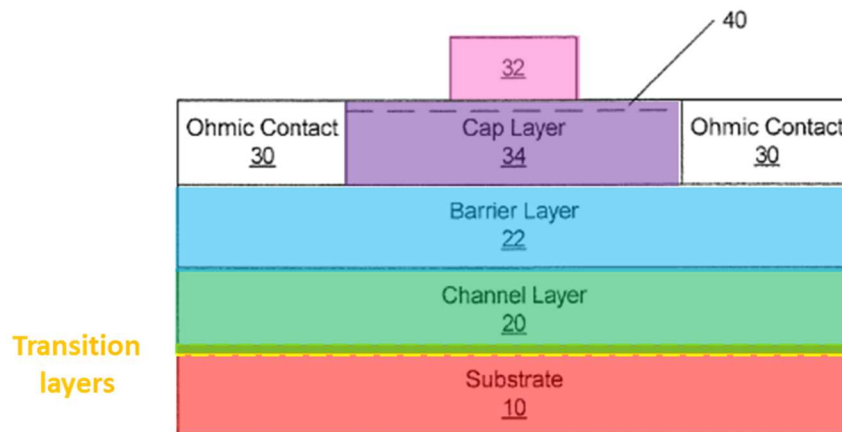


Figure 2A

Smith, Fig. 2A (modified).

E. Claim 2 - The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.

Smith, alone or in combination with *Kigami* or *Uemoto*, renders claim 2 obvious. *Shealy*, [0165]-[0168].

Ground 1A: As explained above, by 2009 a POSITA would have known that hydrogen passivates acceptor dopants. *Supra* §IV.C; *Shealy*, [0166]. A POSITA would have known that hydrogen is naturally present in as-grown GaN layers and that hydrogen forms complexes with acceptor dopants, inactivating or passivating them. *Id.* Because *Smith* discloses cap layer 34 being acceptor doped, a POSITA would have recognized that *Smith*'s cap layer 34 would be naturally passivated with hydrogen.

Grounds 1B and 1C: Each of *Kigami* and *Uemoto* also discloses that acceptor dopants are passivated with hydrogen. *Shealy*, [0167]-[0168]. *Kigami* discloses that “introduced hydrogen atoms inactivate the p-type impurity.” *Kigami*, [0014]. *Uemoto* discloses that magnesium (an acceptor) is inactivated when combined with hydrogen. *Uemoto*, [0049], [0063]. The *Smith/Kigami* and *Smith/Uemoto* combinations, which incorporate hydrogen into **cap layer 34**, disclose **cap layer 34** containing acceptor type dopants atoms passivated with hydrogen.

F. Claim 3 - The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be, and Ca.

Smith discloses claim 3, by disclosing that **cap layer 34** can be doped with p-type dopants, including “Mg, Be, Zn, Ca and/or C.” . *Shealy*, [0169]; *Smith*, [0087].

G. Claim 4

1. [4p] A column III Nitride transistor comprising:

[4p] is identical to [1p]. *Smith* discloses [4p] for the same reasons. *Supra* §VIII.D.1; *Shealy*, [0170]; *Ford Motor Co. v. Paice LLC*, IPR2015-00784, Paper 12 at 19 (PTAB Oct. 29, 2015) (accepting the same incorporation by reference).

2. [4a] a substrate,

[4a] is identical to [1a]. *Smith* discloses [4a] for the same reasons. *Supra* §VIII.D.2; *Shealy*, [0171].

3. [4b] a set of III-N transition layers above the substrate,

[4b] is identical to [1b]. *Smith* discloses [4b] for the same reasons. *Supra* §VIII.D.3; *Shealy*, [0172].

4. [4c] a III-N buffer layer above the set of transition layers,

[4c] is identical to [1c]. *Smith* discloses [4c] for the same reasons. *Supra* §VIII.D.4; *Shealy*, [0173].

5. [4d] a III-N barrier layer, and

[4d] is substantially similar to [1d]. *Supra* §VIII.D.5. The difference is that unlike [1d], [4d] does not require the barrier layer to be “above the buffer layer.” *Shealy*, [0174]. Because element [4d] is broader than [1d], *Smith* discloses [4d] for the same reasons. *Id.*

6. [4e] a semi-insulating III-N layer above the barrier layer.

Smith discloses [4e]. *Id.*, [0175]-[0176]. *Smith* discloses that cap layer 34 can be a “semi-insulating III-N layer,” describing that cap layer 34 can be formed with “[t]echniques for co-doping Group III-nitride materials.” *Smith*, [0085]. In *Saxler*⁸⁷⁴ (Ex. 1016), which *Smith* incorporates by reference, *Smith* explains that co-doping “provide[s] semi-insulating Group III nitride semiconductor layers.” *Saxler*⁸⁷⁴, [0005]. *Smith*’s incorporation of *Saxler*⁸⁷⁴ makes it effectively part of *Smith*’s disclosure. *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906 (Fed. Cir. 2018) (“Incorporation by reference provides ‘a method for integrating material from

various documents into a host document[] ... by citing such material in a manner that makes clear that the material is effectively part of the host document as if it were explicitly contained therein.” (alteration in original) (quoting *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000)). And because *Smith* incorporates *Saxler*⁸⁷⁴ specifically for the formation of cap layer 34 (*Smith*, [0085]), *Smith* itself provides express motivation. *Shealy*, [0175]-[0176].

Like the '294 patent, *Smith* discloses the semi-insulating layer being formed with AlGa_N or Ga_N, doped with deep level dopants. Compare *Smith*, [0089] (“cap layer 34, 34' may be a Ga_N based cap layer, such as a Ga_N layer and/or an AlGa_N ... deep level dopants may be Fe, C, V, Cr, Mn, Ni, Co”), with '294 patent, 3:57-59 (“Semi-insulating layer 39 may comprise, for example, AlGa_N or Ga_N, with deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni.”).

Figure 2A shows *Smith*'s **semi-insulating cap layer 34** above **barrier layer 22**.

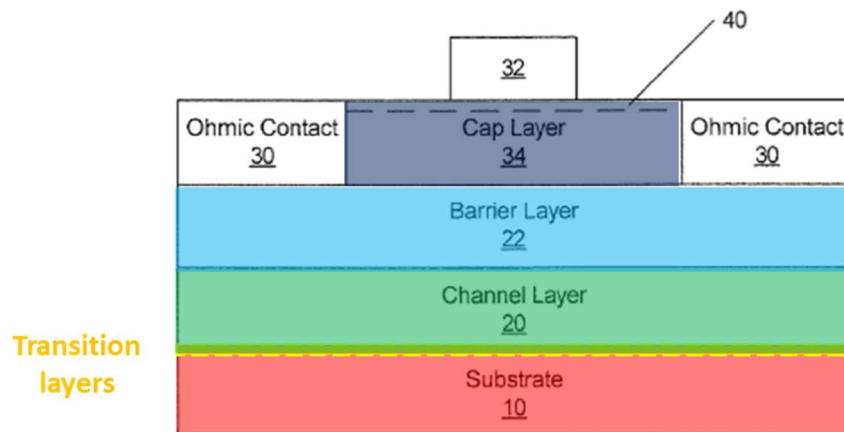


Figure 2A

Smith, Fig. 2A (modified).

H. Claim 5 - The transistor of claim 4, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms.

Smith discloses claim 5. *Shealy*, [0177]. *Smith* discloses that a **semi-insulating cap layer 34** includes “a region doped with deep level dopants.” *Smith*, [0089]. *Smith* specifies examples of deep level dopants such as “Fe, C, V, Cr, Mn, Ni and/or Co.” *Id.*, [0085]. These are the same deep level dopants the ’294 patent identifies as “deep acceptor type.” ’294 patent, claim 6; *Shealy*, [0177].

I. Claim 6 - The transistor of claim 5 where the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.

Smith discloses claim 6, by disclosing **semi-insulating cap layer 34** being “doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co.” *Shealy*, [0178]; *Smith*, [0015], [0089].

J. Claim 7

1. [7p] A column III Nitride transistor comprising:

[7p] is identical to [1p]. *Smith* discloses [7p] for the same reasons. *Supra* §VIII.D.1; *Shealy*, [0179].

2. [7a] a substrate,

[7a] is identical to [1a]. *Smith* discloses [7a] for the same reasons. *Supra* §VIII.D.2; *Shealy*, [0180].

3. [7b] a set of III-N transition layers above the substrate,

[7b] is identical to [1b]. *Smith* discloses [7b] for the same reasons. *Supra* §VIII.D.3; *Shealy*, [0181].

4. [7c] a III-N buffer layer above the set of transition layers,

[7c] is identical to [1c]. *Smith* discloses [7c] for the same reasons. *Supra* §VIII.D.4; *Shealy*, [0182].

5. [7d] a III-N barrier layer, and

[7d] is identical to [4d]. *Smith* discloses [7d] for the same reasons. *Supra* §VIII.G.5; *Shealy*, [0183]; *Shealy*, [0183].

**6. [7e] a semi-insulating III-N layer above the barrier layer,
and**

[7e] is identical to [4e]. *Smith* discloses [7e] for the same reasons. *Supra* §VIII.G.6; *Shealy*, [0184].

7. [7f] a confinement layer above the semi-insulating III-N layer.

Smith, alone or in combination with *Uemoto*, renders obvious [7f].

Ground 1A/B: *Smith* discloses [7f] by disclosing a “passivation layer” above **semi-insulating cap layer 34**. *Shealy*, [0185]-[0187]. *Smith* discloses a “passivation layer 100” formed on cap layers—including **semi-insulating cap layer 34**. *Smith*, [0095] (Describing use of “passivation layer 100” with “cap layer 34”). *Smith* discloses the “passivation layer 100” may be incorporated with materials “such as SiN or SiOx.” *Id.*, [0090]. *Smith*’s passivation layer, thus, is composed with the same materials the ’294 patent associates with the confinement layer. ’294 patent, 4:34-35 (“confinement layer can be composed of AlGaIn, SiN, SiO₂”). Therefore, despite the difference in nomenclature, *Smith* discloses the “confinement layer” of [7f] by describing the “passivation layer 100.” *Smith*, [0090]-[0095]; *Adasa* 55 F.4th at 913; *In re Bond*, 910 F.2d at 832-33. Modified Figure 3B substitutes cap layer 24 for cap layer 34 as discussed in *Smith* (*Smith*, [0095]), and highlights *Smith*’s **passivation layer** above the **semi-insulating cap layer 34**.

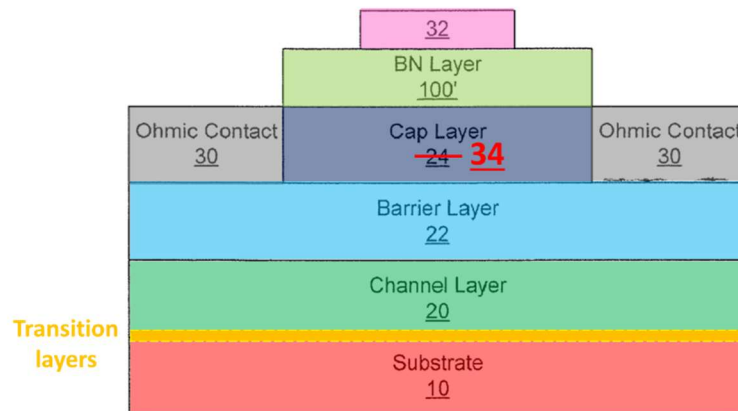


Figure 3B

Smith, Fig. 3B (modified).

Ground 1C: The *Smith/Uemoto* combination renders obvious [7f]. When *Smith* is combined with *Uemoto* to include a “hydrogen diffusion film,” the diffusion film discloses “a confinement layer above the semi-insulating III-N layer.” *Shealy*, [0188]-[0189]. *Uemoto* discloses the hydrogen diffusion film is “made of silicon nitride (SiN).” *Uemoto*, [0063]. This is the same material the ’294 patent associates with the “confinement layer.” ’294 patent, 4:34-35. A POSITA would have been motivated incorporate *Uemoto*’s hydrogen diffusion film on *Smith*’s cap layers. *Supra* §VIII.C.3. Modified Figure 2A shows that in the combination of *Smith* and *Uemoto*, *Uemoto*’s **hydrogen diffusion film** is above **semi-insulating cap layer 34**.

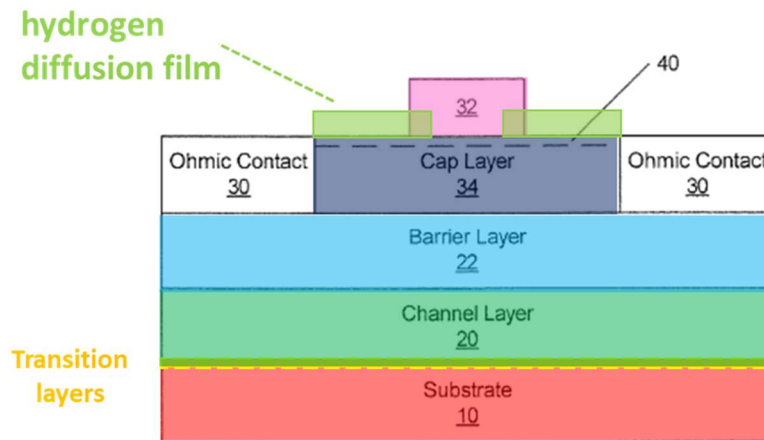


Figure 2A

Smith, Fig. 2A (modified).

K. Claim 8 - The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.

Claim 8 is substantially similar to claim 6 (requiring “the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V”), which depends from claim 5 (further requiring “the semi-insulating III-N layer contains deep acceptor type dopant atoms”). *Shealy*, [0190]. *Smith* discloses claim 8 for the same reasons. *Supra* §VIII.I.

L. Claim 9 - The transistor of claim 7, wherein the confinement layer is made of SiN, SiO₂, Al₂O₃, HfO₂, Ga₂O₃, or InAlGaN.

Smith, alone or in combination with *Uemoto*, renders obvious claim 9. *Shealy*, [0191]-[0194].

Ground 1A/B: *Smith* discloses **passivation layer 100** being made of SiN or SiO₂, disclosing **passivation layer 100** “may be incorporated with layers of other materials, such as SiN or SiO_x.” *Smith*, [0090]; *Shealy*, [0192].

Ground 1C: *Uemoto* discloses **hydrogen diffusion film 17** being “made of silicon nitride (SiN).” *Uemoto*, [0063]; *Shealy*, [0193].

M. Claim 10

1. [10p] A compensated gate MISFET transistor comprising:

Smith, alone or in combination with *Kigami* or *Uemoto*, discloses [10p]. *Shealy*, [0195]-[0198].

Ground 1A: *Smith* discloses various GaN transistors, which the '294 patent identifies as “MISFET.” '294 patent, Abstract (“[a] MISFET, such as a GaN transistor”). *Smith* also discloses transistors including MIS layers. *Smith*, [0090] (“[I]n the embodiments illustrated in FIG. 3B, a MISHEMT may be provided”). And *Smith* discloses transistors with “compensated” or “semi-insulating” cap layers. *Supra* §§VIII.D.6, VIII.G.6; *Shealy*, [0196]. *Smith*’s Figure 3B is reproduced below, but substituting cap layer 24 for cap layer 34 (as disclosed in *Smith*’s paragraph [0095]), illustrating the “compensated gate MISFET transistor” disclosure.

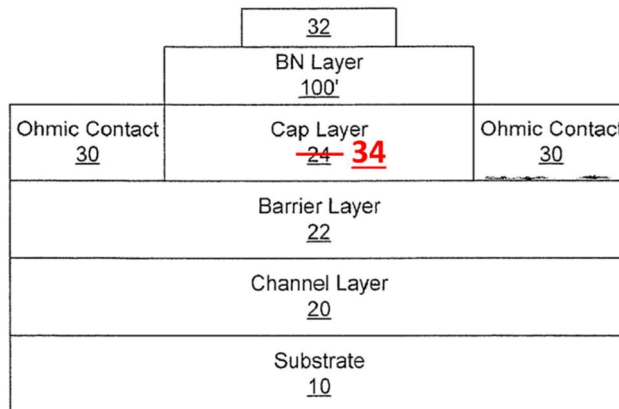


Figure 3B

Smith, Fig. 3B (modified)

Ground 1B/C: Additionally, each of the *Smith/Kigami* and *Smith/Uemoto* combinations discloses a “compensated gate MISFET transistor.” *Kigami* discloses forming the transistor as a “semiconductor device having the MIS-type gate.” *Kigami*, [0014]. *Uemoto* discloses a “structure for obtaining the normally-off type FET” and describes transistors using the MIS-type structures. *Uemoto*, [0007], [0043], [0055], Fig. 7; *Shealy*, [0197]-[0198].

2. [10a] a III-N barrier layer beneath a gate contact,

[10a] is substantially similar to [1d]. *Supra* §VIII.D.5. The difference is that in [10a] the barrier layer is “beneath a gate contact,” instead of being “above the buffer layer” like in [1d]. *Shealy*, [0199]-[0200]. As shown below, however, *Smith* also discloses barrier layer 22 beneath gate contact 32. *Smith* thus discloses [10a].

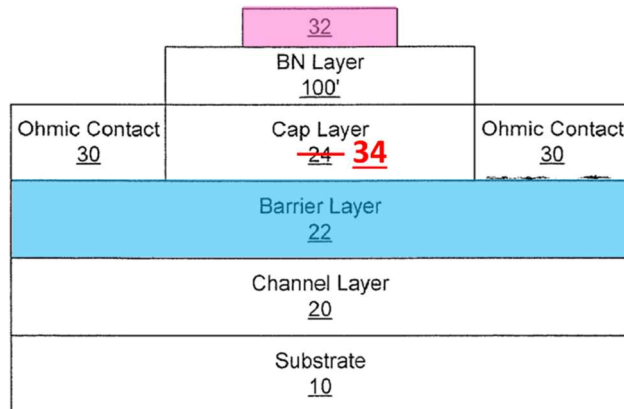


Figure 3B

Smith, Fig. 3B (modified).

3. [10b] a drain contact, a source contact, and

Smith discloses [10b]. *Shealy*, [0201]. *Smith* discloses that “ohmic contacts 30 are provided on the barrier layer 22” and that “the ohmic contacts 30 provide source and drain contacts.” *Smith*, [0080]-[0081]. Figure 3B shows *Smith*’s ohmic contacts 30 providing the source and drain.

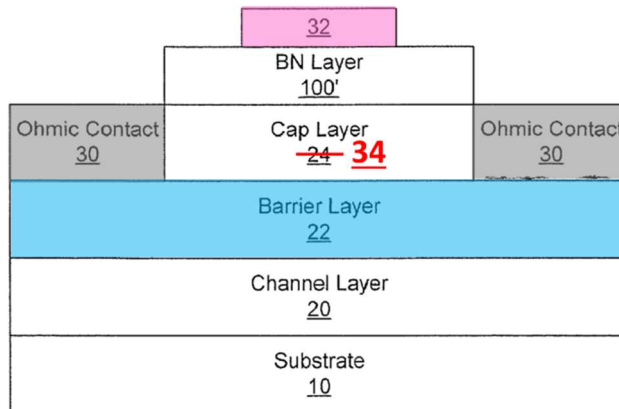


Figure 3B

Smith, Fig. 3B (modified).

4. [10c] a semi-insulating III-N layer between the barrier layer and the gate contact.

[10c] is substantially similar to [4e]. *Supra* §VIII.G.6. The difference is that in [10c] the semi-insulating layer is “between the barrier layer and the gate contact,” instead of being “above the barrier layer” like in [4e]. *Shealy*, [0202]-[0203]. But as shown below, *Smith* describes a **semi-insulating cap layer 34** (*supra* §VIII.G.6) and discloses the **semi-insulating cap layer 34** being between **barrier layer 22** and **gate contact 32**. *Smith* discloses [10c].

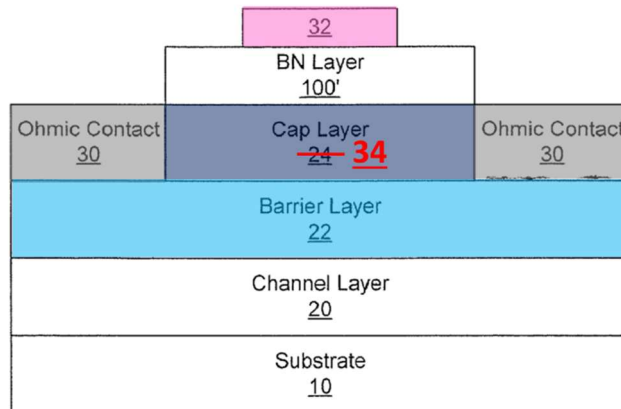


Figure 3B

Smith, Fig. 3B (modified).

N. Claim 11 - The transistor of claim 10, further comprising a confinement layer above the semi-insulating III-N layer.

Claim 11's feature is identical to [7f]. *Shealy*, [0204]. *Smith* discloses claim 11 for the same reasons. *Supra* §VIII.J.7. *Smith*'s "**passivation layer 100**" discloses the confinement layer in the claim. *Id.* Further, as shown below, *Smith* discloses **passivation layer 100** being above **semi-insulating cap layer 34**.

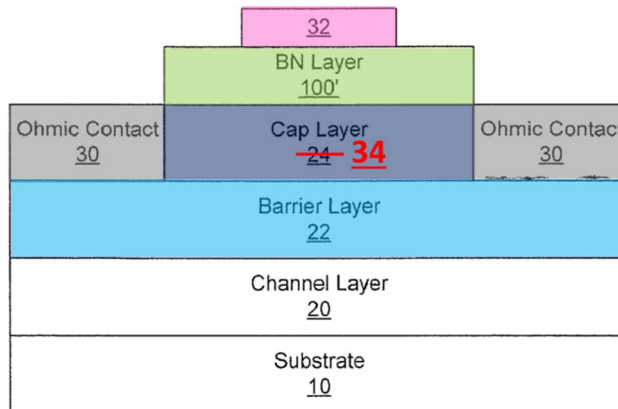


Figure 3B

Smith, Fig. 3B (modified).

- O. Claim 12 - The transistor of claim 10, further comprising a spacer layer between the semi-insulating layer and the barrier layer.**

Smith discloses claim 12. *Shealy*, [0205]-[0211]. *Smith* discloses fabricating transistors “with barrier/spacer layer” and discloses that **barrier layer 22** is “provided with multiple layers.” *Smith*, [0061], [0120]. *Smith* discloses that the barrier layer “may include, for example, barrier layers having combinations of GaN, AlGaN and/or AlN layers.” *Id.*, [0120]. *Smith* also incorporates by reference *Chavarkar* (Ex. 1021), making *Chavarkar* part of *Smith*’s disclosure, and *Chavarkar* discloses the formation of the transistor “with barrier/spacer layer” for “improved high frequency performance.” *Chavarkar*, Title, Abstract; *Paice*, 881 F.3d at 906. Because *Smith* incorporates *Chavarkar* specifically for the formation of barrier layer 22 (*Smith*, [0075]), *Smith* itself provides an express motivation. *Shealy*, [0206].

By disclosing that the barrier layer is provided with multiple layers and “with barrier/spacer layer,” *Smith* discloses “a spacer layer between the semi-insulating layer and the barrier layer,” because one of the layers in the “combinations of GaN, AlGaIn and/or AlN layers” works as the “spacer.” *Id.*, [0207]. Any layer in the *Smith*’s barrier combination would be “a low Mg region,” the characteristic the ’294 patent associates with the “spacer.” ’294 patent, 4:67-5:1 (“spacer layer 49, which is a low Mg region”). Figure 3B below, which has been modified to exemplify *Smith*’s disclosure of **barrier layer 22** being formed with multiple layers, shows that the multilayer barrier would include a *spacer layer* between **semi-insulating layer cap layer 43** and **barrier layer 22**. *Shealy*, [0208].

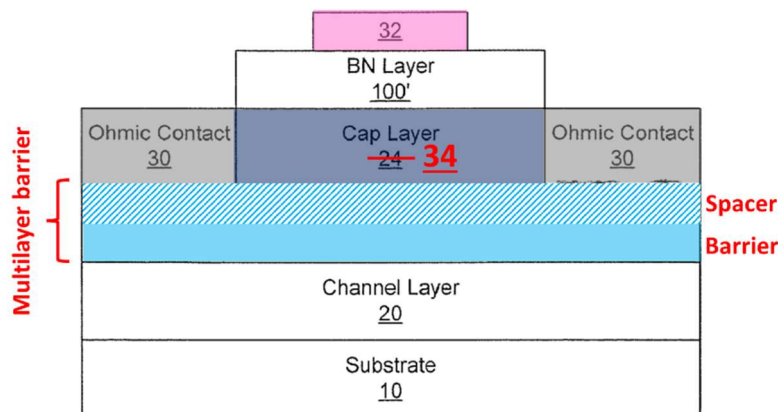


Figure 3B

Smith, Fig. 3B (modified).

Smith additionally discloses the claim 12 feature by disclosing cap layers can be formed as “a multilayer cap layer (73', 74', 75) on the **barrier layer 22**.” *Smith*,

[0113]. *Smith* discloses that layers in the multilayer cap can be adjusted to control the depth or spacing of the gate, stating that the “thickness of the layers of the multilayer cap (GaN, AlN, and AlGaIn) and the composition of the AlGaIn can all be adjusted to obtain the improved device performance.” *Id.*, [0117]; *Shealy*, [0209]. In disclosing a “multilayer cap,” *Smith* discloses “a spacer layer between the semi-insulating layer and the barrier layer,” because one of the layers in the multilayer cap works as the “spacer.” *Shealy*, [0210]-[0211] Any layer in the multilayer cap, and particularly lower layers (outside *Smith*’s doped region 40), would be “a low Mg region,” the characteristic the ’294 patent associates with the “spacer.” ’294 patent, 4:67-5:1. Figure 3B has been modified to exemplify *Smith*’s disclosure of the cap layer being formed with multiple layers and disclosing the feature of claim 12.

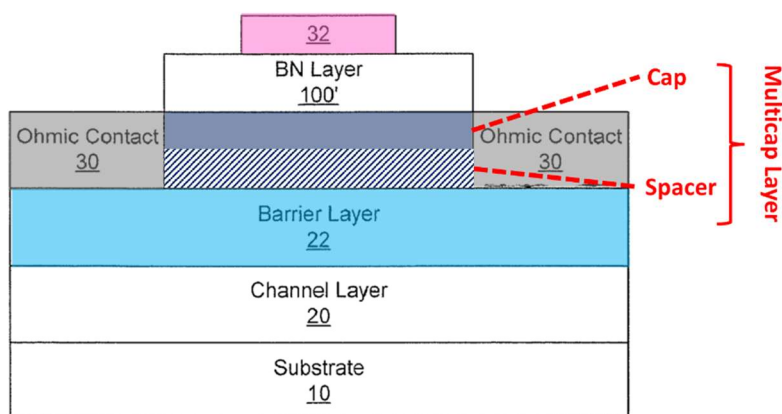


Figure 3B

Smith, Fig. 3B (modified).

IX. GROUND 2: *UEMOTO* IN VIEW OF *SMITH* RENDERS CLAIMS 1-12 OBVIOUS.

A. Overview of the *Uemoto* Ground

Uemoto discloses transistors formed by stacking the admittedly “conventional” layers (e.g., **transition**, **buffer**, **barrier**) on a **substrate** and forming the **gate**, **source**, and **drain**. *Uemoto*, [0031]-[0035]; *Shealy*, [0212]-[0213].

Uemoto discloses forming a “compensated GaN layer” under both Parties’ proposed constructions. *Uemoto* discloses that “a third nitride semiconductor layer 15” is formed with GaN doped with magnesium. *Uemoto*, [0033], [0054]. And *Uemoto* discloses layer 15 being “compensated,” under both proposed constructions, because *Uemoto* discloses that the impurities in region 15b of the layer 15 are inactivated when “hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment.” *Id.*, [0063]. Because *Uemoto* discloses layer 15 being magnesium doped GaN and processed with a hydrogen diffusion step so that hydrogen inactivates the magnesium, *Uemoto* discloses “a compensated GaN layer” under both parties’ constructions. *Shealy*, [0214].

To the extent the claims require using multiple “transition layers,” *Uemoto* only explicitly discloses one. *Id.*, [0215]. *Uemoto* also does not explicitly disclose using a “semi-insulating layer” or a “spacer layer.” *Id.* And *Uemoto* does not

expressly disclose the specific “deep dopants” recited in certain dependent claims (e.g., “C, Fe, Mn, Cr and V”). *Id.* But a POSITA knew about the deep level dopants, and about the transition, semi-insulating, and spacer layers, and would have found it obvious to include them in *Uemoto*, based on either general knowledge or *Smith*. *Id.*, [0216].

Smith discloses the “transition layers,” deep level dopant “semi-insulating layer,” and “spacer layer.” *Id.*, [0217]; *supra* §§VIII.D.3 (limitation [1b]), VIII.G.6 (limitation [4e]), VIII.I (claim 6), VIII.O (claim 12). As explained above, a POSITA would have considered *Uemoto* and *Smith* analogous art and their teachings combinable. *Supra* §VIII.C.3. A POSITA would have been motivated to modify *Uemoto* to incorporate the “transition layers,” “semi-insulating layer” (with deep level dopants), and “spacer layers” as disclosed in *Smith*.

1. Motivation to incorporate *Smith*’s “transition layers” in *Uemoto*

Smith teaches that “transition layers ... provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device.” *Smith*, [0070]. *Smith* also discloses that the transition layers can be useful for “strain balancing.” *Id.* And incorporating by reference *Saxler015* (Ex. 1013) and *Saxler482* (Ex. 1022)—making these publications part of its disclosure—*Smith* discloses how transition layers “provide means for reducing stress” and prevent

cracking. *Saxler015*, [0026]; *Saxler482*, [0021]; *Shealy*, [0219]; *Paice*, 881 F.3d at 906. A POSITA would have considered these effects advantageous to *Uemoto*'s transistor, particularly because *Uemoto* describes using the same substrate and GaN layer materials as *Smith*. *Uemoto*, [0054]; *Smith*, [0069]; *Shealy*, [0219]. Because *Smith* incorporates *Saxler015* and *Saxler482* specifically for the formation of buffers and transition layers (*Smith*, [0070]), *Smith* itself provides an express motivation. *Shealy*, [0218]-[0219].

Uemoto's transistors already include a transition layer (buffer layer 12), and *Smith* discloses that including additional transition layers over the buffer improves strain balancing, minimizing cracking. *Shealy*, [0220]. *Saxler015* discloses that including additional transition layers over a buffer—like “device match,” “graded,” and “mismatch” layers—improve the transistor robustness because “the likelihood of the total strain of the structure exceeding a threshold at which cracking occurs may be reduced.” *Saxler015*, [0042], Fig. 2. A POSITA would have considered the reduction in the likelihood of cracking and the ability to better match lattices advantageous to *Uemoto*'s transistor. *Shealy*, [0220]. *Uemoto*, like *Smith*, was also concerned with improvements in the transistor fabrication and robustness. *Uemoto*, [0079]; *Shealy*, [0220].

A POSITA would have also incorporated the transition layers of *Smith* to *Uemoto* with a reasonable expectation of success. *Shealy*, [0221]. The '294 patent

does not explain how to form the transition layers over a silicon substrate, acknowledging instead that they were conventional. '294 patent, 1:55-2:2; *Shealy*, [0221]. Providing multiple transition layers in *Uemoto*'s device would have required only conventional techniques in their ordinary and expected manner. *Shealy*, [0221]. A POSITA would have reasonably expected to succeed in using *Smith*'s multiple transition layers when fabricating *Uemoto*'s device. *Id.*

2. Motivation to make *Uemoto*'s layer 15 semi-insulating by including deep level dopants as disclosed in *Smith*

Smith discloses that using co-doping and deep level dopants in cap layers improve transistor characteristics. *Id.*, [0223]. *Smith* discloses that deep level dopants can “screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents.” *Smith*, [0089]. *Smith* also discloses that “co-doping [of] Group III-nitride materials” improves transistor stability, reduces leakage current, and provides predictable semi-insulating characteristics. *Id.*, [0085], [0089]. For example, in describing methods to form cap layers, *Smith* incorporates *Saxler874* (Ex. 1016) by reference, making *Saxler874* part of *Smith*'s disclosure. *Smith*, [0085]; *Paice*, 881 F.3d at 906. *Saxler874* explains that the “co-doping of a Group III nitride layer ... provide[s] a predictable characteristic of a semi-insulating Group III nitride layer.” *Saxler874*, [0018], [0027] (“[T]he resulting layer may be

more readily reproducible and the variations between processing runs may be reduced”).

A POSITA would have understood *Smith*’s process of forming a stable semi-insulating layer would be advantageous to *Uemoto*. *Shealy*, [0222]-[0224]. *Uemoto* also aims to reduce leakage current and improve device fabrication. *Uemoto*, [0061], [0079]. A POSITA would have identified that the leakage and fabrication improvements *Smith* discloses with semi-insulating layers would be beneficial and applicable to *Uemoto*. *Shealy*, [0224]. A POSITA, thus, would have recognized *Uemoto*’s transistor as a base device improvable with *Smith*’s teachings because both references disclose the same materials and similar structure. *Id.*

Further, a POSITA would have implemented *Smith*’s suggested co-doping and use of deep level dopant to *Uemoto* with a reasonable expectation of success. *Id.*, [0225]. By 2009, incorporation of deep level dopants in GaN layers was well-known. *Supra* §IV.C. *Smith* (incorporating *Saxler874*) specifies the techniques for the fabrication of the co-doped layer with deep level impurities. *Smith*, [0085], [0089]; *Saxler874*, [0018]-[0019], Fig. 3. A POSITA would have had a reasonable expectation of success in modifying *Uemoto* with *Smith*’s teachings based on the POSITA’s general knowledge and *Smith*’s disclosure. *Shealy*, [0225].

Incorporating *Smith*’s use of deep level dopants in *Uemoto*’s transistor would have also been a simple substitution of one known element for another. *Id.*, [0226].

The modification would be a simple substitution of doping elements or techniques. *Id.* *Uemoto* discloses doping the third nitride layer with magnesium. *Uemoto*, [0033]. A POSITA would have found it obvious to substitute the magnesium doping with the deep level dopants (or the co-doping) from *Smith*. *Shealy*, [0226]. As evidenced by *Saxler874* and *Smith*, the function and effect of co-doping and deep level dopants were known in the art. *Smith*, [0085]; *Saxler874*, [0026]. A POSITA would have found it obvious to substitute *Uemoto*'s magnesium doping with *Smith*'s deep level dopants or doping techniques. *Shealy*, [0226]. The results of the substitution would have been predictable (e.g., altering resistivity and stability as discussed in *Saxler874*). *Id.*

3. Motivation to modify *Uemoto*'s barrier layer to become a multilayer barrier "with barrier/spacer," as taught by *Smith*

Smith discloses techniques for the fabrication of transistors "with barrier/spacer layer" and discloses embodiments in which the barrier layer is "provided with multiple layers." *Smith*, [0061], [0120]. *Smith* explains that using multiple barrier layers is advantageous to, for example, "reduce or prevent alloy scattering." *Id.*, [0120]. In describing methods to form barrier layers, *Smith* incorporates by *Chavarkar*, making it part of *Smith*'s disclosure. *Smith*, [0075]; *Paice*, 881 F.3d at 906. *Chavarkar* explains that forming the transistor with multiple "barrier/spacer" layers "keeps the HEMT's gate leakage low" and "reduces the

piezoelectric scattering between the layers” improving electron mobility. *Chavarkar*, [0016], [0032]. A POSITA would have recognized that these effects were beneficial to *Uemoto* because *Uemoto* was also concerned with reducing leakage and having a large operating current. *Uemoto*, [0040], [0061]; *Shealy*, [0227]-[0228].

A POSITA would have implemented *Smith’s* suggested incorporation of a multilayer barrier to *Uemoto* with a reasonable expectation of success. *Shealy* [0229]. As the ’294 patent admits, it was “conventional” to form barrier layers in the III-nitride transistors. ’294 patent, 1:55-2:2. Turning *Uemoto’s* barrier layer into a multiple layer barrier would have required only applying conventional techniques in their ordinary and expected manner. *Shealy* [0229]. A POSITA would have reasonably expected to succeed in using *Smith’s* multibarrier layer “with barrier/spacer” when fabricating *Uemoto’s* device. *Id.*

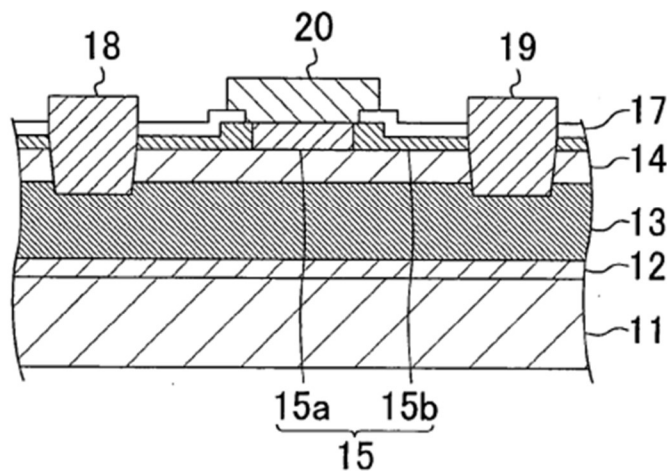
Moreover, to a POSITA, the modification of *Uemoto’s* barrier layer in view of *Smith’s* teachings would also have been a simple substitution of one known element for another. *Id.*, [0230]. The modification would be a simple substitution of a single layer barrier to a multi-layer barrier. *Id.* As *Smith* discloses, these two were interchangeable. *Smith*, [0120]; *Shealy*, [0230].

B. Claim 1

1. [1p]

Uemoto discloses [1p]. *Shealy*, [0231]. *Uemoto* specifies its invention relates to “nitride semiconductor transistors” and discloses transistors made with “III Nitride materials.” *Uemoto*, [0005], [0031]-[0032]. In the figures, such as Figure 7, *Uemoto* illustrates cross-sectional schematics of the transistors.

FIG. 7

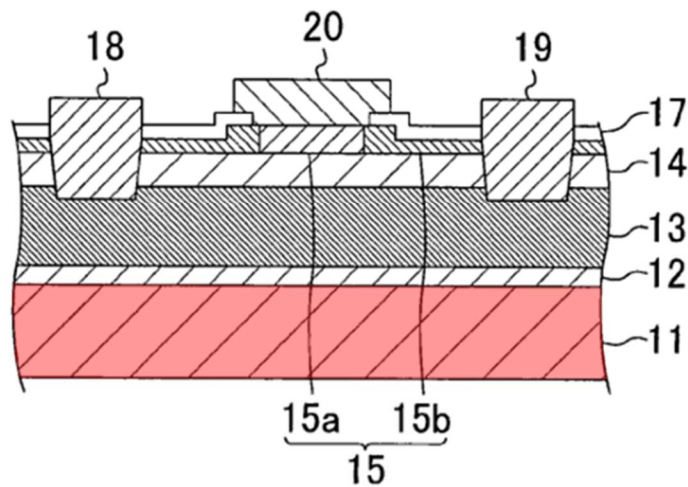


Uemoto, Fig. 7.

2. [1a]

Uemoto discloses [1a]. *Shealy*, [0232]. *Uemoto* discloses “a **substrate 11** [that] is made of silicon,” like the '294 patent. *Compare Uemoto*, [0031] (“substrate 11 is made of silicon”); *with '294 patent*, 2:57-59 (“substrate 31 ... may comprise, for example, silicon”).

FIG. 7

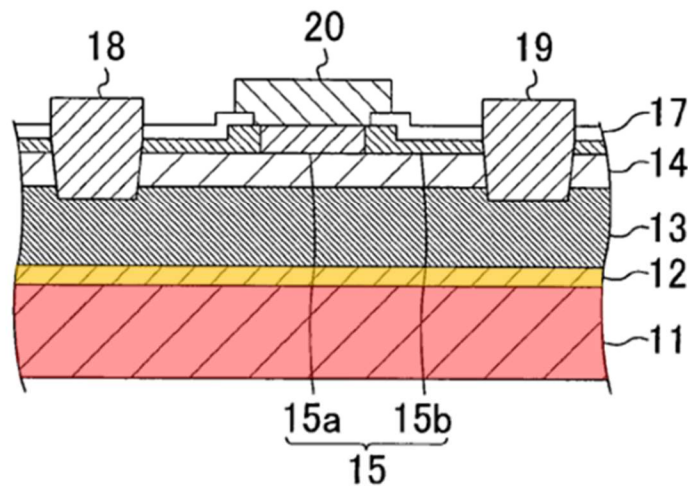


Uemoto, Fig. 7.

3. [1b]

Uemoto, alone or in combination with *Smith*, renders obvious [1b] by describing a “**buffer layer 12** of AlN having a thickness of 100 nm is formed on the principal plane of the **substrate 11**.” *Shealy*, [0233]-[0235]; *Uemoto*, [0031]. *Uemoto*’s “buffer layer 12” is formed with the same materials and thicknesses as the transition layers of the ’294 patent. *Compare Uemoto*, [0031] (describing the buffer layer being AlN), *with* ’294 patent, 2:60-62 (“[t]ransition layers 32 may comprise, for example, AlN”). Despite nomenclature differences, *Smith* discloses the “III-N transition layers” of [1b] by describing the buffer layer. *Adasa* 55 F.4th at 913; *In re Bond*, 910 F.2d at 832-33.

FIG. 7



Uemoto, Fig. 7.

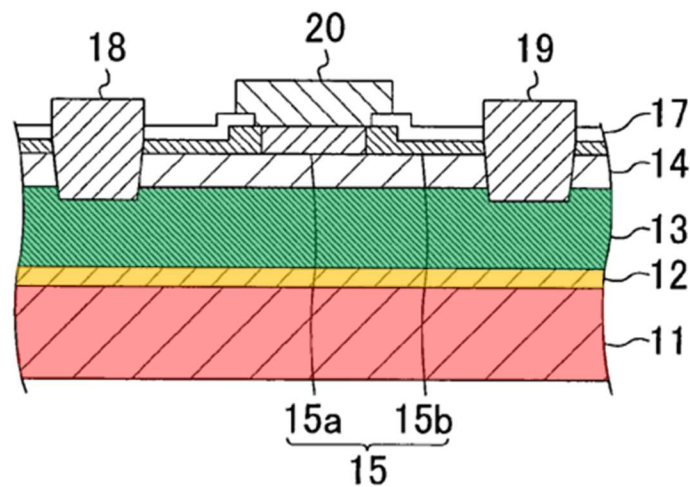
To the extent *Uemoto* does not explicitly disclose [1b] (e.g., disclosing a single **buffer layer**), the combination of *Uemoto* and *Smith* renders [1b] obvious. *Shealy*, [0235]. *Smith* discloses a transistor with “strain balancing **transition layer(s)**.” *Smith*, [0070]; *supra* §VIII.D.3. As discussed above, a POSITA would have found it obvious to incorporate *Smith*’s multiple transition layers in *Uemoto*’s device, rendering [1b] obvious. *Shealy*, [0235]; *supra* §VIII.A.1.

4. [1c]

Uemoto discloses [1c] by disclosing “[a] first nitride **semiconductor layer 13** ... formed on the **buffer layer 12**.” *Uemoto*, [0032]; *Shealy*, [0236]-[0238]. *Uemoto*’s layer 13 is formed with “undoped GaN having a thickness of 2 μm .” *Id.* This is the same material and thickness the ’294 patent associates with a “buffer layer.” ’294 patent, 2:62-66 (“[B]uffer layer 33 is preferably formed of InAlGaN

with any concentration of In and Al (including 0% In and/or Al) and has a thickness between 0.5 and 3 μm .”).

FIG. 7

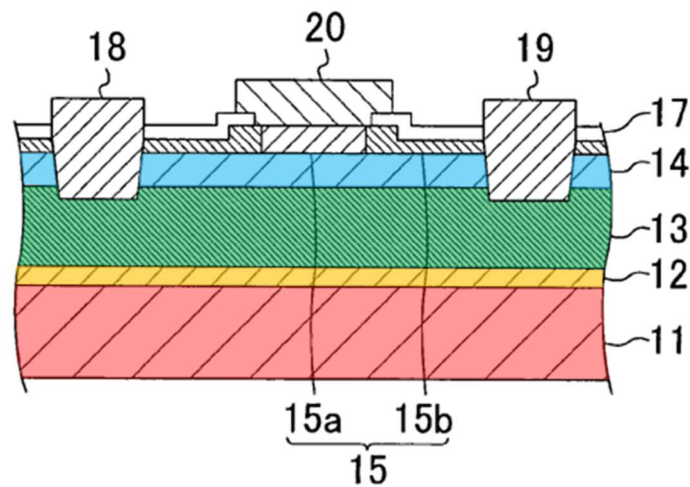


Uemoto, Fig. 7.

5. [1d]

Uemoto discloses [1d] by disclosing “a second nitride **semiconductor layer 14**” formed above the first nitride **semiconductor layer 13**. *Uemoto*, [0032]; *Shealy*, [0239]-[0240]. *Uemoto*’s layer 14 is formed with “ $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ ” (*Uemoto*, [0032]), the same material the ’294 patent discloses for “barrier layer.” ’294 patent, 2:66-3:1 (“[B]arrier layer 34 is formed of AlGaN”).

FIG. 7



Uemoto, Fig. 7.

6. [1e]

Uemoto discloses [1e] under both parties' constructions by disclosing "a high resistive region 15b in which Mg is not activated." *Uemoto*, [0033]; *Shealy*, [0241]-[0247].

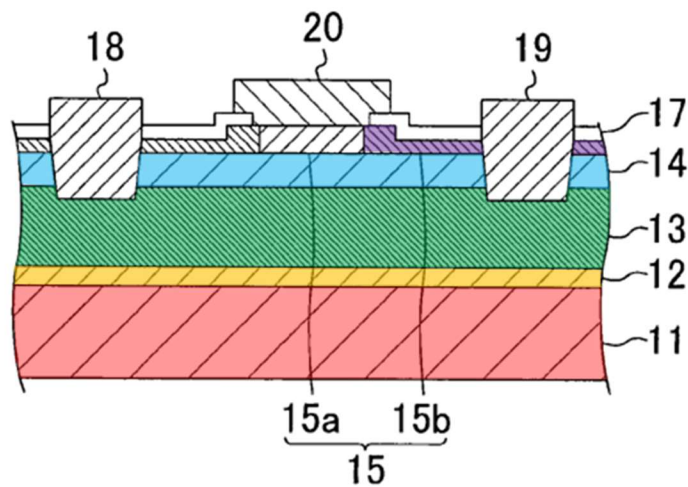
Uemoto discloses that a third nitride semiconductor layer 15 is formed "[o]n the second nitride **semiconductor layer 14**." *Uemoto*, [0033]. *Uemoto* teaches layer 15 can be made of GaN. *Id.*, [0054] ("third nitride semiconductor layer may be made of GaN"), Claim 10. *Uemoto*'s layer 15, therefore, discloses the "GaN layer above the barrier layer" of [1e]. *Shealy*, [0242].

Uemoto additionally discloses that layer 15 is processed to include "a control region 15 a in which Mg is activated to exhibit a p-type conductivity; and a high resistive region 15 b in which Mg is not activated to offer a higher resistance." *Id.*,

[0033], [0063]. *Uemoto* explains that the difference in resistivity within layer 15 can be achieved using a diffusion film so that hydrogen “is supplied during a thermal treatment for selectively inactivating impurities.” *Id.*, [0063], [0049] (“Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom”). *Uemoto*, thus, teaches region 15b is “a compensated GaN layer” under both parties’ proposed constructions. *Uemoto* discloses region 15b is doped with magnesium inactivated through a hydrogen diffusion process and, thus, *Uemoto*’s resistive region 15b discloses a “doped GaN layer formed with a step to passivate its impurities,” the Petitioner’s construction. *ITC Constructions*, 9; *Shealy*, [0244]-[0245]. Additionally, because *Uemoto*’s layer 15 is a GaN material with diffused hydrogen and magnesium dopants (where the hydrogen inactivates the magnesium), *Uemoto*’s layer 15 is also “semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor),” Patent Owner’s construction. *ITC Constructions*, 1; *Shealy*, [0246].

Figure 7 shows *Uemoto*’s high resistive **region 15b** above the **semiconductor layer 14**. *Shealy*, [0247].

FIG. 7



Uemoto, Fig. 7.

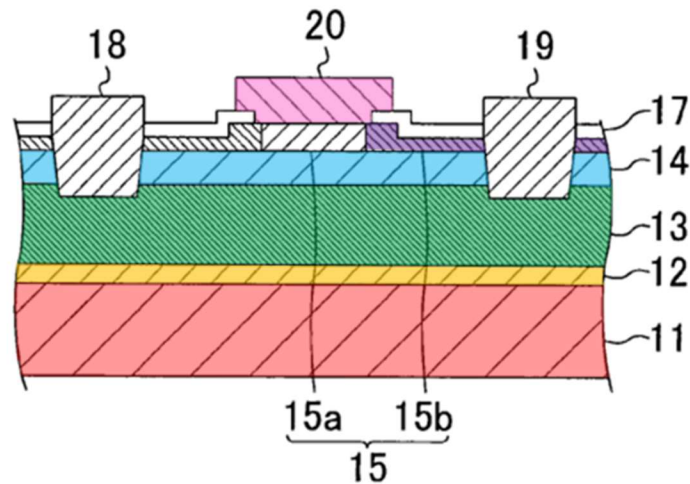
7. [1f]

Uemoto discloses [1f]. *Shealy*, [0248]-[0251]. *Uemoto*'s transistor comprises a "gate electrode 20." *Uemoto*, [0034]. Like the '294 patent, *Uemoto* discloses the gate electrode can be made of different conductors. *Uemoto*, [0056]; '294 patent, 3:4-7. Further, *Uemoto* discloses the gate electrode 20 is above⁵ resistive region 15b.

⁵ Under its plain and ordinary meaning, "above" does not require contact or alignment, only to be over or higher. See *EMI Grp. N. Am., Inc. v. Cypress Semiconductor Corp.*, 68 F. Supp. 2d 421, 431 (D. Del. 1999) (construing "above" as "higher than, but not necessarily directly in contact with"); *Whirlpool Corp. v. LG Elecs., Inc.*, No. 1:04-CV-100, 2005 WL 2990187, at *6 (W.D. Mich. Nov. 8, 2005)

Shealy, [0249]. *Uemoto* specifies gate electrode 20 is formed on the diffusion film. *Uemoto*, [0034] (specifying the gate electrode is formed “[o]n the hydrogen diffusion barrier film”), [0062]. As shown below, this process places **gate electrode 20** above **region 15b**.

FIG. 7



Uemoto, Fig. 7.

To the extent is argued *Uemoto*’s **gate electrode 20** is not “above” **region 15b**, it would have been obvious to increase the overlap between **region 15b** and **gate electrode 20**. For example, a POSITA would have been motivated, and found it obvious, to adjust the width or proportion of **gate electrode 20** as a mere

(construing “above” as “over”); *Terlep v. Brinkman Corp.*, No. 02-CV-5127, 2004 U.S. Dist. LEXIS 28453, at *12 (W.D. Ark. Mar. 23, 2004) (construing “above” as “in a higher place than or overhead”).

change in size or proportion. *Id.*, [0250]. *Uemoto* explains that **gate electrode 20** should be made to “cover the opening” in the diffusion layer and to “come[] into ohmic contact with the control region 15a.” *Uemoto*, [0034]. A POSITA would have recognized that **gate electrode 20** would have been more easily aligned with the opening during transistor fabrication if **gate electrode 20** was wider; so that **gate electrode 20** would be more easily placed fully covering the opening. *Shealy*, [0250]. A POSITA would have recognized that such optimization increases the overlap between **gate electrode 20** above **region 14b**, further placing **gate electrode 20** over **region 15b**. *Id.*

Uemoto, therefore, discloses the “gate contact above the compensated GaN layer” of [1f] by disclosing **gate electrode 20** being above **region 15b**. To the extent it is argued **gate electrode 20** is not above **region 15b**, which Petitioner does not concede, a POSITA would have found it obvious to adjust dimensions in *Uemoto*’s transistors to increase the overlap between **gate electrode 20** and **region 15b**, further placing **gate electrode 20** over **region 15b**. *Shealy*, [0251]

C. Claim 2

Uemoto discloses claim 2. *Id.*, [0252]. *Uemoto* discloses layer 15 is doped with magnesium, an acceptor type dopant. *Uemoto*, [0046] (“the third nitride semiconductor layer 15 of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ is grown with Mg doped as a p-type impurity”). *Uemoto* also discloses that in layer 15 (specifically in **region 15b**)

hydrogen passivates the magnesium, explaining that “hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment for selectively inactivating impurities.” *Id.*, [0063].

D. Claim 3

Uemoto discloses claim 3 by disclosing the acceptor type dopant is magnesium. *Shealy*, [0253]; *Uemoto*, [0033] (“layer 15 is ... doped with magnesium”).

E. Claim 4

1. [4p]

[4p] is identical to [1p]. *Uemoto* discloses [4p] for the same reasons. *Supra* §IX.B.1; *Shealy*, [0254].

2. [4a]

[4a] is identical to [1a]. *Uemoto* discloses [4a] for the same reasons. *Supra* §IX.B.2; *Shealy*, [0255].

3. [4b]

[4b] is identical to [1b]. *Uemoto* discloses [4b] for the same reasons. *Supra* §IX.B.3; *Shealy*, [0256].

4. [4c]

[4c] is identical to [1c]. *Uemoto* discloses [4c] for the same reasons. *Supra* §IX.B.4; *Shealy*, [0257].

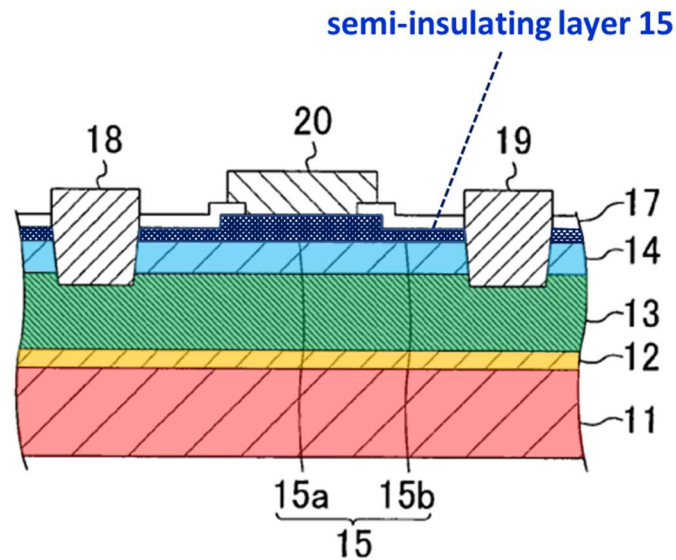
5. [4d]

[4d] is substantially similar to [1d]. *Supra* §IX.B.5. The primary difference is that [4d] does not require the barrier layer to be “above the buffer layer.” *Shealy*, [0258]. Because element [4d] is broader than [1d], *Uemoto* discloses [4d] for the same reasons as [1d]. *Id.*

6. [4e]

Uemoto in view of *Smith* renders obvious [4e]. *Shealy*, [0259]-[0260]. *Uemoto* discloses a “III-N layer above the barrier layer” by disclosing a third nitride semiconductor layer 15 formed on **second nitride semiconductor layer 14** (the barrier). *Uemoto*, [0033]; *supra* §IX.B.6. *Uemoto*, however, does not explicitly disclose layer 15 being “semi-insulating.” But *Smith* does. *Smith* discloses embodiments with a **semi-insulating cap layer 34** above **barrier layer 22**. *Smith*, [0085] (disclosing cap layer 34 being formed as a “semi-insulating III-N layer”); *supra* §VIII.G.6. As explained above, a POSITA would have been motivated to apply *Smith*’s disclosure of forming semi-insulating layers with deep level dopants to *Uemoto*. *Supra* §IX.A.2. Modified Figure 7 below shows *Uemoto*’s layer 15 being formed as a **semi-insulating layer 15** (as taught in *Smith*) and above **semiconductor layer 14**.

FIG. 7



Uemoto, Fig. 7 (modified).

F. Claim 5

Uemoto in view of *Smith* renders obvious claim 5. *Shealy*, [0261]-[0262]. A POSITA would have been motivated and found it obvious to incorporate *Smith*'s semi-insulating layer (e.g., with deep level dopants or co-doping techniques) and turn *Uemoto*'s layer 15 into a **semi-insulating layer 15**. *Supra* §IX.E.6. *Smith* also specifies doping "with deep level dopants" and discloses doping being performed with deep acceptor type dopants. *Id.* §VIII.H; *Smith*, [0089]; *Shealy*, [0261]-[0262].

G. Claim 6

Uemoto in view of *Smith* renders obvious claim 6. *Shealy*, [0263]-[0264]. A POSITA would have been motivated and found it obvious to incorporate *Smith*'s deep level dopants or co-doping techniques to form a **semi-insulating layer 15** in

Uemoto. Supra §IX.E.6. *Smith* specifies “[t]he deep level dopants may be Fe, C, V, Cr, Mn, Ni, Co or other rare earth elements.” *Smith*, [0089]; *supra* §VIII.I

H. Claim 7

1. [7p]

[7p] is identical to [1p]. *Uemoto* discloses [7p] for the same reasons. *Supra* §IX.B.1; *Shealy*, [0265]-[0266]

2. [7a]

[7a] is identical to [1a]. *Uemoto* discloses [7a] for the same reasons. *Supra* §IX.B.2; *Shealy*, [0267].

3. [7b]

[7b] is identical to [1b]. *Uemoto* discloses [7b] for the same reasons. *Supra* §IX.B.3; *Shealy*, [0268].

4. [7c]

[7c] is identical to [1c]. *Uemoto* discloses [7c] for the same reasons as [1c]. *Supra* §IX.B.4; *Shealy*, [0269].

5. [7d]

[7d] is identical to [4d]. *Uemoto* discloses [7d] for the same reasons. *Supra* §IX.E.5; *Shealy*, [0270].

6. [7e]

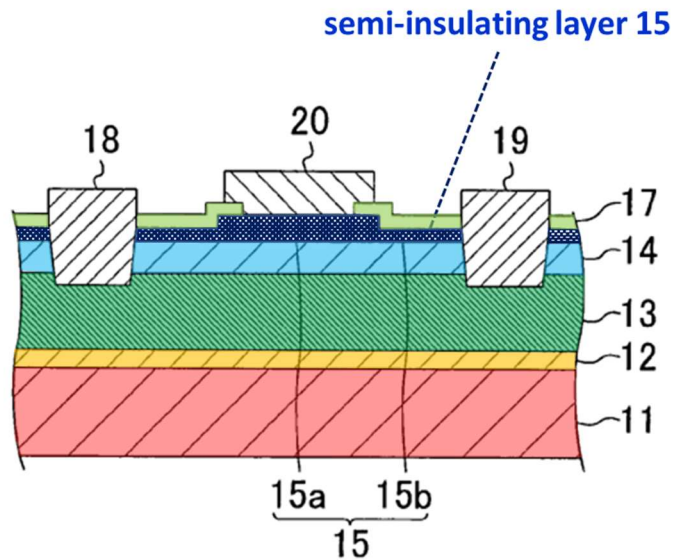
[7e] is identical to [4e]. *Uemoto* discloses [7e] for the same reasons. *Supra* §IX.E.6; *Shealy*, [0271].

7. [7f]

Uemoto in view of *Smith* renders obvious [7f]. *Shealy*, [0272]-[0274]. *Uemoto* discloses forming a hydrogen diffusion film 17 on top of the third nitride semiconductor layer 15. *Uemoto*, [0063]. *Uemoto* discloses a hydrogen diffusion film 17 is “made of silicon nitride.” *Id.* Silicon nitride is the same material the ’294 patent associates with the “confinement layer.” *Shealy*, [0272]; ’294 patent, 4:34-35 (describing the confinement layer can be composed of “SiN”). Despite nomenclature differences, *Uemoto* discloses the “confinement layer” of [7f] by describing the “hydrogen diffusion film 17.” *Shealy*, [0272]; *Adasa*, 55 F.4th at 913; *In re Bond*, 910 F.2d at 832-33.

Because a POSITA would have been motivated to combine *Uemoto* and *Smith*, and to a POSITA it would have been obvious to make *Uemoto*’s layer 15 semi-insulating, forming a **semi-insulating layer 15** (*supra* §§IX.A.2, IX.E.6), the combination of *Uemoto* and *Smith* discloses the **hydrogen diffusion film 17** being above the **semi-insulating layer 15**. *Shealy*, [0273]-[0274].

FIG. 7



Uemoto, Fig. 7 (modified).

I. Claim 8

Claim 8 is substantially similar to claim 6. *Supra* §VIII.K *Uemoto* in combination with *Smith* renders obvious claim 8 for the same reasons. *Shealy*, [0275]; *Supra* §IX.G.

J. Claim 9

Uemoto discloses claim 9. *Shealy*, [0276]. *Uemoto* specifies **hydrogen diffusion film 17** is made of silicon nitride. *Uemoto*, [0063]. Silicon nitride is one of the materials recited in claim 9 for the confinement layer. *Shealy*, [0276].

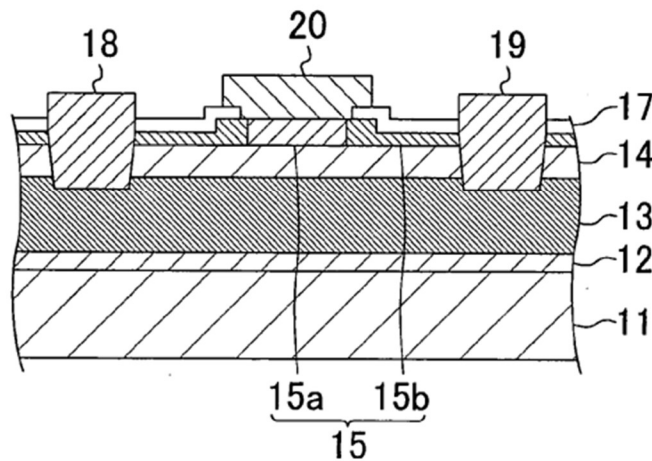
K. Claim 10

1. [10p]

Uemoto discloses or renders obvious [10p]. *Shealy*, [0277]. *Uemoto* discloses various GaN transistors, which the '294 patent identifies as "MISFET." '294 patent,

Abstract (“[a] MISFET, such as a GaN transistor”); *Shealy*, [0277]. *Uemoto* also discloses transistors including MIS layers by disclosing, for example, a metal gate electrode, over an insulating diffusion film, over the third nitride semiconductor. *Uemoto*, [0034], [0063]. And *Uemoto* discloses transistors with “compensated” gates. *Supra* §IX.B.6; *Shealy*, [0277].

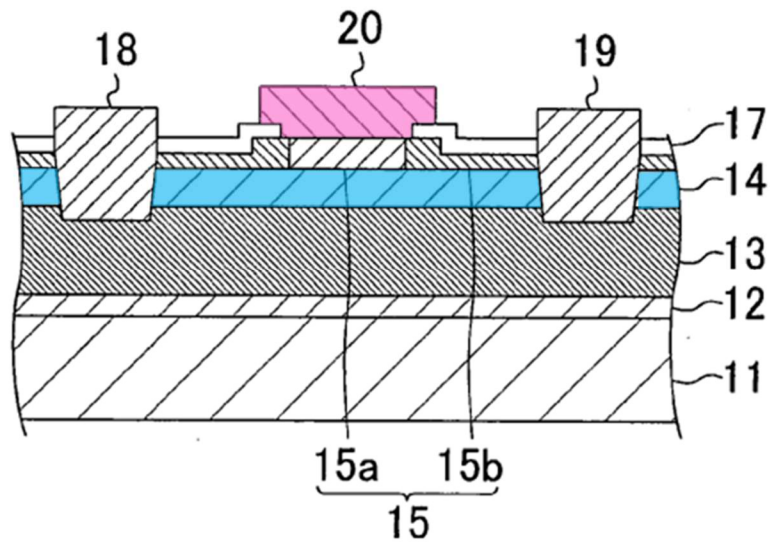
FIG. 7



Uemoto, Fig. 7.

2. [10a]

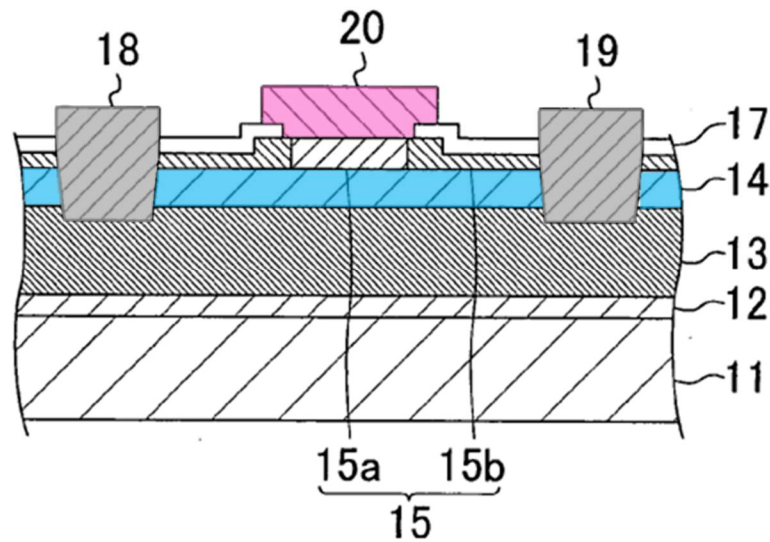
[10a] is substantially similar to [1d]. *Supra* §IX.B.5. The primary difference is that in [10a] the barrier layer is “beneath a gate contact,” instead of being “above the buffer layer.” *Shealy*, [0278]-[0279]. *Uemoto*, however, also discloses **second nitride semiconductor layer 14**, which discloses a barrier (*supra* §IX.B.5), being beneath **gate contact 22**.



Uemoto, Fig. 7.

3. [10b]

Uemoto discloses [10b]. *Shealy*, [0280]-[0281]. *Uemoto* discloses “a source electrode 18 and a drain electrode 19.” *Uemoto*, [0035]. *Uemoto* also discloses that the “**source electrode 18** and the **drain electrode 19** are each made of titanium (Ti) and aluminum (Al).” *Id.*

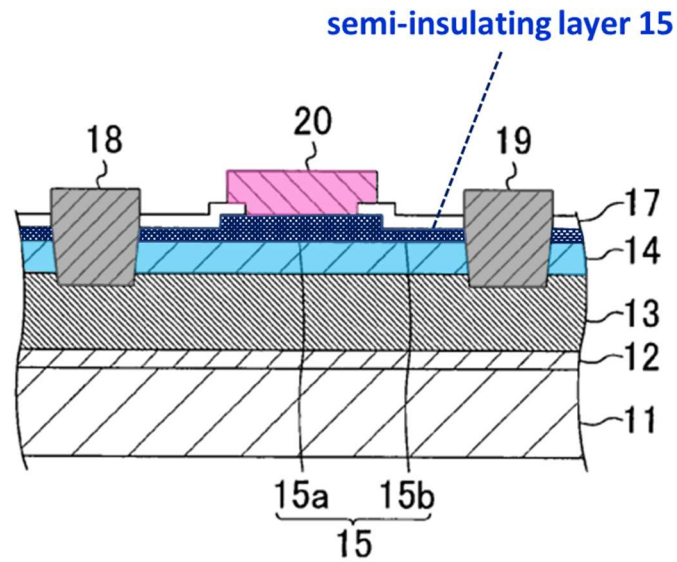


Uemoto, Fig. 7.

4. [10c]

[10c] is substantially similar to [4e]. *Supra* §IX.E.6. The difference is that in [10c] the semi-insulating layer is “between the barrier layer and the gate contact,” instead of being “above the barrier layer.” *Shealy*, [0282]-[0284]. *Uemoto*, however, discloses layer 15 being between **second nitride semiconductor layer 14** and **gate contact 22**. *Id.*; *Uemoto*, [0033]-[0034]. Because a POSITA would have found it obvious to make *Uemoto*’s layer 15 semi-insulating based on *Smith*, thus forming a **semi-insulating layer 15** (*supra* §§IX.A.2, IX.E.6), the *Uemoto/Smith* combination discloses [10c].

FIG. 7

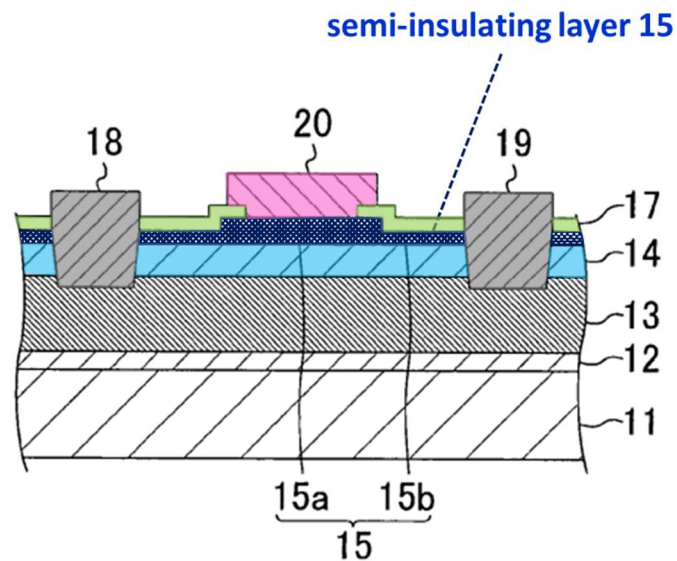


Uemoto, Fig. 7 (modified).

L. Claim 11

Claim 11's feature is identical to [7f]. *Uemoto* discloses claim 11 for the same reasons. *Supra* §IX.H.7. Annotated Figure 7 shows *Uemoto*'s hydrogen diffusion film 17 above the semi-insulating layer 15. *Shealy*, [0285].

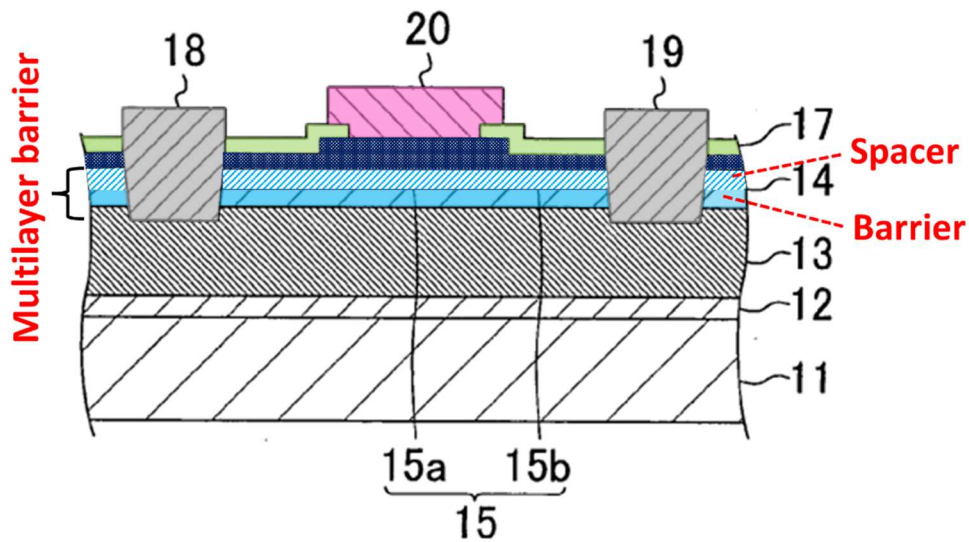
FIG. 7



Uemoto, Fig. 7 (modified).

M. Claim 12

Uemoto in view of *Smith* renders obvious claim 12. *Shealy*, [0286]-[0288]. Although *Uemoto* does not explicitly disclose the claimed “spacer layer,” *Smith* does. *Supra* §VIII.O. *Smith* discloses fabrication of transistors “with barrier/spacer layer” and discloses embodiments in which the barrier layer is “provided with multiple layers.” *Id.*; *Smith*, [0075], [0120]. *Smith*’s disclosure of the “barrier/spacer” and the multilayer barrier discloses a spacer layer. *Supra* §VIII.O. A POSITA would have been motivated to modify *Uemoto*’s layer 14 to a multilayer barrier, including a “barrier/spacer,” as taught by *Smith*. *Id.*, §IX.A.3. A POSITA would have found it obvious and been motivated to perform such a modification to improve *Uemoto*’s device performance by “reduc[ing] or prevent alloy scattering,” as disclosed in *Smith*. *Uemoto*’s Figure 7 below is modified to depict the incorporation of *Smith*’s semi-insulating doping and spacer layer. *Shealy* [0287]-[0288]; *Smith*, [0120]; *supra* §IX.A.3.



Uemoto, Fig. 7 (modified).

X. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *Fintiv* Denial Is Improper

In view of the Office’s interim guidance dated June 21, 2022 (“*Interim Procedures*”), *Fintiv* does not apply here. The Interim Procedures state “the PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding,” so the parallel ITC Investigation does not implicate *Fintiv*. *Interim Procedures*, 7.

Moreover, the *Fintiv* factors in view of the parallel district court action weigh strongly in favor of institution because the district court case has minimal investment from the Court or Parties, does not have a trial date, and has been stayed. *Efficient Power Conversion Corp. v. Innoscience (Zhuhai) Tech. Co.*, No. 2:23-cv-04026, Dkt. 26 (C.D. Cal. July 27, 2023).

B. 35 U.S.C. § 325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017), favor institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-11 (PTAB Feb. 13, 2020) (precedential).

Advanced Bionics, step 1, and *Becton, Dickinson* factors (a), (b), and (d) favor institution because none of the references in this Petition were before the Office during prosecution. *See Prosecution History*; '294 patent, Cover. The references are also not cumulative of the prosecution prior art, at least because they teach “forming a ‘compensated GaN layer above [a] barrier layer,’” which applicants argued was not present in the examined art (*Prosecution History*, 106), and they disclose “a compensated GaN layer above the barrier layer,” which Examiner identified as part of the reasons for allowance (*id.*, 149). The references are also not cumulative because they disclose the intentional incorporation of hydrogen in GaN layers and the use of semi-insulating cap layers, which are not disclosed in the prosecution prior art. *Shealy*, [0089].

XI. MANDATORY NOTICES

A. Real Parties-in-Interest

The real parties-in-interest are Innoscience (Zhuhai) Technology Company, Ltd., Innoscience America, Inc., and Innoscience (Suzhou) Technology Company, Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '294 patent is involved in:

Name	Number	Court	Filed
<i>Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd.; Innoscience, Inc.; Innoscience America, Inc.</i>	2:23-cv-04026-AB-AS	C.D. Cal.	May 24, 2023
<i>In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same</i>	337-TA-1366	ITC	May 26, 2023

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Petitioner consents to electronic service at the following email address
Innoscence-EPC-IPRs@finnegan.com.

XII. STANDING

The '294 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR.

XIII. CONCLUSION

Petitioner requests institution of *inter partes* review and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 11, 2023

/Lionel M. Lavenue/

Lionel M. Lavenue
Reg. No. 46,859

CLAIM APPENDIX

1. **[1p]** A column III Nitride transistor comprising:
 - [1a]** a substrate,
 - [1b]** a set of III-N transition layers above the substrate,
 - [1c]** a III-N buffer layer above the set of transition layers,
 - [1d]** a III-N barrier layer above the buffer layer,
 - [1e]** a compensated GaN layer above the barrier layer, and
 - [1f]** a gate contact above the compensated GaN layer.
2. The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
3. The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.
4. **[4p]** A column III Nitride transistor comprising:
 - [4a]** a substrate,
 - [4b]** a set of III-N transition layers above the substrate,
 - [4c]** a III-N buffer layer above the set of transition layers,
 - [4d]** a III-N barrier layer, and
 - [4e]** a semi-insulating III-N layer above the barrier layer.
5. The transistor of claim 4, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms.

6. The transistor of claim 5 where the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.
7. **[7p]** A column III Nitride transistor comprising:
 - [7a]** a substrate,
 - [7b]** a set of III-N transition layers above the substrate,
 - [7c]** a III-N buffer layer above the set of transition layers,
 - [7d]** a III-N barrier layer,
 - [7e]** a semi-insulating III-N layer above the barrier layer, and
 - [7f]** a confinement layer above the semi-insulating III-N layer.
8. The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.
9. The transistor of claim 7, wherein the confinement layer is made of SiN, SiO₂, Al₂O₃, HfO₂, Ga₂O₃, or InAlGa₂N.
10. **[10p]** A compensated gate MISFET transistor comprising:
 - [10a]** a III-N barrier layer beneath a gate contact,
 - [10b]** a drain contact, a source contact, and
 - [10c]** a semi-insulating III-N layer between the barrier layer and the gate contact.

11. The transistor of claim 10, further comprising a confinement layer above the semi-insulating III-N layer.
12. The transistor of claim 10, further comprising a spacer layer between the semi-insulating layer and the barrier layer.

37 C.F.R. § 42.24(D) CERTIFICATION

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), Petitioner certifies that this petition complies with the requirements of 37 C.F.R. § 42.24. Excluding parts of this Petition exempted under § 42.24(a), this Petition contains 13,687 words, as measured by the word-processing system used to prepare this paper.

Dated: September 11, 2023

By: Lionel M. Lavenue/

Lionel M. Lavenue

Reg. No. 46,859

CERTIFICATE OF SERVICE

The undersigned certifies that a copy of this Petition for *Inter Partes* Review of U.S. Patent 8,350,294, the Powers of Attorney, and Exhibits 1001 through 1024, were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's Patent Center website for the '294 patent:

Dipu Doshi
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1825 Eye Street, NW
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Date: September 11, 2023

By: /Lisa C. Hines/
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