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APPLICATION NUMBER: 12/756,906

FILING DATE: *April 08, 2010*

PATENT NUMBER: 8350294

ISSUE DATE: *January 08, 2013*



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	Not Yet Assigned
				Filing Date	April 8, 2010
				First Named Inventor	Alexander Lidow
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	E0101.0008/P008

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2006/0273347	12-07-2006	Hikita et al.	

FOREIGN PATENT DOCUMENTS						
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		X. Hu, et al. "Enhancement Mode AlGaIn/GaN HFET With Selectively Grown pn Junction Gate", <i>Electronics Letters</i> , Vol 35, No. 8, pp. 753-754, April 13, 2000	
		T. Fuji et al. "High On/Off Ratio in Enhancement-Mode AlxGa1-xN/GaN Junction Heterostructure Field-Effect Transistors with P-Type GaN Gate Contact", <i>Japanese Journal of Applied Physics</i> , Vol. 45, No. 39, pp. L1048-L1050, 2006	
		Y. Uemoto et al. "Gate Injection Transistor (GIT) - A Normally-Off AlGaIn/GaN Power Transistor Using Conductivity Modulation, <i>IEEE Transactions on Electron Devices</i> , Vol. 54, No. 12, pp. 3393-3399, December 2007	

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$$TLR = \frac{\frac{1}{2} \sigma_n^2}{P_{local}} \quad (1)$$

The value of TLR must be chosen such that it minimises the BER.

Simulation results: In the simulation, the spreading gain N was set to 128. The spreading code was chosen to be a Walsh-Hadamard code with length 128. All the users were assumed to suffer from independent Rayleigh fading. It was also assumed that the fading were independent among the different subcarriers. The signal to noise ratio (SNR) was defined throughout the simulation as $SNR = P_{local}/\sigma_n^2$, where σ_n^2 is the additive white Gaussian noise (AWGN) noise power.

Fig. 3 shows the optimal value of TLR required to minimise the BER performance of a 10-user system at a particular SNR value. As expected, the optimal TLR value decreases while the SNR increases. If we consider the situation where the signal power P_{local} is constant, the TLR should be higher, when the SNR is small, to effectively eliminate deep fading or noise contaminated subcarriers. On the other hand, when the SNR is large, the optimal value of TLR will be small since the noise or fading level is not high. It is observed that the optimal TLR changes from -0.3 to -0.5 dB as the SNR varies from 1 to 15 dB.

A BER performance comparison is shown in Fig. 4. It is obvious that the suggested controlled MRC algorithm with power control outperforms the MRC algorithm. Here the optimal threshold was used in the simulation for the controlled MRC with power control algorithm. The improvement is about five users for $BER = 10^{-3}$. However, for larger SNR values, the improvement is not as high. This can be explained as follows. When the noise level is low or no deep fading signal is present, then few or no subcarriers will be cut off, therefore the difference between controlled MRC and MRC will be insignificant.

Conclusion: A controlled MRC algorithm has been proposed for an MC-CDMA uplink system under Rayleigh fading channel and AWGN conditions. The optimal threshold value for such an algorithm has been obtained by simulation for various SNR values. It has been shown that the controlled MRC algorithm can improve the MC-CDMA uplink performance, especially in low SNR environments. However, when the SNR is high, the proposed method does not lead to noticeable improvements.

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Electronics Letters Online No: 20000549
DOI: 10.1049/el:20000549

15 February 2000

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References

1. HARA, S., and PRASAD, R.: 'Overview multicarrier CDMA', *IEEE Commun. Mag.*, December 1997, pp. 126-133
2. YEE, J.-P., and LINNARTZ, N.: 'Multi-carrier CDMA in an indoor wireless radio channel'. Internal Report, University of California at Berkeley, 1993

Enhancement mode AlGaIn/GaN HFET with selectively grown pn junction gate

X. Hu, G. Simin, J. Yang, M. Asif Khan, R. Gaska and M.S. Shur

A report is presented into the fabrication and characterisation of an enhancement mode AlGaIn/GaN heterojunction field-effect transistor (HFET) with selectively grown pn junction gate. At zero gate bias the device channel is depleted due to the high built-in potential of the gate-channel junction. The selective area growth approach enables both depletion and enhancement mode HFETs to be fabricated on the same wafer thus opening up the possibility of designing high speed, low consumption GaN-based logical integrated circuits.

Since the first demonstration of a depletion mode AlGaIn/GaN high electron mobility transistor (HEMT) [1], there has been rapid progress towards the realisation of high power microwave devices [2, 3]. However to date few reports have been made of AlGaIn/GaN based enhancement mode transistors. Khan *et al.* reported such a device using AlGaIn/GaN heterojunctions where a Schottky barrier gate was used [4]. For high temperature digital IC applications it is ideal to fabricate both enhancement and depletion mode (AlGaIn/GaN) devices in selective areas on the same wafer. In this Letter we describe a novel approach to realising an enhancement mode AlGaIn/GaN heterostructure field effect transistor (HFET) with a selective area grown pn junction gate. The p -GaIn layers for the gate were grown in selective areas defined by openings in an SiO_2 mask. Our novel approach therefore opens up the possibility of monolithically integrating AlGaIn/GaN based normally-on and normally-off logic devices on a single wafer.

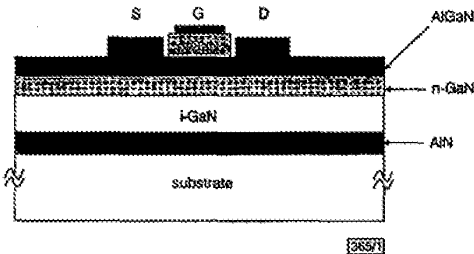


Fig. 1 Schematic diagram of structure of pn junction regrown gate HFET

The epilayer structure for our devices is schematically shown in Fig. 1. It was deposited over a basal plane sapphire substrate using low pressure metal organic chemical vapour deposition (MOCVD) epitaxy. The 300 Å AlN buffer layer of our structure was deposited at 400°C and 76 torr. All the other layers were deposited at 1000°C and 76 torr. The $Al_{0.2}Ga_{0.8}N$ barrier layer was 300 Å thick and was silicon-doped to $N = 3 \times 10^{18} \text{ cm}^{-3}$. All layers of the structure were grown with a low-level flux of trimethylindium (TMI). This incorporates trace amount of In in all the layers and helps with the layer and interface smoothness. For the structure, the room temperature sheet carrier density and mobility were measured to be $n_s = 8 \times 10^{12} \text{ cm}^{-2}$ and $\mu = 1000 \text{ cm}^2/\text{Vs}$.

Mg-doped 1000 Å thick p -GaIn ($p = 10^{17} \text{ cm}^{-3}$) was then selectively grown using $10 \mu\text{m} \times 150 \mu\text{m}$ openings in a 1000 Å thick SiO_2 masking layer. The SiO_2 mask layer was deposited using a plasma enhanced chemical vapour deposition (PECVD) system. Transistors were then fabricated with Ti/Au/Ti/Au (100 Å/200 Å/100 Å/500 Å) source-drain contacts. The contacts were then RTA annealed at 850°C for 1 min in a nitrogen ambient. Ni/Au contacts were then deposited over the selective area grown p -GaIn regions. These were annealed at 450°C in oxygen ambient. Our transistor structure thus had a gate length of $10 \mu\text{m}$ and a gate width of $150 \mu\text{m}$. The source drain opening was $10 \mu\text{m}$. Note that this geometry was selected only for a proof of principle. For higher performance devices much shorter gate lengths and source drain distances will be required.

In Fig. 2a we include the source drain current-voltage characteristics. As seen at zero gate bias the device does not conduct because the channel is depleted due to the high built-in voltage of the pn junction gate. With positive gate voltage the device reaches a saturation current of 40 mA/mm at +4 V gate bias. Fig. 2b shows the external transconductance g_m as a function of gate bias measured at 25 V drain to source voltage. The peak g_m value of 10 mS/mm is reached at +3 V gate bias. These I_d and g_m values are limited by the low channel conductance from the very large gate and channel length ($10 \mu\text{m}$). Assuming an inverse linear dependence of both saturation current and transconductance on the gate length, we estimate these values to be 400 mA/mm and 150 mS/mm, respectively, for a $1 \mu\text{m}$ -gate device. These estimated values of I_d and g_m are quite close to those typically reported for depletion mode devices.

The maximum current for heterostructure field-effect transistors depends on the maximum charge induced in the device channel.

This charge increases with the increase in positive gate bias (for an n -channel device). Thus the maximum saturation current is limited by the gate leakage at positive bias. For our enhancement mode transistor with a pn junction gate, the range of positive gate bias which maintains a low gate leakage current is significantly larger than that for a regular Schottky-gate device. This is illustrated by Fig. 3 showing gate channel I-V curves for a pn junction gate enhancement mode HFET and a regular Schottky gate HFET on the same wafer. As seen, for a pn junction gate device the maximum operating gate voltage can be as high as 3V as compared to ~ 1 V maximum operating voltage for a Schottky gate HFET. This proves that in principle, pn junction gate enhancement mode HFETs can provide much higher induced channel charge, and hence, saturation current and transconductance as compared to a Schottky gate depletion mode HFET.

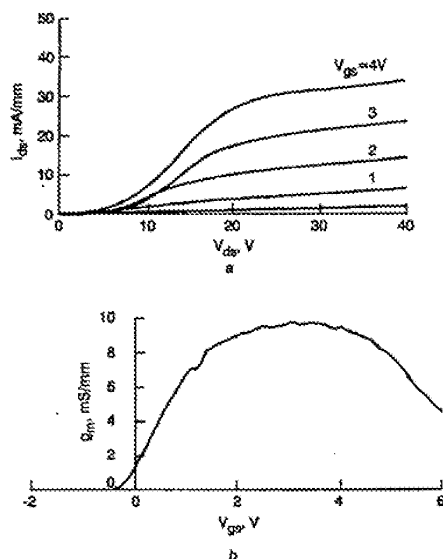


Fig. 2 Current-voltage characteristics of enhancement mode pn junction gate HFET

a Channel current dependence on drain to source voltage
b Transconductance dependence on gate bias

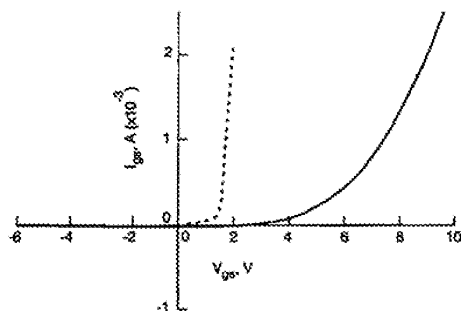


Fig. 3 Current voltage characteristics of pn junction and Schottky gate devices

----- pn junction device
----- Schottky gate device

Our estimates of the threshold voltage as a function of the distance between the channel and the gate showed that the effective channel-to-gate separation is close to the thickness of the AlGaIn layer. This means that the p -type AlGaIn layer operates as a p -type gate. As a result, the threshold voltage is shifted by ~ 2.5 V towards positive values (i.e. by the difference between the GaN energy gap and the Schottky barrier height).

In Fig. 3 it can be seen that the differential resistance of the pn junction gate is ~ 1 k Ω . This resistance is largely due to the relatively low doping level in regrown p -material as well as to the low hole mobility in p -GaN. The pn junction gate capacitance was measured to be < 1 pF. Using these values of gate series resistance and capacitance, we estimate the characteristic time constant RC of our enhancement mode HFET to be < 1 ns. By making use of a higher doping level in the p -GaN gate material and with shorter gate length this time constant can be considerably decreased to achieve switching rates in the gigabit per second range.

In conclusion we have fabricated a new enhancement mode GaN/AlGaIn HEMT with a selective area deposited pn junction gate. We have also established the feasibility of our approach to produce enhancement and depletion mode GaN/AlGaIn HEMTs on the same wafer. This is an important step towards the goal of realising monolithically integrated logic circuits based on AlGaIn/GaN heterojunctions.

Acknowledgment: This work was supported by the Ballistic Missile Defense Organization (BMDO) under Army SSDC contract DASG60-97-C 0066, monitored by B. Strickland and K. Wu. The work at RPI was partially supported by the Office of Naval Research (Program monitor J. Zolper).

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Electronics Letters Online No: 20000557
DOI: 10.1049/el:20000557

21 February 2000

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References

- ASIF KHAN, M., BHATTARAI, A., KUZNETS, I.N., and OLSON, D.T.: 'High electron mobility transistor based on a GaN-Al_{0.3}Ga_{0.7}N heterojunction', *Appl. Phys. Lett.*, 1993, 63, (9), pp. 1214-1215
- SHEPPARD, S.T., DOVERSPIKE, K., PRIBBLE, W.L., ALLEN, S.T., PALMOUR, J.W., KEHIAS, L.T., and JENKINS, T.J.: 'High-power microwave GaN/AlGaIn HEMTs on semi-insulating silicon carbide substrates', *IEEE Electron Device Lett.*, 1999, 20, (4), pp. 161-163
- LI, R., CAI, S.J., WONG, L., CHEN, Y., WANG, K.L., SMITH, R.P., MARTIN, S.C., BOUTROS, K.S., and REDWING, J.M.: 'An Al_{0.3}Ga_{0.7}N/GaN undoped channel heterostructure field effect transistor with f_{max} of 107 GHz', *IEEE Electron Device Lett.*, 1999, 20, (7), pp. 323-325
- ASIF KHAN, M., CHEN, Q., SUN, C.J., YANG, J.W., BLASINGAME, M., SHUR, M.S., and PARK, H.: 'Enhancement and depletion mode GaN/AlGaIn heterostructure field effect transistors', *Appl. Phys. Lett.*, 1996, 68, (4), pp. 514-516

Laser processing for enhanced performance thin film electroluminescent devices

W.M. Cranton, E.A. Mastio, C.B. Thomas, C. Tsakonas and R. Stevens

A technique for enhancing the performance of thin film electroluminescent devices is presented. Thin film phosphors have been processed with 20ns pulses of 880mJ/cm² laser irradiation from a 249nm KrF excimer laser. Electroluminescent characterisation demonstrates a four-fold improvement in emitted luminous intensity, as compared to thermally annealed structures.

Introduction: Thin film electroluminescent (TFEL) devices utilising ZnS:Mn phosphor films are important in the field of large area flat panel displays. These displays have benefits such as ruggedness, low power, high contrast, full colour capability, high temperature operating range, and large viewing angle [1]. They are suitable for both text and graphics based systems and, as demonstrated by the Displays Group at Nottingham Trent University

High On/Off Ratio in Enhancement-Mode $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ Junction Heterostructure Field-Effect Transistors with P-Type GaN Gate Contact

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(Received July 29, 2006; accepted August 20, 2006; published online September 29, 2006)

An excellent on/off ratio of drain-source current (I_{DS}) density over 6 orders of magnitude by changing the gate voltage (V_{G}) from 3 to 0 V was confirmed in p-GaN/u- $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{u-GaN}$ junction heterostructure field-effect transistors. These devices show an extremely low leakage I_{DS} density of as low as 15.5 nA/mm at V_{DS} and V_{G} of 10 and 0 V. On resistance is as low as 2.65 m $\Omega\cdot\text{cm}^2$ at $V_{\text{G}} = 3.0$ V. [DOI: 10.1143/JAP.45.L1048]

KEYWORDS: $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$, JHFET, enhancement mode, leakage current, p-type GaN gate, on/off ratio of drain-source current

$\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure field-effect transistors (HFETs) are attractive for high-temperature, high-power, and high-frequency devices. Large numbers of high-performance $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HFETs have been reported.^{1–5)} Most $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HFETs are operated in the depletion mode or normally on mode, because of the high-density two-dimensional electron gas (2DEG) induced by the polarization field.^{6,7)} From the application viewpoint, enhancement-mode or normally off-mode HFETs are strongly required because of their circuit simplicity and low stand-by-power dissipation. In addition, to realize fail-safe circuit systems, a normally off-mode HFET is essential.

We reported enhancement-mode $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ junction HFETs transistors (JHFETs) using a p-type GaN (p-GaN) gate contact.⁸⁾ In order to achieve high transconductance (g_m) and precise control of the threshold voltage (V_{th}) in JHFETs, it is necessary to control the thickness and alloy composition in the unintentionally doped $\text{Al}_x\text{Ga}_{1-x}\text{N}$ (u- $\text{Al}_x\text{Ga}_{1-x}\text{N}$) layer.⁹⁾ V_{th} is defined by the following well-known expression.

$$V_{\text{th}} = \phi_{\text{B}} - \frac{qN_{\text{D}}d^2}{2\epsilon} - \Delta E_{\text{C}},$$

where ϕ_{B} denotes energy difference between conduction band minimum and Fermi level of p-GaN side of u- $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{p-GaN}$ heterointerface, N_{D} , remaining donor density of u- $\text{Al}_x\text{Ga}_{1-x}\text{N}$, d , thickness of u- $\text{Al}_x\text{Ga}_{1-x}\text{N}$, ϵ , dielectric constant of u- $\text{Al}_x\text{Ga}_{1-x}\text{N}$, ΔE_{C} , discontinuity of conduction band of u- $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{u-GaN}$ heterostructure.

For high-efficiency systems, such as in-vehicle low-loss switching devices, both a low external leakage current in the off state and a high on/off ratio of the drain-source current (I_{DS}) are necessary. In the case of in-vehicle switching devices, the off time is very long, therefore the loss must be low. It is also important that on resistance (R_{on}) should be as low as possible for high switching efficiency. Suppression of the leakage of the drain current at zero gate voltage (V_{G}) is very important for enhancement-mode HFETs. Generally, an HFET using a recess structure can be operated in an enhancement mode with a very thin u- $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier of less than 10 nm.^{10,11)} The leakage current density of I_{DS} at zero V_{G} is at least 20 $\mu\text{A}/\text{mm}$ ($V_{\text{DS}} = 20$ V).¹²⁾ The leakage current at the off state is too large for use in high-efficiency

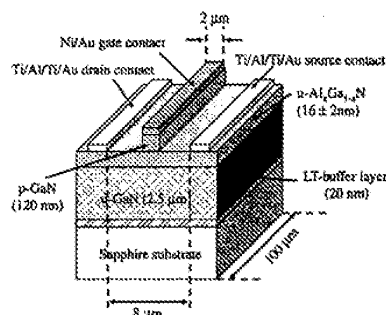


Fig. 1. Schematic diagram of fabricated $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFETs with p-GaN gate contact.

switching devices. In switching devices, a large leakage current leads to a decrease in the on/off ratio. To improve the efficiency of the in-vehicle switching device, a reduction in R_{on} and leakage currents and an increase in the on/off ratio are very important.

In this study, an extremely low leakage of I_{DS} in the off state of enhancement-mode $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFETs with a p-GaN gate contact is reported. An on/off ratio of the I_{DS} density over 6 orders of magnitude between V_{G} of 0 and 3 V is demonstrated.

Figure 1 shows a schematic diagram of the sample structure. All devices were grown by organometallic vapor phase epitaxy on a sapphire (0001) substrate covered with a low-temperature-deposited (LT-) buffer layer.¹³⁾ After depositing the LT-buffer layer (20 nm) at 500 °C, unintentionally doped GaN (u-GaN) 2.5 μm in thickness, u- $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer (16 $\pm$ 2 nm) and a Mg-doped p-GaN layer (120 nm) with a Mg concentration of $3 \times 10^{19} \text{ cm}^{-3}$ were grown at 1,100 °C. The hole concentration in the p-GaN layer was $1 \times 10^{18} \text{ cm}^{-3}$ at room temperature. Table I shows a summary of the device parameters, i.e., AlN molar fraction x and the thickness of the u- $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer for samples A–D. After the activation of Mg acceptors at 650 °C for 5 min in air, mesa isolation was performed by Cl_2 reactive ion etching (RIE). Next, the p-GaN layer was etched by RIE except in the gate region. Then, Ti/Al/Ti/Au was

Table 1. Summary of device parameters of $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer.

Sample name	AlN molar fraction x in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer	Thickness of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer (nm)
Sample A	0.15	16 ± 2
Sample B	0.17	
Sample C	0.27	
Sample D	0.36	

deposited as the source and drain contacts on $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$. Subsequently, a Ni/Au ohmic contact was deposited as a gate contact on p-GaN. The devices had a gate length of 2 μm , a gate width of 100 μm , and an interval of 8 μm between the drain and source contacts.

Figure 2 shows the current-voltage (I - V) characteristics of I_{DS} when the V_{G} values are 0 and 3 V in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFETs for (a) sample C (AlN molar fraction: 0.27) and (b) sample A (AlN molar fraction: 0.15). Sample C did not show a normally off mode with I_{DS} of 11.6 mA/mm when V_{G} and the drain-source voltage (V_{DS}) were 0 and 10 V, respectively. In contrast, a low external leakage current of 15.5 nA/mm was achieved in sample A when V_{G} and V_{DS} were 0 and 10 V, respectively. Also, R_{on} was 2.65 $\text{m}\Omega\text{-cm}^2$ in the $V_{\text{G}} = 3.0$ V active field. However, the on current at $V_{\text{G}} = 3.0$ V was not as high as expected from the sheet carrier concentration in sample A. This is caused by the high sheet resistance of 1500 $\Omega/\square$ in sample A, which is about 3 times larger than that of sample C. Such a high sheet resistance is thought to be caused by the fluctuation in etching depth, etching damage by RIE, and a change in the surface level in $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$. Therefore we can expect further improvement in the on current by optimizing the etching process and using a surface passivation procedure.

Figure 3 shows a summary of I_{DS} when V_{G} and V_{DS} are 0 and 10 V, respectively, for various AlN molar fractions in the $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer. Figure 3 also shows V_{th} as a function of AlN molar fraction. As shown in Fig. 3, with increasing AlN molar fraction x in the $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer, the I_{DS} at $V_{\text{G}} = 0$ V and $V_{\text{DS}} = 10$ V increases and V_{th} decreases. V_{th} decreases as the density of the 2DEG under the gate increases. Therefore, the leakage current increases when V_{th} decreases.

Figure 4 shows the conduction band and Fermi level of the JHFETs as functions of AlN molar fraction x in the $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer simulated by SiLENSe Ver. 1.0.¹⁴⁾ SiLENSe Ver. 1.0 is governed by the electric continuity and Poisson equations. The piezoelectric field is determined by a piezoelectric tensor. The details of SiLENSe Ver. 1.0 are shown in ref. 14. The conduction band of the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterointerface increases with decreasing AlN molar fraction x in the $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer. When the conduction band is above the Fermi level, 2DEG is not generated. The energy difference between the conduction band minimum and the Fermi level at the interface of u-GaN and $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ is as large as 0.86 eV when the AlN molar fraction is 0.15 in the $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer. If the AlN molar fraction is 0.27, high-density 2DEG is generated. Such a large difference causes the difference in the leakage current in the enhancement-mode $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFETs.

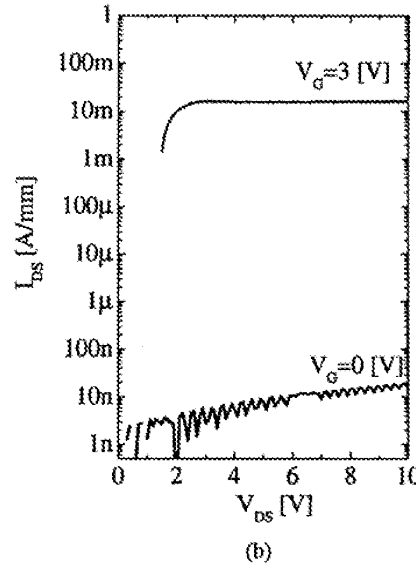
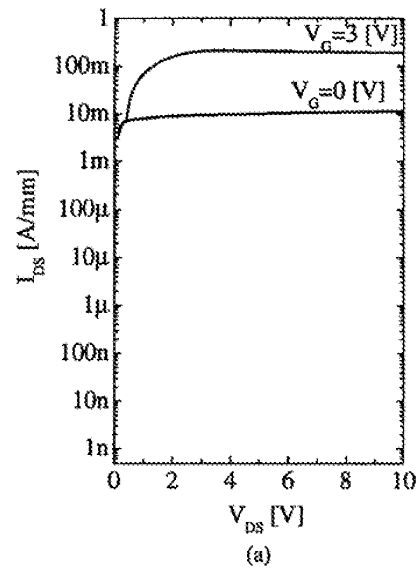


Fig. 2. I - V characteristics of I_{DS} with V_{G} of 0 and 3 V in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFETs for (a) sample C (AlN molar fraction: 0.27) and (b) sample A (AlN molar fraction: 0.15).

Figure 5 shows the on/off current ratio for V_{G} of 0 and 3 V for various AlN molar fractions x in the $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer. The maximum on/off ratio of I_{DS} is over 6 orders of magnitude in the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFET with an AlN molar fraction of 0.15 and a $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer thickness of 15 nm. Therefore, we believe that $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFETs with a p-type GaN gate contact will be a key device for the realization of a low-loss in-vehicle switching device.

In summary, the important device parameters for attaining an extremely low leakage current and a high on/off ratio in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ JHFETs with a p-GaN gate contact were verified. By optimizing the AlN molar fraction in the u-

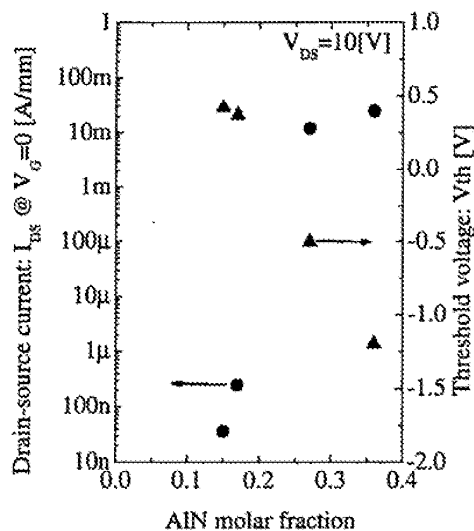


Fig. 3. Leakage current (●) and threshold voltage (▲) at drain source when V_G is 0 V for various AlN molar fractions x of $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer.

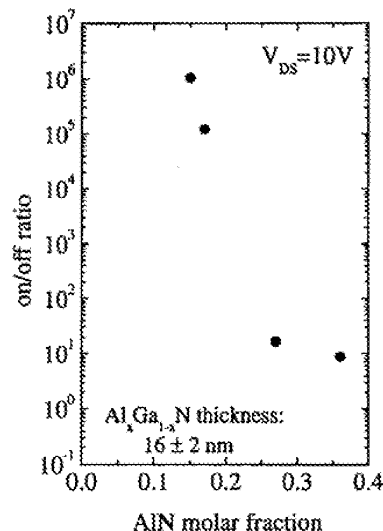


Fig. 5. On/off ratio of I_{DS} with V_G of 0 and 3 V for various AlN molar fractions x of $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer ($\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ thickness: $d = 16 \pm 2$ nm).

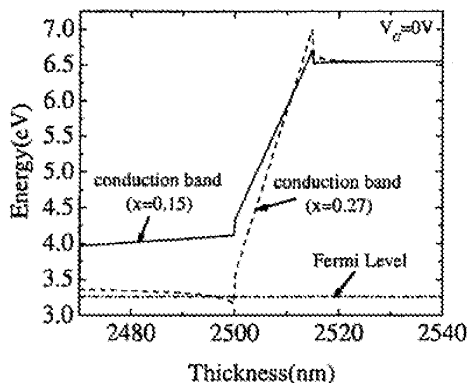


Fig. 4. Simulated results of conduction band diagrams under gate contact with AlN molar fractions of 0.15 and 0.27 in $\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer ($\text{u-Al}_x\text{Ga}_{1-x}\text{N}$ thickness: $d = 16$ nm).

$\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer, the drain-source leakage current became as low as 15.5 nA/mm at V_{DS} and V_G of 10 and 0 V, and an on current 6 orders of magnitude higher than the leakage current was realized at $V_G = 3$ V. R_{on} was $2.65 \text{ m}\Omega\text{-cm}^2$ in the $V_G = 3.0$ V active field.

Acknowledgements

This work was partly supported by the Ministry of Education, Culture, Sports, Science and Technology (MEXT) (#18206036, 18760259), Iketani Science and

Technology Foundation and the Akasaki Research Center in Nagoya University.

- 1) M. A. Khan, J. N. Kuznia, M. Van Hove, N. Pan and J. Carter: Appl. Phys. Lett. **60** (1992) 3027.
- 2) S. N. Mohamud, A. A. Salvador and H. Morkoc: Proc. IEEE **83** (1995) 1306.
- 3) S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour and T. Jenkins: IEEE Electron Device Lett. **18** (1997) 293.
- 4) O. Akatas, Z. F. Fan, A. Botcharov, S. N. Mohammad, M. Roth, T. Jenkins, L. Kehias and H. Morkoc: IEEE Electron Device Lett. **18** (1997) 293.
- 5) S. Keller, Y.-F. Wu, G. Parish, N. Zhiang, J. J. Xu, B. P. Keller, S. P. DenBaars and U. K. Mishra: IEEE Trans. Electron Devices **48** (2001) 552.
- 6) M. Micovic, N. X. Nguyen, P. Janke, W. S. Wong, P. Hashimoto, L. M. McCray and C. Nguyen: Electron. Lett. **36** (2000) 358.
- 7) V. Kumar, W. Lu, R. Schwindt, A. Kuliev, G. Simin, J. Yang, M. A. Khan and I. Adesida: IEEE Electron Device Lett. **23** (2002) 455.
- 8) N. Tsuyukuchi, K. Nagamatsu, Y. Hirose, M. Iwaya, S. Kamiyama, H. Amano and I. Akasaki: Jpn. J. Appl. Phys. **45** (2006) L319.
- 9) T. Fujii, N. Tsuyukuchi, Y. Hirose, M. Iwaya, S. Kamiyama, H. Amano and I. Akasaki: submitted to Jpn. J. Appl. Phys.
- 10) T. Hashizume, S. Ananthanasam, N. Negora, E. Sano, H. Hasegawa, K. Kumakura and T. Makimoto: Jpn. J. Appl. Phys. **43** (2004) L777.
- 11) A. Endoh, Y. Yamashita, K. Ikeda, M. Higashiwaki, K. Hikosaka, T. Matsui, A. Hiayamizu and S. Mimura: Jpn. J. Appl. Phys. **43** (2004) 2255.
- 12) T. Kawasaki, K. Nakata and S. Yaegashi: Ext. Abstr. (52nd Spring Meet., 2005); Japan Society of Applied Physics and Related Societies, 1p-S-7 (in Japanese).
- 13) H. Amano, N. Sawaki, I. Akasaki and Y. Toyoda: Appl. Phys. Lett. **48** (1986) 353.
- 14) <http://www.semitech.us/products/SILENSE/>

Gate Injection Transistor (GIT)—A Normally-Off AlGaIn/GaN Power Transistor Using Conductivity Modulation

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Abstract—We have developed a normally-off GaN-based transistor using conductivity modulation, which we call a gate injection transistor (GIT). This new device principle utilizes hole-injection from the p-AlGaIn to the AlGaIn/GaN heterojunction, which simultaneously increases the electron density in the channel, resulting in a dramatic increase of the drain current owing to the conductivity modulation. The fabricated GIT exhibits a threshold voltage of 1.0 V with a maximum drain current of 200 mA/mm, in which a forward gate voltage of up to 6 V can be applied. The obtained specific ON-state resistance ($R_{ON} \cdot A$) and the OFF-state breakdown voltage (BV_{DS}) are $2.6 \text{ m}\Omega \cdot \text{cm}^2$ and 800 V, respectively. The developed GIT is advantageous for power switching applications.

Index Terms—Conductivity modulation, GaN, high breakdown voltage, high power switching device, hole injection, low specific ON-state resistance, normally off, Si substrate.

I. INTRODUCTION

AlGaIn/GaN heterojunction field effect transistors (HFETs) are widely investigated for high-power switching applications. Most of the reported AlGaIn/GaN HFETs are the normally-on type taking advantage of the inherent high sheet carrier density caused by the built-in polarization electric field [1], [2]. However, such normally-on-type HFETs are not applicable to actual power switching applications in which safe operation is the main concern. Thus, in these applications, Si-based power MOSFETs/insulated gate bipolar transistors (IGBTs) have been exclusively used so far. A normally-off operation is strongly desired for AlGaIn/GaN HFETs while keeping the low ON-state resistance. To meet such requirements, it is necessary to reduce the 2-D electron gas (2DEG) density in the channel. Since the 2DEG is caused by the difference of the polarization-induced fixed charges between GaN and AlGaIn, reduction of the Al mole fraction or the thickness of AlGaIn effectively reduces those carriers and thereby shifts the threshold voltage toward the positive direction. This approach easily achieves the normally-off operation; however, the result-

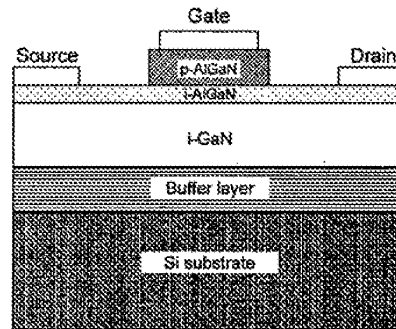


Fig. 1. Schematic illustration of the GIT structure.

ing drain current would be low since the applicable positive gate voltage is limited by the low barrier height on the AlGaIn with high sheet resistance. Thus, the reduction of the ON-state resistance is limited in this approach [3]–[6].

In this paper, we demonstrate a new operation principle of a GaN-based normally-off transistor with high drain current, which we call a gate injection transistor (GIT). The GIT utilizes hole injection from the p-type gate to the 2DEG region bringing out the conductivity modulation as observed in IGBTs [7]. This new concept enables both normally-off operation and high current driving capability by applying high positive gate voltage with low gate current.

II. OPERATION PRINCIPLE OF GIT

The most notable feature of the GIT is the p-AlGaIn gate formed over the undoped AlGaIn/GaN heterostructure, as shown in Fig. 1. The p-AlGaIn lifts up the potential at the channel, which enables normally-off operation, as shown in the band diagram in Fig. 2.

Fig. 3 illustrates the basic operation of the GIT. At the gate voltage of 0 V, the channel under the gate is fully depleted, and the drain current does not flow. At the gate voltages up to the forward built-in voltage V_F of the p-n junction, the GIT is operated as a field effect transistor (FET). Further increase of the gate voltage exceeding the V_F results in the hole injection to the channel from the p-AlGaIn. Note that the injection of the electrons from the channel to the gate is well suppressed by the heterobarrier at AlGaIn/GaN. The injected holes accumulate

Manuscript received May 14, 2007; revised August 13, 2007. The review of this paper was arranged by Editor M. A. Shibib.

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Digital Object Identifier 10.1109/TED.2007.908601

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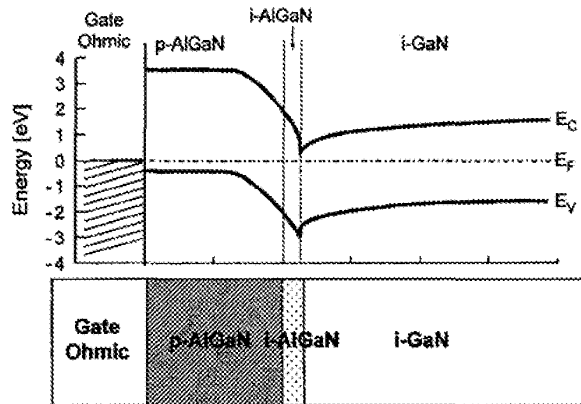


Fig. 2. Calculated band diagram of the GIT under a gate bias of 0 V.

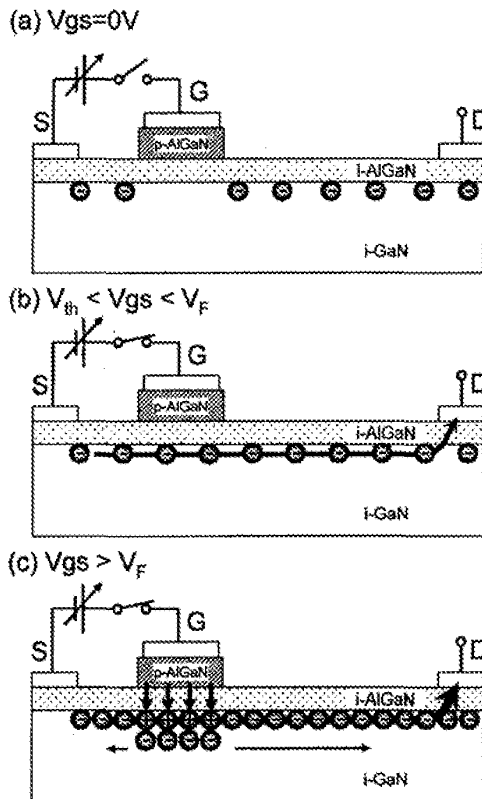


Fig. 3. Schematics of the various GIT operation conditions with various gate voltages. (a) Normally-off operation with the fully depleted channel under the gate at $V_{gs} = 0$ V. (b) FET operation without hole injection at $V_{th} < V_{gs} < V_p$. (c) GIT operation with hole injection at $V_{gs} > V_p$.

the equal number of electrons that flow from the source to keep charge neutrality at the channel. The accumulated electrons are moved by the drain bias with high mobility, while the injected holes stay around the gate because the hole mobility is at least two orders of magnitude lower than that of the electron. This conductivity modulation results in a significant increase of the drain current, which keeps the low gate current.

Fig. 4 shows the distributions of holes and electrons in the GIT obtained by a 2-D device simulation at three gate voltages, where a drain voltage of 0.1 V is applied. With the gate voltage of 0 V, the channel under the gate is fully depleted. With the gate voltage of 2 V, the drain current flows with the increased sheet charge density in the 2DEG, although the p-n junction gate is not in the ON-state, and no hole is injected into the i-GaN layer. With the gate voltage of 6 V, the holes start to be injected into the i-GaN, generating large numbers of electrons.

Fig. 5 shows the simulated drain current and the gate current as a function of the gate voltages for both a GIT and for a conventional Schottky-metal gate HFET (MESFET). The drain current of the conventional MESFET is saturated when the gate current flows with the gate bias over 2 V. On the contrary, the drain current of the GIT is dramatically increased by the aforementioned conductivity modulation, even though the gate current starts to flow. The simultaneously accumulated electrons move to the drain with high mobility and relatively low gate current is maintained with the gate voltages up to 6 V. The dramatic increase of the drain current with the low gate current enables low ON-state resistances to keep the normally-off operation.

III. DEVICE STRUCTURE AND FABRICATION

The process flow of the GIT of which a cross section is shown in Fig. 1 is summarized as follows. A p-AlGaAs/i-AlGaAs/GaN heteroepitaxial structure for the GIT is grown on a Si substrate with buffer layers consisting of the GaN/AlN multilayers on top of the AlGaAs/AlN initial layers. Both layers effectively relieve the strain in the overgrown GaN caused by the lattice and thermal mismatch between GaN and Si [8]. The total thickness of the nitride epitaxial layer is 4.7 μm . To realize the normally-off operation, the Al mole fraction and the thickness of i-AlGaAs are optimized to be 15% and 25 nm. The p-type gate is formed by the selective etching of the p-AlGaAs. The Al mole fraction and the thickness of the p-AlGaAs are chosen to be 15% and 100 nm. After the formation of the device isolation area, the Ti/Al source/drain and Pd gate metals are formed. As a passivation film, 400-nm-thick SiN was deposited by PECVD. Au interconnections are made by electroplating.

A cross-sectional SEM image of the fabricated GIT is shown in Fig. 6. The gate length defined by the p-AlGaAs width is 2.0 μm , and the distance between the gate and the drain is 7.5 μm .

IV. DEVICE PERFORMANCES

Fig. 7 shows ON-state and OFF-state I_{ds} - V_{ds} characteristics of the fabricated GITs. A normally-off operation with the threshold voltage of 1.0 V is achieved. The maximum drain current I_{max} is as high as 200 mA/mm. The resulting specific ON-state resistance is 2.6 $\text{m}\Omega \cdot \text{cm}^2$, and the OFF-state breakdown voltage is 800 V. No current offset is observed at zero drain bias, as shown in Fig. 7(a), indicating a low level of the gate current under the forward gate voltage. The fabricated GIT has a slightly positive temperature dependence in which the threshold voltage is 1.0 V at 25 $^{\circ}\text{C}$ and 1.05 V at 150 $^{\circ}\text{C}$,

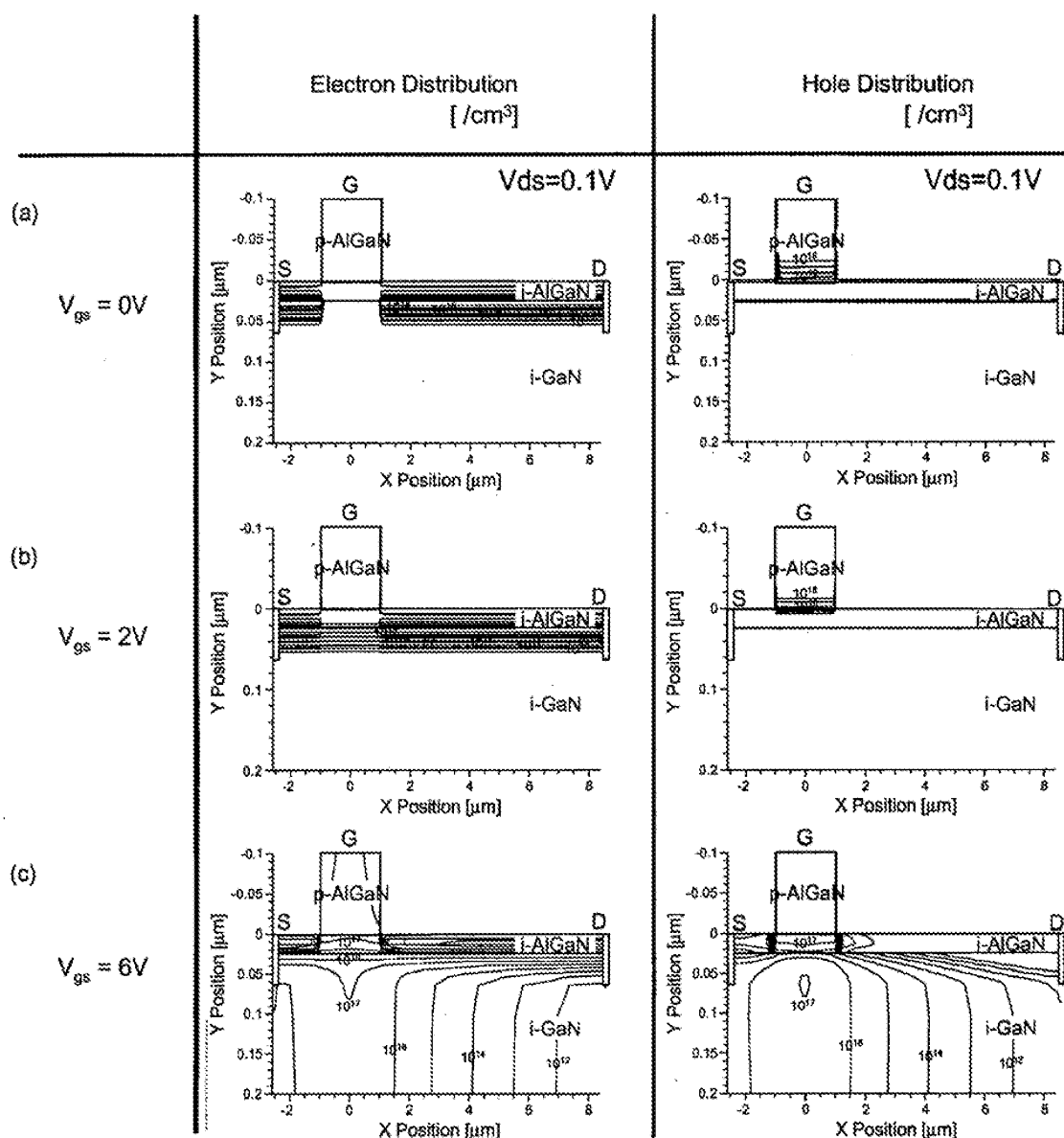


Fig. 4. Contour maps of distributions of holes and electrons in a GIT with various gate voltages calculated by a 2-D device simulation. (a) $V_{gs} = 0$ V; normally-off. (b) $V_{gs} = 2$ V; without hole injection. (c) $V_{gs} = 6$ V; with hole injection.

respectively. This is due to the increase of the gate resistance at the elevated temperature. Thus, a thermal positive feedback does not occur in the GIT, and therefore, the GIT can safely be operated even at higher temperatures.

Fig. 8 shows the I_{ds} - V_{gs} and gm - V_{gs} characteristics of the fabricated GIT compared with those of the conventional Schottky-gate MESFET. For the GIT, the forward gate voltages up to 6 V can be applied, while the applicable forward gate voltage is limited below 2 V in the conventional MESFET. The GIT exhibited peculiar transconductance characteristics with two peaks, as seen in Fig. 8. The device is operated as a FET up to the gate voltage of 3 V. Further increase of the gate voltage superlinearly increases the drain current corresponding

to the second gm peak. This observed second peak of the gm is the evidence of the hole injection in the GIT. At such high gate voltages, the recombination of the injected holes and electrons in the 2DEG causes light emission, as shown in Fig. 9. The electroluminescence at 364 nm corresponds to the optical band gap of GaN. The light emission is diminished when the drain bias is given. This indicates that the accumulated electrons move to the drain so that the recombination is suppressed.

Typical Gummel plots of the GIT and the MESFET, the drain and gate currents as functions of the gate voltages, are shown in Fig. 10(a). The drain current of the GIT increases due to the hole injection at higher gate voltages, where the gate current

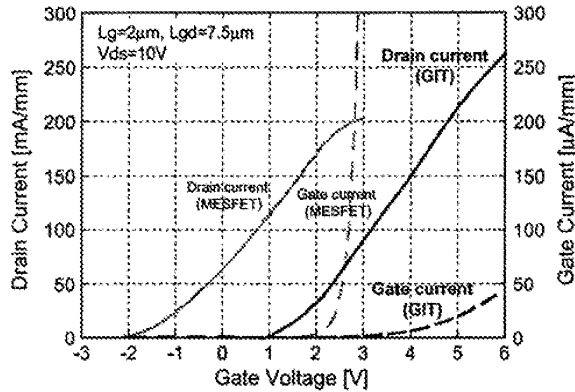


Fig. 5. Calculated drain current and gate current as a function of the gate voltage for both a GIT and for a conventional MESFET.

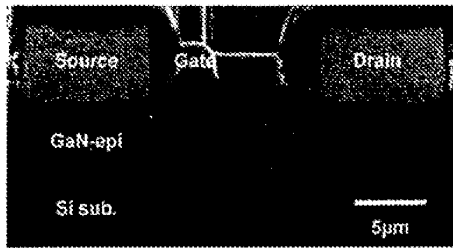


Fig. 6. Cross-sectional SEM image of the fabricated GIT on a Si substrate.

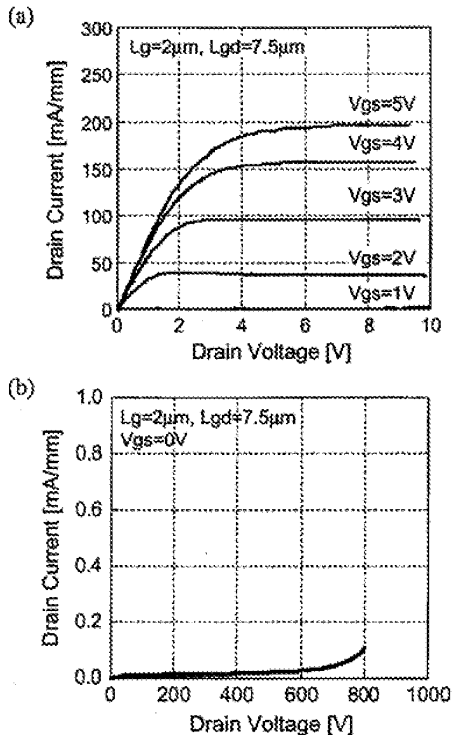


Fig. 7. (a) ON state and (b) OFF state at $V_{gs} = 0$ V I_{ds} - V_{ds} characteristics of the fabricated GIT ($V_{th} = +1.0$ V, $R_{ON} \cdot A = 2.6$ m $\Omega \cdot$ cm ^{2} , $I_{max} = 200$ mA/mm, and breakdown voltage = 800 V).

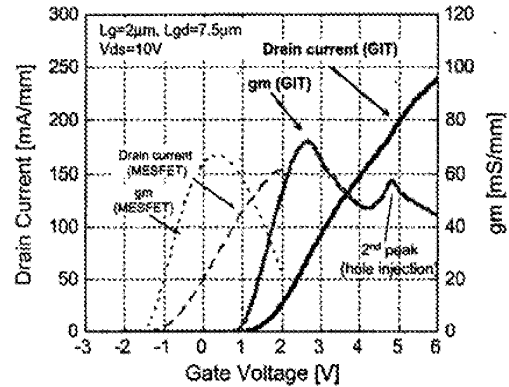


Fig. 8. I_{ds} - V_{gs} and gm - V_{gs} characteristics of (a) a fabricated GIT and (b) a MESFET. GIT exhibited peculiar transconductance characteristics with two peaks.

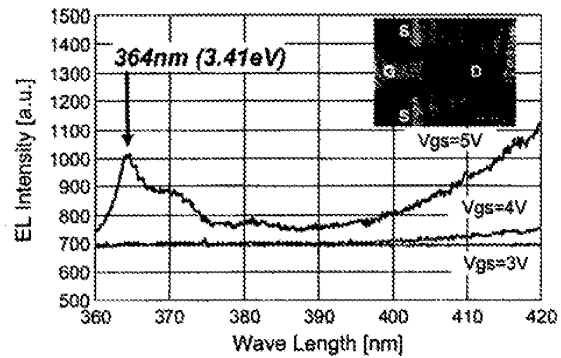


Fig. 9. Electroluminescence spectrum obtained from the fabricated GIT with different gate voltages.

increases. Such increase of the drain current is not observed with the MESFET. The ratio of ΔI_d to ΔI_g , the current gain h_{FE} , is plotted as a function of the gate voltages in Fig. 10(b). At higher gate voltages, the h_{FE} of the GIT stays from 100 to 1000. This experimentally obtained h_{FE} s agrees well with the mobility ratio of the electrons to the holes, which supports the operation principle of the GIT.

Fig. 11 summarizes the switching characteristics of the fabricated GIT. The circuit diagram for the measurement and the definition of the switching parameters are summarized in Fig. 11(a). The given drain bias and driving current are 100 V and 10 A, respectively, using 10 Ω load resistance. The rise, fall, on-delay, and off-delay times of the drain current are measured by varying the gate voltages, as shown in Fig. 11(b). The measured rise and on-delay times are on the order of 10 ns, which are shorter than those of the conventional Si-based MOSFETs and IGBTs. The fall and off-delay times are slightly longer due to the slow recombination of the injected holes, even though the values are still smaller than those of Si-based MOSFETs and IGBTs.

In addition to the normally-off operation, suppression of the so-called current collapse has been strongly desired for the GaN-based power switching devices. The drain current is significantly reduced by the current collapse after applying high

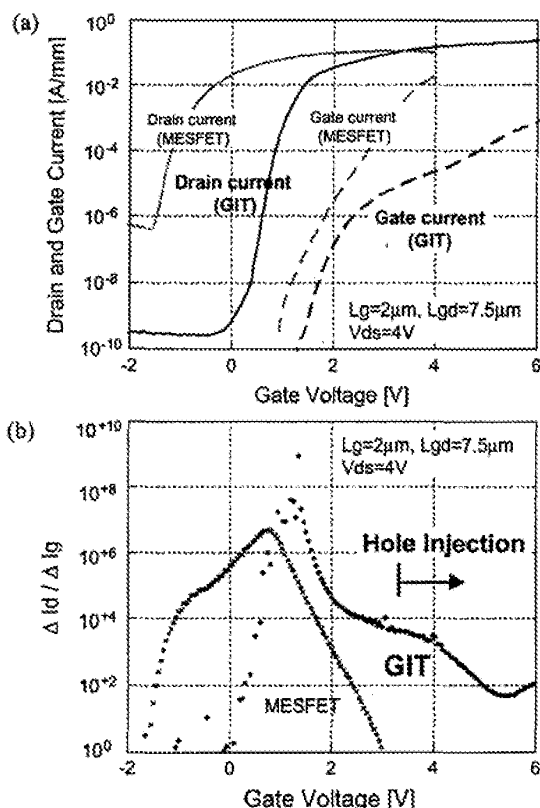


Fig. 10. Comparison of the obtained characteristics of the GIT and the MESFET. (a) Gummel plots. (b) Ratio of ΔI_d to ΔI_g (the current gain h_{FE}).

drain voltages presumably due to the surface or bulk traps. Fig. 12 shows the results of the pulsed I_{ds} - V_{ds} measurements for the GIT with different initial bias conditions. The almost identical I_{ds} - V_{ds} characteristics imply that the GIT is operated free from the current collapse. It is experimentally found that the presented GIT is not affected by surface traps without any special structures such as gate field plates.

Fig. 13 summarizes the state-of-the-art performances of the normally-off GaN-based power transistors, as compared with those of SiC and Si-based power transistors [3], [4], [9]–[13]. The $R_{ON} \cdot A$ and breakdown voltage of the GIT are the best values among the GaN-based normally-off transistors to the best of our knowledge. Note that they are as comparably good as those of SiC devices. The GIT on a Si substrate can provide the following advantages in addition to the low-cost fabrication. The use of a conductive substrate enables source–via grounding (SVG) structure [1]. By the SVG, the source can be ohmic-contacted to the conductive Si substrate through the surface via hole. The SVG plays three important roles. First, it reduces the source interconnection resistance, which makes the specific ON-state resistance in a large area device to be much lower. Second, the source parasitic inductance is also significantly reduced because of the eliminated source wires and bonding. Third, the SVG structure relieves the electric field between the drain and the gate since the grounded substrate acts as a backside field plate.

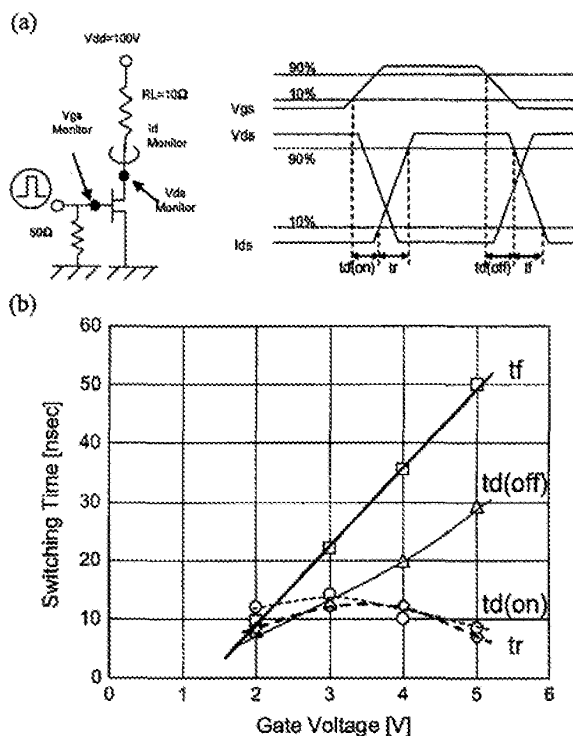


Fig. 11. (a) Circuit diagram for measurement and the definition of the switching parameters. (b) Switching characteristics of the fabricated GIT.

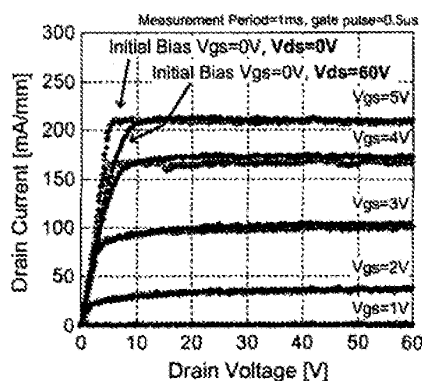


Fig. 12. Pulsed I_{ds} - V_{ds} characteristics of the fabricated GIT. Two sets of the initial bias are used ($V_{gs}=0\text{V}$, $V_{ds}=0\text{V}$ and $V_{gs}=0\text{V}$, $V_{ds}=60\text{V}$). The used pulsewidth and period are $0.5\mu\text{s}$ and 1ms , respectively.

V. CONCLUSION

We have successfully developed a new normally-off AlGaIn/GaN transistor with a high drain current. The transistor, which we call a GIT, utilizes hole injection from the p-AlGaIn formed over the i-AlGaIn/GaN, resulting in a dramatic increase of the drain current at high gate voltages due to the conductivity modulation. The resulting $R_{ON} \cdot A$ and the breakdown voltage are $2.6\text{ m}\Omega \cdot \text{cm}^2$ and 800 V , respectively. The GIT achieves a high drain current of 200 mA/mm with the threshold voltage of 1.0 V . It is noted that using Si substrates makes the GIT more

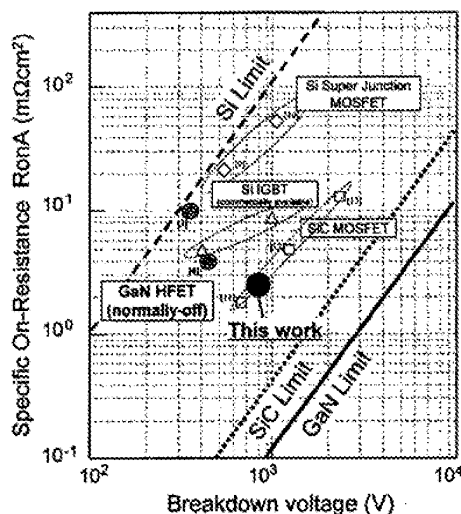
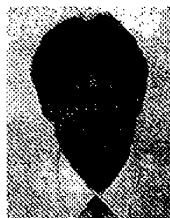


Fig. 13. State-of-the-art $R_{ON} \cdot A$ and breakdown voltage of normally-off GaN-based devices compared with those of Si-based devices and SiC MOSFETs.

cost-effective than ordinary GaN-based HFETs fabricated on sapphires or on SiCs. The presented GIT is advantageous for power switching applications.

REFERENCES

- [1] M. Hikita, M. Yanagihara, K. Nakazawa, H. Ueno, Y. Hirose, T. Ueda, Y. Uemoto, T. Tanaka, D. Ueda, and T. Egawa, "350 V/150 A AlGaIn/GaN power HFET on silicon substrate with source-via grounding (SVG) structure," in *IEDM Tech. Dig.*, Dec. 2004, pp. 803–806.
- [2] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and H. Ohashi, "High breakdown voltage AlGaIn/GaN power-HEMT design and high current density switching behavior," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003.
- [3] N. Ikeda, J. Li, and S. Yoshida, "Normally-off operation power AlGaIn/GaN HFET," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 369–372.
- [4] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-voltage AlGaIn/GaN HEMT for power electronics applications," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 356–362, Feb. 2006.
- [5] M. A. Khan, Q. Chen, C. J. Sun, J. W. Yang, M. Basingame, M. S. Shur, and H. Park, "Enhancement and depletion mode GaN/AlGaIn heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 68, no. 4, pp. 514–516, Jan. 1996.
- [6] W. B. Lanford, T. Tanaka, Y. Otaki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electron. Lett.*, vol. 41, no. 7, pp. 449–450, Mar. 2005.
- [7] B. J. Baliga, M. S. Adler, P. V. Gray, and R. P. Love, "The insulated gate rectifier (IGR)," in *IEDM Tech. Dig.*, Dec. 1982, pp. 264–267.
- [8] H. Ishikawa, M. Kato, M. S. Hao, T. Egawa, and T. Jimbo, "Growth of GaN on 4-inch Si substrate with a thin AlGaIn/AlN intermediate layer," in *Proc. 5th Int. Conf. Nitride Semicond. Tech. Dig.*, 2003, p. 424.
- [9] S. Iwamoto, K. Takahashi, H. Kuribayashi, S. Wakimoto, K. Mochizuki, and H. Nakazawa, "Above 500 V class superjunction MOSFETs fabricated by deep trench etching and epitaxial growth," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2005, pp. 31–34.
- [10] W. Saito, I. Omura, S. Aida, S. Koduki, M. Izumisawa, H. Yoshioka, and T. Ogura, "Over 1000 V semi-superjunction MOSFET with ultra-low on-resistance below the Si-limit," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2005, pp. 27–30.
- [11] S. Harada, M. Kato, K. Suzuki, M. Okamoto, T. Yatsuo, K. Fukuda, and K. Arai, "1.8 mΩ · cm², 10 A power MOSFET in 4H-SiC," in *IEDM Tech. Dig.*, Dec. 2006, pp. 903–906.
- [12] N. Miura, K. Fujihira, Y. Nakao, T. Watanabe, Y. Tarui, S. Kinouchi, M. Imaizumi, and T. Oomori, "Successful development of 1.2 kV 4H-SiC MOSFETs with very low on-resistance of 5 mΩcm²," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2006, pp. 261–264.
- [13] S. H. Ryu, S. Krishnaswami, M. Das, J. Richmond, A. Agarwal, J. Palmour, and J. Scofield, "4H-SiC DMOSFETs for high speed switching applications," *Mat. Sci. Forum*, vol. 483–485, pp. 797–800, 2005.



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Hiroaki Ueno received the B.E., M.E., and Dr.E. degrees in electronic engineering, for carrier transport investigations in GaAs heterostructure, from Osaka University, Osaka, Japan, in 1995, 1997, and 1999, respectively.

From 1999 to 2004, he had been a research associate with the Graduate School of Advanced Sciences of Matter, Hiroshima University, Hiroshima, Japan, where he worked on compact modeling in deep submicron MOSFETs. Since 2004, he has been with Matsushita Electric Industrial Company Ltd., Osaka, Japan, working on the development of the III-nitride RF devices.



Hisayoshi Matsuo received the B.S. and M.S. degrees in electrical and electronic engineering from Nagoya University in 2001 and 2003, respectively.

He joined the Semiconductor Device Research Center, Matsushita Electric Industrial Company Ltd., Osaka, Japan, in 2003. Since then, he has been engaged in III-nitride-based RF and high-power devices.



Hidetoshi Ishida (M'96) received the B.S. and M.S. degrees in electronics engineering from the Kyoto Institute of Technology, Kyoto, Japan, in 1989 and 1991, respectively, and the Ph.D. degree in electronics engineering from Osaka University, Osaka, Japan, in 2001.

Since 1991, he has been with Matsushita Electric Industrial Company Ltd., Osaka, Japan, where he worked on the research and development of GaAs HFETs, HBTs, and GaAs MMICs with the Semiconductor Device Research Center, and since 2003, he

has been working on III-nitride-based RF and switching power devices.

Dr. Ishida is a member of the IEEE Electron Device Society, the Japan Society of Applied Physics, and the Institute of Electronics, Information, and Communication Engineers of Japan.



Manabu Yanagihara received the B.S. and Ph.D. degrees in applied physics from Tokyo University, Tokyo, Japan, in 1985 and 1998, respectively.

He joined Matsushita Electric Industrial Company Ltd., Osaka, Japan, in 1985. He is currently a Staff Engineer with the Semiconductor Device Research Center, Matsushita Electronics Corporation, Kyoto, Japan, working on the research and development of GaAs-based HBTs and MESFETs for wireless communications.

Dr. Yanagihara is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information, and Communication Engineers of Japan.



Tetsuzo Ueda (M'95) received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1987 and 1989, respectively.

He joined the Electronics Research Laboratory, Matsushita Electronics Corporation, Osaka, Japan, in 1989, working on the research and development of GaAs MESFETs and MMICs. From 1995 to 2001, he had been a Visiting Research Scholar with Stanford University, Stanford, CA, as well as a Research Engineer with Panasonic Technologies Inc., Cupertino, CA, working on the epitaxial growth of

GaN with Prof. J. S. Harris, Jr. Since 2001, he has been with Matsushita Electric Industrial Company, Ltd., Osaka, Japan, working on the research and development of GaN-based optoelectronic devices, including lasers and LEDs, with the Semiconductor Device Research Center until 2004 and is currently a Manager with the Compound Semiconductor Device Group. His current interests include GaN-based electronic/optoelectronic devices and GaAs-based vertical cavity surface emitting lasers.

Mr. Ueda is a member of the American Vacuum Society and the Institute of Electronics, Information, and Communication Engineers. He had been a Far East Liaison Committee of the IEEE International Solid-State Circuits Conference from 1996 to 2001.



Tsuyoshi Tanaka (M'96) received the B.S. and M.S. degrees in applied physics and the Ph.D. degree in electrical engineering from Osaka University, Osaka, Japan, in 1983, 1985, and 2000, respectively.

Since 1985, he has been with Matsushita Electric Industrial Company Ltd., working on the research and development of microwave semiconductor devices, III-V FETs, HBTs, MMICs, and III-Nitride RF devices.

Dr. Tanaka is a member of the Institute of Electronics, Information, and Communication Engineering of Japan. He was a recipient of the Okochi prize in 1996.



Daisuke Ueda (M'96-SM'06) received the B.S. and M.S. degrees in electronics engineering from Kyushu Institute of Technology, Fukuoka, Japan, in 1977 and 1979, respectively, and the Ph.D. degree from Osaka University, Osaka, Japan, in 1987.

Since 1979, he has been with the Matsushita Electric Industrial Company Ltd., Osaka, Japan, where he is currently the Director of the Semiconductor Device Research Center, Semiconductor Company. He started with the research on semiconductor power devices and then developed the world-first trench

power MOSFET and trench IGBT with anode-short structure from 1980 to 1987. Since 1987, he has been working on the development of compound semiconductor devices, then developed III-V power HBT on silicon substrate with Prof. Jim Harris at Stanford University, Stanford, CA, as a Visiting Scholar from 1987 to 1988. He worked on the industrialization of a variety of GaAs devices and processes such as front-end MMIC with on-chip Barium Strontium Titanate (BST) capacitor, microwave switch with super self-aligned technology, spike-gate power FET with high PAE, and novel gate-orientation arrangement to obtain zero-temperature coefficient. He was a Lecturer with the Kyoto Institute of Technology from 1992 to 1994 and a Visiting Professor with Hokkaido University from 1997 to 1998. He has also been a Lecturer with Osaka University since 1988 and a Visiting Professor with Nagoya Institute of Technology since 2002. He is the author or coauthor of more than 100 technical papers. He served as an Editor of *Electron Device Letter* from 1998 to 2003. He is the holder of more than 80 patents. His current research interests include the practical realization of III-nitride devices from optical to microwave devices.

Dr. Ueda is a member of the Institute of Electronics, Information, and Communication Engineering of Japan (IEICE) and the Japan Society of Applied Physics. He was the Vice Chair of the Electronic Society of the IEICE from 2000 to 2002, Chair of Electron Devices Technical Working Group of the IEICE from 1998 to 2000, and the Chair of the IEEE Kansai Chapter from 2001 to 2003. He was twice the recipient of the Okochi Prize for the achievements on those GaAs MMICs in 1996 and Power Amplifiers in 2002.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Alexander Lidow		
Filer:		Stephen A. Soffen/Teresa Joel		
Attorney Docket Number:		E0101.0008/P008		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	82	82
Utility Search Fee	2111	1	270	270
Utility Examination Fee	2311	1	110	110
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				462

Electronic Acknowledgement Receipt	
EFS ID:	7380956
Application Number:	12756906
International Application Number:	
Confirmation Number:	1573
Title of Invention:	COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Alexander Lidow
Customer Number:	24998
Filer:	Stephen A. Soffen/Teresa Joel
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0008/P008
Receipt Date:	08-APR-2010
Filing Date:	
Time Stamp:	18:50:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$462
RAM confirmation Number	7895
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		8.pdf	8747804	yes	46
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal of New Application		1	1	
	Specification		2	10	
	Claims		11	12	
	Abstract		13	13	
	Drawings-only black and white line drawings		14	26	
	Oath or Declaration filed		27	31	
	Transmittal Letter		32	33	
	Information Disclosure Statement (IDS) Filed (SB/08)		34	34	
	NPL Documents		35	46	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	33075	no	2
			2441e1209a64891dbc1293c3fe181a90fe74131a		
Warnings:					
Information:					
Total Files Size (in bytes):			8780879		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

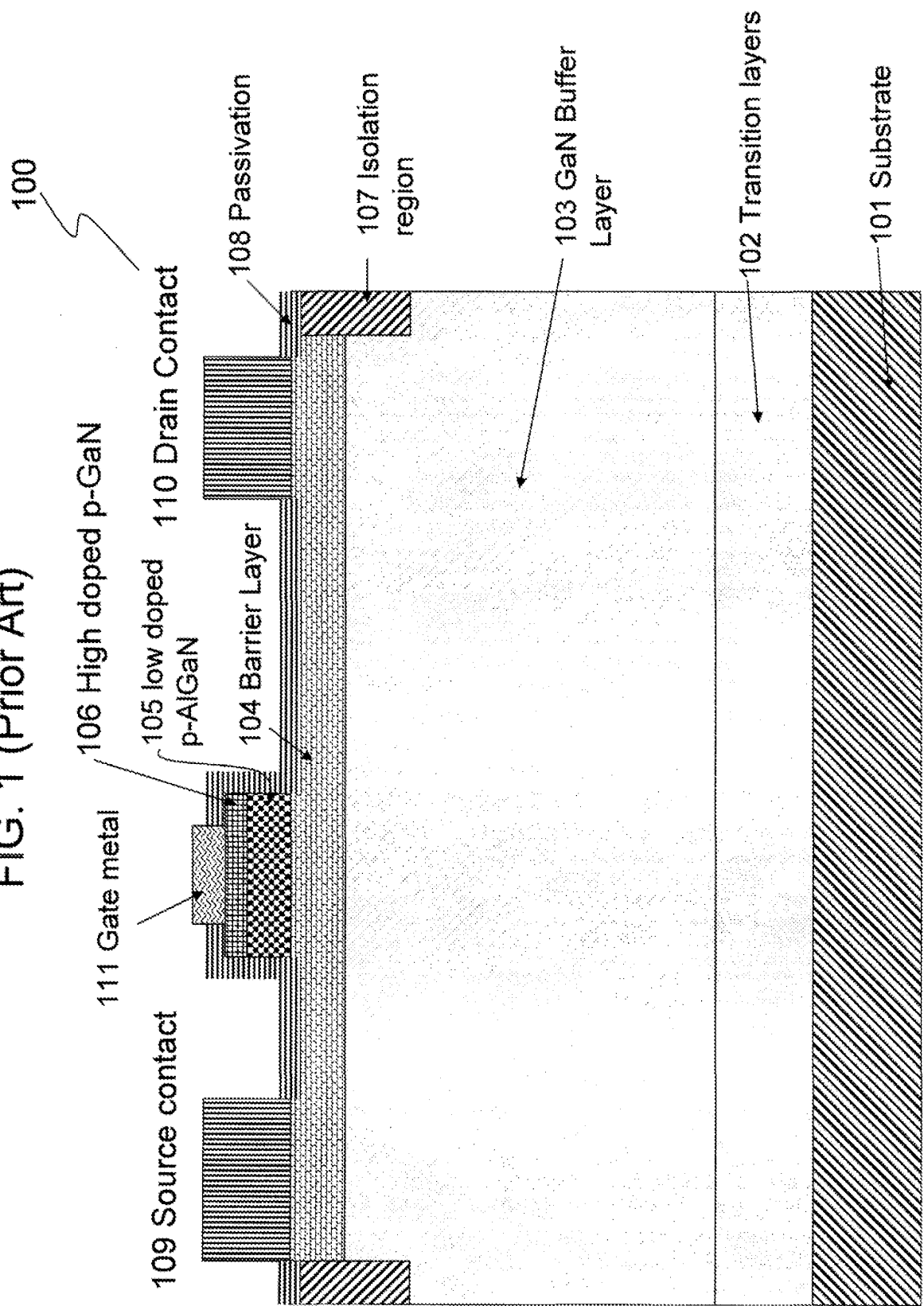
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UTILITY PATENT APPLICATION TRANSMITTAL (ONLY FOR NEW NONPROVISIONAL APPLICATIONS UNDER 37 CFR 1.53(B))		Attorney Docket No. E0101.0008/P008	
		First Inventor Alexander Lidow	
		Title COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME	
		Express Mail Label No. _____	

APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
1. ☐ Fee Transmittal Form (e.g., PTO/SB/17) 2. ☒ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification [Total Pages 12] Both the claims and abstract must start on a new page (For information on the preferred arrangement, see MPEP 606.01(a)) 4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 13] 5. Oath or Declaration [Total Sheets 5] a. ☒ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 18 completed) i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☐ Application Data Sheet. See 37 CFR 1.76 7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix) ☐ Landscape Table on CD 8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. - c. are required) a. ☐ Computer Readable Form (CRF) b. Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies 18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76: ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____ Prior application information: Examiner _____ Art Unit: _____	ACCOMPANYING APPLICATION PARTS 9. ☒ Assignment Papers (cover sheet & document(s)) Name of Assignee 10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney (when there is an assignee) 11. ☐ English Translation Document (if applicable) 12. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☒ Copies of citations attached 13. ☐ Preliminary Amendment 14. ☐ Return Receipt Postcard (MPEP 503) (Should be specifically itemized) 15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 17. ☐ Other:

19. CORRESPONDENCE ADDRESS	
☒ The address associated with Customer Number: 24998 OR ☐ Correspondence address below	
Name	Stephen A. Soffen DICKSTEIN SHAPIRO LLP
Address	1825 Eye Street, NW
City	Washington State DC Zip Code 20006-5403
Country	US Telephone (202) 420-2200 Email _____
Signature	
Name (Print/Type)	Stephen A. Soffen
Date	April 8, 2010
Registration No. (Attorney/Agent)	31,063

FIG. 1 (Prior Art)



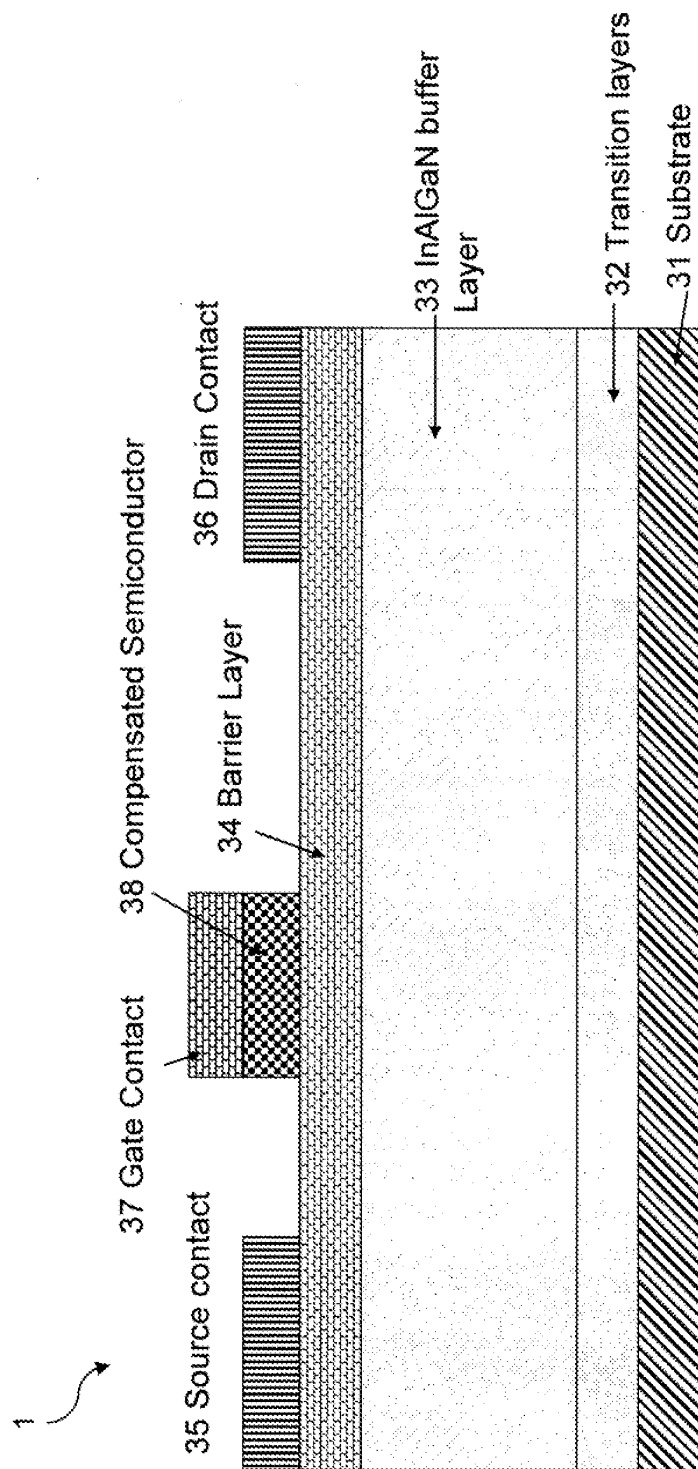


FIG. 2

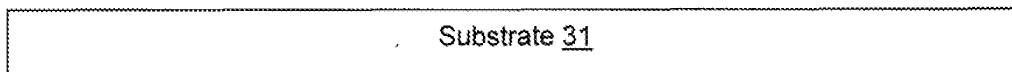


FIG. 3

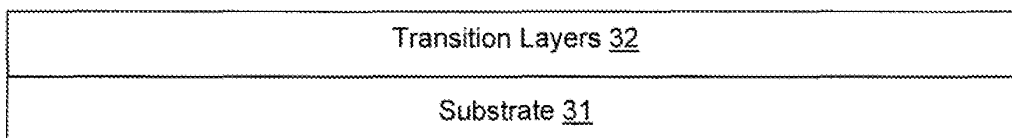


FIG. 4

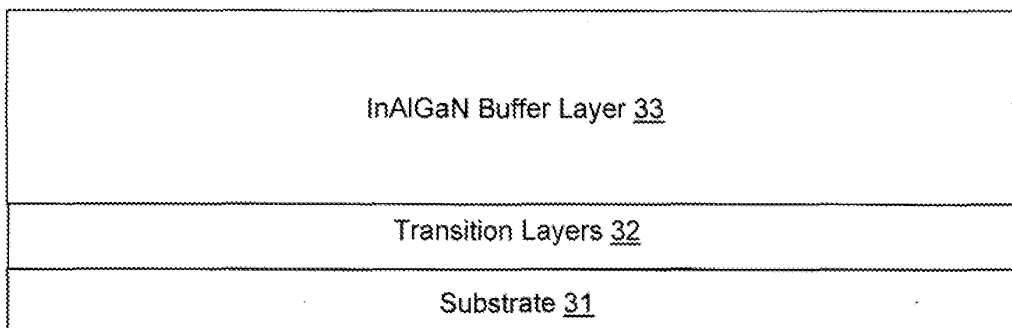


FIG. 5

Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 6

Compensated Semiconductor <u>38</u>
Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 7

Gate Contact <u>37</u>
Compensated Semiconductor <u>38</u>
Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 8

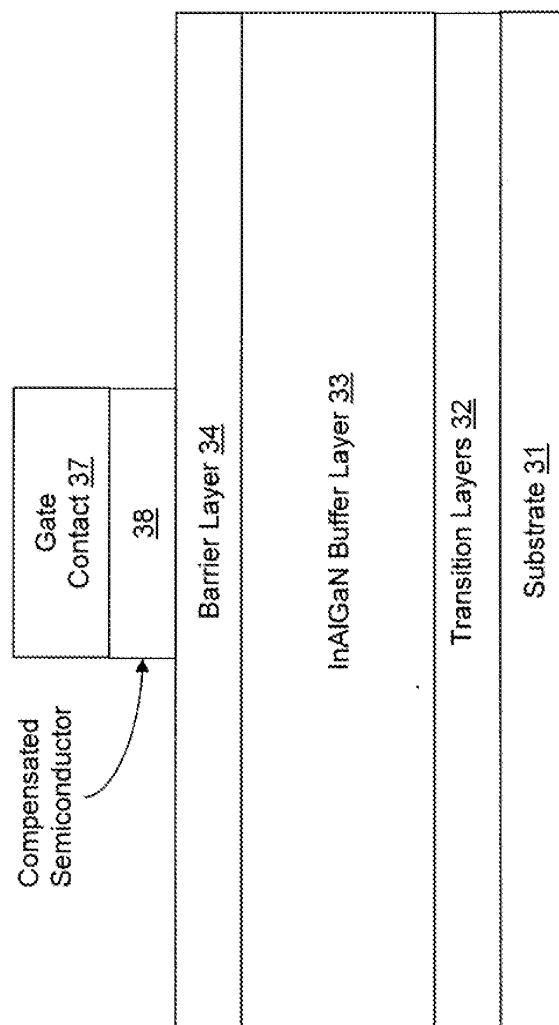


FIG. 9

2

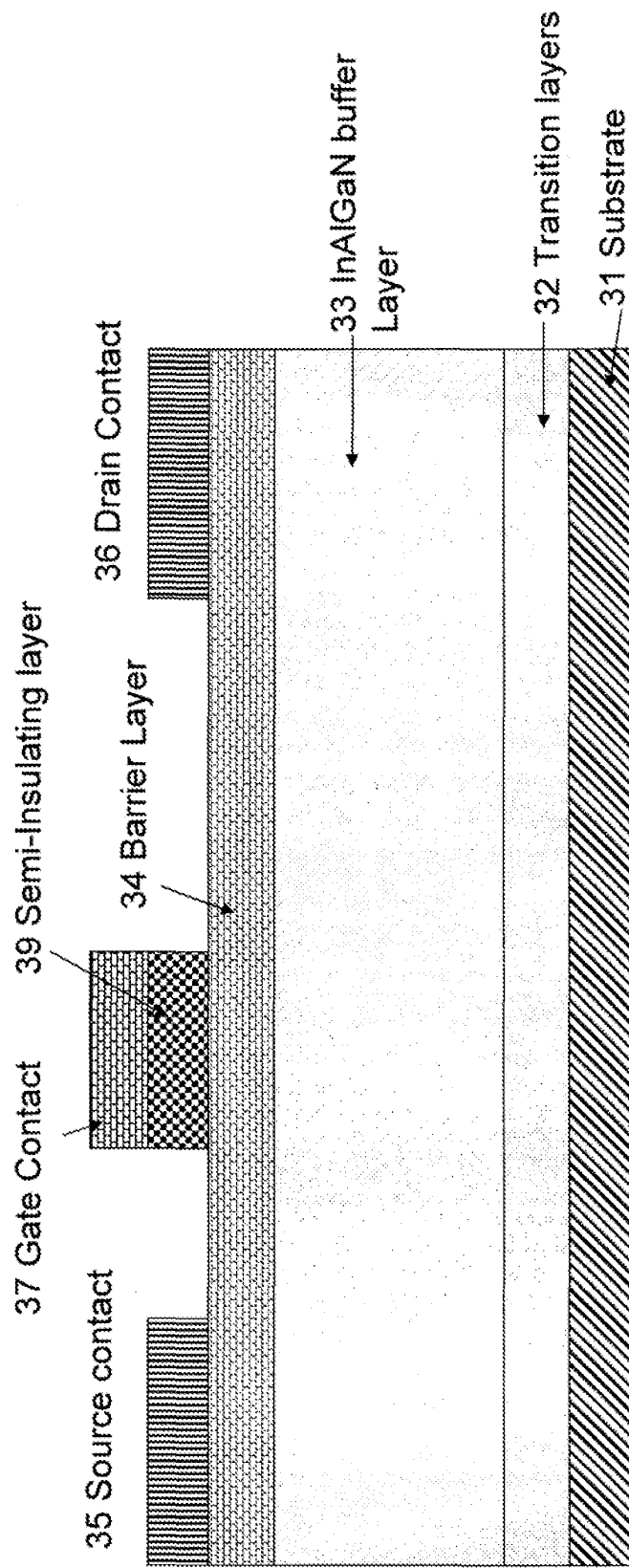


FIG. 10

Semi-insulating layer <u>39</u>
Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 11

Gate Contact <u>37</u>
Semi-insulating layer <u>39</u>
Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 12

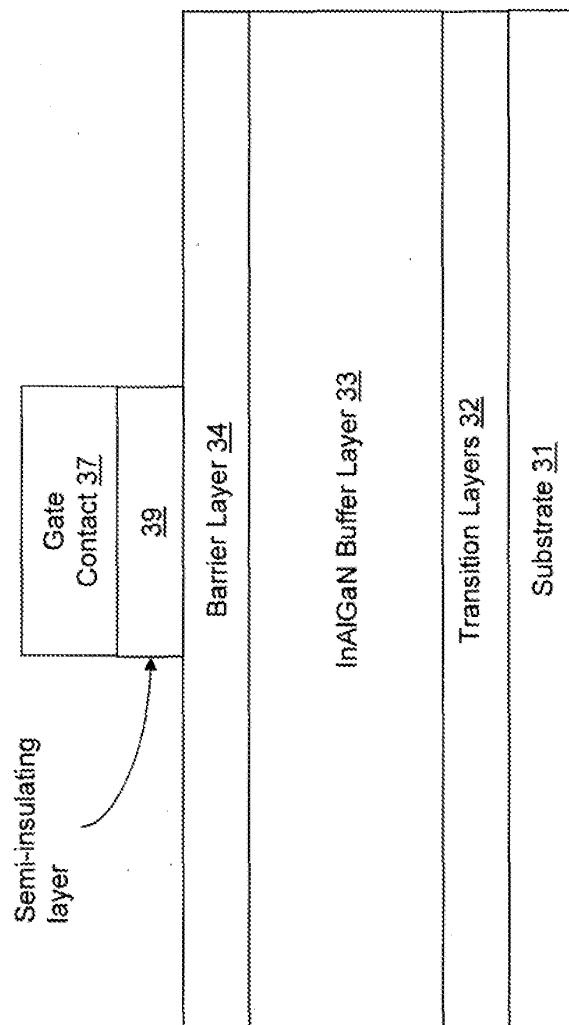


FIG. 13

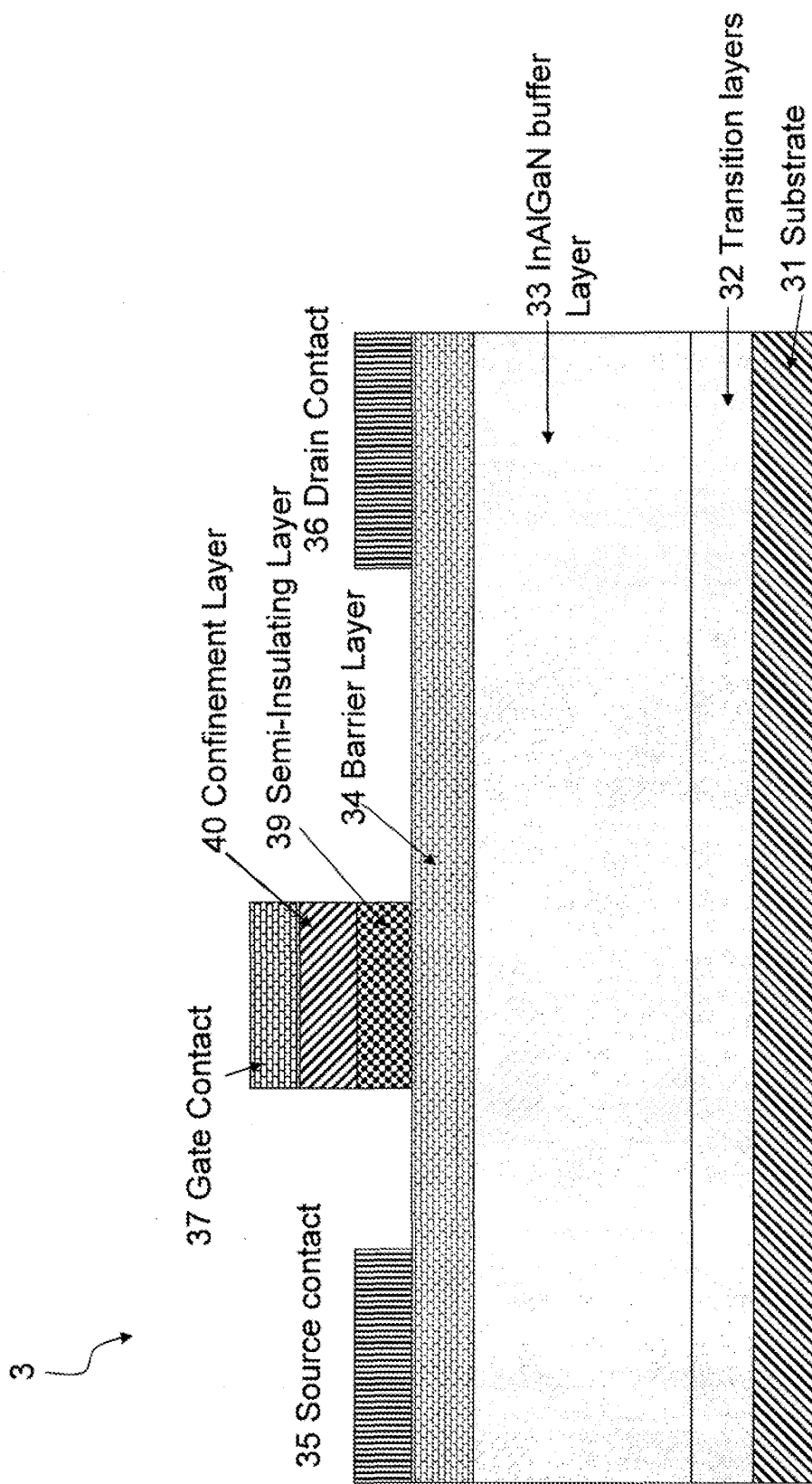


FIG. 14

Gate Contact <u>37</u>
Confinement Layer <u>40</u>
Semi Insulating Layer <u>39</u>
Barrier Layer <u>34</u>
InAlGaN Buffer Layers <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 15

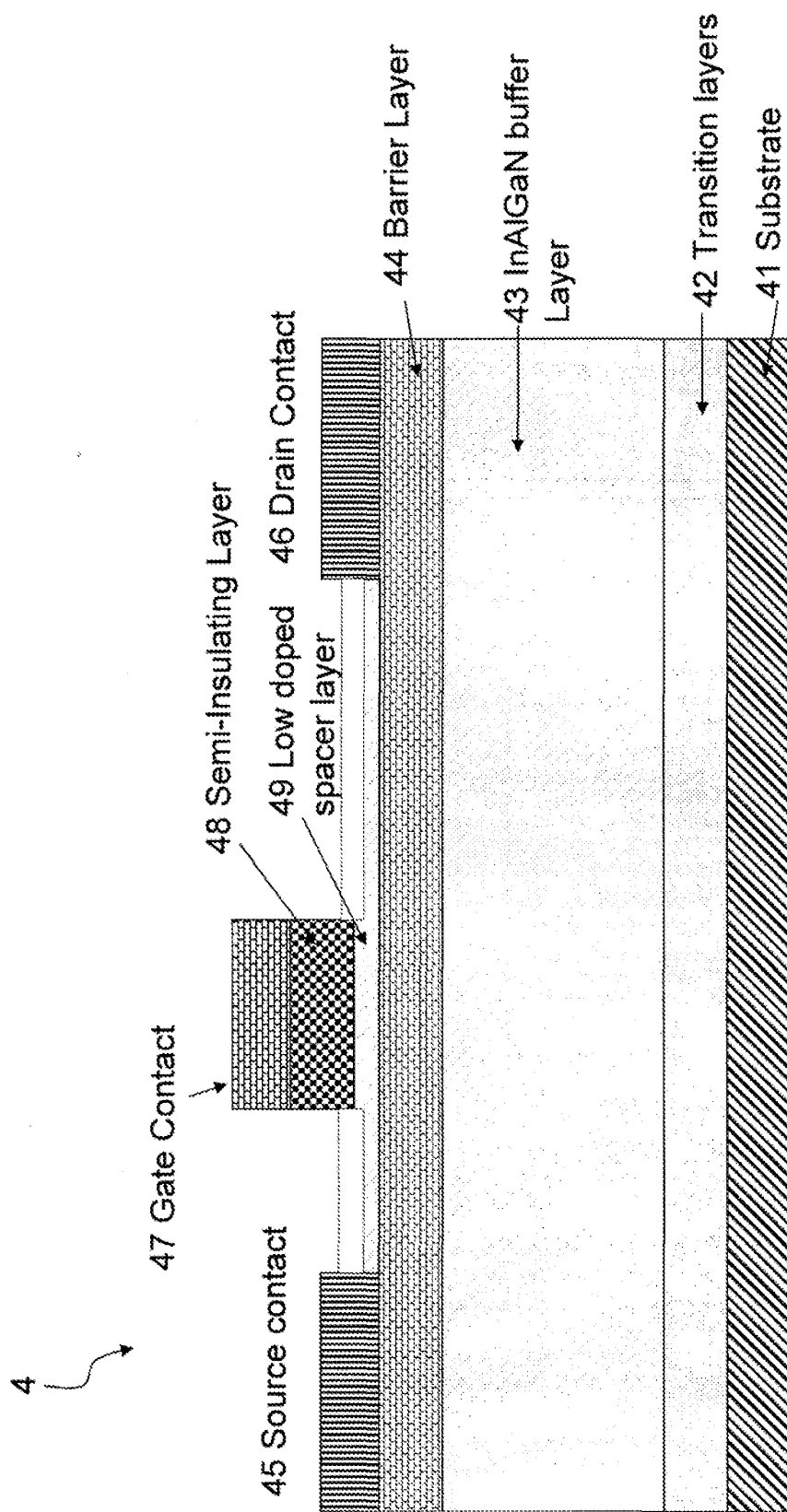


FIG. 16

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

COMPENSATED GATE MISFET AND METHOD FOR FABRICATING SAME

the specification of which is attached hereto.

In the event that the filing date and/or Application No. are not entered above at the time I execute this document, and if such information is deemed necessary, I hereby authorize and request my attorneys/agent(s) at **Dickstein Shapiro LLP**, 1825 Eye Street, NW, Washington, DC 20006-5403, to insert above the filing date and/or Application No. of said application.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to herein.

I acknowledge the duty to disclose all information known to me that is material to patentability as defined in 37 CFR 1.56.

FOREIGN PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

☒ no such foreign applications have been filed

☐ such foreign applications have been filed as follows:

**EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION**

Application Number	Country	Date of Filing	Priority Claimed Under 35 USC 119

**ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION**

Application Number	Country	Date of Filing

CLAIM FOR BENEFIT OF EARLIER U.S. PROVISIONAL APPLICATIONS

I hereby claim priority benefits under Title 35, United States Code §119(e), of any United States provisional patent application(s) listed below:

- ☐ no such U.S. provisional applications have been filed.
- ☒ such U.S. provisional applications have been filed as follows:

Application Number	Date of Filing	Priority Claimed Under 35 USC 119
61/167,792	April 8, 2009	Yes

CLAIM FOR BENEFIT OF EARLIER U.S./PCT APPLICATION(S)

I hereby claim the benefit under Title 35, United States Code, §120 of the United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information that is material to patentability as defined in 37 CFR 1.56 which became available to me between the filing date of the prior application and the national or PCT international filing date of this application:

- ☒ no such U.S./PCT applications have been filed.
- ☐ such U.S./PCT applications have been filed as follows:

Application Number	Relationship	Parent Application	Date of Filing

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint:

All practitioners at Customer Number 24998

all of **Dickstein Shapiro LLP**, 1825 Eye Street, NW, Washington, DC 20006-5403, jointly, and each of them severally, my attorneys at law/patent agent(s), with full power of substitution, delegation and revocation, to prosecute this application, to make alterations and amendments therein, to receive the patent, and to transact all business in the U.S. Patent and Trademark Office connected therewith.

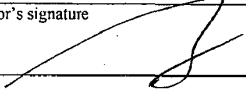
The undersigned hereby authorizes the U.S. attorney or agent named herein to accept and follow instructions from Efficient Power Conversion Corporation as to any action to be taken in the United States Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorney or agent named herein will be so notified by the undersigned.

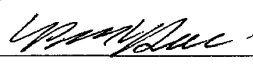
Please mail all correspondence to Stephen A. Soffen, whose address is:

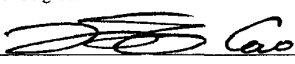
Dickstein Shapiro LLP
1825 Eye Street, NW
Washington, DC 20006-5403

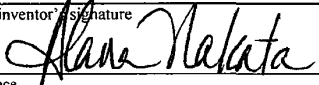
Please direct telephone calls to: Stephen A. Soffen at (202) 420-4879.

Please direct facsimiles to: (202) 420-2201

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Sole or first inventor's signature 	Date 4/6/11
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Second inventor's signature 	Date 4/6/2010
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Citizenship US	
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Third inventor's signature 	Date 4/6/2010
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Fourth inventor's signature 	Date 4/6/2010
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Fifth inventor's signature <i>Guang Yuan Zhao</i>	Date 4/6/2016
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Citizenship China	
Mailing Address 20606 Anza Ave. #19 Torrance, California 90503	

Full name of sixth inventor, if any	
Sixth inventor's signature	Date
Residence	
Citizenship	
Mailing Address	

Full name of seventh inventor, if any	
Seventh inventor's signature	Date
Residence	
Citizenship	
Mailing Address	

Full name of eighth inventor, if any	
Eighth inventor's signature	Date
Residence	
Citizenship	
Mailing Address	

Docket No.: E0101.0008/P008
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alexander Lidow et al.

Application No.: Not Yet Assigned

Confirmation No.: N/A

Filed: April 7, 2010

Art Unit: N/A

For: COMPENSATED GATE MISFET AND
METHOD FOR FABRICATING THE SAME

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

In accordance with 37 CFR 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as

DSMDB-2776919v01

Application No.: Not Yet Assigned

Docket No.: E0101.0008/P008

defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. E0101.0008/P008.

Dated: April 8, 2010

Respectfully submitted,

By 

Stephen A. Soffen

Registration No.: 31,063

DICKSTEIN SHAPIRO LLP

1825 Eye Street, NW

Washington, DC 20006-5403

(202) 420-2200

Attorney for Applicant

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

Inventors:

Alexander Lidow
Robert Beach
Jianjun Cao
Alana Nakata
GuangYuan Zhao

DICKSTEIN SHAPIRO LLP
1825 Eye Street NW
Washington, DC 20006-5403
(202) 420-4879

DSMDB-2772874

COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional Application No. 61/167,792 filed on April 8, 2009, which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to the field of enhancement mode gallium nitride (GaN) transistors. More particularly, the invention relates to an enhancement mode GaN transistor with a compensated GaN layer or a semi-insulating GaN layer below the gate contact and above the barrier layer.

DETAILED DESCRIPTION OF THE INVENTION

[0003] Gallium nitride (GaN) semiconductor devices are increasingly desirable for power semiconductor devices because of their ability to carry large current and support high voltages. Development of these devices has generally been aimed at high power/high frequency applications. Devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFET), high electron mobility transistors (HEMT), or modulation doped field effect transistors (MODFET). These types of devices can typically withstand high voltages, e.g., 100 Volts, while operating at high frequencies, e.g., 100 kHz-10 GHz.

[0004] A GaN HEMT device includes a nitride semiconductor with at least two nitride layers. Different materials formed on the semiconductor or on a buffer layer causes the layers to have different band gaps. The different material in the adjacent nitride layers also causes polarization, which contributes to a conductive two dimensional electron gas (2DEG) region near the junction of the two layers, specifically in the layer with the narrower band gap.

[0005] The nitride layers that cause polarization typically include a barrier layer of AlGa_N adjacent to a layer of Ga_N to include the 2DEG, which allows charge to flow through the device. This barrier layer may be doped or undoped. Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted, i.e. removed, below the gate at zero applied gate bias, the device can be an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

[0006] FIG. 1 illustrates a conventional enhancement mode Ga_N transistor device 100. Device 100 includes substrate 101 that can be composed of silicon (Si), silicon carbide (SiC), sapphire, or other material, transition layers 102 typically composed of Al_N and AlGa_N that is about 0.1 to about 1.0 μm in thickness, buffer material 103 typically composed of Ga_N that is about 0.5 to about 10 μm in thickness, barrier material 104 typically composed of AlGa_N where the Al to Ga ratio is about 0.1 to about 0.5 with thickness from about 0.005 to about 0.03 μm, p-type AlGa_N 105, heavily doped p-type Ga_N 106, isolation region 107, passivation region 108, ohmic contact metals 109 and 110 for the source and drain, typically composed of Ti and Al with a capping metal such as Ni and Au, and gate metal 111 typically composed of a nickel (Ni) and gold (Au) metal contact over a p-type Ga_N gate.

[0007] There are several disadvantages of the conventional Ga_N transistors shown in FIG. 1. One problem is that the leakage current of the gate contact during device conduction is very high due to gate charge injection.

[0008] It therefore would be desirable to provide a MISFET, particularly a Ga_N transistor, that does not leak current during device conduction and that is easier to manufacture.

SUMMARY OF THE INVENTION

[0009] The present invention is directed to a MISFET, such as a GaN transistor, with low gate leakage. In one embodiment, the gate leakage is reduced with a compensated GaN layer below the gate contact and above the barrier layer. In another embodiment, the gate leakage is reduced by employing a semi-insulating layer below the gate contact and above the barrier layer.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0010] FIG. 1 is a cross-section of a prior art transistor.
- [0011] FIG. 2 is a transistor according to an embodiment described herein.
- [0012] FIG. 3 is a cross-sectional view at a stage of processing.
- [0013] FIG. 4 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 3.
- [0014] FIG. 5 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 4.
- [0015] FIG. 6 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 5.
- [0016] FIG. 7 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 6.
- [0017] FIG. 8 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 7.
- [0018] FIG. 9 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 8.
- [0019] FIG. 10 is a transistor according to an embodiment described herein.

[0020] FIG. 11 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 6.

[0021] FIG. 12 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 11.

[0022] FIG. 13 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 12.

[0023] FIG. 14 is a transistor according to an embodiment described herein.

[0024] FIG. 15 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 11.

[0025] FIG. 16 is a transistor according to an embodiment described herein.

DETAILED DESCRIPTION OF THE INVENTION

[0026] FIG. 2 shows a MISFET in the form of GaN transistor 1 according to an embodiment of the present invention. GaN transistor 1 is formed on a substrate 31 that may comprise, for example, silicon Si, silicon carbide SiC or sapphire. Over and in contact with the substrate 31 are transition layers 32. Transition layers 32 may comprise, for example, AlN or AlGa_N, with a thickness of between 0.1 to 1.0μm. A buffer layer 33 separates the transition layers 32 from a barrier layer 34. The buffer layer 33 is preferably formed of InAlGa_N with any concentration of In and Al (including 0% In and/or Al) and has a thickness between 0.5 and 3μm. The barrier layer 34 is formed of AlGa_N and has a thickness between 0.005 and 0.03μm and an Al percentage of about 10% to 50%. Source and drain contacts 35, 36 are disposed over the barrier layer. Source and drain contacts are formed of Ti or Al with a capping metal such as Ni and Au or Ti and TiN. A gate contact 37, formed of for example, Ta, Ti, TiN, W, or WSi₂, and having a thickness of between 0.05 and 1.0μm, is provided between the source and drain contacts. In accordance with the present invention, a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the gate contact 37. Compensated semiconductor layer 38 preferably comprises AlGa_N or Ga_N with a deep level passivated p-type impurity such as, for example, Mg,

Zn, Be, Cd, or Ca. Buffer layer 33 and barrier layer 34 are made of a III Nitride material. A III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ where $x + y \leq 1$.

[0027] Advantageously, the high doping level of compensated layer 38 leads to enhancement mode devices. In addition, using a compensated semiconductor layer 38 leads to low gate leakage during device operation. Finally, the insulating nature of compensated layer 38 reduces the gate capacitance of the device.

[0028] Figures 3-9 describe an example method of manufacturing the GaN transistor 1 shown in FIG. 2. Referring to FIG. 3, the first step is to provide a substrate 31. Referring to FIG. 4, the next step is to nucleate and grow transition layers 32 on top of the substrate 31. Referring to FIG. 5, the next step is to grow a buffer layer 33 over the transistor layer 32. Referring to FIG. 6, the next step is to grow a barrier layer 34 over the buffer layer 33.

[0029] Referring to FIG. 7, the next step is to grow a compensated semiconductor layer 38 over the barrier layer 34. Referring to FIG. 8, the next step is to deposit a gate contact 37 on the compensated semiconductor layer 38. Referring to FIG. 9, the next step is to apply a gate photo mask to etch away the gate contact layer 37, and to etch away the compensated semiconductor layer 38, except the portion beneath gate contact layer 37. The gate photo resist mask is then removed. An additional hydrogen passivation can be performed by exposing the device to ammonia or hydrogen plasma at a high temperature. The final step is to provide the source and drain ohmic contacts 35, 36 over the barrier layer 34, which results in the finished GaN transistor 1 shown in FIG. 2.

[0030] The critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen. The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material. Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art.

[0031] FIG. 10 shows a GaN transistor 2 according to a second embodiment of the present invention. GaN transistor 2 is similar to GaN transistor 1 (FIG. 2), except that GaN transistor 2 has a semi-insulating layer 39 in place of the compensated semiconductor layer 38 (FIG. 2). Semi-insulating layer 39 may comprise, for example, AlGaIn or GaN, with deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni. Additionally, a GaN transistor may have both a semi-insulating layer and a compensated semiconductor layer.

[0032] The second embodiment of the invention has the same advantages as the first embodiment. The high doping of semi-insulating layer 39 leads to enhancement mode devices, the semi-insulating layer 39 leads to low gate leakage during device operation, and the insulating nature of semi-insulating 39 reduces the gate capacitance of the device. In addition, the performance of the device of the second embodiment is not as sensitive to future processing steps involving hydrogen and/or high temperatures.

[0033] The method of manufacturing GaN transistor 2 is the same as the method of manufacturing GaN transistor 1 for the steps shown in FIGS. 3-6. Referring to FIG. 11, the next step in the production of the second embodiment, after the step shown in FIG. 6, is the growth of semi-insulating layer 39 incorporating impurity atoms.

[0034] Referring to FIG 12, the next step is to deposit a gate contact layer 37 on the semi-insulating layer 39. Referring to FIG. 13, the next step is to apply a photo mask to etch away the gate contact layer 37, and to etch away the semi-insulating layer 39, except the portion under gate contact layer 37. The photo resist mask is then removed. The next step is to provide the source and drain ohmic contacts 35, 36 over the barrier layer 34 which results in the finished device 2 shown in FIG. 10.

[0035] The device of the present invention has the following characteristics that distinguish it over the prior art: (1) the capacitance from gate to channel layer when the device is on is lower than in the prior art; (2) the gate bias can be driven much more positive without significant current through the gate (typically, in the prior art, the gate begins to conduct current between 2.5V to 3.5V), which the present invention can be driven to 5V without dramatic gate leakage occurring;

and (3) hole injection from the gate into the channel layer is dramatically reduced relative to the prior art.

[0036] Figure 14 shows a GaN transistor 3 according to the third embodiment of the present invention. GaN transistor 3 is similar to GaN transistor 2, except that a confinement layer is placed above the semi-insulating layer and below the gate contact layer. This confinement layer can be composed of AlGaN, SiN, SiO₂, or other insulating material.

[0037] The method of manufacturing GaN transistor 3 is the same as the method of manufacturing GaN transistor 1 for steps shown in FIGS. 3-6 and GaN transistor 2 for the step shown in FIG. 11. Referring to FIG. 15, the next step is the deposition of an insulating confinement layer 40.

[0038] The third embodiment has the advantage of further reduced gate leakage compared to embodiment 1 or embodiment 2. The disadvantage is a further reduction in conductivity when the device is turned on by applying a positive voltage to the gate contact. A unique advantage of the third embodiment is the creation of a variable threshold voltage device. The confinement layer thickness can be adjusted such that very little leakage occurs under normal operating voltages, such as when the device is turned on and off, usually at 5V applied to the gate for on and 0V applied to the gate to turn the device off. However, at higher biases, current can penetrate through the confinement layer and charge the semi-insulating GaN layer. This charge is then trapped between the barrier layer and the confinement layer. This trapped charge leads to a shift in the voltage at which the device turns on and off. By appropriate application of gate voltage, the device can be changed to a depletion mode device, such that it is on at 0V on the gate. Alternatively, the device can be changed to an enhancement mode device that requires more than the gate drive to turn on, effectively making an open circuit. These two types of devices can be useful when programming an integrated circuit that controls a GaN FET with integrated gate drive.

[0039] FIG. 16 shows a GaN transistor 4 according to a fourth embodiment of the present invention. GaN transistor 4 is similar to GaN transistor 2, except that it has a spacer layer 49 beneath semi-insulating layer 48 and above barrier layer 44. Associated with spacer layer 49, which

is a low Mg region, is a doping offset thickness. The low Mg concentration near the barrier layer reduces the back diffusion into the barrier layer.

[0040] The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described herein. Modifications and substitutions to specific process conditions can be made. Accordingly, the embodiments of the invention are not considered as being limited by the foregoing description and drawings.

CLAIMS

We claim:

1. A column III Nitride transistor comprising:
 - a substrate,
 - a set of III-N transition layers above the substrate,
 - a III-N buffer layer above the set of transition layers,
 - a III-N barrier layer, and
 - a compensated III-N layer above the barrier layer.
2. The transistor of claim 1, wherein the compensated III-N layer contains acceptor type dopant atoms passivated with hydrogen.
3. The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.
4. A column III Nitride transistor comprising:
 - a substrate,
 - a set of III-N transition layers above the substrate,
 - a III-N buffer layer above the set of transition layers,
 - a III-N barrier layer, and
 - a semi-insulating III-N layer above the barrier layer.
5. The transistor of claim 4, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms.

6. The transistor of claim 5 where the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.

7. A column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer,

a semi-insulating III-N layer above the barrier layer, and

a confinement layer above the semi-insulating III-N layer.

8. The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.

9. The transistor of claim 7, wherein the confinement layer is made of SiN, SiO₂, Al₂O₃, HfO₂, Ga₂O₃, or InAlGa₂N.

10. A compensated gate MISFET transistor comprising:

a barrier layer beneath a gate contact,

a drain contact,

a source contact, and

further comprising one of a compensated or semi-insulating III-N layer between the barrier layer and the gate contact.

11. The transistor of claim 10, further comprising a confinement layer above the one of a compensated or semi-insulating III-N layer.

ABSTRACT

A MISFET, such as a GaN transistor, with low gate leakage. In one embodiment, the gate leakage is reduced with a compensated GaN layer below the gate contact and above the barrier layer. In another embodiment, the gate leakage is reduced by employing a semi-insulating layer below the gate contact and above the barrier layer.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008

CONFIRMATION NO. 1573

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

FORMALITIES LETTER



Date Mailed: 04/28/2010

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
 - The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 1,2,10,14,16.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

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The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of \$110 as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$110 for a small entity

- Total additional claim fee(s) for this application is \$110
 - \$110 for 1 independent claims over 3.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/756,906	04/08/2010	2811	462	E0101.0008/P008	11	4

CONFIRMATION NO. 1573

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DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

FILING RECEIPT



OC000000041246210

Date Mailed: 04/28/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

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Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/167,792 04/08/2009

Foreign Applications

If Required, Foreign Filing License Granted: 04/22/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/756,906**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

Preliminary Class

257

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/756,906
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APPLICATION AS FILED – PART I			SMALL ENTITY		OTHER THAN SMALL ENTITY	
	(Column 1)	(Column 2)	RATE (\$)	FEE (\$)		RATE (\$)
FOR		NUMBER FILED				
BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A	82		N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A	270		N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A	110		N/A
TOTAL CLAIMS (37 CFR 1.16(i))	11	minus 20 =	x\$26			x\$52
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4	minus 3 =	x\$110	110		x\$220
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390
			TOTAL	572		TOTAL

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II						SMALL ENTITY		OTHER THAN SMALL ENTITY	
	(Column 1)	(Column 2)	(Column 3)						
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	X =			X =	
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X =			X =	
	Application Size Fee (37 CFR 1.16(s))								
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						N/A			N/A
					TOTAL ADD'T FEE			TOTAL ADD'T FEE	

APPLICATION AS AMENDED – PART II						SMALL ENTITY		OTHER THAN SMALL ENTITY	
	(Column 1)	(Column 2)	(Column 3)						
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)
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	Independent (37 CFR 1.16(h))	*	Minus ***	=	X =			X =	
	Application Size Fee (37 CFR 1.16(s))								
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						N/A			N/A
					TOTAL ADD'T FEE			TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Docket No.: E0101.0008/P008
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alexander Lidow et al.

Application No.: 12/756,906

Confirmation No.: 1573

Filed: April 8, 2010

Art Unit: 2811

For: COMPENSATED GATE MISFET AND
METHOD FOR FABRICATING THE SAME

Examiner: Not known

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS
FILING DATE GRANTED

MS Missing Parts
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Dear Sir:

Responsive to the Notice to File Corrected Application Papers – Filing Date Granted, mailed April 28, 2010, submitted herewith for filing in the captioned application are five replacement sheets of drawings, depicting Figures 1, 2, 10, 14 and 16, in compliance with 37 C.F.R. §§ 1.84 and 1.121(d).

Payment of the required \$110.00 claim fee is being made by credit card. In addition, the Director is authorized to charge any deficiency in the fees filed, asserted to be filed, or which should have been filed herewith, or credit any overpayment, to Deposit Account No. 04-1073, under Order No. E0101.0008/P008.

DSMDB-2802015v1

Application No.: 12/756,906

Docket No.: E0101.0008/P008

An early action on the merits is requested.

Dated: June 17, 2010

Respectfully submitted,

By 

Stephen A. Soffen

Registration No. 31,063

Amy M. Kuo

Registration No. 62,374

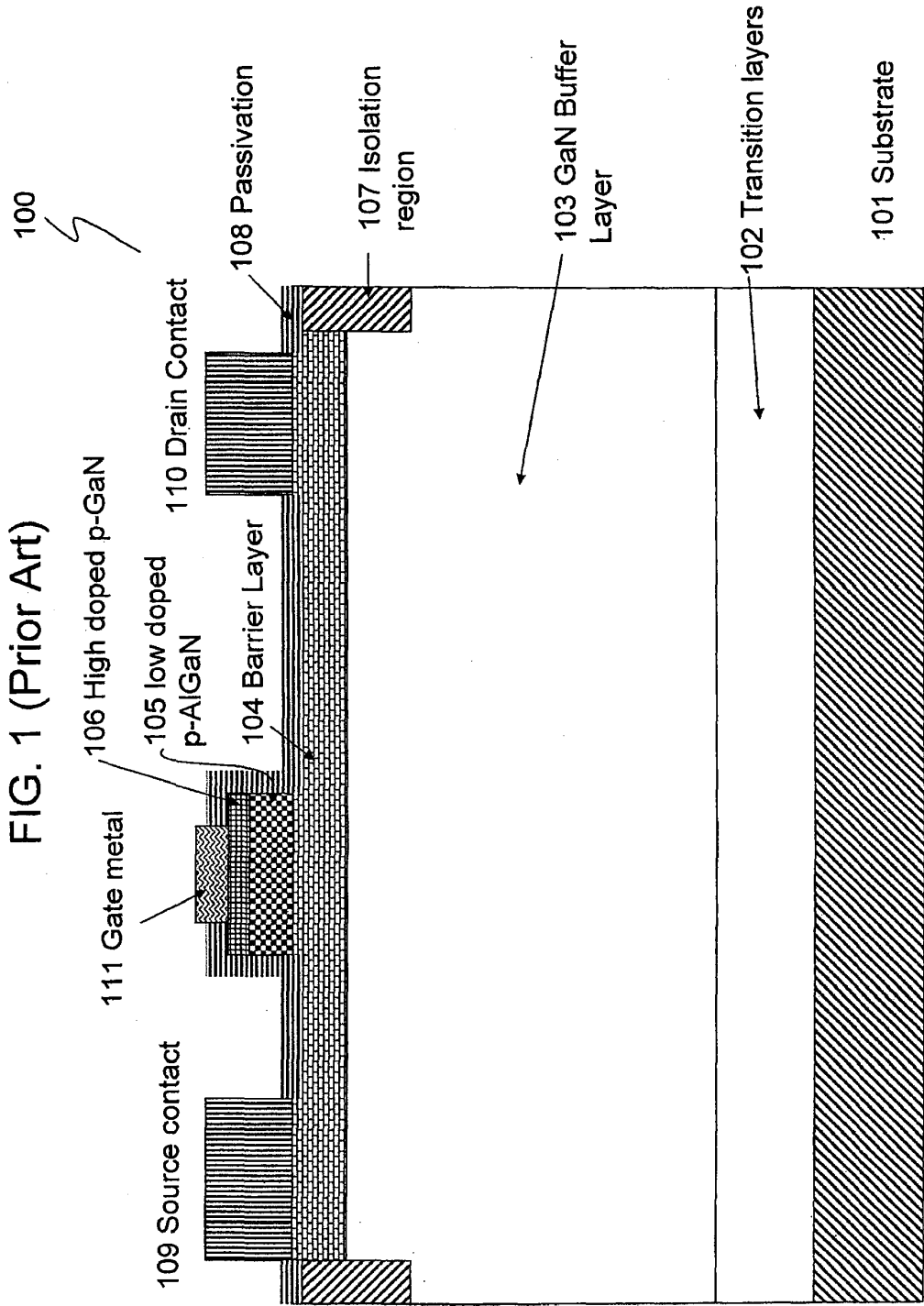
DICKSTEIN SHAPIRO LLP

1825 Eye Street, NW

Washington, DC 20006-5403

(202) 420-2200

Attorneys for Applicants



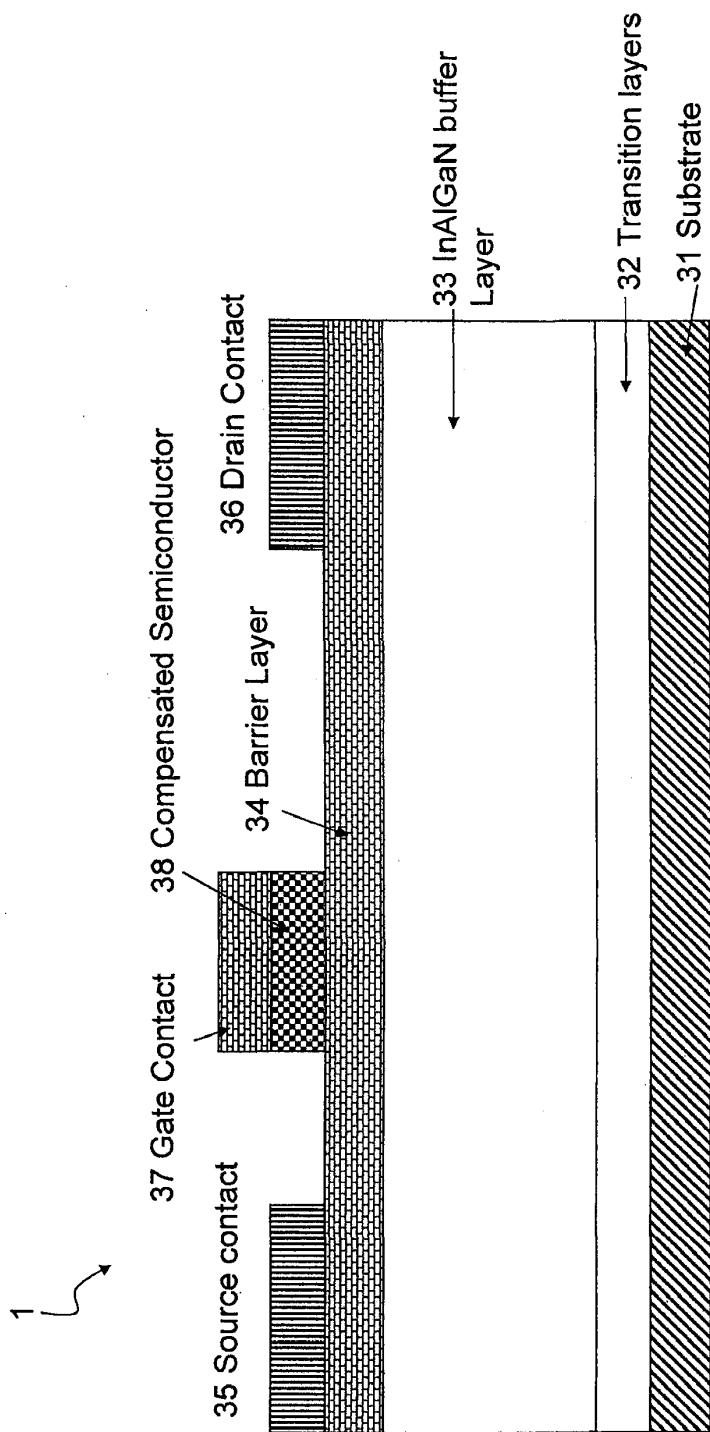


FIG. 2

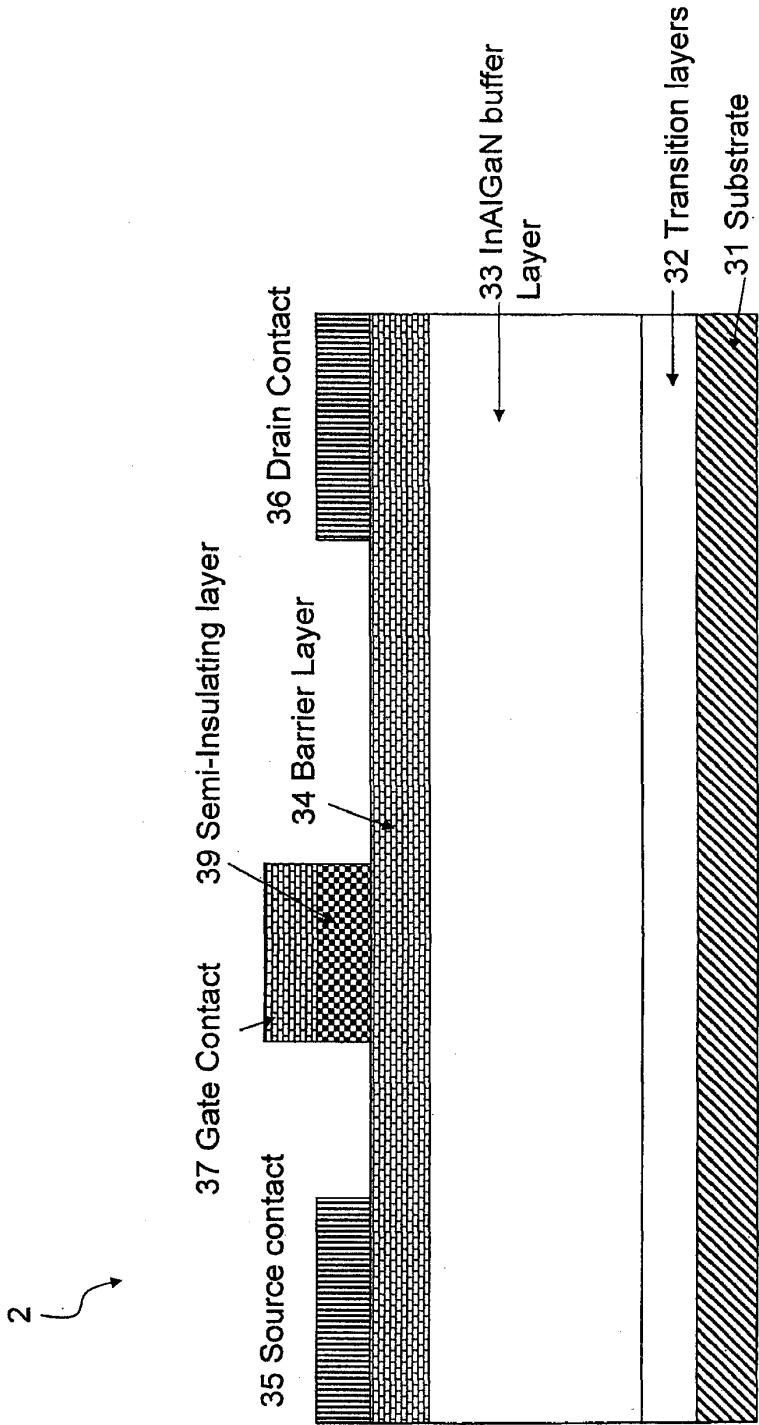


FIG. 10

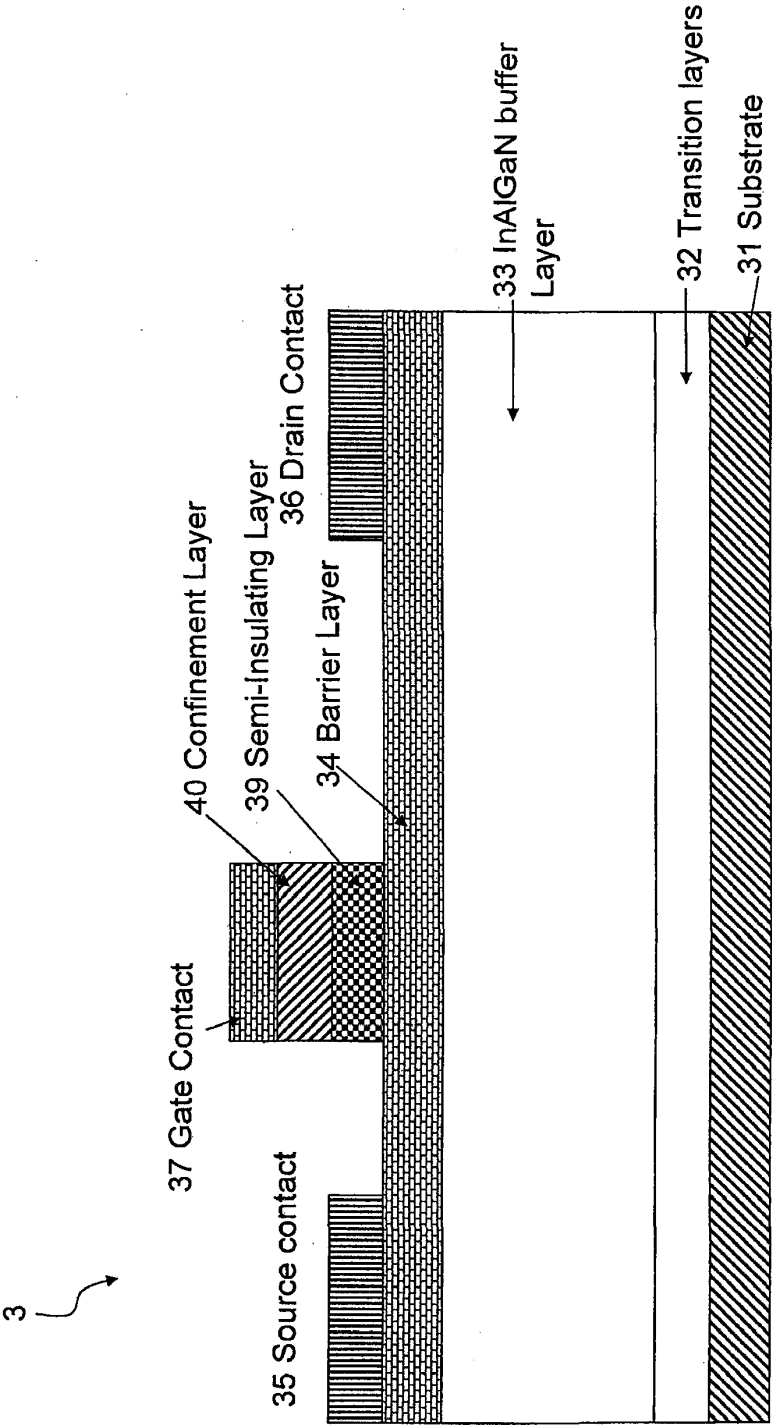


FIG. 14

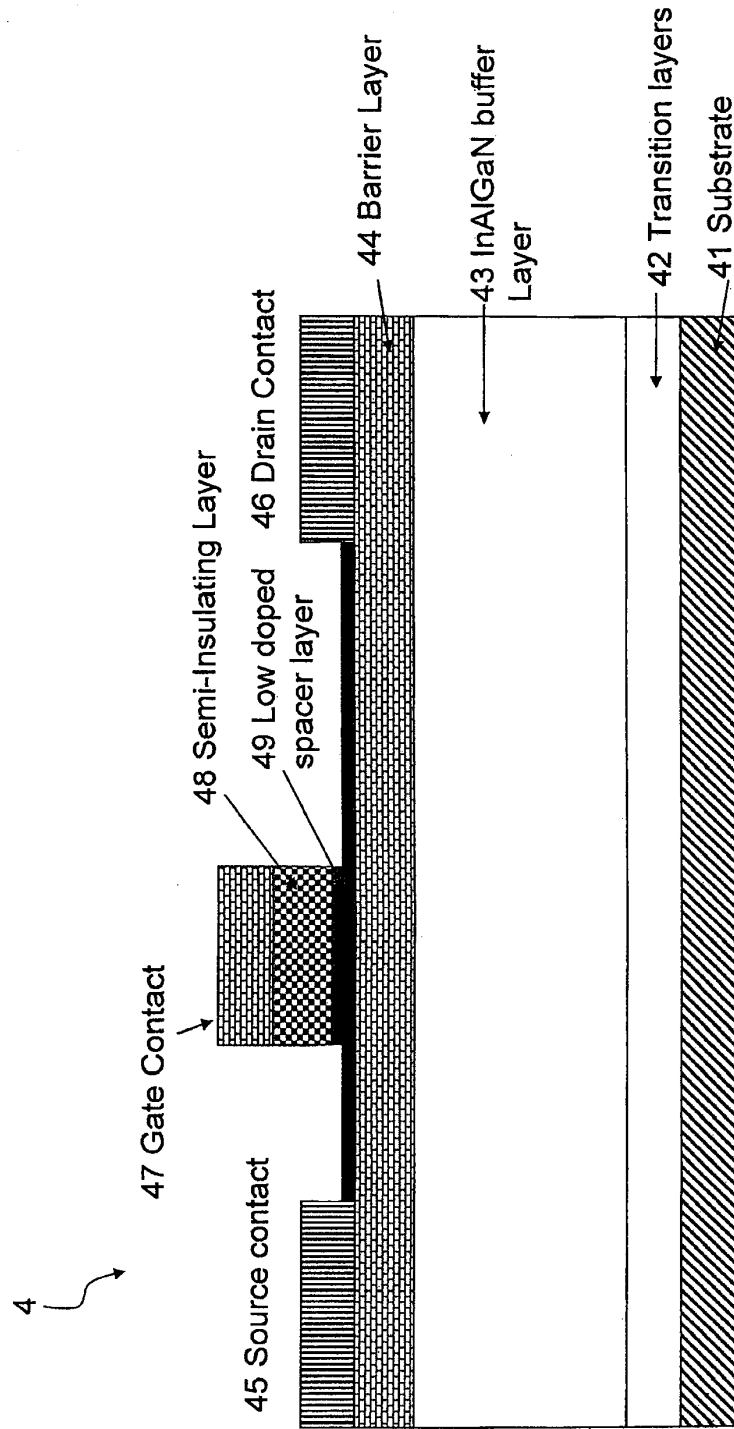


FIG. 16

Electronic Patent Application Fee Transmittal				
Application Number:		12756906		
Filing Date:		08-Apr-2010		
Title of Invention:		COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Alexander Lidow		
Filer:		Mark J. Thronson/robin lamalchaux		
Attorney Docket Number:		E0101.0008/P008		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	2201	1	110	110
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				110

Electronic Acknowledgement Receipt	
EFS ID:	7836353
Application Number:	12756906
International Application Number:	
Confirmation Number:	1573
Title of Invention:	COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Alexander Lidow
Customer Number:	24998
Filer:	Mark J. Thronson/robin lamalchaux
Filer Authorized By:	Mark J. Thronson
Attorney Docket Number:	E0101.0008/P008
Receipt Date:	17-JUN-2010
Filing Date:	08-APR-2010
Time Stamp:	15:08:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$110
RAM confirmation Number	1596
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		Document.pdf	203860 655a522218a25e3d187735e49a9dd7a0ad3db4a9	yes	7
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Response to Pre-Exam Formalities Notice		1	2	
	Drawings-only black and white line drawings		3	7	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30393 7868c170e57d9f615b6d48a4ed07fe9660eb240c	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			234253		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/756,906	04/08/2010	2811	572	E0101.0008/P008	11	4

CONFIRMATION NO. 1573

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

UPDATED FILING RECEIPT



0C000000042273889

Date Mailed: 06/24/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Alexander Lidow, Marina Del Ray, CA;
Robert Beach, La Crescenta, CA;
Jianjun Cao, Torrance, CA;
Alana Nakata, Redondo Beach, CA;
Guang Yuan Zhao, Torrance, CA;

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/167,792 04/08/2009

Foreign Applications

If Required, Foreign Filing License Granted: 04/22/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/756,906**

Projected Publication Date: 10/14/2010

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

page 2 of 3

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	12/756,906-Conf. #1573
				Filing Date	April 8, 2010
				First Named Inventor	Alexander Lidow
				Art Unit	2811
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	E0101.0008/P008

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA*	6,537,838	03-25-2003	Stockman	
	AB*	6,235,547	05-22-2001	Sakuma et al.	
	AC*	4,987,462	01-22-1991	Kim et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference E01010008P008PC	FOR FURTHER ACTION		see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2010/030193	International filing date <i>(day/month/year)</i> 07 April 2010	(Earliest) Priority Date <i>(day/month/year)</i> 08 April 2009	
Applicant EFFICIENT POWER CONVERSION CORPORATION			

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

a. With regard to the **language**, the international search was carried out on the basis of:

- ☒ the international application in the language in which it was filed
☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II)

3. ☐ **Unity of invention is lacking** (see Box No. III)

4. With regard to the **title**,

- ☒ the text is approved as submitted by the applicant
☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

- ☒ the text is approved as submitted by the applicant
☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings**,

- a. the figure of the **drawings** to be published with the abstract is Figure No. 2
☒ as suggested by the applicant
☐ as selected by this Authority, because the applicant failed to suggest a figure
☐ as selected by this Authority, because this figure better characterizes the invention
- b. ☐ none of the figures is to be published with the abstract

Form PCT/ISA/210 (first sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2010/030193

A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - H01L 29/778 (2010.01) USPC - 257/194 According to International Patent Classification (IPC) or to both national classification and IPC												
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC(8) - H01L 29/772, 778, 78 (2010.01) USPC - 257/20, 22, 25, 28, 194, 256, 268 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PatBase, Google Patent												
C. DOCUMENTS CONSIDERED TO BE RELEVANT												
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.										
Y	Applicant's Admitted Prior Art, paragraph 5 figure 1	1-9										
Y	US 6,537,838 B2 (STOCKMAN) 25 March 2003 (25.03.2003) entire document	1-3										
Y	US 6,235,547 B1 (SAKUMA et al) 22 May 2001 (22.05.2001) entire document	4-11										
Y	US 4,987,462 A (KIM et al) 22 January 1991 (22.01.1991) entire document	10-11										
☐ Further documents are listed in the continuation of Box C. ☐												
* Special categories of cited documents: <table border="0"><tr><td>"A" document defining the general state of the art which is not considered to be of particular relevance</td><td>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td></tr><tr><td>"E" earlier application or patent but published on or after the international filing date</td><td>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td></tr><tr><td>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td><td>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td></tr><tr><td>"O" document referring to an oral disclosure, use, exhibition or other means</td><td>"&" document member of the same patent family</td></tr><tr><td>"P" document published prior to the international filing date but later than the priority date claimed</td><td></td></tr></table>			"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family	"P" document published prior to the international filing date but later than the priority date claimed	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention											
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone											
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art											
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family											
"P" document published prior to the international filing date but later than the priority date claimed												
Date of the actual completion of the international search 25 May 2010		Date of mailing of the international search report 03 JUN 2010										
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201		Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774										

Form PCT/ISA/210 (second sheet) (April 2005)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: STEPHEN SOFFEN
DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006-5403

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year)

03 JUN 2010

Applicant's or agent's file reference

E01010008P008PC

FOR FURTHER ACTION

See paragraph 2 below

International application No.
PCT/US2010/030193

International filing date (day/month/year)
07 April 2010

Priority date (day/month/year)
08 April 2009

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 29/778 (2010.01)
USPC - 257/194

Applicant
EFFICIENT POWER CONVERSION CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US
Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-3201

Date of completion of this opinion
25 May 2010

Authorized officer:

Blaine Copenheaver

PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2010/030193

Box No. I Basis of this opinion

1. With regard to the language, this opinion has been established on the basis of:

- ☒ the international application in the language in which it was filed.
☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, this opinion has been established on the basis of:

a. type of material

- ☐ a sequence listing
☐ table(s) related to the sequence listing

b. format of material

- ☐ on paper
☐ in electronic form

c. time of filing/furnishing

- ☐ contained in the international application as filed
☐ filed together with the international application in electronic form
☐ furnished subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2010/030193

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-11	YES
	Claims	None	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-11	NO
Industrial applicability (IA)	Claims	1-11	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1-3 lack an inventive step under PCT Article 33(3) as being obvious over Applicant Admitted Prior Art, hereinafter referred to as AAPA in view of Stockman.

Regarding claim 1, AAPA teaches a column III Nitride transistor (figure 1) comprising: a substrate (101, figure 1), a set of III-N transition layers above the substrate (102, figure 1), a III-N buffer layer above the set of transition layers (103, figure 1), a III-N barrier layer (104, figure 1, paragraph 0005), and a III-N layer above the barrier layer (105, figure 1); yet fails to teach a compensated III-N layer. Stockman teaches GaN based III-V semiconductor devices such as heterojunction bipolar transistors and lowering the resistivity of buried p-type layers (column 1, lines 8-12).

Stockman teaches a compensated III-N layer (column 4, lines 20-30) for the purpose of providing a layer which is p-type and fairly resistive (column 2, lines 21-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of AAPA include the teaching of a compensated III-N layer as taught by Stockman for the purpose of providing a layer which is p-type and fairly resistive as taught by Stockman.

Regarding claims 2-3, AAPA and Stockman teach the transistor of claim 1, wherein AAPA fails to teach the compensated III-N layer contains acceptor type dopant atoms, passivated with hydrogen, selected from the group consisting of Mg, Zn, Be and Ca. Stockman teaches the compensated III-N layer contains acceptor type dopant atoms, passivated with hydrogen, selected from the group consisting of Mg, Zn, Be and Ca (column 4, lines 20-30) for the purpose of providing a layer which is p-type and fairly resistive (column 2, lines 21-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of AAPA include the teaching of the compensated III-N layer contains Mg acceptor type dopant atoms passivated by hydrogen as taught by Stockman for the purpose of providing a layer which is p-type and fairly resistive as taught by Stockman.

Claims 4-9 lack an inventive step under PCT Article 33(3) as being obvious over AAPA in view of Sakuma et al., hereinafter referred to as Sakuma.

Regarding claim 4, AAPA teaches a column III Nitride transistor (figure 1) comprising: a substrate (101, figure 1), a set of III-N transition layers above the substrate (102, figure 1, paragraph 0005), a III-N buffer layer above the set of transition layers (103, figure 1), a III-N barrier layer (104, figure 1, paragraph 0005), and yet fails to teach a semi-insulating III-N layer above the barrier layer.

Sakuma teaches a semiconductor device and structure thereof (abstract).

Sakuma teaches a semi-insulating III-N layer (52, figure 15B, column 19, lines 55-56) above the barrier layer (50, figure 15B, column 19, line 54) for the purpose of improving integration density (column 20, lines 54-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of AAPA include the teaching of a semi-insulating III-N layer above the barrier layer as taught by Sakuma for the purpose of improving the integration density as taught by Sakuma.

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2010/030193

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Regarding claims 5-6, AAPA and Sakuma teach the transistor of claim 4, wherein AAPA fails to teach the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group of C, Fe, Mn, Cr and V.

Sakuma teaches the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group of C, Fe, Mn, Cr and V (Fe doped semi-insulating InP layer 52, column 19, lines 55-56) for the purpose of improving integration density and providing a large P/V ratio (column 20, lines 54-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of AAPA include the teaching of the semi-insulating layer containing deep acceptor Fe atoms as taught by Sakuma for the purpose of improving integration density and providing a large P/V ratio as taught by Sakuma.

Regarding claim 7, AAPA teaches a column III Nitride transistor (figure 1) comprising: a substrate (101, figure 1), a set of III-N transition layers above the substrate (102, figure 1, paragraph 0005), a III-N buffer layer above the set of transition layers (103, figure 1), a III-N barrier layer (104, figure 1, paragraph 0005), yet fails to teach a semi-insulating III-N layer above the barrier layer, and a confinement layer above the semi-insulating III-N layer.

Sakuma teaches a semi-insulating III-N layer (52, figure 15B, column 19, lines 55-56) above the barrier layer (50, figure 15B, column 19, line 54), and a confinement layer (53, figure 15B, column 19, line 62) above the semi-insulating III-N layer (52, figure 15B) for the purpose of improving integration density and providing a large P/V ratio (column 20, lines 54-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of AAPA include the teaching of a semi-insulating III-N layer and a confinement layer as taught by Sakuma for the purpose of improving integration density and providing a large P/V ratio as taught by Sakuma.

Regarding claim 8, AAPA and Sakuma teach the transistor of claim 7, wherein AAPA fails to teach the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.

Sakuma teaches the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V (Fe doped semi-insulating InP layer 52, column 19, lines 55-56) for the purpose of improving integration density and providing a large P/V ratio (column 20, lines 54-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of AAPA include the teaching of the semi-insulating layer containing deep acceptor Fe atoms as taught by Sakuma for the purpose of improving integration density and providing a large P/V ratio as taught by Sakuma.

Regarding claim 9, AAPA and Sakuma teach the transistor of claim 7, wherein AAPA fails to teach the confinement layer is made of SiN, SiO₂, Al₂O₃, HfO₂, Ga₂O₃, or InAlGaN.

Sakuma teaches the confinement layer is made of SiN, SiO₂, Al₂O₃, HfO₂, Ga₂O₃, or InAlGaN (SiO₂ film 53, figure 15B, column 19, line 62) for the purpose of improving integration density and providing a large P/V ratio (column 20, lines 54-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of AAPA include the teaching of the confinement layer being made of SiO₂ as taught by Sakuma for the purpose of improving integration density and providing a large P/V ratio as taught by Sakuma.

Claims 10-11 lack an inventive step under PCT Article 33(3) as being obvious over Kim et al., hereinafter referred to as Kim in view of Sakuma.

Regarding claim 10, Kim teaches a compensated gate MISFET transistor (abstract) comprising: a barrier layer (40, figure 1, column 4, lines 3-4) beneath a gate contact (46, figure 1, column 4, line 6), a drain contact, a source contact (source and drain contacts 48, 50, figure 1, column 4, lines 7-9), and further comprising an insulating layer between the barrier layer and the gate contact (insulator layer 44, figure 1, column 4, line 5) yet fails to teach the layer between the barrier and contact comprising one of a compensated or semi-insulating III-N layer.

Sakuma teaches a semi-insulating III-N layer (52, figure 15B, column 19, lines 55-56) for the purpose of improving integration density and providing a large P/V ratio (column 20, lines 54-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of Kim include the teaching of a semi-insulating layer as taught by Sakuma for the purpose of improving integration density and providing a large P/V ratio as taught by Sakuma.

Regarding claim 11, Kim and Sakuma teach the transistor of claim 10, Kim fails to teach further comprising a confinement layer above the one of a compensated or semi-insulating III-N layer.

Sakuma teaches a confinement layer (53, figure 15B, column 19, line 62) above the one of a compensated or semi-insulating III-N layer (52, figure 15B) for the purpose of improving integration density and providing a large P/V ratio (column 20, lines 54-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of Kim include the teaching of a confinement layer above the semi-insulating layer as taught by Sakuma for the purpose of improving integration density and providing a large P/V ratio as taught by Sakuma.

Claims 1-11 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

Electronic Acknowledgement Receipt	
EFS ID:	8024802
Application Number:	12756906
International Application Number:	
Confirmation Number:	1573
Title of Invention:	COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Alexander Lidow
Customer Number:	24998
Filer:	Stephen A. Soffen/Jamie Alfaro
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0008/P008
Receipt Date:	15-JUL-2010
Filing Date:	08-APR-2010
Time Stamp:	15:46:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		E01010008IDS.PDF	580720	yes	9
			5640d02a2c77339c5f00b87b6a5a1ef428195ae7		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Filed (SB/08)	3	3
	NPL Documents	4	9
Warnings:			
Information:			
Total Files Size (in bytes):		580720	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Docket No.: E0101.0008/P008
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alexander Lidow et al.

Application No.: 12/756,906

Confirmation No.: 1573

Filed: April 8, 2010

Art Unit: 2811

For: COMPENSATED GATE MISFET AND
METHOD FOR FABRICATING THE SAME

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

In accordance with 37 CFR 1.98(a)(2)(ii), Applicants have not submitted copies of U.S. patents and U.S. patent applications.

Applicants are aware of the following documents, cited in a June 3, 2010 International Search Report and Written Opinion for International Application No. PCT/US2010/030193, which

corresponds to the above referenced application. A copy of the International Search Report and Written Opinion is enclosed.

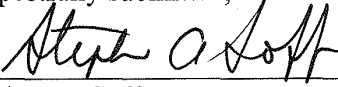
In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. E0101.0008/P008.

Dated: July 15, 2010

Respectfully submitted,

By 

Stephen A. Soffen

Registration No.: 31,063
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008

CONFIRMATION NO. 1573

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

PUBLICATION NOTICE



OC000000043986881

Title:COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

Publication No.US-2010-0258848-A1

Publication Date:10/14/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008	1573

24998	7590	11/09/2011
DICKSTEIN SHAPIRO LLP		
1825 EYE STREET NW		
Washington, DC 20006-5403		

EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2829	

MAIL DATE	DELIVERY MODE
11/09/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/756,906	LIDOW ET AL.	
	Examiner	Art Unit	
	KEVIN QUINTO	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 1-11 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☒ Claim(s) 4-9 is/are allowed.

7) ☒ Claim(s) 1-3, 10 and 11 is/are rejected.

8) ☐ Claim(s) ____ is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☒ The drawing(s) filed on 8 April 2010 and 17 June 2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>7/15/2010, 4/08/2010</u> .	6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh et al (United States Patent Application Publication No. US 2008/0296618 A1) in view of Bowers (USPN 5,985,687) and further in view of Tsuyukuchi et al. ("Low-Leakage-Current Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact," Japanese Journal of Applied Physics, Vol. 45, No. 11, 2006, p. L319-L321).

3. In reference to claim 1, Suh et al. (United States Patent Application Publication No. US 2008/0296618 A1, hereinafter referred to as the "Suh" reference) discloses a similar device. Figure 1(a) of Suh discloses a column III nitride transistor comprising a substrate (110). There is a set of III-N transition layers (108) above the substrate (p. 6, paragraph 90) with a III-N buffer layer (106) above the transition layers (108). There is a III-N layer (104) above the buffer layer (106). Suh does not disclose that the III-N layer (104) is a compensated layer. However Bowers et al. (USPN 5,985,687, hereinafter referred to as the "Bowers" reference) discloses that it is well known in the art that hydrogen passivates or compensates Mg dopants in a GaN material (column 8,

lines 31-35). Furthermore Tsuyukuchi et al. ("Low-Leakage-Current Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact," Japanese Journal of Applied Physics, Vol. 45, No. 11, 2006, p. L319-L321, hereinafter referred to as the "Tsuyukuchi" reference) discloses that the p-type concentration (Mg in the case of Tsuyukuchi) of the gate contact layer determines the operating conditions of an enhancement mode column III nitride transistor (p. L319). Thus Tsuyukuchi makes it clear that the activated p-type dopant in the gate contact layer is a result effective variable. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to adjust the activated p-type dopant, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In view of Bowers and Tsuyukuchi, it would therefore be obvious to use a compensated III-N gate contact layer in order to optimize the operating characteristic of the enhancement mode transistor of Suh.

4. With regard to claim 2, the device of Suh constructed in view of Bowers and Tsuyukuchi has a compensated III-N layer which contains acceptor type dopant atoms passivated by hydrogen.

5. In reference to claim 3, Suh makes it clear the Mg is used as the p-type dopant (p. 4, paragraph 68).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suh et al (United States Patent Application Publication No. US 2008/0296618 A1) in view of

Bowers (USPN 5,985,687) and further in view of Tsuyukuchi et al. ("Low-Leakage-Current Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact," Japanese Journal of Applied Physics, Vol. 45, No. 11, 2006, p. L319-L321).

7. In reference to claim 10, Suh (United States Patent Application Publication No. US 2008/0296618 A1) discloses a similar device. Figure 1(a) of Suh discloses a transistor with barrier layer (106) beneath a gate contact (102). There is a drain contact (122) and a source contact (120). Suh does not disclose that the doped p-type (Mg) layer (104) between the barrier layer (106) and the gate contact (102) is a compensated layer. However Bowers (USPN 5,985,687) discloses that it is well known in the art that hydrogen passivates or compensates Mg dopants in a GaN material (column 8, lines 31-35). Furthermore Tsuyukuchi ("Low-Leakage-Current Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact," Japanese Journal of Applied Physics, Vol. 45, No. 11, 2006, p. L319-L321) discloses that the p-type concentration (Mg in the case of Tsuyukuchi) of the gate contact layer determines the operating conditions of an enhancement mode column III nitride transistor (p. L319). Thus Tsuyukuchi makes it clear that the activated p-type dopant in the gate contact layer is a result effective variable. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to adjust the activated p-type dopant, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In view of Bowers and Tsuyukuchi, it would therefore be

obvious to use a compensated layer between the barrier layer and the gate contact in order to optimize the operating characteristic of the enhancement mode transistor of Suh.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suh et al (United States Patent Application Publication No. US 2008/0296618 A1) in view of Bowers (USPN 5,985,687) and further in view of Tsuyukuchi et al. ("Low-Leakage-Current Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact," Japanese Journal of Applied Physics, Vol. 45, No. 11, 2006, p. L319-L321) as applied to claim 10 above and further in view of Derluyn et al. (United States Patent Application Publication No. US 2008/0006845 A1).

9. In reference to claim 11, neither Suh nor Tsuyukuchi disclose the use of a confinement layer above the compensated layer. However Derluyn et al. (United States Patent Application Publication No. US 2008/0006845 A1, hereinafter referred to as the "Derluyn" reference discloses that adding an additional layer in the form of SiO₂, Al₂O₃, and HfO₂ helps to alleviate high leakage current as well as problems caused by the reaction of the metal with the semiconductor (p. 5, paragraph 48). In view of Derluyn, it would therefore be obvious to use a confinement layer in the form of SiO₂, Al₂O₃, and HfO₂ in the device of Suh constructed in view of Bowers and Tsuyukuchi.

Allowable Subject Matter

10. Claims 4-9 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a column III nitride transistor with a set of III-N transition layers above a substrate, a III-N buffer layer above the III-N transition layers, a III-N barrier layer and a semi-insulating layer above the barrier layer as suggested by the applicant in claims 4 and 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN QUINTO whose telephone number is (571)272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin Quinto/
Examiner, Art Unit 2829

/HA TRAN T NGUYEN/
Supervisory Patent Examiner, Art Unit 2829

Notice of References Cited	Application/Control No. 12/756,906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.	
	Examiner KEVIN QUINTO	Art Unit 2829	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,985,687	11-1999	Bowers et al.	438/46
*	B	US-2008/0006845 A1	01-2008	Derluyn et al.	257/192
*	C	US-2008/0296618 A1	12-2008	Suh et al.	257/190
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Tsuyukuchi et al., "Low-Leakage-Current Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact," Japanese Journal of Applied Physics, 2006, Japan Society of Applied Physics, Vol. 45, No. 11, p. L319-L321
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt date: 04/08/2010

12756906 - GAU: 2829

Used in Lieu of PTO/SB/08A/B
(Based on PTO 10-07 version)

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	~~Not Yet Assigned~~ 12756906		
		Filing Date	April 8, 2010		
		First Named Inventor	Alexander Lidow		
		Art Unit	~~Not Yet Assigned~~ 2829		
		Examiner Name	~~Not Yet Assigned~~ Kevin Quinto		
Sheet	1	of	1	Attorney Docket Number	E0101.0008/P008

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2006/0273347	12-07-2006	Hikita et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ CITE NO.: Those application(s) which are marked with an single asterisk () next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. ² Applicant's unique citation designation number (optional). ³ See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ⁴ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁵ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁶ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST 15 if possible. ⁷ Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		X. Hu, et al. "Enhancement Mode AlGaIn/GaN HFET With Selectively Grown pn Junction Gate", <i>Electronics Letters</i> , Vol 35, No. 8, pp. 753-754, April 13, 2000	
		T. Fuji et al. "High On/Off Ratio in Enhancement-Mode AlxGa1-xN/GaN Junction Heterostructure Field-Effect Transistors with P-Type GaN Gate Contact", <i>Japanese Journal of Applied Physics</i> , Vol. 45, No. 39, pp. L1048-L1050, 2006	
		Y. Uemoto et al. "Gate Injection Transistor (GIT) - A Normally-Off AlGaIn/GaN Power Transistor Using Conductivity Modulation, <i>IEEE Transactions on Electron Devices</i> , Vol. 54, No. 12, pp. 3393-3399, December 2007	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	/Kevin Quinto/	Date Considered	11/03/2011
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KQ/

Used in Lieu of PTO/SB/08A/B
(Based on PTO 10-07 version)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	12/756,906-Conf. #1573
				Filing Date	April 8, 2010
				First Named Inventor	Alexander Lidow
				Art Unit	~~2811~~ 2829
				Examiner Name	~~Not Yet Assigned~~ Kevin Quinto
Sheet	1	of	1	Attorney Docket Number	E0101.0008/P008

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA*	6,537,838	03-25-2003	Stockman	
	AB*	6,235,547	05-22-2001	Sakuma et al.	
	AC*	4,987,462	01-22-1991	Kim et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	/Kevin Quinto/	Date Considered	11/03/2011
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KQ/

<i>Search Notes</i> 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

SEARCHED			
Class	Subclass	Date	Examiner
257	190, 191, 192, 194, 195	11/2/2011	KQ
same as above	same as above	11/3/2011	KQ
same as above	same as above	11/4/2011	KQ
same as above	same as above	11/5/2011	KQ

SEARCH NOTES		
Search Notes	Date	Examiner
EAST BRS	11/1/2011	KQ
EAST BRS	11/3/2011	KQ
EAST BRS	11/4/2011	KQ
EAST BRS	11/5/2011	KQ

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	11/06/2011								
	1	✓								
	2	✓								
	3	✓								
	4	=								
	5	=								
	6	=								
	7	=								
	8	=								
	9	=								
	10	✓								
	11	✓								

Low-Leakage-Current Enhancement-Mode AlGa_xN/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact

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(Received October 28, 2005; accepted January 22, 2006; published online March 10, 2006)

An enhancement-mode AlGa_xN/GaN heterostructure field-effect transistor (HFET) using a p-type GaN gate was fabricated. Its leakage current density was 18.2 μA/mm at a gate–source bias of 0 V and a drain–source bias of 20 V, indicating a good pinched-off operation. [DOI: 10.1143/JJAP.45.L319]

KEYWORDS: GaN, normally off mode, heterojunction field-effect transistor, p-type, pn junction, wide band gap, AlGa_xN/GaN heterostructure

The power density of Si-based power devices is approaching the material limit.¹⁾ GaN-based group III nitride semiconductors are some of the most promising materials for high-voltage, high-power, and high-speed devices, because the breakdown electric field and electron saturation velocity of GaN are about 10-fold and 3-fold larger than those of Si, respectively.²⁾ GaN-based electron devices have received much attention for a variety of high-power and/or high-speed electronics applications such as wireless communications, satellite communications, and inverter systems. In particular, the inverter system is effective for saving energy. Therefore, practical applications of this system are eagerly awaited. In this system, normally off mode devices are strongly desired because of their circuit simplicity and low power consumption. However, most GaN-based devices of this type have been fabricated as depletion-mode (normally on mode) devices to date. Enhancement-mode (normally off mode) devices using a Schottky contact have already been realized.^{3,4)} However, very precise controls of film thickness, etching depth and AlN molar fraction are necessary. Moreover, an increase in built-in voltage using the Schottky contact in such a GaN-based electron device is difficult. On the other hand, a pn junction induces a high built-in voltage greater than 3 V, which causes a full depletion of the device channels at a zero gate bias. Hu *et al.*⁵⁾ fabricated an Al_xGa_{1-x}N/GaN heterostructure field-effect transistor (HFET) by selectively growing a pn junction gate. However, the leakage current at a zero gate–source bias was not negligible. To achieve low-power-consumption circuits, a reduction in the leakage current at a zero gate–source bias is necessary. We consider that the occurrence of the nonnegligible leakage current at a zero gate–source bias is due to the use of regrowth and selective growth techniques.⁶⁾ In this study, we fabricated an Al_xGa_{1-x}N/GaN HFET with a p-GaN gate contact using no regrowth or selective growth techniques. This device is a normally off mode device with a low leakage drain current (I_D) at a zero gate–source bias.

We simulated the device structure with a p-GaN gate contact using SiLENSe 1.0. The key factors in operating the device in the normally off mode are the Mg concentration in p-GaN, residual donor concentration, AlN molar fraction and the thickness of unintentionally doped Al_xGa_{1-x}N. Table I shows the parameters used in the simulation. To

Table I. Parameters used in simulation.

	p-GaN	u-Al _x Ga _{1-x} N	u-GaN
AlN molar fraction	—	$x = 0.10, 0.22, 0.40$	—
Mg concentration (cm ⁻³)	3×10^{19}	—	—
Donor concentration (cm ⁻³)	—	1×10^{17}	1×10^{16}
Dielectric constant	8.9	8.86 ($x = 0.10$)	8.9
		8.812 ($x = 0.22$)	
		8.74 ($x = 0.40$)	
Energy gap (eV)	3.4	3.59 ($x = 0.10$)	3.4
		3.8444 ($x = 0.22$)	
		4.28 ($x = 0.40$)	
Spontaneous polarization (C/m ²) ⁸⁾	-0.029	-0.0368621 ($x = 0.10$)	-0.029
		-0.0469967 ($x = 0.22$)	
		-0.0636444 ($x = 0.40$)	
Electron effective mass	0.2	0.205 ($x = 0.10$)	0.2
		0.211 ($x = 0.22$)	
		0.22 ($x = 0.40$)	
Hole effective mass	1.7	1.81 ($x = 0.10$)	1.7
		1.942 ($x = 0.22$)	
		2.14 ($x = 0.40$)	

fabricate a high-performance normally off mode HFET, an increase in the Mg concentration in p-GaN and a reduction in the residual donor concentration in unintentionally doped Al_xGa_{1-x}N are necessary. However, they cannot be controlled beyond a certain limit when nitrides are grown by metalorganic vapor-phase epitaxy. In general, it is thought that the residual donor concentration in unintentionally doped Al_xGa_{1-x}N is limited to be approximately 1×10^{17} cm⁻³. Moreover, when the Mg concentration in p-GaN is increased beyond 3×10^{19} cm⁻³, the crystalline quality of the layer deteriorates. Hence, in our simulation, the Mg and donor concentrations resulting from unintentional doping were fixed at 3×10^{19} and 1×10^{17} cm⁻³, respectively. Moreover, when we consider the feasibility of a device process such as etching, to realize a normally off mode HFET, an Al_xGa_{1-x}N layer thicker than the p-GaN layer is desirable. Therefore, the thicknesses of the Al_xGa_{1-x}N and p-GaN layers were fixed at 15 and 7 nm, respectively. Simulation results show that the device operates in the

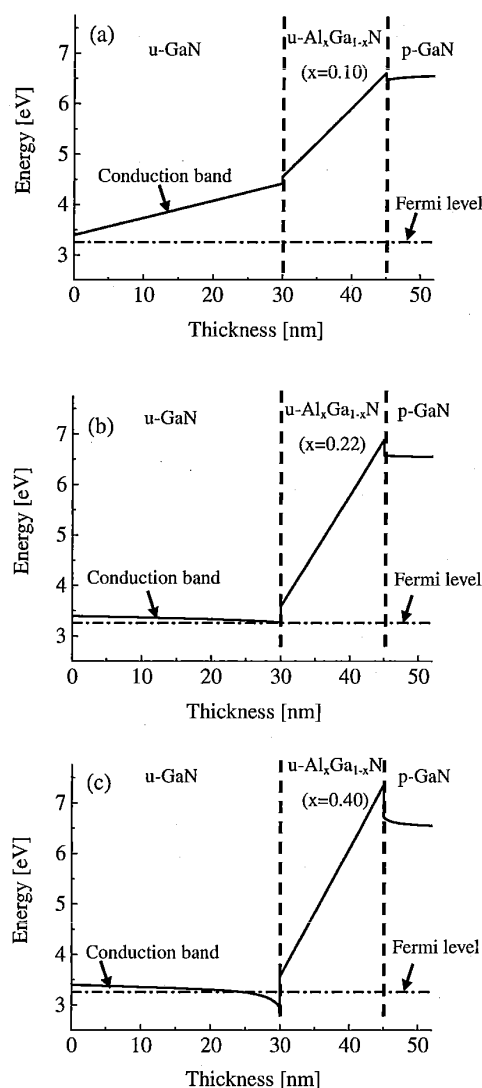


Fig. 1. Simulated conduction band diagrams near gates with AlN molar fractions of 0.10, 0.22, and 0.40 in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer.

normally off mode when the AlN molar fraction and thickness of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ are approximately 0.22 and 15 nm, respectively. Figures 1(a)–1(c) show conduction band diagrams near gates with AlN molar fractions of (a) 0.10, (b) 0.22, and (c) 0.40 in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer. Polarization electric field increases with AlN molar fraction and the device does not operate in the normally off mode. Hence, to fabricate a normally off mode device, it is essential to keep the AlN molar fraction less than 0.22. In this study, to realize the normally off mode operation, we fabricated devices with an $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer with an AlN molar fraction of approximately 0.07, which is much lower than the 0.22 estimated by the simulation.

Figure 2 shows the schematic device structure. The device was grown on a sapphire (0001) substrate by metalorganic vapor-phase epitaxy. The device consists of a low-temper-

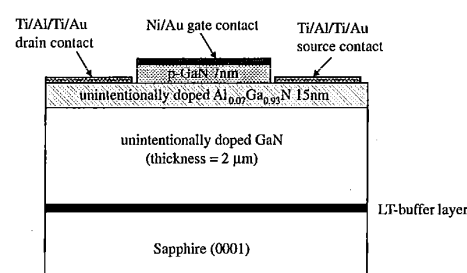


Fig. 2. Schematic device structure. The device consists of a low-temperature buffer layer, a 2- μm -thick unintentionally doped GaN layer, a 15-nm-thick unintentionally doped $\text{Al}_{0.07}\text{Ga}_{0.93}\text{N}$ layer, and a 7-nm-thick Mg-doped p-GaN layer (Mg concentration: $\sim 3 \times 10^{19} \text{ cm}^{-3}$).

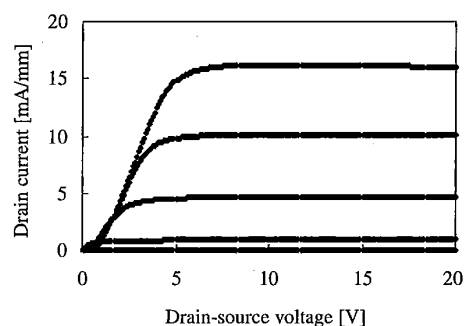
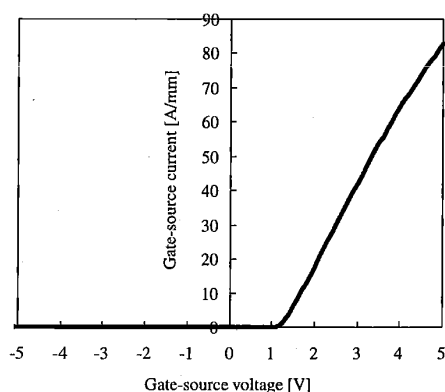


Fig. 3. I - V characteristic of I_D dependence on drain-source bias voltage. The gate-source bias was varied from 0 to 1.2 V with an interval of 0.3 V.

ature buffer layer,⁶⁾ a 2- μm -thick unintentionally doped GaN layer, a 15-nm-thick unintentionally doped $\text{Al}_{0.07}\text{Ga}_{0.93}\text{N}$ layer, and a 7-nm-thick Mg-doped p-GaN layer with a Mg concentration of $3 \times 10^{19} \text{ cm}^{-3}$. The hole concentration in the p-GaN layer was $1 \times 10^{18} \text{ cm}^{-3}$ at room temperature. After the activation of Mg acceptors at 800 °C for 5 min, mesa isolation was performed by Cl_2 reactive ion etching (RIE). Next, a Ni/Au ohmic contact was deposited as a gate contact on p-GaN; then another area of p-GaN was etched by RIE. Subsequently, the source and drain contacts on AlGaN were fabricated as Ti/Al/Ti/Au. The devices had a gate length of 2 μm , a gate width of 100 μm , and an interval of 8 μm between the drain and the source.

Figure 3 shows the current-voltage (I - V) characteristic of the I_D dependence on drain-source bias voltage. Gate-source bias was varied from 0 to 1.2 V with an interval of 0.3 V. The leakage current density was 18.2 $\mu\text{A/mm}$ at a gate-source bias of 0 V and a drain-source bias of 20 V, indicating a good pinched-off operation. Thus, the normally off mode operation was realized in this device. The I_D was 16.0 mA/mm at a gate-source bias of 1.2 V and a drain-source bias of 20 V. The gate leakage was negligibly small in this gate-source bias as shown in Fig. 4.

Figure 4 shows the I - V characteristic of the gate current (I_G) dependence on gate bias voltage. The on voltage (V_{ON}) determined from this I - V characteristic was approximately 1 V. Therefore, the sweeping range of gate bias voltage was limited to less than 1 V. This value is lower than the built-in

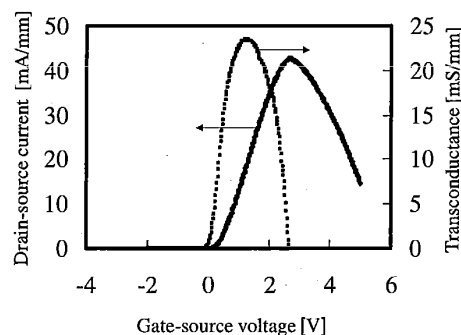
Fig. 4. I - V characteristic of I_G dependence on gate-source bias voltage.

voltage of the pn junction in nitrides. In this device, the thickness of the p-type GaN layer is less than the minority carrier diffusion length, which was reported to be about 200 nm in GaN with a Mg doping concentration of $3 \times 10^{19} \text{ cm}^{-3}$.⁷⁾ When the p-type GaN layer is thicker than 200 nm, we can expect a much wider sweeping range of gate-source bias voltage and a higher I_D .

As reference, an HFET with a Schottky gate contact was also fabricated. The Schottky gate HFET had precisely the same structure as the p-GaN gate HFET except for the gate. The I_D of the Schottky gate HFET was 142.0 mA/mm at a gate-source bias of 2.0 V and a drain-source bias of 20 V. The I_D of the p-GaN gate HFET was about one order of magnitude lower than that of the Schottky gate HFET. In the p-GaN gate HFET, gate leakage limits the sweeping range of gate voltage, thus limiting I_D . There is also another possibility that the AlGaIn layer was partially etched when the p-GaN layer was etched by RIE to fabricate the source and drain contacts. Therefore, this AlGaIn layer may be thinner than that in Schottky gate HFET. The source resistance of the p-GaN gate HFET was higher than that of the Schottky gate HFET. The on-resistances of the p-GaN and Schottky gate HFETs were 461.0 and 29.9 $\Omega \cdot \text{mm}$, respectively.

We can expect higher I_{DS} if we grow much thicker p-GaN and achieve a more accurate etching of the p-GaN layer simultaneously.

Figure 5 shows the I - V characteristics of the transconductance and I_D dependences on gate-source bias voltage. The threshold voltage determined from these I - V characteristics was 0.05 V. The maximum transconductance

Fig. 5. I - V characteristics of transconductance and I_D dependences on gate-source bias voltage.

was 23.4 mS/mm.

We fabricated an enhancement-mode AlGaIn/GaN HFET using a p-type GaN gate contact. The device consisted of a 2- μm -thick unintentionally doped GaN layer, a 15-nm-thick unintentionally doped $\text{Al}_{0.07}\text{Ga}_{0.93}\text{N}$ layer, and a 7-nm-thick Mg-doped p-GaN layer (Mg concentration: $\sim 3 \times 10^{19} \text{ cm}^{-3}$). This device exhibits the normally off mode operation. Its leakage current density was 18.2 $\mu\text{A}/\text{mm}$ at a gate-source bias of 0 V and a drain-source bias of 20 V, indicating a good pinched-off operation. Its maximum transconductance was 23.4 mS/mm.

Acknowledgements

This work was partly supported by the Ministry of Education, Culture, Sports, Science and Technology (Contracts Nos. 15206003 and 17650155) and Akasaki Research Center in Nagoya University.

- 1) Y. Ohno: FED Review 1 (2001) 13 [in Japanese].
- 2) H. Okumura: Oyo Buturi 73 (2004) 315 [in Japanese].
- 3) J. S. Moon, D. Wong, T. Hussain, M. Micovic, P. Deelman, M. Hu, M. Antcliffe, C. Ngo, P. Hashimoto and L. McCray: Conf. Dig. 60th Device Research Conf., 2002, p. 23.
- 4) A. Endoh, Y. Yamashita, K. Ikeda, M. Higashiwaki, K. Hikosaka, T. Matsui, S. Hiyamizu and T. Mimura: Jpn. J. Appl. Phys. 43 (2004) 2255.
- 5) X. Hu, G. Simin, J. Yang, M. Asif Khan, R. Gaska and M. S. Shur: Electron. Lett. 36 (2000) 753.
- 6) H. Amano, N. Sawaki, I. Akasaki and Y. Toyoda: Appl. Phys. Lett. 48 (1986) 353.
- 7) K. Kumakura, T. Makimoto, N. Kobayashi, T. Hashizume, T. Fukui and H. Hasegawa: Appl. Phys. Lett. 86 (2005) 052105.
- 8) V. Fiorentini, F. Bernardini and O. Ambacher: Appl. Phys. Lett. 80 (2002) 1204.

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S10	3	S8 and S9	US-PGPUB; USPAT	OR	ON	2011/11/01 18:04
S11	38	S9 and (gate near (p\$1type or (p adj type)))	US-PGPUB; USPAT	OR	ON	2011/11/01 18:06
S25	20	S24 and (iii\$1v or (iii adj v))	US-PGPUB; USPAT	OR	ON	2011/11/01 18:47
S70	16	S69 and (iii\$1v or (iii adj v))	US-PGPUB; USPAT	OR	ON	2011/11/03 21:00
S116	5	S114 and (gan or algan or ingan or (gallium adj nitride))	US-PGPUB; USPAT	OR	ON	2011/11/04 18:38
S145	6	S144 not S143	US-PGPUB; USPAT	OR	ON	2011/11/05 18:20
S200	6	S199 not S197	US-PGPUB; USPAT	OR	ON	2011/11/05 21:41

EAST Search History (Interference)

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Docket No.: E0101.0008/P008
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alexander Lidow et al.

Application No.: 12/756,906

Confirmation No.: 1573

Filed: April 8, 2010

Art Unit: 2829

For: COMPENSATED GATE MISFET AND
METHOD FOR FABRICATING THE SAME

Examiner: Kevin V. Quinto

AMENDMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action mailed on November 9, 2011, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

DSMDB-3027526v1

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer, and

a compensated ~~III-N~~ GaN layer above the barrier layer.
2. (Currently amended) The transistor of claim 1, wherein the compensated ~~III-N~~ GaN layer contains acceptor type dopant atoms passivated with hydrogen.
3. (Original) The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.
4. (Original) A column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer, and

a semi-insulating III-N layer above the barrier layer.
5. (Original) The transistor of claim 4, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms.

6. (Original) The transistor of claim 5 where the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.

7. (Original) A column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer,

a semi-insulating III-N layer above the barrier layer, and

a confinement layer above the semi-insulating III-N layer.

8. (Original) The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.

9. (Original) The transistor of claim 7, wherein the confinement layer is made of SiN, SiO₂, Al₂O₃, HfO₂, Ga₂O₃, or InAlGa₂N.

10. (Currently amended) A compensated gate MISFET transistor comprising:

a III-N barrier layer beneath a gate contact,

a drain contact,

a source contact, and

~~further comprising one of a compensated or a~~ semi-insulating III-N layer between the barrier layer and the gate contact.

11. (Original) The transistor of claim 10, further comprising a confinement layer above the one of a compensated or semi-insulating III-N layer.

REMARKS

Applicants gratefully acknowledge the allowance of claims 4-9. Claims 1, 2 and 10 have been amended. No new matter has been introduced by the amendments. Applicants reserve the right to pursue the original and other claims in this and in other applications.

Claims 1-3, 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Suh in view of Bowers and Tsuyukuchi. The rejection is respectfully traversed.

Claim 1, as amended, recites a column III Nitride transistor comprising a “substrate, a set of III-N transition layers above the substrate, a III-N buffer layer above the set of transition layers, a III-N barrier layer, and a compensated GaN layer above the barrier layer.” Applicants respectfully submit that the cited combination fails to teach or suggest the invention as recited in claim 1.

The Examiner admits that Suh fails to teach a compensated III-N above the barrier layer. Office Action at 2. Accordingly, Suh does not teach or suggest a “compensated GaN layer above [a] barrier layer” as now recited in claim 1. The Examiner attempts to combine Suh with Bowers, motivated by Tsuyukuchi, for the suggestion that a compensated III-N layer is obvious and merely a design choice. Applicants traverse this argument and respectfully submit that Bowers merely states that it is known “that hydrogen passivates the p-type dopants in Mg doped GaN.” Bowers at Col. 8, lines 31-15. Nothing in Bowers, which relates to forming cleaved facets for lasers, teaches or suggests forming a “compensated GaN layer above [a] barrier layer” in a column III Nitride transistor. Tsuyukuchi (not attached to the Office Action) also fails to teach or suggest this limitation. Accordingly, the cited combination fails to teach or suggest all of the limitation recited in claim 1, and claim 1 is submitted to be allowable. Claims 2 and 3 depend from claim 1 and are submitted to be allowable along with claim 1.

Claim 10 as amended recites a compensated gate MISFET transistor comprising “a III-N barrier layer beneath a gate contact, a drain contact, a source contact, and a semi-insulating III-N layer between the barrier layer and the gate contact.” The Examiner has indicated that the recited transistor structure with a “semi-insulating layer above the barrier layer” is allowable (claim 10

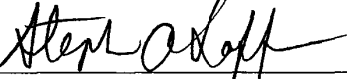
previously recited “one of a compensated or a semi-insulating layer above the barrier layer.”)
Accordingly, Applicants respectfully submit that claim 10, as amended, is allowable over the cited combination. Claim 11 depends from claim 10 and is allowable along with claim 10.

For the above reasons, the § 103 rejection should be withdrawn and the claims allowed.

In view of the above, Applicants believe that the pending application is in condition for allowance.

Dated: February 9, 2012

Respectfully submitted,

By 

Stephen A. Soffen

Registration No.: 31,063

Gianni Minutoli

Registration No.: 41,198

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1825 Eye Street, NW

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Attorneys for Applicants

Electronic Acknowledgement Receipt	
EFS ID:	12042910
Application Number:	12756906
International Application Number:	
Confirmation Number:	1573
Title of Invention:	COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Alexander Lidow
Customer Number:	24998
Filer:	Stephen A. Soffen/Kanessa Howard
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0008/P008
Receipt Date:	09-FEB-2012
Filing Date:	08-APR-2010
Time Stamp:	17:24:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment_Filing.pdf	154078	yes	6
			3673f128fac6662d7c44a6b1d6ef143b035a c75		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	6
Warnings:			
Information:			
Total Files Size (in bytes):		154078	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/756,906		Filing Date 04/08/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	02/09/2012	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 11	Minus ** 20	= 0	X \$30 =	0	OR	X \$ =		
	Independent (37 CFR 1.16(h))	* 4	Minus *** 4	= 0	X \$125 =	0	OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE		
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X \$ =		OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

 Legal Instrument Examiner:
 /RENEE COLLINS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008	1573
24998 7590 04/24/2012 DICKSTEIN SHAPIRO LLP 1825 EYE STREET NW Washington, DC 20006-5403			EXAMINER QUINTO, KEVIN V	
			ART UNIT 2829	PAPER NUMBER
			MAIL DATE 04/24/2012	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Claim Objections

1. Claim 11 is objected to because of the following informalities: claim 11 describes "the one of a compensated or semi-insulating III-N layer" but newly amended parent claim 10 no longer describes the "compensated layer." Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh et al (United States Patent Application Publication No. US 2008/0296618 A1, hereinafter "Suh") in view of Bowers (USPN 5,985,687, hereinafter "Bowers") and further in view of Tsuyukuchi et al. ("Low-Leakage-Current Enhancement-Mode AlGaIn/GaN Heterostructure Field-Effect Transistor Using p-Type Gate Contact," Japanese Journal of Applied Physics, Vol. 45, No. 11, 2006, p. L319-L321, hereinafter "Tsuyukuchi").
4. In reference to claim 1, Suh discloses a similar device. Figure 1(a) of Suh discloses a column III nitride transistor comprising a substrate (110). There is a set of

III-N transition layers (108) above the substrate (p. 6, paragraph 90) with a III-N buffer layer (106) above the transition layers (108). There is a III-N barrier layer (104 or 106, p. 6, paragraph 90). There is a GaN layer (104) above the buffer layer (106). Suh does not disclose that the GaN layer (104) is a compensated layer. However Bowers discloses that it is well known in the art that hydrogen passivates or compensates Mg dopants in a GaN material (column 8, lines 31-35). Furthermore Tsuyukuchi discloses that the p-type concentration (Mg in the case of Tsuyukuchi) of the gate contact layer determines the operating conditions of an enhancement mode column III nitride transistor (p. L319). Thus Tsuyukuchi makes it clear that the activated p-type dopant in the gate contact layer is a result effective variable. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to adjust the activated p-type dopant, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In view of Bowers and Tsuyukuchi, it would therefore be obvious to use a compensated III-N gate contact layer in order to optimize the operating characteristic of the enhancement mode transistor of Suh.

5. With regard to claim 2, the device of Suh constructed in view of Bowers and Tsuyukuchi has a compensated GaN layer which contains acceptor type dopant atoms passivated by hydrogen.

6. In reference to claim 3, Suh makes it clear the Mg is used as the p-type dopant (p. 4, paragraph 68).

Allowable Subject Matter

7. Claim 10 is allowed. Claims 4-9 were allowed in the previous Office action.
8. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a transistor with a III-N barrier layer beneath a gate contact, a drain contact, a source contact, and a semi-insulating layer between the barrier layer and the gate contact as suggested by the applicant in claim 10.
9. Claim 11 would be allowable if amended to overcome the objection raised in the above section titled *Claim Objections*.

Response to Arguments

10. Applicant's arguments filed February 9, 2012 have been fully considered but they are not persuasive. The remarks concerning claims 1-3 have not been found to be persuasive. The applicant argues that the examiner attempted "to combine Suh with Bowers, motivated by Tsuyukuchi, for the suggestion that a compensated III-N layer is obvious and merely a design choice." Bowers was cited to show that is well known in the art that hydrogen passivated or compensates Mg dopants in GaN material. Furthermore the previous Office action as well as the above Office action make it clear that Tsuyukuchi teaches that the amount of activated p-type dopant in the gate contact layer is a result effective variable; it would be obvious to one with ordinary skill in the art to adjust the activated p-type dopant. Therefore claims 1-3 stand rejected.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN QUINTO whose telephone number is (571)272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

Art Unit: 2829

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin Quinto/
Examiner, Art Unit 2829

/HA TRAN T NGUYEN/
Supervisory Patent Examiner, Art Unit 2829

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S256	2	S254 and S255	US-PGPUB; USPAT	OR	ON	2012/04/05 20:31
S257	7	S253 and ((semi\$1insulating or (semi adj (insulating or insulative)) or semi\$1insulative))	US-PGPUB; USPAT	OR	ON	2012/04/05 20:33
S261	3	S260 not (S259 or S258)	US-PGPUB; USPAT	OR	ON	2012/04/05 20:36
S263	3	S262 and ((compensate or compensating or compensation or compensated) with hydrogen)	US-PGPUB; USPAT	OR	ON	2012/04/06 16:39
S265	15	S264 and (hemt)	US-PGPUB; USPAT	OR	ON	2012/04/06 16:45

EAST Search History (Interference)

< This search history is empty >

4/ 7/ 2012 5:47:35 PM

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<i>Index of Claims</i> 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	11/06/2011	04/16/2012												
	1	✓	✓												
	2	✓	✓												
	3	✓	✓												
	4	=	=												
	5	=	=												
	6	=	=												
	7	=	=												
	8	=	=												
	9	=	=												
	10	✓	=												
	11	✓	O												

<i>Search Notes</i> 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

SEARCHED			
Class	Subclass	Date	Examiner
257	190, 191, 192, 194, 195 (text limited)	4/5/2012	KQ
same as above	same as above	4/6/2012	KQ

SEARCH NOTES			
Search Notes		Date	Examiner
EAST BRS		4/5/2012	KQ
EAST BRS		4/6/2012	KQ

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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Docket No.: E0101.0008/P008
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alexander Lidow et al.

Application No.: 12/756,906

Confirmation No.: 1573

Filed: April 8, 2010

Art Unit: 2829

For: COMPENSATED GATE MISFET AND
METHOD FOR FABRICATING THE SAME

Examiner: Kevin V. Quinto

AMENDMENT AFTER FINAL ACTION UNDER 37 C.F.R. 1.116

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated April 24, 2012, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer above the buffer layer, and

a compensated GaN layer above the barrier layer, and

a gate contact above the compensated GaN layer.
2. (Previously presented) The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
3. (Original) The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.
4. (Original) A column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer, and

a semi-insulating III-N layer above the barrier layer.

5. (Original) The transistor of claim 4, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms.

6. (Original) The transistor of claim 5 where the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.

7. (Original) A column III Nitride transistor comprising:

a substrate,

a set of III-N transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer,

a semi-insulating III-N layer above the barrier layer, and

a confinement layer above the semi-insulating III-N layer.

8. (Original) The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.

9. (Original) The transistor of claim 7, wherein the confinement layer is made of SiN, SiO₂, Al₂O₃, HfO₂, Ga₂O₃, or InAlGaN.

10. (Previously presented) A compensated gate MISFET transistor comprising:

a III-N barrier layer beneath a gate contact,

a drain contact,

a source contact, and

a semi-insulating III-N layer between the barrier layer and the gate contact.

11. (Currently amended) The transistor of claim 10, further comprising a confinement layer above the ~~one of a compensated or~~ semi-insulating III-N layer.

12. (New) The transistor of claim 10, further comprising a spacer layer between the semi-insulating layer and the barrier layer.

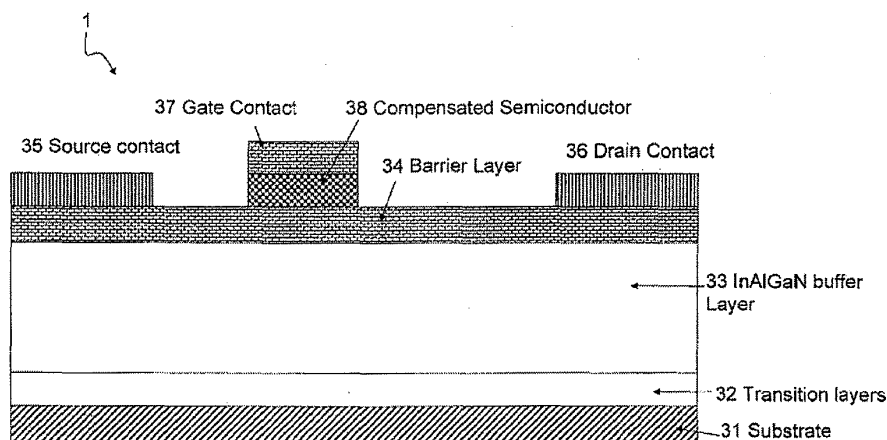
REMARKS

Applicants gratefully acknowledge the allowance of claims 4-10 and the statement that claim 11 contains allowable subject matter. Claims 1 and 11 have been amended. No new matter has been introduced by the amendments. Applicants reserve the right to pursue the original and other claims in this and in other applications.

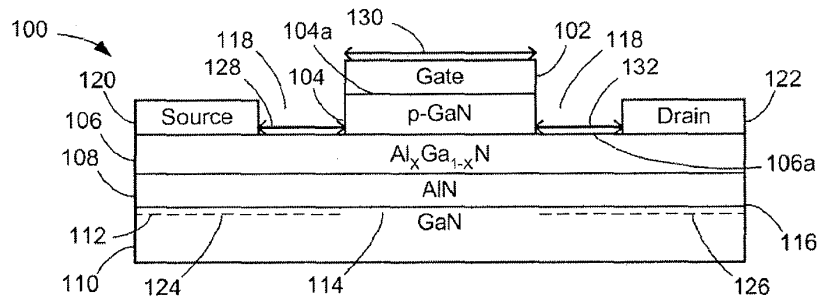
Claim 11 stands objected to based on informalities. Claim 11 has been amended to address the concern raised in the Office Action. As such, the objection should be withdrawn and claim 11 allowed.

Claims 1-3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Suh in view of Bowers and Tsuyukuchi. The rejection is respectfully traversed.

Claim 1 recites a column III Nitride transistor. The claim 1 transistor comprises “a substrate, a set of III-N transition layers above the substrate, a III-N buffer layer above the set of transition layers, a III-N barrier layer, a compensated GaN layer above the barrier layer, and a gate contact above the compensated GaN layer.” An example embodiment of the claim 1 invention is illustrated below.



Applicants respectfully submit that the cited combination fails to teach or suggest the claim 1 transistor. Specifically, Applicants note that the cited combination fails to teach or suggest all of the claimed layers of the claim 1 configuration, which requires “a set of III-N transition layers above [a] substrate, a III-N buffer layer above the set of transition layers, a III-N barrier layer above the buffer layer, a compensated GaN layer above the barrier layer, and a gate contact above the compensated GaN layer.” That is, claim 1 specifically recites **at least four layers** between a “substrate” and a “gate contact.” In contrast, the primary reference Suh, reproduced below, only teaches **three layers** (AlN layer 108, AlGaN layer 106 and p-GaN layer 104) between a substrate (GaN layer 110 according to the Office Action) and gate 102.



This fact is tacitly acknowledged in the Office Action, in which two of Suh’s layers are deemed to meet three separately claimed and specifically arranged layers. That is, according to the Office Action, either layer 104 or layer 106 is the claimed barrier layer, yet layer 106 is also be read on the claimed buffer layer while layer 104 is also being read on the separate GaN layer required to be over the claimed buffer layer. The Examiner relies on Suh ¶ 90 for support of this reading, but Suh ¶ 90 only states:

[a]lso, the p-GaN 104, AlGaN 106, and AlN 108 layers do not have to be abrupt, as they can be gradually graded (in terms of Al composition).
Suh ¶ 90.

Applicants respectfully submit that nothing in this paragraph, or the remainder of Suh or the other cited references for that matter, supports using layers 104 and 106 as *three* separate layers. This is one reason why claim 1 is allowable over the cited combination.

Moreover, Applicants maintain the prior position that the cited combination fails to teach or suggest the claim 1 “compensated GaN layer.” The Examiner continues to combine Suh with Bowers, motivated by Tsuyukuchi, for the suggestion that a compensated III-N layer is obvious and merely a design choice. Applicants traverse this argument and respectfully submit that Bowers merely states that it is known “that hydrogen passivates the p-type dopants in Mg doped GaN.” Bowers at col. 8, lines 31-15. Nothing in Bowers, which relates to forming cleaved facets for lasers, teaches or suggests forming a “compensated GaN layer above [a] barrier layer” in a column III Nitride transistor. Tsuyukuchi also fails to teach or suggest this limitation. This is one more reason why claim 1 is allowable over the cited combination.

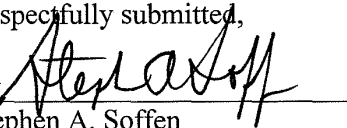
Claims 2 and 3 depend from claim 1 and are allowable along with claim 1. As such, the rejection should be withdrawn and the claims allowed.

New claim 12 depends from allowed claim 10 and is allowable along with claim 10.

In view of the above, Applicants believe that the pending application is in condition for allowance.

Dated: July 24, 2012

Respectfully submitted,

By 

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Registration No.: 31,063

Gianni Minutoli

Registration No.: 41,198

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Attorneys for Applicants

Electronic Acknowledgement Receipt	
EFS ID:	13321250
Application Number:	12756906
International Application Number:	
Confirmation Number:	1573
Title of Invention:	COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Alexander Lidow
Customer Number:	24998
Filer:	Gianni Minutoli/Cheryl deLopez
Filer Authorized By:	Gianni Minutoli
Attorney Docket Number:	E0101.0008/P008
Receipt Date:	24-JUL-2012
Filing Date:	08-APR-2010
Time Stamp:	10:16:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		amendp008.pdf	282652	yes	7
			65c1bc711c7ba103e2d2daee465aa87b126a586		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment After Final	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	7
Warnings:			
Information:			
Total Files Size (in bytes):		282652	
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APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	07/24/2012	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X \$30 =	0	OR	X \$ =	
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$125 =	0	OR	X \$ =	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/AJAY R. DAVID/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008	1573
24998 7590 08/15/2012 DICKSTEIN SHAPIRO LLP 1825 EYE STREET NW Washington, DC 20006-5403			EXAMINER QUINTO, KEVIN V	
			ART UNIT 2829	PAPER NUMBER
			MAIL DATE 08/15/2012	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 12/756,906	Applicant(s) LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 24 July 2012 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires _____ months from the mailing date of the prior Advisory Action or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because:

a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☐ They raise the issue of new matter (see NOTE below);

c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: The new limitations regarding the exact positions of the gate contact and the buffer layer would require a further search. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

STATUS OF CLAIMS

14. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: _____.

Claim(s) withdrawn from consideration: _____.

/HA TRAN T NGUYEN/ Supervisory Patent Examiner, Art Unit 2829	
--	--

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S354	2	S352 not S353	US-PGPUB; USPAT	OR	ON	2012/07/27 15:39
S356	10	S355 and (channel with hydrogen)	US-PGPUB; USPAT	OR	ON	2012/08/02 18:06
S358	32	S357 and (enhancement)	US-PGPUB; USPAT	OR	ON	2012/08/02 21:45
S360	16	S359 and (iii\$1v or (iii adj v))	US-PGPUB; USPAT	OR	ON	2012/08/03 17:49

EAST Search History (Interference)

< This search history is empty >

8/ 3/ 2012 5:59:00 PM

C:\ Users\ kquinto\ Documents\ EAST\ Workspaces\ 12756906.wsp

<i>Search Notes</i> 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

SEARCHED			
Class	Subclass	Date	Examiner
257	190, 191, 192, 194, 195 (text limited)	7/27//2012	KQ
same as above	same as above	8/2/2012	KQ
same as above	same as above	8/3/2012	KQ

SEARCH NOTES			
Search Notes		Date	Examiner
EAST BRS		7/27/2012	KQ
EAST BRS		8/2/2012	KQ
EAST BRS		8/3/2012	KQ

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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Do not enter the AF amendment filed on July 24, 2012. /KQ/

Docket No.: E0101.0008/P008
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Alexander Lidow et al.

Application No.: 12/756,906

Confirmation No.: 1573

Filed: April 8, 2010

Art Unit: 2829

For: COMPENSATED GATE MISFET AND
METHOD FOR FABRICATING THE SAME

Examiner: Kevin V. Quinto

AMENDMENT AFTER FINAL ACTION UNDER 37 C.F.R. 1.116

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated April 24, 2012, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

<i>Index of Claims</i> 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	11/06/2011	04/16/2012	08/03/2012						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	=	=	=						
	5	=	=	=						
	6	=	=	=						
	7	=	=	=						
	8	=	=	=						
	9	=	=	=						
	10	✓	=	=						
	11	✓	O	O						

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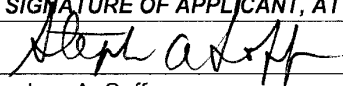
Request for Continued Examination (RCE) Transmittal Address to: Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Application Number	12/756,906-Conf. #1573
	Filing Date	April 8, 2010
	First Named Inventor	Alexander Lidow
	Art Unit	2829
	Examiner Name	Quinto, Kevin V.
	Attorney Docket Number	E0101.0008/P008

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
- a. ☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
- i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ii. ☒ Other Amendment After Final filed on July 24, 2012
- b. ☐ Enclosed
- i. ☐ Amendment/Reply
- iii. ☐ Information Disclosure Statement (IDS)
- ii. ☐ Affidavit(s)/Declaration(s)
- iv. ☐ Other _____
2. **Miscellaneous**
- a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
- b. ☐ Other _____
3. **Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
- a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any Overpayments, to Deposit Account No. 04-1073.
- i. ☒ RCE fee required under 37 CFR 1.17(e)
- ii. ☒ Extension of time fee (37 CFR 1.136 and 1.17)
- iii. ☐ Other _____
- b. ☐ Check in the amount of \$ _____ enclosed
- c. ☒ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED			
Signature		Date	August 24, 2012
Name (Print/Type)	Stephen A. Soffen	Registration No.	31,063

Electronic Patent Application Fee Transmittal				
Application Number:		12756906		
Filing Date:		08-Apr-2010		
Title of Invention:		COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Alexander Lidow		
Filer:		Stephen A. Soffen/Cheryl deLopez		
Attorney Docket Number:		E0101.0008/P008		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	2251	1	75	75

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	2801	1	465	465
Total in USD (\$)				540

Electronic Acknowledgement Receipt	
EFS ID:	13584329
Application Number:	12756906
International Application Number:	
Confirmation Number:	1573
Title of Invention:	COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Alexander Lidow
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl deLopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0008/P008
Receipt Date:	24-AUG-2012
Filing Date:	08-APR-2010
Time Stamp:	15:44:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 540
RAM confirmation Number	2311
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		rcep008.pdf	95839 62d439e1031fd4467385363593ef641f338c24a5	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Request for Continued Examination (RCE)		1	1	
	Extension of Time		2	2	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32093 4ad1ceae28c873d248fdd3bf833a0ac1bf953e5	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			127932		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/756,906		Filing Date 04/08/2010		☐ To be Mailed			
APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY				
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A		OR		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A		OR		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A		OR		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =		OR		X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =		OR		X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.												
APPLICATION AS AMENDED – PART II												
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	08/24/2012	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X \$30 =	0	OR	X \$ =			
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$125 =	0	OR	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

Legal Instrument Examiner:
/DOROTHY BELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

24998 7590 09/14/2012
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER

QUINTO, KEVIN V

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 09/14/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008	1573

TITLE OF INVENTION: COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$870	\$300	\$0	\$1170	12/14/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24998 7590 09/14/2012

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008	1573
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TITLE OF INVENTION: COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$870	\$300	\$0	\$1170	12/14/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
QUINTO, KEVIN V	2829	257-192000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008	1573

24998	7590	09/14/2012
DICKSTEIN SHAPIRO LLP		
1825 EYE STREET NW		
Washington, DC 20006-5403		

EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/14/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 123 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 123 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/756,906	LIDOW ET AL.	
	Examiner	Art Unit	
	KEVIN QUINTO	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 24 August 2012.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-12.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 24, 2012 has been entered.

Allowable Subject Matter

2. Claims 1-3, 11, and 12 are allowed. Claims 4-10 were allowed in previous Office actions.

3. The following is an examiner's statement of reasons for allowance: the examiner is unaware of any prior art which suggests or renders obvious a column III nitride transistor with a set of III-N transition layers above a substrate, a III-N buffer layer above the III-N transition layers, a III-N barrier layer above the buffer layer, a compensated GaN layer above the barrier layer and a gate contact above the compensated GaN layer as suggested by the applicant in claim 1. Claim 11, indicated to be allowable if amended to correct a minor error, has been amended and is thus allowed. The examiner is also unaware of any prior art which suggests or renders obvious a compensated gate MISFET transistor with a III-N barrier layer beneath a gate contact, a

drain contact, a source contact, a semi-insulating III-N layer between the barrier layer and the gate contact, while having a confinement layer above the semi-insulating III-N layer or a spacer layer between the semi-insulating layer and the barrier layer as suggested by the applicant in claims 11 and 12. The allowable subject matter of claims 4, 7, and 10 were discussed in previous Office actions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN QUINTO whose telephone number is (571)272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

Art Unit: 2829

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kevin Quinto/
Examiner, Art Unit 2829

/HA TRAN T NGUYEN/
Supervisory Patent Examiner, Art Unit 2829

<i>Search Notes</i> 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

SEARCHED			
Class	Subclass	Date	Examiner
257	190, 191, 192, 194, 195, E29.001, E29.166, E29.169, E29.226, E29.241-E29.253 (text limited)	9/5/2012	KQ
same as above	same as above	9/7/2012	KQ
same as above	same as above	9/8/2012	KQ

SEARCH NOTES		
Search Notes	Date	Examiner
EAST BRS	9/5/2012	KQ
EAST BRS	9/7/2012	KQ
EAST BRS	9/8/2012	KQ

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	192, E29.242	9/7/2012	KQ
same as above	same as above	9/8/2012	KQ

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UNITED STATES DEPARTMENT OF COMMERCE
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 Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 1573

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/756,906	04/08/2010	257	2829	E0101.0008/P008		
APPLICANTS Alexander Lidow, Marina Del Ray, CA; Robert Beach, La Crescenta, CA; Jianjun Cao, Torrance, CA; /KQ/ Alana Nakata, Redondo Beach, CA; Guang Yuan Zhao, Torrance, CA;						
** CONTINUING DATA ***** This appln claims benefit of 61/167,792 04/08/2009 /KQ/						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED *** SMALL ENTITY ** 04/22/2010						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /KEVIN QUINTO/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 13	TOTAL CLAIMS 11	INDEPENDENT CLAIMS 4
ADDRESS DICKSTEIN SHAPIRO LLP 1825 EYE STREET NW Washington, DC 20006-5403 UNITED STATES						
TITLE COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME						
FILING FEE RECEIVED 572	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S364	16	S363 and (iii\$1v or (iii adj v))	US-PGPUB; USPAT	OR	ON	2012/09/05 20:35
S375	2	S372 not S374	US-PGPUB; USPAT	OR	ON	2012/09/07 22:54
S388	2	S386 and (barrier near2 (semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative))	US-PGPUB; USPAT	OR	ON	2012/09/08 17:58
S396	15	S394 and ((iii\$1v or (iii adj v)))	US-PGPUB; USPAT	OR	ON	2012/09/08 18:09
S398	4	S394 and (gan or ((gallium or indium or aluminum) adj nitride) or gainn or algan or algainn)	US-PGPUB; USPAT	OR	ON	2012/09/08 18:13
S401	9	S400 and (barrier near2 (semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative))	US-PGPUB; USPAT	OR	ON	2012/09/08 18:14
S404	17	S403 and barrier	US-PGPUB; USPAT	OR	ON	2012/09/08 18:20
S413	1	S412 and (gate with ((semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative) adj (layer or film)))	US-PGPUB; USPAT	OR	ON	2012/09/08 18:23
S415	6	S403 and (barrier near2 (layer or film))	US-PGPUB; USPAT	OR	ON	2012/09/08 18:25
S417	1	S416 and (((semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative) adj (layer or film)))	US-PGPUB; USPAT	OR	ON	2012/09/08 18:27
S443	16	S442 and ((semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative) with gate)	US-PGPUB; USPAT	OR	ON	2012/09/08 20:35
S445	3	S444 and ((semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative))	US-PGPUB; USPAT	OR	ON	2012/09/08 20:37
S452	3	S451 and ((semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative))	US-PGPUB; USPAT	OR	ON	2012/09/08 20:46
S453	0	S451 and (barrier with (gate adj (insulating or insulative or insulator)))	US-PGPUB; USPAT	OR	ON	2012/09/08 20:47
S456	6	S455 and ((iii\$1v or (iii adj v)))	US-	OR	ON	2012/09/08

			PGPUB; USPAT			20:48
S470	11	S468 and gate and barrier	US- PGPUB; USPAT	OR	ON	2012/09/08 21:12
S473	3	S472 and (semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative)	US- PGPUB; USPAT	OR	ON	2012/09/08 21:14
S476	20	S475 not S469	US- PGPUB; USPAT	OR	ON	2012/09/08 21:15
S479	31	S478 and nitride and barrier	US- PGPUB; USPAT	OR	ON	2012/09/08 21:17
S483	26	S482 and gate	US- PGPUB; USPAT	OR	ON	2012/09/08 21:27

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S377	28	S376 and (enhancement)	USPAT; UPAD	OR	ON	2012/09/07 22:50
S379	9	S378 and (hemt or hfet or modfet)	USPAT; UPAD	OR	ON	2012/09/07 22:53
S485	7	S484 and (iii\$1v or (iii adj v))	USPAT; UPAD	OR	ON	2012/09/08 17:48
S489	2	S485 and ((semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative))	USPAT; UPAD	OR	ON	2012/09/08 21:20
S493	20	S490 and (iii\$1v or (iii adj v)) and gate not schottky	USPAT; UPAD	OR	ON	2012/09/08 21:36
S495	3	S494 and ((semi\$1insulator or (semi adj (insulating or insulative or insulator)) or semi\$1insulating or semi\$1insulative))	USPAT; UPAD	OR	ON	2012/09/08 21:42

9/ 8/ 2012 10:21:36 PM**C:\ Users\ kquinto\ Documents\ EAST\ Workspaces\ 12756906.wsp**

Issue Classification 	Application/Control No. 12756906	Applicant(s)/Patent Under Reexamination LIDOW ET AL.
	Examiner KEVIN QUINTO	Art Unit 2829

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
257		192				H	0	1	L	29 / 66 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
257	E29.242																	

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
6	6														
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9	9														
10	10														
11	11														
12	12														

/KEVIN QUINTO/ Examiner.Art Unit 2829 (Assistant Examiner)	9/8/2012 (Date)	Total Claims Allowed: 12	
/HA TRAN T NGUYEN/ Supervisory Patent Examiner.Art Unit 2829 (Primary Examiner)	09/09/2012 (Date)	O.G. Print Claim(s) 7	O.G. Print Figure 14

PART B -FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

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DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/756,906	04/08/2010	Alexander Lidow	E0101.0008/P008	1573

TITLE OF INVENTION: COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	yes	\$885.00	\$300.00		\$1,200.00	12/14/2012
EXAMINER		ART UNIT	CLASS-SUBCLASS			
Quinto, K.V.		2829	257-192			

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached.
Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Dickstein Shapiro LLP

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Efficient Power Conversion Corporation

El Segundo, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 5

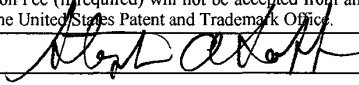
4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 04-1073 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature 
Typed or printed name Stephen A. Soffen

Date December 6, 2012

Registration No. 31,063

Electronic Patent Application Fee Transmittal				
Application Number:		12756906		
Filing Date:		08-Apr-2010		
Title of Invention:		COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Alexander Lidow		
Filer:		Stephen A. Soffen/Kanessa Howard		
Attorney Docket Number:		E0101.0008/P008		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	885	885
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	5	3	15
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	14404532
Application Number:	12756906
International Application Number:	
Confirmation Number:	1573
Title of Invention:	COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Alexander Lidow
Customer Number:	24998
Filer:	Stephen A. Soffen/Kanessa Howard
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0008/P008
Receipt Date:	06-DEC-2012
Filing Date:	08-APR-2010
Time Stamp:	16:57:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1200
RAM confirmation Number	4331
Deposit Account	041073
Authorized User	SOFFEN, STEPHEN A.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	E0101_0008_Issue_Fee_Transmittal.pdf	82940	no	1
			06212c7f1ebbf18bcd3d071718d295edf e672a		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	33676	no	2
			a97c8a877d8e510975f9101f26552e787249 e415		

Warnings:

Information:

Total Files Size (in bytes): 116616

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/756,906	01/08/2013	8350294	E0101.0008/P008	1573

24998 7590 12/18/2012
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 123 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

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Alana Nakata, Redondo Beach, CA;
Guang Yuan Zhao, Torrance, CA;

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