

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD. AND

INNOSCIENCE AMERICA, INC.,

Petitioner

v.

EFFICIENT POWER CONVERSION CORPORATION,

Patent Owner

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Case No. IPR2023- 01381

U.S. Patent No. 8,350,294

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**DECLARATION OF JAMES RICHARD SHEALY, PH.D.**

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**I. INTRODUCTION**

[01] I have been retained by Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively “Innoscience”), as an independent expert for the above-identified inter partes review proceeding involving U.S. Patent No. 8,350,294 (“the ’294 patent”).

[02] I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

[03] Although I am being compensated for my time in connection with this proceeding at my standard hourly consulting rate and reimbursed for reasonable out-of-pocket expenses, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

[04] I have been asked to provide my opinion whether the claims of the ’294 patent would have been obvious to a person of ordinary skill in the art at the time of the earliest claimed priority date of the ’294 patent. In performing my analysis, I have been asked to assume that the priority date is April 8, 2009. My opinions are set forth below.

[05] Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not

intended to suggest that they are the only support for the propositions for which they are cited.

## **II. SUMMARY OF OPINIONS**

[06] This declaration analyses claims 1-12 of the '294 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for my opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

[07] Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of April 8, 2009), it is my opinion that claims 1-12 of the '294 patent would have been obvious based on the asserted grounds discussed below.

## **III. QUALIFICATIONS AND BACKGROUND**

[08] I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A.

[09] I am competent to write this Declaration.

[010] I have been involved in the science and engineering of high-power compound semiconductor transistors for over 40 years. I have been deeply involved in the research and design of III-V compound semiconductor devices over

the course of my career. I have been a Professor at Cornell University, School of Electrical and Computer Engineering, and have been teaching and conducting research at Cornell since 1987. In 2022, I was granted emeritus status.

[011] I received a B.S. degree from North Carolina State University in 1978, a M.S. from Rensselaer Polytechnic Institute in 1980, and a Ph.D. from Cornell University in 1983. I joined the Cornell faculty in 1987. And I am currently a Full Professor at Cornell's School of Electrical and Computer Engineering.

[012] In 1978, I joined the technical staff of General Electric's Corporate Research and Development Center under an Edison Fellowship. While there, among other work, I developed GaAs epitaxial materials for high voltage electronics. I was the inventor of two patents on Vertical Field Effect Transistors.

[013] In 1980, I transferred to General Electric's Advanced Electronics Laboratory where I developed materials and processes for the fabrication of AlGaAs LEDs as well as developing an OMVPE (also known as MOCVD) reactor and related processes for the fabrication of AlGaAs quantum well laser diodes. In 1985, I was designated Principal Staff Scientist at General Electric in recognition of my research contributions.

[014] While at General Electric, I was also concurrently working at Cornell. In 1984, my group at Cornell developed the first single quantum well red laser by

Organometallic Vapor-Phase Epitaxy (“OMVPE”), a technique used for growing semiconductor crystals. The fabrication of these devices involved multi-level metallization and dielectric passivation.

**[015]** I joined the Cornell faculty in 1987 as a Professor of Electrical and Computer Engineering (ECE) and Materials Science and Engineering (MSE). While at Cornell I have continued my research in OMVPE, particularly as it relates to high frequency transistors, LEDs, and laser diodes. I have also researched GaN and related materials for both high-power transistors and LEDs.

**[016]** In 1997, I was named the Director of Cornell's Optoelectronics Technology Center. In 1998, I was promoted to full professor at Cornell. I have published over 120 articles and am the inventor of over 19 patents, many of which deal with GaN-based materials and devices. Over the years, I have received numerous teaching awards for delivering quality instruction to undergraduates in Materials Science and Electrical Engineering.

**[017]** In 1998-99, the research group that I led invented and patented a single temperature method for nucleation and growth of GaN materials on sapphire, SiC, and Si substrates. This technique has become the preferred method for growing GaN-based transistors and LED today. This nucleation method was used to grow AlN/GaN layers on silicon. By mid-1999, my research group had

produced a gallium nitride-on-silicon (GaN-Si) RF transistor, a technology currently used by several GaN companies for high efficiency power convertors and RF amplifiers.

**[018]** By the early 2000s, my research group produced the first RF integrated circuits with gallium nitride-on-silicon carbide (GaN on SiC) transistors including X Band VCOs, TR switches, frequency doublers, and internally matched power amplifiers. By 2008, my group discovered a new passivation technology (LPCVD of AlSiN, patented) for GaN-based FETs which, when applied to GaNSiC HEMTs, produced the largest power density operation (over 18 Watts/mm at 10 GHz) ever observed on submicron gated devices. These devices also delivered record power-added-efficiencies and linear gain during 10 GHz operation (PAE > 65 %, Gain > 36 dB at 60 V bias). These benchmarks remain unchallenged today.

**[019]** In 2015, I cofounded Akoustis Technology (AKTS on the NASDAQ), a company which manufactures AlN bulk acoustic wave filters which are required for 5G communications. In 2019, I cofounded Odyssey Semiconductor, a company which is developing GaN Vertical field effect transistors for the emerging power convertor market. Odyssey Semiconductor also recently developed the fabrication techniques and built micro-LED Arrays in both AlGaInP and AlGaInN materials.

[020] I have remained current in the field, as evidenced by my publications listed in my curriculum vitae.

[021] I have also served as an expert in certain legal proceedings relating to GaN transistors, including materials growth, device fabrication, and packaging. A list of cases in which I have testified at trial, hearing, or by deposition is provided in my curriculum vitae.

#### IV. MATERIALS CONSIDERED

[022] In forming my opinions, I read and considered the '294 patent and its prosecution history, the exhibits listed in the Exhibit List filed with the petition for *inter partes* review of the '294 patent, as well as any other materials referenced herein. I have reviewed the following at least the following documents:

| Exhibit  | Description                                                                                     |
|----------|-------------------------------------------------------------------------------------------------|
| Ex. 1001 | U.S. Patent No. 8,350,294 B2 to Lidow et al. ("the '294 patent")                                |
| Ex. 1002 | Prosecution History of the '294 Patent (" <i>Prosecution History</i> ")                         |
| Ex. 1005 | U.S. Patent Application Publication No. US 2007/0164315 A1 to Smith et al. (" <i>Smith</i> ")   |
| Ex. 1006 | U.S. Patent Application Publication No. US 2008/0087915 A1 to Uemoto et al. (" <i>Uemoto</i> ") |
| Ex. 1007 | Japanese Patent Publication No. JP2006-253224 A to Kigami et al.                                |

| Exhibit  | Description                                                                                                                                                                                     |
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| Ex. 1008 | Certified English Translation of Japanese Patent Publication No. JP2006-253224 A (“ <i>Kigami</i> ”)                                                                                            |
| Ex. 1009 | Translator’s Declaration for Certified English Translation of JP 2006-253224 A to Kigami et al.                                                                                                 |
| Ex. 1010 | Umesh K. Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, vol. 90, no. 6 (June 2002), pp. 1022-1031 (“ <i>Mishra</i> ”).      |
| Ex. 1011 | Excerpts of Rüdiger Quay, <i>Gallium Nitride Electronics</i> , vol. 96, Springer Science & Business Media (2008) (“ <i>Quay</i> ”).                                                             |
| Ex. 1012 | Excerpts of Stephen J. Pearton et al., <i>Gallium Nitride Processing for Electronics, Sensors and Spintronics</i> , Springer Science & Business Media (2006) (“ <i>Pearton</i> ”).              |
| Ex. 1013 | U.S. Patent Application Publication No. US 2004/0012015 A1 to Saxler (“ <i>Saxler015</i> ”)                                                                                                     |
| Ex. 1014 | X. Hu et al., <i>Enhancement mode AlGaIn/GaN HFET with selectively grown pn junction gate</i> , Electronics Letters, vol. 36, no. 8 (2000), pp. 753-754 (“ <i>Hu</i> ”).                        |
| Ex. 1015 | Excerpts of Chang Soo Suh, Enhancement-Mode GaN-Based HEMTs for High-Voltage Switching Applications (Dec. 2008) (Ph.D. dissertation, University of California, Santa Barbara) (“ <i>Suh</i> ”). |
| Ex. 1016 | U.S. Patent Application Publication No. US 2005/0145874 A1 to Saxler (“ <i>Saxler874</i> ”)                                                                                                     |
| Ex. 1017 | Chris G. Van de Walle et al., “Hydrogen in III-V Nitrides,” <i>Semiconductors and Semimetals</i> , vol. 57 (1998), pp. 157-184 (“ <i>Van de Walle</i> ”).                                       |

| Exhibit  | Description                                                                                                                                                                                                                                                                                                                                   |
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| Ex. 1018 | Shuji Nakamura et al., <i>Hole Compensation Mechanism of P-Type GaN Films</i> ,” Japanese Journal of Applied Physics, vol. 31 (1992), pp. 1258-1266 (“ <i>Nakamura</i> ”).                                                                                                                                                                    |
| Ex. 1019 | Complainant’s Proposed Constructions & Respondents’ Proposed Constructions in related International Trade Commission investigation: <i>In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same</i> , Inv. No. 337-TA-1366, dated September 5, 2023 (“ <i>ITC Constructions</i> ”). |
| Ex. 1020 | U.S. Patent No. 5,985,687 to Bowers et al. (“ <i>Bowers</i> ”)                                                                                                                                                                                                                                                                                |
| Ex. 1021 | U.S. Patent Application Publication No. 2002/0167023 A1 to Chavarkar et al. (“ <i>Chavarkar</i> ”)                                                                                                                                                                                                                                            |
| Ex. 1022 | U.S. Patent Application Publication No. 2003/0102482 A1 to Saxler (“ <i>Saxler482</i> ”)                                                                                                                                                                                                                                                      |
| Ex. 1023 | Shuji Nakamura – Biographical, NobelPrize.org, Nobel Prize Outreach AB 2023, <a href="http://www.nobelprize.org/prizes/physics/2014/nakamura/biographical/">www.nobelprize.org/prizes/physics/2014/nakamura/biographical/</a> (last visited Aug. 28, 2023) (“ <i>Biographical Nakamura</i> ”)                                                 |
| Ex. 1024 | Excerpts of Vasco Matias, Defect characterization of Europium implanted Gallium Nitride (2008) (Ph.D. dissertation, KU University, Belgium) (“ <i>Matias</i> ”).                                                                                                                                                                              |

[023] I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

**V. LEGAL STANDARDS**

[024] I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

[025] I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

[026] I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

[027] I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-12 of the '294 patent from the perspective

of a person of ordinary skill in the art at the '294 patent's earliest claimed priority date in 2009, as described in more detail below.

[028] I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means "more likely than not."

[029] For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

**A. Level of Ordinary Skill in the Art**

[030] I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

[031] I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

**B. Anticipation**

[032] I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

**C. Obviousness**

[033] I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

[034] I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;

- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

[035] I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the challenged claims is April 8, 2009. My opinions would not change if I assumed a later date of invention.

[036] I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

[037] I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve

the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

[038] In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

[039] I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may

drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

**[040]** I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

**[041]** I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to

whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

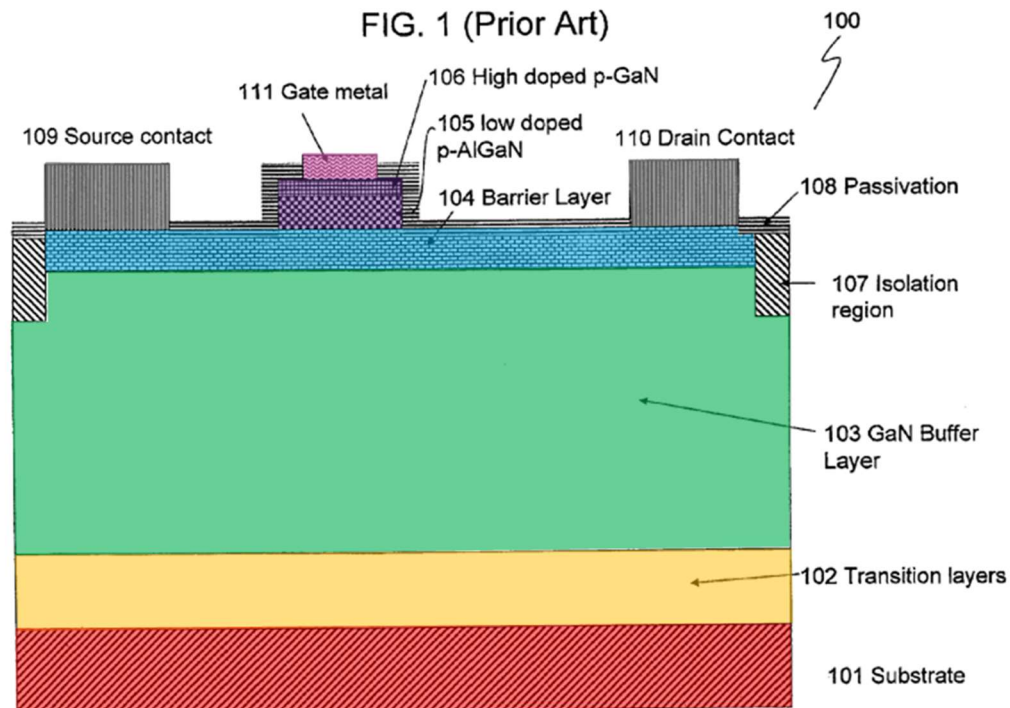
[042] I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '294 patent.

[043] I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

## **VI. OVERVIEW OF THE '294 PATENT**

[044] The application that issued as the '294 patent was filed on April 8, 2010, claiming priority to a provisional application filed on April 8, 2009. '294 patent, Cover. The patent issued on January 8, 2013, with 12 claims, 4 of which are independent. '294 patent, Cover, 5:10-6:27.

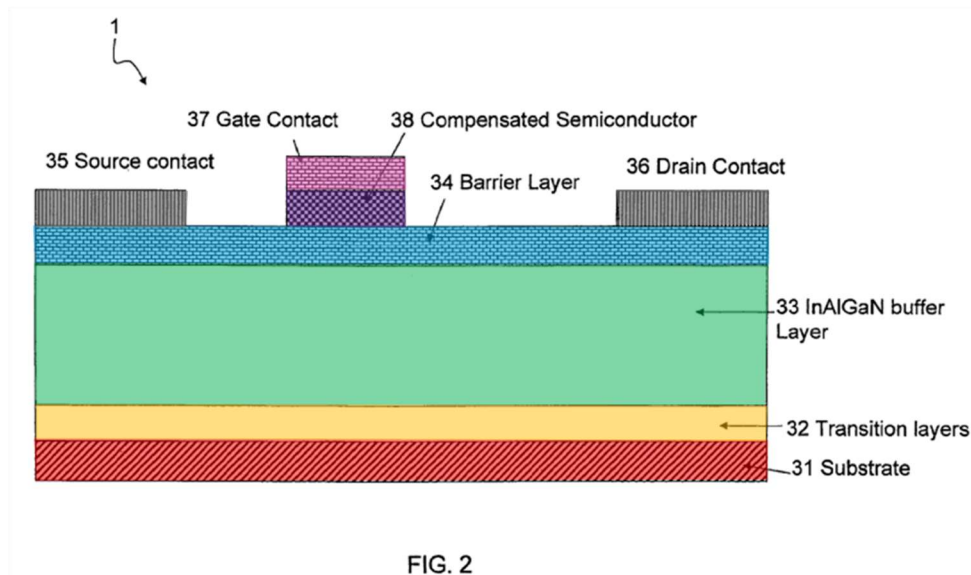
[045] The '294 patent relates to a “transistor with a compensated GaN layer or a semi-insulating GaN layer below the gate contact and above the barrier.” '294 patent, 1:16-18. The '294 patent admits that the GaN transistors were known in the “prior art.” '294 patent, 1:55-2:2, Fig. 1. Particularly, the '294 patent admits as prior art the “conventional enhancement mode GaN transistor” formed with a **substrate**, **transition layers**, **buffer layer**, **barrier layer**, **p-type layers**, and contacts for **gate** and **source/drain**. '294 patent, 1:55-2:2, Fig. 1. The admitted prior art is shown in Figure 1, reproduced and color coded below.



'294 Patent, Fig. 1 (annotated)

[046] The '294 patent purports to address leakage issues in the conventional transistor. '294 patent, 2:3-9. According to the patent, leakage could be reduced by forming the “compensated GaN” or “semi-insulating” layers “below the gate contact.” '294 patent, 3:17-21, 3:63-67. The '294 patent describes the steps to form the conventional transistor layers. '294 patent, 3:22-20, Figs. 2-9. The '294 patent, however, then pinpoints its “invention” as the formation of the compensated or semi-insulating layer, emphasizing that “[t]he critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen.” '294 patent, 3:43-45. According to the '294 patent, this “critical step” of passivation leads to “compensated semi-insulating material” below the gate metal. '294 patent, 3:45-52, 4:20-29.

[047] The '294 patent presents four transistor embodiments using the “compensated” or “semi-insulating” layers. The first embodiment has the same **substrate**, **transition**, **buffer**, **barrier**, and **gate** of the conventional transistor, admitted as prior art, but substitutes the **p-type layers** in the conventional structure with a “[c]ompensated semiconductor layer 38 [that] preferably comprises AlGaN or GaN with a deep level passivated p-type impurity.” '294 patent, 3:10-11. The first embodiment is shown in Figure 2, reproduced and color-coded below:



'294 patent, Fig. 2 (annotated)

[048] Comparing to the first embodiment with the admitted prior art, the only difference is the purported use of a “compensated semiconductor” layer under the gate (labeled as element 38) instead of the doped p-type layers (labeled as elements 105 and 106). Every other element is the same<sup>1</sup>:

<sup>1</sup> Figure 2 labels the buffer layer (element 33) as “InAlGaN buffer layer.” But the use of InAlGaN is just an embodiment of the patent, and refers to a generic formulation. '294 patent, 2:63-65. The patent and claims are clear the buffer layer is “made of a III Nitride material,” which “can be composed of  $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$  where  $x+y \leq 1$ ,”—including just GaN. '294 patent, 3:12-15.

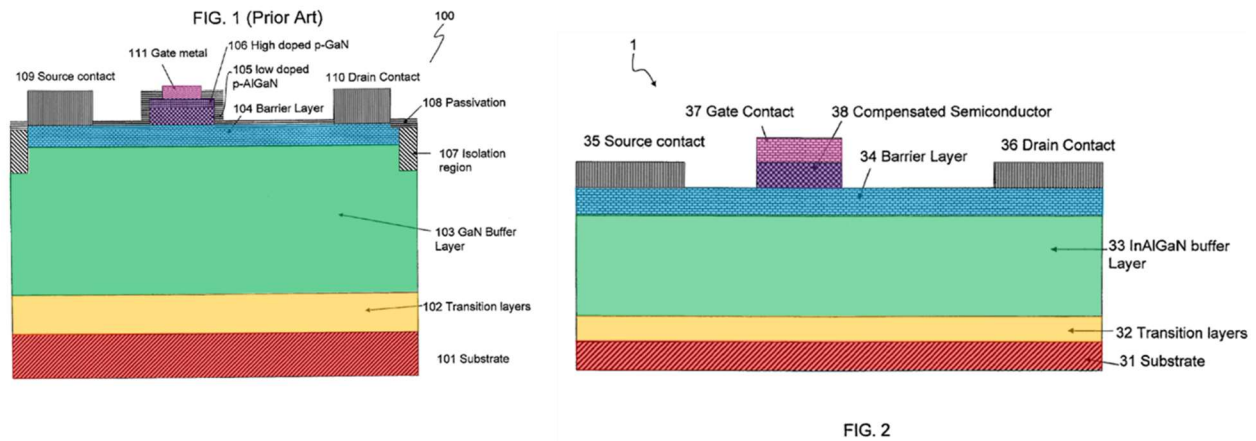


FIG. 2

'294 patent, Figs. 1, 2 (annotated)

[049] The second embodiment uses “a semi-insulating layer 39 in place of the compensated semiconductor layer 38.” '294 Patent, 3:56-57. The '294 patent states that the “[s]emi-insulating layer 39 may comprise, for example, AlGa<sub>0.5</sub>N or GaN, with deep level impurity atoms” and that the transistor could “have both a semi-insulating layer and a compensated semiconductor layer.” '294 patent, 3:57-61. The second embodiment is shown in Figure 10, reproduced and color-coded below:

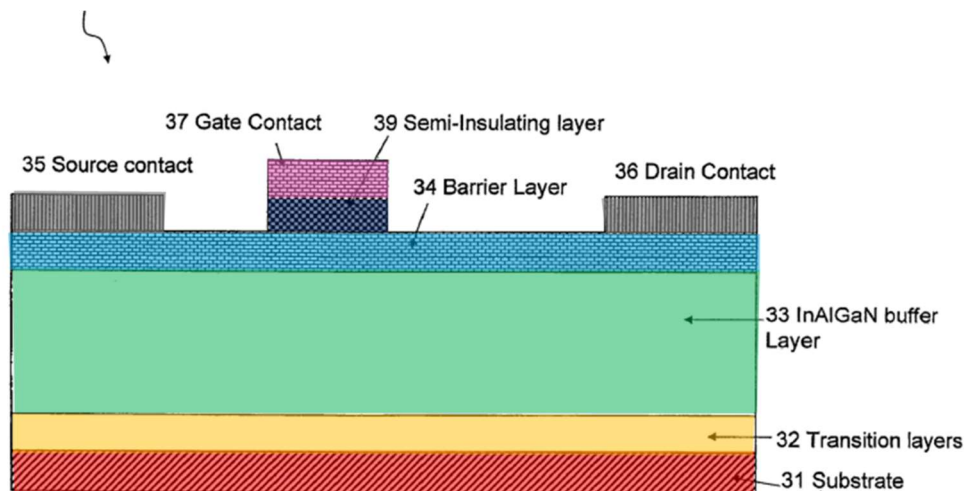


FIG. 10

'294 Patent, Fig. 10 (annotated)

[050] The remaining embodiments include additional layers: the third embodiment adds “a confinement layer . . . above the semi-insulating layer” ('294 patent, 4:32-33), the fourth embodiment adds a “a spacer layer 49 beneath semi-insulating layer” ('294 patent, 4:65-66). The third and fourth embodiments are shown in Figures 14 and 16 respectively.

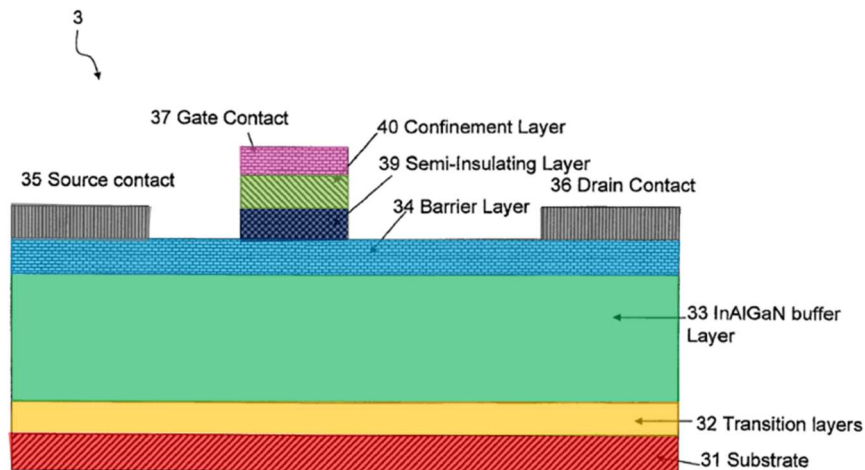


FIG. 14

'294 Patent, Fig. 14 (annotated)

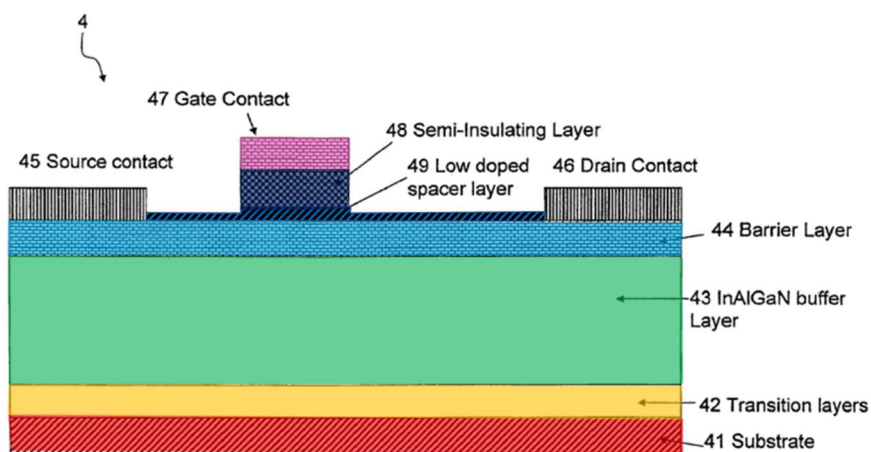


FIG. 16

'294 Patent, Fig. 16 (annotated)

[051] All of the '294 patent embodiments are related solely to variations of the layers between the gate and barrier layer, while using the same conventional layers that the patent admits are prior art.

**VII. LEVEL OF ORDINARY SKILL IN THE ART**

[052] In rendering the opinions set forth in this declaration, I have been asked to consider the '294 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the art," "skilled artisan," "POSITA," "POSA" or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

[053] Taking the factors described in the Legal Standards – Level of Ordinary Skill in the Art section into consideration, it is my opinion that a person of ordinary skill in the art for the '294 patent would have had at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa.

[054] Based on my educational background and experience, I was at least a person of ordinary skill in the art at the earliest priority date of the '294 patent.

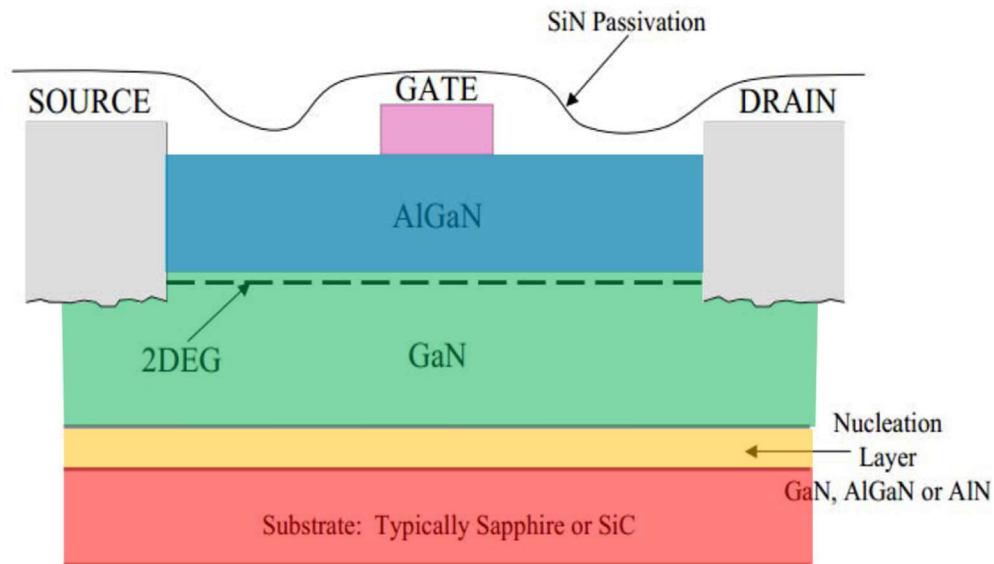
## VIII. TECHNOLOGY BACKGROUND AND STATE OF THE PRIOR ART

### A. III-Nitride Transistors

[055] The '294 patent and its claims are directed to III-nitride transistors. '294 patent, Claims 1-12. These are transistors fabricated with semiconductors that combine a group III element (e.g., indium or gallium) with nitrogen. The III-nitride transistor technology dates back to the mid-1990's. *Mishra*, Fig. 1; *Quay*, §2.5.5; *Pearton*, §6.2. By April 2009, the priority date of the '294 patent, III-nitride transistors had been known for over a decade. A person of ordinary skill knew well the transistors' structures, characteristics, operation, and fabrication.

[056] For example, in 2009 a person of ordinary skill knew that III-nitride transistors could be fabricated by layering III-nitride semiconductor materials with different band gap (*i.e.*, the potential energy distance of electrons between the valence band and the conduction band). *Mishra*, §II. A person of ordinary skill was familiar with different III-nitride transistor structures. One transistor structure that was very well-known in 2009 was the high-electron mobility transistor (HEMT)—a type of III-nitride transistor. The person of ordinary skill understood the basic HEMT structure consisting of nucleation, channel, barrier, and gate layers stacked on a substrate (reproduced and color-coded below). *Mishra*, Fig. 4 (describing a “Basic HEMT structure”). This “Basic HEMT structure” is

reproduced below using the same color coding used in labeling the figures in the overview of the '294 patent in section.

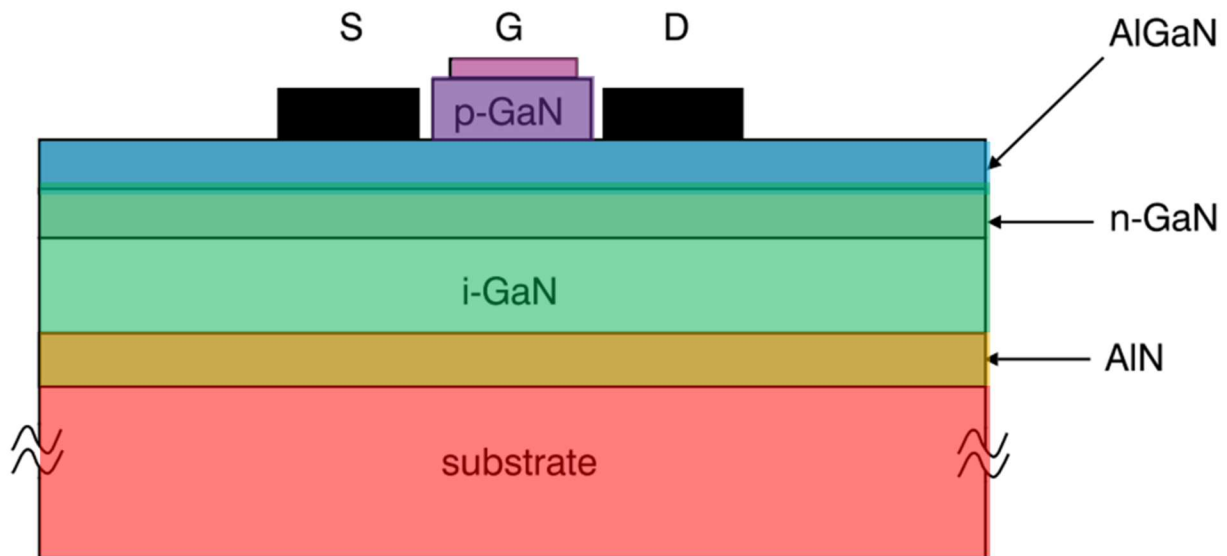


*Mishra, Fig. 4*

[057] A person of ordinary skill knew about the transistors' operation, its characteristics, and design considerations. A person of ordinary skill in the art knew, for example, that transition or buffers between the different layers could be used to balance lattice and thermal mismatch relieving mechanical stress, which could lead to undesired bending and cracking. *Quay*, §2.2.6; *Saxler015*, Abstract, [0002]. A person of ordinary skill in the art also knew that the aluminum in the barrier layer generated a barrier potential that induced a two-dimensional electron gas (2DEG). *Mishra*, Fig. 6; *Quay*, §2.2.3. A person of ordinary skill knew that this 2DEG formed the transistor channel in the HEMT devices.

## B. Cap Layers

[058] In the early 2000's, researchers reported the use of a "cap layer" between **barrier** and **gate** modifying the basic transistor structure. *Hu*, pp. 1-2; *Suh*, §4.1; *Quay*, §3.4.2. Cap layers were added to, among other things, control the transistor's threshold voltage and enable enhancement (i.e., normally off) operation. *Hu*, p. 1; *Suh*, §4.1. A schematic of a transistor having the **cap layer** is reproduced below using the same color coding used in labeling the figures in the overview of the '294 patent.



*Hu*, Fig. 1

[059] By 2009, a person of ordinary skill knew well about cap layers and their effect on the transistor characteristics. *Suh*, §4.1; *Quay*, §3.4.2. The effect of cap layers had been thoroughly studied. Many had experimented and implemented

different cap layers. And researchers had investigated and reported how cap layer thickness and composition impacted the device performance. *Quay* §3.4.2; *Suh*, §4.4. A person of ordinary skill understood how cap layer characteristics could be used to tailor the transistor performance. A person of ordinary skill knew, for example, how cap layer variables (e.g., thickness, doping, or composition) could be tailored in a “design space” (i.e., the ranges of materials, processes, and attributes that could be selected by a device designer) seeking different transistor characteristics. *Suh*, §4.2. A person of ordinary skill also knew how different cap layer combinations tailored transistor’s performance. *Suh*, §4.2; *Hu*, pp. 1-2; *Smith*, [0008]-[0017].

### **C. Acceptor Doping and Hydrogen Passivation**

[060] By April 8, 2009, doping of III-nitride materials had also been profoundly studied and was well understood. A person of ordinary skill understood how doping defined optoelectronic characteristics of the layers. *Quay*, §2.2.5; *Pearton*, §1.2; *Saxler* 874, [0004]. A person of ordinary skill knew well the doping processes and doping elements.

[061] A person of ordinary skill in the art understood, for example, that beryllium, magnesium, calcium, carbon, or zinc, were all elements that could be used as acceptor dopants and used to form p-type III-nitride layers. *Quay*, §§ 2.2.5,

3.3.1; *Saxler*874, [0006]. A person of ordinary skill in the art also understood that deep level dopants such as iron, chromium, titanium, and vanadium, could be used as dopants to form induced isolation and create higher resistivities. *Pearton*, §1.4.

[062] Among the various doping mechanisms, magnesium doping received special attention. Magnesium was identified as a suitable acceptor dopant early, in the 1970's. *Pearton*, §1.3.1. By 2009, magnesium doping was deeply understood. It was well known, for example, that magnesium dopants tended to naturally interact with hydrogen during the epitaxial growth processes (e.g., during Metal-Organic Chemical Vapour Deposition, or MOCVD) and that even "as-grown" materials (i.e., materials without modifications) included an innate hydrogen concentration. *Quay*, §3.3; *Pearton*, §1.2; *Van de Walle*, §I.1.c. A person of ordinary skill knew that hydrogen played an important role in magnesium doping and passivation, and that hydrogenation (the incorporation of hydrogen) influenced the layer's resistivity because hydrogen would be naturally incorporated in the doped layers and interact with magnesium. *Quay*, §3.3.1; *Pearton*, §1.2; *Uemoto*, [0049]; *Kigami*, [0007].

[063] By 2009 the hydrogenation process in doped GaN, and its effects on resistivity, had been widely reported. Hydrogenation in doped GaN was first reported in the early 1990's by Nobel prize winner Dr. Shuji Nakamura. Dr.

Nakamura explained that hydrogenation “naturally occurs” in as-grown MOCVD GaN materials. *Nakamura*, p. 1265. Dr. Nakamura explained that “as-grown GaN films are hydrogen passivated,” demonstrated how hydrogen passivation affected resistivity, and described how to deal with the phenomenon of naturally incorporated hydrogen. *Nakamura*, p. 1266. Dr. Nakamura won the Nobel prize, in part, for this work. *Biographical Nakamura*, p. 7 (“Shuji also clarified the mechanism of hole compensation, which had been a mystery for twenty years. Atomic hydrogen produced from the dissociation of ammonia gas forms Mg-H complexes. This formation prevents magnesium acceptors from behaving as acceptors.”).

[064] By 2009, a person of ordinary skill in the art was well versed on the mechanisms of hydrogen passivation and understood that, as Dr. Nakamura found, hydrogen would be “naturally” present in as-grown MOCVD layers.

## **IX. CLAIM CONSTRUCTION**

[065] I am not an attorney. However, I have been informed by counsel of certain legal standards that apply with respect to claim construction and indefiniteness, and have used those standards, described below in formulating my opinions.

[066] I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent (Ex. 1002). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent’s written description, the patent’s prosecution history, or both.

[067] I understand that claim interpretation may also be informed by “extrinsic evidence” (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the relevant time period.

[068] I am also informed by counsel that the applicant of the ’294 patent can act as their own lexicographer, to set forth a definition of a claim term in the

specification. The definition provided by the applicant can differ from the claim term's plain and ordinary meaning. I have also been informed by counsel that when a patent claim uses the term "comprises" as a transitional statement after the preamble, there is a presumption that the claim is open-ended and not limited to the recited elements.

[069] I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '294 patent, other than as identified below.

[070] Based on my review of these materials and my personal knowledge and experience, I have considered the plain and ordinary meaning of each term of the '294 patent as it would have been understood by one skilled in the art at the earliest claimed priority date of the '294 patent of April 8, 2009. I apply the plain and ordinary meaning of each claim term throughout this declaration, other than as identified below.

[071] I have been informed that the owner of the '294 patent Efficient Power Conversion Corporation (EPC or Patent Owner) and Petitioner Innoscience have agreed in a related matter that the term "a compensated GaN layer" in claim 1

of the '294 patent should be construed. *ITC Constructions*, pp. 1, 9. The parties have proposed the following constructions:

| Petitioner's Proposal                                                                                       | Patent Owner's Proposal                                                                                                                                                                                                                  |
|-------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| "Doped GaN layer formed with a step to passivate its impurities" which is a "product-by-process" limitation | "A semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)." |

**A. Petitioner's Proposed Construction Should Apply**

[072] In my opinion, the Petitioner's proposed construction is correct because in light of the claim language, the specification, and the prosecution history, a person of ordinary skill in the art would have understood "a compensated GaN layer" means "a doped GaN layer formed with a step to passivate its impurities."

[073] In my opinion, the claim language itself supports the Petitioner's construction because the claim use of the verb in past tense "compensated" as an

adjective to define the layer, indicating that an action or step for compensation has occurred. So the claim language itself is indicating that the “GaN layer” was “compensated” or had been subject to a compensation step. I note, for example, that none of the other layers in claim 1 are described with past tense verbs. In my opinion, this would indicate to a person of ordinary skill in the art that the “compensated GaN layer” reflects the layer was subject to a compensation action or step during the manufacture of the device.

[074] The written description also clarifies the meaning of “compensated GaN layer” and supports the Petitioner’s construction. In its description, the ’294 patent admits p-type doped GaN caps were known and emphasizes that the invention distinguishes from the prior art based on the “critical step” of “passivation of a p-type impurity using hydrogen.” ’294 patent, 3:43-45. The patent specifies that it is this “critical step” of passivation that leads to a “highly compensated” material. ’294 patent, 3:46-48. The patent also describes the “compensated” layer as a layer “with a deep level passivated p-type impurity” and discloses the passivation “can be performed by exposing the device to ammonia or hydrogen.” ’294 patent, 3:11-39. In light of this description, a person of ordinary skill would have understood that in the ’294 patent a layer is “compensated” when

it is formed with this “critical step” to passivate its impurities, confirming the Petitioner’s construction.

[075] The arguments against the prior art that the patent applicant submitted to the Patent Office during examination also support the Petitioner’s construction. During prosecution, the Examiner initially rejected the “compensated GaN layer” limitation based on prior art *Bowers*. *Prosecution History*, 87. *Bowers* had disclosed that “[i]t is known that hydrogen passivates the p-type dopants in Mg doped GaN.” *Bowers*, 8:31-35. Citing *Bowers*, the Patent Office Examiner concluded that, “it is well known in the art that hydrogen passivates or compensates Mg dopants in a GaN material” and rejected the claim as obvious. *Prosecution History*, 88. In response, however, the Applicant argued that while *Bowers* disclosed knowledge about hydrogen passivation, it failed to disclose “**forming** a ‘compensated GaN layer.’” *Prosecution History*, 107 (emphasis added). The patent applicant remarks to distinguish from the prior art support the Petitioner’s proposed construction because they clarify that the claimed “compensated GaN layer” requires undertaking steps for “*forming*” the compensated layer, as opposed the natural passivation of Magnesium by hydrogen in as-grown p-GaN described by *Bowers*. Applicant’s remarks clarified that the mere presence of hydrogen in the layer, which (as the Patent Office found and a

person of ordinary skill in the art would understand) had been well known in the art, is not the “compensated GaN layer” required in the claim. In my opinion, the Applicant’s remarks in the prosecution history, therefore, support the Petitioner’s construction.

[076] Additionally, it is my opinion that extrinsic evidence supports Petitioner’s construction. As discussed above, Dr. Nakamura had reported the mechanisms and effects of hydrogenation in as-grown III-nitride materials in the early 1990s. By 2009, hydrogenation in as-grown III-nitride materials had been known for over a decade. Textbooks and articles confirm the Patent Office Examiner’s finding that hydrogen passivation was well known. The prior and contemporary articles and textbooks confirm that “compensated,” which the ’294 patent identifies as the “critical step” distinguishing from the prior art, cannot be interpreted as the mere presence of hydrogen in as-grown material because such the natural hydrogenation had been known for over a decade. The extrinsic evidence, thus, also in my opinion supports the Petitioner’s construction.

**B. Patent Owner’s Proposed Construction is Incorrect And Renders The Claim Ambiguous**

[077] In contrast, it is my opinion that the Patent Owner’s proposed construction is improper because it is divorced from the claim language, the specification, and the intrinsic record. Based on my review, neither the patent

specification nor the extrinsic record support construing “a compensated GaN layer” as “[a] semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor),” as proposed by the Patent Owner. *ITC Constructions*, p. 1.

[078] Patent Owner’s proposed construction renders the claim ambiguous and indefinite to a person of ordinary skill in the art. Patent Owner’s proposed construction introduces undefined relative terms and construes the claim term with “examples” that make the scope of the claim ambiguous. In my opinion, if Patent Owner construction is adopted, a person of ordinary skill would not be able to determine the scope of the claim, even in light of the patent specification.

[079] For example, Patent Owner’s proposed construction introduces the terms such as “imperfection,” “partially cancels,” or “electrical effects,” that are not used in the claims or disclosed in the specification. Indeed, based on my review, these terminologies are not used, let alone defined, anywhere in the ’294 patent or in the prosecution history. These terms introduce ambiguity into the claim term.

[080] For example, the term “partially cancels the electrical effects” in Patent Owner’s proposed construction makes the limitation indefinite because a

person of ordinary skill would not be able to determine what “electrical effect” is meant, or when the “partial” cancelation is achieved. “Electrical effects” could refer to virtually any electrical phenomena, making it impossible for a person of ordinary skill in the art to know what “effects” are desired to be canceled. And, even if a person of ordinary skill in the art knew which effect this term referred to, he or she would not have any guidance to determine when a material would be “partially cancelled” and when a material would not be “partially cancelled,” because the boundaries of this cancelation are not given under Patent Owner’s proposed construction.

[081] Further, Patent Owner’s proposed construction defining the term based on a list of optional elements, “dopant[s], impurity[ies], or imperfection[s]” and then reciting “examples” is confusing and ambiguous. Patent Owner’s proposed construction lists different elements as alternatives (in disjunctive form) reciting “dopant, impurity, *or* imperfection.” But it is unclear what the intended difference between each of “dopant, impurity, or imperfection.”

[082] Indeed, it is my opinion that Patent Owner’s proposed construction cannot apply because it is so vague that it would permit an interpretation to cover *any* GaN material, even the materials that the ’294 patent admits as prior art. Any GaN material would fall under the definition of “material in which one type of

dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor).” A person of ordinary skill would have known that GaN materials are never ideal, they always have some trace unintentional dopants (which could be interpreted as “dopants” or “impurities”), and inevitable defects (“imperfections”). *Matias*, §3.1 (“in a real crystal, the structure is always disturbed by some irregularities. Crystalline imperfections, or defects, will always be present at normal pressure and temperatures”), §3.2 (“[t]he several types of point defects can interact with each other.”). Even setting aside the intentionally doped materials (which are purposefully modified to include impurities), a person of ordinary skill would have recognized that intrinsic GaN layers still have defects that affect their properties. And a person of ordinary skill in the art would appreciate these “dopant[s], impurity[ies], or imperfection[s]” are at least passivated by the most common impurity: hydrogen, the smallest atom on the periodic table. Hydrogen is easily diffusible through lattices, present “naturally” in GaN layers (even in “as-grown” material, particularly when formed through MOCVD), and forms the naturally occurring (and inevitable) acceptor-H complexes during growth.

*Nakamura*, pp. 1265-66; *Van de Walle*, §§I.1, III.3 *Quay*, §3.3.1; *Pearton*, §1.2.

Further the electrical characteristics of GaN materials depend on the material

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structure of the GaN layer, including these “dopants, impurities, and imperfections.” *Quay*, §2.2.5; *Pearton*, §1.2; *Saxler* 874, [0004].

[083] Therefore, *any* GaN material would include a “dopant, impurity, or imperfection” that affects or “partially cancels” the “electrical effects” of other types of “dopant[s], impuritie[s], or imperfection[s].” *Matias*, §3.1. One common prior art example material would be, as *Bowers* and *Nakamura* explain, the relationship between hydrogen and magnesium in p-type GaN. *Bowers*, 8:31-35; *Nakamura*, p. 1265. But it would also include any n-type GaN, intrinsic GaN, or other III-nitride materials that include Gallium and Nitrogen such as AlGaN. Such a broad construction, in my opinion, is nonsensical, particularly in view of the ’294 patent intrinsic record that highlights the “compensated” layers as the feature distinguishing from the prior art. ’294 patent, 3:43-52; *Prosecution History*, p. 106.

[084] For example, Patent Owner’s construction fail to recognize that the ’294 patent specifies that “[t]he critical step in the above process *that differentiates the device of the present invention from the prior art device (FIG. 1)* is the passivation of a p-type impurity using hydrogen” and that the passivation leads to “the compensated semiconductor layer 38.” ’294 patent, 3:43-53 (emphasis added). And, as explained above, the admitted prior art used a “doped p-type GaN” layer in its cap. ’294 patent, 1:55-2:2. Further, as explained above,

person of ordinary skill in the art would know the magnesium in p-type GaN (the p-type dopant) is naturally passivated by hydrogen. *Nakamura*, p. 1265. The Patent Owner's proposed construction therefore ignores the admitted prior art in the '294 patent because the proposed construction would read on that same prior art, because the hydrogen would be one "type of dopant, impurity, or imperfection" that "partially cancels the electrical effects," through passivation, of the magnesium, the other "type of dopant, impurity, or imperfection." *ITC Constructions*, p. 1.

[085] Patent Owner's proposed construction also fails to consider the patent applicant's arguments during prosecution. The patent application argued the "compensated GaN layer" distinguished from the prior based on its formation, as described above, at least because it could not be met without a step to "form" the "compensated GaN layer." In particular, patent applicant distinguished from *Bowers* arguing that *Bowers* described only the "known" relationship that "hydrogen passivates the p-type dopants in Mg doped GaN" grown without a specific step for "forming" a compensated GaN layer. *Bowers*, 8:31-35.

[086] For at least the foregoing reasons, it is my opinion that Patent Owner's proposed construction is incorrect.

**C. Under Both Proposed Constructions, The Claims Are Unpatentable in View of the Prior Art**

[087] Notwithstanding the foregoing, I have addressed both constructions of “a compensated GaN layer” throughout this declaration. And in my opinion, as further noted below, the challenged claims are unpatentable under both constructions of “a compensated GaN layer.” Regardless of whether “compensated GaN layer” is construed with Petitioner’s or Patent Owner’s proposed constructions, the claims are unpatentable. Indeed, as explained above, a person of ordinary skill would understand Patent Owner’s construction includes within it Petitioner’s construction (and indeed, virtually all GaN based semiconductor materials), and so any reference which demonstrates this limitation is met under Petitioner’s construction would also mean Patent Owner’s construction is met. But the term should be construed as proposed by the Petitioner because a POSITA would understand “a compensated GaN layer” to mean “a doped GaN layer formed with a step to passivate its impurities” in light of both the intrinsic and extrinsic records.

[088] To the extent further comments on claim terms are warranted, I provide them below in the relevant sections when addressing how the claims read on the prior art.

**X. THE PRIOR ART**

[089] In forming my opinions, I found the following prior art relevant when considering whether the claims of the '294 patent would have been obvious to a person of ordinary skill in the art:

- Ex. 1005, U.S. Patent Publication No. 2007/0164315 to Smith ("*Smith*");
- Ex. 1006, U.S. Patent Publication No. 2008/0087915 to Uemoto ("*Uemoto*");
- Ex. 1007, Japanese Patent Publication No. JP2006-253224 to Kigami and its English translation Ex. 1008 ("*Kigami*")

In my opinion, these references disclose information that was not disclosed in the prior art the Examiner considered during prosecution. *Prosecution History*; '294 patent, Cover. Based on my review, *Smith*, *Uemoto*, and *Kigami* are not cumulative of the prior art considered during prosecution because *Smith*, *Uemoto*, and *Kigami* teach the claim feature the patent applicant argued was not disclosed by the prior art. Specifically, and as further discussed below, the *Smith*, *Uemoto*, and *Kigami* references disclose "forming a 'compensated GaN layer above [a] barrier layer,'" which was the feature the patent applicant argued was not present in the prior art he considered. *Prosecution History*, 106. The *Smith*, *Uemoto*, and *Kigami* references disclose "a compensated GaN layer above the barrier layer," which was a feature the Patent Office Examiner identified as part of the reasons for allowance.

*Prosecution History*, 149. Additionally, *Smith*, *Uemoto*, and *Kigami* are not cumulative from what the Examiner considered because, as I further discuss in my analysis below, they disclose the intentional incorporation of hydrogen in GaN layers and the use of semi-insulating cap layers, which are not disclosed in the references the Examiner considered during prosecution.

**A. *Smith* (US 2007/0164315)**

[090] *Smith* is a U.S. patent application publication that published July 19, 2007. *Smith*, Cover. The corresponding application had been filed in March 12, 2007. *Smith*, Cover.

[091] Like the '294 patent, *Smith* discloses transistors formed with III-nitride materials, and specifically transistors made with GaN-based materials. *Smith*, [0002], [0008]. *Smith* discloses several embodiments of III-nitride transistors, describing them as including many of the well-known features and structures of conventional nitride transistors. *Smith*, [0069], [0077], Figs. 1A-9. *Smith* discloses the transistors are fabricated with the well-known technique of stacking several nitride semiconductor layers on a substrate to that form a transition from the substrate, a channel, a barrier, and a cap. *Smith*, [0069]-[0077]. *Smith* also discloses the transistors are formed with ohmic contacts that form

source/drain nodes, and a gate electrode; a transistor arrangement known for many decades. *Smith*, [0070]-[0080].

[092] *Smith* describes its transistors with cross-sectional schematics illustrated in Figures 1A-9. As shown in the figures, *Smith* discloses the use of different cap layers and gate contacts in nitride transistors to adjust the transistor's electrical characteristics. *Smith*, [0068]. For example, as shown below in Figures 1A and 1B (reproduced below), *Smith* discloses alternative transistor structures, some using a “recessed gate” (Figure 1A) others using “non-recessed gate” (Figure 2A). *Smith*, [0068]-[0069].

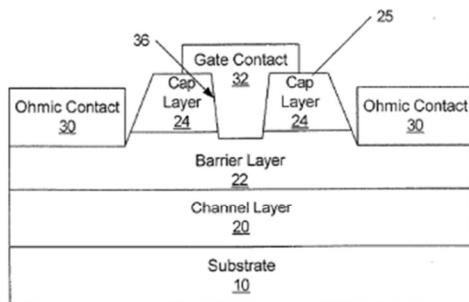


Figure 1A

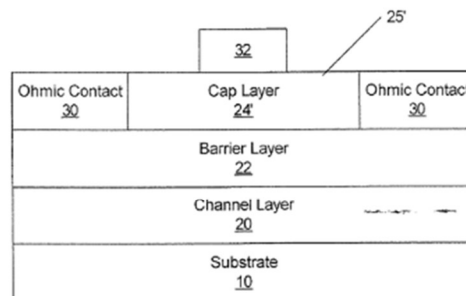


Figure 1B

*Smith*, Figs. 1A, 1B.

[093] *Smith* also discloses transistors with cap layers of different composition, thickness, and doping. *Smith*, [0077], [0085], [0097]. *Smith* explains that cap layers can adjust transistor variables like leakage current, threshold voltage, and frequency performance. *Smith*, [0081]. And *Smith* discloses further

adjustments to the transistor characteristics to control the transistor characteristics using multilayers, passivation, and protective layers in the cap region.

*Smith*, [0092], [0100], [0108]; Figs. 3A-8.

[094] Overall, *Smith* discloses multiple structures and fabrication methods for nitride-based transistors, describing how different features (or combination of features) can adjust transistor electrical characteristics to seek performance and/or fabrication advantages.

**B. *Uemoto* (US 2008/0087915)**

[095] *Uemoto* is a U.S. patent application publication that published April 17, 2008. *Uemoto*, Cover. The corresponding application had been filed in July 24, 2007. *Uemoto*, Cover

[096] *Uemoto*, like the '294 patent, relates normally-off (also known as enhancement mode) III-nitride semiconductor transistors. *Uemoto*, [0003]. Like the '294 patent (and *Smith*), *Uemoto* discloses its transistors are formed by stacking multiple nitride layers on a substrate and using electrodes to form the transistor source, gate, and drain. *Uemoto*, [0031]-[0035]. In Figure 1, reproduced below, *Uemoto* illustrates one of its transistor embodiments.



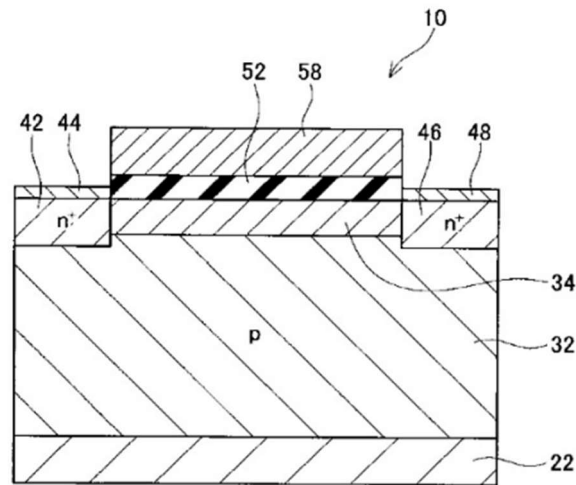
performing a thermal treatment, hydrogen may be selectively introduced or kept in specific regions of the layer 15, forming regions 15a and 15b and yielding improved gate-drain leakage and temperature stability. *Uemoto*, [0059], [0063]; Fig. 8.

**C. *Kigami* (JP 2006-253224)**

[099] *Kigami* is a Japanese patent application publication that published September 21, 2006. *Kigami*, Cover. The corresponding application had been filed March 8, 2005. *Kigami*, Cover

[0100] Like the '294 patent, *Kigami* discloses III-V semiconductors, particularly GaN semiconductors, formed to operate as normally-off III-nitride transistors. *Kigami*, [0001]-[0005]. In *Kigami*, a doped GaN layer is formed on a substrate. *Kigami*, [0024], Fig. 2. And a transistor is formed on the GaN layer with a MIS (Metal-Insulator-Semiconductor) gate structure and source/drain contacts. *Kigami*, [0024], Fig. 4. *Kigami*'s transistor is shown in Figure 1, reproduced below.

FIG. 1

*Kigami*, Fig. 1

[0101] *Kigami* discloses that the III-nitride transistor can be improved by introducing hydrogen in the GaN layer to locally passivate impurities in a “local region 34” of the GaN layer 32 (both shown in Figure 1 above). *Kigami*, [0007], [0022]. *Kigami* discloses that hydrogen can be introduced in layer 32 by exposing the transistor to an ionized hydrogen gas. *Kigami*, [0026], Fig. 5. *Kigami* discloses that the introduced hydrogen atoms form a composite with magnesium, inactivating the impurities and making the “local region 34” more resistive. *Kigami*, [0026]. *Kigami* explains that the hydrogenation (i.e., introduction of

hydrogen) reduces and stabilizes the threshold voltage while keeping a high withstand or breakdown voltage.<sup>2</sup> *Kigami*, [0006], [0023], [0029].

## **XI. GROUNDS OF UNPATENTABILITY**

[0102] Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my opinion that claims 1-12 of the '294 patent would have been obvious to one of ordinary skill in the art.

[0103] In particular, it is my opinion that claims 1-12 of the '294 patent would have been obvious to one of ordinary skill in the art, based on the grounds shown below:

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<sup>2</sup> *Kigami* uses the term “withstand voltage” instead of the more common “breakdown voltage.” Both terms, however, are related. Withstand voltage is the voltage that a device can sustain (or withstand) without causing breakdown. Therefore, a high withstand voltage is equivalent to a high breakdown voltage. To a person of ordinary skill in the art “withstand” and “breakdown” have equivalent technical meaning.

| Grounds | Challenged Claims | Basis | Prior Art               |
|---------|-------------------|-------|-------------------------|
| 1A      | 1-12              | § 103 | <i>Smith</i>            |
| 1B      | 1-12              | § 103 | <i>Smith and Kigami</i> |
| 1C      | 1-12              | § 103 | <i>Smith and Uemoto</i> |
| 2       | 1-12              | § 103 | <i>Uemoto and Smith</i> |

**XII. GROUNDS 1A-1C: THE CHALLENGED CLAIMS ARE UNPATENTABLE AS OBVIOUS IN VIEW OF *SMITH*, EITHER ALONE (1A), IN VIEW OF *KIGAMI* (1B), OR IN VIEW OF *UEMOTO* (1C)**

[0104] Claims 1-12 of the '294 patent are unpatentable in view of the prior art. In particular, a person of ordinary skill would have found *Smith*, either alone or in combination with *Kigami* or *Uemoto*, render all the challenged claims obvious.

**A. Overview of the Unpatentability Ground Based on *Smith* (Ground 1A)**

[0105] By itself, *Smith* renders obvious all elements of the challenged claims. *Smith* discloses all the layers the '294 patent admits as prior art (e.g., **substrate**, **transition**, **buffer**, **barrier**, and **gate**). *Smith*, [0068], Fig. 1A. *Smith* also discloses transistors with **cap layers** and describes several embodiments with different **cap layers** selected or combined to adjust the transistor's characteristics. *Smith*, Figs. 1A-9, [0068]. *Smith* not only discloses the "conventional" transistor

structure the '294 patent admits as prior art, *Smith* also discloses the very elements the '294 patent highlights as allegedly distinguishing from the prior art. For example, *Smith* discloses transistors that include the “semi-insulating,” “confinement,” and “spacer” layers as disclosed in the '294 patent. *Smith*, [0087], [0090], [0120]. And *Smith* also discloses, or at a minimum renders obvious, the purportedly inventive limitation of “a compensated GaN layer above the barrier layer,” recited in claim 1, regardless of how the term is construed.

**1. *Smith* itself discloses “compensated GaN layer” under Petitioner’s construction**

[0106] If “a compensated GaN layer” is construed with Petitioner’s construction (as “doped GaN layer formed with a step to passivate its impurities,” *ITC Constructions*, 9), which I believe is the correct construction, *Smith* discloses the “a compensated GaN layer above the barrier layer,” limitation in claim 1.

[0107] I have been informed that under Petitioner’s construction the “compensated GaN layer” limitation should be interpreted as a “product-by-process.” I have been informed that a “product-by-process” limitation defines a product based on how it was produced (instead of its structural characteristics). And counsel has informed me that product-by-process limitations are anticipated by any prior art that discloses the resulting structure, regardless of how the product is made. I understand, thus, that unpatentability analyses of product-by-process

limitations need not show the “process” to demonstrate unpatentability only the “product.” In other words, the “process” in “product-by-process” limitations do not serve to distinguish from the prior art because the limitation is anticipated by a product with the resulting structure or “product,” even if it was achieved with a different “process.”

[0108] Therefore, when “compensated GaN layer” is properly construed, as proposed by the Petitioner, and interpreted as a “product-by-process” limitation, any prior art disclosing a GaN layer with passivated impurities, regardless of the passivation method, meets the “compensated GaN layer ” limitation. And *Smith* discloses a GaN layer with passivated impurities.

[0109] *Smith* discloses its cap layers being formed with different materials, dopants, and thicknesses. *Smith*, [0085]-[0089]. As discussed in the technology background, by 2009 it was well-known that—as Dr. Nakamura reported—“as-grown GaN films are hydrogen passivated.” *Nakamura*, p. 1266. Therefore, a person of ordinary skill in the art would have recognized that *Smith*’s cap layer meets the “GaN layer formed with a step to passivate its impurities,” because the cap layer would include passivated impurities, and the process of passivation would not be relevant for unpatentability. When the “compensated GaN limitation”

is read as a “product-by-process” under Petitioner’s construction, *Smith* discloses the limitation, regardless of the specific passivation process.

[0110] Moreover, if the “compensated GaN layer” limitation of claim 1 is not interpreted as “product-by-process” under Petitioner’s construction, it is my opinion that *Smith* would still render the limitation obvious. While *Smith* does not explicitly disclose a step to passivate impurities, *Smith*’s disclosure makes such step or GaN formation obvious. *Smith* discloses that cap layers can be doped with acceptors and that the level of doping is a variable that should be adjusted to reduce or control leakage. In particular, *Smith* specifies that “[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths by becoming a conductive layer.” *Smith*, [0014], [0085], [0087]. One of ordinary skill would have understood that by “level of doping” *Smith* referred to the level of active (non-passivated) impurities. And one of ordinary skill knew that well-known processing steps, like the hydrogenation discussed above in the technology background section, would passivate dopants, affecting the doping level.

[0111] Because it was well-known that passivation affected the level of doping, and *Smith* identifies level of doping as a variable to adjust leakage, a

person of ordinary skill in the art would have been motivated to control the level of doping in *Smith*'s cap layers by including the known hydrogenation processes.

Therefore, as further discussed below, if the limitation of "compensated GaN layer" is construed as "doped GaN layer formed with a step to passivate its impurities," but not interpreted as a "product-by-process," *Smith* would still render the limitation obvious as an obvious modification of a result effective variable.

**2. *Smith* itself discloses "compensated GaN layer" under Patent Owner's construction**

[0112] Moreover, if "compensated GaN layer" is construed as proposed by the Patent Owner (as "[a] semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)."), which I believe is ***not*** the correct construction, *Smith* also discloses it.

[0113] As discussed in the technology background section, by 2009 it was well established that "hydrogen passivation occurs in as-grown GaN films." *Nakamura*, p. 1265. If "compensated GaN layer" is interpreted with Patent Owner's proposal, a person of ordinary skill in the art would have recognized that *Smith*'s cap layer was already "a compensated GaN layer." For example, a person of ordinary skill in the art would have recognized *Smith*'s cap layer incorporated

both magnesium and hydrogen, because *Smith* specifies cap layer being doped with magnesium (*Smith*, [0085]) and it was well-known that hydrogen is naturally incorporated in as-grown doped GaN layers.

[0114] Therefore, a person of ordinary skill would have recognized that *Smith*'s cap layer is a "semiconductor GaN gate material, in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)." *Smith*'s cap layer is a "semiconductor GaN gate material" because it is formed with GaN and is part of the gate material. *Smith*, [0085], [0087], Fig. 2A. And *Smith*'s cap layer is a material "in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)" because in *Smith*'s cap layer the innate hydrogen (which is "one type of dopant, impurity, or imperfection"). The hydrogen "partially cancels" (as the term appears to be used in Patent Owner's construction) the electric effects of magnesium by forming the Mg-H complexes. And magnesium is "other type of dopant, impurity, or imperfection." In my opinion, *Smith* would also disclose the "compensated GaN layer" limitation under the Patent Owner proposed construction.

[0115] Therefore, as I further detail in my analysis below, *Smith* renders obvious all of the elements claims 1-12 of the '294 patent. *Smith* discloses both the layers in admitted prior art and also the layers that the '294 patent identified as distinguishing from the prior art, including the “compensated GaN layer” under both of the proposed constructions.

**B. Overview of the Unpatentability Grounds Based on *Smith* Combined With *Kigami* (Ground 1B) or *Uemoto* (Ground 1C)**

[0116] Even if the knowledge of the person of ordinary skill is deemed insufficient to show obviousness based on *Smith* alone, other references demonstrate that the claims of '294 patent would have been obvious to one of ordinary skill. In particular, even if *Smith* is deemed insufficient to render obvious the “compensated GaN layer” limitation, incorporating the “compensated GaN layer” in *Smith*’s device would have been obvious based on the prior art. Each of *Kigami* (Ground 1B) and *Uemoto* (Ground 1C) discloses the “compensated GaN layer” under both proposed constructions. And a person of ordinary skill in the art would have been motivated to modify *Smith*’s transistor in view of *Kigami* or *Uemoto* to include “a compensated GaN layer above the barrier layer.”

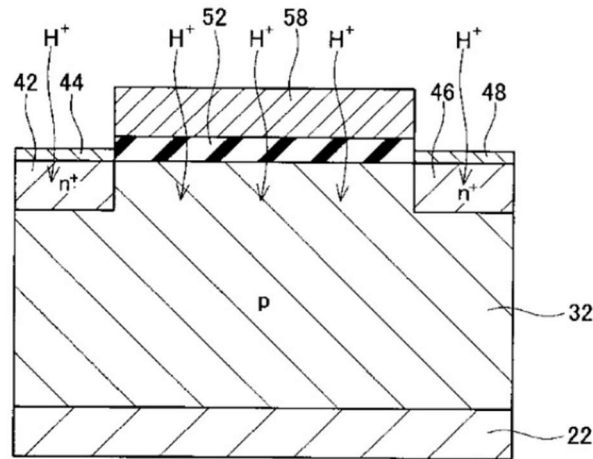
**1. Ground 1B: *Smith* combined with *Kigami***

[0117] For Ground 1B, a person of ordinary skill in the art would have applied *Kigami*’s hydrogenation method for passivating or inactivating impurities

with ionized gas to passivate impurities in *Smith's* cap layer seeking to improve *Smith's* transistor's operation.

[0118] *Kigami* discloses that III-nitride transistors can be improved by introducing hydrogen in the GaN layer that opposes the gate electrode. *Kigami*, [0007], [0022]. According to *Kigami*, the hydrogenation locally passivates impurities resulting in better threshold and breakdown voltage. *Kigami*, [0007], [0022]. For example, *Kigami* discloses that passivating the GaN layer with a hydrogenation step improves the transistor performance by reducing and stabilizing the threshold voltage while maintaining a high withstand voltage. *Kigami*, [0006], [0023], [0029]. *Kigami's* processing step of exposing the device to an ionized gas to introduce hydrogen in doped GaN layers is exemplified in *Kigami's* Figure 5 (reproduced below). *Kigami*, [0026].

FIG. 5

*Kigami*, Fig. 5

[0119] As further discussed below, using *Kigami*'s hydrogenation process to *Smith* would "compensate," as the term is used in the 294 patent, *Smith*'s cap layer and disclose the "compensated GaN layer above the barrier" under both parties' constructions.

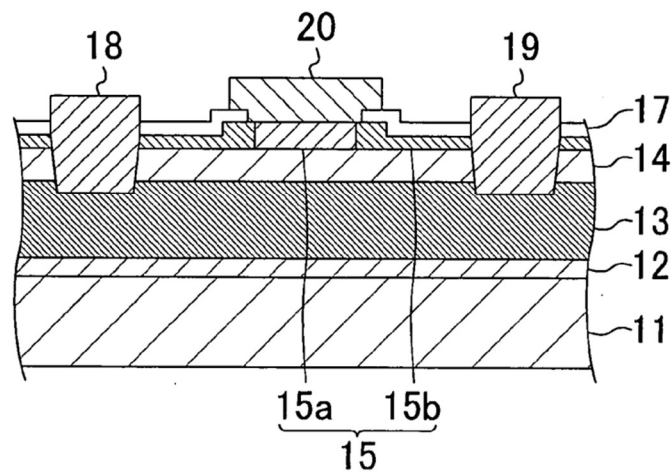
## 2. Ground 1C: *Smith* combined with *Uemoto*

[0120] In Ground 1C, a person of ordinary skill in the art would have employed *Uemoto*'s method of passivating impurities with a hydrogen diffusion layer and a thermal processing step seeking to, for example, reduce leakage current in *Smith*'s transistor.

[0121] As discussed in the prior art section, *Uemoto* teaches how to form a high resistive region 15b through a hydrogen diffusion step. *Uemoto*, [0063],

Fig. 8. *Uemoto* also discloses that forming the high resistive region improves transistor performance and stability. *Uemoto*, [0071]. For example, *Uemoto*'s Figure 7 shows the high resistive region 15b being formed beneath gate electrode 20.

FIG. 7

*Uemoto*, Fig. 7.

[0122] *Uemoto* discloses that the formation of the high resistive region 15b through hydrogen diffusion reduces gate leakage. *Uemoto*, [0063], [0071]. A person of ordinary skill would have been motivated to incorporate *Uemoto*'s technique to reduce leakage. And, as further discussed below, applying *Uemoto*'s technique to create high resistive regions to *Smith* results in a "compensated GaN layer above the barrier layer," under both parties' constructions.

**C. A person of ordinary skill would have been motivated to “compensate” *Smith*’s cap layer based on teachings in *Smith*, *Kigami*, or *Uemoto*.**

**1. (Ground 1A) A person of ordinary skill would have been motivated to adjust the level of doping in *Smith*’s cap layer using hydrogen passivation**

**[0123]** A person of ordinary skill would have been motivated to adjust the level of doping in *Smith* by employing the known hydrogen passivation.

**[0124]** I have been informed that when the prior art recognizes that a variable achieves a recognized result, such variable should be recognized as a “result-effective variable” (i.e., a variable which achieves a recognized result). I have been informed that when the prior art recognizes a “result-effective variable” it is not inventive to discover workable ranges by routine experimentation. That is, if the prior art has identified a variable as “result-effective” it is consider obvious to adjust that variable levels with already known techniques, such adjustments are considered just routine experimentation and not patentable.

**[0125]** In my opinion, *Smith* recognizes the level of doping in cap layers is a result-effective variable. *Smith* discloses that the level of doping in cap layers is a result-effective variable to control leakage, explaining that “[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide

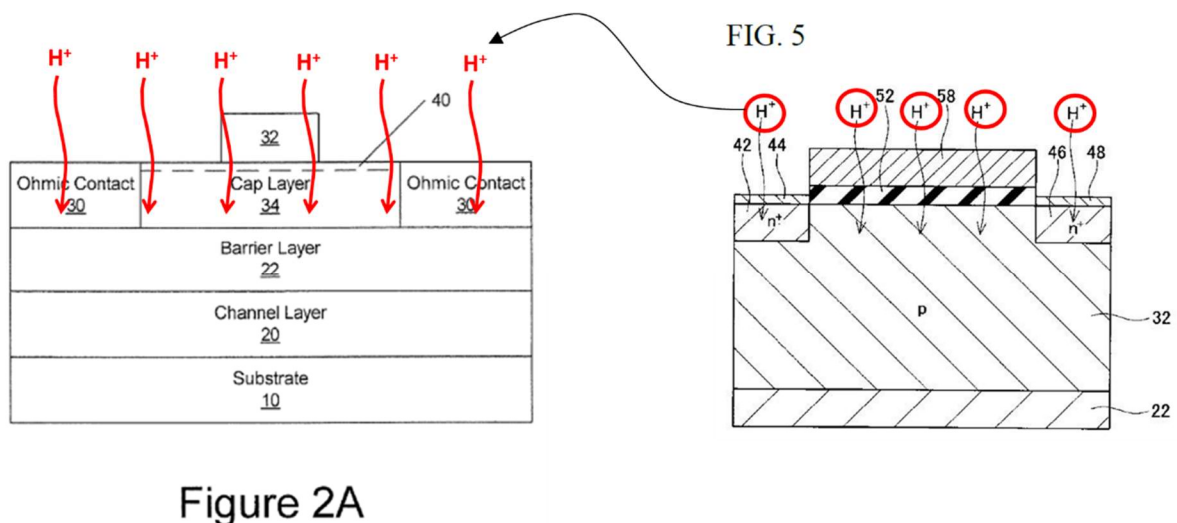
introduce traps or leakage paths by becoming a conductive layer.” *Smith*, [0087]. A POSITA would have understood *Smith*’s “level of doping” in cap layers was related to the level of active (non-passivated) impurities. Additionally, as discussed above in the technology background section, one of ordinary skill knew about hydrogen passivation and its effects on doping. One of ordinary skill knew that hydrogen passivation, and hydrogenation processes, adjusted the doping level.

[0126] Because a person of ordinary skill in the art knew that hydrogenation can affect the “level of doping” in GaN layers and *Smith* identified level of doping as a result effective variable, a person of ordinary skill in the art would have found it obvious to adjust doping in cap layers through hydrogenation. For example, to a person of ordinary skill in the art it would have been obvious to adjust the level of doping as a result-effective variable to control leakage, as disclosed by *Smith*, using hydrogenation seeking to improve the transistor’s characteristics.

[0127] *Smith*, by itself, motivates a person of ordinary skill to adjust the level of doping and to “compensate,” as the term is used in the ’294 patent, cap layers using the well-known hydrogenation processes.

**2. (Ground 1B) A person of ordinary skill would have been motivated to incorporate *Kigami*'s hydrogenation process in *Smith***

[0128] A person of ordinary skill in the art would have been motivated to apply *Kigami*'s processing step for hydrogenation to passivate impurities in *Smith*'s cap layers. Specifically, a person of ordinary skill in the art would have been motivated to use *Kigami*'s hydrogen incorporation through ionized gas to passivate impurities in *Smith*'s cap layer. For example, to a person of ordinary skill in the art it would have been obvious to employ *Kigami*'s ionized gas hydrogenation (*Kigami*, [0026]) to passivate impurities in *Smith*'s doped cap layer (*Smith*, [0085]). The resulting combination is exemplified in the figure below that modifies *Smith*'s Figure 2A based on *Kigami*'s Figure 5 to show the incorporation of *Kigami*'s hydrogenation in *Smith*:



*Smith*, Fig. 2A; *Kigami*, Fig. 5 (annotated to show their combination)

[0129] In my opinion, multiple rationales support the combination.

[0130] For example, *Smith* and *Kigami* are combinable because they are directed to the same field and the same techniques. Both *Smith* and *Kigami* relate to nitride-based transistors. *Smith*, Abstract; *Kigami*, Abstract. Both references specifically describe techniques for fabricating nitride High Electron Mobility Transistors (HEMTs). *Smith*, [0031]; *Kigami*, [0010]. And both references describe structures and techniques that seek to improve the HEMTs robustness and operation. *Smith*, [0064]; *Kigami*, [0010]. For example, *Smith* describes that its structures and processes “improve robustness of the device during processing and/or device operation.” *Smith*, [0063]. Similarly, *Kigami* states that its structures and fabrication methods seek to resolve transistor operation and robustness problems, enabling “a low threshold voltage and a high withstand voltage.” *Kigami*, [0006]-[0007]. *Smith* and *Kigami* are, thus, analogous art and a skilled artisan would have considered their teachings highly relevant and combinable.

[0131] Further, a person of ordinary skill in the art would have been motivated to modify *Smith*’s device in view of *Kigami* because *Kigami* suggests and motivates the combination of its disclosed techniques in III-nitride devices, like *Smith*’s. *Kigami* teaches that introducing hydrogen into GaN transistor layers, like those of *Smith*, improves transistor performance. *Kigami*, [0007]. In particular,

*Kigami* states that “utilizing the phenomenon in which the p-type impurity is inactivated by hydrogen atoms” to locally lower active impurity concentrations permits “having a low threshold voltage and a high withstand voltage.”

*Kigami*, [0007]. *Kigami* further suggests using its intentional hydrogen passivation explaining it has “effects of stabilized threshold voltage, increased switching speed, and the like.” *Kigami*, [0029]. In my opinion, *Kigami*’s touted advantages suggest the incorporation of *Kigami*’s techniques into *Smith* because a person of ordinary skill in the art would have considered these effects advantageous to *Smith*’s device. A person of ordinary skill in the art would have recognized that *Smith* was also concerned with improving the transistor’s operation. *Smith*, [0003]-[0007] (seeking to use transistors for “high frequency applications”); [0081] (seeking to adjust performance characteristics “such as threshold voltage, frequency performance, etc.”), [0089] (controlling the level of p-type or deep level dopants to reduce leakage current but not become a conductive layer or cause significant trapping). And a person of ordinary skill in the art would have recognized that *Kigami*’s techniques could be helpful to achieve *Smith*’s goals. Indeed, *Kigami* directly suggests applying his techniques to transistors that, like *Smith*’s, use magnesium dopants stating that its “invention is particularly useful in situations in which magnesium is used as a p-type impurity.” *Kigami*, [0012].

[0132] Moreover, a person of ordinary skill in the art would have also combined *Kigami* and *Smith* recognizing the combination to be the use of a known technique to improve a similar device. *Kigami*'s discloses a known technique, the hydrogen incorporation through ionized gas to locally lower the number of activated p-type impurities in GaN layers. *Kigami*, [0012]. *Kigami* explains that the incorporating of hydrogen reduces the transistor's threshold voltage, maintains a high "withstand" (or breakdown) voltage, and increases switching speed. *Kigami*, [0007]-[0008], [0029]. Accordingly, a person of ordinary skill in the art would have been motivated to use *Kigami*'s technique to improve *Smith*'s transistor in the same way because *Smith* also had the goal of controlling the transistor's threshold voltage, having high breakdown, operating at high frequencies, and controlling the level of doping. *Smith*, [0003]-[0007], [0081], [0087]. In my opinion, a person of ordinary skill in the art would have seen *Smith*'s transistor as a base device that could be improved with *Kigami*'s hydrogenation technique. *Smith*, [0003]-[0007], [0081], [0087]. And because *Smith*'s and *Kigami*'s devices are comparable, both being nitride transistors, a person of ordinary skill in the art would have applied *Kigami*'s technique to *Smith*'s device in the same way.

[0133] Moreover, in my opinion a person of ordinary skill in the art would have implemented *Kigami*'s suggested incorporation of hydrogen in *Smith*'s

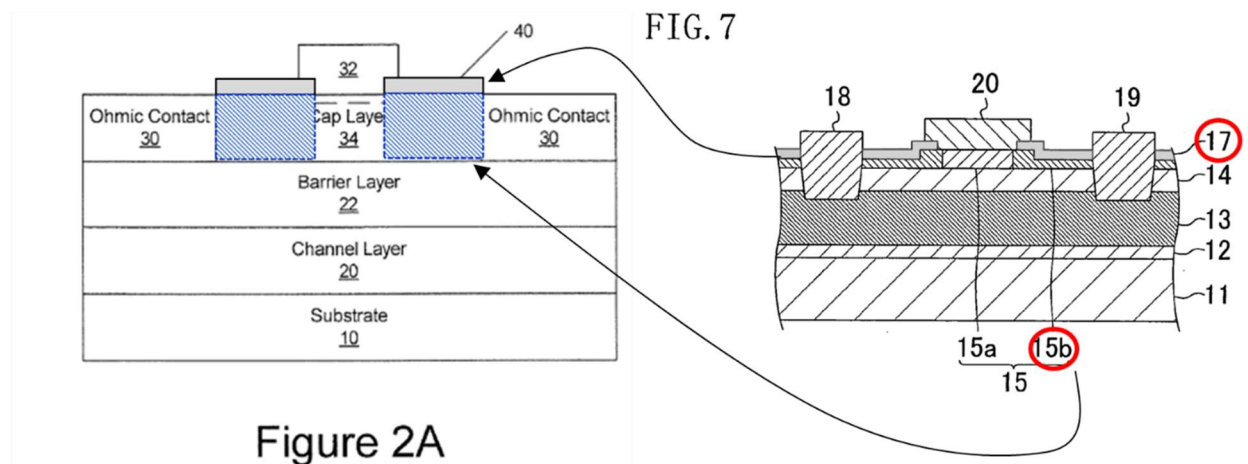
transistor with a reasonable expectation of success. By April 2009, the earliest priority for the '294 patent, it was well-known that hydrogen passivated impurities in GaN layers and affected the layer's conductivity. *Prosecution History*, 88. *Kigami* also provides experimental data showing the effect of introducing hydrogen atoms in transistor performance. *Kigami*, [0028], Fig. 6. And *Kigami* explains the mechanisms for hydrogen diffusion and impurity passivation, detailing how the hydrogen diffusion would be performed. *Kigami*, [0022]-[0026], Fig. 5. In view of its general knowledge about doping and passivation, and in view of *Kigami*'s disclosure, it is my opinion that a person of ordinary skill in the art would have had a reasonable expectation of success in modifying *Smith* with *Kigami*'s hydrogen incorporation technique.

**3. (Ground 1C) A person of ordinary skill would have been motivated to modify *Smith* to include a hydrogen diffusion layer and diffuse hydrogen in the AlGaN layer, as disclose in *Uemoto***

[0134] In my opinion, a person of ordinary skill in the art would also have been motivated to apply *Uemoto*'s hydrogen diffusion technique to selectively increase the resistivity of *Smith*'s cap layers. Particularly, a person of ordinary skill in the art would have been motivated to use *Uemoto*'s "hydrogen diffusion film 17" in *Smith*'s transistor to from the "high resistive region 15b" because *Uemoto* teaches the incorporation of the hydrogen diffusion film helps reducing

gate leakage and *Smith* was also concerned with reducing leakage. *Uemoto*, [0059], [0063]; *Smith*, [0085].

[0135] In my opinion, a person of ordinary skill in the art it would have found it obvious to use *Uemoto*'s hydrogen diffusion film in *Smith*'s cap layer seeking to selectively inactive impurities, generate the highly resistive regions, and reduce leakage. The resulting combination is exemplified in the figure below that modifies *Smith*'s Figure 2A based on *Uemoto*'s Figure 7 to show the incorporation of *Uemoto*'s hydrogen diffusion film in *Smith*:



*Smith*, Fig. 2A; *Uemoto*, Fig. 7 (annotated to show their combination)

[0136] In my opinion, multiple rationales support the combination.

[0137] *Smith* and *Uemoto* are combinable because they both relate to III-nitride transistors. *Smith*, Abstract; *Uemoto*, [0003]. Specifically, both references describe techniques for fabricating transistors with gallium nitride. *Smith*, [0031];

*Uemoto*, [0005]. And both references describe structures and techniques that seek to improve transistor operation by, for example, reducing leakage currents.

*Smith*, [0064], [0087], [0089]; *Uemoto*, [0059]. Therefore, *Smith* and *Uemoto* are analogous art and a person of ordinary skill in the art would have considered their teachings highly relevant and combinable.

[0138] Moreover, a person of ordinary skill in the art would have been motivated to modify *Smith*'s device in view of *Uemoto* because *Uemoto* suggests and motivates the modification by teaching the formation of the highly resistive regions through hydrogen diffusion improves transistor performance and stability.

*Uemoto* suggests using a hydrogen diffusion film to selectively inactivate impurities in a GaN layer, explaining that inactivating impurities increases and stabilize resistivity, and reduce leakage. *Uemoto*, [0059], [0063]. *Uemoto* teaches that the diffusion film releases hydrogen during a thermal treatment, selectively inactivating impurities and enhancing resistivity. *Uemoto*, [0063]-[0068], Fig. 8.

*Uemoto* also teaches that with its hydrogen diffusion technique "a greater amount of leakage current between the gate and the drain can be reduced."

*Uemoto*, [0059]. In my opinion, a person of ordinary skill in the art would have considered *Uemoto*'s reduction of leakage current advantageous to *Smith*'s device because *Smith* was also concerned with fabrication methods that reduce transistor

leakage. *Smith*, [0087], [0089] (describing doping considerations “to reduce leakage currents”). Indeed, *Uemoto* directly suggests applying his techniques to fabrication of nitride transistors—like *Smith*’s—stating that his invention “is useful for a nitride semiconductor transistor such as a power transistor with a high breakdown voltage, and for its fabrication method.” *Uemoto*, [0079].

[0139] A person of ordinary skill would, in my opinion, have also been motivated to combine *Uemoto* and *Smith* recognizing it was the application of a known technique to improve a similar device. In particular, a person of ordinary skill in the art would have been motivated to apply *Uemoto*’s hydrogen diffusion method to *Smith*’s transistor, because a person of ordinary skill in the art would have recognized that *Uemoto*’s method to selectively increase resistivity could improve *Smith*. *Uemoto* discloses that its hydrogen diffusion technique reduces leakage current. *Uemoto*, [0059]. A person of ordinary skill in the art would have been motivated to use *Uemoto*’s technique to improve *Smith*’s transistor in the same way. *Smith* was also concerned with reducing the leakage current in its transistors and used the same materials, dopants, and structures as *Uemoto*. *Smith*, [0064], FIG 2A; *Uemoto*, [0054], Fig. 7. Because *Smith* and *Uemoto*’s devices are comparable, a person of ordinary skill in the art would have been

motivated to take *Smith*'s transistor as a base device and improve it with *Uemoto*'s hydrogen diffusion to form high resistive regions and reduce leakage.

[0140] Additionally, it is my opinion that a person of ordinary skill in the art would have incorporated *Uemoto*'s hydrogen diffusion film technique to *Smith* with a reasonable expectation of success. The mechanisms and effects of hydrogen incorporation into doped GaN layers had been well-established by 2009.

*Prosecution History*, 88. And *Uemoto* provides both experimental data and theoretical analyses that support the use of the hydrogen diffusion film to selectively increase resistivity and improve transistor characteristics.

*Uemoto*, [0038], [0049], Figs. 4-8. In view of its general knowledge and *Uemoto*'s disclosure, a person of ordinary skill in the art would have incorporated *Uemoto*'s hydrogen diffusion technique to *Smith* with a reasonable expectation of success.

#### **D. Independent Claim 1**

[0141] In my opinion, *Smith*, alone or in combination with *Kigami* or *Uemoto*, renders claim 1 obvious.

##### **1. [1p] A column III Nitride transistor comprising:**

[0142] *Smith* discloses a column III Nitride transistor. *Smith* specifies its invention relates to “transistors that incorporate nitride-based active layers” and discloses (and claims) a “Group III-nitride high electron mobility transistor

(HEMT).” *Smith*, [0002], [0008], Claim 1. *Smith* also explains its invention can be used for “nitride-based devices such as Group III-nitride based HEMTs.”

*Smith*, [0060]. And in the figures, *Smith* illustrates cross-sectional schematics of the transistors. In Figure 2A, for example, *Smith* illustrates the “cross-sectional schematic” of one of its transistors.

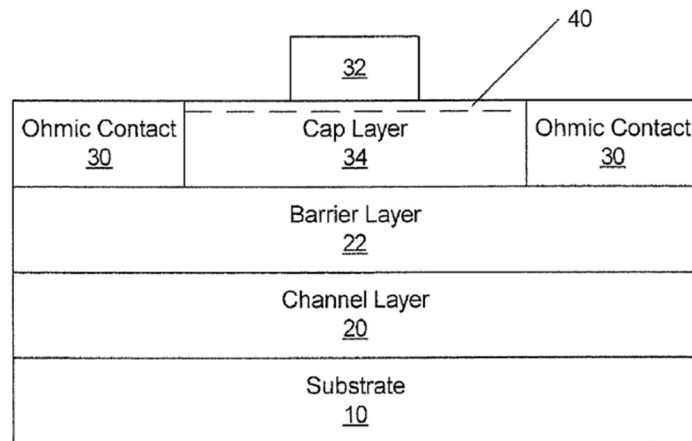


Figure 2A

*Smith*, Fig. 2A

**2. [1a] a substrate,**

[0143] *Smith* discloses a substrate. Specifically, *Smith* discloses a “substrate 10 . . . on which nitride based devices may be formed.” *Smith*, [0069]. Additionally, *Smith* discloses the same substrate materials and the ’294 patent. Like the ’294 patent, *Smith* discloses the substrate can be formed with silicon

carbide (SiC). *Smith*, [0069]; '294 patent, 2:58-59. Annotated Figure 2A below highlights *Smith*'s **substrate 10**.

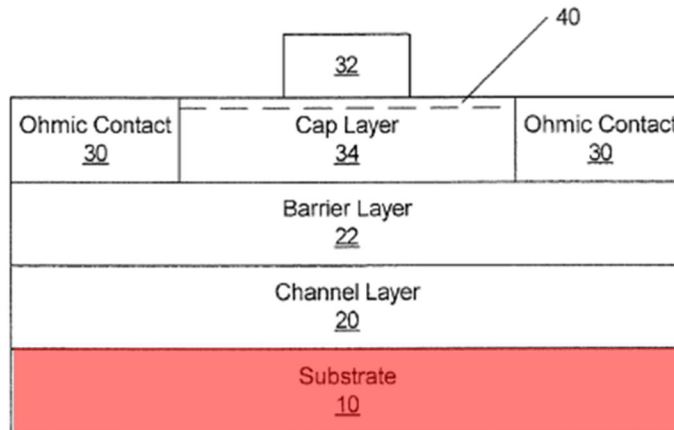


Figure 2A

*Smith*, Fig. 2A (annotated)

3. [1b] a set of III-N transition layers above the substrate,

[0144] *Smith* discloses a set of III-N transition layers above the substrate.

*Smith* discloses the transistor includes “transition layers” that “may be provided on the **substrate 10**.” *Smith*, [0070]. *Smith* discloses the transition layers can be formed with a III-N material, AlN specifically. *Smith*, [0070]. This is the same material specified in the '294 patent for transition layers. *Compare Smith*, [0070] (describing AlN transition layers) *with* '294 patent, 1:58-59 (same).

[0145] Figure 2A below is annotated to illustrates *Smith*'s **transition layers**, which *Smith* describes but does not show, above **substrate 10**.

*Smith*, [0070](“**transition layers** (not shown) may be provided on the **substrate 10**”).

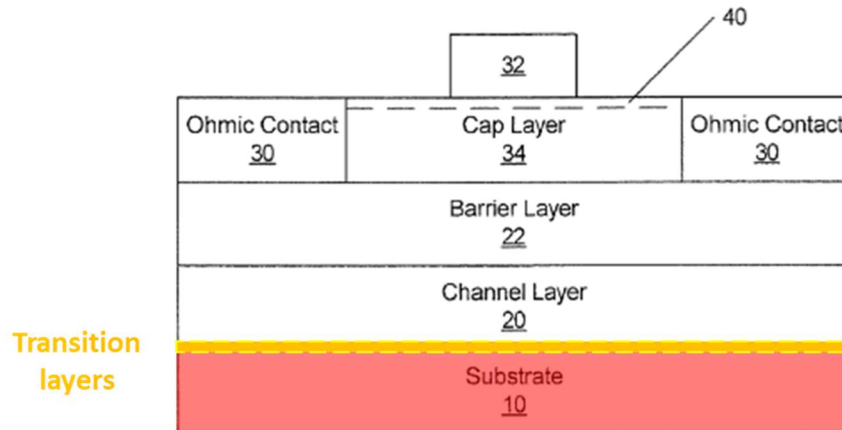


Figure 2A

*Smith*, Fig. 2A (annotated and modified to show the “transition layers” described in *Smith* paragraph [0070])

4. [1c] a III-N buffer layer above the set of transition layers,

[0146] *Smith* discloses a III-N buffer layer above the set of transition layers.

In my opinion, *Smith* discloses this element by disclosing a “channel layer 20 [that] may be deposited on the **substrate 10** using buffer layers, **transition layers**, and/or nucleation layers.” *Smith*, [0073].

[0147] *Smith* discloses the “channel layer 20 is a Group III-nitride, such as  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  where  $0 \leq x < 1$ ” (*Smith*, [0074]), describing overlapping formulations to the ones the '294 patent associates with the buffer layer. '294 patent, 2:63-65 (describing “InAlGaN with any concentration of In and Al (including 0%. In

and/or Al)"). And *Smith*'s channel layer serves the same function of "separat[ing] the transition layers 32 from a barrier layer 34" ('294 patent, 2:63) as the buffer layer in the '294 patent. *Smith*, [0070], [0073].

[0148] I have been informed that the difference in nomenclature does not affect an unpatentability analysis because having the same terminology is not required, the prior art need not use the same terminology as the challenged claims. Therefore, while *Smith* and the '294 patent use different nomenclatures (the '294 patent using buffer layer and *Smith* using channel layer), in my opinion *Smith* discloses the "III-N buffer layer" of [1c] by describing the "channel layer 20." *Smith*, [0074].

[0149] Annotated Figure 2A highlights *Smith*'s **channel layer 20**, above the **transition layers**.

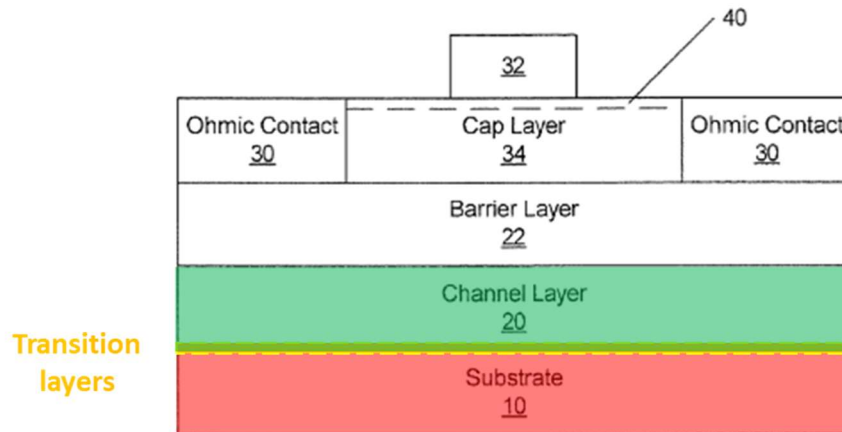


Figure 2A

*Smith*, Fig. 2A (annotated and modified)

**5. [1d] a III-N barrier layer above the buffer layer,**

[0150] *Smith* discloses a III-N barrier layer above the buffer layer. *Smith*'s transistor comprises a "barrier layer 22 [that] is provided on the channel layer 20." *Smith*, [0075]. *Smith* discloses "[t]he barrier layer 22 may be a Group III-nitride." *Smith*, [0075]. And like the '294 patent, *Smith* discloses the barrier layer is formed with AlGaN. Compare *Smith*, [0075] ("barrier layer 22 is AlN, AlInN, **AlGa**N or AlInGaN") with '294 patent, 2:66-67 ("barrier layer 34 is formed of AlGaN"). *Smith*'s **barrier layer 22** is highlighted below in annotated Figure 2A, above **channel layer 20**.

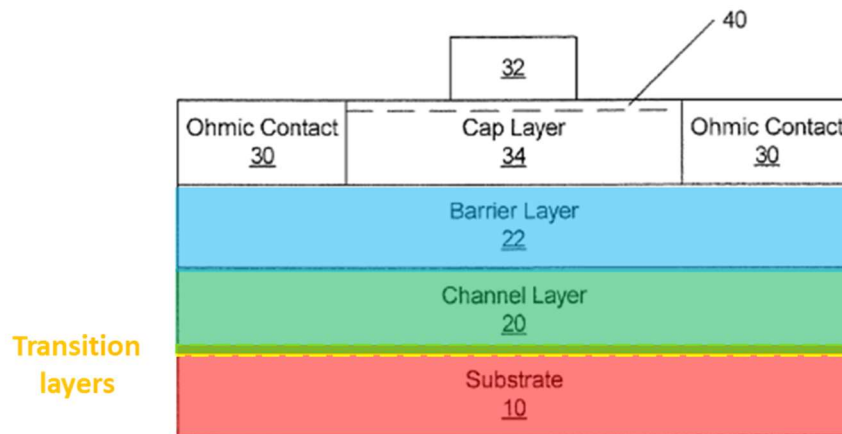


Figure 2A

*Smith*, Fig. 2A (annotated and modified)

**6. [1e] a compensated GaN layer above the barrier layer, and**

[0151] *Smith*, alone or in view of *Kigami* or *Uemoto*, render “a compensated GaN layer above the barrier layer” obvious under both proposed constructions of “a compensated GaN layer.”

[0152] *Smith* teaches a “GaN layer above the barrier layer” by disclosing a “cap layer 34.” *Smith*, [0035]. *Smith* specifies “cap layer 34, 34’ may be a GaN based cap layer, such as a GaN layer.” *Smith*, [0035]. *Smith* further discloses the cap layer being doped, with “a dopant incorporated throughout the cap layer 34” and a “doped region 40 [that] may be provided by a region of increased dopant concentration.” *Smith*, [0085]. *Smith* teaches that the level of doping should be controlled to be high enough to reduce leakage current, but low enough to not act

as a conductive layer. *Smith*, [0087]. *Smith*'s **cap layer 34** is highlighted below in annotated Figure 2A, showing **cap layer 34** above the **barrier layer 22**.

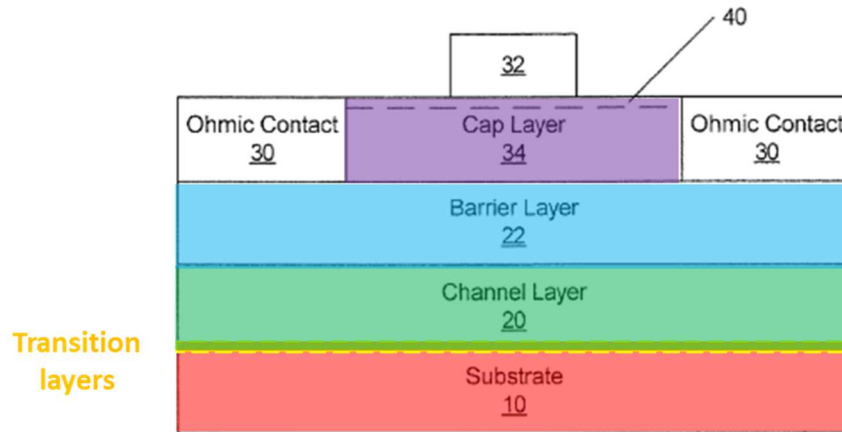


Figure 2A

*Smith*, Fig. 2A (annotated and modified)

**Mapping Under Petitioner's Construction**

[0153] If “a compensated GaN layer” is construed as “*doped GaN layer formed with a step to passivate its impurities,*” as Petitioner proposes, *Smith*, alone or in combination with *Kigami* or *Uemoto*, render element [1e] obvious.

[0154] In Ground 1A, *Smith* itself renders obvious element [1e]. As discussed above, in the claim construction section, I understand that under Petitioner's construction element [1e] should be interpreted as a “product-by-process” limitation. Under such interpretation, any prior art with the resulting structure meets the limitation, even if it was achieved with a different process.

And, in my opinion, *Smith* discloses the resulting structure required by [1e] because *Smith* discloses **cap layer 34** is doped with acceptors (*Smith*, [0087]) and it was well known that “as-grown GaN films are hydrogen passivated.” *Nakamura*, p. 1265. A person of ordinary skill in the art, thus, would have recognized that *Smith*’s **cap layer 34** is a “doped GaN layer formed with a step to passivate its impurities,” regardless of the specific compensation process.

[0155] Further, still in Ground 1A, if the “compensated GaN layer” limitation is construed as proposed by the Petition but not interpreted as product-by-process, *Smith* would still render element [1e] obvious. *Smith* identifies the level of doping as a result effective variable to control leakage. *Smith*, [0087] (“The level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths by becoming a conductive layer”). And a person of ordinary skill in the art knew that hydrogenation affected the level of doping. Because a person of ordinary skill in the art knew that hydrogenation can affect the “level of doping” in a GaN layer, and *Smith* identified the level of doping as a result-effective variable, a person of ordinary skill in the art would have found it obvious to adjust doping in **cap layer 34** “with a step to passivate its impurities,” as required by [1e] when properly construed.

[0156] For Ground 1B, the combination of *Smith* and *Kigami* discloses [1e] because applying *Kigami*'s hydrogenation to *Smith* "compensates" (as the term is used in the '294 patent) **cap layer 34**. A person of ordinary skill would have recognized that applying *Kigami*'s ionized gas hydrogenation to *Smith* makes **cap layer 34** results in a "doped GaN layer formed with a step to passivate its impurities," Petitioner's proposed construction. *ITC Constructions*, p. 9. And, as I analyzed above, a person of ordinary skill in the art would have been motivated to apply *Kigami*'s hydrogenation of GaN layers to *Smith*. Such modification would introduce hydrogen into *Smith*'s **cap layer 34**, passivating its acceptor impurities. Therefore, when modified based on *Kigami*, *Smith*'s **cap layer 34** would be a "doped GaN layer formed with a step to passivate its impurities." The combination of *Smith* and *Kigami*, therefore, render element [1e] obvious.

[0157] In Ground 1C, the combination of *Smith* and *Uemoto* also discloses [1e] because applying *Uemoto*'s technique to selectively diffuse hydrogen would result in **cap layer 34** being "compensated," as the term is used in the '294 patent. Incorporating *Uemoto*'s hydrogen diffusion technique, using a hydrogen diffusion film and a thermal diffusion, to *Smith* makes **cap layer 34** a "doped GaN layer formed with a step to passivate its impurities," Petitioner's proposed construction. *ITC Constructions*, p. 9. As discussed above, a person of ordinary skill in the art

would have found it obvious to use *Uemoto*'s technique to selectively diffuse hydrogen into *Smith*'s **cap layer 34**. Such modification introduces hydrogen in **cap layer 34** and passivates acceptor impurities to form high resistive regions that reduce leakage. If combined with *Uemoto*, *Smith*'s **cap layer 34** would be a "doped GaN layer formed with a step to passivate its impurities." The combination of *Smith* and *Uemoto*, therefore, render element [1e] obvious.

#### **Mapping Under Patent Owner Construction**

[0158] In my opinion, *Smith*, alone or in combination with *Kigami* or *Uemoto*, discloses element [1e] when the term "compensated GaN layer" is properly construed with Petitioner's construction. But *Smith* itself, and when combined with *Kigami* or *Uemoto*, also discloses [1e] under the Patent Owner's construction.

[0159] First, Patent Owner's proposed construction is vague and overly broad. As I analyzed above, a person of ordinary skill would understand Patent Owner's construction encompasses Petitioner's construction (and indeed, virtually all GaN based semiconductor materials). So any reference which demonstrates limitation [1e] under Petitioner's construction would show it under Patent Owner's construction. Nonetheless, **Grounds 1A-1C**, also explicitly disclose limitation [1e] under Petitioner's construction.

[0160] In Ground 1A, If “compensated GaN layer” is construed with Patent Owner’s proposal (as “A semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)”), *Smith* discloses element [1e]. *Smith* specifies that **cap layer 34** is a GaN layer doped with a “p-type dopant, such as Mg, Be, Zn, Ca, and/or C.” *Smith*, [0085]. As explained in the technical background, by 2009 it was well-known that hydrogen would be naturally present in such layers. It was known that hydrogen would be present even in as-grown GaN materials, forming acceptor-H neutral complexes that passivate the impurity. *Nakamura*, pp. 1265-1266; *Quay*, §3.3.1. Therefore, if “compensated GaN layer” is construed as the Patent Owner proposed, *Smith* discloses [1e] by disclosing the acceptor-doped **cap layer 34**. *Smith*’s **cap layer 34** is a “semiconductor GaN gate material” because it is formed with GaN and is part of the gate material. *Smith*, [0085], [0087], Fig. 2A. And *Smith*’s **cap layer 34** is a material “in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)” because: in *Smith*’s **cap layer 34** the innate hydrogen is “one type of dopant, impurity, or imperfection;” the magnesium (or acceptors) from *Smith*’s doping is “other type of

dopant, impurity, or imperfection (for example, acceptor);” and the hydrogen “partially cancels” (as the term appears to be used in Patent Owner’s construction) the electric effects of magnesium by forming the Mg-H complexes. Accordingly, *Smith* itself discloses “a compensated GaN layer” if the term is construed as proposed by the Patent Owner.

[0161] In Ground 1B, the combination of *Smith* and *Kigami* also discloses element [1e] under the Patent Owner’s construction. If “compensated GaN layer” is construed as proposed by the Patent Owner (as “A semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)”) *Smith* combined with *Kigami* renders element [1e] obvious. *Smith* discloses **cap layer 34** is doped with magnesium. *Smith*, [0087]. And *Kigami* discloses the incorporation of hydrogen.

*Kigami*, [0027]. Thus, when *Smith* is combined with *Kigami*, *Smith*’s **cap layer 34** would be a “compensated GaN layer” under Patent Owner’s construction. *Smith*’s **cap layer 34** is a “semiconductor GaN gate material” because it is formed with GaN and is part of the gate material. *Smith*, [0085], [0087], Fig. 2A. And in the combination of *Smith* and *Kigami*, *Smith*’s **cap layer 34** is a material “in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the

electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)” because the hydrogen incorporated with *Kigami*’s hydrogen is “one type of dopant, impurity, or imperfection;” *Smith*’s **cap layer 34** is doped with acceptors (such as magnesium) (*Smith*, [0085]); and, as discussed in *Kigami*, the hydrogen introduced with *Kigami*’s process “partially cancels” (as the term appears to be used in Patent Owner’s construction) the electric effects of magnesium by inactivating it (*Kigami*, [0012]). The combination of *Smith* and *Kigami* in Ground 1B, therefore, makes *Smith*’s **cap layer 34** a “semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor).” *ITC Constructions*, p. 1.

[0162] In Ground 1C, the combination of *Smith* with *Uemoto* discloses element [1e] under the Patent Owner’s construction. If “compensated GaN layer” is interpreted to be “semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor),” the *Smith* and *Uemoto* combination render [1e] obvious. *Smith*’s **cap layer 34** is a “semiconductor GaN gate material” because it is formed with GaN and is part of the gate material. *Smith*, [0085], [0087], Fig. 2A. And in the

combination of *Smith* and *Uemoto*, *Smith*'s **cap layer 34** is a material "in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)" because the hydrogen incorporated with *Uemoto*'s diffusion technique is "one type of dopant, impurity, or imperfection;" *Smith*'s **cap layer 34** is doped with acceptors (such as magnesium); and, as disclosed in *Uemoto*, the hydrogen "partially cancels" (as the term appears to be used in Patent Owner's construction) the electric effects of magnesium by inactivating it (*Uemoto*, [0063]). The combination of *Smith* and *Uemoto* in Ground 1C, therefore, makes *Smith*'s **cap layer 34** a "semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)." *ITC Constructions*, p. 1.

[0163] Therefore, *Smith*, alone or in combination with *Kigami* or *Uemoto*, also disclose element [1e] when the term "compensated GaN layer" is with Patent Owner's construction.

**7. [1f] a gate contact above the compensated GaN layer.**

[0164] *Smith* discloses a gate contact above the compensated GaN layer. *Smith*'s transistor comprises a "gate contact 32 may also be formed on the cap

layer.” *Smith*, [0082], [0085]. And *Smith* discloses embodiments in which “the gate contact 32 is provided directly on the doped region 40.” *Smith*, [0088]. Further, *Smith* discloses the gate contact being formed with “conventional materials capable of making a Schottky contact to a nitride based semiconductor . . . such as Ni, Pt, NiSix, Cu, Pd, Cr, W and/or WSiN.” *Smith*, [0082]. These are the materials the ’294 patent specifies for the gate contact. ’294 patent, 3:4-5 (“gate contact 37, formed of for example, Ta, Ti, TiN, W, or WSi2”). *Smith*’s **gate contact 32** is highlighted below, in annotated Figure 2A, and shown above **cap layer 14**.

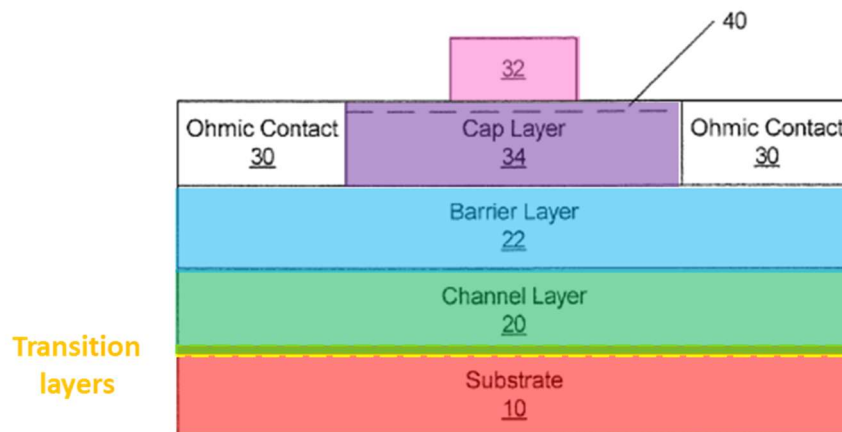


Figure 2A

*Smith*, Fig. 2A (annotated and modified)

**A. Claim 2- The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.**

[0165] *Smith*, alone or in combination with *Kigami* or *Uemoto*, discloses “the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.”

[0166] In Ground 1A, *Smith* itself renders the limitation in claim 2 obvious because by 2009 a person of ordinary skill in the art knew that in as-grown layers hydrogen passivates acceptor type dopants. As I explained above, by 2009, a person of ordinary skill in the art knew that hydrogen is naturally present in as-grown GaN layers and that hydrogen forms complexes with acceptor dopants, inactivating or passivating them. Because *Smith* discloses **cap layer 34** being doped with p-type dopants (i.e., acceptors), a person of ordinary skill in the art would have recognized that *Smith*’s **cap layer 34** would be naturally passivated with hydrogen. Therefore, *Smith* alone discloses Claim 2’s limitation.

[0167] In Grounds 1B, *Smith* in combination with *Kigami* renders the limitation of claim 2 obvious because *Kigami* discloses that acceptor dopants are passivated with hydrogen. For example, *Kigami* discloses that “introduced hydrogen atoms inactivate the p-type impurity.” *Kigami*, [0014]. When combined as explained above, with hydrogen being incorporated into *Smith*’s **cap layer 34**,

using *Kigami*'s hydrogenation, the combination of *Smith* and *Kigami* results in **cap layer 34** containing acceptor type dopants atoms passivated with hydrogen. The *Smith* and *Kigami* combination, therefore, renders Claim 2's limitation obvious.

[0168] In Grounds 1C, *Smith* in combination with *Uemoto* renders the limitation of claim 2 obvious because *Uemoto* discloses that acceptor dopants are passivated with hydrogen. For example, *Uemoto* discloses that magnesium (an acceptor type atom) is inactivated when combined with a hydrogen atom. *Uemoto*, [0049]. When combined as discussed above, with hydrogen being diffused into *Smith*'s **cap layer 34**, using *Uemoto*'s hydrogen diffusion method, the combination of *Smith* and *Uemoto* results in **cap layer 34** containing acceptor type dopants atoms passivated with hydrogen. The *Smith* and *Uemoto* combination, therefore, also renders Claim 2's limitation obvious.

**B. Claim 3 - The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.**

[0169] *Smith* discloses "the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca." *Smith* discloses that **cap layer 34** can be doped with p-type dopants, including "Mg, Be, Zn, Ca and/or C." *Smith*, [0087]. Therefore, *Smith* discloses the same elements for acceptor type dopants recited in the claim.

**C. Independent Claim 4****1. [4p] A column III Nitride transistor comprising:**

**[0170]** The preamble of claim 4 is the same as the preamble in claim 1. As further discussed above, *Smith* discloses the preamble of claim 4. My analysis for claim's 1 preamble applies to claim 4.

**2. [4a] a substrate,**

**[0171]** Feature [4a] of claim 4 is the same as feature [1a] of claim 1. My analysis for [1a] applies to [4a]. *Smith* discloses this feature of claim 4.

**3. [4b] a set of III-N transition layers above the substrate,**

**[0172]** Feature [4b] of claim 4 is the same as feature [1b] of claim 1. My analysis for [1b] applies to [4b]. *Smith* discloses this feature of claim 4.

**4. [4c] a III-N buffer layer above the set of transition layers,**

**[0173]** Feature [4c] is the same as feature [1c]. My analysis for [1c] applies to [4c]. *Smith* thus discloses this feature of claim 4.

**5. [4d] a III-N barrier layer, and**

**[0174]** Feature [4d] of claim 4 is substantially similar to feature [1d] of claim 1. The primary difference between [4d] and [1d] is that [4d] does not require the barrier layer to be “above the buffer layer.” While [1d] recites “a III-N buffer layer above the set of transition layers,” [4d] only recites “a III-N barrier layer,” without requiring “above the set of transition layers.” As element [4d] is broader

than [1d], my analysis of unpatentability of element [1d] applies to [4d]. *Smith* discloses this feature of claim 4.

**6. [4e] a semi-insulating III-N layer above the barrier layer.**

[0175] *Smith* discloses a semi-insulating III-N layer above the barrier layer. *Smith* discloses that cap layer 34 can be a “semi-insulating III-N layer.” *Smith*, [0085]. *Smith* discloses that cap layer 34 can be formed with “[t]echniques for co-doping Group III-nitride materials.” *Smith*, [0085]. And, in *Saxler874* (Ex. 1016, which *Smith*’s incorporated by reference), *Smith* explains that the disclosed co-doping “provide semi-insulating Group III nitride semiconductor layers.” *Saxler874*, [0005]. Further, like the ’294 patent, *Smith* discloses the semi-insulating layer being formed with AlGaN or GaN, doped with deep level impurity atoms. *Compare Smith*, [0089] (“cap layer 34, 34’ may be a GaN based cap layer, such as a GaN layer and/or an AlGaN . . . deep level dopants may be Fe, C, V, Cr, Mn, Ni, Co) with ’294 patent, 2:66-67 (“Semi-insulating layer 39 may comprise, for example, AlGaN or GaN, with deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni”).

[0176] *Smith*, thus, discloses cap layer 34, being “a semi-insulating III-N layer,” disclosing element [4e]. *Smith*’s **semi-insulating cap layer 34** is highlighted below in annotated Figure 2A, showing it above **barrier layer 22**.

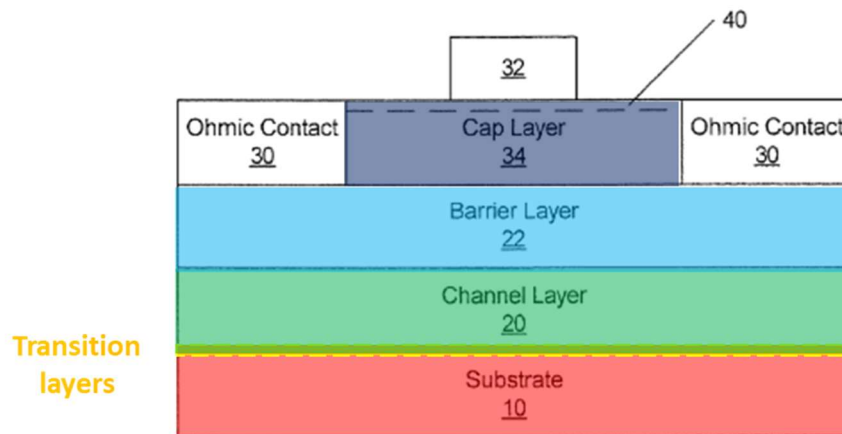


Figure 2A

*Smith*, Fig. 2A (annotated and modified)

**D. Claim 5- The transistor of claim 4, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms.**

[0177] *Smith* discloses the semi-insulating III-N layer contains deep acceptor type dopant atoms. *Smith* discloses **semi-insulating cap layer 34** includes “a region doped with deep level dopants.” *Smith*, [0089]. *Smith* further discloses acceptor deep level dopants providing deep level dopant acceptors such as “Fe, C, V, Cr, Mn, Ni and/or Co.” *Smith*, [0085]. These are the same deep level dopants the 294 patent identifies as “deep acceptor type.” ’294 patent, Claim 6. Further, in my opinion a person of ordinary skill in the art would have recognized *Smith*’s disclosure of carbon doping as p-type (acceptor) doping. *Quay*, §3.3.1.

Accordingly, *Smith* discloses Claim 5’s limitation.

**E. Claim 6 - The transistor of claim 5 where the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.**

[0178] *Smith* discloses “the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.” *Smith* discloses cap layer 34 being “doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co.” *Smith*, [0015], [0089]. Therefore, *Smith* discloses the same elements for deep acceptor type dopants recited in the claim.

**F. Independent Claim 7**

**1. [7p] A column III Nitride transistor comprising:**

[0179] The preamble of claim 7 is the same as the preamble in claims 1 and 4. My analysis for claims’ 1 and 4 preambles apply to claim 7. As discussed above, *Smith* discloses the preamble of claim 7.

**2. [7a] a substrate,**

[0180] Feature [7a] of claim 7 is the same as features [1a] of claim 1 and [4a] of claim 7. My analyses for [1a] and [4a] apply to [7a]. *Smith* discloses this feature of claim 7.

**3. [7b] a set of III-N transition layers above the substrate,**

[0181] Feature [7b] of claim 7 is the same as features [1b] of claim 1 and [4b] of claim 7. My analyses for [1b] and [4b] apply to [7b]. *Smith* discloses this feature of claim 7.

4. [7c] a III-N buffer layer above the set of transition layers,

[0182] Feature [7c] of claim 7 is the same as features [1c] of claim 1 and [4c] of claim 7. My analyses for [1c] and [4c] apply to [7b]. *Smith* discloses this feature of claim 7.

5. [7d] a III-N barrier layer, and

[0183] Feature [7d] of claim 7 is the same as feature [4d] of claim 4. My analysis for [4d] applies to [7d]. *Smith* thus discloses this feature of claim 7.

6. [7e] a semi-insulating III-N layer above the barrier layer, and

[0184] Feature [7e] of claim 7 is the same as feature [4e] of claim 4. My analysis for [4e] applies to [7e]. *Smith* thus discloses this feature of claim 7.

7. [7f] a confinement layer above the semi-insulating III-N layer.

[0185] *Smith*, alone or in combination with *Uemoto*, discloses a confinement layer above the semi-insulating III-N layer.

[0186] In Ground 1A, *Smith* itself discloses this feature by disclosing a “passivation layer” above **semi-insulating cap layer 34**. *Smith* discloses a “passivation layer 100” formed on its cap layers—including **semi-insulating cap layer 34**. *Smith*, [0095] (“While FIGS. 3A, 3B and 4A, 4B illustrate passivation layers 100, 100' and 110, 110' on a cap layer 24, other cap layers, such as the cap layer 34”). *Smith* discloses the “passivation layer 100, 100' may be provided as a

single layer or may be multiple layers and may be incorporated with layers of other materials, such as SiN or SiOx.” *Smith*, [0090]. *Smith*’s passivation layer is composed with the same materials the ’294 patent associates with the confinement layer. ’294 patent, 2:63-65 (describing the “confinement layer can be composed of AlGaN, SiN, SiO<sub>2</sub>, or other insulating material.”). Despite the difference in nomenclature, *Smith* discloses the “confinement layer” of [7f] by describing the “passivation layer 100.” *Smith*, [0090]-[0095].

[0187] Annotated Figure 3B, modified to show **semi-insulating cap layer 34** instead of cap layer 24 (as disclosed in *Smith*’s paragraph [0095]), highlights *Smith*’s **passivation layer**, above the **semi-insulating cap layer 34**.

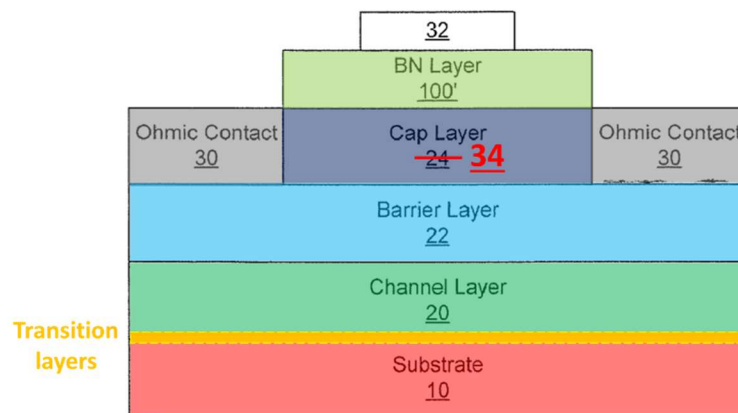


Figure 3B

*Smith*, Fig. 3B (annotated and modified to show transition layers and substitute “cap layer 24” for “cap layer 34”)

[0188] In Ground 1C, the combination of *Smith* and *Uemoto* also discloses “a confinement layer above the semi-insulating III-N layer.” When *Smith* is combined with *Uemoto* to include a “hydrogen diffusion film,” the “diffusion film” becomes “a confinement layer above the semi-insulating III-N layer.” *Uemoto* discloses the hydrogen diffusion film is “made of silicon nitride (SiN).” *Uemoto*, [0063]. The diffusion film is, thus, made of the same material the ’294 patent associates with the “confinement layer.” ’294 patent, 4:34-35 (defining “confinement layer can be composed of AlGa<sub>N</sub>. SiN. SiO<sub>2</sub>”). As discussed above, a person of ordinary skill in the art would have been motivated incorporate *Uemoto*’s hydrogen diffusion film on *Smith*’s cap layers.

[0189] Annotated Figure 2B below, modified to show *Uemoto*’s hydrogen diffusion film incorporate in *Smith*, shows that in the combination of *Smith* and *Uemoto*, *Uemoto*’s **hydrogen diffusion film** is above **semi-insulating cap layer 34**.

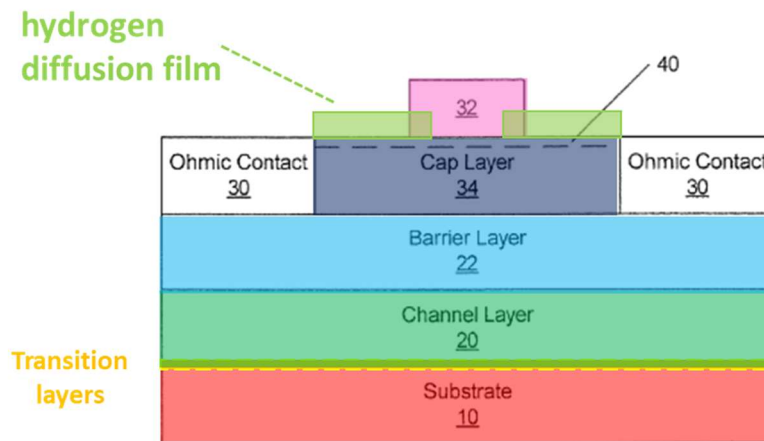


Figure 2A

*Smith*, Fig. 2A (annotated and modified to include *Uemoto*'s "hydrogen diffusion film")

- G. Claim 8 - The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.**

[0190] The limitation of claim 8 is substantially similar to the limitation of claim 6. While claim 6 only requires "the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V," claim 6 depends from claim 5, which requires "the semi-insulating III-N layer contains deep acceptor type dopant atoms." Claims 8 and 6, thus, have substantially similar scope. My analysis for claim 6 applies to claim 8. Therefore, *Smith* discloses claim 8's limitation.

**H. Claim 9 - The transistor of claim 7, wherein the confinement layer is made of SiN, SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, Ga<sub>2</sub>O<sub>3</sub>, or InAlGaN.**

[0191] *Smith*, alone or in combination with *Uemoto*, discloses “the confinement layer is made of SiN, SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, Ga<sub>2</sub>O<sub>3</sub>, or InAlGaN.”

[0192] In Ground 1A, *Smith* itself discloses **passivation layer 100** being made of SiN or SiO<sub>2</sub>, disclosing that **passivation layer 100** “may be incorporated with layers of other materials, such as SiN or SiO<sub>x</sub>.” *Smith*, [0090]. Therefore, *Smith* itself discloses the feature of claim 7.

[0193] In Ground 1C, *Uemoto* discloses **hydrogen diffusion film 17** being made of “made of silicon nitride (SiN).” *Uemoto*, [0063]. Therefore, *Smith* in combination with *Uemoto* also discloses the feature of claim 7.

[0194] Therefore, both *Smith* itself (in Ground 1A) and the *Smith* in combination with *Uemoto* (in Ground 1C) each discloses claim 9’s limitation.

**I. Independent Claim 10**

**1. [10p] A compensated gate MISFET transistor comprising:**

[0195] *Smith*, alone or in combination with *Kigami* or *Uemoto*, discloses a compensated gate MISFET transistor.

[0196] In Ground 1A, *Smith* discloses GaN transistors, which the ’294 patent identifies as “MISFET.” ’294 patent, Abstract (“a MISFET, such as a GaN transistor”). *Smith* also discloses transistors including MIS (i.e., metal-insulator-

semiconductor) layers. *Smith*, [0090] (“in the embodiments illustrated in FIG. 3B, a MISHEMT may be provided”). And, as discussed above, *Smith* discloses transistors with “compensated” or “semi-insulating” cap layers. *Smith*’s Figure 3B is reproduced below but substituting cap layer 24 for cap layer 34 (as disclosed in *Smith*’s paragraph [0095]). The annotated Figure 3B illustrates *Smith*’s disclosure of the “compensated gate MISFET transistor” of [10p].

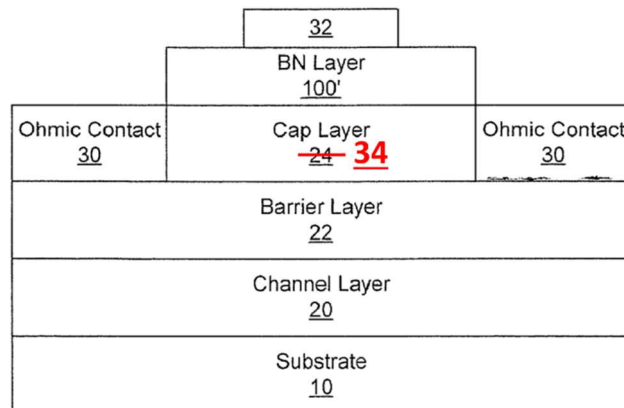


Figure 3B

*Smith*, Fig. 3B (modified to substitute “cap layer 24” for “cap layer 34”)

[0197] In Ground 1B, The *Smith* and *Kigami* combination discloses “compensated gate MISFET transistor.” *Kigami* discloses forming the transistor as a “semiconductor device having the MIS-type gate.” *Kigami*, [0014]. Therefore the *Smith* and *Kigami* combination would also disclose the preamble [10p].

[0198] In Ground 1C, the *Smith* and *Uemoto* combination also discloses “compensated gate MISFET transistor.” *Uemoto* discloses a “structure for obtaining the normally-off type FET” and describes transistors using the MIS-type structures. *Uemoto*, [0007], [0043], [0055], Fig. 7. Therefore the *Smith* and *Uemoto* combination would also disclose the preamble [10p].

**2. [10a] a III-N barrier layer beneath a gate contact,**

[0199] Element [10a] is substantially similar to elements [1d], [4d], or [7d]. The primary difference between [10a] and the other elements is that in [10a] the barrier layer is “beneath a gate contact,” instead of being “above the buffer layer” or having no relative position.

[0200] As shown below in modified Figure 3B, modified to substitute cap layer 24 for cap layer 34 as disclosed in *Smith* [0095], *Smith* discloses the **barrier layer 22** being beneath the **gate contact 32**. *Smith* thus discloses [10a].

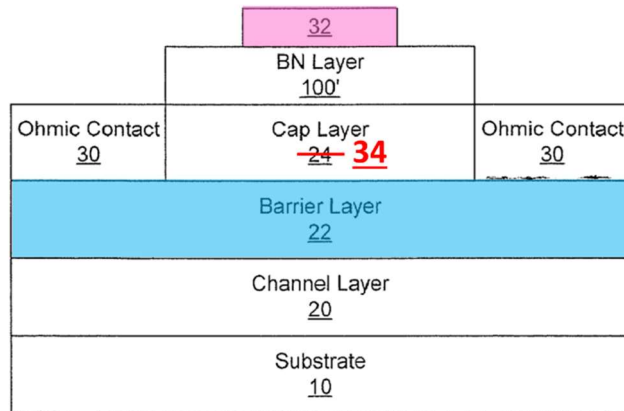


Figure 3B

*Smith*, Fig. 3B (annotated and modified)

**3. [10b] a drain contact, a source contact, and**

[0201] *Smith* discloses this “a drain contact, a source contact.” *Smith* discloses that “ohmic contacts 30 are provided on the barrier layer 22” and that “the ohmic contacts 30 provide source and drain contacts.” *Smith*, [0081]. Figure 3B below highlights *Smith*’s **ohmic contacts 30** providing the source and drain.

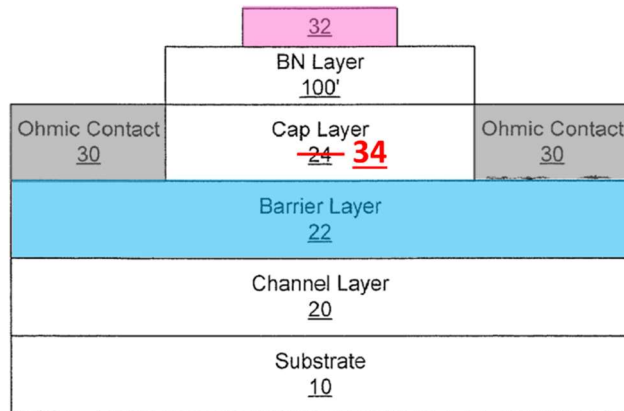


Figure 3B

*Smith*, Fig. 3B (annotated and modified)

4. **[10c] a semi-insulating III-N layer between the barrier layer and the gate contact.**

[0202] Element [10c] is substantially similar to elements [4e] and [7e]. The difference between [10c] and the other elements, is that in [10c] the semi-insulating layer is “between the barrier layer and the gate contact,” instead of being “above the barrier layer.” For example, while element [4e] recites “a semi-insulating III-N layer above the barrier layer,” element [10c] recites “a semi-insulating III-N layer between the barrier layer and the gate contact.”

[0203] As discussed above, however, *Smith* discloses a **semi-insulating cap layer 34**. And as shown below, *Smith* discloses the **semi-insulating cap layer 34** being between **barrier layer 22** and **gate contact 32**. *Smith* thus discloses [10c].

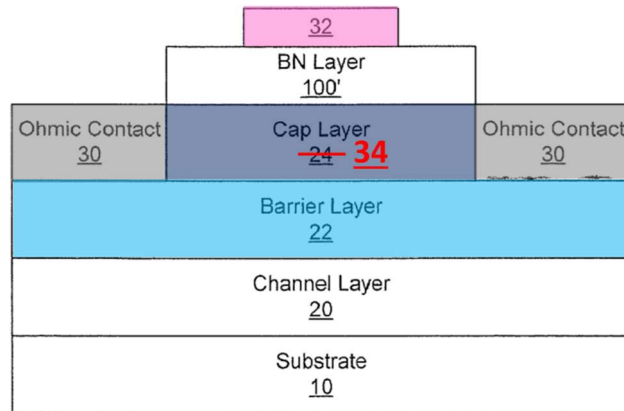


Figure 3B

*Smith*, Fig. 3B (annotated and modified)

**J. Claim 11 - The transistor of claim 10, further comprising a confinement layer above the semi-insulating III-N layer.**

[0204] The feature of claim 11 is the same as feature [7f]. As discussed above, *Smith*'s "**passivation layer 100**" discloses the confinement layer of the '294 patent and my same analysis applies here. Further, as shown below in modified Figure 3B, modified to show cap layer 34 instead of cap layer 24 (as disclosed in *Smith*, [0095]), *Smith* discloses "**passivation layer 100**" being above **semi-insulating cap layer 34**.

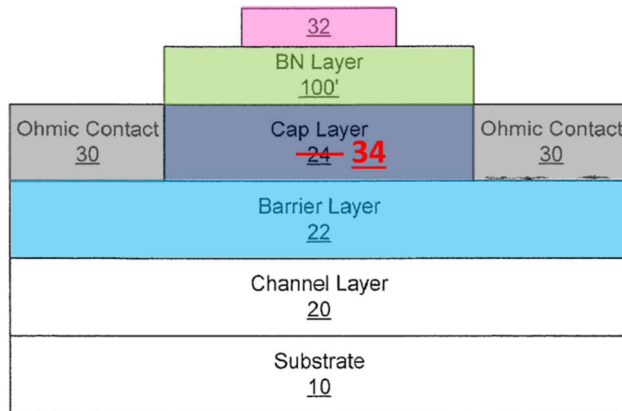


Figure 3B

Smith, Fig. 3B (annotated and modified)

**K. Claim 12 - The transistor of claim 10, further comprising a spacer layer between the semi-insulating layer and the barrier layer.**

[0205] *Smith* discloses “a spacer layer between the semi-insulating layer and the barrier layer.”

[0206] *Smith* discloses techniques for the fabrication of transistors “with barrier/spacer layer” and discloses embodiments in which **barrier layer 22** is “provided with multiple layers.” *Smith*, [0061], [0120]. In particular, *Smith* discloses that the barrier layer “may include, for example, barrier layers having combinations of GaN, AlGaIn and/or AlN layers.” *Smith*, [0120]. And *Smith* incorporates by reference *Chavarkar* (Ex. 1021), which discloses the formation of the transistor “with barrier/spacer layer” for “improved high frequency performance.” *Chavarkar*, Title, Abstract.

[0207] In my opinion, *Smith*'s disclosure of forming the barrier layer with multiple layers and "with barrier/spacer layer," discloses, or at a minimum renders obvious, "a spacer layer between the semi-insulating layer and the barrier layer." Any one of the layers in *Smith*'s multilayer barrier, such as the "combinations of GaN, AlGaN and/or AlN layers," works as the "spacer." Any layer in the *Smith*'s barrier combination would be "a low Mg region," the characteristic the '294 patent associates with the "spacer." '294 patent, 4:67 ("spacer layer 49, which is a low Mg region"). Therefore, despite the differences in nomenclature, *Smith* discloses, "a spacer layer between the semi-insulating layer and the barrier layer" by disclosing the barrier may be a multilayer barrier with a combination of different nitride materials.

[0208] Figure 3B below, has been modified to exemplify *Smith*'s disclosure of **barrier layer 22** being formed with multiple layers. The modified figure shows that the multilayer barrier would include a *spacer layer* between the **semi-insulating layer cap layer 43** and the **barrier layer 22**.

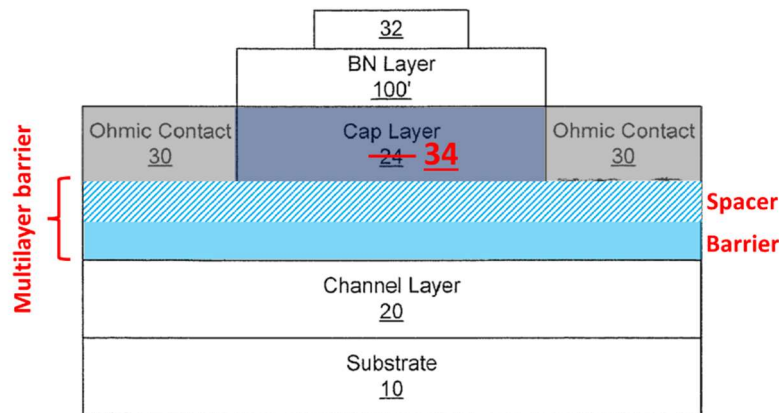


Figure 3B

*Smith*, Fig. 3B (annotated and modified)

[0209] *Smith* additionally discloses the claim 12 feature by disclosing cap layers can be formed as “a multilayer cap layer (73', 74', 75) on the barrier layer 22.” *Smith*, [0113]. *Smith* discloses embodiments in which cap layers are formed with several layers having materials of different composition and thickness. *Smith*, [0113]. *Smith* explains that the multilayers can be adjusted to control the depth or spacing of the gate, stating that the “thickness of the layers of the multilayer cap (GaN, AlN, and AlGaN) and the composition of the AlGaN can all be adjusted to obtain the improved device performance.” *Smith*, [0117].

[0210] In my opinion, by disclosing that the cap layer may be formed as a “multilayer cap,” *Smith* discloses “a spacer layer between the semi-insulating layer

and the barrier layer,” because one of the layers in the “multilayer cap (GaN, AlN, and AlGaN)” works as the “spacer.” Any layer in the multilayer cap, and particularly lower layers (out of *Smith*’s doped region 40), would be “a low Mg region,” the characteristic the 294 patent associates with the “spacer.” ‘294 patent, 4:67. Therefore, despite the differences in nomenclature, *Smith* discloses , “a spacer layer between the semi-insulating layer and the barrier layer” by disclosing the cap layer may be a multilayer barrier with a combination of different nitride materials.

[0211] Figure 3B, has been modified to exemplify *Smith*’s disclosure of the **semi-insulating cap layer** being formed with multiple layers. The modified figure shows that the multilayer cap layer would include a *spacer layer* between the **semi-insulating layer cap layer 43** and the **barrier layer 22**.

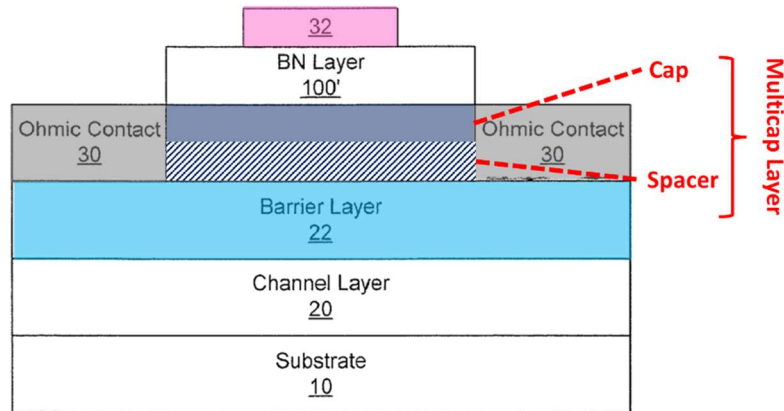


Figure 3B

*Smith*, Fig. 3B (annotated and modified)

### XIII. GROUND 2: THE CHALLENGED CLAIMS ARE UNPATENTABLE AS OBVIOUS BASED ON UEMOTO AND SMITH

[0212] Claims 1-12 of the '294 patent are also unpatentable because a person of ordinary skill would have found *Uemoto* in view of *Smith* render all the challenged claims obvious.

#### A. Overview of the Unpatentability Ground Based on *Uemoto* Combined with *Smith*

[0213] *Uemoto* discloses its transistors are formed by stacking the “conventional” layers the '294 patent admits as prior art (e.g., **transition**, **buffer**, **barrier**) on a **substrate** and using electrodes to form the transistor **gate**, **source**, and **drain**. *Uemoto*, [0031]-[0035].

[0214] *Uemoto* also discloses forming a “compensated GaN layer” under both parties’ construction. *Uemoto* discloses that “a third nitride semiconductor layer 15” is formed with GaN and doped with magnesium. And *Uemoto* discloses the layer 15 being a “compensated GaN layer,” under both proposed constructions, because *Uemoto* discloses that the impurities in the layer 15 are inactivated when “hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment.” *Uemoto*, [0063]. Because *Uemoto* discloses layer 15 being magnesium doped GaN and processed with a hydrogen passivation diffusion step, *Uemoto*’s layer 15 discloses a “doped GaN layer formed with a step to passivate its impurities” (Petitioner’s construction). *ITC Constructions*, p. 9. Additionally, because *Uemoto* discloses layer 15 being part of the gate transistor structure and formed by doping with magnesium and then including hydrogen to inactivate magnesium, *Uemoto*’s also discloses a “semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor).” (Patent Owner’s construction). *ITC Constructions*, p. 1.

[0215] Depending on how claims are interpreted, however, *Uemoto* may not explicitly disclose certain features of the challenged claims. For example, to the extent it is determined the claims require using multiple “transition layers,”

*Uemoto* only explicitly discloses one (buffer layer 12). *Uemoto* also does not explicitly disclose using a “semi-insulating layer” or a “spacer layer.” *Uemoto* also does not expressly disclose the specific “deep dopants” recited in certain dependent claims (e.g., “C, Fe, Mn, Cr and V”).

[0216] A person of ordinary skill in the art, however, knew about the use of a group of transition layers, the incorporation of a “semi-insulating layer” or a “spacer layer,” and the use of deep level dopants in III-nitride transistors. To a person of ordinary skill in the art it would have been obvious to include these layers and dopants to *Uemoto*’s device, either based on its knowledge or on other prior art, like *Smith*.

[0217] For example, as detailed in my analysis above, *Smith* discloses the “transition layers,” “semi-insulating layer” with deep level dopants, and “spacer layer.” And a person of ordinary skill in the art would have considered *Uemoto* and *Smith* analogous art and their teachings relevant and combinable. In my opinion, a person of ordinary skill in the art would have been motivated to modify *Uemoto* to incorporate the “transition layers,” the “semi-insulating layer” with deep level dopants, or the “spacer layer” disclosed in *Smith*.

**1. A person of ordinary skill in the art would have been motivated to incorporate *Smith*'s "transition layers" in *Uemoto***

**[0218]** In my opinion, a person of ordinary skill would have been motivated to incorporate *Smith*'s transition layers to *Uemoto* seeking to, for example, improve an appropriate crystalline structure transition in *Uemoto*'s transistor.

**[0219]** *Smith* teaches that "transition layers . . . provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device." *Smith*, [0070]. *Smith* also discloses that the transition layers can be useful for "strain balancing." And incorporating by reference *Saxler015* and *Saxler482*, *Smith* discloses how transition layers "provide means for reducing stress" and prevent cracking. *Saxler015*, [0026]. *Saxler482* also discloses how layers can be formed with tensile stress and thickness selected so that less "cracking or defect formation occurs." *Saxler482*, [0021]. A person of ordinary skill in the art would have considered these effects advantageous to *Uemoto*'s transistor, particularly because *Uemoto* describes using the same substrate and GaN layer materials as *Smith*, making *Smith*'s disclosure of crystalline structure particularly relevant to *Uemoto*. *Uemoto*, [0054]; *Smith*, [0069].

**[0220]** Indeed, *Uemoto*'s transistors already include a transition layer (buffer layer 12), and *Smith* discloses that including additional transition layers

over the buffer improves strain balancing and minimizes cracking. For example, *Smith* incorporates by reference *Saxler015* (Ex. 1013). And *Saxler015* discloses that including additional transition layers over a buffer—such as a “device match,” “graded,” and “mismatch” layers—improve the transistor robustness because “the likelihood of the total strain of the structure exceeding a threshold, which cracking occurs may be reduced.” *Saxler015*, [0042], Fig. 2 (describing additional transition layers over the buffer 14). *Saxler015* also discloses that the inclusion of multiple transition layers permit adjusting lattices “so as to provide the desired strained in-plane lattice constant.” *Saxler015*, [0038]. In my opinion, a person of ordinary skill in the art would find that *Smith*’s touted reduction in likelihood of cracking and the ability to better match layer would have been advantageous to *Uemoto*’s transistor. For example, *Uemoto*, like *Smith*, was also concerned with improvements in the transistor fabrication and robustness (*Uemoto*, [0079]), and *Smith*’s suggested incorporation of transition layers would have been recognized as an improvement to *Uemoto*.

[0221] Moreover, in my opinion a person of ordinary skill in the art would have incorporated the transition layers of *Smith* to *Uemoto* with a reasonable expectation of success. The ’294 patent does not explain how to form the transition layers over a silicon substrate, acknowledging instead that they were

“conventional.” ‘294 patent, 1:55-6. That is because growing multiple transition layers was and well understood in the art by 2009. Accordingly, providing multiple transition layers in *Uemoto*’s device would have required only conventional techniques in their ordinary and expected manner. A person of ordinary skill in the art would have reasonably expected to succeed in using *Smith*’s multiple transition layers when fabricating *Uemoto*’s device.

**2. A person of ordinary skill in the art would have been motivated to make *Uemoto*’s layer 15 semi-insulating by including deep level dopants as disclosed in *Smith***

[0222] In my opinion, a person of ordinary skill would have been motivated to make *Uemoto*’s semiconductor nitride layer 15 semi-insulating using the doping (or co-doping) with deep level dopants disclosed in *Smith*. A person of ordinary skill would have modified *Uemoto* based on *Smith* doping seeking to, for example, reduce leakage current.

[0223] *Smith* discloses that doping (or co-doping) of cap layers with deep level dopants improve transistor characteristics. For example, *Smith* discloses that deep level dopants can “screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents.” *Smith*, [0089]. *Smith* also discloses that “co-doping [of] Group III-nitride materials” improve transistor

stability, reduce leakage current, and provide predictable semi-insulating characteristics. *Smith*, [0085], [0089]. For example, in describing methods to form cap layers, *Smith* incorporates *Saxler874* (Ex. 1016) by reference. *Smith*, [0085]. *Saxler874* explains that the “co-doping of a Group III nitride layer . . . provide a predictable characteristic of a semi-insulating Group III nitride layer.” *Saxler874*, [0018], [0027] (“the resulting layer may be more readily reproducible and the variations between processing runs may be reduced”).

[0224] In my opinion, a person of ordinary skill in the art would have acknowledged that *Smith*’s process doping techniques to form a stable semi-insulating layer would be advantageous to *Uemoto*. *Uemoto* also aims to reduce leakage current and improve the device’s fabrication. *Uemoto*, [0061], [0079]. A person of ordinary skill in the art would have identified that the leakage and fabrication improvements *Smith* discloses with its semi-insulating layers would be beneficial and applicable to *Uemoto*. In my opinion, a person of ordinary skill in the art would have identified *Uemoto*’s transistor as a base device that would be improved with *Smith*’s teachings. And a person of ordinary skill in the art would have recognized that *Smith*’s doping methods could be applied in *Uemoto*, because both references disclose the same materials and similar structure.

[0225] Further, in my opinion a person of ordinary skill in the art would have implemented *Smith*'s suggested co-doping or doping with deep level dopants in *Uemoto*'s transistor with a reasonable expectation of success. By the earliest '294 priority date, incorporation of deep level dopants in GaN layers was a well-known technique. And *Smith* (incorporating *Saxler874*) specifies the techniques for the fabrication of the co-doped layer with deep level impurities. *Smith*, [0085], [0089]; *Saxler874*, [0018]-[0019], Fig. 3. A person of ordinary skill in the art would have had a reasonable expectation of success in modifying *Uemoto* with *Smith*'s teachings based on the person of ordinary skill in the art's general knowledge and *Smith*'s disclosure.

[0226] Moreover, to a person of ordinary skill in the art, incorporating *Smith*'s deep level doping in *Uemoto*'s transistor would also have been a simple substitution of one known element for another. In particular, the modification would be a simple substitution of doping elements or techniques. *Uemoto* already discloses doping the third nitride layer with magnesium. *Uemoto*, [0033]. A person of ordinary skill in the art would have found it obvious to substitute the magnesium doping with deep level dopants for doping (or co-doping) as disclosed in *Smith*. As evidenced by *Saxler874* and *Smith*, the function and effect of co-doping and doping with deep-level dopants were known in the art. *Smith*, [0085];

*Saxler874*, [0026]. A person of ordinary skill in the art would have found it obvious to substitute *Uemoto*'s magnesium doping with *Smith*'s deep level dopants or doping techniques. And, in my opinion, the result of the substitution would have been predictable (e.g., altering resistivity and stability as discussed in *Saxler874*).

**3. A person of ordinary skill in the art would have been motivated to modify *Uemoto*'s barrier layer to become a multilayer barrier "with barrier/spacer," as taught by *Smith***

[0227] In my opinion, a person of ordinary skill would have been motivated to make *Uemoto*'s barrier, described as semiconductor nitride layer 14, into a multilayer barrier as disclosed in *Smith*. A person of ordinary skill would have modified *Uemoto* based on *Smith* barrier formation seeking to, for example, reduce scattering or leakage.

[0228] *Smith* discloses techniques for the fabrication of transistors "with barrier/spacer layer" and discloses embodiments in which the barrier layer is "provided with multiple layers." *Smith*, [0061], [0120]. *Smith* explains that the use of multiple barrier layers is advantageous to, for example, "reduce or prevent alloy scattering." *Smith*, [0120]. In describing methods to form barrier layers, *Smith* incorporates by reference *Chavarkar* (Ex. 1021). *Smith*, [0075]. *Chavarkar* explains that forming the transistor with multiple "barrier/spacer" layers "keeps the HEMT's gate leakage low" and "reduces the piezoelectric scattering between the

layers that can limit the 2DEG mobility.” *Chavarkar*, [0016], [0032]. A person of ordinary skill in the art would have recognized that these effects were beneficial to *Uemoto* because *Uemoto* was also concerned with reducing leakage and having a large operating current. *Uemoto*, [0040], [0061].

**[0229]** Further, in my opinion, a person of ordinary skill in the art would have implemented *Smith*’s suggested incorporation of a multilayer barrier to *Uemoto*’s transistor with a reasonable expectation of success. As the ’294 patent admits, it was “conventional” to form barrier layers in the III-nitride transistors. Turning *Uemoto*’s barrier layer into a multiple barrier would have required only required applying conventional techniques in their ordinary and expected manner. A person of ordinary skill in the art would have reasonably expected to succeed in using *Smith*’s multibarrier layer “with barrier/spacer” when fabricating *Uemoto*’s device.

**[0230]** Moreover, to a person of ordinary skill in the art, the modification of *Uemoto*’s barrier layer in view of *Smith*’s teachings would also have been a simple substitution of one known element for another. The modification would be a simple substitution of *Uemoto*’s single layer barrier to *Smith*’s multi-layer barrier. As *Smith* discloses, these two were interchangeable. *Smith*, [0120] (“the barrier layer 22 may also be provided with multiple layers”). A person of ordinary skill in

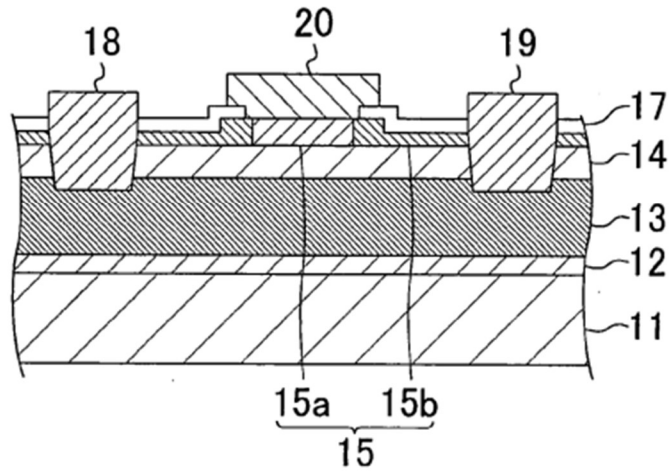
the art would have found it obvious to substitute *Uemoto*'s single layer barrier for *Smith*'s multilayer barrier.

**B. Independent Claim 1**

**1. [1p] A column III Nitride transistor comprising:**

[0231] *Uemoto* discloses “[a] column III Nitride transistor comprising” as recited in the preamble of claim 1. *Uemoto* specifies its invention relates to “nitride semiconductor transistors” and discloses transistors made with “III Nitride materials,” disclosing transistors are “not only GaN but also aluminum nitride (AlN), indium nitride (InN).” *Uemoto*, [0005], [0031]-[0032]. In its figures, *Uemoto* illustrates cross-sectional schematics of the transistors. For example, in Figure 7, *Uemoto* illustrates “a cross sectional view showing a nitride semiconductor transistor.”

FIG. 7

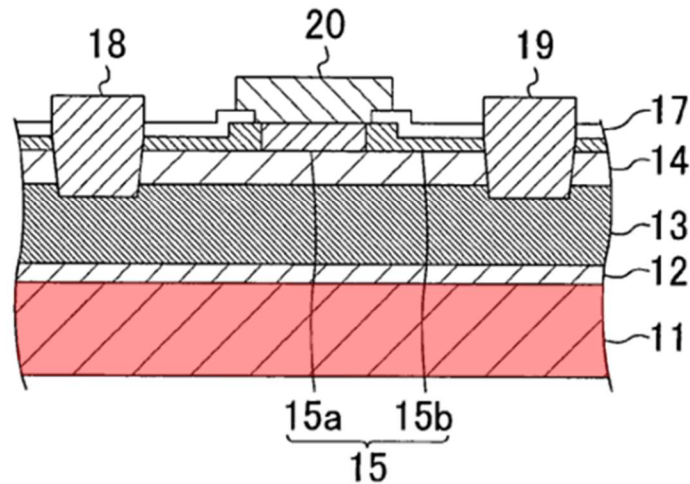
*Uemoto*, Fig. 7

## 2. [1a] a substrate,

[0232] *Uemoto* discloses “a substrate.” *Uemoto* discloses “a substrate 11 is made of silicon and its principal plane is the (111) plane.” *Uemoto*, [0031].

*Uemoto* discloses the substrate being formed with the same materials as the '294 patent. Like the '294 patent, *Uemoto* discloses the substrate being formed with silicon. *Uemoto*, [0031] (“substrate 11 is made of silicon”); '294 patent, 2:58-59 (“substrate 31 that may comprise, for example, silicon”). Annotated Figure 7 below highlights *Uemoto*'s **substrate 11**.

FIG. 7

*Uemoto*, Fig. 7 (annotated)

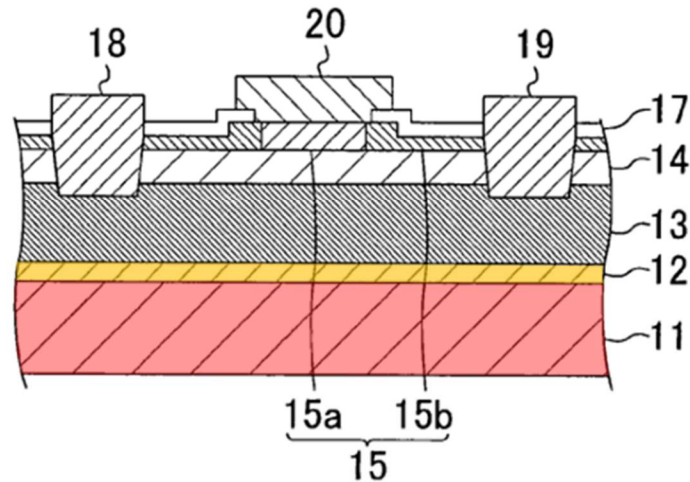
3. [1b] a set of III-N transition layers above the substrate,

[0233] *Uemoto*, alone or in combination with *Smith*, discloses, or renders obvious, “a set of III-N transition layers above the substrate.” In particular, *Uemoto* discloses or renders obvious the feature of [1b] by describing a “buffer layer 12 of AlN having a thickness of 100 nm is formed on the principal plane of the **substrate 11**.” *Uemoto*, [0031].

[0234] *Uemoto*’s “buffer layer 12” is formed with the same materials and thicknesses as the transition layers of the ’294 patent. *Compare Uemoto*, [0031] (describing the buffer layer being AlN) *with* ’294 patent, 2:60-61 (“[t]ransition layers 32 may comprise, for example, AlN”). Despite the difference in nomenclature, *Smith* discloses the “III-N transition layers” of [1b] by describing

the buffer layer. Annotated Figure 7 highlights *Smith*'s **buffer layer 12**, above the **substrate 11**.

FIG. 7



*Uemoto*, Fig. 7 (annotated)

[0235] If the claim is interpreted to require multiple transition layers, and *Uemoto* is deemed to not explicitly disclose “a set of III-N transition layers above the substrate” (e.g., disclosing only a single **buffer layer 12**), the combination of *Uemoto* and *Smith* renders [1b] obvious. As discussed above in my analysis for ground 1, *Smith* discloses a transistor with “strain balancing **transition layer(s)**.” *Smith*, [0070]. A person of ordinary skill in the art would have found it obvious to incorporate *Smith*'s transition layers in *Uemoto*'s device rendering [1b] obvious.

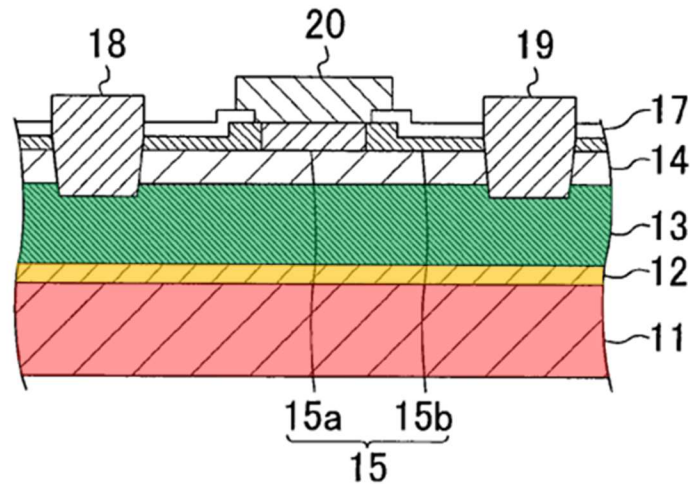
**4. [1c] a III-N buffer layer above the set of transition layers,**

**[0236]** *Uemoto* discloses “a III-N buffer layer above the set of transition layers” by disclosing “[a] first nitride semiconductor layer 13 . . . formed on the **buffer layer 12.**” *Uemoto*, [0032].

**[0237]** *Uemoto*’s layer 13 is formed with “undoped GaN having a thickness of 2  $\mu\text{m}$ .” *Uemoto*, [0032]. This is the same material and thickness the ’294 patent associates with a “buffer layer.” ’294 patent, 2:62-66 (“buffer layer 33 is preferably formed of InAlGaN with any concentration of In and Al (including 0% In and/or Al) and has a thickness between 0.5 and 3  $\mu\text{m}$ ”). Despite the difference in nomenclature, *Smith* discloses the “III-N buffer layer above the set of transition layers” of [1c] by describing the first nitride semiconductor layer 13.

**[0238]** Annotated Fig. 7 below highlights *Uemoto*’s **semiconductor layer 13** showing it above the **buffer layer 12.**

FIG. 7

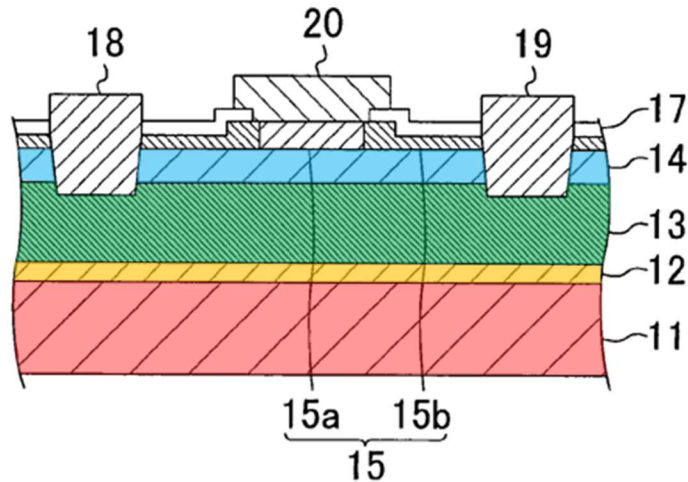
*Uemoto, Fig. 7 (annotated)*

**5. [1d] a III-N barrier layer above the buffer layer,**

[0239] *Uemoto* discloses “a III-N barrier layer above the buffer layer” by disclosing “a second nitride semiconductor layer 14” formed above the first nitride semiconductor layer 13. *Uemoto*, [0032]. *Uemoto*’s layer 14 is formed with “undoped  $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$  having a thickness of 25 nm” (*Uemoto*, [0032]), the same material and thickness the ’294 patent associates with a “barrier layer.” ’294 patent, 2:66-3:1 (“barrier layer 34 is formed of AlGa<sub>N</sub> and has a thickness between 0.005 and 0.03  $\mu\text{m}$ ”). Despite the difference in nomenclature, *Smith* discloses the “III-N barrier layer above the buffer layer” of [1d] by describing the second nitride semiconductor layer 14.

[0240] Annotated Fig. 7 below highlights *Uemoto*'s **semiconductor layer 14** showing it above the **semiconductor layer 13**.

FIG. 7



*Uemoto*, Fig. 7 (annotated)

6. [1e] a compensated GaN layer above the barrier layer, and

[0241] *Uemoto* discloses “a compensated GaN layer above the barrier layer” by disclosing a third nitride semiconductor layer 15 that includes “a high resistive region 15 b in which Mg is not activated.” *Uemoto*, [0033].

[0242] *Uemoto* discloses that a third nitride semiconductor layer 15 is formed “[o]n the second nitride **semiconductor layer 14**.” *Uemoto*, [0033]. *Uemoto* also discloses layer 15 can be made of GaN. *Uemoto*, [0054] (“third nitride semiconductor layer may be made of GaN”), Claim 10. *Uemoto*'s layer 15, therefore, discloses the “GaN layer above the barrier layer” of [1e].

[0243] *Uemoto* additionally discloses that the layer 15 is processed to include “a control region 15 a in which Mg is activated to exhibit a p-type conductivity; and a high resistive region 15 b in which Mg is not activated to offer a higher resistance.” *Uemoto*, [0033], [0063]. *Uemoto* explains that the difference in resistivity within layer 15 can be achieved using a diffusion film so that hydrogen “is supplied during a thermal treatment for selectively inactivating impurities.” *Uemoto*, [0063]. In particular, *Uemoto* discloses that in “a portion of the third nitride semiconductor layer 15 covered with the hydrogen diffusion film 17, hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment for selectively inactivating impurities.” *Uemoto*, [0063], [0049] (“Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom”). *Uemoto*, thus, teaches that the high resistive region 15 b is a “compensated GaN layer,” under both parties’ proposed constructions.

[0244] Because *Uemoto* discloses high resistive region 15 b is doped with magnesium inactivated through a hydrogen diffusion process, *Uemoto*’s high resistive region 15b discloses both a “doped GaN layer formed with a step to passivate its impurities” (Petitioner’s construction) and a “semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity,

or imperfection (for example, acceptor).” (Patent Owner’s construction). *ITC Constructions*, pp. 1, 9.

[0245] *Uemoto*’s resistive region 15b is a “doped GaN layer formed with a step to passivate its impurities” because the region 15b is doped with magnesium, and is formed with a hydrogen diffusion step to passivate its impurities.

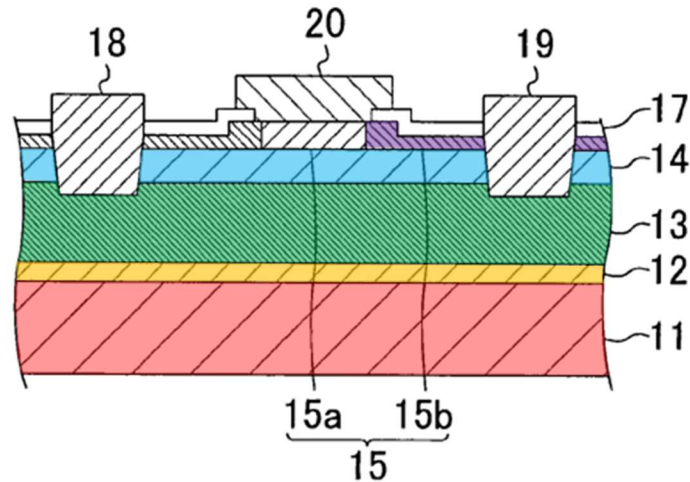
*Uemoto*, [0033], [0063]. *Uemoto*’s resistive region 15b is “a compensated GaN layer” under Petitioner’s construction.

[0246] Further, *Uemoto*’s resistive region 15b is a “semiconductor GaN gate material” because it is formed with GaN and is part of the gate material.

*Uemoto*, [0033], [0058]-[0060], Fig. 7. And *Uemoto*’s region 15b is a material “in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)” because the hydrogen incorporated with *Uemoto*’s diffusion technique is “one type of dopant, impurity, or imperfection;” *Uemoto*’s region 15b is doped with magnesium (“other type of dopant, impurity, or imperfection”); and, as disclosed in *Uemoto*, the hydrogen “partially cancels” (as the term appears to be used in Patent Owner’s construction) the electric effects of magnesium by inactivating it. *Uemoto*, [0033], [0063]. *Uemoto*, therefore, discloses the “compensated GaN layer” under Patent Owner construction.

[0247] Annotated Fig. 7 below highlights *Uemoto*'s high resistive **region 15 b** showing it above the **semiconductor layer 14**.

FIG. 7



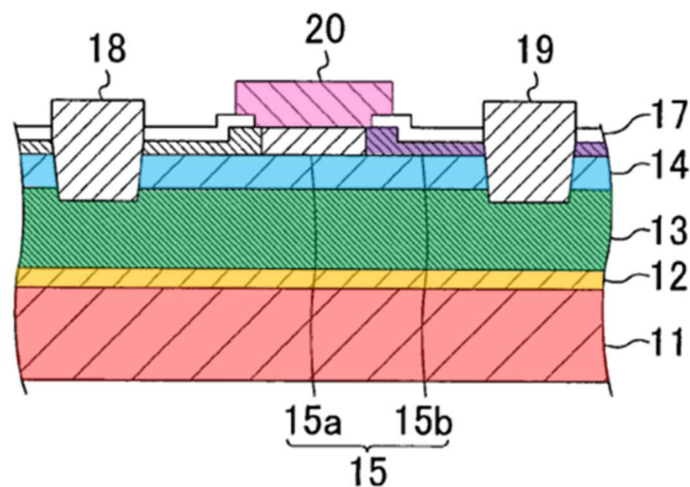
*Uemoto*, Fig. 7 (annotated)

7. [1f] a gate contact above the compensated GaN layer.

[0248] *Uemoto* discloses “a gate contact above the compensated GaN layer.” *Uemoto*'s transistor comprises a “gate electrode 20.” *Uemoto*, [0034]. Like the '294 patent, *Uemoto* discloses the gate electrode can be made of different conductors as long as they “can be brought into ohmic contact with the control region.” *Uemoto*, [0056]; '294 patent, 3:4-5 (“gate contact 37, formed of for example, Ta, Ti, TiN, W, or WSi<sub>2</sub>”). Further, *Uemoto* discloses the gate electrode 20 is above high resistive **region 15 b**. For example, *Uemoto* specifies gate electrode 20 is formed on the diffusion film. *Uemoto*, [0034] (specifying the gate

electrode is formed “[o]n the hydrogen diffusion barrier film 16”); [0062]. And as shown in *Uemoto*’s Figures, such process places the gate electrode 20 above the **region 15 b**. Annotated Figure 7 below highlights the **gate electrode 20** being above **region 15 b**.

FIG. 7

*Uemoto*, Fig. 7 (annotated)

[0249] As shown in Figure 7, **gate electrode 20** is above **region 15b**. And while the two layers only overlap in one portion, the right portion of **gate electrode 20** overlaps with the left portion of **region 15b**, in my opinion a person of ordinary skill in the art would have understood the **gate electrode 20** is above **region 15b** because **gate electrode 20** is higher and/or over **region 15b**.

[0250] Moreover, in my opinion a person of ordinary skill in the art would have found it obvious to increase the overlap between **region 15b** and **gate**

**electrode 20**. To a person of ordinary skill in the art it would have been obvious to adjust the width or proportion of the **gate electrode 20** as a mere change in size or proportion seeking to, for example, facilitate the transistor fabrication. *Uemoto* explains that gate electrode 20 should be made to “cover the opening” in the diffusion layer and to “come[] into ohmic contact with region 15a.”

*Uemoto*, [0056]. A person of ordinary skill in the art would have recognized that increasing the width or proportion of **gate electrode 20** would have facilitated alignment during the transistor fabrication so that **gate electrode 20** could be more easily placed fully covering the opening. A person of ordinary skill in the art would have recognized that such optimization increase the overlap between **gate electrode 20** and **region 14b**, making it obvious that the **gate electrode 20** is above **region 14b**.

[0251] *Uemoto*, therefore, discloses the “gate contact above the compensated GaN layer” of [1f] by disclosing **gate electrode 20** is above **region 15b**. And, even if it is considered the overlap between **gate electrode 20** and **region 15b** is not sufficient to consider **gate electrode 20** being above **region 15b**, which I do not agree with, a person of ordinary skill in the art would have found it obvious to adjust dimensions in *Uemoto*’s transistors to increase the **gate electrode 20** above and aligned with **region 15b**.

**C. Claim 2 - The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.**

[0252] *Uemoto* discloses “the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.” *Uemoto* discloses layer 15 is doped with magnesium, which a person of ordinary skill in the art recognizes is an acceptor type dopant. *Uemoto*, [0046] (“the third nitride semiconductor layer 15 of Al<sub>0.15</sub>Ga<sub>0.85</sub>N is grown with Mg doped as a p-type impurity”). *Uemoto* also discloses that in layer 15 (including specifically **region 15b**) hydrogen inactivates or passivates the magnesium, explaining that “hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment for selectively inactivating impurities.” *Uemoto*, [0063], [0049] (“Mg, introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom.”). Therefore, *Uemoto* discloses Claim 2’s limitation.

**D. Claim 3 - The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.**

[0253] *Uemoto* discloses “the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.” *Uemoto* discloses the acceptor type atom is selected from the group consisting of Mg, Zn, Be and Ca, because *Uemoto* discloses the acceptor type dopant being magnesium. *Uemoto* [0033] (“layer 15 is

. . . doped with magnesium (Mg)’’). Therefore, *Uemoto* discloses Claim 3’s limitation.

**E. Independent Claim 4**

**1. [4p] A column III Nitride transistor comprising:**

[0254] The preamble of claim 4 is the same as the preamble in claim 1. As further discussed above, *Uemoto* discloses the preamble of claim 4. My analysis for claim’s 1 preamble applies to claim 4.

**2. [4a] a substrate,**

[0255] Feature [4a] of claim 4 is the same as feature [1a] of claim 1. My analysis for [1a] applies to [4a]. *Uemoto* discloses this feature of claim 4.

**3. [4b] a set of III-N transition layers above the substrate,**

[0256] Feature [4b] of claim 4 is the same as feature [1b] of claim 1. My analysis for [1b] applies to [4b]. *Uemoto* discloses this feature of claim 4.

**4. [4c] a III-N buffer layer above the set of transition layers,**

[0257] Feature [4c] of claim 4 is the same as feature [1c] of claim 1. My analysis for [1c] applies to [4c]. *Uemoto* discloses this feature of claim 4.

**5. [4d] a III-N barrier layer, and**

[0258] Feature [4d] of claim 4 is substantially similar to feature [1d]. The primary difference between [4d] and [1d] is that [4d] does not require the barrier layer to be “above the buffer layer.” Element [1d] recites “a III-N barrier layer

above the buffer layer,” while element [4d] only recites “a III-N barrier layer.” As element [4d] is broader than [1d], my analysis of unpatentability of element [1d] applies to [4d]. *Uemoto* discloses [4d].

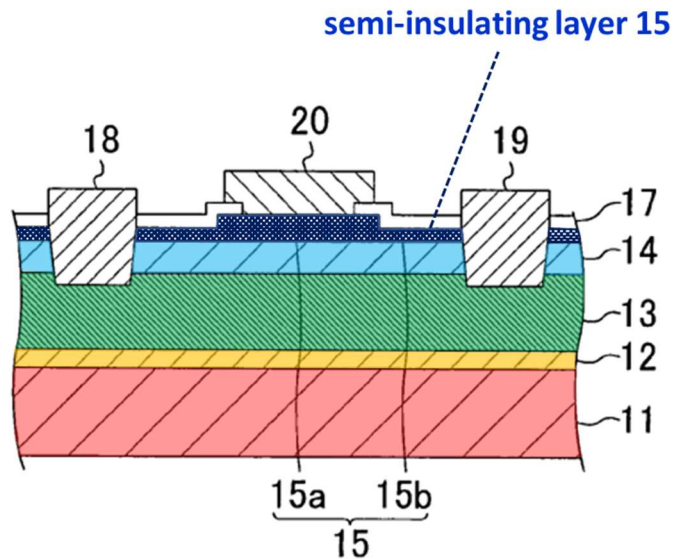
**6. [4e] a semi-insulating III-N layer above the barrier layer.**

[0259] In my opinion, *Uemoto* in view of *Smith* renders obvious element [4e]. *Uemoto* discloses a “III-N layer above the barrier layer” by disclosing a third nitride semiconductor layer 15 formed on **second nitride semiconductor layer 14** (the barrier). *Uemoto*, [0033]. And while *Uemoto* does not explicitly disclose layer 15 being “semi-insulating,” *Smith* discloses forming a semi-insulating layer, and a person of ordinary skill in the art would have been motivated to incorporate *Smith*’s formation of semi-insulating layers to *Uemoto*. As described in my analysis for Grounds 1, *Smith* discloses embodiments with a **semi-insulating cap layer 34**, above **barrier layer 22**, *Smith*, [0085] (disclosing cap layer 34 being formed as a “semi-insulating III-N layer”). My analysis above also shows that a person of ordinary skill in the art would have been motivated to apply *Smith*’s teachings forming semi-insulating layers with deep level dopants to *Uemoto*.

[0260] Annotated Figure 7 exemplifies the combination of *Uemoto* and *Smith*, showing *Uemoto* with a **semi-insulating layer 15**, as taught by *Smith*,

above the **semiconductor layer 14**. The combination of *Uemoto* and *Smith* discloses [4e].

FIG. 7



*Uemoto*, Fig. 7 (annotated and showing the incorporation of *Smith*'s semi-insulating layer)

**F. Claim 5 - The transistor of claim 4, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms.**

[0261] *Uemoto* in view of *Smith* renders obvious the semi-insulating III-N layer contains deep acceptor type dopant atoms.

[0262] As discussed in my analysis above, a person of ordinary skill in the art would have found it obvious to incorporate *Smith*'s semi-insulating layer (e.g., with deep level or co-doping techniques) and turn *Uemoto*'s layer 15 into a **semi-insulating layer 15**. *Smith* also specifies doping "with deep level dopants" and discloses the deep level doping being performed with acceptor type dopant atoms.

*Smith*, [0089] Accordingly, the combination of *Uemoto* and *Smith* renders claim 5 obvious.

**G. Claim 6 - The transistor of claim 5 where the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.**

[0263] *Uemoto* in view of *Smith* render obvious “the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V.”

[0264] As discussed in my analysis above, a person of ordinary skill in the art it would have been obvious to incorporate *Smith*’s deep level doping or co-doping techniques to form a **semi-insulating layer 15** in *Uemoto*’s device.

Additionally, *Smith* specifies “[t]he deep level dopants may be Fe, C, V, Cr, Mn, Ni, Co or other rare earth elements,” which are the same elements recited in claim 6. *Smith*, [0089]. Accordingly, the combination of *Uemoto* and *Smith* renders claim 6 obvious.

**H. Independent Claim 7**

**1. [7p] A column III Nitride transistor comprising:**

[0265] The preamble of claim 4 is the same as the preamble in claim 1. As further discussed above, *Uemoto* discloses the preamble of claim 4. My analysis for claim’s 1 preamble applies to claim 4.

**[0266]** The preamble of claim 7 is the same as the preamble in claims 1 and 4. As discussed above, *Uemoto* discloses the preamble of claim 7. My analysis for claims' 1 and 4 preamble applies to claim 7.

**2. [7a] a substrate,**

**[0267]** Feature [7a] of claim 7 is the same as feature [1a] and feature [4a]. My analysis for [1a] and [4a] applies to [7a]. *Uemoto* discloses this feature of claim 7.

**3. [7b] a set of III-N transition layers above the substrate,**

**[0268]** Feature [7b] of claim 7 is the same as features [1b] of claim 1 and [4b] of claim 7. My analyses for [1b] and [4b] apply to [7b]. *Uemoto* discloses this feature of claim 7.

**4. [7c] a III-N buffer layer above the set of transition layers,**

**[0269]** Feature [7c] of claim 7 is the same as features [1c] of claim 1 and [4c] of claim 7. My analyses for [1c] and [4c] apply to [7c]. *Uemoto* discloses this feature of claim 7.

**5. [7d] a III-N barrier layer, and**

**[0270]** Feature [7d] of claim 7 is the same as feature [4d] of claim 4. My analysis for [4d] applies to [7d]. *Uemoto* discloses this feature of claim 7.

**6. [7e] a semi-insulating III-N layer above the barrier layer, and**

[0271] Feature [7e] of claim 7 is the same as feature [4e] of claim 4. My analysis for [4e] applies to [7e]. *Uemoto* discloses this feature of claim 7.

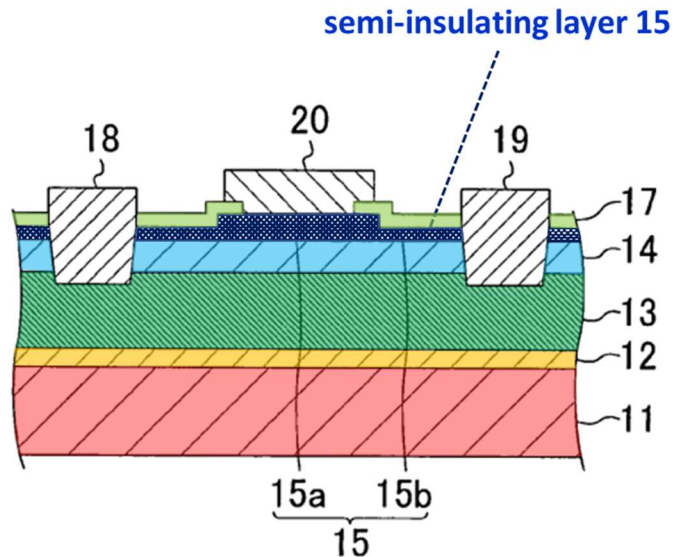
**7. [7f] a confinement layer above the semi-insulating III-N layer.**

[0272] *Uemoto* in view of *Smith* renders obvious a confinement layer above the semi-insulating III-N layer. *Uemoto* discloses forming a hydrogen diffusion film 17 on top of the third nitride semiconductor layer 15. *Uemoto*, [0063]. *Uemoto* discloses hydrogen diffusion film 17 is “made of silicon nitride.” *Uemoto*, [0063]. Silicon nitride is the same material the ’294 patent associates with the “confinement layer.” ’294 patent, 2:63-65 (describing the “confinement layer can be composed of AlGaN, SiN, SiO<sub>2</sub>, or other insulating material.”). Despite the difference in nomenclature, *Uemoto* discloses the “confinement layer” of [7f] by describing the “hydrogen diffusion film 17.”

[0273] Further, because a person of ordinary skill in the art would have found it obvious to make *Uemoto*’s layer 15 semi-insulating making a **semi-insulating layer 15** (as explained in my analysis above), the combination of *Uemoto* and *Smith* discloses the hydrogen diffusion film 17 being above the **semi-insulating layer 15**.

[0274] Annotated Figure 7, highlights *Uemoto*'s **hydrogen diffusion film**, above the **semi-insulating layer 15**. The combination of *Uemoto* and *Smith* discloses [7f].

FIG. 7



*Uemoto*, Fig. 7 (annotated and showing the incorporation of the *Smith*'s semi-insulating layer)

- I. Claim 8 - The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.**

[0275] Claim 8 is substantially similar to the limitation of claim 6. While claim 6 only requires “the deep acceptor type atoms are selected from the group consisting of C, Fe, Mn, Cr and V,” claim 6 depends from claim 5, which requires “the semi-insulating III-N layer contains deep acceptor type dopant atoms.”

Claims 8 and 6, thus, have substantially similar scope. My unpatentability analysis

for claim 6 applies to claim 8. The *Uemoto* and *Smith* combination render claim 8 obvious.

**J. Claim 9 - The transistor of claim 7, wherein the confinement layer is made of SiN, SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, Ga<sub>2</sub>O<sub>3</sub>, or InAlGaN.**

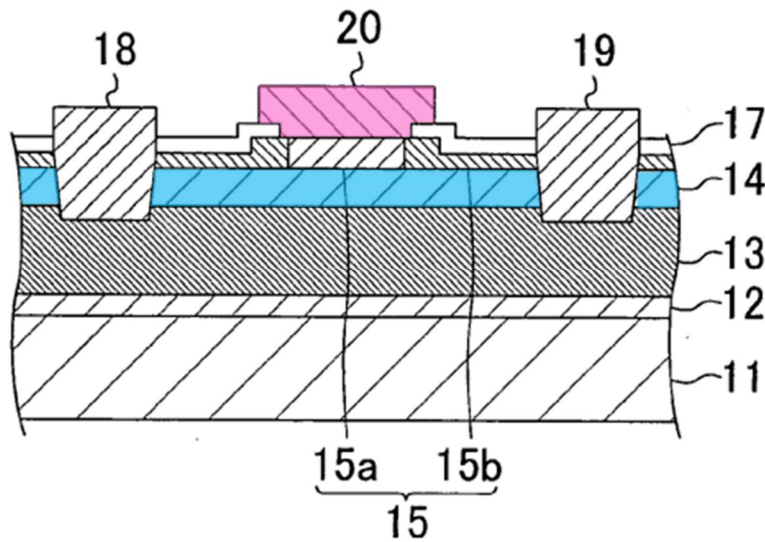
[0276] *Uemoto* discloses “the confinement layer is made of SiN, SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, Ga<sub>2</sub>O<sub>3</sub>, or InAlGaN.” For example, *Uemoto* specifies “the hydrogen diffusion film 17 is . . . made of silicon nitride (SiN).” *Uemoto*, [0063]. Silicon nitride is one of the materials recited in claim 9 for the confinement layer. Therefore, *Uemoto* discloses Claim 9’s limitation.

**K. Independent Claim 10**

**1. [10p] A compensated gate MISFET transistor comprising:**

[0277] *Uemoto* discloses “A compensated gate MISFET transistor comprising.” *Uemoto* discloses different embodiments of GaN transistors, which the ’294 patent identifies as “MISFET.” ’294 patent, Abstract (“a MISFET, such as a GaN transistor”). *Uemoto* also discloses transistors including MIS (i.e., metal-insulator-semiconductor) layers by disclosing, for example, a metal gate electrode, over an insulating diffusion film, over the third nitride semiconductor. *Uemoto*, [0034], [0063]. And, as described in my analysis above, *Uemoto* discloses transistors with “compensated” gates. *Uemoto*’s Figure 7 illustrates *Smith*’s disclosure of the “compensated gate MISFET transistor” of [10p].



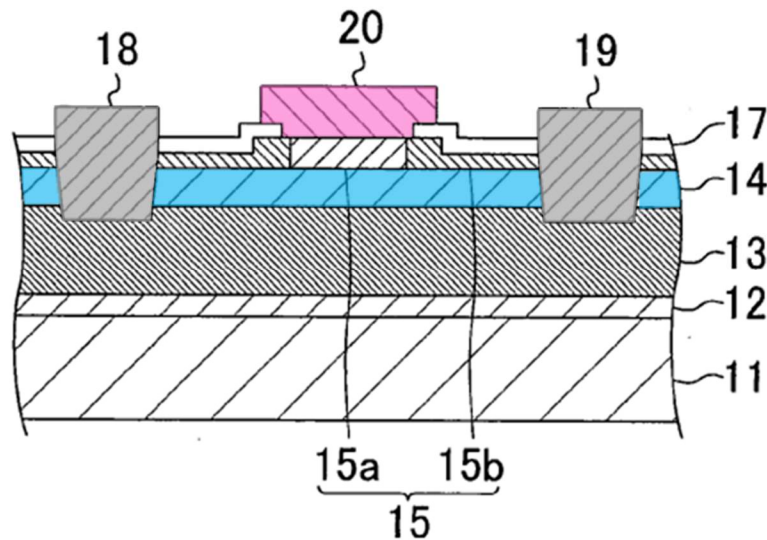


*Uemoto*, Fig. 7 (annotated)

3. [10b] a drain contact, a source contact

[0280] *Uemoto* discloses a drain contact, a source contact. *Uemoto* discloses that “a source electrode 18 and a drain electrode 19.” *Uemoto*, [0035]. *Uemoto* also discloses that the “source electrode 18 and the drain electrode 19 are each made of titanium (Ti) and aluminum (Al).” *Uemoto*, [0035].

[0281] Annotated Figure 7 below highlights *Uemoto*’s **source electrode 18** and **drain electrode 19**.



*Uemoto*, Fig. 7 (annotated)

4. **[10c] a semi-insulating III-N layer between the barrier layer and the gate contact.**

[0282] Element [10c] of claim 10 is substantially similar to elements [4e] and [7e] of claims 4 and 7. The difference between [10c] and the other elements is that in claim 10 the semi-insulating layer is “between the barrier layer and the gate contact,” instead of being “above the barrier layer.” For example, while [4d] recites “a semi-insulating III-N layer above the barrier layer,” [10c] recites “a semi-insulating III-N layer between the barrier layer and the gate contact.”

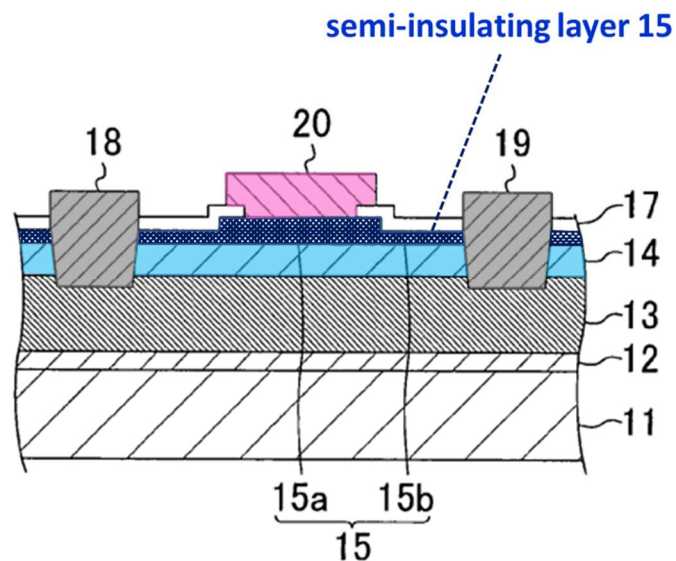
[0283] *Uemoto*, however, also discloses layer 15 being between **second nitride semiconductor layer 14** and **gate contact 22**. *Uemoto*, [0033]-[0034].

And because a person of ordinary skill in the art would have found it obvious to

make *Uemoto*'s layer 15 semi-insulating, making a **semi-insulating layer 15**, the combination of *Uemoto* and *Smith* disclose element [10c].

[0284] Annotated Figure 7, highlights **semi-insulating layer 15**, between **second nitride semiconductor layer 14** and **gate contact 22**.

FIG. 7



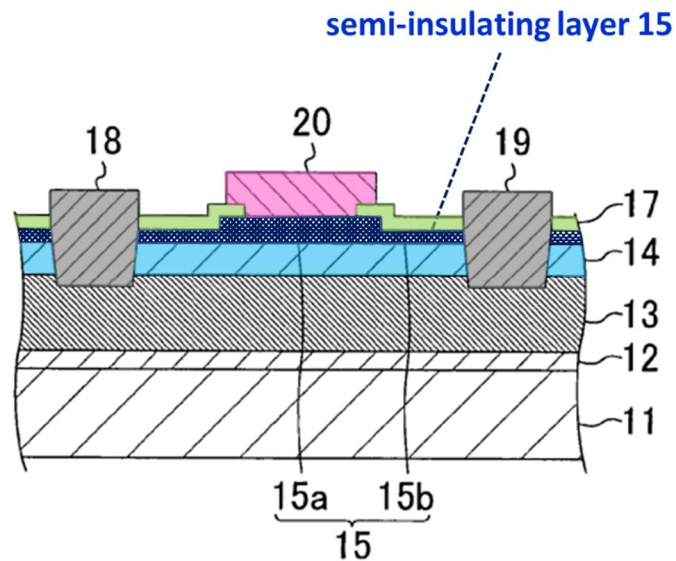
*Uemoto*, Fig. 7 (annotated and showing the incorporation of the *Smith*'s semi-insulating layer)

**L. Claim 11 - The transistor of claim 10, further comprising a confinement layer above the semi-insulating III-N layer.**

[0285] The feature of claim 11 is the same as feature [7f] of claim 7.

*Uemoto* discloses this feature of claim 11 for the same reasons as in my analysis above. For example, annotated Figure 7, highlights **hydrogen diffusion film 17** above the **semi-insulating layer 15**.

FIG. 7



*Uemoto*, Fig. 7 (annotated and showing incorporation of *Smith*'s semi-insulating layer)

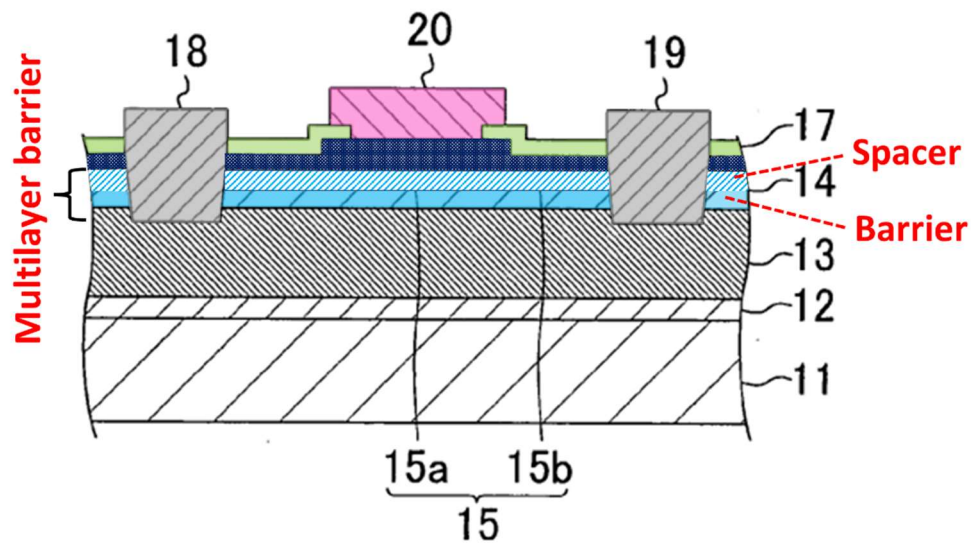
**M. Claim 12 - The transistor of claim 10, further comprising a spacer layer between the semi-insulating layer and the barrier layer.**

[0286] *Uemoto* in view of *Smith* render claim 12 obvious. Although *Uemoto* does not explicitly disclose the claimed "spacer layer," *Smith* discloses a "spacer layer" in its transistor (as shown in my analysis above). Specifically, *Smith* discloses a spacer layer by describing fabrication of transistors "with barrier/spacer layer" and discloses embodiments in which the barrier layer is "provided with multiple layers." *Smith*, [0075], [0120]. *Smith*'s disclosure of the "barrier/spacer" and the multilayer barrier disclose "a spacer layer."

[0287] As discussed in my analysis above, a person of ordinary skill in the art would have been motivated to modify *Uemoto*'s layer 14 to become a

multilayer barrier, including a “barrier/spacer,” as taught by *Smith*. A person of ordinary skill in the art would have been motivated to perform such modification seeking to improve *Uemoto*’s device performance by, for example, “reduc[ing] or prevent[ing] alloy scattering” as disclosed in *Smith*. *Smith*, [0120].

[0288] Figure 7 below has been modified to exemplify the modification of *Uemoto*’s layer 14 into a multilayer “with barrier/spacer” (as disclosed in *Smith*), showing the combination discloses the feature of claim 12.



*Uemoto*, Fig. 7 (annotated and showing incorporation of *Smith*’s semi-insulating layer and multilayer barrier)

**XIV. CONCLUSION**

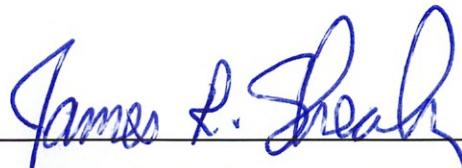
[0289] For the reasons set forth above, in my opinion, a person of ordinary skill in the art would have found claims 1-12 of the '294 patent obvious.

[0290] In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

[0291] I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 11, 2023

By: / /

  
James Richard Shealy, Ph.D.

# APPENDIX A

James R. Shealy  
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### Biography

B.S. – 1978 (North Carolina State); M.S. – 1980 (Rensselaer Polytechnic); Ph.D. – 1983 (Cornell University)

In 1978, Shealy joined the technical staff of General Electric's Corporate Research & Development Center under an Edison Fellowship, where he developed GaAs epitaxial materials for high voltage electronics, and composite dielectrics for device fabrication by MOCVD. From this work, Shealy received two patents based on GaAs vertical field effect transistors. In 1980, Shealy transferred to General Electric's Advanced Electronics Laboratory where he developed the materials and a process for the fabrication of AlGaAs Light Emitting Diodes (LEDs). Shealy then developed an MOCVD reactor and process for the fabrication of AlGaAs quantum well laser diodes which resulted in the highest power, lowest threshold devices realized at that time. A novel and patented gas purification technique was developed and applied to the MOCVD process. Con-currently with the General Electric employment, Shealy worked at Cornell, and in 1984, Shealy's group at Cornell developed the first single quantum well red laser by MOCVD (emitting over 1 watt of power at 650 nm). In 1985, Shealy was designated a Principle Staff Scientist in General Electric in recognition of his research contributions.

After a decade with General Electric, Shealy joined the Cornell faculty in 1987. He continued the MOCVD related materials research which included the preparation of epitaxial structures for LEDs, laser diodes and high frequency transistors, all using GaAs or InP based materials. Also during this time, he developed a direct write process for laser stimulated epitaxial growth of quantum dots. In 1994, Shealy began research on GaN and related materials for both LEDs and high power transistors. This work resulted in a new nucleation technique for GaN materials on substrates including sapphire, SiC and Si. Shealy's group then produced the first operational GaN microwave transistor on a Si substrate. In 1997, Shealy became the Director of Cornell's Optoelectronics Technology Center, a joint research program with UCSB focusing on compound semiconductor optoelectronic devices. With a decade of funding (from the Office of Naval Research and DARPA), which includes a MURI program which Shealy was PI, several bench marks on GaN transistor performance were achieved, and several patents were issued on key aspects of the technology. In 1999, Shealy's group at Cornell realized the first operational GaN microwave transistors on Silicon substrates, a technology that is currently entering production in dozens of companies worldwide. In parallel, work progressed on realizing defect free GaN materials on micro-machined Si (also patented) which led to the development of operational pyramidal pn junction diodes in GaN. These structures are under investigation for realizing high efficiency surface emitting UV LEDs.

In 1998, Shealy was promoted to Full Professor at Cornell and he is a member of the graduate faculty of Electrical and Computer Engineering and Materials Science. He has received multiple awards for excellence in under-graduate teaching and has developed new courses in semiconductor materials and nanofabrication. While at Cornell, he has also consulted for dozens of US companies (including GE, GM, Motorola, Raytheon, NGC, Cree, RFMD, Honeywell, Welch Allyn) on the subject of compound semiconductor materials and devices. Shealy has published in excess of 250 Journal articles and is the inventor of over 15 patents, roughly half of which, involve GaN-based materials and devices. Shealy's work also includes the development of new dielectric passivation materials for GaN transistors which has resulted in unprecedented power performance for submicron-gated GaN transistors. This level of performance still represents the state-of-the-art in the present day. Shealy's publications have received over 10,000 citations by colleagues around the world working in semiconductor electronics.

In 2002, Shealy was co-founder and technical advisor to RF Nitro Communications which developed high performance GaN-based electronics. RF Nitro became the Charlotte division of RF Micro-Devices, a US company which merged into Qorvo in 2015. In 2009, Shealy co-founded two other companies, one involved in the manufacture of GaAs-based MMICs and the other taking advantage of new intellectual property in pursuit of high power GaN electronics. In 2015, Shealy co-founded Akoustis Technologies (publicly traded on the NASDAQ) which has developed next generation Bulk Acoustic Wave (BAW) filters using AlN single crystal materials for use in the 5G mobile communications cellular market. Akoustis is currently manufacturing these devices in their MEMs fabrication facility in upstate New York. In 2019, Shealy co-founded Odyssey Semiconductor which is developing vertical GaN field effect transistors for high voltage, power switching applications.

#### **EXPERT WITNESS EXPERIENCE:**

Since 2007, Shealy has engaged in expert witness related consulting in technical field of Gallium Nitride electronics and optoelectronics. A list of engagements follow. Note that the parties name appears in **boldface** for the side which Shealy represented.

- ITC in 2007-2009, Investigation No. 337-TA-640,"Certain LEDs, Laser Diodes and Products Containing Same," **Rothschild** vs. Sony, Toshiba, Sharp, etc. Albert Jacobs LLP.,US Patent 5,252,499.
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- US District Court, Central District of California, Western Div. in 2017-2018, U.S. Patent No. 8,344,417, U.S. Patent No. 8,592,862, U.S. Patent No. 8,928,034, U.S. Patent No. 8,937,335, MACOM Technology vs. **Infineon**, Baker Botts, LLP.
- US District Court in 2019-present, U.S. Patent No. 6,465,961, **CAO Lighting** vs. various lighting companies , Barnes & Thornburg, LLP.
- US District Court, District of Delaware in 2023, U.S. Patent No. 6,465,961, **CAO Lighting** vs. General Electric, OSRAM and LEDVANCE LLC., Barnes & Thornburg, LLP.

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