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(54) Title of Invention
Semiconductor Device and Manufacturing Method Thereof

(57) Abstract

Problem

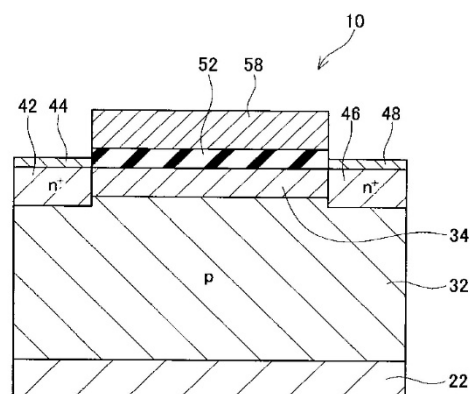
To lower the threshold voltage of an MIS-type gate structure in a semiconductor device that uses gallium nitride (GaN).

Solution

A semiconductor device 10 comprises: a semiconductor layer 32 of gallium nitride (GaN) that contains magnesium; and a gate electrode 58 that opposes that semiconductor layer 32 across a gate-insulating film 52. It is characterized in that a local region 34, in which hydrogen atoms are locally distributed unevenly, is formed in a region of the semiconductor layer 32 that the gate electrode 58 opposes. In the local region 34, the magnesium is inactivated.

Selected Figure

FIG. 1



CLAIMS

1. A semiconductor device comprising:

a III-V group compound semiconductor, which contains a p-type impurity; and
a gate electrode, which opposes the III-V group compound semiconductor across an insulating film;

wherein hydrogen atoms are unevenly distributed in a local region of the III-V group compound semiconductor that opposes the gate electrode across the insulating film.

2. The semiconductor device according to claim 1, wherein the concentration of the p-type impurity of the III-V group compound semiconductor is $1 \times 10^{17} \text{ cm}^{-3}$ or more.

3. The semiconductor device comprising:

a first-type III-V group compound semiconductor that contains a p-type impurity; and
a second-type III-V group compound semiconductor that is in contact with the first-type III-V group compound semiconductor and has a band gap that is wider than the band gap of the first-type III-V group compound semiconductor;

wherein hydrogen atoms are unevenly distributed in a region in the vicinity of the surface of the first-type III-V group compound semiconductor that is in contact with the second-type III-V group compound semiconductor.

4. The semiconductor device according to any one of claims 1–3, wherein the concentration of the hydrogen atoms in the uneven-distribution region of the hydrogen atoms is greater than the concentration of the p-type impurity.

5. The semiconductor device according to any one of claims 1–4, wherein the p-type impurity is magnesium.

6. The semiconductor device according to any one of claims 1–5, wherein the III-V group compound semiconductor is $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{N}$ (where $0 \leq x \leq 1$, $0 \leq y \leq 1$, and $0 \leq 1 - x - y \leq 1$).

7. A semiconductor-device manufacturing method, comprising:

a process of forming an insulating film on the front surface of a III-V group compound semiconductor that contains a p-type impurity;
a process of forming a gate electrode on the front surface of the insulating film; and
a process of heat treating the III-V group compound semiconductor in a gas atmosphere that contains hydrogen atoms.

8. A semiconductor-device manufacturing method comprising:

a process of forming, on the front surface of a first-type III-V group compound semiconductor that contains a p-type impurity, a second-type III-V group compound semiconductor, which has a band gap that is greater than the band gap of the first-type III-V group compound semiconductor; and

a process of heat treating the first-type III-V group compound semiconductor and the second-type III-V group compound semiconductor in a gas atmosphere that contains hydrogen atoms.

9. The manufacturing method according to claim 7 or 8, wherein the heat-treatment process is performed within a temperature range of 400°C–1,000°C.

10. The manufacturing method according to any one of claims 7–9, wherein the heat-treatment process is performed after other heat-treatment processes needed to manufacture the semiconductor device have ended.

DETAILED DESCRIPTION OF THE INVENTION

FIELD OF THE INVENTION

[0001]

The present invention relates to a semiconductor device that uses a III-V group compound semiconductor, and to a manufacturing method thereof. In particular it relates to a semiconductor device having a region in which, within a III-V group compound semiconductor that contains a p-type impurity, the concentration of an "activated p-type impurity" is locally adjusted to be low, and to a manufacturing method thereof.

BACKGROUND ART

[0002]

The development of semiconductor devices that use III-V group compound semiconductors is actively being pursued. Within that, the development of semiconductor devices that use III-V group compound semiconductors—the general formula being expressed by $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{N}$ (where $0 \leq x \leq 1$, $0 \leq y \leq 1$, and $0 \leq 1 - x - y \leq 1$), such as gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN), etc.—is actively being pursued. Because III-V group compound semiconductors have high breakdown-field strength and high saturation electron mobility, their use in switching semiconductor devices is anticipated.

[0003]

III-V group compound semiconductors have properties that differ from those of other semiconductor materials.

Non-Patent Document 1 reports that, when added to gallium nitride, the diffusion rate of magnesium, which behaves as a p-type impurity, is extremely high.

Non-Patent Document 2 reports on the behavior of hydrogen atoms contained in a III-V group compound semiconductor. Non-Patent Document 2 reports that hydrogen atoms contained in a III-V group compound semiconductor form a composite with a p-type impurity that exists in the vicinity, and thereby deactivates the p-type impurity.

Non-Patent Document 1

C. J. Pan, G. C. Chi: "Solid-State Electronics" (1999) 43, p. 621–623.

Non-Patent Document 2

S. J. Pearton, C. R. Abernathy, R. G. Wilson, J. M. Zavada, C. Y. Song, M. G. Weinstein, M. Stavola, J. Han, R. J. Shul: "Nuclear Instruments and Methods in Physics Research" (1999) 147, p. 171–174.

DISCLOSURE OF THE INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

[0004]

In one technique of forming a switching semiconductor device using a semiconductor, a technique is known in which an opposing gate electrode is formed, through an insulating film, on a semiconductor that contains a p-type impurity. The resistance of the semiconductor in the region opposing the gate electrode can be increased/decreased by adjusting the voltage impressed on the gate electrode.

In this situation, there is a demand to lower the concentration of the p-type impurity contained in the semiconductor. By lowering the concentration of the p-type impurity, the region opposing the gate electrode becomes easy to invert, and thereby the gate voltage required to turn the switching semiconductor device ON and OFF can be made small. The gate voltage when the switching semiconductor device is turned ON is called the threshold voltage. To lower the threshold voltage, it is advantageous to lower the concentration of the p-type impurity.

Nonetheless, on the other hand, there is also demand to raise the concentration of the p-type impurity. That is because, when the concentration of the p-type impurity is lowered, the withstand voltage of the switching semiconductor device decreases.

In a switching semiconductor device that uses a III-V group compound semiconductor that contains a p-type impurity, there is a tradeoff relationship: it is advantageous to lower the concentration of the p-type impurity in order to lower the threshold voltage, and it is

advantageous to raise the concentration of the p-type impurity in order to increase the withstand voltage.

The region in which it is desired to lower the concentration of the p-type impurity in order to lower the threshold voltage is a local region that opposes the gate electrode; in contrast, the region in which it is desired to raise the concentration of the p-type impurity in order to increase the withstand voltage is the entire region of the semiconductor. Accordingly, even if the concentration of the p-type impurity is lowered locally in the region opposing the gate electrode in order to lower the threshold voltage, the withstand voltage of the switching semiconductor device can be ensured as long as the concentration of the p-type impurity in the remainder of the semiconductor is maintained high. In addition, the relationship to the threshold voltage is not the concentration of the p-type impurity itself but rather the concentration of the "activated p-type impurity." From this, within the III-V group compound semiconductor that has a p-type impurity concentration that can ensure the required withstand voltage, as long as a region is created in which the concentration of the "activated p-type impurity" is lowered locally, the above-mentioned tradeoff relationship can be broken, and therefore it becomes possible to implement a switching semiconductor device that has a combination of a low threshold voltage and a high withstand voltage.

[0005]

In another technique of forming a switching semiconductor device using a III-V group compound semiconductor, a technique is known that uses a contact interface between a III-V group compound semiconductor having a narrow band gap and a III-V group compound semiconductor having a wide band gap. This structure attempts to implement a switching semiconductor device by creating a two-dimensional, electron-gas layer at the contact interface. To implement a normally-OFF type using this structure, the concentration of the "activated p-type impurity" contained in the III-V group compound semiconductor that has a narrow band gap must be lowered in a local region that contacts the III-V group compound semiconductor having a wide band gap. The two-dimensional, electron-gas layer cannot be formed in the ON state if the concentration of the "activated p-type impurity" cannot be lowered.

That is, if a III-V group compound semiconductor can be obtained in which the concentration of the p-type impurity is lowered locally, then a switching semiconductor device having a low threshold voltage and a high withstand voltage or a switching semiconductor device that operates as normally OFF can be implemented. Nevertheless, in

actuality, it is difficult to obtain a III-V group compound semiconductor in which the concentration of a p-type impurity is lowered locally.

[0006]

In a III-V group compound semiconductor, it is difficult to form a p-type impurity diffusion region using the ion-injecting technique. That is because, even if a p-type impurity is ion injected into a III-V group compound semiconductor, the injected p-type impurity tends not to be activated. In addition, there is also the problem in which, when ion injecting into a III-V group compound semiconductor, a large quantity of crystalline defects is formed. If the ion-injecting technique can be used, then it is possible to obtain semiconductor crystals of a III-V group compound in which the concentration of the p-type impurity differs by location; however, because the ion-injecting technique cannot be used with a III-V group compound semiconductor, it is difficult to obtain semiconductor crystals in which the p-type impurity concentration differs by location.

Accordingly, next, a technique is hypothesized in which a crystal-growing technique, such as the MOCVD method, is used to grow crystals of a III-V group compound semiconductor, wherein the concentration of the p-type impurity is low, on a substrate of a III-V group compound semiconductor having a p-type impurity concentration that can ensure the required withstand voltage. Nevertheless, because p-type impurities tend to diffuse in III-V group compound semiconductors, the p-type impurity contained in the III-V group compound semiconductor of the substrate adversely is taken into the III-V group compound semiconductor, the crystals of which are grown on the substrate. The problem of using magnesium in the p-type impurity becomes marked, and the same type of problem exists even in p-type impurities other than magnesium. With the miniaturization of semiconductor devices, even with p-type impurities other than magnesium, it has become impossible to avoid the phenomenon in which the p-type impurity adversely diffuses into the region in which it is desired to keep the concentration of the p-type impurity low.

Even if a crystal-growing technique is used, a semiconductor crystal cannot be obtained in which a III-V group compound semiconductor having a high concentration of a p-type impurity to the extent that the required withstand voltage can be ensured and a III-V group compound semiconductor having a low concentration of a p-type impurity to the extent that a low threshold voltage can be achieved are in contact with each other. Alternatively, a semiconductor crystal cannot be obtained that comprises a III-V group compound semiconductor having a low concentration of a p-type impurity to the extent that normally-OFF operation can be implemented.

The present invention solves the above-mentioned problems. The present invention makes use of a finding in which the relationship to the threshold voltage or normally-OFF operation is not the concentration of the p-type impurity itself but rather the concentration of the "activated p-type impurity." In the present invention, a switching semiconductor device having a low threshold voltage and a high withstand voltage or a switching semiconductor device that operates as normally OFF is implemented by, instead of obtaining a semiconductor crystal in which a region having a high concentration of a p-type impurity and a region having a low concentration of a p-type impurity are in contact with each other, obtaining a III-V group compound semiconductor in which a p-type impurity contained in a III-V group compound semiconductor is locally inactivated.

MEANS FOR SOLVING THE PROBLEMS

[0007]

The present inventors observed the use of a phenomenon described in Non-Patent Document 2. In Non-Patent Document 2, it is reported that, when hydrogen atoms exist in a III-V group compound semiconductor that contains a p-type impurity, the hydrogen atoms form a composite with the p-type impurity that exists in the vicinity, the p-type impurity is inactivated, and the resistance of the III-V group compound semiconductor is made high, and it reports the need to remove the hydrogen atoms from the III-V group compound semiconductor. On the other hand, in the present invention, the phenomenon in which the p-type impurity is inactivated by hydrogen atoms is actively utilized. By utilizing the phenomenon in which the p-type impurity is inactivated by hydrogen atoms, a III-V group compound semiconductor is obtained in which the concentration of the "activated p-type impurity" is locally lowered. If a III-V group compound semiconductor can be obtained in which the concentration of the activated p-type impurity is lowered locally, then a switching semiconductor device having a low threshold voltage and a high withstand voltage or a switching semiconductor device that operates as normally OFF can be implemented.

[0008]

The present invention can be embodied in a semiconductor device having an MIS-type gate structure. A semiconductor device, wherein the present invention is embodied in a semiconductor device having an MIS-type gate structure, comprises: a III-V group compound semiconductor, which contains a p-type impurity; and a gate electrode, which opposes that III-V group compound semiconductor; wherein hydrogen atoms are unevenly distributed in a local region of the III-V group compound semiconductor that opposes at least the gate electrode across the insulating film.

In addition to magnesium, it is possible to use calcium, zinc, beryllium, cadmium, or the like as the p-type impurity contained in the III-V group compound semiconductor. These p-type impurities have a property in that they are adversely inactivated by forming a composite with the hydrogen atoms. The range over which the hydrogen atoms are unevenly distributed should include the region opposing the gate electrode and may extend outside the region opposing the gate electrode. However, it must not extend to a range of the majority of the III-V group compound semiconductor. The hydrogen atoms must not exist as far as the range required to ensure the withstand voltage.

The above-mentioned MIS-type gate structure switches the semiconductor device ON and OFF by forming an n-type channel in a semiconductor region that opposes the gate electrode. That is, by impressing the ON voltage on the gate electrode, an n-type inversion layer is formed in the semiconductor region that opposes the gate electrode. In the above-mentioned semiconductor device, hydrogen atoms are unevenly distributed in the semiconductor region in which the n-type inversion layer is formed. In the semiconductor region in which the n-type inversion layer is formed, the hydrogen atoms form a composite with the p-type impurity, and the p-type impurity is inactivated. Accordingly, the gate voltage needed to form the n-type inversion layer is lowered. The threshold voltage is low. The above-mentioned semiconductor device can operate with a low threshold voltage and can ensure the required withstand voltage.

[0009]

The concentration of the p-type impurity of the III-V group compound semiconductor preferably is $1 \times 10^{17} \text{ cm}^{-3}$ or more.

An MIS-type gate structure generally has a pair of n-type semiconductor regions that are separated by a p-type semiconductor region. For example, an n-type source region and an n-type drain region are spaced apart by the p-type semiconductor region. When the impurity concentration in the p-type semiconductor region is low and the OFF voltage is impressed on the gate electrode, a phenomenon, i.e., the so-called punch-through phenomenon, occurs in which a depletion layer, which extends from the p-n interface between the n-type drain region and the p-type semiconductor region to the interior of the p-type semiconductor region, reaches the n-type source electrode, and thereby the withstand voltage decreases adversely. To avoid the occurrence of the punch-through phenomenon, the length of the semiconductor region that spaces apart the source region and the drain region must be made long; however, when made long, channel resistance adversely becomes large. To avoid the occurrence of the

punch-through phenomenon while keeping the channel resistance small, it is preferable to set the concentration of the p-type impurity of the p-type semiconductor region to $1 \times 10^{17} \text{ cm}^{-3}$ or more. Incidentally, if an attempt is made to form an n-type inversion layer in a semiconductor in which the concentration of the p-type impurity is $1 \times 10^{17} \text{ cm}^{-3}$ or more, then the threshold voltage needed to be impressed on the gate electrode adversely becomes high. In particular, because the band gap of the III-V group compound semiconductor is wide, the threshold voltage required to form the n-type inversion layer tends to become large.

In the MIS-type gate structure of the present invention, by locally introducing hydrogen atoms to the semiconductor region opposing the gate electrode, the threshold voltage can be made low even if the concentration of the p-type impurity is $1 \times 10^{17} \text{ cm}^{-3}$ or more. It is possible to obtain an MIS-type gate structure that has a combination of a low threshold voltage and a high withstand voltage.

[0010]

The present invention can be embodied in a semiconductor device having a HEMT (high-electron-mobility transistor) structure. The semiconductor device in which the present invention is embodied in a HEMT comprises: a first-type III-V group compound semiconductor that contains a p-type impurity; and a second-type III-V group compound semiconductor that is in contact with the first-type III-V group compound semiconductor and has a band gap that is wider than the band gap of the first-type III-V group compound semiconductor. The semiconductor device of the present invention is characterized in that hydrogen atoms are unevenly distributed in a region in the vicinity of the surface of the first-type III-V group compound semiconductor that is in contact with the second-type III-V group compound semiconductor.

A HEMT structure is obtained by a first-type III-V group compound semiconductor having a narrow band gap and a second-type III-V group compound semiconductor having a wide band gap being in contact with each other. Because the HEMT structure is constituted by using the III-V group compound semiconductor containing a p-type impurity, a two-dimensional, electron-gas layer does not form in the state in which the gate voltage is not impressed.

In the above-mentioned semiconductor device, hydrogen is unevenly distributed in a region in the vicinity of the surface of the first-type III-V group compound semiconductor that is in contact with the second-type III-V group compound semiconductor. When the semiconductor device has been turned ON, the hydrogen atoms form a composite with the p-

type impurity in the region in which the two-dimensional, electron-gas layer is formed, and thereby the p-type impurity is inactivated. Thereby, when the semiconductor device has been turned ON, the two-dimensional, electron-gas layer is easily formed in the region in the vicinity of the surface of the first-type III-V group compound semiconductor that is in contact with the second-type III-V group compound semiconductor. A semiconductor device that operates as normally OFF can be obtained.

It is noted that, even if the p-type impurity in the region in which the two-dimensional, electron-gas layer is formed is inactivated, when the semiconductor device is turned OFF, a depletion layer that extends from the first-type III-V group compound semiconductor can sweep out the electrons existing in the region in which the two-dimensional, electron-gas layer is formed, and therefore the normally-OFF characteristic is maintained.

The above-mentioned semiconductor device implements a HEMT structure in which the channel resistance is small.

[0011]

The concentration of the hydrogen atoms in the uneven-distribution region of the hydrogen atoms preferably is greater than the concentration of the p-type impurity.

By setting the concentration of the hydrogen atoms higher than the concentration of the p-type impurity, substantially all of the p-type impurity existing in the uneven-distribution region of the hydrogen atoms is inactivated and constitutes a substantially i-type region. An MIS-type gate structure, in which the threshold voltage is extremely small, and a normally-OFF-type HEMT structure can be obtained.

[0012]

The p-type impurity preferably is magnesium.

As mentioned above, because the magnesium diffusion rate is extremely high, it is difficult to form a III-V group compound semiconductor in which the magnesium concentration is locally lowered. In the present invention, by forming a composite with the hydrogen atoms, the magnesium is inactivated. By locally inactivating the magnesium, a region can be formed in which the concentration of the "activated magnesium" is locally low. Even if the concentration of the "activated magnesium" is set low locally, because the concentration of the magnesium itself is the same as that of other regions, magnesium does not diffuse in from other regions. The present invention is particularly useful in situations in which magnesium is used as a p-type impurity.

[0013]

The III-V group compound semiconductor preferably is $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{N}$ (where $0 \leq x \leq 1$, $0 \leq y \leq 1$, and $0 \leq 1 - x - y \leq 1$).

A nitride-based III-V group compound semiconductor, in which the general formula is expressed by $\text{Al}_x\text{Ga}_y\text{In}_{1-x-y}\text{N}$, has a wide band gap compared with other semiconductor materials such as silicon. Consequently, compared with silicon and the like, the threshold voltage becomes adversely large. In addition, in this type of III-V group compound semiconductor, the magnesium diffusion rate is high.

The semiconductor device of the present invention is particularly useful in situations in which such a semiconductor material is used.

[0014]

The semiconductor device having the MIS-type gate structure of the present invention can be manufactured by the manufacturing method below, i.e., a manufacturing method comprising: a process of forming an insulating film on the front surface of a III-V group semiconductor that contains a p-type impurity; a process of forming a gate electrode on the front surface of the insulating film; and a process of heat treating the III-V group compound semiconductor in a gas atmosphere that contains hydrogen atoms.

When the heat treatment is performed, hydrogen atoms can be introduced into the front surface of the III-V group compound semiconductor. That is, hydrogen atoms can be introduced into the front surface of the III-V group compound semiconductor opposing the gate electrode. The introduced hydrogen atoms inactivate the p-type impurity. Thereby, an MIS-type gate structure, in which the threshold voltage has been adjusted to be small, can be obtained. A switching semiconductor device, having a combination of a low threshold voltage and a high withstand voltage, can be manufactured.

[0015]

With regard to the semiconductor device having the HEMT structure of the present invention, the semiconductor manufacturing method comprises, that is: a process of forming, on the front surface of a first-type III-V group compound semiconductor that contains a p-type impurity, a second-type III-V group compound semiconductor, which has a band gap that is greater than the band gap of the first-type III-V group compound semiconductor; and a process of heat treating the first-type III-V group compound semiconductor and the second-type III-V group compound semiconductor in a gas atmosphere that contains hydrogen atoms.

When the layered structure of the first-type and second-type III-V group compound semiconductors is heat treated, hydrogen atoms can be introduced into the region in the vicinity of the surface at which the first-type and second-type III-V group compound semiconductors are in contact with each other. A semiconductor device having a HEMT structure that operates as normally OFF can be obtained.

[0016]

The heat-treatment process that introduces hydrogen atoms preferably is performed within a temperature range of 400°C–1,000°C.

When heat treatment is performed in the above-mentioned temperature range, the hydrogen atoms can be efficiently introduced.

[0017]

The heat-treatment process that introduces hydrogen atoms preferably is performed after other heat-treatment processes needed to manufacture the semiconductor device have ended.

It is often the case that the processes of manufacturing the semiconductor device generally involve a process in which heat treatment is performed at high temperature. When the hydrogen atoms are introduced earlier than such a heat-treatment process, hydrogen atoms that were introduced into the III-V group compound semiconductor by subsequently performed heat-treatment processes adversely escape to the exterior. Accordingly, it is preferable that the hydrogen atoms be introduced after other heat-treatment processes needed to manufacture the semiconductor device have ended. When the hydrogen atoms are introduced in the final heat treatment, the hydrogen atoms introduced into the III-V group compound semiconductor can be made to remain in the III-V group compound semiconductor.

It is noted that, because the size of the hydrogen atoms is extremely small, even if some other structure such as a gate electrode is formed, the hydrogen atoms pass through that structure and can be introduced into the III-V group compound semiconductor.

EFFECTS OF THE INVENTION

[0018]

When the present invention is used, a region can be formed in which the concentration of an "activated p-type impurity" is locally lowered in a semiconductor device that uses a III-V group compound semiconductor. That is, it is possible to manufacture a semiconductor device that uses a III-V group compound semiconductor in which the concentration of the "activated p-type impurity" varies by location.

Even if the concentration of the p-type impurity that achieves a low threshold voltage and the concentration of the p-type impurity that achieves a high withstand voltage differ, it becomes possible to individually optimize the concentration of the "activated p-type impurity" in the region that affects the threshold voltage and the concentration of the "activated p-type impurity" in the region that affects the withstand voltage, and thereby a switching semiconductor device that has a combination of a low threshold voltage and a high withstand voltage can be implemented.

In the ON state, even if the concentration of the p-type impurity that implements the formation of the two-dimensional, electron-gas layer and the concentration of the p-type impurity needed to implement normally-OFF operation differ, it becomes possible to individually optimize the concentration of the "activated p-type impurity" in the region that affects the formation of the two-dimensional, electron-gas layer and the concentration of the "activated p-type impurity" in the region that affects the normally-OFF operation, and thereby it is possible to implement a HEMT-type switching semiconductor device that operates as normally OFF.

BEST MODES FOR CARRYING OUT THE INVENTION

[0019]

(First Embodiment) Hydrogen gas, a gas mixture of hydrogen gas and nitrogen gas, a gas mixture of hydrogen gas and argon (Ar) gas, a gas mixture of hydrogen gas and helium (He) gas, or the like can be used as a gas for introducing hydrogen atoms into a p-type semiconductor region.

(Second Embodiment) Hydrogen atoms penetrate from a front surface of a semiconductor device. The region in which it is desired to locally lower the concentration of an "activated p-type impurity" by introducing hydrogen preferably exists in the vicinity of the front surface of the semiconductor device. A channel region opposing a planar-gate electrode is in the vicinity of the front surface of the semiconductor device, and therefore the present invention can be applied satisfactorily. Alternatively, in a HEMT structure, in which a thin layer of a III-V group compound semiconductor having a wide band gap is layered on a III-V group compound semiconductor having a narrow band gap, a two-dimensional, electron-gas layer is formed directly below the thin layer. The region formed by the two-dimensional, electron-gas layer is in the vicinity of the front surface of the semiconductor device, and therefore the present invention can be applied satisfactorily.

(Third Embodiment) A heat-treatment process that introduces hydrogen atoms is performed after other heat-treatment processes required to manufacture the semiconductor

device have ended. The other heat-treatment processes include a heat-treatment process for forming a diffusion region, a heat-treatment process for forming various electrodes, and the like.

[Working Examples]

[0020]

The details of working examples will be explained below, with reference to the drawings.

(Working Example 1)

FIG. 1 schematically shows a longitudinal, cross-sectional view of the principal parts of a semiconductor device 10 having an MIS-type gate structure.

The semiconductor device 10 comprises, on its rear-surface side, a substrate 22 of sapphire (Al_2O_3). A semiconductor layer 32 of gallium nitride (GaN) is formed on the sapphire substrate 22. Magnesium is added to the semiconductor layer 32, and the magnesium acts as a p-type impurity of the semiconductor layer 32. A gate-insulating film 52 is formed on a portion of the front surface of the semiconductor layer 32, and a gate electrode 58 is formed on the front surface of the gate-insulating film 52. The gate electrode 58 is formed of polysilicon, and the gate-insulating film 52 is formed of silicon oxide. A local region 34 on a front-surface-side portion of the semiconductor layer 32 opposes the gate electrode 58 across the gate-insulating film 52.

A source region 42, which is composed of n^+ -type gallium nitride, and a drain region 46, which is composed of n^+ -type gallium nitride, are formed on the remainder of the front-surface side of the semiconductor layer 32. The n^+ -type source region 42 and the n^+ -type drain region 46 are spaced apart by the p-type semiconductor layer 32. The source region 42 is in contact with a source electrode 44, which is composed of aluminum (Al)/titanium (Ti). The drain region 46 is in contact with a drain electrode 48, which is composed of Al/Ti. A large amount of the hydrogen atoms is unevenly distributed in the local region 34 of the semiconductor layer 32 that opposes the gate electrode 58.

[0021]

The concentration of the magnesium impurity contained in the semiconductor layer 32 is adjusted to $1 \times 10^{19} \text{ cm}^{-3}$. Because the energy level of the magnesium impurity is deep, i.e., 160 meV, the Hall concentration at this time is approximately $1 \times 10^{17} \text{ cm}^{-3}$. Thereby, when the OFF voltage (e.g., 0 V) is impressed on the gate electrode 58, the OFF voltage is prevented from reaching the n^+ -type source region 42 by a depletion layer, which extends

from the p-n interface between the n⁺-type drain region 46 and the p-type semiconductor layer 32 to the interior of the p-type semiconductor layer 32. The occurrence of the so-called punch-through phenomenon is prevented. In addition, the distance between the source region 42 and the semiconductor layer 32 spaced apart from the drain region 46, which is necessary to avoid the occurrence of the punch-through phenomenon, is set by adjusting the impurity concentration of the semiconductor layer 32 to $1 \times 10^{19} \text{ cm}^{-3}$ such that it does not become too large. It is also possible to set the channel resistance so that it does not become too large while avoiding the occurrence of the punch-through phenomenon. By adjusting the impurity concentration of the p-type semiconductor layer 32 to $1 \times 10^{19} \text{ cm}^{-3}$, the occurrence of the punch-through phenomenon can be avoided while keeping the channel resistance small.

[0022]

The concentration of the hydrogen atoms existing in the local region 34 (uneven-hydrogen-distribution region) is higher than the concentration of the magnesium contained in the semiconductor layer 32. It is noted that, although it will be detailed in the explanation of a subsequent manufacturing method, the local region 34 is formed on a portion of the semiconductor layer 32. Accordingly, the concentration of the magnesium contained in the local region 34 is equal to the concentration of the magnesium contained in the remainder of the semiconductor layer 32. The hydrogen atoms contained in the local region 34 form a composite with the magnesium contained in the local region 34. Because the concentration of the hydrogen atoms of the local region 34 is higher than the concentration of the magnesium contained in the local region 34, substantially all of the magnesium forms a composite with the hydrogen atoms. Substantially all of the magnesium contained in the local region 34 is inactivated. The local region 34 is substantially an i-type region.

[0023]

When the ON voltage (positive voltage) is impressed on the gate electrode 58, an n-type inversion layer is formed in the substantially i-type local region 34, and the region between the source region 42 and the drain region 46 becomes conducting. Because the local region 34 is substantially an i-type, the gate voltage required to form an n-type inversion layer is low. The semiconductor device 10 has the characteristics of being able to operate at a low threshold voltage, having low loss, and having a high withstand voltage.

[0024]

Next, a method of manufacturing the semiconductor device 10 will be explained, with reference to FIG. 2 to FIG. 5.

First, as shown in FIG. 2, the sapphire substrate 22 is prepared. Next, the semiconductor layer 32 of gallium nitride (GaN), which contains magnesium, is formed on the sapphire substrate 22 using the metalorganic vapor-phase epitaxial (MOCVD) method. At this time, trimethyl gallium (TMGa) can be used as the gallium raw material, ammonia gas (NH₃) can be used as the nitrogen raw material, and cyclopentadienylmagnesium (CP2Mg) can be used as the impurity material. The amount of cyclopentadienylmagnesium (CP2Mg) supplied is adjusted such that the concentration of the magnesium of the semiconductor layer 32 becomes $1 \times 10^{19} \text{ cm}^{-3}$ or more.

It is noted that, prior to forming the semiconductor layer 32 of gallium nitride, which contains magnesium, a buffer layer, which is composed of gallium nitride that does not contain magnesium, may be formed on the sapphire substrate 22 using the metalorganic vapor-phase epitaxial method. At this time, trimethyl gallium (TMGa) can be used as the gallium raw material, and ammonia gas (NH₃) can be used as the nitrogen raw material.

[0025]

Next, as shown in FIG. 3, after a trench, which extends from a prescribed region of the front surface of the semiconductor layer 32 to the interior of the semiconductor layer 32, has been formed, the source region 42 and the drain region 46 are formed within that trench using the metalorganic vapor-phase epitaxial method. To form the trench, for example, the RIE (reactive-ion etching) method can be used. To form the source region 42 and the drain region 46, the metalorganic vapor-phase epitaxial method can be used, wherein trimethyl gallium (TMGa) is used as the gallium raw material, ammonia gas (NH₃) is used as the nitrogen raw material, and monosilane (SiH₄) is used as the impurity material. It is noted that, instead of the above-mentioned manufacturing method, crystals of n⁺-type gallium nitride may be grown uniformly on the front surface of the semiconductor layer 32 and subsequently etched selectively so that the source region 42 and the drain region 46 remain.

Next, as shown in FIG. 4, the gate-insulating film 52, which is composed of silicon oxide, is formed using the CVD (chemical vapor deposition) method on the front surface of the semiconductor layer 32, which spaces apart the source region 42 and the drain region 46.

Next, the gate electrode 58, which is composed of polysilicon, is formed using the CVD method.

Next, the source electrode 44, which is composed of Al/Ti, and the drain electrode 48, which is composed of Al/Ti, are formed using the sputtering method. The source electrode 44

is in contact with the source region 42, and the drain electrode 48 is in contact with the drain region 46.

[0026]

Next, the semiconductor device 10 formed up to the above-mentioned stage is heat treated inside a chamber, which is supplied with a gas mixture of hydrogen gas (H_2) and nitrogen gas (N_2). The hydrogen-gas concentration at this time is adjusted to 10%, the heating temperature is 900°C, and the heat-treatment time is 20 min.

As shown in FIG. 5, the hydrogen gas is ionized, and a portion of those hydrogen ions (H^+) pass through the gate electrode 58 and the gate-insulating film 52 and are introduced into the front-surface side of the semiconductor layer 32. Because the size of hydrogen ions (H^+) is small, the hydrogen ions can pass through the gate electrode 58 and the gate-insulating film 52. As needed, the region into which the hydrogen atoms are to be introduced, the concentration distribution of the hydrogen atoms to be introduced, and the like can be adjusted by forming in advance on the front-surface side of the semiconductor device 10 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these.

The hydrogen atoms introduced form a composite (MgH) with the magnesium existing in the semiconductor layer 32. The magnesium that has formed a composite with the hydrogen atoms is inactivated. Thereby, as shown in FIG. 1, the local region 34, which has been substantially changed to an i-type, is formed on the front-surface side of the semiconductor layer 32 opposing the gate electrode 58.

It is noted that a portion of the hydrogen atoms is also introduced into the source region 42 and the drain region 46. Nevertheless, the impurity concentrations of the source region 42 and the drain region 46 are sufficiently large compared with the concentrations of the hydrogen atoms introduced. Accordingly, no problem is created by the introduction of hydrogen atoms to the source region 42 and the drain region 46.

[0027]

By adjusting the heating temperature, the heat-treatment time, etc., the amount of hydrogen atoms introduced can be adjusted. The heating temperature is preferably in the range of 400°C–1,000°C. The hydrogen atoms can be introduced efficiently. In particular, it is important that the upper limit of the heating temperature is adjusted so that it does not exceed 1,200°C. If the heating temperature is too high, then the front surface will not only be ruined but the nitrogen atoms of GaN will adversely separate and escape to the exterior. In addition, by adjusting the heating temperature to 1,000°C or lower, the hydrogen atoms can

be introduced into the interior of the semiconductor layer 32. To inhibit the escape of the introduced hydrogen atoms to the exterior, it is preferable to set the process sequence such that the heat-treatment process that introduces the hydrogen atoms is performed after all other heat-treatment processes needed to manufacture the semiconductor device 10 have ended, i.e., in the last stage. In the present working example, because the heat treatment for introducing the hydrogen atoms is performed in the last stage, the escape of the introduced hydrogen atoms to the exterior by other heat treatments is prevented. The introduced hydrogen atoms can be caused to remain inside the local region 34.

[0028]

FIG. 6 shows the relationship between the gate voltage and the drain current of the semiconductor device 10. Plot 10 in FIG. 6 is the result of the semiconductor device 10. Plot 12 in FIG. 6 is the result of a comparative example, in which the heat-treatment process for introducing the hydrogen atoms is not performed.

With regard to the drain current in the case of the comparative example, the drain current starts to increase when the gate voltage exceeds approximately 15 V. On the other hand, with regard to the drain current in the case of the semiconductor device 10, the drain current starts to increase when the gate voltage exceeds approximately 5 V. It is understood that the threshold voltage of the semiconductor device 10 is lowered compared with the threshold voltage of the comparative example. From this, it is understood that the threshold voltage is lowered by performing the heat treatment that introduces the hydrogen atoms.

[0029]

The above-mentioned manufacturing method additionally has the following features.

(1) Even though hydrogen atoms are introduced, crystalline defects do not occur all that much in the semiconductor layer 32. Because the characteristics of the semiconductor device are not degraded, it is possible to form the local region 34 in which hydrogen is unevenly distributed.

(2) By forming the local region 34, in which hydrogen is unevenly distributed, at the junction interface between the gate-insulating film 52 and the semiconductor layer 32, the interface energy level can be reduced. The effects of stabilized threshold voltage, increased switching speed, and the like are obtained.

(3) By adjusting the temperature, the time, and the like of the heat treatment for introducing hydrogen atoms, the introduction of hydrogen atoms as far as the deep part of the semiconductor layer 32 can be prevented. Hydrogen atoms can be introduced limited to the region in the vicinity of the interface between the gate-insulating film 52 and the

semiconductor layer 32. Thereby, the range over which the local region 34 is formed can be set to outside the range that is affected by the OFF voltage of the gate electrode 58.

Accordingly, even if it is assumed that the substantially i-type local region 34 has been provided, the punch-through phenomenon does not occur when the semiconductor device 10 has been turned OFF.

(4) As was explained in the Background Art section, the rate of diffusion of the magnesium contained in the gallium nitride is extremely fast. Consequently, it is difficult to locally form a region that contacts the semiconductor layer of gallium nitride, which contains magnesium, and in which the magnesium concentration is adjusted lower than the concentration of the magnesium impurity of that semiconductor layer. In the above-mentioned manufacturing method, the magnesium is inactivated by the use of hydrogen atoms. By inactivating the magnesium, a local region is formed in which the concentration of active magnesium is low. New magnesium does not diffuse from other regions. The above-mentioned manufacturing method is particularly useful in the situation in which magnesium is used as a p-type impurity.

[0030]

(Working Example 2)

FIG. 7 schematically shows a longitudinal, cross-sectional view of the principal parts of a semiconductor device 100, which has a HEMT structure.

On its rear-surface side, the semiconductor device 100 comprises a sapphire substrate 122. A first semiconductor layer 132 of gallium nitride (GaN) is formed on the sapphire substrate 122. Magnesium, which is a p-type impurity, is added to the first semiconductor layer 132. A second semiconductor layer 136 of aluminum gallium nitride (AlGaN) is formed in contact with the first semiconductor layer 132. The second semiconductor layer 132 contains aluminum and has a band gap that is wider than that of the first semiconductor layer 132. A gate-insulating film 152 is formed on a portion of the front surface of the second semiconductor layer 132, and a gate electrode 158 is formed on the front surface of the gate-insulating film 152. The gate electrode 158 opposes the front surface of the second semiconductor layer 136 across the gate-insulating film 152. The gate electrode 158 is formed of polysilicon, and the gate-insulating film 152 is formed of silicon oxide. A local region 134 (uneven-hydrogen-distribution region), in which a large amount of hydrogen atoms exists, is formed in a region in the vicinity of the surface of the first semiconductor layer 132 that is in contact with the second semiconductor layer 136.

A source electrode 144 and a drain electrode 148 are formed at locations that are spaced apart by the gate electrode 158. The source electrode 144 and the drain electrode 148 have a layered structure of titanium (Ti) and aluminum (Al) and make ohmic contact with the second semiconductor layer 136.

It is noted that it is also possible to use a structure in which, instead of the gate electrode 158 and the gate-insulating film 152, for example, a gate electrode having a layered structure of nickel (Ni) and gold (Au) can be caused to form a Schottky junction with the front surface of the second semiconductor layer 136.

[0031]

The concentration of the hydrogen atoms unevenly distributed in the local region 134 is higher than the concentration of the magnesium impurity contained in the first semiconductor layer 132. It is noted that, although detailed in the explanation of a subsequent manufacturing method, the local region 134 is formed as a portion of the first semiconductor layer 132. Accordingly, the concentration of the magnesium contained in the local region 134 equals the concentration of the magnesium contained in the remainder of the first semiconductor layer 132. The hydrogen atoms contained in the local region 134 form a composite with the magnesium contained in the local region 134. Because the concentration of the hydrogen atoms of the local region 134 is higher than the concentration of the magnesium contained in the local region 134, substantially all of the magnesium forms a composite with the hydrogen atoms and is electrically inactivated. The local region 134 is substantially an i-type region.

[0032]

The first semiconductor layer 132 and the second semiconductor layer 136 constitute a HEMT structure. Thereby, a two-dimensional, electron-gas layer (2DEG) is formed in a region in the vicinity of the surface of the first semiconductor layer 132 that is in contact with the second semiconductor layer 136. When the semiconductor device 100 is ON, electrons travel along this two-dimensional, electron-gas layer. Because the above-mentioned HEMT structure is constituted using the p-type first semiconductor layer 132, the two-dimensional, electron-gas layer is not formed in the state in which the gate voltage is not impressed. It can be caused to operate as so-called normally OFF.

It is noted that, even if the local region 134 is provided, because the depletion layer extending from the first semiconductor layer 132 can sweep out the electrons existing in the local region 134 when the semiconductor device 100 has been turned OFF, normally-OFF operation is maintained.

[0033]

Next, a method of manufacturing the semiconductor device 100 will be explained, with reference to FIG. 8 to FIG. 11.

First, as shown in FIG. 8, the sapphire substrate 122 is prepared. Next, the first semiconductor layer 132, which is composed of gallium nitride that contains magnesium, is formed on the sapphire substrate 122 using the metalorganic vapor-phase epitaxial method. At this time, trimethyl gallium (TMGa) can be used as the gallium raw material, ammonia gas (NH₃) can be used as the nitrogen raw material, and cyclopentadienylmagnesium (CP2Mg) can be used as the impurity material.

It is noted that, prior to forming the first semiconductor layer 132, a buffer layer composed of gallium nitride that does not contain magnesium may be formed on the sapphire substrate 122 using the metalorganic vapor-phase epitaxial method. At this time, trimethyl gallium (TMGa) can be used as the gallium raw material, and ammonia gas (NH₃) can be used as the nitrogen raw material.

[0034]

Next, the AlGaN layer 34 is formed on the first semiconductor layer 132 using the metalorganic vapor-phase epitaxial method. At this time, trimethyl aluminum (TMAI) can be suitably used as the aluminum raw material, trimethyl gallium (TMGa) can be suitably used as the gallium raw material, and ammonia gas (NH₃) can be suitably used as the nitrogen raw material. It is noted that, monosilane (SiH₄), which is for introducing silicon that behaves as an n-type impurity, may be used at the same time in the film-forming process of the second semiconductor layer 136. An n-type impurity may be introduced into the second semiconductor layer 136.

[0035]

Next, various electrodes are formed on the front-surface side of the second semiconductor layer 136.

First, titanium (Ti) and aluminum (Al) are vapor deposited, in order, on the second semiconductor layer 136. Subsequently, the source electrode 144 and the drain electrode 148 are patterned using a photolithographic technique and an etching technique. After patterning, the source electrode 144 and the drain electrode 148 are brought into ohmic contact with the second semiconductor layer 136 by performing a heat treatment.

Next, the gate-oxide film 152 is formed between the source electrode 144 and the drain electrode 148 using the CVD method. Next, the gate electrode 158, which is composed of polysilicon, is formed using the CVD method.

It is noted that, in the situation in which a gate electrode of a type that forms a Schottky junction is used, the gate electrode can be formed using the lift-off method. That is, after the resist film has been formed outside of the location at which it is desired to form the gate electrode, nickel (Ni) and gold (Au) are vapor deposited, in order. Subsequently, the resist film, together with the nickel (Ni) and the gold (Au) formed on that resist film, are stripped. Thereby, a gate electrode that forms a Schottky junction with a prescribed positional relationship can be formed.

[0036]

Next, the semiconductor device 100 formed up to the above-mentioned stage is heat treated inside a chamber, which is supplied with a gas mixture of hydrogen gas (H_2) and nitrogen gas (N_2). The hydrogen-gas concentration at this time is adjusted to 10%, the heating temperature is $900^\circ C$, and the heat-treatment time is 20 min.

As shown in FIG. 11, the hydrogen gas is ionized, and a portion of those hydrogen ions (H^+) pass through the gate electrode 158, the gate-insulating film 152, and the second semiconductor layer 136, and are introduced into the front-surface side of the first semiconductor layer 132. Because the size of hydrogen ions (H^+) is small, the hydrogen ions can pass through the gate electrode 158, the gate-insulating film 152, and the second semiconductor layer 136. As needed, the vicinity into which the hydrogen atoms are to be introduced, the concentration distribution of the hydrogen atoms to be introduced, and the like can be adjusted by forming in advance on the front-surface side of the semiconductor device 100 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these.

The hydrogen atoms introduced form a composite (MgH) with the magnesium existing in the first semiconductor layer 132. The magnesium that has formed a composite is inactivated. Thereby, as shown in FIG. 7, the substantially i-type local region 134 is formed in the region in the vicinity of the interface between the first semiconductor layer 132 and the second semiconductor layer.

[0037]

Concrete examples of the present invention were explained in detail above, but these are merely illustrative examples and do not limit the scope of the claims. Various modifications and changes to the concrete examples illustrated above are included in the techniques described in the scope of the claims.

In addition, the technical elements described in the present specification and the drawings exhibit technical utility independently or in various combinations and are not

limited to the combinations described in the claims when the patent application was filed. In addition, the techniques illustrated in the present specification and the drawings can simultaneously achieve a plurality of objects and have technical utility on their own in achieving a single object among them.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038]

FIG. 1 schematically shows a longitudinal, cross-sectional view of the principal parts of a semiconductor device according to Working Example 1.

FIG. 2 shows a process (1) of manufacturing the semiconductor device according to Working Example 1.

FIG. 3 shows a process (2) of manufacturing the semiconductor device according to Working Example 1.

FIG. 4 shows a process (3) of manufacturing the semiconductor device according to Working Example 1.

FIG. 5 shows a process (4) of manufacturing the semiconductor device according to Working Example 1.

FIG. 6 shows the relationship between the gate voltage and the drain current of the semiconductor device according to Working Example 1.

FIG. 7 schematically shows a longitudinal, cross-sectional view of the principal parts of the semiconductor device according to Working Example 2.

FIG. 8 shows a process (1) of manufacturing the semiconductor device according to Working Example 2.

FIG. 9 shows a process (2) of manufacturing the semiconductor device according to Working Example 2.

FIG. 10 shows a process (3) of manufacturing the semiconductor device according to Working Example 2.

FIG. 11 shows a process (4) of manufacturing the semiconductor device according to Working Example 2.

EXPLANATION OF THE REFERENCE NUMBERS

[0039]

22, 122	Sapphire substrates
32	Semiconductor layer
34, 134	Regions in which hydrogen is locally distributed unevenly
42	Source region

44, 144	Source electrodes
46	Drain region
48, 148	Drain electrodes
52, 152	Gate-insulating films
58, 158	Gate electrodes
132	First semiconductor layer
136	Second semiconductor layer

FIG. 4

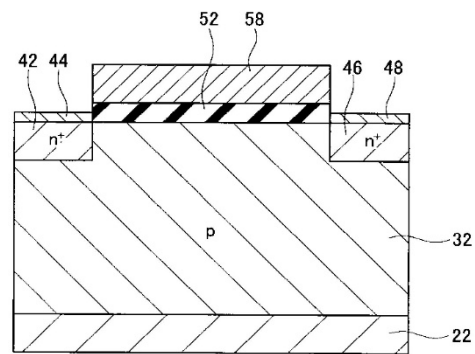


FIG. 5

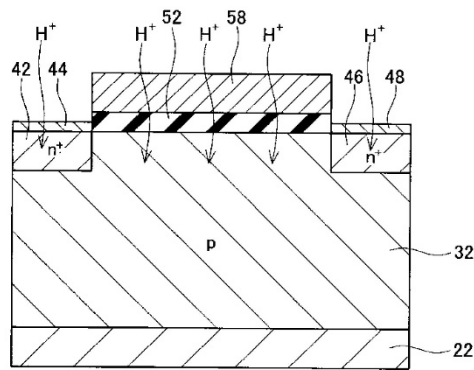


FIG. 7

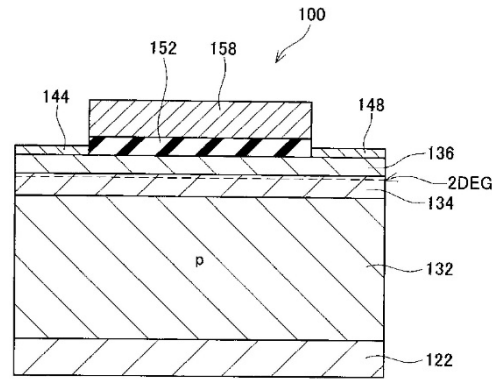


FIG. 6

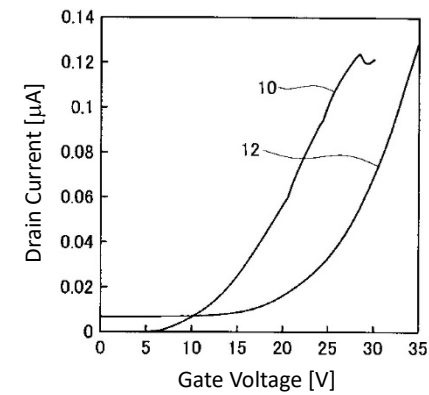
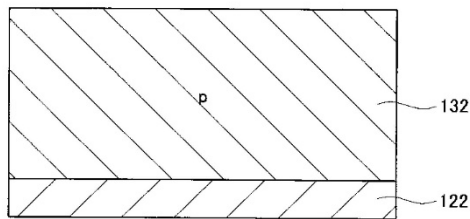


FIG. 8



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FIG. 11

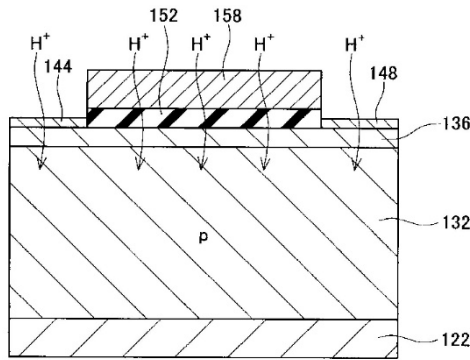
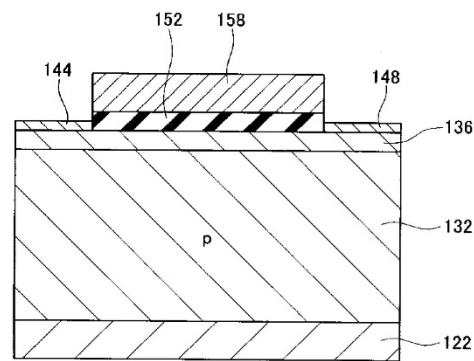


FIG. 10



Continuation of front page

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GG44 GG58 HK03 HK04 HK08 HK21 HK33 HK34
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BC17 BD06 BE10 BF01 BF04 BG28 BG44 BH25 BH26 BH27
BJ07 BJ11 BJ15 BK09 BK18 BK29