

Rüdiger Quay

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Gallium Nitride Electronics

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III-N Materials, and the State-of-the-Art of Devices and Circuits

In this chapter, general material and transport properties, advantages, and theoretical electrical and thermal limits of nitride semiconductors are presented with respect to electronic applications. This chapter further provides an overview of substrate materials. The state-of-the-art for nitride-based materials, electronic devices, and circuits are reviewed systematically. The last section defines application-specific requirements on nitride semiconductor devices from a more system oriented point of view. The chapter concludes with a number of problems.

2.1 State-of-the-Art of Materials Research

A systematic overview of the material properties is given in the following. For a systematic introduction, Fig. 2.1 depicts the bandgap at a lattice temperature of 300 K for various semiconductor materials as a function of lattice constant. The selection of the specific material constant as lattice constant in noncentrosymmetric materials may be arbitrary, however, is useful for a systematic introduction. With the bandgap of InN recently suggested to be about 0.8 eV and the bandgap of AlN to be 6.2 eV at room temperature, the III-N material system covers a very broad range of energies and thus emission wave lengths from the infrared to the deep ultraviolet unchallenged by any other available material. Electronically, a very broad range of bandgap energies is found resulting in extremely high bulk material breakdown voltages, which can be traded in for low-effective mass and high mobility of GaN with $m_n = 0.2 m_e$, or even of InN with $m_n = 0.11 m_e$ (potentially even $m_n = 0.04 m_e$ [2.122]) by changing the material compositions in the heterostructures. At the same time, a second trade-off is imminent and different from any other semiconductor material system. Due to the strong polar material properties, the modification of the material composition results in dramatic modifications of the polar crystal properties, and thus of available

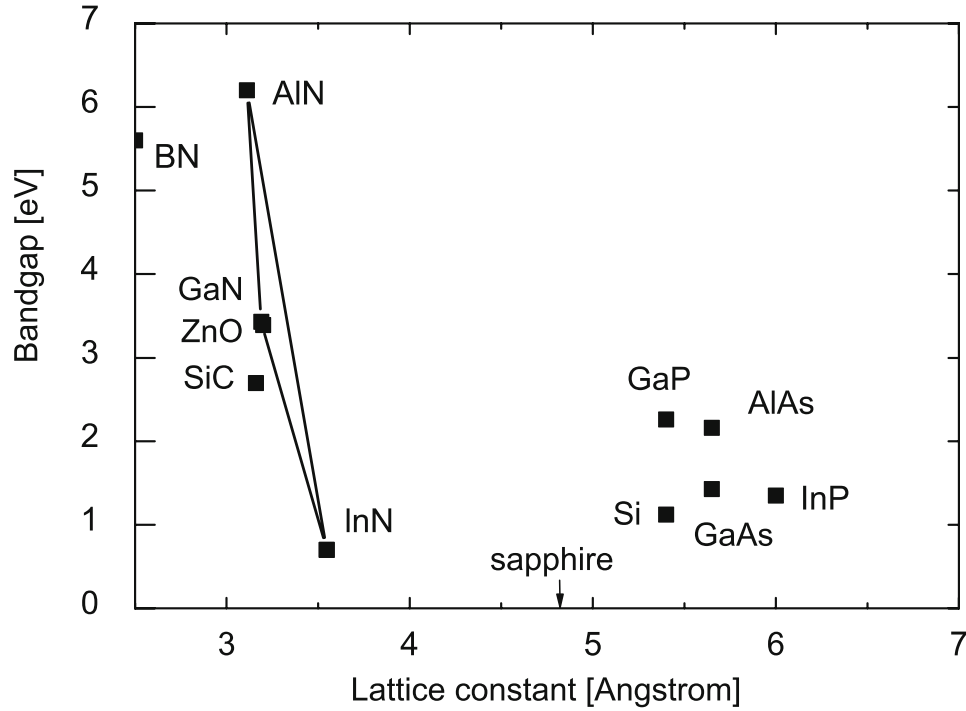


Fig. 2.1. Bandgap energy at $T_L = 300$ K as a function of lattice constant of III-N semiconductors: Other III-V semiconductors are given for comparison

carrier concentrations obtained at the interfaces and thus available in the devices. Thus, and in some respect very similar to silicon, the huge success of III-N material is not mainly due to the intrinsic bulk material transport properties (especially the p-material properties do not compare well with n-properties in III-N materials), but due to the interface properties. In the case of silicon, the success is based on the formation of a native oxide which can be optimized and used tremendously, e.g., [2.411], and is recently replaced by other dielectrics, which also are well behaved on silicon, e.g., [2.136, 2.145].

In the case of III-N heterostructures, the interfaces allow for the formation of n-channels and intrinsically provide extremely high carrier concentrations $\geq 10^{13} \text{ cm}^{-2}$ through polarization engineering without further impurity doping. On the contrary, and unlike silicon, the semiconductor–dielectric interfaces remain a challenge in the III-N world, as suitable interfaces can be formed from a practical point of view, however, these interfaces and their long term behavior are not well understood mainly due to the high-sheet charge concentrations.

2.1.1 Binary Materials

The binaries of the elements Al–In–Ga–B–N are the basic materials for the semiconductor material class named Nitrides: gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN), and boron nitride (BN). Epi-

taxially grown silicon nitride (SiN), although not of crystalline quality, may be added from time to time. Boron nitride (BN) is still relatively immature as a semiconductor material [2.99]. Initial results on the material and device level are available [2.99], featuring the especially good thermal conductivity of BN, second only to diamond when semiconductor materials are compared. Good overview papers and collections are available, with a focus also on optoelectronic and general material properties, and, e.g., in [2.100, 2.101, 2.244, 2.315, 2.324, 2.369, 2.389]. Laser diodes are particularly addressed in [2.323]. The properties of SiN and SiO₂ are reviewed, e.g., in [2.440].

Crystal Structures for Electronic Applications

The III-N semiconductors can be found in three common crystal structures:

- Wurtzite
- Zincblende
- Rock salt

At room temperature GaN, AlN, and InN are found in the wurtzite structure, while BN prevails mostly in the cubic structure. The zincblende structure can also be found for GaN and InN for thin films, while for AlN no stable zincblende phase has yet been detected [2.99]. However, this work addresses also some mostly theoretical work on Zb-AlN. The rock salt phase is of no importance to electronic devices so far. In the wurtzite structure the growth is typically performed along the *c*-axis. Recently, growth along the *m*-plane has been reported [2.61, 2.342], as the resulting nonpolar material has a positive influence on diodes efficiency in optoelectronics.

Gallium Nitride (GaN)

Gallium Nitride (GaN) is the basic material of this material class which is typically used for all device layers requiring fast carrier transport with a high breakdown voltage. GaN is used as the channel material in various FETs and also as the base material in AlGaIn/GaN HBTs, e.g., [2.311]. Most of the ohmic contact layers in any device incorporate binary n-doped and p-doped GaN. GaN can further be grown as a semi-insulating material with growth parameters close to those of the semiconducting layers.

Mechanical and Optical Properties

The crystal structure and the mechanical and thermal properties of GaN are discussed in a number of publications, e.g., in [2.4, 2.244, 2.315, 2.389]. The data of all III-N binaries are also compiled in table form in the Appendix. As an initial quantity, Table 2.1 compiles the data on the mass density. The Vickers hardness and fracture toughness of bulk GaN in comparison to other semiconductors are given in [2.92]. More recent results are presented in [2.524]. Table 2.2 compares the values of the hardness *H* and fracture toughness *K_C*.

Table 2.1. Mass density of III-N and other semiconductor materials

Material	GaN	AlN	InN	BN	Si	Ref.
Mass density (g cm^{-3})	6.1	3.23	6.81	3.48	2.33	[2.17, 2.99, 2.443]
<i>Wz</i> wurtzite, <i>Zb</i> zincblende, <i>c</i> cubic, <i>d</i> diamond						

Table 2.2. Vickers hardness H and fracture toughness K_C of III-N and other semiconductor materials

Material	GaN	AlN	InN	BN	SiC	Si	Ref.
H (GPa)	12	14	11.2	55–65	33	9	[2.92, 2.451]
K_C ($\text{MPa m}^{1/2}$)	0.8	2.6	–	–	3.3	0.7	[2.92, 2.244]

Table 2.3. Elastic constants of wurtzite III-N semiconductors and other materials

	GaN (Wz)	AlN (Wz)	InN (Wz)	BN (c)	Ref.
C_{11} (GPa)	390	396	223	831	[2.99, 2.275, 2.372, 2.449, 2.485]
C_{33} (GPa)	398	373	200	–	[2.99, 2.275, 2.372, 2.449, 2.485]
C_{44} (GPa)	105	116	48	450	[2.372, 2.451, 2.485]
C_{12} (GPa)	145	137	115	190	[2.99, 2.275, 2.372, 2.449, 2.485]
C_{13} (GPa)	106	108	92	–	[2.275, 2.372, 2.449, 2.485]
<i>Wz</i> wurtzite, <i>c</i> cubic					

Table 2.4. Elastic constants of zincblende III-N semiconductors

	GaN (Zb)	AlN (Zb)	InN (Zb)	BN (c)	Si	Ref.
C_{11} (GPa)	293	304	187	820	165.8	[2.244, 2.371, 2.485]
C_{44} (GPa)	155	193	86	480	79.6	[2.244, 2.371, 2.485]
C_{12} (GPa)	159	160	125	190	63.9	[2.244, 2.371, 2.485]
<i>Wz</i> wurtzite, <i>Zb</i> zincblende, <i>c</i> cubic						

Table 2.5. Coefficients of thermal expansion (CTE) of III-N semiconductors and other materials at room temperature

	GaN (Wz)	GaN (Sa)	AlN (p)	InN (p)	BN (c)	SiC	Sap.	Si	Ref.
α_a ($10^{-6} K^{-1}$)	3.1	3.8	2.9	3.6	1.15	3.2	4.3	2.6	[2.99, 2.222, 2.243]
α_c ($10^{-6} K^{-1}$)	2.8	2.9	3.4	2.6	–	3.2	3.2	2.6	[2.222, 2.243]
<i>Wz</i> wurtzite, <i>Sa</i> epitaxially on sapphire substrate, <i>c</i> cubic, <i>p</i> powder									

c-BN is a particularly hard material, while GaN, AlN, and InN have nearly the same hardness. This hardness makes c-BN attractive in various ceramic materials. The elastic constants of wurtzite gallium nitride determined by Brillouin scattering are reported, for example, in [2.372] and are compiled in Table 2.3. A prediction of the high-temperature elastic constants of GaN, AlN, and InN is given in [2.381]. Deduced from this, a bulk modulus B_0 of GaN is found to be 210 GPa. For BN, a comparison of the different calculated and measured values is given in [2.99]. First principle calculations of the properties of zincblende AlN and GaN are given in [2.177]. The elastic constants of the zincblende phase are compiled in Table 2.4. The pressure dependence of the elastic constants of zincblende BN, AlN, GaN, and InN is analyzed in [2.178].

The linear coefficients of thermal expansion (CTE) at room temperature and at elevated temperatures are important for the growth. Those of wurtzite GaN have been measured between room temperature and ≥ 750 K for both bulk GaN and epitaxial layers grown on sapphire, e.g., in [2.243]. The data are compiled in Table 2.5. Table 2.5 further compares the CTE of III-N semiconductors to silicon carbide and other typical substrates materials. The differences in CTE and its temperature dependence have a similar impact to layer growth of heterostructures as the lattice constants, as discussed in Chapter 3. The thermal conductivity of GaN was initially reported in [2.423] and many of the references date back to this publication. More recent measurements, especially as function of dislocation density in thin layers, can be found in [2.120, 2.216, 2.264] and are discussed later with respect to the modeling and the importance of the crystalline quality. The data are compiled in Table 2.16.

Dielectric Constants

Compiling the basic dielectric properties, Table 2.6 gives both the static and the high-frequency dielectric constants. The dielectric constant of GaN is slightly lower than in silicon and GaAs (not shown). InN has the highest values of the three binary materials.

Overviews of further optical functions of GaN such as the refractive index are given in [2.3, 2.298]. The absorption spectrum of GaN at room temperature and the absorption coefficient are presented in [2.64].

Table 2.6. Dielectric constants of III-N and other semiconductor materials

Material	GaN	AlN	InN	GaN	BN	Si	Ref.
	(Wz)	(Wz)	(Wz)	(Zb)	(c)		
ϵ_r	9.5 $\perp$, 10.4 $\parallel$	8.5	15.3	9.5	7.1	11.9	[2.3, 2.64, 2.492]
ϵ_r^{inf}	5.5	4.77	8.4	5.35	4.5	—	[2.3, 2.64, 2.492]

Wz wurtzite, Zb zincblende, and c cubic

Basic Transport Properties

Electronic transport in GaN is mostly understood, but a number of issues remain for further research. These include, e.g., the maximum carrier velocity v_{peak} in bulk material and at heterointerfaces, which are discussed later. General electrical properties of GaN, as well as AlN and $\text{Al}_x\text{Ga}_{1-x}\text{N}$, are compiled in [2.123]. An early, but accurate estimate of the carrier concentration dependence of the bulk mobility in GaN, InN, and AlN using the variational method is given in [2.64]. Based on more recent data, a mobility and carrier vs. doping concentration analysis for wurtzite MOCVD-grown bulk GaN is provided in [2.259]. Both donor and acceptor concentrations in the order of 10^{17} cm^{-3} are extracted. A specific mobility model for bulk GaN including the dependence on the free electron concentration is given in [2.308]; however, newer experimental results require an update of the actual parameters.

Table 2.7. Comparison of the low-field mobility values in various III-N bulk and 2DEG materials

Material	n/p	T_L (K)	N_D/N_A (cm^{-3})	μ ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	Method	Ref.
GaN (Wz)	n	300	$N_D = 1 \times 10^{17}$	990	MC	[2.113]
GaN (Wz)	n	450	$N_D = 1 \times 10^{17}$	391	MC	[2.113]
GaN (Wz)	n	600	$N_D = 1 \times 10^{17}$	215	MC	[2.113]
GaN (Wz)	p	300	$N_A = 3.6 \times 10^{16}$	150	meas.	[2.123]
GaN (Wz)	n 2DEG	300	0	2,000	MC	[2.337]
GaN (Wz)	n	77	$N_D = 1 \times 10^{16}$	6,000	VP	[2.64]
GaN (Zb)	n	300	$N_D = 1 \times 10^{17}$	1,100	MC	[2.17]
GaN (Zb)	n 2DEG	300	0	2,100	MC	[2.337]
GaN (Zb)	p	300	$N_A = 1 \times 10^{13}$	350	meas.	[2.21]
AlN (Wz)	n	300	$N_D = 1 \times 10^{17}$	135	MC	[2.349]
AlN (Wz)	n	77	$N_D = 1 \times 10^{16}$	2,000	VP	[2.64]
AlN (Zb)	n	300	0	200	MC	[2.17]
AlN (Zb)	n	100	0	400	MC	[2.17]
InN (Wz)	n	300	$N_D = 1 \times 10^{17}$	3,000	MC	[2.35]
InN (Wz)	n	300	$N_D = 1.5 \times 10^{17}$	3,570	meas.	[2.114]
InN (Wz)	n	77	$N_D = 1 \times 10^{16}$	30,000	VP	[2.64]
InN (Zb)	n	100	$N_D = 1 \times 10^{17}$	9,000	MC	[2.17]
BN (c)	p	300	$N_A = 5 \times 10^{18}$	500	meas.	[2.253]

Wz wurtzite, Zb zincblende, c cubic, VP variational principle, MC Monte Carlo, meas. measured

Low-Field Mobility

Several predictions and measurements are available for obtaining estimates for the maximum low-field mobility in both bulk and 2DEG electron gas. Table 2.7 compiles the data of the low-field mobility with respect to temperature and impurity dependence of the mobility in III-N bulk materials. The maximum values from [2.64] are given for completely uncompensated material.

Recent advances in material growth show great improvements in channel mobility of optimized AlGaIn/GaN 2DEG channel-layer material with Hall mobility values of up to $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [2.435] at room temperature in agreement with theoretical predictions [2.337]. For the analysis of the mobility in bulk and 2DEG-GaN, the temperature dependence is plotted in Fig. 2.2 taken from [2.37] and data therein. The effects to influence mobility include:

- Phonon scattering by acoustic and optical phonons
- Ionized impurity scattering [2.37] at both background impurities and surface donors
- Threading dislocations [2.258, 2.329, 2.435]
- Alloy scattering [2.34, 2.414]

The maximum drift mobility of wurtzite bulk GaN is about $1,100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The hole mobility in bulk GaN is much lower with maximum values of $175 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The reduced impurity scattering in 2DEG channels at

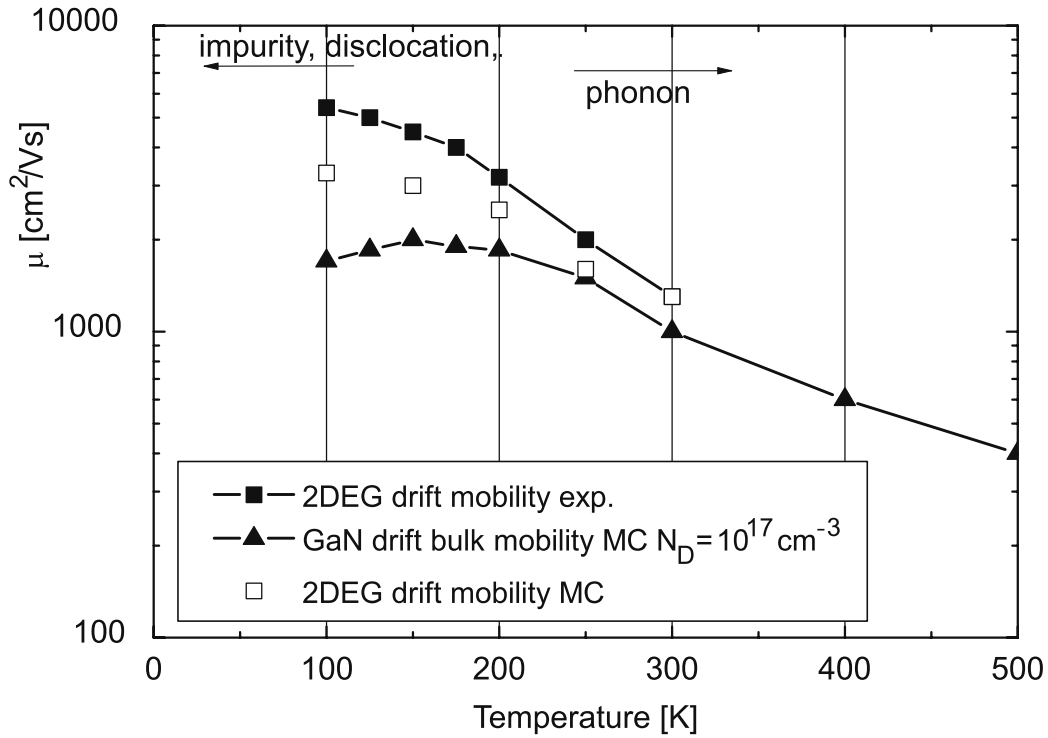


Fig. 2.2. Drift mobility as a function of lattice-temperature T_L for bulk GaN and 2DEG-GaN depicting the different limiting effects from [2.37, 2.329]

very low surface scattering levels yield 2DEG-mobility values of up to $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for both wurtzite and zincblende material. A theory of charged dislocation scattering in GaN is given [2.258]. The fit of the temperature-dependent Hall data can be correlated with the dislocations observed by TEM. The impact of threading dislocations on the transverse mobility in GaN is further discussed in [2.493]. The model explains the impact of trap occupancy and related scattering on the mobility at different doping levels. Alloy disorder is a limiting factor to transport at GaN heterointerfaces, as discussed in [2.414]. Further analysis is provided in Chapter 3. AlN is an insulator due to the high activation energy of the donors and the large bandgap. The theoretical low-field mobility of AlN is discussed in [2.17]. It is found to be phonon-limited with the electron mobility values given in Table 2.7. Theoretical values for the drift mobility of $135 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for fully uncompensated material have been found. Similar to InN, the hole transport properties of AlN are not understood very well. The predicted low-field drift mobility of InN at room temperature is found to be as high as $3,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in [2.35] and $3,700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in [2.17]. At 100 K, a maximum low-field mobility as high as $9,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is predicted for zincblende InN material [2.17]. Variational principle calculations leads to predictions of $30,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 77 K for completely uncompensated material at low impurity concentrations of 10^{16} cm^{-3} . Again, hole transport in InN is not well understood due to the lack of proper p-doping [2.170].

High-Field Transport

Several MC calculations of the velocity-field characteristics of wurtzite GaN considering the high-field transport are available and given, e.g., in [2.37, 2.121]. There is a significant discussion on the extraction of delay times in HFETs and resulting carrier velocities, which disagree with the MC calculations, see also Sect. 2.2.7. Table 2.8 compiles the bulk saturation velocity and critical field parameters from various sources. The comparison reveals the increase of both the saturation velocity v_{sat} and the critical field E_{crit} compared to other high-speed materials such as silicon, GaAs, and SiC. Peak velocity values as high as $3 \times 10^7 \text{ cm s}^{-1}$ are found for electrons in GaN. The differences between wurtzite and zincblende semiconductors are found to be insignificant. AlN has a very high critical field in agreement with the high bandgap energy, whereas the critical field of InN is lower than in GaN. The predicted electron peak velocity in InN can be as high as $4 \times 10^7 \text{ cm s}^{-1}$.

Apart from bulk material, MC simulations in 2DEG AlGaIn/GaN channels including hot-phonon and degeneracy effects are provided in [2.380] by a combined MC and Schrödinger–Poisson analysis. The wavefunctions for the confined electrons are calculated. The simulation suggests that the degeneracy in the 2DEG reduces the electron drift velocity, while hot phonons reduce the drift velocity and increase the electron energy relaxation time. The energy relaxation time at RT extract by MC simulation amounts to

Table 2.8. Comparison of the velocity-field characteristics in various bulk materials

Material	n/p	T_L (K)	E_{crit} (kV cm ⁻¹)	v_{peak} (10 ⁷ cm s ⁻¹)	v_{sat} (10 ⁷ cm s ⁻¹)	N_D/N_A (cm ⁻³)	Ref.
GaN (Wz)	n	300	175	2.5	—	2×10^{16}	[2.500]
GaN (Wz)	n	300	150	2.7	2.5	1×10^{16}	[2.37]
GaN (Wz)	n	300	140	2.9	1.8	1×10^{17}	[2.121]
GaN (Wz)	n	77	150	3.2	2.7	1×10^{16}	[2.37]
GaN (Wz)	p	300	—	—	0.48	—	[2.286]
GaN (Zb)	n	300	145	2.6	1.34	1×10^{17}	[2.17]
GaN (Zb)	p	300	—	—	0.92	—	[2.286]
AlN (Wz)	n	300	450	1.7	1.4	1×10^{17}	[2.121, 2.349]
AlN (Wz)	n	300	447	2.3	2.16	1×10^{17}	[2.113]
AlN (Wz)	p	300	—	—	—	—	—
AlN (Zb)	n	300	550	1.8	1.59	1×10^{17}	[2.17]
AlN (Zb)	p	300	—	—	—	—	—
InN (Wz)	n	300	65	4.2	1.8	1×10^{17}	[2.121]
InN (Wz)	n	300	52	3.4	—	1×10^{17}	[2.113]
InN (Zb)	n	300	45	2.9	1.4	1×10^{17}	[2.17]
InN (Zb)	p	300	—	—	—	—	—

Wz wurtzite, Zb zincblende, c cubic

0.3 ps at 10 kV cm⁻¹ [2.380]. Experimental determination of the hot electron energy relaxation time in MBE-grown n-GaN is presented in [2.521]. The extracted value amounts to 0.2 ps at a carrier concentration of 10¹⁸ cm⁻³. Similar field-dependent investigations in AlGaN/GaN heterostructures based on microwave noise are given in [2.281]. RT data yields energy relaxation times of 0.3 ps at 10 kV cm⁻¹ and 1 ps at 2 kV cm⁻¹. The transient electron transport based on MC simulations in wurtzite GaN, InN, and AlN is discussed in [2.121]. In the transient situation very high theoretical overshoot values are observed. However, the paper also depicts the trade-off between transient overshoot and saturated velocity in bulk FET-like transient transport.

Band Structure of GaN

The band structure of GaN has been analyzed in a number of publications, e.g., in [2.108, 2.127, 2.128, 2.238, 2.522]. However, it is not yet fully understood, especially with respect to the higher energy bands. A comprehensive overview of the band parameters of wurtzite and zincblende GaN, AlN, and InN is given in [2.485] in a continuation of the great III-V overview in [2.486]. A consistent set of parameters is presented for both the wurtzite and zincblende binary III-N materials. From an experimental point of view, absorption coefficient,

energy gap, exciton binding energy, and recombination lifetime of Wz-GaN are measured and reported in [2.317]. From these both bandgap, exciton energies, and radiative constants can be derived.

Table 2.9 compiles available mass parameters from band structure calculations and measurements. Various predictions exist for the effective electron mass in GaN, e.g., in [2.128]. The conduction band electron effective mass in wurtzite GaN is measured to be $0.2 m_e$, as reported in [2.91]. The effective mass parameters are further collected from the band structure calculations in [2.127, 2.128, 2.238, 2.486]. The heavy hole masses $m_{p,h}$ are further distinguished along the x - and z -direction. The hole effective mass in p-GaN and the influence of band splitting and band anisotropy on free hole statistics

Table 2.9. Comparison of the effective mass parameters in various III-N semiconductor materials

	m_n (m_e)	$m_n(\Gamma - K)$ (m_e)	$m_n(\Gamma - A)$ (m_e)	$m_n(\Gamma - M)$ (m_e)	Ref.
GaN (Wz)	0.2	0.36	0.27	0.33	[2.91]
AlN (Wz)	0.48	0.42	0.33	0.40	[2.349]
InN (Wz)	0.11 (0.05)	–	–	–	[2.122, 2.486]
	$m_n(\Gamma)$ (m_e)	$m_{n,l}(X)$ (m_e)	$m_{n,t}(X)$ (m_e)	Ref.	
GaN (Zb)	0.15	0.5	0.30	[2.108, 2.485]	
AlN (Zb)	0.25	0.53	0.31	[2.108, 2.485]	
InN (Zb)	0.07–0.11	0.48	0.27	[2.485]	
	$m_{p,h}$ (m_e)	$m_{p,l}$ (m_e)	$m_{p,so}$ (m_e)	Ref.	
GaN (Wz)	1.4	0.3	0.6	[2.108, 2.244]	
AlN (Wz)	3.52 (z)	3.53 (z)	0.25 (z)	[2.108, 2.244]	
AlN (Wz)	10.42 (x)	0.24 (x)	3.81 (x)	[2.108, 2.244]	
InN (Wz)	1.63	0.27	0.65	[2.108, 2.244]	
	$m_{p,h}$ (m_e)	$m_{p,l}$ (m_e)	$m_{p,so}$ (m_e)	Ref.	
GaN (Zb) [100]	0.74	0.21	0.33	[2.108]	
GaN (Zb) [111]	1.82	0.18	0.33	[2.108]	
GaN (Zb) [110]	1.51	0.19	0.33	[2.108]	
AlN (Zb) [100]	1.02	0.35	0.51	[2.108]	
AlN (Zb) [111]	2.85	0.30	0.51	[2.108]	
AlN (Zb) [110]	2.16	0.31	0.51	[2.108]	

Wz wurtzite, Zb zincblende

in wurtzite GaN are discussed in [2.400]. The degeneracy effects are strong and require detailed investigations to obtain the effective hole mass at the particular density-of-states.

Bandgap Energies

The bandgap energy parameters of different crystal structures in III-N materials are compared in Table 2.10. Further, the intervalley separation energies in k-space are of practical importance for the high-field transport of electrons and holes. They are compiled in Table 2.11 for both wurtzite and zincblende structures. The uncertainty of the band structure and energy gap prevails specifically for AlN and InN for the higher bands.

The data of wurtzite GaN and AlN are based on the first principle calculations in [2.441] and the erratum [2.442]. At heterointerfaces between two semiconductors, the energy band discontinuities and bandgap alignments are of high importance, as they determine the energy barriers which the carriers have to surmount. All III-N materials lead to so-called type-I transitions. However, in conventional heterostructures, the alignments are symmetrical with respect to the growth order starting from the substrate. In highly polar semiconductors, such as the III-N material system, this is not necessarily the case, due to the strain effects depending on the substrate (bottom), and the resulting strain and thus polarization charge in the thin top layer. The valence band discontinuities for GaN, AlN, and InN have been compiled, e.g., in [2.275]. The valence band alignment energies are found for the three binary materials, as given in Table 2.12. The additional transitions toward ternary material are also discussed later. BN is not included in this comparison, as the cubic phase BN cannot be grown lattice-matched to the other materials.

Table 2.10. Comparison of the bandgap parameters in various bulk materials at 300 K

(Wz)				Ref.				(Zb)				Ref.			
GaN	E_{g,Γ_1}	(eV)	3.43	[2.121]	$E_{g,\Gamma}$	(eV)	3.38, 3.1, 3.2	[2.108]							
GaN	E_{g,Γ_3}	(eV)	5.29	[2.121]	$E_{g,X}$	(eV)	4.57, 4.7	[2.108]							
GaN	$E_{g,L-M}$	(eV)	5.49	[2.121]	$E_{g,L}$	(eV)	5.64, 6.2	[2.108]							
AlN	E_{g,Γ_1}	(eV)	6.2, 6.12	[2.121, 2.245]	$E_{g,\Gamma}$	(eV)	5.94, 6.0	[2.108]							
AlN	$E_{g,L-M}$	(eV)	6.9	[2.121]	$E_{g,X}$	(eV)	5.1, 4.9	[2.108]							
AlN	$E_{g,G-A}$	(eV)	7.2	[2.121]	$E_{g,L}$	(eV)	9.42, 9.3	[2.108]							
InN	E_{g,Γ_1}	(eV)	0.77	[2.501]	$E_{g,\Gamma}$	(eV)	0.75	[2.486]							
InN	$E_{g,G-A}$	(eV)	4.09	[2.121]	$E_{g,X}$	(eV)	2.486	[2.486]							
InN	E_{g,Γ_3}	(eV)	4.49	[2.121]	$E_{g,L}$	(eV)	5.79	[2.486]							

Wz wurtzite, Zb zincblende

Table 2.11. Comparison of the intervalley separation energies in various bulk materials at 300 K

	(Wz)	Ref.		(Zb)	Ref.
GaN –	(eV) –	–	Γ	(eV) –	–
GaN $\Gamma - 3$	(eV) 1.9	[2.121]	$\Gamma - X$	(eV) 1.4	[2.17, 2.244]
GaN $L - M$	(eV) 2.1	[2.121]	$\Gamma - L$	(eV) 1.6–1.9	[2.244]
AlN Γ	(eV) –	–	–	(eV) –	–
AlN $\Gamma - (L - M)$	(eV) 0.7	[2.121, 2.441]	–	(eV) –	–
AlN $\Gamma - K$	(eV) 1.0	[2.121, 2.441]	–	(eV) –	–
InN –	(eV) –	–		(eV) –	–
InN $\Gamma - (M - L)$	(eV) 2.9–3.9	[2.244]		(eV) –	–
InN $\Gamma - A$	(eV) 0.7–2.7	[2.244]		(eV) –	–

Wz wurtzite, Zb zinblende

Table 2.12. Comparison of the bandgap alignment parameters in various bulk materials at 300 K

	Bottom	GaN	AlN	InN	Ref.
Top	(eV)	(Wz)	(Wz)	(Wz)	
GaN	(Wz)	0	0.7	1.05	[2.275]
AlN	(Wz)	0.7	0	1.81	[2.275]
InN	(Wz)	1.05	1.81	0	[2.275]
	Bottom	GaN	AlN	InN	Ref.
Top	(eV)	(Zb)	(Zb)	(Zb)	
GaN	(Zb)	0	0.85	0.51	[2.324]
AlN	(Zb)	0.85	0	1.09	[2.324]
InN	(Zb)	0.51	1.09	0	[2.324]

Wz wurtzite, Zb zinblende

Further empirical pseudopotential calculations of wurtzite GaN and InN are given in [2.522]. For the complete band structure, a nonlocal pseudopotential calculation of the III-nitride wurtzite phase materials system is performed in [2.128] for binary compounds such as GaN, AlN, and InN. Band structure calculations of wurtzite-type GaN and AlN are given in [2.298, 2.441]. Particularly the complicated valence band structure and the effective mass parameters of the wurtzite nitrides are obtained. The cubic approximation is found to be fairly successful in the analysis for the valence-band structures of the wurtzite-type nitrides.

Table 2.13. Comparison of the direct recombination parameters in various bulk materials at 300 K

	GaN (Wz)		AlN (Wz)		InN (Wz)	
B ($\text{cm}^3 \text{s}^{-1}$)	1.1×10^{-8}	[2.317]	0.4×10^{-10}	[2.489]	2×10^{-10}	[2.533]
<i>Wz</i> wurtzite						

The band structure in zincblende GaN, AlN, and AlGa_xN is described in [2.108]. Particularly, the energies of Γ , X , and L valley of Al_xGa_{1-x}N as a function of mole fraction x of are calculated.

Table 2.13 gives the direct recombination parameters of the III-N semiconductors for the direct band structure. As can be derived, the direct recombination in GaN is very strong and about an order of magnitude higher than, e.g., in GaAs.

Aluminum Nitride (AlN)

Second to GaN, AlN is the most important binary material in the III-N material family for electronic applications and is mostly used as its ternary compound Al_xGa_{1-x}N, e.g., in barriers heterostructures. It is characterized to be an insulator due to the high-bandgap energy and the high-activation energy of donors. Binary AlN is usually grown nucleation layer to start the growth on s.i. SiC or sapphire substrates, e.g., [2.96] and as an interlayer at the channel/barrier interface, e.g., [2.66].

Mechanical and Optical Properties

Basic properties such as the crystal structure, mechanical properties, and thermal properties of AlN are compiled in [2.287]. The mass density of AlN is much smaller than in GaN or InN, as given in Table 2.1. As depicted in Tables 2.2 and 2.3, thermal expansion and Vickers hardness of AlN are relatively similar to those of GaN. Elastic constants of AlN are given for the wurtzite phase in Table 2.3 and for the zincblende phase in Table 2.4.

The intrinsic thermal conductivity of AlN is determined in [2.428]. Its high-thermal conductivity is better than that of any other semiconductor apart from BN, SiC, and diamond, as is compiled in Table 2.16. This makes AlN a potentially attractive substrate material. The optical functions, such as the refractive index n , of AlN are given in [2.287]. The optical functions are also compiled in [2.260], including the dielectric functions and the absorption functions.

Basic Carrier Transport Properties

Although not of primary importance to most devices except in very thin layers close to the channel, transport in AlN is relatively well investigated

by MC simulations, also with respect to the understanding of the transport in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ for various material compositions x . An early compilation of the transport data of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and AlN is given in [2.123], yielding the low mobility of wurtzite AlN for both n- and p-type material, as given in Table 2.8. The low-field electron mobility of AlN is calculated to be $135\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at room temperature and at a doping concentration of 10^{17} cm^{-3} .

High-Field Transport

The electron high-field transport in wurtzite AlN is investigated by MC simulations in [2.349]. Further MC simulations on the transient transport in AlN are given in [2.121]. The characteristics are determined by the relatively high-effective electron mass of $0.48 m_e$, the large bandgap of $\approx 6.2\text{ eV}$, and the very small intervalley separation. The resulting velocity-field characteristic yields a very high critical field of 450 kV cm^{-1} [2.349], as shown in Table 2.7. The saturation velocity in AlN reaches $1.4 \times 10^7\text{ cm s}^{-1}$ at room temperature, while the peak velocity in the bulk is calculated to be $1.7 \times 10^7\text{ cm s}^{-1}$ at a doping concentration of $1 \times 10^{17}\text{ cm}^{-3}$.

Band Structure of AlN

The high-bandgap energy of AlN of 6.2 eV at room temperature allows the bandgap in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ to be modified in a broad range from the value of GaN to that of AlN . With the bandgap of InN found to be even smaller than that of GaN , an even wider range is available for the material $\text{In}_x\text{Al}_{1-x}\text{N}$. Early calculations of the band structure of wurtzite and zincblende AlN are collected in [2.236]. The band structure of wurtzite AlN is calculated in [2.128]. Electronic band structure properties of zincblende AlN are further calculated by the empirical pseudopotential method in [2.108]. From these calculations, effective electron and hole mass parameters can be obtained, as compiled in Table 2.9. The direct recombination parameter is depicted in Table 2.13, taken from [2.489] and used for the development of light-emitting diodes with very high bandgap and resulting photon energy.

Indium Nitride (InN)

InN and its compounds $\text{In}_x\text{Ga}_{1-x}\text{N}$ and $\text{In}_x\text{Al}_{1-x}\text{N}$ so far are not yet widely used in electronic devices [2.230]. When used, both InAlN/GaN [2.143] as well as AlGaIn/InGaIn [2.425] heterostructures have been reported. The indium contents are low, e.g., in [2.85, 2.150], to achieve the lattice match to GaIn buffer layers. The MOCVD growth of InN is complicated caused by the high-growth temperature and resulting defect background concentrations and the high amount of residual nitrogen vacancies due to the higher growth temperatures required relative to MBE growth, as described in Chapter 3. The MBE growth of InN is under development and allows improved material quality and thus the use of the full range of material composition in the

material $\text{In}_x\text{Ga}_{1-x}\text{N}$. High-quality InN has been recently grown by MBE, e.g., [2.114,2.501]. A full review of the epitaxial growth is given in [2.38]. A bulk electron mobility of $3,570 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K is obtained. The mobility at 150 K is as high as $5,100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. P-type InN has been recently reported in [2.170], which is essential for the realization of bipolar or optoelectronic pn-devices.

Mechanical and Optical Properties

An initial compilation of mechanical, optical, and thermal properties of InN is given in [2.449,2.451]. Mechanical data are compiled in Tables 2.1 and 2.2; however, the data are relatively uncertain, due to the lack of real bulk InN material [2.449]. Elastic constants of InN are given in Table 2.3. The thermal expansion coefficients CTE in both wurtzite and zincblende structures are compiled in Table 2.5. The CTE and the lattice constants suggest the growth on sapphire substrates [2.54]. The thermal conductivity and the heat capacity of InN are still primarily based on estimates and extrapolations, as explained in [2.449], see also Table 2.16. The optical functions of InN are compiled in [2.299]. Due to the new research on samples with improved material quality, the bandgap and optical functions of InN are reconsidered, e.g., in [2.278, 2.279,2.425]. This fact also had a drastic impact on the calculation of transport properties and the higher band, which have not yet been fully repeated based on the new band structure.

Basic Carrier Transport Properties

An early compilation of the transport properties in InN is given in [2.54,2.453]. The early data are characterized by high background concentrations of 10^{19} – 10^{20} cm^{-3} and associated low mobilities. An early evaluation of the InN mobility as a function of temperature and compensation ratio using variational principle calculations is given in [2.64]. In theory, very high mobility values of $4,400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are calculated, which, however, have not been fully reached experimentally. An electron mobility of $1,200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a sheet carrier concentration of $1.2 \times 10^{14} \text{ cm}^{-2}$ have been obtained experimentally at the InN/AlN interface, as reported in [2.307]. Polarization engineering of n-InAlN/GaN HFETs and the effect on DC- and RF-performance are described in [2.186,2.187]. The use of $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ is critical, as the polarization-induced charge (PIC) is a much stronger function of the material composition x than in the AlGaIn/GaN material system, as explained later. P-channel $\text{In}_x\text{Ga}_{1-x}\text{N}$ HFETs based on polarization doping are demonstrated in [2.450]. Hall measurements indicate a 2D-hole gas (2DHG) mobility of approximately $700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at a low temperature $T_L = 66 \text{ K}$.

High-Field Transport

Mostly, the simulated results on transport in InN are still based on the assumption of a direct bandgap of InN of 1.89 eV and an associated band structure.

This was recently corrected to the much smaller bandgap value of ≈ 0.77 eV at room temperature [2.501]. Most of the initial MC simulations thus have to be taken with a grain of salt. Electron transport in wurtzite-InN is calculated by Leary in [2.348]. Further ensemble MC calculations on the wurtzite material by Bellotti et al. are given in [2.35]. The intervalley separation energies are given in Table 2.11. As depicted in Table 2.8, the velocity-field characteristics yield a maximum carrier velocity of up to 4.2×10^7 cm s $^{-1}$ at a critical field of about 52–65 kV cm $^{-1}$ in the homogenous bulk case [2.113, 2.121]. These properties are promising, however, compared to GaAs or InGaAs material they are not really surprising when considering the low effective mass, the low bandgap, and maximum electron velocity. Transient-transport calculations in InN given in [2.121] report velocity overshoot values above 10^8 cm s $^{-1}$. Quite outstanding theoretical HFET cut-off frequencies are derived from these simulations as upper bounds for a theoretical pure InN-channel-FET performance.

Band Structure

The data for the band structure of InN are taken, e.g., from the band structure calculations in [2.128], which do not yet account for the recent modification of InN bandgap energy. More experimental data on the electronic structure of MBE-grown InN are provided in [2.307]. The effective electron mass of InN has been found to be $0.11 m_e$ [2.486], as compiled in Table 2.9. This effective mass value has to be considered high relative to the bandgap of 0.77 eV, when we compare it to other semiconductors, such as InAs or InP. Initial values of the optical bandgap of InN were reported by Tansley in [2.450]. This leads to a value of 1.89 eV at room temperature. More recent reports on the optical properties of InN, resolving the discrepancies of several publications at different growth and doping conditions, are given in [2.278, 2.279]. The bandgap of InN is found to be 0.77 eV at room temperature [2.425], as given in Table 2.10. The difference is explained by the existence of oxy-nitrides, which have a much larger bandgap. This low bandgap means a really conventional electronic III-V material, e.g., with respect to the expected breakdown of devices. Optically it means that a very broad range of wave lengths is available in the III-N systems from deep ultraviolet to red. The intervalley separation energies of both wurtzite are compiled in Table 2.11, based on the bandgap of 1.89 eV. Currently, there is little information on the intervalley energies of Zb-InN.

Boron Nitride (BN)

Boron nitride can be found in several crystallographic forms. The most important insulating or semiconducting form of BN is cubic material, which is metastable under normal conditions [2.53, 2.99, 2.253]. Ceramic BN is widely used for industrial tools as abrasive. The great advantage of cubic-BN is its Vickers hardness [2.253] and its good thermal conductivity, as compiled in Table 2.16. Even ultraviolet pn-diodes can be formed from c-BN, as given

in [2.300]. Despite the material growth problems, ultraviolet LED can be formed [2.491], which operate up to very high temperatures of 530°C [2.300].

Mechanical and Optical Properties

The mass density of cubic c-BN is given in [2.99], as compiled in Table 2.1. The outstanding Vickers hardness of BN can be observed in Table 2.2 [2.99]. Elastic constants of cubic BN are compiled in Table 2.3. The thermal expansion for cubic BN is given in Table 2.5. The values for the cubic phase are very similar to those of Zb-GaN. Thermal conductivity measurements and heat capacity measurements of cubic BN will be given in Table 2.16. The thermal conductivity of BN amounts to values of up to $750 \text{ W m}^{-1}\text{K}^{-1}$, which is higher than in any other semiconductor. The theoretical limit found is as high as $1,300 \text{ W m}^{-1}\text{K}^{-1}$.

Basic Carrier Transport Properties

Basic mobility evaluation of cubic BN as a function of carrier concentration have been provided, e.g., in [2.253]. Cubic BN is typically p-doped [2.135]. A Hall mobility of $500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is found at a carrier concentration of $5 \times 10^{18} \text{ cm}^{-3}$ [2.253]. For n-type material, only few experimental data exist, e.g., [2.300, 2.496]. As c-BN is an insulator [2.496], the transport is characterized by high-activation energies of the carriers of $\geq 0.2 \text{ eV}$.

High-Field Transport

Band structure calculations are given in [2.71] with the result that cubic BN is an insulator with a bandgap of 7.1 eV. Thus, no MC transport calculations are available for c-BN.

Dielectric Breakdown Fields

Table 2.14 compiles measured dielectric electric breakdown fields for various III-N bulk materials. The dielectric breakdown field of GaN is reported to be about 3 MV cm^{-1} . AlN has a much higher breakdown field due to the higher bandgap, which can be even higher than the value given in Table 2.14 [2.388]. The dielectric breakdown field of InN is not well investigated. The latter is due to the high trap concentrations N_T and the new findings for the fundamental bandgap. The breakdown fields of bulk c-BN reported in [2.53] vary from 2 to 6 MV cm^{-1} .

Table 2.14. Comparison of the bulk breakdown fields in various bulk materials at 300 K

	GaN	Ref.	AlN	Ref.	InN	Ref.	BN	Ref.
	(Wz)		(Wz)		(Wz)		(c)	
E_{break} (MV cm^{-1})	3.3	[2.61]	8.4	[2.388]	1.2	[2.244]	2–6	[2.253]
Wz wurtzite, c cubic								

Band Structure of BN

Band structure calculations of cubic BN are available [2.496]. Similar calculations, but not of cubic phase BN, are provided in [2.237]. The bandgap of cubic BN is found to be similar to AlN and reported to be $E_g \approx 6.4$ eV at RT in [2.253]. Further calculations of cubic BN in pseudopotential local density formalism are provided in [2.497]. The calculated charge density of the BN is very similar to other III-V semiconductors. A defect analysis of Be, Mg, and Si in cubic BN is reported in [2.135, 2.448]. The substitution of B by Mg or Be typically leads to the p-type behavior of the grown material.

2.1.2 Material Limitations

The transport properties of III-N materials and the limitations of these materials have been discussed above. Further issues are discussed in the next paragraphs.

Recombination, Generation, and Breakdown

Recombination and generation are of fundamental importance for optoelectronic and bipolar electronic devices. However, due to the influence of electron trapping in FETs, these effects also critically determine their device performance. For high-field effects at increased driving forces, an experimental evaluation of impact ionization in GaN is discussed in [2.229]. The impact ionization parameters are extracted from a AlGaIn/GaN HFET device with a gate length of $0.9 \mu\text{m}$. For the high-field region of $\geq 10^6 \text{ V cm}^{-1}$ the data can be fitted to the classical relation:

$$\alpha_n = A \cdot \exp(-K/E), \quad (2.1)$$

$$\alpha_n = 2.9 \times 10^8 \exp(-3.4 \times 10^7/E). \quad (2.2)$$

For lower fields, this expression needs to be modified, as the field dependence is weaker due to the weakness of real carrier multiplication. The relations in (2.1)/(2.2) suggest that the critical field is a factor of 8 higher when compared to GaAs-data taken from a similar extraction procedure. MC simulations of electron impact ionization in both zincblende and wurtzite GaN are provided in [2.212]. At comparable fields, the electrons are cooler in the wurtzite structure, thus the ionization rates are lower than in the zincblende phase. A similar study on the electron initiated impact ionization in Zb-GaN can be found in [2.340]. The simulations suggest a very soft breakdown threshold similar to the device findings in [2.229]. MC simulations of hole-initiated impact ionization in both GaN-phases are discussed in [2.339]. The critical field for the hole-initiated II in Zb-GaN are found to be similar to those for the electron-initiated II and amount to 3 MV cm^{-1} . For the wurtzite structure, the breakdown is similar for high-electric fields, while for lower field, the hole II-rate appears to be greater. Electron-initiated impact ionization

Table 2.15. Breakdown fields, bandgap energies, and dielectric constants for various semiconductor materials

Material	Breakdown field (MV cm ⁻¹)	E_g (eV)	ϵ_r (-)	Ref.
Si	0.3	1.12	11.9	[2.463]
GaAs	0.4	1.43	12.5	[2.463]
InP	0.45	1.34	12.4	[2.463]
GaN (Wz)	3.3	3.43	9.5	[2.463]
AlN (Wz)	8.4	6.2	8.5	[2.388, 2.463]
InN (Wz)	1.2	0.7	15.3	[2.244, 2.451]
BN (c)	2–6	6.4	7.1	[2.253]
4H-SiC	3.5	3.2	10	[2.463]
6H-SiC	3.8	2.86	10	[2.463]
Diamond	5	5.6	5.5	[2.463]

in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is evaluated by ensemble MC simulation in [2.56] for the full material composition range. The results obey the simple expression, as given in (2.1). As expected, the critical fields increase with the increase in the material composition and bandgap. Very low impact ionization rates are observed for $\text{Al}_x\text{Ga}_{1-x}\text{N}$ in general. A study of RF-breakdown in bulk GaN and GaN MES-FETs is given in [2.112]. It is found that the RF-breakdown voltage increases with the frequency of the applied RF-large-signal excitation. The difference is explained by the time-response of the particle energy. The critical field for impact ionization at AlGaN/GaN HFETs is found to be around 3 MV cm^{-1} at room temperature, as reported in [2.95]. This agrees well with the breakdown field in bulk GaN. Breakdown fields and related material properties are again compiled for comparison in Table 2.15 for various homogeneous materials. Generally, the increase of the breakdown fields with increasing bandgap is observed. The wide bandgap materials have breakdown fields, which are an order of magnitude higher than those of conventional semiconductors. The substrate material SiC and diamond have breakdown fields similar to III-N semiconductors.

2.1.3 Thermal Properties and Limitations

In addition to their electrical limits III-N semiconductor devices are subject to strong thermal (self-)heating. Table 2.16 compiles the thermal properties of several binary semiconductor materials. The temperature dependence of the thermal conductivity is modelled according to:

$$\kappa_L(T_L) = \kappa_{300 \text{ K}} \cdot \left(\frac{T_L}{300 \text{ K}} \right)^\alpha, \quad (2.3)$$

as also stated in Chapter 8.

Table 2.16. Thermal properties of III-nitride binary and ternary materials at 300 K

	κ_{300} (W K ⁻¹ m ⁻¹)	α (-)	c_{300} (J K ⁻¹ kg ⁻¹)	Ref.
Si	148	-1.35	711	[2.406]
GaAs	54	-1.25	322	[2.356]
InP	68	-1.4	410	[2.356]
GaN (Wz)	130	-0.43	491	[2.120, 2.423]
AlN (Wz)	285	-1.57	748	[2.428]
InN (Wz)	38.5, 45, 80, 176	-	325	[2.223, 2.428, 2.449]
BN (c)	749	-	600	[2.99]
6H-SiC	390	-1.5	715	[2.57]
6H-SiC	490	-	690	[2.244, 2.331]
4H-SiC	330	-	690	[2.244, 2.416]
V-doped SiC	370	-	690	-
Sapphire	42	-	750	-
Diamond	2,000–2,500	-1.85	520	[2.405]

Thermal Conductivity and Heat Capacity

Silicon serves as a reference. The thermal conductivity of silicon is not reached by GaAs. On the contrary, GaN has a thermal conductivity similar to silicon. The thermal conductivity at 300 K κ_{300} of AlN is better than the κ_{300} of GaN, while InN has a very low value [2.223]. BN has the best value of all III-N materials. Initial determination of thermal properties of GaN is given in [2.423]. Further thermal data is compiled in [2.4]. The intrinsic thermal conductivity for AlN is determined in [2.428]. The thermal conductivity of GaN is often quoted dating back to the work of Sichel [2.423]. However, several investigations are available which especially focus on the effects of dislocations on the thermal conductivity. A good overview of the data are presented and the methods of measurements are compiled in [2.120]. The effect of dislocations on the thermal conductivity in GaN is investigated experimentally in [2.264]. The measurements show a dramatic increase of the thermal conductivity at reduced dislocation density of 10^8 cm^{-2} , especially at temperatures below 200 K. The theoretical predictions in [2.216] support a maximum value for the thermal conductivity in GaN of nearly $200 \text{ W K}^{-1} \text{ m}^{-1}$. The experimental data for the thermal conductivity of InN ($\leq 45 \text{ W K}^{-1} \text{ m}^{-1}$) is much lower than the theoretical predictions of $176 \text{ W K}^{-1} \text{ m}^{-1}$ [2.223].

The data for the heat capacity are also compiled in Table 2.16. The heat capacity is given for constant pressure. For SiC, the measured value of the polytype 6H-SiC is used for SiC in general [2.356]. The heat capacity of the binary semiconductors is lower than of the substrate material. More analysis with respect to the packaging materials and to the dynamic response is provided in Chapter 8.

2.1.4 Ternary and Quaternary III-N Materials

The existence of ternary and even quaternary materials in the III-N system is a fundamental advantage relative to other wide bandgap semiconductor materials, such as SiC. The possibility of growing $\text{Al}_x\text{Ga}_{1-x}\text{N}$, $\text{In}_x\text{Ga}_{1-x}\text{N}$, and $\text{In}_x\text{Al}_{1-x}\text{N}$ in heterostructures with the III-N binaries allows bandgap engineering. This has tremendous impact on the electronic and optoelectronic application of the materials. The material parameters of the quantity P are combined by quadratic interpolation in the following two approaches:

$$P_{\text{Al}_x\text{B}_{1-x}\text{N}} = P_{\text{A}} \cdot x + P_{\text{B}} \cdot (1 - x) + C_{\text{P,AB}} \cdot x \cdot (1 - x). \quad (2.4)$$

In the second approach, (2.4) can be written in another way, i.e.:

$$P_{\text{Al}_x\text{B}_{1-x}\text{N}} = a + b \cdot x + c \cdot x^2 \quad (2.5)$$

resulting in different coefficients, which can be directly correlated with the binary materials. Sometimes (2.5) is extended to a third-order polynomial:

$$P_{\text{Al}_x\text{B}_{1-x}\text{N}} = a + b \cdot x + c \cdot x^2 + d \cdot x^3. \quad (2.6)$$

All relevant quantities will be analyzed in the following sections using the aforementioned formulae in quadratic interpolation. If necessary, cubic or other interpolation schemes will be mentioned.

Aluminum Gallium Nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$)

$\text{Al}_x\text{Ga}_{1-x}\text{N}$ is the most important ternary compound, as the lattice-mismatch relative to GaN can be effectively controlled for nearly all material compositions. A distinction may be required for wurtzite and zincblende AlGa_N materials, as the zincblende material has a transition from a direct to an indirect semiconductor [2.235].

Mechanical and Optical Properties

For mass density, Vickers hardness, and dielectric constants, typically no bowing is applied, and the values can be interpolated linearly with high precision between the binary values of GaN and AlN. The heat capacity of the ternaries is interpolated linearly as given in (2.7):

$$c_{\text{L,AB}} = (1 - x) \cdot c_{\text{L,A}} + x \cdot c_{\text{L,B}}. \quad (2.7)$$

The thermal conductivity of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is interpolated as the following equation (2.8), taken from [2.357]. Data for the thermal conductivity of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is given in [2.255]. The derived parameters are given in Table 2.17.

$$\kappa_{\text{AB}} = \left(\frac{(1 - x)}{\kappa_{\text{A}}} + \frac{x}{\kappa_{\text{B}}} + \frac{x \cdot (1 - x)}{C_{\kappa,\text{AB}}} \right)^{-1}. \quad (2.8)$$

Table 2.17. Interpolation of the thermal conductivity κ in III-N ternary materials

	$C_{\kappa,AB}$ (W m ⁻¹ K ⁻¹)	Ref.
Al _x Ga _{1-x} N	6.95	[2.255]
In _x Ga _{1-x} N	1.4	[2.356]
In _x Al _{1-x} N	3.3	[2.356]

Similarly, the temperature dependence α_{AB} is interpolated linearly.

$$\alpha_{AB} = (1 - x) \cdot \alpha_A + x \cdot \alpha_B. \quad (2.9)$$

The strong material composition dependence of the thermal conductivity is found for all ternary III-V semiconductors [2.356]. A thermal conductivity of 25 W m⁻¹K⁻¹ is found for Al_{0.4}Ga_{0.6}N [2.255].

Basic Carrier Transport Properties

An evaluation of temperature-dependent transport properties in zincblende Al_xGa_{1-x}N and In_xGa_{1-x}N semiconductors using MC simulations is given in [2.17]. The data for (2.6) are compiled in Table 2.18. The table further gives the interpolation of the low-field mobility according to the harmonic mean:

$$\frac{1}{\mu_{AB}} = \frac{x}{\mu_A} + \frac{1-x}{\mu_B} + \frac{x \cdot (1-x)}{C_{\mu,AB}}. \quad (2.10)$$

The database for the mobility of In_xAl_{1-x}N and In_xGa_{1-x}N is still relatively poor. However, initial values are provided based on the investigations in [2.65]. The alloy-scattering potential is found to be important for the bowing of the drift mobility of both In_xGa_{1-x}N and In_xAl_{1-x}N, both for room temperature and at 77 K [2.65]. The alloy scattering is considered relatively less important for Al_xGa_{1-x}N in [2.65]. However, the value extracted for the mobility of Al_xGa_{1-x}N in [2.113] show also a strong dependence on the material composition. This is confirmed by the numerical study of the alloy scattering in AlGa_{0.4}N and InGa_{0.4}N [2.34].

The values for the bowing of the drift mobility are given in Table 2.18.

High-Field Transport

Table 2.19 compiles values for the bowing of the saturation velocity, which is calculated both according to the polynomial approach of (2.6) and according to quadratic bowing, as given in (2.14).

As can be found in [2.17], the critical field and the peak velocities typically do not vary linearly as a function of material composition for Al_xGa_{1-x}N or In_xGa_{1-x}N between the binary constituents. Again a polynomial approach is used, as given in Table 2.19. In another approach, quadratic bowing can be applied:

$$v_{\text{sat},AB} = (1-x) \cdot v_{\text{sat},A} + x \cdot v_{\text{sat},B} + x \cdot (1-x) \cdot C_{v_{\text{sat}},AB}, \quad (2.11)$$

$$v_{\text{peak},AB} = (1-x) \cdot v_{\text{peak},A} + x \cdot v_{\text{peak},B} + x \cdot (1-x) \cdot C_{v_{\text{peak}},AB}, \quad (2.12)$$

$$E_{\text{crit},AB} = (1-x) \cdot E_{\text{crit},A} + x \cdot E_{\text{crit},B} + x \cdot (1-x) \cdot C_{E_{\text{crit}},AB}. \quad (2.13)$$

Table 2.18. Interpolation of the mobility μ in III-N ternary compounds for different models at RT

$\mu(x)$	a ($\text{cm}^2 (\text{Vs})^{-1}$)	b ($\text{cm}^2 (\text{Vs})^{-1}$)	c ($\text{cm}^2 (\text{Vs})^{-1}$)	d ($\text{cm}^2 (\text{Vs})^{-1}$)	N_D (cm^{-3})	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$ (Zb)	1,157	-1,329	-283	671	10^{17}	[2.17]
$\text{In}_x\text{Ga}_{1-x}\text{N}$ (Zb)	465	755	-61	676	10^{17}	[2.17]

$\mu(x)$	$C_{\mu,n,AB}$ ($\text{cm}^2 (\text{Vs})^{-1}$)	$C_{\mu,p,AB}$ ($\text{cm}^2 (\text{Vs})^{-1}$)	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$ (Wz)	40	1e6	[2.113, 2.356]
$\text{In}_x\text{Ga}_{1-x}\text{N}$ (Wz)	97	1e6	[2.65]
$\text{In}_x\text{Al}_{1-x}\text{N}$ (Wz)	1e6	1e6	[2.65, 2.452]

Wz wurtzite, Zb zincblende

Table 2.19. Interpolation of the saturation velocity v_{sat} , the peak velocity v_{peak} , and E_{crit} in III-N ternary compounds

v_{sat}	a (10^7 cm s^{-1})	b (10^7 cm s^{-1})	c (10^7 cm s^{-1})	N_D (cm^{-3})	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	1.3425	0.574	-0.3215	10^{17}	[2.17]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	1.3286	0.3657	-0.2857	10^{17}	[2.17]

	$C_{v_{\text{sat}},AB}$ (10^7 cm s^{-1})	$C_{v_{\text{peak}},AB}$ (10^7 cm s^{-1})	$C_{E_{\text{crit}},AB}$ (kV cm^{-1})	N_D (cm^{-3})	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	-3.85	-0.1	50	10^{17}	[2.17, 2.356]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	0.35	-1	-25	10^{17}	[2.17]
$\text{In}_x\text{Al}_{1-x}\text{N}$	-	-	-	-	-

	E_{crit} (kV cm^{-1})	N_D (cm^{-3})	Ref.
GaN (Wz)	225	2×10^{16}	[2.211, 2.500]
GaN (Wz)	140	10^{17}	[2.121]
AlN (Wz)	450	10^{17}	[2.121]
InN (Wz)	65	10^{17}	[2.121]
GaN (Zb)	150	10^{17}	[2.17]
AlN (Zb)	550	10^{17}	[2.17]
InN (Zb)	45	10^{17}	[2.17]

The parameters are also given in Table 2.19. The values of the velocities of the binaries are given in Table 2.8, while the critical fields E_{crit} are repeated in Table 2.19 from Table 2.8.

Band Structure

Band structure properties of ternary $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloys are given in [2.127, 2.235]. The bowing of the effective masses m_ν and the bandgap E_g are described by quadratic interpolation:

$$m_{\nu,\text{AB}} = (1-x) \cdot m_{\nu,\text{A}} + x \cdot m_{\nu,\text{B}} + x \cdot (1-x) \cdot C_{m_\nu,\text{AB}}, \quad (2.14)$$

$$E_{g,\text{AB}} = (1-x) \cdot E_{g,\text{A}} + x \cdot E_{g,\text{B}} + x \cdot (1-x) \cdot C_{E_g,\text{AB}}. \quad (2.15)$$

For $\text{Al}_x\text{Ga}_{1-x}\text{N}$, the dependence of the fundamental bandgap on alloy material composition and on pressure are discussed in [2.410]. A relatively strong bowing is observed for $\text{Al}_x\text{Ga}_{1-x}\text{N}$. The bowing parameters are compiled in Table 2.21. Further information on the dependence of the bandgap on the material composition of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ for $(0 \leq x \leq 1)$ based on ultraviolet photodetectors grown on sapphire are given in [2.489]. The parameters for the bowing of the masses and bandgap are given in Table 2.20 and Table 2.21. As can be seen the bowing is mostly neglected. Band structure nonlocal pseudopotential calculations of the III-N wurtzite phase materials of the ternary alloys $\text{Al}_x\text{Ga}_{1-x}\text{N}$, $\text{In}_x\text{Ga}_{1-x}\text{N}$, and $\text{In}_x\text{Al}_{1-x}\text{N}$ are given in [2.127]. The data include a systematic collection of the effective mass bowing parameters at the relevant conduction band minima. The interpolation of the bandgap energies is given in Table 2.21. The recent changes for InN are included. Distinctions of the bowing are necessary in the zincblende structure, as direct-indirect transitions occur for $\text{In}_x\text{Al}_{1-x}\text{N}$ and $\text{Al}_x\text{Ga}_{1-x}\text{N}$. For $\text{Al}_x\text{Ga}_{1-x}\text{N}$, this occurs at $x = 0.69$ [2.254], while for $\text{In}_x\text{Al}_{1-x}\text{N}$, this occurs for $x = 0.187$ [2.256].

Table 2.20. Interpolation of the effective masses in III-N ternary materials

	$C_{m_n,\text{AB}}$ (Wz)	$C_{m_p,\text{AB}}$ (Wz)	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	0.0048	0	[2.127, 2.485]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	0	0	[2.485]
$\text{In}_x\text{Al}_{1-x}\text{N}$	0	0	[2.485]
<i>Wz</i> wurtzite, <i>Zb</i> zincblende			

Table 2.21. Interpolation of the bandgap energy in III-N ternary materials

	$C_{E_{\text{gap}},\text{AB}}$ (Wz)	$C_{E_{\text{gap}},\text{AB}}$ (Zb)	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	-0.7, -1.33	Γ :-0.7, X :-0.61	[2.410, 2.485]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	-1.4	-1.4	[2.279, 2.485]
$\text{In}_x\text{Al}_{1-x}\text{N}$	-2.5	Γ :-2.5, X :-0.61	[2.485]

Indium Gallium Nitride ($\text{In}_x\text{Ga}_{1-x}\text{N}$) and Indium Aluminum Nitride ($\text{In}_x\text{Al}_{1-x}\text{N}$)

The importance of InN and its ternary compounds is due to the smaller bandgap relative to GaN, allowing for a broader variety of layers for bandgap engineering also into the visible optical range for optoelectronic devices. High-quality $\text{In}_x\text{Ga}_{1-x}\text{N}$ layers were recently grown by MBE, e.g., in [2.114, 2.501], mostly on sapphire substrates. $\text{In}_x\text{Al}_{1-x}\text{N}$ is lattice-matched to GaN for $x = 0.17$, which has recently drawn attention to this material for HEMT device applications [2.230, 2.485].

Mechanical and Optical Properties

Initial layer preparation and optical properties of $\text{Ga}_{1-x}\text{In}_x\text{N}$ thin films are demonstrated and compiled in [2.352]. The initial material is mostly polycrystalline. The thermal conductivity and the heat capacity of $\text{In}_x\text{Ga}_{1-x}\text{N}$ are interpolated from the binaries, as shown in (2.7) and (2.8) with parameters from Table 2.16 and Table 2.17.

Basic Carrier Transport Properties

Similar to InGaAs and InAlAs, initial expectations for InN and its compounds yield lower effective mass than GaN [2.128]. However, good quality films, especially for high In-contents, have not been realized with MOCVD growth, e.g., [2.181]. MBE growth has allowed InN to be grown with improved material quality, e.g., [2.86]. An initial compilation of the transport properties in $\text{In}_x\text{Ga}_{1-x}\text{N}$ is given in [2.54, 2.453] and in the references therein.

High-Field Transport

MC analysis of the wurtzite $\text{In}_x\text{Ga}_{1-x}\text{N}$ is given in [2.113]. The analysis is based on the wrong bandgap of InN. The analysis of peak velocities and mobility of the ternary material is strongly dependent on the alloy scattering in the resulting ternary material [2.34]. The parameters for the peak velocity v_{peak} , the saturation velocity v_{sat} , and the critical field E_{crit} are compiled in Table 2.19. MC simulations of the temperature-dependent transport properties of zincblende $\text{In}_x\text{Ga}_{1-x}\text{N}$ are given in [2.17] and are also compiled in Table 2.19. The critical field E_{crit} decreases strongly with the indium content. Similarly the saturation velocity of $\text{In}_x\text{Ga}_{1-x}\text{N}$ increases from GaN to InN. Very few data are available on the transport properties of $\text{In}_x\text{Al}_{1-x}\text{N}$. Al-rich $\text{In}_x\text{Al}_{1-x}\text{N}$ will certainly reveal insulating properties similar to AlN. $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ is the most important composition to understand. Calculations and initial data on the low-field mobility can be found in [2.452]. The prediction yields a low-field mobility of $\leq 200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x \leq 0.5$. High-field transport in InAlN is so far not understood very well.

Band Structure

For the band structure, nonlocal pseudopotential calculations of $\text{In}_x\text{Ga}_{1-x}\text{N}$ and $\text{In}_x\text{Al}_{1-x}\text{N}$ are given in [2.127] and are still based on a fundamental bandgap of 1.89 eV. The conduction band offset of InGaN/GaN is reported in [2.530]. The ratio of conduction to valence band offset is 58:42. With the improvements in material quality based on MBE growth, small bandgap bowing has been reported, e.g., in [2.501]. The bandgap bowing has been thoroughly investigated with respect to both bowing of InGaN and the bandgap value of InN in [2.86, 2.278]. InN is found to be a small bandgap semiconductor with a bandgap energy of 0.77 eV at RT [2.86]. The data are extracted from optical absorption, photoluminescence, and photomodulated reflectance. The higher bands are still under consideration, e.g., [2.163, 2.373, 2.523].

2.2 Polar Semiconductors for Electronics

Next to the basic knowledge on the bulk material properties, further substantial material analysis is required. III-N semiconductors provide the occurrence of significant electrical polarization effects that dominate especially the interfaces [2.499]. This fact deserves discussion in an extra section, since the effects are much stronger than in any of the semiconductors in use so far. A good overview is given in [2.499]. Precisely defining doping and doping profiles is one of the core competencies of silicon CMOS electronics, e.g., [2.32, 2.149]. However, for III-N devices, control of the polarization effects gains an importance similar or even greater than the impact of the impurity doping profiles in other semiconductor materials. Fig. 2.3 gives the crystal structure of wurtzite GaN, as described, e.g., in [2.11, 2.12]. The noncentrosymmetric GaN crystal leads to a strong ionicity and a residual electrical polarity of the semiconductor. Fig. 2.3 depicts the planar nature of the polarity. The analysis of the crystal structure further reveals the physical mechanisms of the charge control, the overall available carrier concentration, and their dependence from the layer structure.

2.2.1 Spontaneous Polarization

A basic understanding of the impact of material growth conditions by various methods in the AlN/GaN/InN material system on the polarization charge is achieved and reported in [2.11, 2.12, 2.90]. The findings are based on the crystal polarization constants of Bernardini et al. in [2.36]. The importance of both spontaneous and piezoelectric components is pointed out there, in contrast to earlier publications, e.g., [2.22]. The spontaneous polarization occurs along the c -axis of wurtzite structures and leads to strong electric fields of 3 MV/cm [2.12]. Results for the PIC of the model are compared in [2.12] to experimental results for HEMT channels achieved at the date of publication; in the meantime, additional progress has been achieved for the improvement

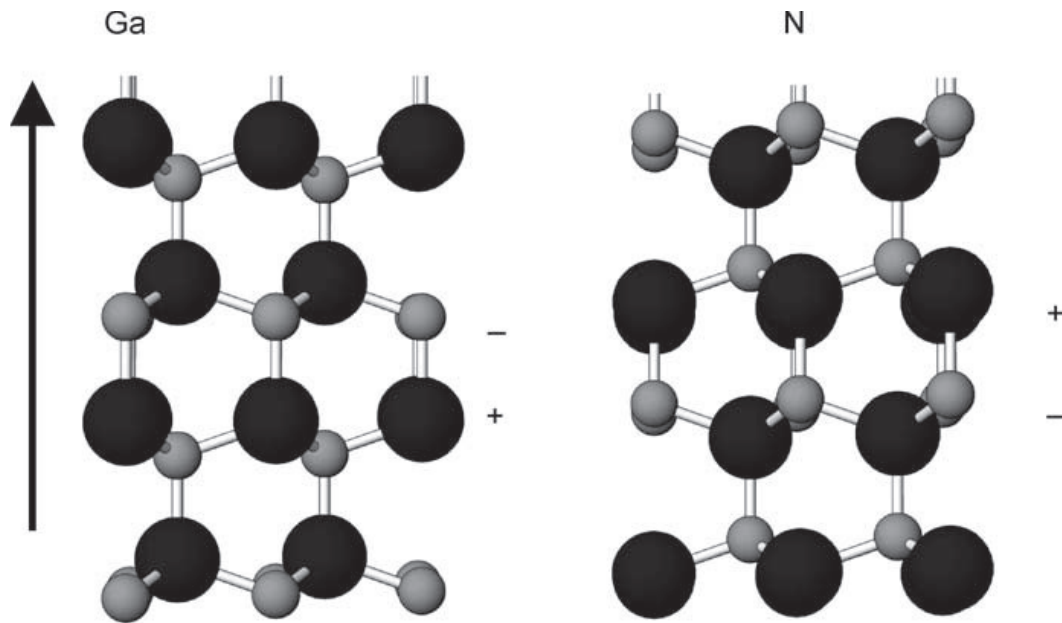


Fig. 2.3. Crystal structures of GaN for (a) (left) Ga-face, and (b) (right) N-face growth

in III-N material quality, i.e., for the reduction of defects. Basic findings for III-N layers grown by the two most important growth techniques, MOCVD and MBE, presented in these and other publications include:

- The absolute value of the piezoelectric constants of III-N semiconductors are ten times higher than in conventional III-V and II-VI semiconductors [2.36].
- Very similar mobility values, sheet carrier concentrations, and material quality are achieved for III-N semiconductors grown by MBE and MOCVD [2.96].
- Spontaneous polarization is more important than piezoelectric polarization for $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure interfaces [2.12, 2.36].
- Spontaneous polarization can be as important as piezoelectric polarization or even more important for $\text{In}(\text{Al})\text{N}/\text{GaN}$ interfaces and still lead to very high sheet carrier densities [2.12, 2.36, 2.231].
- The polarity of the polarization can be changed and even be inversed as a function of strain and thus of material composition.
- A difference exists between MBE- and MOCVD-grown material with respect to the variety of the polarity at the charged interfaces [2.12, 2.90].
- Theoretical and experimental results agree to a certain extent [2.11].
- Uncertainties arise from the impact of surface conditions [2.11] and Fermi-level pinning at the passivation interfaces, dislocations [2.11], possible polarity intermixing; the latter, however, is unlikely in good structures.
- Surface roughness and nonabrupt interfaces are considered less influencing the sheet carrier concentration.

Table 2.22. Parameter sets for the spontaneous polarization of III-N binary semiconductors

Material	GaN (C m ⁻²)	AlN (C m ⁻²)	InN (C m ⁻²)	Ref.
P_{SP}	-0.029	-0.081	-0.032	[2.36]
P_{SP}	-0.034	-0.090	-0.042	[2.485]

GaN layers can either be grown Ga-face(-up) or N-face(-up), compare Fig. 2.3. For the orientation of the polarization in this book, the positive direction points from the metallic cation (Ga,In) to the nitride anion (N) along the c -axis. Thus, in the case of a Ga-face interface, the polarization points toward the substrate, while for a N-face interface, the polarization is directed toward the surface of the layer sequence. For further evaluation, the devices are either (a) considered to be grown on a thick buffer, relaxing the mismatch from the substrate to the lattice constant of the device layers, or (b) the strain is residual in the device material. For the polarization analysis Table 2.22 gives parameter sets for the spontaneous polarization for the binary III-N materials from various sources. For all materials, the effective spontaneous polarization is negative and the magnitude increases from GaN to InN to AlN.

Interfaces between Binary and Ternary Materials

The following interpolation schemes can be used for the spontaneous polarization in the GaN/AlN, the InN/GaN, and the InN/AlN material system:

$$P_{\text{SP,Al}_x\text{Ga}_{1-x}\text{N/GaN}}(x) = \left(-0.052 \cdot x - 0.029 \right) (\text{Cm}^{-2}), \quad (2.16)$$

$$P_{\text{SP,In}_x\text{Ga}_{1-x}\text{N/GaN}}(x) = \left(-0.003 \cdot x - 0.029 \right) (\text{Cm}^{-2}), \quad (2.17)$$

$$P_{\text{SP,In}_x\text{Al}_{1-x}\text{N/GaN}}(x) = \left(0.049 \cdot x - 0.081 \right) (\text{Cm}^{-2}). \quad (2.18)$$

The methodology and the parameter values for the AlGa_N/GaN interface are taken from [2.36]. A similar theoretical study of the macroscopic polarization and the impact on the GaN HEMT in a nonlinear model of the material composition is given in [2.527].

2.2.2 Piezoelectric Polarization

In addition to spontaneous polarization, piezoelectric effects were first considered to be responsible for the sheet carrier densities in GaN devices, e.g., in [2.525]. Early C - V measurements of the piezoelectrically induced charge (spontaneous polarization is not considered explicitly) in Al_xGa_{1-x}N/GaN heterostructure FETs are given in [2.525] for both MBE- and MOCVD-grown material. The piezoelectric polarization is based on strain to the III-N crys-

Table 2.23. Piezoelectric constants e_{ij} , dielectric constants ϵ_{ij} , and lattice parameter a_i , c_i sets of III-N binary wurtzite semiconductors

Material	GaN	AlN	InN	BN	Ref.
e_{33} (C m ⁻²)	0.73	1.46	0.97	–	[2.36]
e_{31} (C m ⁻²)	–0.49	–0.6	–0.57	–	[2.36]
e_{33} (C m ⁻²)	–	1.55	–	–	[2.12]
e_{31} (C m ⁻²)	–	–0.58	–	–	[2.12]
e_{15} (C m ⁻²)	–	–0.48	–	–	[2.12]
e_{33} (C m ⁻²)	1	–	–	–	[2.338]
e_{31} (C m ⁻²)	–0.36	–	–	–	[2.338]
e_{15} (C m ⁻²)	–0.3	–	–	–	[2.338]
ϵ_{11} (–)	9.5	9.0	–	–	[2.29, 2.36]
ϵ_{33} (–)	10.4	10.7	–	–	[2.29, 2.36]
a_0 (Å)	3.189	3.112	3.54	2.534	[2.11]
c_0 (Å)	5.185	4.982	5.705	4.191	[2.11]

tal and a displacement of the anion-sublattice to the cation-sublattice, see Fig. 2.3. This can lead to very high electric fields of 2 MV/cm.

Table 2.23 gives a summary of the piezoelectric constants of the different III-N binary materials [2.11] for comparison and further evaluation. The lattice parameters have been added where necessary. In various publications, e.g., [2.36], the piezoelectric component is considered to have the highest uncertainty relative to the other components. The piezoelectric polarization induced by strain along the c -axis in a strained layer of wurtzite-type III-N semiconductors is calculated, according to [2.11]:

$$P_{\text{PZ}} = 2 \cdot \frac{a - a_0}{a_0} \left(e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}} \right). \quad (2.19)$$

In (2.19), C_{13} and C_{33} denote the elastic constants, which require special attention due to the residual strain in the semiconductor layers on top of the buffer. a and a_0 are the lengths along the hexagonal edge, which are similarly modified. For the lattice, elastic, and piezoelectric constants, the following linear interpolations are used for the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ material system [2.12]:

$$a_0(x) = (-0.077 \cdot x + 3.189) \cdot 10^{-10} \text{ (m)}, \quad (2.20)$$

$$c_0(x) = (-0.203 \cdot x + 5.189) \cdot 10^{-10} \text{ (m)}, \quad (2.21)$$

$$C_{13}(x) = (5 \cdot x + 103) \text{ (GPa)}, \quad (2.22)$$

$$C_{33}(x) = (-32 \cdot x + 405) \text{ (GPa)}, \quad (2.23)$$

$$e_{33}(x) = 0.73 \cdot x + 0.73 \text{ (C m}^{-2}\text{)}, \quad (2.24)$$

$$e_{31}(x) = -0.11 \cdot x - 0.49 \text{ (C m}^{-2}\text{)}. \quad (2.25)$$

For the $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ material system, where GaN forms the channel, the interpolation reads:

$$a_0(x) = (0.418 \cdot x + 3.112) \cdot 10^{-10} \text{ (m)}, \quad (2.26)$$

$$c_0(x) = (0.723 \cdot x + 4.982) \cdot 10^{-10} \text{ (m)}, \quad (2.27)$$

$$C_{13}(x) = (-16 \cdot x + 108) \text{ (GPa)}, \quad (2.28)$$

$$C_{33}(x) = (-149 \cdot x + 373) \text{ (GPa)}, \quad (2.29)$$

$$e_{33}(x) = -0.49 \cdot x + 1.46 \text{ (C m}^{-2}\text{)}, \quad (2.30)$$

$$e_{31}(x) = 0.03 \cdot x - 0.6 \text{ (C m}^{-2}\text{)}. \quad (2.31)$$

For the $\text{GaN}/\text{In}_x\text{Ga}_{1-x}\text{N}$ material system, where GaN forms the barrier layer with the higher bandgap energy the interpolation reads growing the InGaN pseudomorphically on GaN:

$$a_0(x) = (0.351 \cdot x + 3.189) \cdot 10^{-10} \text{ (m)}, \quad (2.32)$$

$$c_0(x) = (0.52 \cdot x + 5.189) \cdot 10^{-10} \text{ (m)}, \quad (2.33)$$

$$C_{13}(x) = (-11 \cdot x + 103) \text{ (GPa)}, \quad (2.34)$$

$$C_{33}(x) = (-176 \cdot x + 405) \text{ (GPa)}, \quad (2.35)$$

$$e_{33}(x) = 0.24 \cdot x + 0.73 \text{ (C m}^{-2}\text{)}, \quad (2.36)$$

$$e_{31}(x) = -0.08 \cdot x - 0.49 \text{ (C m}^{-2}\text{)}. \quad (2.37)$$

The calculation of the PIC derived from the above polarization results is described later.

2.2.3 Device Design Using Polarization-Induced Charges

Deduced from the above considerations, the resulting charge can be calculated for the various interface combinations and growth conditions in several device configurations. In this context, mechanisms of the 2D-electron gas formation in AlGaN/GaN HEMTs are investigated by synchrotron radiation emission spectroscopy in [2.160]. The surface Fermi-level at the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ interface is found to be pinned at an energy of 1.6 eV below the conduction band minimum independent of the Al-content. Initial measurements of the piezoelectrically induced charge in AlGaN/GaN HFETs are given in [2.525]. For a heterointerface, the following formulae hold for the interface charge σ_B derived from the tensor of the wurtzite crystals mentioned above [2.11]:

$$\sigma_B = \mathbf{n} \cdot \mathbf{P}, \quad (2.38)$$

$$= P_{\text{bottom}} - P_{\text{top}}, \quad (2.39)$$

$$= P_{\text{SP,bottom}} - [P_{\text{SP,top}} + P_{\text{PZ,top}}], \quad (2.40)$$

$$= \sigma_{B,\text{SP}} + \sigma_{B,\text{PZ}}. \quad (2.41)$$

Deduced from (2.38)–(2.41), various interface combinations and devices can be constructed for their use in heterostructure FETs and HBTs. Some will be

discussed later. The situations are displayed graphically in Fig. 2.4 with focus on electron devices. Hole-based devices are neglected due to the poor transport properties in the III-N system. For an electron channel, two conditions must be fulfilled:

- A positive interface charge must be present at the interface based on the overall polarization
- The bandgap in the semiconductor, to where the electrons are driven, must be smaller than of the other layer (as III-N semiconductor only form type I transitions).

I: $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ Single Heterojunction HEMT

For an $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer grown on top of a relaxed GaN layer, spontaneous polarization and piezoelectric polarization are parallel and under tensile strain. Depending on the growth conditions, the following situations occur:

1. In the case of Ga-face, i.e., a anion surface, the polarity of the parallel polarization components results in an electron GaN channel formation at the interface.
2. In the case of N-face or cation-type growth, however, the orientations of both the polarization components are changed and thus no electron channel formation occurs at the $\text{AlGa}_{1-x}\text{N}/\text{GaN}$ interface.

In this context it is an important assumption for the charge analysis that no additional material or layers are grown on top of the $\text{AlGa}_{1-x}\text{N}$ barrier layer. Additional surface states and the interaction with additional interfaces reduce the carrier concentration at the interface under consideration. This is also true for nucleation layer sequences used to compensate the lattice-mismatch directly at the substrate–buffer interface.

II: $\text{GaN}/\text{In}_x\text{Ga}_{1-x}\text{N}$ Single and Double Heterojunction HEMT

For the interface of $\text{In}_x\text{Ga}_{1-x}\text{N}$ with various concentrations grown pseudomorphically on top of a relaxed GaN buffer, the $\text{In}_x\text{Ga}_{1-x}\text{N}$ layer is under compressive strain for all material compositions. Spontaneous and piezoelectric polarization are antiparallel and the piezoelectric polarization is stronger than the spontaneous polarization. The following situations can occur, depending on growth conditions:

1. In the case of Ga-face growth, the residual polarization points toward the GaN, thus the effective charge at the interface is negative, and no electron channel is formed.
2. In the case of N-face growth, the effective interface charge is positive and a 2DEG forms a channel in the $\text{In}_x\text{Ga}_{1-x}\text{N}$.

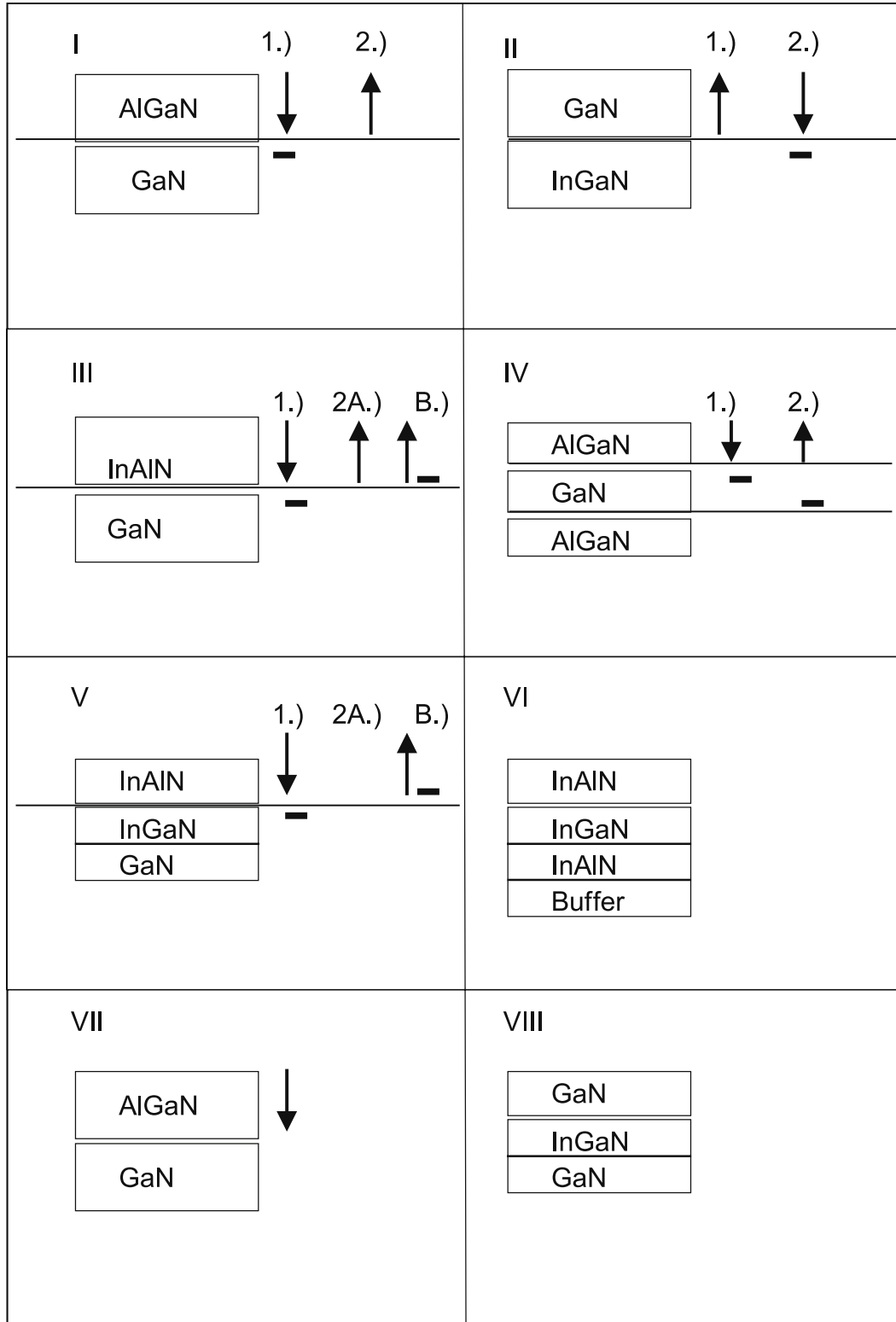


Fig. 2.4. Polarization situations for various III-N devices

III: $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ Single Heterojunction HEMT

For the interface $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$, the two binaries InN and AlN forming $\text{In}_x\text{Al}_{1-x}\text{N}$ have a bandgap both smaller and larger than the bandgap of GaN , which makes the situation more complicated. The GaN buffer is grown relaxed on the substrate, thus the $\text{In}_x\text{Al}_{1-x}\text{N}$ layer on top is under different strain unless for $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$, which is lattice-matched to crystalline GaN .

1. For Ga-face growth, both polarization components are parallel for $x < 0.17$, and an electron channel forms in the GaN layer for $x < 0.3$ due to the resulting overall polarization, e.g., [2.231].
2. For N-face growth the interesting situation arises for $x > 0.3$. Both polarization types are antiparallel in the $\text{In}_x\text{Al}_{1-x}\text{N}$ with the following distinction:
 - A.) For $0.3 < x < 0.6$, no electron channel forms in the $\text{In}_x\text{Al}_{1-x}\text{N}$ as the bandgap of $\text{In}_x\text{Al}_{1-x}\text{N}$ is still bigger than of GaN .
 - B.) For $0.6 \leq x \leq 1$ the bandgap of GaN is larger than of $\text{In}_x\text{Al}_{1-x}\text{N}$, thus a 2DEG and thus an electron channel forms in the $\text{In}_x\text{Al}_{1-x}\text{N}$.

IV: $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}/\text{Al}_y\text{Ga}_{1-y}\text{N}$ Double Heterojunction HEMT

The realization of double heterojunction devices is very desirable due to enhanced carrier confinement for both HEMT and HBT and improved back-side isolation for FETs. The assumption of a relaxed GaN buffer on top of the substrate has to be dropped in this case. A good trap-free $\text{Al}_y\text{Ga}_{1-y}\text{N}$ material has to be grown relaxed on a substrate such as SiC or sapphire with a material composition grading of the $\text{Al}_y\text{Ga}_{1-y}\text{N}$ buffer and leading to an $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}/\text{Al}_y\text{Ga}_{1-y}\text{N}$ heterostructure. Double heterostructure FETs are realized, e.g., in [2.289]. A smaller composition y is chosen for the buffer layer to reduce the mismatch toward the substrate. When growing AlGaIn on top of SiC , either N-face or Ga-face polarization can be chosen for the first interface:

- In the case of a Ga-face growth, a conventional double heterojunction FET forms with an electron channel at the upper heterointerface.
- In the case of an N-face growth, an inverted double heterojunction FET forms with an electron gas at the lower interface under the assumption, that the upper barrier does not modify the strain of the GaN channel layer.

Typically, a Ga-face approach will be chosen which improves the isolation of the channel toward the buffer layer and thus typically reduces the I_{Dmin} for FETs. Further, in [2.289], the transconductance g_m is increased as compared to the single heterojunction device.

V: $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}$ Double Heterojunction HEMT on GaN Buffer

In the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ material system, the sheet carrier concentration density in the channel is increased by the increase of x and at the same

time limited by the increase of defect concentration in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer for rising x and the onset of relaxation. An $\text{In}_y\text{Ga}_{1-y}\text{N}$ channel layer is a more general case of the situation III of the InAlN/GaN HFET. An $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$ double heterojunction FET can be formed in this case. The formation of electron or hole gases is dependent on both material compositions x and y . In [2.230], mole fractions of $0.08 \leq x \leq 0.27$ and $(0 \leq y \leq 0.18)$ are suggested for the formation of HFETs, based on the analysis of the maximum strain values possible in the $\text{In}_x\text{Al}_{1-x}\text{N}$ barrier. $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ is lattice-matched to GaN. Strain analysis based on a relaxed GaN buffer yields the following distinction [2.230]:

- For $\text{In}_x\text{Al}_{1-x}\text{N}$ with $x \leq 0.17$ the $\text{In}_x\text{Al}_{1-x}\text{N}$ is under tensile strain and the piezoelectric field in the channel is in favor of the increase in electron concentration.
- For $\text{In}_x\text{Al}_{1-x}\text{N}$ with $x \geq 0.17$, the $\text{In}_x\text{Al}_{1-x}\text{N}$ is under compressive strain, and the strain reduces the electron concentration [2.231].
- Assuming an $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ barrier lattice-matched to GaN, the channel material $\text{In}_y\text{Ga}_{1-y}\text{N}$ can be varied:
- The compressive strain in the $\text{In}_y\text{Ga}_{1-y}\text{N}$ can be varied in the range $0.08 \leq x \leq 0.27$ in order to further enhance the charge carrier density and the upper $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}$ interface. A value of $y = 0.1$ and $x = 0.17$ is suggested in [2.230] to double the drain current density, as compared to the $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ structure.

The situation V 2B.) in Fig. 2.4 becomes very unlikely in this case, as the bandgap of the InGaN in the channel reduces with increasing y . Very high currents are predicted for these HFETs in [2.230] with maximum current levels beyond 4 A mm^{-1} . Technical realizations yield maximum drain currents of 0.4 A mm^{-1} , e.g., in [2.232]. High-saturated drain current levels of 1.33 A mm^{-1} have been reported in [2.84].

VI: $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}/\text{In}_z\text{Al}_{1-z}\text{N}$ Double Heterojunction HEMT on Arbitrary Buffer

The assumption of the growth on relaxed GaN buffer must be further modified for the growth on arbitrary substrates. Double heterojunction devices can be formed in the $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}$ material system. An $\text{In}_z\text{Al}_{1-z}\text{N}$ buffer will be grown on top of a substrate. The selection $z = 0.17$ yields a situation with the buffer lattice-matched to GaN. Arbitrary mole fractions yield the most complicated situation, i.e., a double $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}/\text{In}_z\text{Al}_{1-z}\text{N}$ heterojunction HEMT with three material compositions x , y , and z . The situation is similar to that of the $\text{AlGaIn}/\text{GaN}/\text{AlGaIn}$ heterostructure device; however, as the two polarization components are antiparallel, more distinctions are necessary. The distinction yields a similar analysis for the material composition as in the case of a single heterojunction using InAlN grown on a GaN layer. However, the transition to any substrate is critical, as a second channel can form at the nucleation layer/ InAlN buffer interface.

VII: $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ NPN-Single Heterojunction Bipolar Transistor

Polarization engineering in III-N HBTs is a secondary concern relative to the present severe issues like collector leakage due to the impact of dislocations, and processing issues, such as aggressive etch processes with subsequent surface damage increasing base ohmic contact resistance, e.g., [2.269, 2.283]. Material growth is, of course, of critical importance in the bipolar device; however, it is important, mostly with respect to mismatch reduction. Subsequent bandgap engineering requires the inclusion of the polarization effects [2.282], as their neglect would be misleading. A very simple AlGaIn/GaN HBT can be grown using a thick GaN n-doped subcollector and a GaN n-doped collector on top of a substrate. A p-doped GaN base is added, as performed, e.g., in [2.383]. The emitter layer consists of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and typically reveals material compositions $x = 0.1$ [2.513]. The AlGaIn emitter is typically capped with a GaN layer which is highly Si-doped, and the transition is either graded or abrupt. The GaN-base p-doping, typically Mg, is degenerate with nominal doping levels of $p \geq 10^{19} \text{ cm}^{-3}$, although the activation is relatively low, i.e., $\leq 10^{18} \text{ cm}^{-3}$. This is due to the high activation energy [2.382] of the deep acceptor Mg with $E_A - E_V \approx 170 \text{ meV}$. The growth at the base/emitter heterointerface will thus be Ga-face with a channel-like (donor-like) positive polarization charge at the emitter(AlGaIn)/base(GaN) junction. This further results in a negative polarization (acceptor-like) charge at the graded AlGaIn/GaN-Si interface near the top contact. Deduced from this, an additional electron barrier is created in the conduction band at the base/emitter junction and within the emitter grading. In [2.282], these additional peaks are flattened by smoothing the interface by material grading. This feature allows the prevention of hole injection into the emitter without hindering the electron transport. Several other issues will be discussed in the context of polarization engineering and its subsequent effects. The carrier lifetimes in the base at the GaN pn-junctions at different mobility levels are discussed in [2.141], yielding values between 24 and 240 ps. The impact of the polarization doping to the base layer is discussed in [2.23, 2.420]. Normal collector-down device/emitter up configuration see reduced p-doping for the Ga-face growth, while collector-up devices experience additional carrier concentration through polarization doping in the p-layers.

VIII: $\text{GaN}/\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ Double Heterojunction Bipolar Transistor (DHBT)

Due to the limited doping activation of Mg in GaN and to several other issues in AlGaIn/GaN HBTs, $\text{GaN}/\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ npn-DHBTs have been developed and successfully demonstrated, e.g., in [2.271]. Again, polarization engineering is only a secondary concern. The advantage of $\text{In}_x\text{Ga}_{1-x}\text{N}$ as a base material is caused by the increase of the p-doping activation, e.g., up to $7 \times 10^{18} \text{ cm}^{-3}$ as reported in [2.269]. This is based on the lower acceptor activation energies in p- $\text{In}_x\text{Ga}_{1-x}\text{N}$. The base layers are grown with a material composition of $0.17 \leq x \leq 0.25$ [2.311], yielding a doping activation of $4 \times$

10^{18} cm^{-3} . A double heterojunction is desirable due to the higher bandgap of GaN in the collector and the increased leakage current of a GaN/InGaN single heterojunction device, as mentioned in [2.269]. On the other hand, the conduction band spike at the collector/base interface has to be reduced, e.g., by material grading in the base towards the lower interface [2.269].

2.2.4 Analytical Calculation of Channel Charge Concentrations

For the calculation of the resulting charge at the heterointerface, the following interpolation formulae have been suggested in [2.22, 2.525], assuming no additional doping in the barrier and no surface effects apart from the interface under consideration:

$$n_{\text{sheet}} = \frac{\sigma(x)}{e} - \left(\frac{\epsilon_0 \cdot \epsilon(x)}{d_{\text{AlGaIn}} \cdot e^2} \right) [e \cdot \phi_B(x) + E_F(x) - \Delta E_C(x)]. \quad (2.42)$$

Derived from (2.42), the maximum sheet carrier concentration of $6 \times 10^{13} \text{ cm}^{-2}$ at a GaN/AlN interface can be calculated [2.12]; however, it strongly depends on the degree of relaxation at the GaN/AlN interface. Recent HFET device examples with very high sheet carrier densities can be found in [2.68] using $\text{Al}_{0.34}\text{Ga}_{0.66}\text{N}/\text{GaN}$ HFETs which yield sheet carrier densities of $1.45 \times 10^{13} \text{ cm}^{-2}$. Fig. 2.5 gives the dependence of the sheet resistance and Fig. 2.6 of the 2D-sheet carrier concentration from the material composition at an $\text{GaN}/\text{Al}_x\text{Ga}_{1-x}\text{N}$ heterostructure interface presented in recent publications. The impact of both barrier thickness and substrate is neglected in Fig. 2.5 and Fig. 2.6. Further the insertion of doping and of an AlN interlayer is depicted, for details see Chapter 3. Fig. 2.5 suggests a statistically proven linear variation of the sheet resistance from 500 to $200 \Omega \text{ sq}^{-1}$. Fig. 2.6 shows a variation of the sheet carrier concentration of $7 \times 10^{12} \text{ cm}^{-2}$ for $x = 0.15$ to $1.6 \times 10^{13} \text{ cm}^{-2}$ for $x = 0.5$. At the same time, the influence of the additional n-doping in the barrier layers on the carrier concentration can be seen in Fig. 2.6, as discussed later. Both MBE and MOCVD provide similar charge concentrations as a function of the mole fraction.

2.2.5 Doping Issues

Independent of the impact of polarization as a source of carriers, bulk doping is of fundamental importance for the definition of material and device characteristics, as in any semiconductor. Review on the doping issues of III-N materials is supplied, e.g., in [2.87, 2.370, 2.437]. Some doping parameters are given in Table 2.25. III-N semiconductors are doped with impurities such as Si, Ge, Se, O, Mg, Be, and Zn. Typical unintentional impurities are C, H, O, and grown-in defects, such as vacancy and antisite point defects [2.417].

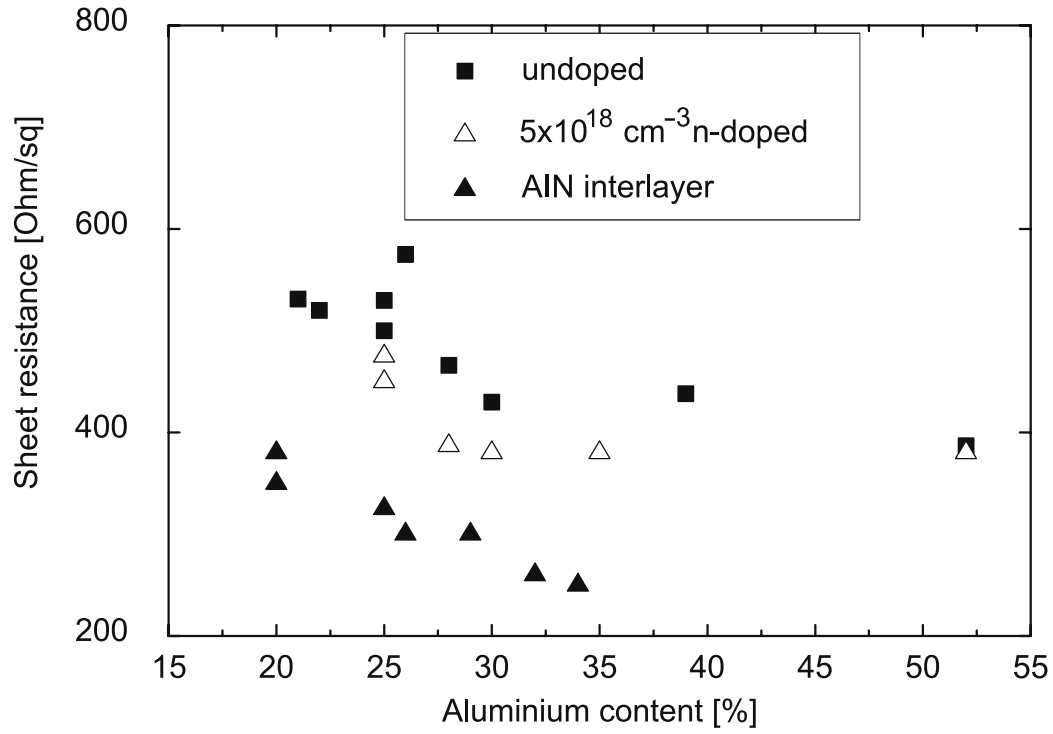


Fig. 2.5. Sheet resistance of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures as a function of aluminum content x

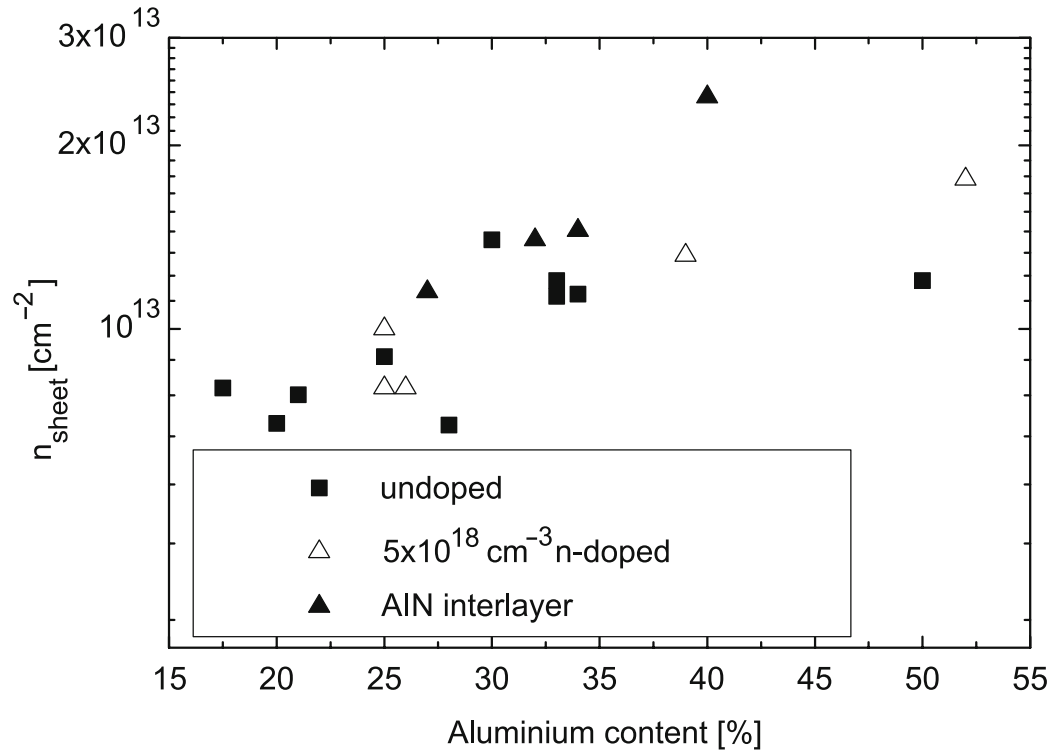


Fig. 2.6. Sheet carrier concentration in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures as a function of aluminum content x

N-Doping

In electronic devices, n-doping is of critical importance for δ -doped high-voltage HFETs and the definition of contacts in FETs and HBTs. NID-GaN is found to be typically n-type. This is caused by either nitrogen vacancies, Ga interstitials or oxygen incorporation depending on the growth method [2.351].

Silicon doping is the typical choice for intended n-doping. The activation energy of silicon in GaN is 5–9 meV which allows effective doping [2.351]. Apart from the polarization doping, silicon doping can serve as additional carrier source in the channel. Given the high-operation voltages, the stability of such silicon doping in the barrier layer is crucial, as δ -doping is affected by the field peaks in any HEMT.

P-Doping

The reduced performance of p-doping of GaN is the most critical issue reducing optoelectronic device performance in III-N materials. This includes diodes [2.322, 2.325, 2.432], laser diodes [2.326], and bipolar transistors [2.383] on the electronic side. The issues involve:

- High-contact resistances and nonohmic behavior at the base [2.383] due to:
 - Reduced current gain at RT due to high-thermal activation energy of Mg of 120–200 meV as an acceptor [2.225]
 - Reduced activation of Mg due to the formation of Mg–H during MOCVD growth
- Mg MOCVD reactor memory leading to soft pn-junction doping profiles and reduced confinement of p-doping to the base layer [2.383] for both MBE- and MOCVD-growth.

Photoluminescence measurements in Mg-doped GaN grown by metal organic vapor-phase epitaxy (MOVPE) are described, e.g., in [2.248]. An ionization energy of the acceptor of 173 meV is concluded. The bandgap narrowing for high doping concentrations is found to be in the order of 10 meV. For MBE growth, the following modifications are necessary:

- No Mg-reactor memory occurs
- Sharper doping profiling is possible

The maximum doping activation of Mg in GaN is thus of the order of $\leq 10^{18} \text{ cm}^{-3}$ at room temperature. More details with respect to the growth conditions will be given in Chapter 3.

2.2.6 Surfaces and Interfaces

Due to the aforementioned properties of III-N heterostructures, surfaces and interfaces require special attention in this book. The principal properties of the different interfaces shall be discussed here, while their technological realization is considered in Chaps. 3 and 4.

III-N/III-N Interfaces

Apart from the polarization effects already discussed in detail, several effects at a semiconductor/semiconductor interface occur, due to the change of the material or the material composition:

1. An energy alignment of the valence band and conduction band is observed.
2. Strain effects occur due to the modification of the lattice constants at the interface.
3. The interface is a preferred location for states, e.g., [2.160].
4. In III-N semiconductors, the differences in the polarization occur at the interface, leading to excess carrier concentrations.
5. Due to the quantization effects near the interface, transport occurs very close to the interface, which is especially true for the III-N materials due to the specific band structures.

The next paragraphs compile the enumerated issues.

Energy Alignment and Bandgap Energies

The energy alignment occurs in three different types of transitions in any semiconductor, e.g., [2.356]. The GaN/Al_xGa_{1-x}N semiconductor/semiconductor interface is a type I interface. For both electrons and holes, energy barriers are formed in one direction. Thus channel or charge-accumulation areas can form, if the appropriate carriers are provided. The conduction band energy offset alignment of a ternary material A_xB_{1-x}N/CN is described, e.g., for the Al_xGa_{1-x}N/GaN interface:

$$\Delta E_C(x) = 0.7 \cdot [E_g(\text{Al}_x\text{Ga}_{1-x}\text{N}) - E_g(\text{GaN})]. \quad (2.43)$$

The bandgap energy for Al_xGa_{1-x}N as a function of material composition can be described as:

$$E_g(x) = x \cdot E_g(\text{AlN}) + (1 - x) \cdot E_g(\text{GaN}) + (1 - x) \cdot x \cdot C_{E_g, \text{AlGa}}. \quad (2.44)$$

The bowing factor $C_{E_{\text{gap}}, \text{AB}}$ is already given in Table 2.21. The valence band offset energy ΔE_V is then determined accordingly from the following equation:

$$E_g(\text{Al}_x\text{Ga}_{1-x}\text{N}) = \Delta E_C + \Delta E_V + E_g(\text{GaN}). \quad (2.45)$$

The above relations can be generalized for several other material combinations A_xB_{1-x}N/C_xD_{1-x}N in the III-N system. Table 2.24 summarizes the parameters for the energy alignment for the combinations in the III-N world. Overviews are given in [2.203, 2.429]. Table 2.24 gives the full summary of all parameters according to (2.43)–(2.45). The alignment of the ternary semiconductors depends critically on the bowing parameters of the bandgap, which are discussed in Table 2.21. The modifications of the bandgap energies due

Table 2.24. Parameters for energy alignment of the III-N binary and ternary interfaces at RT

Material	Interface type (–)	E_g (eV)	E_g (eV)	ΔE_C (eV)	ΔE_V (eV)	Ratio (–)	Ref.
AlN/GaN (Wz)	Type I	6.2	3.43	1.97	0.8	0.7/0.3	[2.11]
AlN/GaN (Zb)	Type I	5.1	3.38	0.92	0.8	0.53/0.47	[2.203]
InN/AlN (Wz)	Type I	0.77	6.2	3.62	1.81	0.66/0.34	[2.203]
InN/AlN (Zb)	Type I	0.75	5.1	3.31	1.04	0.76/0.24	[2.203]
InN/GaN (Wz)	Type I	0.77	3.43	1.61	1.05	0.6/0.4	[2.203]
InN/GaN (Zb)	Type I	0.75	3.38	1.58	1.05	0.6/0.4	[2.203]
GaN/Al _{0.2} Ga _{0.8} N	Type I	3.43	3.79	0.252	0.108	0.7/0.3	[2.230]
GaN/In _{0.17} Al _{0.83} N	Type I	3.43	4.7	0.66	0.61	0.52/0.48	[2.230]
In _{0.1} Ga _{0.9} N/ In _{0.17} Al _{0.83} N	Type I	3.03	4.7	0.868	0.801	0.52/0.48	[2.230]
GaN/In _{0.2} Ga _{0.8} N	Type I	3.43	3.58	0.09	0.06	0.6/0.4	[2.203]

to the different directions of the polarization at the interface and in quantum wells are discussed, e.g., in [2.498]. The energy levels in $\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ quantum wells are analyzed for thickness between 23 and 130 Å. By variation of the composition the energy levels can be adjusted to the needs of the application.

Bulk and Interface Traps

Typical trap energies and other defect properties observed experimentally at the heterojunctions and in the bulk are given in Table 2.25. Good overview of defects in bulk materials are given in [2.89,2.221,2.315,2.389,2.390]. The occurrence of traps is of critical importance. It is partly caused by the heteroepitaxy, i.e., the growth on nonnative substrates. As the wide bandgap properties are modified by these traps with activation energies in the range of conventional semiconductors, such as Si or GaAs, the breakdown properties are critically affected, i.e., reduced. Table 2.25 compiles typical trap parameters. At the interfaces, traps lead to the pinning of the Fermi-level, as is described in [2.160]. The pinning of the Fermi-level in GaN is found to be about midgap, which puts GaN in a similar situation as GaAs. Other reports suggest a Fermi-level pinning at $E_C - 0.5$ eV [2.250] due to nitrogen vacancies or at $E_C - 0.8$ eV due to oxygen. Further details are given below.

Strain in III-N Semiconductors

As is discussed with the polarization effects, strain is a very important parameter in the design of substrate semiconductor buffer. In addition, the lattice-mismatch among different semiconductor layers is important for the resulting material quality and crystal stability. Table 2.26 compiles the lattice constants a_0 and the resulting lattice-mismatch along a_0 between the various III-N mate-

Table 2.25. Trap and doping parameters in III-nitride materials

	Doping	Energy (eV)	Donor	Ref.
GaN	n	$E_C - 0.44$	–	[2.490]
GaN	n	$E_C - 0.5$	–	[2.250]
GaN	n	$E_C - 0.005$	Si	[2.351]
GaN	p	$E_V + 0.22$	Mg	[2.350, 2.475]
GaN	p	$E_V + 0.23$	C	[2.350]
GaN	p	$E_V + 0.25$	Be	[2.350]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	n	$E_C - 0.017$ ($x = 0$)	Si	[2.351]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	n	$E_C - 0.054$ ($x = 0.18$)	Si	[2.351]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	n	$E_C - 0.090$ ($x = 0.6$)	Si	[2.351]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	p	$E_V + 0.4$	Mg	[2.475]

Table 2.26. Lattice constant a_0 (matrix diagonal) and mismatch for the III-N binary materials at 300 K

Material	GaN (Å)(%)	AlN (Å)(%)	InN (Å)(%)	SiC (Å)(%)	Sapphire (Å)(%)	Silicon (Å)(%)	Ref.
GaN (sub.)	3.189	2.3	10.6	3.3	14.8	–	[2.449]
AlN (sub.)	2.4	3.119	12	1.0	12.5	–	[2.323]
InN (sub.)	10.6	12	3.5446	14	25.4	–	[2.323]
SiC (sub.)	3.3	1.0	14	3.081	–	–	[2.323]
Sapphire (sub.)	14.8	12.5	25.4	11.5	2.777 (4.758)	–	[2.323]
Silicon (sub.)	16.9	18.7	7.6	–	–	3.84 (5.431)	[2.419]

rials and substrates. The lattice-mismatch is calculated according to

$$f_c = \frac{a - a_0}{a_0}. \quad (2.46)$$

For SiC substrates, the lattice-mismatch is calculated from the lattice constant a . For silicon and sapphire the calculation needs some explanation. Silicon is a well investigated material and only the III-N-relevant parameters shall be given. GaN can be grown in the hexagonal phase on the 111-plane of the silicon. In this case the effective lattice constant of 3.84 Å can be used. For sapphire, the growth is along the 0001-direction. This leads to an effective constant of 2.77 Å . Applying the rules of Matthews and Blakeslee [2.280] or Fischer [2.11] for the pseudomorphic growth of III-N materials, the critical thicknesses given in Table 2.27 are obtained for the semiconductor/semiconductor transitions. Table 2.27 gives estimates of the critical thickness for typical material compositions. $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ can only be grown with a thickness of 20 nm on top of fully relaxed GaN. The less conservative calculation approach of Fischer [2.115] leads to a critical thickness of 40 nm for $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$. Thus AlGaN relaxation can occur for the composition $0 \leq x \leq 0.4$ for thicknesses

Table 2.27. Critical thicknesses obtained by various methods

Material	Thickness (nm)	Method	Ref.
Al _{0.2} N _{0.8} N on GaN (sub.)	20	calc. (MB)	[2.11]
Al _{0.2} N _{0.8} N on GaN (sub.)	40	calc. (Fischer)	[2.11]
AlN on GaN (sub.)	2.9	measured	[2.199]
In _{0.1} Ga _{0.9} N on GaN (sub)	10	calc. elastic	[2.146]
In _{0.17} Al _{0.83} N on GaN (sub)	∞	—	[2.231]
In _{0.27} Ga _{0.77} N on GaN (sub)	15	calc. (Fischer)	[2.231]

MB Matthews/Blakeslee

of up to 30 nm in AlGa_xN barriers grown on GaN. In_xAl_{1-x}N can be grown lattice-matched on GaN for $x = 0.17$. The critical thickness of In_{0.1}Ga_{0.9}N on GaN is 10 nm. This leaves ample opportunities for heterostructure design.

III-N/Dielectric Interfaces

The physical nature of the III-N semiconductor surfaces toward vacuum, gases, liquids, or any dielectric material determines device performance to a high extent. A key property of GaAs materials as compared to silicon-based device technology is the lack of an unpinned GaAs/oxide interface [2.117,2.118]. Similar surfaces prevail for III-N devices with SiN. For GaN, a Fermi-level pinning close to a midgap energy level is described in [2.483]. Using SiO₂ as a dielectric, the interface GaN/SiO₂ is found to have a very low surface charge density, as reported in [2.276,2.277]. For the Al_{0.24}Ga_{0.76}N surface, experimental evidence for the Fermi-level pinning is found in [2.154,2.160]. The underly-

Table 2.28. Fermi-level (surface potential) energies of III-N semiconductors at vacuum and dielectric interfaces

Material	Surface potential (eV)	Ref.
n-GaN/Vacuum	$E_C - 1.2$	[2.303]
n-GaN/Vacuum	$E_C - 2.8$	[2.477]
n-GaN(Si)/Vacuum	$E_C - 1.5, E_C - 0.2$	[2.205]
GaN/SiN	$E_C - 2.4$	[2.82]
GaN/Si ₃ N ₄	$E_C - 0.27$	[2.25]
GaN/SiO ₂	$E_C - 0.13$	[2.25]
Al _{0.34} Ga _{0.66} N/Vacuum	$E_C(\text{Al}_{0.34}\text{Ga}_{0.66}\text{N}) - 1.65 \text{ eV}$	[2.154]
Al _{0.24} Ga _{0.76} N/Vacuum	$E_C(\text{Al}_{0.24}\text{Ga}_{0.76}\text{N}) - 1.6 \text{ eV}$	[2.160]
Al _{0.35} Ga _{0.65} N/Vacuum	$E_C(\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}) - (1.4 \text{ to } 1.7 \text{ eV})$	[2.209]
GaN/Al _{0.35} Ga _{0.65} N/Vacuum	$E_C(\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}) - (1.4 \text{ to } 0.6 \text{ eV})$	[2.208]
In _{0.3} Ga _{0.7} N/Vacuum	$E_C(\text{In}_{0.3}\text{Ga}_{0.7}\text{N})$	[2.247, 2.477]
InN/Vacuum	$E_C(\text{InN}) + 0.6 \text{ eV}$	[2.477]

ing data are obtained by synchrotron radiation photoemission spectroscopy (SRPES). Table 2.28 compiles available surface and interface data. Due to the more ionic bond between gallium and nitrogen relative to more covalent semiconductors such as GaAs and InP, the pinning or Fermi-level stabilization at the surface should be less pronounced, as argued in [2.429]. However, several reports exist on the stabilization of the Fermi-level for GaN, $\text{Al}_x\text{Ga}_{1-x}\text{N}$, and InN [2.154, 2.160].

III-N/Metal Interfaces

The properties of III-N/metal interfaces are essential for the performance of nearly all device applications.

N-type Ohmic Contacts

The formation of ohmic contacts is a fundamental component in the fabrication of semiconductor devices. For n-contacts in III-N, intrinsic doping is the most important contender for reducing the contact resistance. Due to the wide bandgap properties, the typical contacts yield special formation properties such as high-annealing temperatures between 500°C [2.197] and 900°C [2.31]. Special geometric definitions, such as recessed ohmic contacts [2.198] or non-alloyed implanted contacts [2.526], have been suggested. At the same time, good ohmic contacts are also more easily achieved for III-N semiconductors, due to the high sheet carrier density at the interface, due to both the impact of polarization or due to impurity doping, especially using silicon.

P-type Ohmic Contacts

P-contacts are very well investigated due to their fundamental importance in the field of optoelectronics, e.g., in [2.325]. P-contacts issues prevail due to both the reduced doping activation and deep activation energies relative to the valence band. These properties of p-doping limit the performance of optoelectronic devices, which is one reason for the great number of publications on this topic. Detailed overview data in this book are given in Chapter 4.3.1.

Schottky Contacts

The formation of Schottky contacts on III-N semiconductors is a very critical capability for two reasons. First, wide bandgap FETs are required to support very high fields because of the high operation voltages required, while the semiconductor/metal transitions form Schottky interfaces with barrier heights of ≤ 1.5 eV. Second, for high-power applications, the Schottky contacts are subject to the very high channel lattice temperatures $\geq 300^\circ\text{C}$. Thus, Schottky contacts currently form a weakpoint within the semiconductor device architecture, especially with respect to reliability. Further overview data are given in Chapter 4.3.2.

2.2.7 Transport Properties in Polarized Semiconductors

The polarization effects at the interface favor very strong quantization effects. The transport properties in this highly quantized situation [2.421] will be discussed again in this section.

Monte Carlo Simulations

Long before the realization of advanced GaN HEMTs, which allow the extraction of high-speed properties, a large number of predictions have been made, especially by ab-initio calculations or by Monte Carlo simulations based on these calculations [2.492]. Initial electron mobilities of GaN, InN, and AlN are calculated by variational principle in [2.64]. Initial MC simulations of the velocity-field characteristics in bulk wurtzite-phase GaN are presented in [2.37]. They predict a maximum electron velocity of $3.1 \times 10^7 \text{ cm s}^{-1}$ and a saturation field of 150 kV cm^{-1} at room temperature. The analysis is performed between 77 and 1,000 K. Simulations of the transient transport in GaN and InN are given in [2.121]. Most of the initial simulations mentioned so far do not consider the interaction of the electrons with longitudinal and transversal optical phonons correctly [2.19, 2.517], and further, in the case of InN, use the bandgap of 1.89 eV at RT, e.g., [2.348]. Fig. 2.7 gives the comparison of simulated and measured velocity-field characteristics of GaN. The data in Fig. 2.7 are taken from [2.37, 2.121]. Additionally, Fig. 2.7 depicts experimental

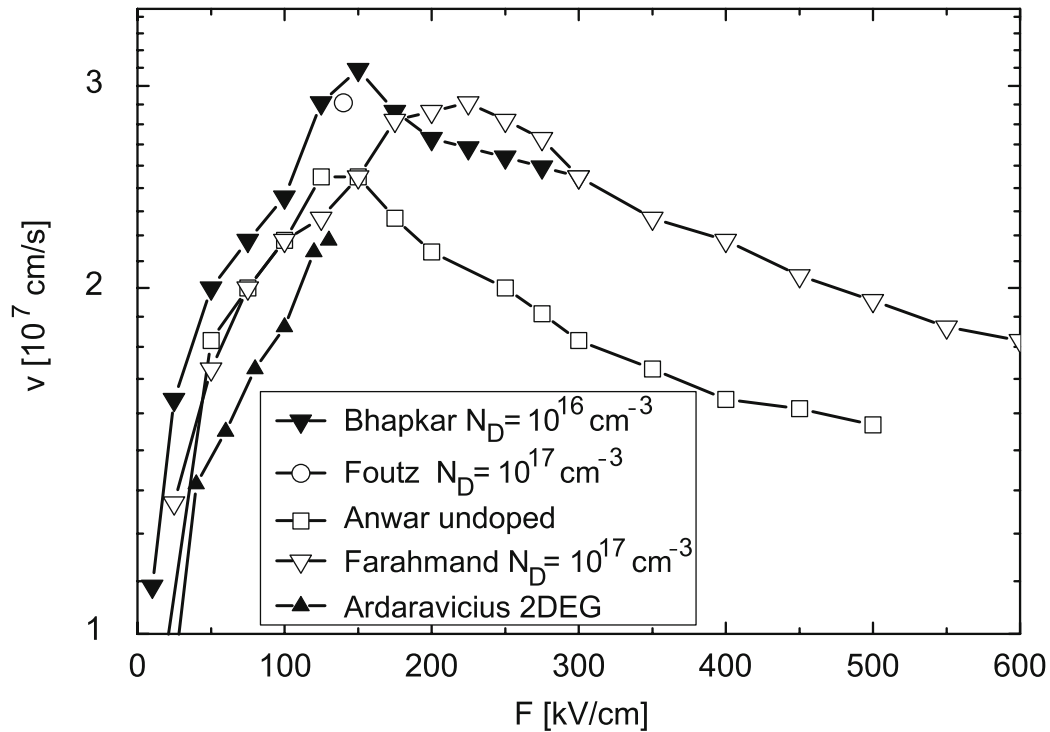


Fig. 2.7. Simulated velocity-field characteristics in bulk GaN by various authors

data of an AlGaIn/GaN DEG which includes the interaction of the nonequilibrium phonon taken from [2.19]. Hot phonons and hot-electron penetration into AlGaIn and GaN layers are responsible for the lower than expected drift velocity. Ensemble Monte Carlo calculations within the density functional theory of GaN and ZnS are given in [2.119]. Ab-initio band structure calculations are used. These simulations propose both lower peak velocities and no occurrence of the Gunn effect in GaN. Device simulations for heterostructures including the quantization effects in the channel are given in [2.46]. The saturation velocity used is as low as $1.2 \times 10^7 \text{ cm s}^{-1}$. The electron relaxation time amounts to 0.1 ps for all materials. Very good agreement of measured velocities and MC simulations can be obtained [2.30], as also given in Fig. 2.7. Measured saturation velocities of $2.5 \times 10^7 \text{ cm s}^{-1}$ and a critical field at 180 kV cm^{-1} are found for n-type bulk GaN. Peak velocities v_{peak} of $3.1 \times 10^7 \text{ cm s}^{-1}$ at an electric field of 140 kV cm^{-1} are reported for AlGaIn/GaN heterostructures. The obvious contradiction of several measurements and simulations will be discussed in the next section.

Velocity Measurements

Bulk and HFET MC simulations are not easily verified by experiment due to the sub-micron gate situation in FETs, the heterointerface situation in HFETs, and the strong field gradient near the gate [2.375]. Time-resolved electroabsorption measurements of the velocity-field characteristics in a bulk GaN pin-diode are presented in [2.500]. A time-of-flight technique is used. They predict a maximum electron velocity v_{peak} in bulk GaN of $1.9 \times 10^7 \text{ cm s}^{-1}$ and a saturation critical field of $E_{\text{crit}} = 225 \text{ kV cm}^{-1}$. The measured peak velocity v_{peak} is still slightly lower than the prediction of the MC analysis. Other extraction techniques lead to stronger deviations. Derived from delay time analysis of HFETs, the maximum effective electron velocity in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMTs, i.e., the quantized channel situation, with $l_g = 1.3 \mu\text{m}$ is found to be $1.2 \times 10^7 \text{ cm s}^{-1}$ in [2.5]. This is lower than the prediction of the MC simulations. Further extractions suggest that parasitic effects mask the real experimental effective velocity of $3.3 \times 10^7 \text{ cm s}^{-1}$ in a channel of AlGaIn/GaN HFETs [2.42], which is found when considering the parasitic effects. Without the consideration of R_S and R_D , an effective velocity of $1.3 \times 10^7 \text{ cm s}^{-1}$ is extracted. The influence of charge control (charge non-confinement or real-space transfer) at the heterostructure interface on carrier velocity is described in [2.462]. The source resistance R_S is found to be modulated in a nonlinear physical model. This modulation at high forward current I_D is correlated with the occurrence of space charge regions and carrier non-confinement from the channel to the barrier under the source contact. Determination of quantum scattering lifetimes by Shubnikov-de Haas oscillations and parallel conduction are given in [2.409]. A ratio of the classical scattering time to the quantum scattering time of 6.1/1 is observed. This ratio indicates what proportion of the lifetime is represented by large angle scattering vs. all

scattering events. The typical range found for the ratio for GaAs heterostructures is in the range 9–13 [2.409]. The results suggest that in addition to the optimization of the channel layers, also the parallel conduction in doped barrier layers has to be taken into account. With these considerations, all effects have been mentioned, which explain the inconsistency of measurements and simulations.

2.2.8 Polarization-Based Devices and Their Specific Properties

The strong polarization effects in III-N materials allow a number of special devices which are unique with respect to their properties. The first unique device is, of course, the classical III-N heterostructure FET, which yields extremely high channel carrier concentrations, even though there is no intentional impurity doping. For regular AlGaIn/GaN HEMTs, the direct effects of spontaneous and piezoelectric polarization effects on the output characteristics of AlGaIn/GaN HEMTs are discussed in [2.391]. The polarization critically influences the channel formation and thus also the output characteristics. The advantage of this paper is to show the direct correlation between device properties and polarization effects.

The high-dielectric constant of piezoelectric layers grown on top of a non-piezoelectric substrates can be effectively used in other electronic devices [2.338]. AlN [2.55] and GaN [2.242] surface-acoustic-wave (SAW) filters using the piezoelectric properties have been demonstrated. Epitaxially grown GaN piezoelectric thin-film SAW filters are grown on amorphous GaN buffers on sapphire. The low surface roughness of the material ensures good wave propagation while the good isolation between the electrodes ensure low electric losses. High-wave propagation velocities of $5,800 \text{ m s}^{-1}$ and low insertion loss of -7.7 dB are achieved [2.242]. The devices provide high fractional bandwidth and very low coefficients of frequency are obtained. Voltage controlled SAW filters on 2DEG AlGaIn/GaN heterostructures are demonstrated in [2.129]. The external voltage applied to transducer is used to minimize the insertion losses in this case. This technology is suggested for cointegration with GaN MMICs. Further sensor devices are discussed with the applications at the end of this chapter.

2.3 Electrical and Thermal Limitations of Materials and Devices

Several predictions are being used to estimate the ultimate performance of nitride-based materials and devices. This section summarizes the most important figures-of-merit used in the analysis to predict the ultimate performance for fully developed device technologies.

2.3.1 Physical Modeling of Devices

Nearly all available simulation approaches have been used to model and predict the performance of III-N semiconductors and semiconductor devices. These include basic material research to obtain the band structure by density functional approaches [2.119], basic transport considerations to perform MC simulations [2.517], device drift-diffusion, and hydrodynamic multidimensional modeling approaches [2.46, 2.48], Monte Carlo approaches for both materials and devices [2.15, 2.111], as well as compact device modeling approaches [2.183, 2.392].

Material Modeling for Polar Devices

Material modeling from basic properties to devices is described, e.g., in [2.49, 2.111]. The complexities that arise in Monte Carlo-based modeling of noncubic symmetry semiconductors and their related devices are discussed in [2.50]. Owing to the increased size and number of atoms per unit cell, the band structure is far more complex in noncubic than in zincblende-phase semiconductors. This leads to a greater number of bands, smaller Brillouin zone, and an increase in the number of band intersections. Example articles are provided in [2.15, 2.49, 2.111, 2.492]. The detailed material properties have already been discussed in this chapter.

Device Simulation Including Polarization Effects

III-N device simulation is not very different from approaches in other semiconductor systems [2.406]. A quasi-2D-modeling of GaN-based heterostructure devices including quantum effects is given in [2.392]. An optimized effective mass-approach is coupled to a quasi-2D-model for the current flow. The PICs are included as surface charge in the Poisson equation which is solved self-consistently with the Schrödinger equation. The idealized model predicts very high drain currents of 2.5 A mm^{-1} for an $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$ HEMT. On the HFET device level, full band Monte Carlo simulation of zincblende GaN MESFETs, including realistic impact ionization rates, are provided in [2.110]. The drain current in GaN MESFETs increases gradually with drain voltage V_{DS} . This is different from the impact ionization in GaAs MESFETs and it is related to the different impact ionization coefficients. Gate length scaling for $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$ HFETs by 2D-full band MC simulation including polarization effect is analyzed in [2.15]. The polarization effects are included by constant interface charges at the barrier ($-\sigma$) and channel interface ($+\sigma$). From this, a cut-off frequency $\times$ gate length product $f_{\text{T}} \times l_{\text{g}}$ of $16 \text{ GHz } \mu\text{m}$ can be deduced for a device with a gate length of 100 nm. The maximum predicted output power P_{out} amounts to 46 W mm^{-1} for a gate length $l_{\text{g}} = 0.9 \mu\text{m}$, and 20 W mm^{-1} for a 100 nm device. The simulated on-state breakdown voltages are 300 and 60 V, respectively. Several other approaches have been described to include strong polarization effects in device simulation. The

carrier-concentration-dependent electron mobility in an AlGaIn/GaN electron gas is analyzed by magnetoresistance and capacitance-conductance analysis in [2.185]. The effects of quantization are included in the mobility analysis. Scattering from interface states in AlGaIn/GaN heterostructures is correlated with the high polarization field in the heterointerface. At temperatures higher than 200 K polar optical phonon scattering dominates the transport, yet both interface charge and roughness affect the mobility at the low and high sheet carrier density. For the compact models, a detailed physically based compact HFET model which includes thermal effects is given in [2.6]. The gradual channel approximation is used based on parameters on MC simulation. The thermal compression of a AlGaIn/GaN device on sapphire substrate can be modeled very accurately. A theoretical study of GaN/AlGaIn HEMTs by a compact model including a nonlinear formulation of the polarization is given in [2.527]. The cut-off frequency, transconductance, and current-voltage characteristics are computed in good agreement to measurements. The effect of the nonlinear polarization model on the sheet carrier density is also presented. An electrothermal Monte Carlo method is used for the investigation of submicrometer GaN HEMTs in [2.393]. The polarization effects are included according to (2.19). Additionally, fixed negative charges can be included to simulate surface traps. Peak velocities of $6 \times 10^7 \text{ cm s}^{-1}$ are reached at the drain side of the gate for a gate length $l_g = 200 \text{ nm}$. The maximum electron energies are as high as 2 eV.

Devices: Field Shaping and Breakdown Management

In addition to basic evaluation studies such as the comparison of zincblende-phase GaN, cubic-phase SiC, and GaAs MESFETs using a full band MC simulator [2.492], field shaping [2.183] and high-breakdown design are the principal applications of device simulations [2.358]. Such approaches allow the estimation and increase of maximum breakdown voltage BV_{DS} , and thus of the maximum output power P_{out} . Examples can be found [2.418, 2.465]. The impact of strain engineering on device level is stressed in [2.47]. Two findings are stressed: first, there are little changes in the DC- and transient-characteristics even for large stresses in overlayers. This is based on the stiffness of nitride semiconductors. A second finding focusses on the relaxation of the AlGaIn. Piezoelectric polarization effects are more pronounced for devices with larger relaxation. Electric field shaping is presented in [2.358] for an AlGaIn/GaN HEMT using field plates. The geometry of a field plate is optimized for reduced field peaking in the channel by 2D-simulation. A closed-form expression for the drain voltage dependence of the electric field using field plate is discussed in [2.183]. Direct analysis of the reverse gate leakage current I_G is provided by 2D-simulation in [2.182]. The mechanisms of direct tunneling, direct tunneling through a thin layer, and trap-assisted tunneling are distinguished by their field sensitivity. This allows to fit measured gate currents for various devices by 2D-simulation.

2.3.2 Devices: Figures-of-Merit

Apart from more specific simulation approaches, the prediction of the ultimate performance of semiconductor devices has a long-standing tradition. A great number of predictions are available for the promising material system of III-N semiconductors. Instead of repeating these various predictions, see, e.g., [2.301, 2.396, 2.462, 2.463], this work systemizes the figures-of-merits (FOMs) and calculates some principal dependencies. A good overview and comparison of different approaches is also given in [2.72].

Early initial predictions for wide bandgap compound semiconductors for superior high-voltage unipolar power devices are given in [2.415]. As given in (2.47), Johnson's FOM describes the power frequency product per unit width [2.167]:

$$\text{FOM}_{\text{Johnson}} = \frac{(v_{\text{sat}} \cdot E_{\text{crit}})^2}{2\pi}. \quad (2.47)$$

In (2.47), E_{crit} denotes the critical dielectric breakdown field and v_{sat} the effective saturation velocity of the material. A more microwave-oriented FOM is provided by Eastman in [2.132]. It combines microwave power, e.g., at 10 GHz, with the transit frequency f_T and the capacitive input reactance X_c [2.132], and the saturation velocity, as given in (2.48) [2.97]:

$$\text{FOM}_{\text{Eastman}} = P_{\text{out}}(\text{Class-A}) \cdot f_{10\text{ dB}} \cdot R_L = 1.210^{23} \text{ W Hz}^2 \Omega. \quad (2.48)$$

$P_{\text{out}}(\text{Class-A})$ is the maximum output power in Class- A operation, $f_{10\text{ dB}}$ is the maximum frequency yielding 10dB of power gain, and R_L is the load impedance. This FOM is dedicated to the analysis of devices for the most important applications in high-power high-efficiency amplifiers. Wu [2.502] stated Baliga's FOM [2.26] as an efficiency measure for GaN HEMTs:

$$\text{FOM}_{\text{Baliga}} = \mu \cdot E_{\text{crit}}^2, \quad (2.49)$$

where again E_{crit} denotes the critical dielectric breakdown field and μ denotes the carrier mobility. High-efficiency devices have high-breakdown voltages (high E_{crit}) and low-access resistances (high mobility μ). The access resistances of III-N devices are typically higher, while the critical fields are significantly higher than in other fast semiconductors. This allows for efficient devices. Another FOM suggests maximizing the product of charge density n_{channel} and mobility μ to maximize gain and eventually, the current gain cut-off frequency f_T :

$$\text{FOM}_{\text{Gain}} = \mu \cdot n_{\text{channel}}. \quad (2.50)$$

Derived from this the channel charge density n_{channel} itself can also be maximized, as given in (2.51):

$$\text{FOM}_{n_{\text{channel}}} = n_{\text{channel}}. \quad (2.51)$$

Derived from (2.51), III-N HEMTs have a tremendous advantage in sheet carrier density as compared to other materials, while the absolute amount

Table 2.29. Properties relevant for low-noise applications for different HEMTs with a gate width $W_g = 2 \times 60 \mu\text{m}$ and a gate length $l_g = 150 \text{ nm}$

Material (–)	$N_{F,\min}$ at 10 GHz (dB)	G_{ass} at 10 GHz (dB)	BV_{DS} (V)	FOM _{LNA}	Ref.
GaAs PHEMT	0.5	14	6	168	[2.474]
InAlAs/InGaAs HEMT	0.3	16	4	213	[2.335]
AlGaIn/GaN HFET	0.6	12	50	1,000	[2.220]

of carriers in the channel is not considered. Further, both (2.50) and (2.51) do not consider any breakdown issues, so an optimization only according to these FOM can be misleading, as the optimization may deteriorate breakdown, e.g., due to on-state channel breakdown. Fig. 2.8 illustrates Johnson's FOM, whereas Fig. 2.9 shows the channel Hall mobility versus charge carrier density as compared to values reported in the literature. As can be seen III-N HEMTs provide much higher sheet carrier densities for similar mobility values, as compared to GaAs HEMTs. A FOM from a thermal point of view is provided by Shenai et al. in [2.415]:

$$\text{FOM}_{\text{Shenai}} = \kappa_L \cdot \sigma_A E_{\text{crit}}. \quad (2.52)$$

In this case, κ_L is the thermal conductivity of the material in the heat-flow path (both semiconductor, substrate, and appropriate transition), σ_A is the electric drift-region-conductance per unit area in the semiconductor, and E_{crit} is the dielectric breakdown field. In terms of heat conductivity and conductance per unit area, III-N materials such as GaN and AlN are in the same order as Si, while the peak electric field at breakdown is significantly higher for III-N materials. For low-noise applications, the following FOM can be used, as defined by Nguyen in (2.53):

$$\text{FOM}_{\text{LNA}} = \frac{G_{\text{ass}} \times BV_{\text{DS}}}{N_{F,\min}}. \quad (2.53)$$

Table 2.29 compares the minimum noise figure $N_{F,\min}$, the associated gain G_{ass} , and the breakdown voltage BV_{DS} for a heterojunction FET with a gate width $W_g = 2 \times 60 \mu\text{m}$ and a gate length $l_g = 150 \text{ nm}$. In this comparison, the linear impact of the breakdown voltage in (2.53) favors the AlGaIn/GaN HEMT very much, while the actual low-noise performance is not outstanding. This FOM is thus suitable for applications which require both low-noise performance and extreme robustness.

2.3.3 III-N Devices: Frequency Dispersion

AlGaIn/GaN HEMTs are found to be highly frequency-dispersive and did not yield the expected output power, especially in the beginning of device development, e.g., in [2.206]. Newer publications, e.g., [2.219], announced

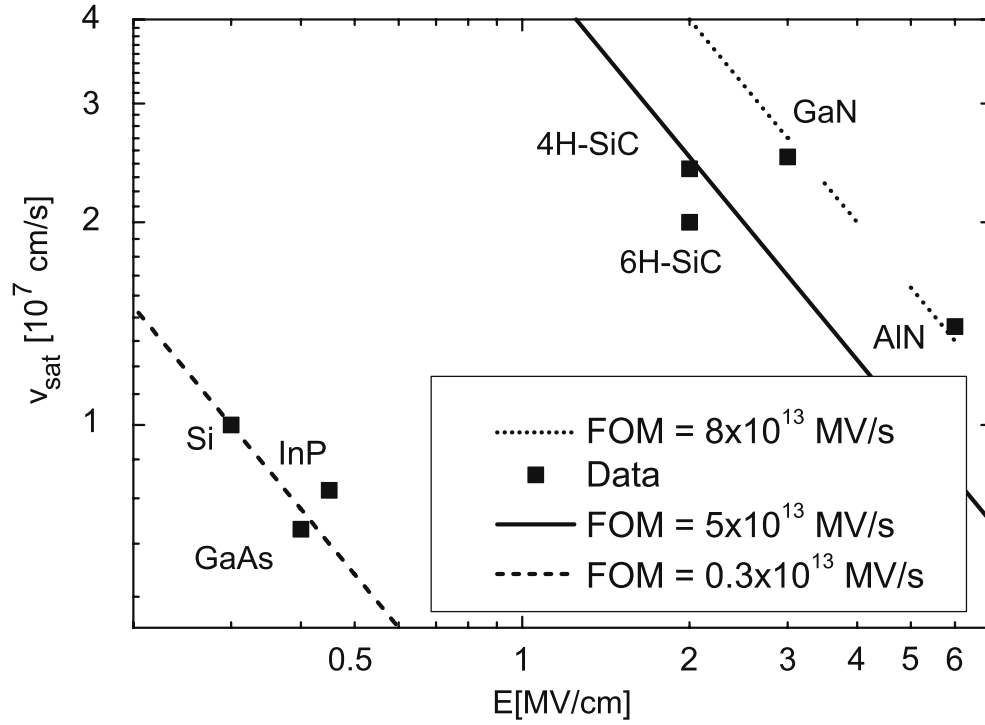


Fig. 2.8. Johnson's figure-of-merit in the E_{crit} vs. v_{sat} diagram

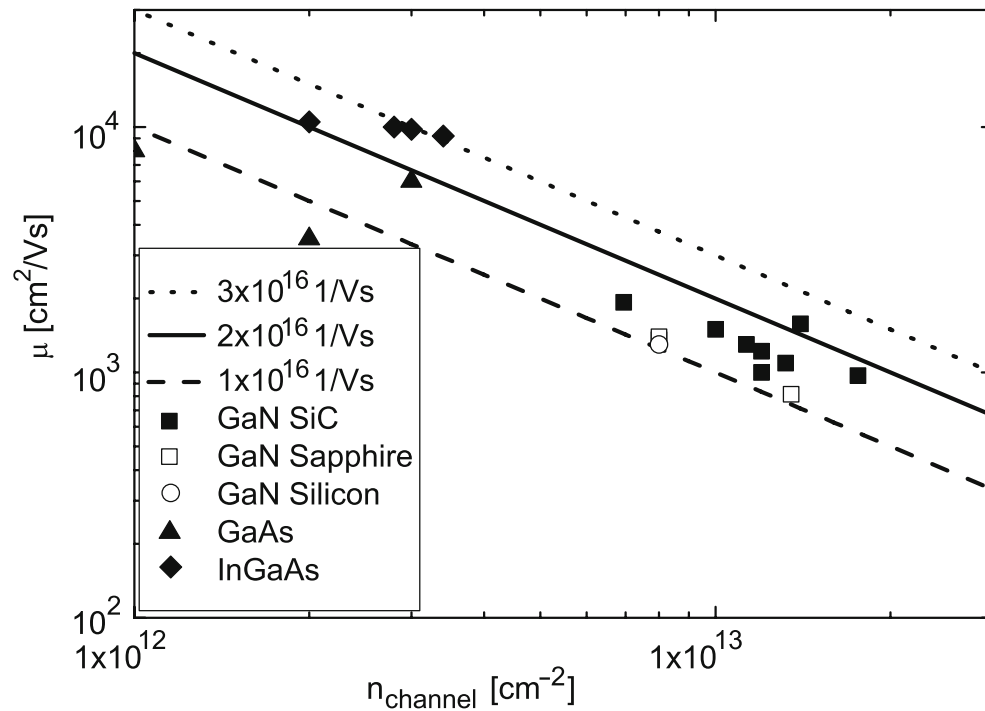


Fig. 2.9. Channel Hall mobility as a function of sheet charge carrier density n_{sheet} in GaN, GaAs, and InGaAs

dispersion-free devices and have to be taken with some caution; however, a lot of knowledge has been acquired for the reproducible control and reduction of dispersion. These results are discussed in more detail in Chapter 4. The aspect of performance degradation through dispersion, as described later, can be taken further. Related reliability issues are analyzed in Chapter 7.

Properties of GaN Semiconductors in Favor of Dispersion

One could ask why dispersion effects are so much correlated with III-N devices. In the GaAs and InGaAs material systems, frequency dispersion has been discussed in detail [2.51] but has not been found that crucial relative to the performance actually expected. In comparison to GaAs MESFETs, to (In)GaAs HEMTs, and other related devices, the physical origins of frequency dispersion in III-N HEMTs are more pronounced due to:

- Very high surface charge densities $n_{\text{sheet}} \geq 10^{13} \text{ cm}^{-2}$
- Lattice-mismatch of semiconductor materials relative to the heterosubstrates
- The relatively high concentration of threading dislocations and other defects due to high epitaxial growth temperatures up to 1,100°C and high growth temperature gradients within the growth process
- The small absolute channel charge relative to the overall possible carrier charge in the whole device including buffer and nucleation layers

In the III-N material system vertical instead of lateral devices have also been realized, such a current aperture vertical electron transistors (CAVETs), e.g., in [2.516], which show reduced dispersion relative to the lateral devices, such as GaN MESFETs and HEMTs.

Observation of Dispersion

In a large number of publications, the following experimental findings are attributed to frequency dispersion; see, e.g., [2.206, 2.480, 2.535]. These include:

- Current collapse; i.e., the difference of continuous-wave (cw) currents measured from different quiescent bias, or a pronounced negative output conductance, which occurs even in devices with small gate width and is not primarily caused by thermal effects [2.336, 2.480]
- DC-current dispersion; i.e., the difference of cw-DC- or pulsed-DC from different quiescent bias [2.480, 2.483]
- Time dependence of the DC-device currents with time constants and related frequencies between the Hz and 100 MHz range [2.209, 2.483]
- RF-current slump; i.e., the difference of DC- and extracted RF-device current characteristics
- A (bias-dependent) shift of the threshold voltage
- RF-power slump; i.e., the reduction of the output power caused by RF-current slump [2.206]

- Premature power and gain compression [2.130]
- Gain reduction through a second virtual gate and thus possible gate length extension

The effects are certainly related, e.g., the RF-power slump in this enumeration is caused by the RF-current slump, i.e., reduction of $I_{DS,RF}$. The above-mentioned current reduction effects intermix with device degradation mechanisms. The suppression of dispersive effects is analyzed in Chapter 3 and Chapter 4. Further, the impact on performance issues and modeling of dispersion is discussed in Chapter 5 and the degradation-related issues are discussed in Chapter 7.

2.4 Substrates for Electronic Devices

Wide bandgap semiconductor substrates are components critical to the system electronics industry. The availability of affordable, freely available, large-diameter, high-quality substrates will heavily influence the final system introduction of wide bandgap devices and MMICs into systems. Good overview articles on the present status are available, e.g., in [2.9, 2.41].

2.4.1 Criteria for Substrate Choice

The following properties of substrates are evaluated in this book:

- Lattice-mismatch relative to the materials of the device layers
- Thermal conductivity κ_L and coefficient of thermal expansion (CTE)
- Maximum electrical isolation (at different temperatures)
- Price and price per area [2.41]
- Availability with respect to diameter (2–8 in.)
- Crystal quality and residual defect density [2.103]
- Surface properties and residual defects density [2.267]
- Wafer warp and wafer bowing [2.341]
- Mechanical and chemical properties with respect to thinning and viahole etching

Table 2.30 gives an overview of the most important physical properties of the substrate materials under consideration for III-N devices. These include lattice-mismatch, thermal conductivity, CTE, and isolation. Some aspects of Table 2.30 are discussed in detail. GaN is a very suitable substrate material choice; however, neither conducting nor semi-insulating GaN substrates are so far available in sufficient diameter and quality [2.106, 2.328]. Some promising results are mentioned in [2.384, 2.385]. GaN substrates can be either produced by growth on a foreign substrate or by a boule growth technique. 3-in. GaN grown by HVPE on sapphire substrates are reported in [2.80]. The situation is similar for AlN, which has also a very good thermal conductivity [2.404]. The thermal conductivity of SiC is outstanding. Due to growth conditions

Table 2.30. Basic properties of substrate and III-N semiconductor materials

Material	Lattice constant a (Å)	Mismatch to GaN (%)	κ_L (W m ⁻¹ K ⁻¹)	CTE (10 ⁻⁶ K ⁻¹)	Isolation (Ω cm)	Ref.
GaN	3.189	0	130	5.59	≥10 ⁹	[2.341, 2.384]
6H SiC	3.08	3.4	490	4.2	≥10 ¹¹	[2.341, 2.384]
6H s.i. SiC	3.08	3.4	370	4.2	≥10 ¹¹	[2.341, 2.384]
Sapphire	4.758/√3	13	50	7.5	—	[2.123]
Silicon	5.4301	17	150	3.59	1–3 10 ⁴	[2.341]
AlN	3.112	1	200	4.2	≥10 ¹²	[2.341, 2.384]

and potential doping, the thermal conductivity of semi-insulating (s.i.) SiC can be reduced relative to pure crystalline SiC. The suitability of sapphire is strongly reduced due to its low thermal conductivity. All other substrate options except sapphire have a better thermal conductivity than GaN. Sapphire, even if thinned to 50 μm, reduces the reported power densities of devices in cw-operation to values of GaAs PHEMTs, e.g., in [2.16]. The difference in CTE of substrates and semiconductor materials affects both material growth and device reliability, because of the strain in the material. The maximum substrate isolation will further define the need to grow additional insulating semiconductor layers in the device. This will affect the attenuation of passive lines. For AlN, GaN, and SiC, the isolation has been developed to levels ≥10⁹ Ω cm at RT. Once the epitaxial layers are grown, one of the most critical consequences of the lattice-mismatch is the resulting bow of the wafer. Based on the data given in Table 2.30, an approximative scaling rule for the wafer bow is suggested in [2.341]:

$$W \approx t_{\text{sem}} \cdot d_{\text{sub}}^2 / t_{\text{sub}}^2. \quad (2.54)$$

Equation (2.54) formulates a relationship between the substrate diameter d_{sub} , the epitaxial layer thickness t_{sem} , and the substrate thickness t_{sub} based on a given bow, known, e.g., for given substrate and epitaxial thicknesses, and diameter. For a typical thickness of up to 4 μm for the epitaxial layers and a 2-in. wafer of a given thickness, a bow of 10 μm results. For a 4-in. wafer of the same thickness, this results in a bowing of 40 μm, which is close to the maximum tolerances of an optical stepper, as mentioned in [2.341]. This is mentioned here, as the bowing has to be accounted for during gate alignment and with respect to the mechanical stress during backside processing. The issues of properties, present availability, and crystal quality are discussed in the next sections for every type of material.

2.4.2 Silicon Carbide Substrates

Semi-insulating silicon carbide is one of the most attractive substrate materials for electronic applications, due to the favorable combination of lattice-

mismatch, isolation, and thermal conductivity [2.9, 2.427]. It is available with increasing quality and diameters up to 4 in. [2.385]. Both polytypes 4H- and 6H-s.i. SiC are used. On the contrary, III-N optoelectronic applications use conductive SiC substrates [2.387] with similar diameters. Most of the outstanding electronic device results have been reported on semi-insulating SiC materials, e.g., [2.362].

Currently, the greatest amount semi-insulating SiC material is produced by Cree [2.427]. The growth method is based on physical vapor transport deposition (PVT). There is a number of other vendors for semi-insulating material, e.g., such as II-VI [2.103, 2.273] and Toyota in [2.320].

Norstel/Okmetic developed a high-temperature CVD (HTCVD) method for the growth of s.i. SiC substrates. II-VI produces undoped 2- and 3-in. 6H-SiC grown by PVT [2.14, 2.103, 2.273]. Detailed examples are given in [2.78, 2.159, 2.484]. Both growth methods PVT and HTCVD result in different substrate properties, e.g., with respect to residual mobility [2.246]. For conductive material, several vendors are available, e.g., [2.159, 2.359, 2.424].

A number of issues remain for the growth of SiC, so a comprehensive substrate analysis is still necessary. These issues include:

- Control and reduction of average micropipe defects density [2.427]
- General defect reduction, such as polytype inclusions and Si segregation [2.103, 2.274]
- Subsurface damage removal [2.273]
- Surface polishing to reduce average roughness [2.433]
- Availability of 2–6-in. wafers of increased and homogenous quality, e.g., [2.360]

Substrate isolation at RT is not considered a problem for SiC anymore, as levels beyond $10^9 \Omega \text{ cm}$ at RT have been repeatedly reported [2.384]. This argument needs to be refined for high-temperature operation, as the substrate isolation mechanism is strongly temperature-dependent depending on the isolation method [2.529]. The availability of 4–6 in. diameters is desirable as most of the current GaAs fabrication lines are operated with these diameters.

SiC Substrate Characterization

Micropipes have been considered as the main obstacles for high quality SiC substrates and have attracted much attention for the definition of substrate quality, e.g., [2.103]. Micropipes are screw defects with a large Burger's vector which stretch through the complete crystals during bulk growth. Fig. 2.10 gives an optical image of a micropipe in a codoped semi-insulating SiC substrate. Polytype-control and background impurity control are of ultimate importance. Roughness is another criterion for substrates. Fig. 2.11 gives a microimage of a single micropipe for a surface with a residual roughness of 3 nm. Contrary to Fig. 2.11, Fig. 2.12 gives a microimage of a surface with a roughness $\text{RMS} = 0.3 \text{ nm}$. The average micropipe density has been reduced

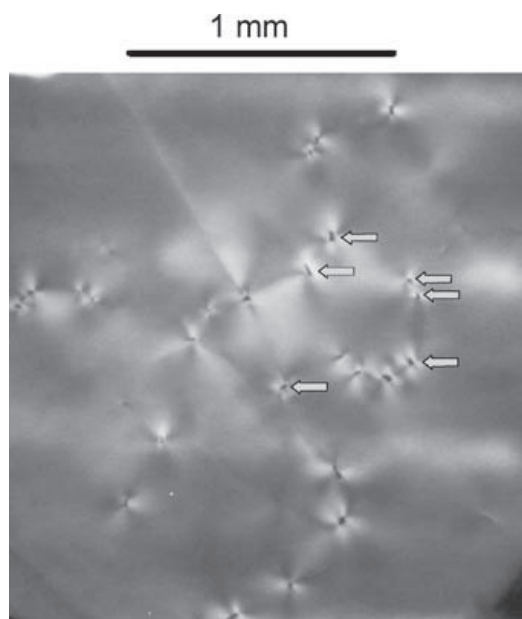


Fig. 2.10. Optical image of a micropipe cluster in s.i. SiC

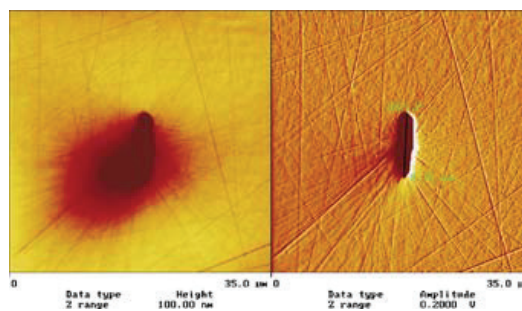


Fig. 2.11. AFM image of a micropipe in s.i. SiC, RMS = 3 nm

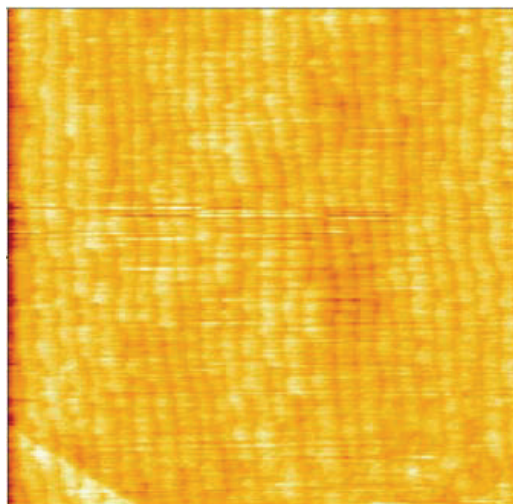


Fig. 2.12. AFM image of a CMP-polished surface of a s.i. SiC, RMS = 0.3 nm

constantly during the substrate development, e.g., [2.384]. However, since micropipes define a killing defect for any active [2.28] and most passive devices (see Chapter 8), such as MIM capacitances, their average reduction is crucial, especially when increasing substrate diameter [2.433]. Filling micropipes by epitaxial growth is nearly impossible due to the typical geometry depicted in Fig. 2.11. Other dislocations than micropipes [2.103, 2.159] have an impact on material quality and on device performance. This is mainly due to the fact that they serve as nucleation centers for other defects in the epitaxial layers [2.274]. Basal-plane as well as screw dislocations have been found by high-resolution X-ray diffraction and synchrotron white beam topography in 4H-SiC [2.159]. The transformation mechanism of threading edge dislocations in the substrate into the epitaxial layer is discussed.

Subsurface damage [2.273] and grain boundaries, especially in the periphery of the crystals, are of significant importance for III-N device performance. Subsurface damage is not visible to some characterization methods. It becomes visible, e.g., after significant thermal or chemical treatment [2.103, 2.174]. The subsurface damage can be removed by the application of chemical-mechanical polishing, as reported in [2.174]. For the final substrate, several characterization methods are possible. Fig. 2.13 gives a comparison of two optical polarization images of 3-in. s.i. SiC substrates for the analysis of overall surface quality. The right image depicts a very good wafer, while the left wafer depicts a mediocre quality. Several other substrate characterization methods are applied. The polarized light microscopy (PLM) method is further explained in [2.267]. The procedure allows a fast method to analyze micropipe (clusters), screw dislocations, and domain boundaries. The wafers can further be analyzed with and without epitaxial layers in order to investigate the defect propagation into the epitaxial layers. Micro-Raman can be used for topography of SiC crystals

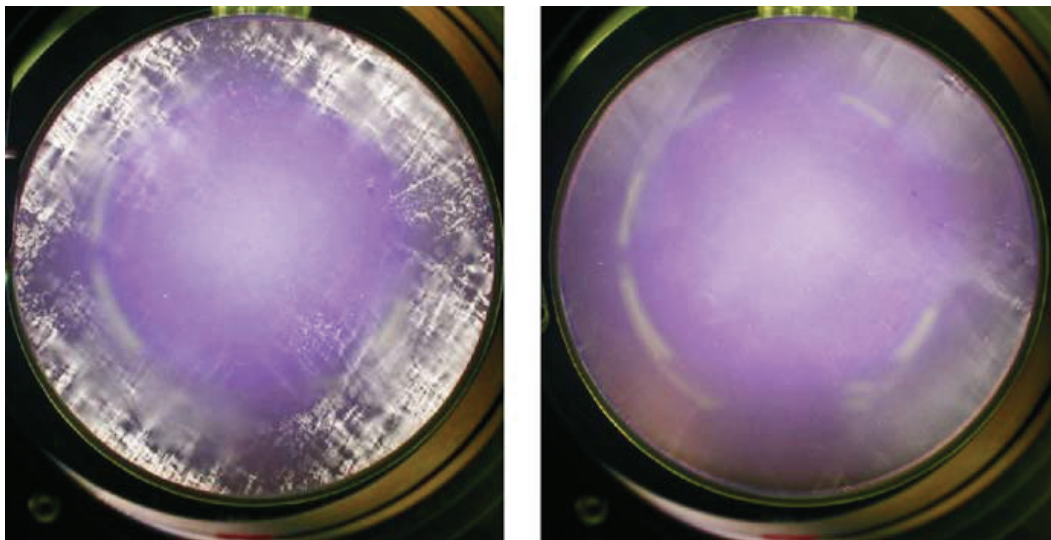


Fig. 2.13. Optical polarization images of two 3-in. s.i. SiC wafers

with a spatial resolution of $1\text{ }\mu\text{m}$ [2.274]. Further, X-ray topography allows detailed analysis of the defect, as is performed, e.g., in [2.204]. The issues now are discussed with the respective substrate growth method.

Doped Conducting SiC Substrates in Electronic Applications

Doped conducting substrates are readily available by several industrial vendors for optoelectronic applications, e.g., [2.41]. N-type SiC substrates are ten times more cost-efficient than semi-insulating substrates and are presented, e.g., in [2.103, 2.316]. The conductivity is achieved by impurity doping with nitrogen. However, there are also significant demonstrations of high-power AlGaIn/GaN HEMTs for electronic applications, e.g., [2.174] on n-doped SiC substrates using $\approx 10\text{ }\mu\text{m}$ -thick HVPE-based AlN interlayers. Very uniform device performance is given on this quasi-semi-insulating substrate approach. Further AlGaIn/GaN HEMTs on p-type 6H-SiC substrates are given in [2.368]. Very high current levels $I_{\text{Dmax}} \geq 1.4\text{ A mm}^{-1}$ and a cut-off frequency of 53 GHz are reported for devices with a gate length $l_g = 0.25\text{ }\mu\text{m}$.

Semi-Insulating Codoped Substrates

For semi-insulating substrates with isolation levels of $\geq 10^6\text{ }\Omega\text{ cm}$ [2.83, 2.384], two basic mechanisms are used to obtain substrate isolation. In a first approach, SiC substrates are compensated by codoping, typically with vanadium [2.484]. The substrates suffer from the limited solubility of vanadium in SiC [2.433]. The following substrate properties result from the codoping:

- The deep traps activate at high-operation voltages and degenerate the performance of SiC MESFETs [2.484].
- Vanadium codoping degrades bulk crystal quality due to increased local stress.
- The micropipe density increases due to the codoping [2.535].
- Codoping reduces lattice thermal conductivity by about 25% [2.83].

High-Purity Semi-Insulating (HPSI) Substrates

The negative effects of the codoping in s.i. SiC were discovered during SiC MESFET development, as discussed, e.g., in [2.433, 2.484]. SiC MESFETs on codoped substrates did not reach the expected power levels, which led to the development of undoped intrinsically compensated semi-insulating substrates. In this second approach, undoped high-resistivity or high-purity semi-insulating substrates (HPSI) [2.9, 2.294] with diameters up to 4 in. are under development with micropipe densities as low as 35 cm^{-2} . They promise the following properties [2.294]:

- Increased uniformity suitable for MMIC processes
- Increased resistivity and isolation

- Increased thermal conductivity [2.83]
- Reduced dispersive effects in the devices

However, in comparison to conducting SiC substrates, a smaller growth parameter window also has to be taken into account [2.535] for the growth of HPSI SiC substrates.

SiC Wafer-Size Scaling

Much of the III-N device results are so far achieved on 2-in. and 3-in. substrates. 3-in. s.i. SiC substrates are available with similar or improved quality relative to the 2-in. wafers [2.384]. Apart from the obvious cost improvement, wafer scaling is extremely desirable, as the history of GaAs has shown that uniformity of the devices eventually increases with increased substrate diameter, e.g., [2.446]. Further, equipment considerations are relevant, as most of the III-V processing facilities today are based on 4–6-in. equipment, which makes 2 and 3-in. processing a very cumbersome and expensive task. Four inch wafers with improving quality have been announced repeatedly [2.360,2.385] and first production of GaN HEMT on 4-in. s.i. SiC substrate has been demonstrated.

2.4.3 Sapphire Substrates

Sapphire is a promising material due to the availability of cost-effective 2–4-in. diameter substrates [2.148]. It is widely used for development issues of electronic devices, and despite the lattice-mismatch, very impressive power densities of $\geq 12 \text{ W mm}^{-1}$ and high-pulsed-output powers have been achieved [2.16,2.66]. In addition to the adaption of the epitaxial parameters, the following substrate-related device issues have to be solved:

- General thermal management due to the reduced thermal conductivity
- Full wafer thinning:
 - Mechanical treatment of this hard material in the course of the thermal management, e.g., thinning from 500/250 μm to 50 μm as suggested in [2.16]
 - Impact of substrate quality during backside process
 - Wafer breakage due to the aforementioned issues
- Mismatch-induced stress and wafer bowing of thinned sapphire substrates due to the high lattice-mismatch to GaN
- Processing issues, e.g., in lithography due to the high substrate-related wafer bowing [2.16]

On the device level, results for AlGaN/GaN HEMTs on 4-in. sapphire substrates are given in [2.20]. The epitaxial growth gives a relatively high standard deviation of $>4\%$ for the Hall mobility. However, the high standard deviation can be well correlated with the standard deviation of the device parameters. The power performance of AlGaN/GaN HEMTs on sapphire substrate at 4 GHz is discussed in [2.478]. Power levels of 5 W mm^{-1} are reached at 2 GHz.

The epitaxial structure exhibits a thickness of $\geq 3\mu\text{m}$. Using an additional HVPE-grown buffer on sapphire substrates, the uniformity of DC- and RF-performance of MBE-grown AlGaIn/GaN HEMTs is analyzed in [2.125]. The fast growth of a GaN buffer layer by HVPE is combined with MBE epitaxial layer growth on 2-in. wafers. The DC-parameters of 258 devices, such as threshold voltage and transconductance show very low standard deviation.

2.4.4 Silicon Substrates

Because of quantity of its use and its economic importance, silicon is the most important semiconductor and substrate material. Thus, the use of silicon as a substrate material is desirable, mostly for cost efficiency reasons. However, the use of silicon also introduces a number of critical issues and engineering challenges for III-N devices, as enumerated below:

- The impact of the lattice-mismatch relative to GaN with respect to material defects, quality, and device reliability [2.169].
- The difference in the thermal expansion coefficients, especially for high-power operation [2.328] (of similar gravity with respect to reliability, but not so often mentioned).
- The availability and cost of 2–6-in. insulating silicon substrates with isolation levels of 10–30 k Ω cm.
- The RF-transmission-line losses of passive lines for RF-frequencies [2.109].

The lattice-mismatch to III-N material in principle is a disadvantage; however, the substrate quality of silicon with respect to defects is outstanding compared to, e.g., SiC. Silicon substrates are virtually defect free, which helps a lot with device reliability [2.306]. To overcome the silicon issues, some very interesting epitaxial procedures have been developed, e.g., [2.168, 2.333], as will be described in Chapter 3. On the device level, AlGaIn/GaN HEMTs on (111) silicon substrates are demonstrated, e.g., in [2.161, 2.162]. Very high power densities on silicon-substrates are reported by Triquint at 10 GHz [2.94, 2.109] and Nitronex at 2 GHz [2.52, 2.169]. Microwave and noise performance of 0.17 μm AlGaIn/GaN HEMTs on (111) high-resistivity silicon substrates are reported. A minimum noise figure $N_{F,\min}$ of 1.1 dB is reported with an associated gain $G_{\text{ass}} = 12$ dB at 10 GHz in [2.296]. The power density is 1.9 W mm $^{-1}$ at 10 GHz [2.295, 2.297], while the PAE is only 18%. Promising reliability results for GaN HEMTs on silicon substrate have been given in [2.94] and [2.333] and are detailed further in Chapter 7.

2.4.5 GaN and AlN Substrates

Native GaN and AlN substrates have been only recently developed and used for electronic applications, although they are most important for optoelectronic applications. However, native substrates face increasing attention to the expected improvement in electronic device reliability, e.g., [2.73]. For native

substrates, the lattice-mismatch is fully eliminated as compared to the heterosubstrates.

GaN Substrates

GaN substrates are only recently available in n-conducting and semi-insulating form with diameters suitable for electronic device fabrication, i.e., in 2-in. format. Free-standing GaN substrates are available based on two growth processes. First of all, GaN templates on sapphire can be used to reduce the defect density for optoelectronic devices, e.g., [2.33, 2.140]. The defect density is $8 \times 10^7 \text{ cm}^{-2}$ for this kind of technique for a $10 \mu\text{m}$ layer grown by MOCVD. This kind of quasibulk approach can be used in a variety of ways, e.g., ELO or related approaches. In some approaches, the host substrate such as sapphire is removed leaving free-standing GaN. The second method is the growth of GaN boules, e.g., in [2.137, 2.328] by HVPE. Si-based n-doping is used for conductive substrates, while Fe doping is used to obtain s.i. substrates. Free-standing GaN substrates based on a similar procedure are provided by Sumitomo, e.g., in [2.140]. Impressive results of AlGaN/GaN HEMTs on free-standing GaN substrates have been demonstrated, e.g., in [2.73, 2.106]. The GaN substrates are fabricated by HVPE and are Fe-doped to achieve a resistivity of $10^6 \Omega \text{ cm}$. The homoepitaxy changes the defect situation in the buffer completely, which makes these devices potentially more reliable. From an electronic device perspective, nitride devices are mostly unipolar devices. The bipolar devices face a number of substantial technological drawbacks, as described in Subsect. 2.5.6. Thus, the lattice-mismatch is relatively less important so far. In order to compare the impact of the crystal lattice constant and crystal quality, Fig. 2.14 gives the reported residual dislocation defect concentration as a function of the substrate lattice-mismatch relative to GaN for various substrate options. Fig. 2.14 shows, that only bulk GaN or ELO techniques (i.e. quasibulk GaN approaches) can provide the very low defect densities required especially for optoelectronic (laser) devices, whereas GaN electronic devices are typically grown with defect densities of 10^8 – 10^9 cm^{-2} on various substrates.

AlN, ZnO, and Diamond Substrates

Native AlN substrates are also under discussion for optoelectronic applications [2.107, 2.403, 2.404, 2.407]. AlN itself is highly resistive and has a better thermal conductivity than GaN, actually the thermal conductivity is very similar to SiC. Further, compared to all other nonnative substrates, it has the lowest lattice-mismatch (Fig. 2.14). For the use of AlN for GaN-based lasers even the residual mismatch of the AlN relative to GaN lattice constant is too high to provide reliable GaN lasers without the use of additional concepts such as epitaxial regrowth techniques (ELO) to reduce the defect concentration [2.321]. This defect concentration of epitaxial layers grown on AlN substrates by migration enhanced MOCVD amounts to mid 10^6 cm^{-2} . However,

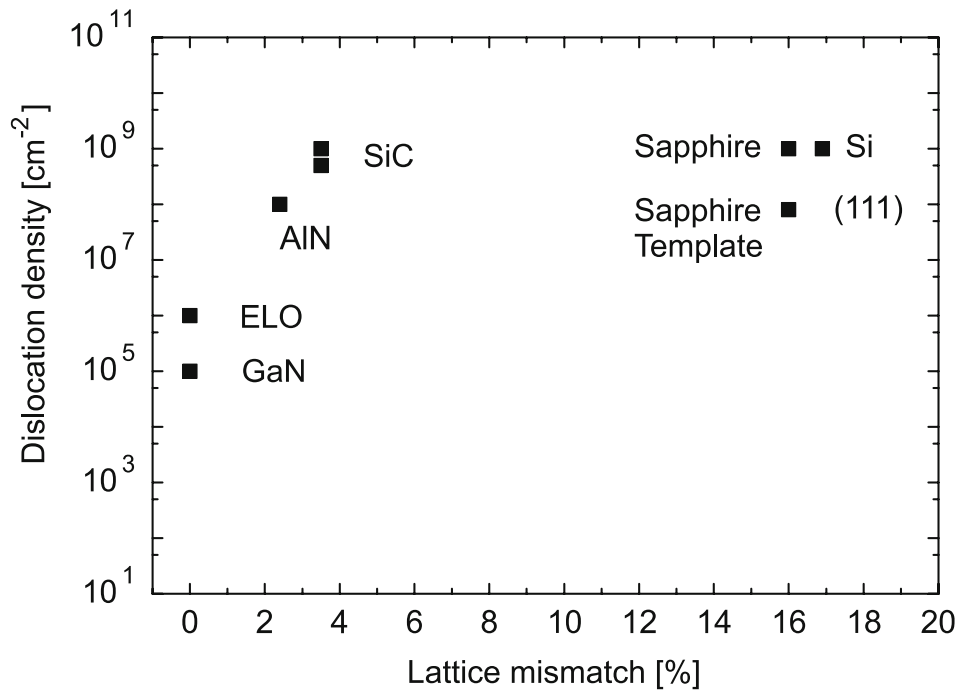


Fig. 2.14. Dislocation density as a function of lattice-mismatch relative to GaN

deep ultraviolet lasers are becoming feasible with the availability of a native substrate [2.404]. Free-standing AlN substrates with a thickness of 112 μm based on an Si(111) host substrate have recently been reported [2.224]. The boule growth of AlN by sublimation–recondensation is described as a growth method of the AlN substrates, e.g., in [2.404, 2.407]. High-purity AlN ceramics is sublimed in nitrogen atmosphere and recondensed on a seed substrate. GaN/AlGaN HEMTs on AlN substrate have been realized as reported, e.g., in [2.151]. The substrate diameter is so far limited; however, AlN substrates may enable more growth orientations and reduce the need of complex strain engineering. Electronic HEMTs on 30 μm -thick intermediate AlN layers grown by HVPE on SiC substrates are reported in [2.239]. The reduction of the gate-lag without surface passivation is attributed to the reduced amount of surface states related to dislocations and other defects. 10 μm -thick AlN layers are used in [2.174] to isolate conductive SiC substrates from the device. This approach is potentially a very low cost solution combining the advantageous thermal conductivity and isolation of AlN/SiC with a conductive low-cost substrate.

Further extending the material choices for substrates, wurtzitic zinc oxide (ZnO) materials and substrates are now available as large single crystals. For the optoelectronic applications, it is attractive due to a lattice-mismatch relative to GaN of only 2% and a large exciton binding energy of 60 meV. An overview of ZnO as a semiconductor material is described, e.g., in [2.257]. Next to the native substrate, also a developed wet-etch chemistry is available for ZnO as compared to the III-N. The advantages for electronic devices are

the high breakdown fields and the high saturation velocity. CVD diamond provides the highest thermal conductivity of any potential substrate material. Recent reports in [2.165] provide AlGaIn/GaN HEMTs on diamond substrate. The devices are initially grown on Si substrate and then transferred to the CVD diamond via an atomic attachment process. The devices are found to be relatively dispersive and the beneficial impact of the improved heat removal cannot be clearly demonstrated.

2.5 State-of-the-Art of Devices and Circuits

Numerous overviews on nitride devices and research issues are available due to its dynamic development, e.g., [2.353, 2.361, 2.401, 2.455, 2.464]. General overviews of GaN/AlGaIn heterostructure devices for photodetectors and field-effect transistors are given, e.g., in [2.96, 2.301, 2.422, 2.465]. General properties of undoped AlGaIn/GaN HEMTs for microwave power amplification are discussed in [2.96]. Early reports of AlGaIn/GaN HEMTs can be found, e.g., in [2.190], while initial reports for GaN MESFETs can be found in [2.418]. Although it is impossible to provide a full picture of all the achievements, a systematic overview of the published key issues, to the best of the author's knowledge, is given in the following. Some of the results may be outdated quite soon; however, the story of the development is highlighted.

2.5.1 Nitride-Based Diodes

GaN Diodes

Nitride-based diodes are attractive due to their high breakdown voltages in combination with high-carrier velocities leading to higher conversion efficiencies [2.76] and improved temperature performance. Possibly GaN also provides the material property of negative feedback leading to Gunn oscillations, as discussed, e.g., in [2.408]. A theoretical discussion of GaN diodes with respect to negative differential resistance is provided in [2.8]. Simulation results for the operation of wurtzite and zincblende GaN Impact Avalanche Transit Time (IMPATT) diodes are given in [2.8, 2.363]. Further, the possibility of high-frequency operation at D-band (140–220 GHz) of GaN-based IMPATT diodes is discussed in [2.8].

SiC-Based Diodes

SiC diodes serve as a reference and target high-speed high-power density switching applications, e.g., [2.387]. They are applied for switch-mode power supplies, e.g., in computer servers [2.359]. Though the overall numbers of SiC Schottky diodes produced so far are very small relative to the mass market of silicon diodes, the high power density, the low R_{on} [2.494], and the high-temperature operation provide very interesting niche markets. Commercial

SiC diode process of Cree in [2.368, 2.427] and Infineon [2.434] are available with strong research efforts underway on circuit and application level, e.g., [2.366, 2.434]. The reduction of the reverse recovery current during conversion and the improvements in conversion efficiency relative to Si diodes are mentioned, especially at frequencies beyond 100 kHz. SiC diodes are further discussed for the replacement of converters in hybrid car power-conversion applications [2.359].

2.5.2 Power Electronics

III-N wide bandgap semiconductors are unique with respect to power electronics from low frequencies to the RF-domain. The motivation for the use of III-N-based diodes [2.76] and FETs [2.397] stems from their increased switching speed and thus their conversion capabilities and more efficient transmission and distribution of electric power at increased operation temperatures, e.g., [2.334]. The target is the development of a technology for fast and efficient GaN-based electrical switches at a wide range of power levels. General overviews of wide bandgap semiconductor power electronics are provided in [2.334, 2.469, 2.494]. Typical expectations and specifications are:

- High stand-off voltage, e.g., >1 kV [2.76, 2.438]
- High absolute current levels, e.g., up to 2 kA conducting current [2.76]
- A low forward voltage drop, e.g., $\leq 2\%$ of the rated voltage
- Higher operation temperature (e.g., 225°C [2.334])
- High frequency switching operation, e.g., at 50 kHz and above

The use of GaN-diodes in low-frequency control applications is discussed in [2.59]. GaN is predicted to have insertion and isolation loss properties similar to other semiconductors. The trade-off between parasitic resistance, breakdown voltage, and off-state capacitance is discussed. GaN devices do not necessarily provide higher breakdown voltages, but GaN FETs provide lower switching energies for the same breakdown voltages. Principal design considerations for III-N high-power devices are given in [2.27]. Planar Schottky devices are fabricated to obtain principal device parameters. Based on that, AlGaIn thyristor switches with breakdown voltages of 5 kV at current densities of 200 A cm^{-2} with frequencies above 2 MHz are predicted based on the basic device parameters. Future military applications of wide bandgap power semiconductor devices are discussed in [2.105]. The high-power handling capabilities of the SiC and GaN devices in general allow more efficient power distribution at higher power levels and more compact device sizes. Estimates of the theoretical limit of lateral wide bandgap semiconductor devices for switching applications are given, e.g., in [2.396]. Lateral switching devices based on GaN and SiC are discussed for breakdown voltages of 1 kV and on-resistances of $1\text{ m}\Omega\text{ cm}^2$. The main advantage of the wide bandgap devices is the drastic reduction in gate width and chip area, and in power loss. At the same time the increase of the power density in the GaN FETs by a factor of

6 leads to an increase of the thermal dissipation and requires a significantly improved packaging technique.

RF-Switches

A high-power Tx/Rx RF-switch IC using AlGaIn/GaN HFETs on sapphire substrate is described in [2.158]. The device is capable of handling a power of 46 dBm at 1 GHz with an insertion loss of 0.26 dB and an isolation of 27 dB. The high-breakdown voltage leads to a reduction of the number of FETs as compared to circuits realized with GaAs technology. A single pole double through (SPDT) switch implemented with GaN HFETs featuring a double recess technique is presented in [2.144]. A low insertion loss of 1.1 dB and an isolation of 21 dB can be realized. The double recess technique including an ohmic and a gate recess allows to optimize the access resistance and leakage current independently.

DC-DC-Converter

Fast and efficient DC-DC-converters are one application for AlGaIn/GaN HEMTs. An overview of the suitability of wide bandgap semiconductors for this application is given in [2.460]. As an example, a 600 V fast DC-DC-converter AlGaIn/GaN power HEMT is demonstrated in [2.397]. An optimized design including a source-terminated field plate delivers $R_{\text{on}} = 0.5 \text{ m}\Omega \text{ cm}^2$ and a maximum switching current density of 850 A cm^{-2} . The power efficiency varies between 83% at 100 kHz and 75% at 500 kHz. A demonstration of a Class-E amplifier with a PAE of 89.6% at 27.1 MHz is given in [2.394, 2.395]. The applied drain voltage is 330 V. The devices are grown on n-SiC substrate and use a source-terminated field plate. Even higher breakdown voltages of 1.6 kV and low $R_{\text{on}} = 3.4 \text{ m}\Omega \text{ cm}^2$ are reported in [2.459]. With the application of conductivity modulation, even higher breakdown voltages are achieved, e.g., [2.471]. A typical FOM for power conversion and switching reads:

$$\text{FOM} = \frac{V_{\text{breakdown}}^2}{R_{\text{on}}} = q \cdot \mu \cdot n_{\text{sheet}} \cdot E_{\text{crit}}^2. \quad (2.55)$$

The limits of the material system used can be deduced with the approximation given in (2.55). A more advanced approximation including a surface limit is given in [2.459]. These limits are also depicted in Fig. 2.15. There are several examples for the trade-off between breakdown voltage and on-resistance for GaN HEMTs in comparison with Si and SiC devices, as given in Fig. 2.15. Data points are taken from [2.2, 2.63, 2.138, 2.213, 2.310, 2.398, 2.438, 2.445, 2.471, 2.472]. Silicon devices beyond the actual Si limit have been realized [2.310]. The third parameter, the switching time, is not explicitly mentioned in Fig. 2.15. However, turn-on delays of 7.2 ns can be reached with GaN FETs. This turn-on delay is only a fraction of the Si MOSFET value. Further improvements are found for wide bandgap semiconductor with respect to heat dissipation and reduced chip area, as discussed in [2.396]. A recent general

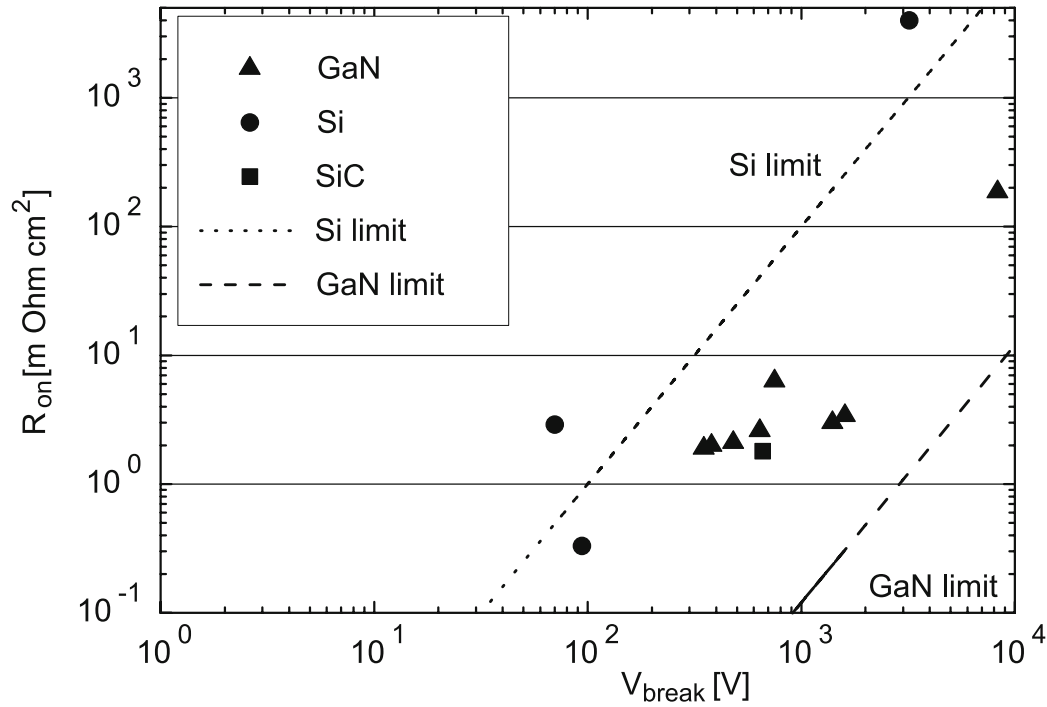


Fig. 2.15. On-resistance R_{on} as a function of breakdown voltage for switching applications

overview on the use of diamond for power applications is given in [2.207]. This material system promises very high breakdown voltages of 10 kV [2.396] and operation temperatures of 1,000°C, while this approach is still in its infancy.

2.5.3 RF-Metal Semiconductor Field-Effect Transistors (MESFETs)

MESFETs have been introduced as the first wide bandgap FETs into industrial production.

SiC MESFETs

A compilation of substrate and semiconductor material properties of SiC is given in [2.139]. Both static induction transistors (SIT) and SiC MESFETs are discussed. Pulsed-output power levels of 900 W of SiC SITs at 425 MHz with a drain efficiency of 80% are reported as well as output power levels of 80 W at 3.1 GHz with MESFETs. Substrate and epitaxial issues for SiC power devices are discussed in [2.433]. A classification of the residual defects is also given. A complete SiC MESFET technology, especially for S-band RF-applications, is provided by Cree [2.75]. The transition of this technology from discrete MESFETs to a high performance MMIC technology is described in [2.293].

The MMIC devices yield excellent wafer-to-wafer uniformity and a high power density of 4 W mm^{-1} up to frequencies of 3.5 GHz. Silicon carbide MESFET performance and its application in broadcast power amplifiers between 0.5 and 0.9 GHz are reported in [2.454]. The SiC devices yield a much higher operation voltages of up to 55 V in comparison to Si LDMOS. This leads to increased output densities of $\geq 2 \text{ W mm}^{-1}$, but especially higher input and output impedances for SiC MESFETs. A comparison of SiC and GaN transistors for microwave power applications is given in [2.463]. The main distinction suggested is the power density of SiC MESFETs with $5\text{--}6 \text{ W mm}^{-1}$ up to X-band, while GaN is predicted to achieve up to 10 W mm^{-1} up to 100 GHz on the device level.

GaN MESFETs

GaN MESFETs provide wideband properties similar to SiC MESFETs; however, both lack the potential advantages of heterojunctions. The advantage of GaN MESFETs relative to SiC MESFETs is the increased speed performance. This speed performance is, however, inferior to GaN heterostructure devices, e.g., as demonstrated in [2.62, 2.379]. A theoretical comparison by simulation of GaN MESFET-based on different GaN material phases wurtzite and zincblende GaN is given in [2.111]. The wurtzite structure yields higher breakdown voltages and lower transconductance than the zincblende structure. The simulated cut-off frequencies of wurtzite MESFETs are significantly lower, again based on the lower transconductance. Another systematic comparison of zincblende-phase GaN, cubic-phase SiC, and GaAs MESFETs using a full-band Monte Carlo simulator is given in [2.492]. A factor-of-four improvement of the breakdown voltage for GaN devices is found as compared to GaAs MESFETs for the same gate length of 100 nm. The experimental realization of doped-channel GaN heterojunction MESFETs are described in [2.62]. The devices with a gate length of $0.25 \mu\text{m}$ yield an output power density of 1.7 W mm^{-1} at 8.4 GHz on sapphire substrates. The doped channel layer has a thickness of 50 nm and is n-doped with $n = 2 - 5 \times 10^{17} \text{ cm}^{-3}$. The $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ layer has thickness of 18 nm. Epitaxially grown GaN junction FETs are given in [2.531]. The cut-off frequencies are $f_T = 6 \text{ GHz}$ and $f_{\text{max}} = 12 \text{ GHz}$ for a gate length of $0.8 \mu\text{m}$. The channel mobility is $270 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for a free carrier concentration of $1.3 \times 10^{18} \text{ cm}^{-3}$. The nominal p-doping of the pn-junction is $5 \times 10^{19} \text{ cm}^{-3}$. The impact of p-doped overlayers on the dispersion in GaN junction FETs is described in [2.166]. The p-doped layer removes the low-frequency dispersion as it screens the channel from the surface states. This concept is promising, as the reproducibility of an epitaxial concept is higher than of a technological approach. However, the Mg trap depth is not sufficient to avoid carrier modulation, which leads to longer effective gate length and thus lower f_T and f_{max} . A GaN MESFET based purely on polarization doping through a graded AlGaIn barrier layout without any impurity doping is compared to a conventional impurity n-doped GaN MESFET

in [2.379]. The polarization-doped devices with a gate length of $0.7\mu\text{m}$ yield $f_T = 19\text{ GHz}$ and $f_{\text{max}} = 46\text{ GHz}$.

2.5.4 Metal Insulator Semiconductor Field-Effect Transistors (MISFETs)

Nitride MISFETs are very attractive candidates for improved performance of the gate diodes relative to nitride MESFETs and HEMTs with metal/semiconductor Schottky-gates. At the same time MISFETs require the mastery of the insulator/semiconductor interface. This interface affects threshold voltages and other device properties to a great extent. GaN-based MOSFETs (Metal Oxide Semiconductor FETs) have been demonstrated, e.g., in [2.191]. The comparison of the $\text{SiO}_2/\text{AlGaIn}/\text{GaN}$ MOSFETs with regular Schottky-gate HEMTs yields similar drain current densities, while the gate current density is reduced by six orders of magnitude for the MOSFET. The threshold voltage is shifted by -3 V for the MOSFET relative to the HEMT. A quarter micron $\text{SiN}/\text{AlGaIn}/\text{GaN}$ MISFET was developed as reported in [2.1]. Again the threshold voltage V_{thr} is shifted to negative values of -7 V . This MISFET further yields a high power density of 6 W mm^{-1} up to 26 GHz . The DC- and small-signal parameters of the MISFET are very similar to those of the HEMT. An overview of III-N insulating gate FETs is further provided in [2.193]. The low-leakage currents of the MISFETs found at RT are also reduced at temperatures of 300°C . Further, the MISFET concept is applied to double heterojunction $\text{AlGaIn}/\text{InGaIn}/\text{GaN}$ structures, which reduce the current collapse to a high extent [2.192, 2.426].

Power Performance of MISFETs

Several demonstrations of the power performance of III-N MISFETs are available [2.69, 2.74]. Reduced gate-leakage of MIS gate devices relative to MESFETs and consequently improved linearity at 4 GHz are demonstrated in [2.69]. The third-order intermodulation ratio of 30 dBc is reached with a power density of 1.8 W mm^{-1} and an associated PAE = 40% at 2 GHz . SiO_2 is used as the gate dielectric. The microwave performance of undoped AlGaIn/GaN MISFETs on sapphire substrates is given in [2.74]. A power density of 4.2 W mm^{-1} at 4 GHz is obtained at $V_{\text{DS}} = 28\text{ V}$, again with a very negative threshold voltage $V_{\text{thr}} = -10\text{ V}$. The extrinsic transconductance is 100 mS mm^{-1} . $\text{SiO}_2/\text{AlGaIn}/\text{InGaIn}/\text{GaN}$ MOS double heterostructure FETs (MOSDHFETs) are demonstrated in [2.192, 2.426] with the introduction of the new channel material InGaIn . The importance of the additional carrier confinement is to reduce the spillover into trapping states. A Cat-CVD Insulated AlN/GaN MISHFET is given in [2.142]. Very thin AlN layers with a thickness of 2.5 nm are used as barrier layers. On top of this barrier a 3 nm SiN layer is deposited by Cat-CVD. This layer combination allows a very small gate-to-channel separation, which is used combination with gate length

of 60 nm to achieve a cut-off frequency $f_T = 107$ GHz. The application of GaN MISFETs for low-loss switching is discussed in [2.217]. A 1 mm wide AlGaIn/GaN MOSHFET yields switching powers of 43 W with 40 dB of isolation and 0.27 dB insertion loss at 100 MHz. The SiO₂ thickness is 7 nm in this case. The very negative threshold $V_{thr} = -9$ V is achieved for the device, which yields a maximum saturated pulsed-drain current of 2 A mm⁻¹.

2.5.5 High-Electron Mobility Transistors (HEMTs)

GaN HEMTs or heterojunction FETs (HFETs) are currently the most widespread and most advanced electronic nitride devices. They make full use of heterostructures and the advantageous breakdown and transport properties of undoped GaN. A huge number of compilations of GaN HEMT data is available, e.g., in [2.39, 2.96, 2.301, 2.302, 2.463]. Initial overviews are given in [2.40, 2.312, 2.422]. Initial microwave results of AlGaIn/GaN HEMTs have been given in [2.40, 2.190, 2.506]. An overview of AlGaIn/GaN HEMT technology is provided by Keller et al. and Mishra et al. from UCSB in [2.188, 2.301]. P_{sat} An overview of the application of GaN-based HFETs for advanced wireless communication is provided in [2.341]. Recent developments and trends in GaN HFETs in Europe are given in [2.455, 2.476]; overviews of the US activities are given, e.g., in [2.361, 2.401]. This section provides a systemized data collection which is presented with emphasis on the frequency aspect and the achievements relative to the theoretical predictions. To systemize device performance, Fig. 2.16 gives a compilation of the product cut-off frequency $f_T \times l_g$ as a function of gate length l_g . A product of 12 GHz μ m is found for $l_g \geq 300$ nm for GaN HFETs. A GaAs reference value of 15 GHz μ m is assumed. For gate lengths smaller than 300 nm, the short-channel effects become visible for GaN HFETs. Fig. 2.17 gives a compilation of the output power per unit gate width as a function of frequency. A distinction is made between pulsed- and cw-output power. The maximum power densities reach 12 W mm⁻¹ without additional measures at the gate, while output power densities ≥ 40 W mm⁻¹ have been reported using field plates [2.511]; however, reliability concerns prevail. Significant improvements of the output power up to 101 GHz have been reported as compared to all other semiconductor technologies [2.291, 2.378]. Similar to Fig. 2.17, Fig. 2.18 gives the absolute cw- and pulsed-output power as a function of frequency. The power levels on the transistor level reach 370 W under cw-operation conditions [2.488] at 2 GHz. Under pulsed-operation with low duty cycles, even higher output power values of up to 1 kW have been reported [2.268, 2.304, 2.503]. For low-noise operation, Fig. 2.19 gives the minimum noise figure $N_{F,min}$ as a function of frequency for both a single-recess GaAs PHEMT and a planar GaN HFET. The comparison yields promising minimum noise figure for the GaN HFET, which is slightly increased relative to the GaAs PHEMT [2.153, 2.262]. The next paragraphs systematically discuss the various frequency bands with respect to power and noise performance.

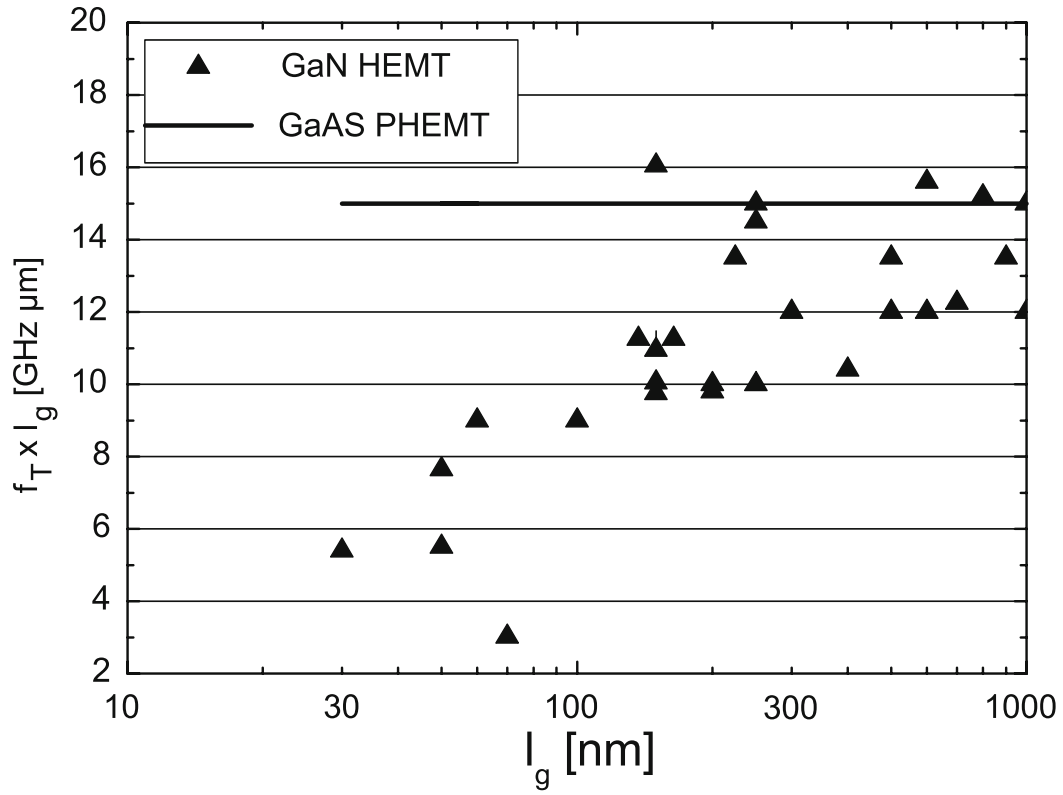


Fig. 2.16. Product cut-off frequencies $f_T \times l_g$ as a function of gate length l_g

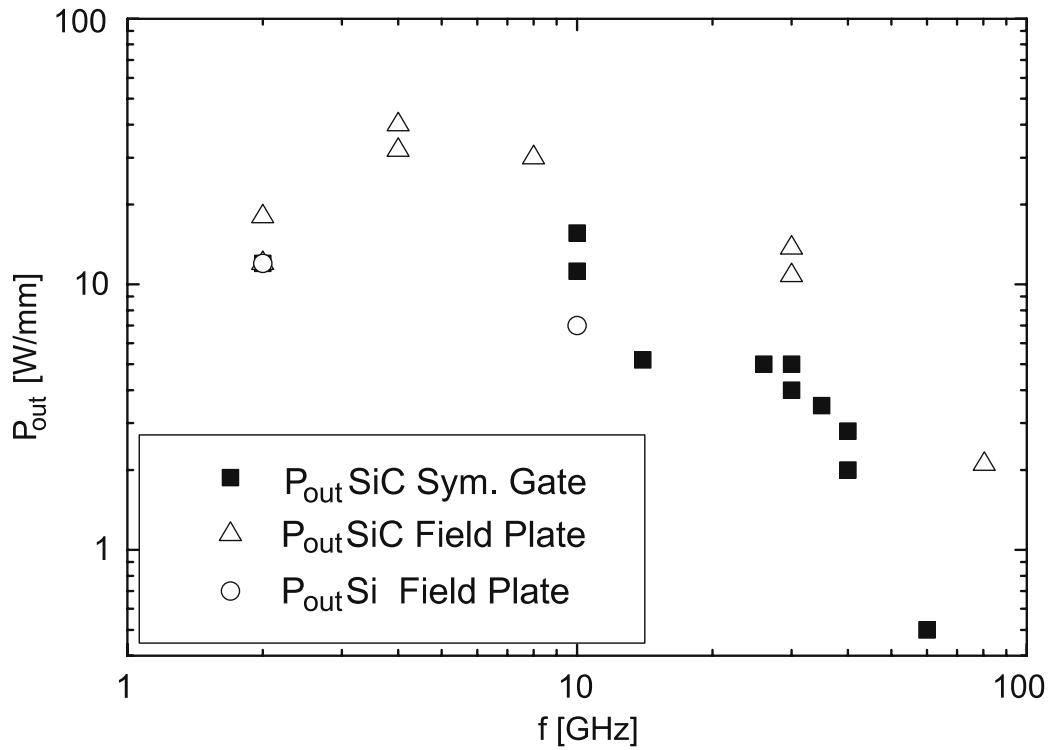


Fig. 2.17. Measured output power per unit gate width as a function of frequency

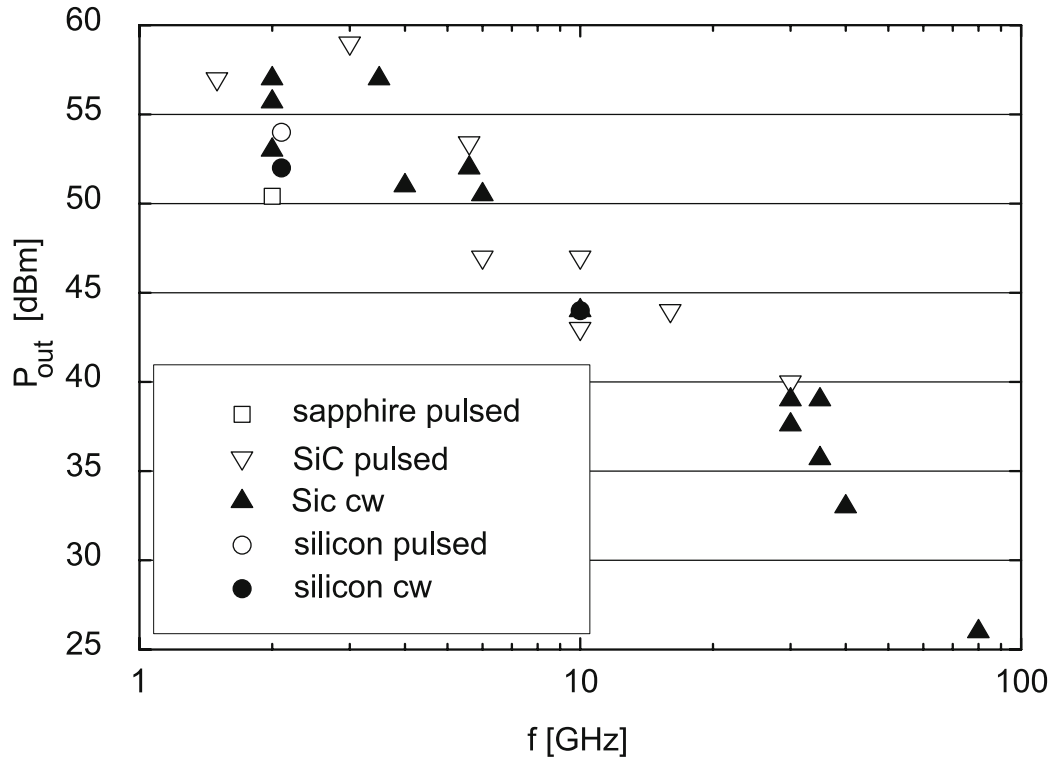


Fig. 2.18. Absolute cw- and pulsed-output power of AlGaN/GaN HFETs on various substrates as a function of frequency

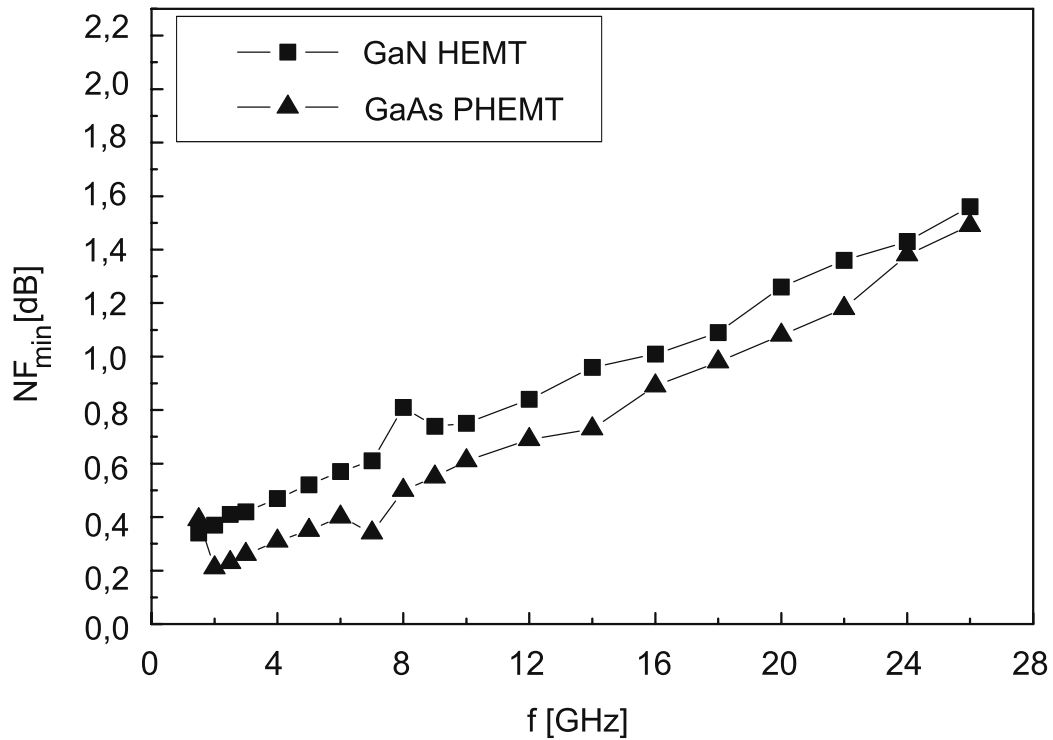


Fig. 2.19. The minimum noise figure $N_{F,min}$ for GaAs and GaN HEMTs as a function of frequency at a drain current $I_D = 100 \text{ mA mm}^{-1}$ for $l_g = 150 \text{ nm}$

L-Band and S-Band Frequencies (1–3 GHz)

GaN HEMTs are attractive for base-station applications, due to the increased operating voltages ≥ 28 V, higher impedance levels, and reduced thermal memory effects. Overviews and guidelines for future directions are given, e.g., in [2.309] and in [2.495].

Mobile Communication

Cree gave the first report of cw-power operation of GaN HEMTs on SiC with output power levels beyond 100 W with 108 W at 2 GHz in [2.362]. Higher power operation at 3.5 GHz has recently been demonstrated in [2.503] with output power levels of 550 W in pulsed-operation with low duty cycle at $V_{DS} = 55$ V in a single-stage design. On s.i. SiC substrate, an 80 W/96 W AlGaIn/GaN HFET with a field-modulation plate is demonstrated by NEC in [2.343, 2.345]. The 24 mm device yields a peak PAE of 54% for an operation bias $V_{DS} = 32$ V. The 4 mm subcell yields a power density of 8.1 W mm^{-1} at $V_{DS} = 41$ V. An AlGaIn/GaN field-plate-FET with a gate width of 32 mm using a recessed gate is demonstrated in [2.344]. The cw-power density is 4.7 W mm^{-1} and the peak PAE is 64% at 2 GHz and $V_{DS} = 47$ V. Similarly, a cw-output power of 179 W is then reported in [2.190] for a gate periphery of 48 mm. The linear gain is 9.3 dB at 2 GHz, the PAE is 64% at $V_{DS} = 46$ V. A similar transistor operated under one-carrier WCDMA conditions presents 280 W of single-ended-amplifier output power in [2.487] with the application of a gate width of 48 mm with a linear gain of 12.6 dB at $V_{DS} = 48$ V. The drain efficiency is 29% at 8 dB of backoff from the saturated power in WCDMA operation. The output power levels can be increased to 370 W with paralleled devices, again achieved under one-carrier WCDMA conditions at 2.14 GHz. In this case the linear gain is 11.2 dB at $V_{DS} = 45$ V. AlGaIn/GaN HFETs on thinned sapphire substrates with 110 W of pulsed-output power at 2 GHz at $V_{DS} = 40$ V are presented by NEC in [2.16] with $W_g = 32$ mm device. The related cw-output power is much lower and reaches 22.6 W for a $W_g = 16$ mm device. The sapphire substrate is thinned to 50 μm in this case.

Fujitsu and Eudyna have demonstrated some of the most advanced device results with respect to base-station applications. Early results present a 36 W cw-AlGaIn/GaN power HEMT using a surface-charge-controlled structure [2.198]. This structure combines a doped GaN cap to screen the polarization charges at the AlGaIn/GaN interface with very well optimized material. Both the barrier thickness and the SiN passivation are optimized. An improved intermodulation distortion profile of such AlGaIn/GaN HEMTs at a drain bias voltage $V_{DS} = 30$ V is reported in [2.318]. No sweet-spot behavior is found for two-tone measurements in deep class-A/B operation. Further technology development is described in [2.195, 2.197]. CW-operation of a 24 mm device at $V_{DS} = 50$ V is achieved with a peak PAE of 60% and an output power of 48 W at 2 GHz. Output power levels of 150 W in cw- and 174 W at 2.1 GHz in WCDMA-operation at $V_{DS} = 63$ V are reported in [2.172, 2.196] for a single

packaged device. The PAE is 54% in cw-operation. For four-carrier WCDMA signals including the application of predistortion system, a peak efficiency of 40% is reached in Class-A/B operation while the WCDMA ACLR specification of -50 dBc at 10 MHz offset is preserved. The gate width is 36 mm with a unit finger length of 400 μm . Based on these devices, a GaN HEMT amplifier in dual-device push-pull configuration is demonstrated in [2.171, 2.195]. The devices are again biased at $V_{\text{DS}} = 50$ V. The cw-output power of the amplifier at 2.1 GHz is 136 W with an associated PAE of 53% and a linear gain of 12.9 dB. The amplifier is further characterized in one-carrier WCDMA operation. With the application of a DPD system, a peak output power of 250 W is reached. The associated drain efficiency is 37% at an ACLR of -55 dBc. The average output power amounts to 46.5 dBm. The technology transfer and very promising reliability results are reported at $V_{\text{DS}} = 60$ V [2.197, 2.330]. The devices can be operated at a compression level of $P_{-3\text{dB}}$ at $V_{\text{DS}} = 60$ V for 1,000 h at room temperature. The resistance of the ohmic contacts is found to stable within 6% at high current density of 2×10^6 A cm $^{-2}$ at 250°C in nitrogen ambient. High-efficiency Class-E amplifiers in this technology are given in [2.473]. The amplifiers reach 82% of drain efficiency at 2.1 GHz, an output power of 10 W, and a linear gain of 19.5 dB. 45% of drain efficiency are reached for two-carrier WCDMA operation at ACLR of -50 dBc. The technology has further been exploited for air traffic radar. Pulsed-output-power levels of 500 W at 1.5 GHz for radar operation are reported in [2.268]. The amplifier consists of four chips with a gate width of 36 mm each with an overall gate width of 144 mm in a dual push-pull configuration. Even higher output power levels are obtained at S-band in [2.304]. A maximum pulsed-output power of 59.3 dBm is obtained between 2.9–3.3 GHz with a linear gain of 14 dB at $V_{\text{DS}} = 65$ V and 10% duty cycle. The pulse width is 200 μs and the associated PAE amounts to 50%. Again a four-chip configuration is used with a single finger gate width of 375 μm and a total gate width of 4×36 mm = 144 mm.

RF Microdevices announced the commercial application of GaN FETs on 4 in. sapphire [2.412] and later on 3 in. s.i. SiC substrates in [2.134, 2.482]. The technology comprises very high power cw-densities of ≥ 22 W mm $^{-1}$ at 2.14 GHz and $V_{\text{DS}} = 80$ V. A 20 mm devices delivers more than 100 W of output power with an associated PAE of 55% at $V_{\text{DS}} = 48$ V. Dual-gate devices are used for driver applications in [2.481]. Different dual-gate technologies are compared to single gate technologies. As an outcome a ground-terminated field plate on top of the SiN yields higher gain per stage, higher PAE, and better reliability under RF-drive.

Freescall provides AlGaN/GaN HEMTs on s.i. SiC for an industrial process [2.131]. Very high cw-power densities of 10–11 W mm $^{-1}$ are reached with PAE levels of 67% at 2.14 GHz. Devices with 12.6 mm periphery yield output power levels of 74 W or nearly 6 W mm $^{-1}$ in cw-operation. The SiC substrates are thinned to 100 μm .

GaN devices on silicon substrates show much economic potential due to the low substrate cost. Conducting and high-resistivity silicon substrates are

suitable candidates for operation of up to 10 GHz [2.109]. The performance of AlGaIn/GaN HFETs fabricated on 100 mm silicon substrates for wireless base-station applications is further evaluated in [2.52]. Despite the high lattice-mismatch, very good reliability data are reported predicting 20 years of lifetime based on a junction temperature of 200°C and 10% drift of the parameters. Cw-power densities of up to 12 W mm⁻¹ at 2.14 GHz and $V_{DS} = 50$ V are reached with this AlGaIn/GaN HEMT technology [2.169]. The gate width in this case is 100 μ m, the maximum PAE 52%, and the power gain 15 dB. Recent reports announce cw-power levels of 150 W at 2.14 GHz with a drain efficiency of 65% and a linear gain of 16 dB, when operated at $V_{DS} = 28$ V [2.319]. The overall gate periphery is 72 mm in a single package with a single finger geometry of 0.7 μ m $\times$ 200 μ m. Promising reliability results have been reported in [2.168, 2.367]. Devices with a periphery of 36 mm are tested under RF-drive with an extrapolated drift of P_{sat} of ≤ 1 dB in 20 years at 28 V. On amplifier level, very promising PAE vs. ACLR results are reported in [2.201, 2.202] with PAE levels of 50% based on Nitronex GaN HEMTs. Envelope-tracking is used to obtain high PAE values of 50% for a nonconstant envelope input. An average output power of 37 W is reached at a peak-to-average ratio (PAR) of 7.67 dB. The linear gain in this operation is 10 dB. With the application of a digital predistortion the error vector magnitude (EVM) of 1.74% is reached with an ACLR of -51 dBc at 5 MHz offset. Specific WiMAX applications based on GaN on silicon are presented in [2.456]. Eight millimeter and 36 mm devices are tested under orthogonal frequency-division multiplexing (OFDM)-modulation between 3.3 GHz and 3.8 GHz. At 3.5 GHz, the 8 mm device delivers an average output power of 1.5 W at 3.5 GHz, while the 36 mm device delivers 7 W. EVM is 2% and the drain efficiency (DE) amounts to $\geq 27\%$. The devices are fully packaged and qualified between -40°C and 85°C.

Several other processes are available. The performance of AlGaIn/GaN HEMTs for 2.8 GHz and 10 GHz power amplifier applications is evaluated in [2.528] for military applications. Pulsed-output power levels of 41 W at 2.8 GHz with power densities up to 9.2 W mm⁻¹ are obtained early in the development.

C-Band Frequencies (4–8 GHz)

C-band frequencies are used for both communication and radar applications and require high-power operation and high-temperature robustness in combination with high PAE. This frequency range typically cannot be reached by either LDMOS or SiC MESFETs. GaN HEMTs on s.i. SiC substrate using a field-plate gate concept are demonstrated at operating voltages of ≥ 90 V, resulting in cw-output power densities $P_{out} \geq 30$ W mm⁻¹ at 4 GHz and 8 GHz [2.512]. Although the scaling of this performance to higher gate widths is questionable with respect to the thermal management, reliability, and efficiency, the fundamental high-speed power performance of GaN is visible. At C-Band, the University of California reported a GaN HEMT on s.i. SiC

with an output power of 2.8 W with a density of 18.8 W mm^{-1} and a PAE of 43%. A maximum PAE of 71% is reported with a power density of 6 W mm^{-1} at 4 GHz [2.67]. A 60 W and 100 W internally matched C-band GaN HEMT with $W_g = 24 \text{ mm}$ is given in [2.346, 2.347]. The cw-output power is 100 W at 5 GHz with 31% PAE and a linear gain of 12.9 dB at $V_{DS} = 56 \text{ V}$. Applying pulsed-operation with 1% duty cycle, an output power of 156 W is found at 4 and 5 GHz [2.346]. Record cw-output power values of 140 W at 5.6 GHz from a single chip are reached with the application of $W_g = 50.4 \text{ mm}$ [2.173, 2.519]. A cell division concept is applied to suppress odd-mode loop oscillations while maintaining good gain. Record output power levels of 220 W at C-band are reported in [2.520] in a two-chip amplifier by improvements of device performance and reduction of the thermal resistance. 167 W are obtained from a single chip at 7 W mm^{-1} . Similarly 60 W of output power are obtained from a 16 mm chip at 45% PAE. These examples demonstrate the combination of high-gain and high-breakdown in GaN HFETs which have demonstrated much higher power densities, output power levels, and operation bias, while maintaining efficiency.

X-Band Frequencies: (8.2–12.4 GHz)

Power operation of AlGaIn/GaN HEMTs at X-band is particularly attractive, due to the increase of operating voltages relative to GaAs while maintaining high-speed operation and thus guaranteeing high-gain and high-efficiency operation. The increase in operating voltage from typically 5–8 V for GaAs PHEMTs to $\geq 40 \text{ V}$ will reduce the need to transport high currents on system level. Applications in the X-frequency band include transmit-receive (TRX) modules for naval and airborne phased array radar applications. Power-added efficiency is a major concern, both on the device and system level. Typical device targets are mentioned in [2.384]. PAE values of 60% are required at $V_{DS} = 40 \text{ V}$ with a power density of 6.4 W mm^{-1} for a device with 1.28 mm. Further the long term reliability of 10^6 h is required. Early reports of the power operation at X-band by the UCSB and Rockwell are given in [2.439, 2.507]. The output power density was 1.7 W mm^{-1} and 2.3 W mm^{-1} at that time for small devices. An early report of very high-power density of AlGaIn/GaN HEMTs on s.i. SiC with 9.8 W mm^{-1} at 8 GHz is demonstrated by the UCSB in [2.504]. Basic predictions of the power operation limits are provided by Trew et al., focusing on the impact of the wide bandgap-material-properties on RF-power performance with respect to dispersion, e.g., in [2.462, 2.463, 2.465]. Output power densities of $10\text{--}12 \text{ W mm}^{-1}$ are predicted at X-band. The experimental power-frequency limits of AlGaIn/GaN HEMTs for X-band are evaluated by Eastman and coworkers, e.g., in [2.96, 2.98, 2.132]. Small periphery devices with $l_g = 300 \text{ nm}$ yield power densities of 11.7 W mm^{-1} at 10 GHz with an associated PAE of only 43% at $V_{DS} = 40 \text{ V}$. At low V_{DS} bias, the PAE is as high as 55%. Geometrical considerations for the operation at X-band, e.g., the barrier-layer thickness, are evaluated in [2.457]. Triquint announced a power

MMIC process for radar applications at X-band [2.467]. Output power densities of 12 W mm^{-1} at 10 GHz have been reported with an associated PAE of 50%. An outstanding performance is also announced on Si substrates at X-band in [2.94]. The power densities for a small periphery device are as high as 7 W mm^{-1} at 10 GHz with an associated PAE of 37% at $V_{\text{DS}} = 40 \text{ V}$. Again, the PAE is limiting in this case.

In cooperation with General Electric, a power density of 9.2 W mm^{-1} with 13.8 W cw-output power at 10 GHz and 55 V drain bias using AlGaIn/GaN HEMTs on SiC substrate are demonstrated by Lockheed in [2.18]. The associated PAE is 35%. At lower bias $V_{\text{DS}} = 30 \text{ V}$, the power density is 6.7 W mm^{-1} with an associated PAE of 55%. Very promising hybrid single-stage X-band amplifiers are demonstrated by Hughes in [2.292] yielding output power values of $\geq 22.9 \text{ W}$ with a cw-PAE as high as 43%. More recent GaN MMICs in microstrip transmission-line technology are given in [2.313]. The devices with a gate length of 150 nm use a field plate. Output power levels of 20 W with 43% PAE are reached in pulsed-operation. The III-N activities of Raytheon for high-power and low-noise X-band applications are discussed in [2.210]. PAE, uniformity, and reliability are considered the main challenges for the application of GaN HEMTs in TRX modules. The thermal management considerations in [2.210] further predict an order of magnitude increase in heat removal within a TR module with the insertion of GaN technology. With the application of innovative power combining techniques, multichip solid-state power amplifiers with overall 150 W output power levels are announced for X-band [2.79]. The PA is based on 16 chips similar to those reported in [2.81]. On hybrid packaged transistor level, Toshiba developed a 11.52 mm-gate-periphery GaN HEMT with a maximum output power of 81 W in cw-operation. The PAE amounts to 34% at 9.5 GHz and a gain compression level of 3 dB [2.444]. The unit gate width is $160 \mu\text{m}$ and no field plate technology is used for a gate length $l_g = 0.7 \mu\text{m}$. A similar result is obtained with a gate periphery of 12 mm and a gate length $l_g = 0.5 \mu\text{m}$ with a hybrid AlGaIn/GaN HEMT. The two chip device yields an output power of $\geq 60 \text{ W}$ and a maximum PAE of 35%. The linear gain is 10 dB at a duty cycle of 10% and $V_{\text{DS}} = 40 \text{ V}$ in Class-B operation [2.518].

Double Heterostructure Devices

Double heterostructure devices overcome the disadvantage of the single heterostructure, which provides only limited electron confinement in the channel. The second heterojunction reduces the poor pinch-off characteristics and high-output conductance, which both degrade power performance and PAE at RF-frequencies for single heterojunction devices [2.289]. Initial reports on AlGaIn/InGaIn/AlGaIn double heterojunction devices (DHFETs, DHHEMTs) based on the AlGaIn/InGaIn material system are given in [2.425], as also mentioned in [2.210]. The AlGaIn/InGaIn/GaN provided an initial output power of 6.3 W mm^{-1} at 2 GHz and $V_{\text{DS}} = 30 \text{ V}$. Very promising AlGaIn/GaN/AlGaIn

DHFETs on s.i. SiC for microwave and millimeter-wave power applications are given in [2.289], grown by MBE at HRL. The DHFETs yield higher transconductance and lower output conductance than SHHEMTs. PAE improvements of 10% are found at 10 GHz for a process with a gate length of 150 nm at $V_{DS} = 30$ V, while the power density is maintained.

Ku-Band (12.4–18 GHz) and K-Band (18–26 GHz)

Ku-band amplifiers find their applications in radio communication systems, such as satellite and mobile phone systems for point-to-point communication [2.314] and for military applications. Traveling-wave-tube amplifiers with very high efficiency levels of 70% and output power levels of 150 W with low weight are given in [2.288]. GaAs-based solid-state reference amplifiers for Ku-band operation can be found, e.g., in [2.314, 2.468], with a 40 W Ku-band high-efficiency hybrid solid-state power amplifier (SSPA). A good comparison of GaAs MMICs is given in [2.249]. Typical MMICs yield maximum output power levels of 5–10 W and PAE levels of $\geq 30\%$. References for conventional HPAs in efficiency-critical applications at K-band can be found in [2.24] based on InP HBTs. Output power levels of 870 mW are found at 20 GHz and 37% PAE. Initial reports of K-band power operation of III-N devices are given in [2.479, 2.505] with an output power density 3 W mm^{-1} at 18 GHz and 20 GHz for AlGaIn/GaN HFETs on s.i. SiC substrate. AlGaIn/GaN HEMTs operating at 20 GHz with a cw-power density $\geq 6 \text{ W mm}^{-1}$ are reported in [2.312]. For applications requiring high efficiency, such as satellite communication, a power density of 3.2 W mm^{-1} with an associated PAE of 71% using AlGaIn/GaN HEMTs at 20 GHz is reported in [2.399], again for a small gate width device. A power density of 6.7 W mm^{-1} at 18 GHz is reported in [2.227] with an associated PAE of 26%. Even higher power densities at 18 GHz have been achieved using field-plated gates, however, with a gain of only 5.8 dB in [2.226] for a small gate width of 100 μm . An output power density of 5.1 W mm^{-1} is reported for AlGaIn/GaN HEMTs on silicon substrate in [2.93]. The devices have a periphery of 100 μm . Residual challenges for Ku-band devices include the increase of power-added efficiency for large periphery devices in applications requiring high efficiency, as GaAs PHEMTs and InP HEMTs have set high standards with respect to this requirement, e.g., [2.24, 2.466].

MM-Wave Frequencies

MM-wave operation of GaN FETs beyond 30 GHz has been demonstrated with improved material homogeneity and an increasing number of electron-beam T-gate processes being available on s.i. SiC, e.g., in [2.179].

Ka-Band (26.5–40 GHz)

GaN HEMTs are very attractive devices for Ka-Band MMIC applications due to their combination of high-speed and high-power performance [2.354].

State-of-the-art GaAs-PHEMT-based reference devices and MMICs can be found, e.g., in [2.214, 2.266] and the references therein. A record compact size MMIC with an area of only 9 mm^2 and 4 W of output power level at 30 GHz is given in [2.215]. Power levels of 10 W at Ka-band can be reached with the grid amplifier concept [2.88] or up to 6 W on MMIC level, see [2.266]. Early reports on short-gate-length AlGaIn/GaN devices with a gate length $l_g = 0.12 \mu\text{m}$ with high contact resistance R_C demonstrate current gain cut-off frequencies $f_T = 46 \text{ GHz}$ and $f_{\text{max}} \geq 100 \text{ GHz}$ in [2.58]. More recent devices with the same gate nominal gate length yield a cut-off frequency f_T of 120 GHz [2.228]. State-of-the-art cw-power densities achieved at 26 GHz with AlGaIn/GaN HEMTs on s.i. SiC substrate are reported in [2.241] yielding a power density of 5 W mm^{-1} and a linear gain of 7 dB with an associated PAE of 30.1% at $V_{\text{DS}} = 25 \text{ V}$. Former TRW, now NGST, demonstrated power operation with 1.6 W mm^{-1} power density at 29 GHz and an associated PAE of 26% in [2.430, 2.431] at an early stage. Ka-band MMICs with pulsed-output power levels of 11 W at 34 GHz are mentioned [2.436]. Strong contributions to AlGaIn/GaN HEMT power operation in Ka-band are provided by NEC. They demonstrated power densities of 7.9 W mm^{-1} at 30 GHz for a $2 \times 60 \mu\text{m}$ device with a gate length of 250 nm in [2.233]. The device with a gate length of 90 nm yields an MSG of 8.3 dB at 60 GHz. Similarly, a cw-output power of 2.3 W at 30 GHz is demonstrated in [2.184] yielding a power-added efficiency of up to 50%. Further, a saturated output power of 5.8 W at 30 GHz for a GaN with $W_g = 1 \text{ mm}$, a peak PAE of 43.2%, and a linear gain of 9.2 dB are demonstrated in [2.156, 2.157] using a gate length of $0.25 \mu\text{m}$ and small contact spacings of $0.7 \mu\text{m}$. For frequencies targeting, e.g., missile radar applications at 35 GHz, Triquint demonstrated saturated power densities of $\geq 4 \text{ W mm}^{-1}$ with an associated PAE of 23% at 35 GHz in [2.240]. The device has a linear gain of 7.5 dB for a gate width $W_g = 200 \mu\text{m}$. Even higher peak PAE values of 53% have recently been reported [2.179]. An output power of 3.5 W at 35 GHz is demonstrated in [2.510] using AlGaIn/GaN HEMTs on s.i. SiC substrate with a gate width of 1.05 mm and a gate length of $0.18 \mu\text{m}$. The compression level for the peak power is $P_{-2\text{dB}}$. The prematched devices yield a linear gain of $\geq 8 \text{ dB}$ at 35 GHz. Further results of field-plate devices evaluated at 30 GHz and 35 GHz are given in [2.508]. Output power levels of 8 W with an associated PAE of 31% at 31 GHz are reached in cw-operation. With the inclusion of an InGaIn back barrier layer, a power density of 13.7 W mm^{-1} in cw-operation is obtained at 30 GHz and $V_{\text{DS}} = 60 \text{ V}$. The associated PAE is 40% [2.509]. At even higher frequencies, 40 GHz power operation is investigated in [2.194, 2.376] yielding power densities of $\geq 1.2 \text{ W mm}^{-1}$ and absolute power levels of 0.5 W. More recently, high performance AlGaIn/GaN HEMTs with a power density of 2.8 W mm^{-1} at 40 GHz and a PAE of 10% are demonstrated in [2.44]. The gate length is $l_g = 0.18 \mu\text{m}$, and the gate width is $W_g = 0.1 \text{ mm}$. Improved devices deliver 4.5 W mm^{-1} at 40 GHz [2.45]. MMICs in this technology with output power levels of 5 W at 30 GHz are given in [2.43]. The dual-stage design gives a linear gain of 13 dB and a PAE

of 20%. The output periphery is 1.6 mm. Even higher power densities have been achieved at 40 GHz. The power density amounts to 10.5 W mm^{-1} and 34% PAE at $V_{\text{DS}} = 30 \text{ V}$ for a $W_{\text{g}} = 2 \times 75 \mu\text{m}$ device [2.354]. The gate length is $l_{\text{g}} = 160 \text{ nm}$.

V-Band (50–75 GHz) and W-Band (75–110 GHz)

Solid-state-based power generation and amplification between 50 and 120 GHz is typically limited to power levels of 25 dBm, see, e.g., [2.155, 2.447]. Operation both at high-power levels as well as higher operation voltages is therefore desirable. The impact of III-N devices can thus be substantial. AlGaIn/GaN dual-gate HEMTs on s.i. SiC substrate are used to demonstrate V-band power operation at 60 and 65 GHz in [2.377]. Power gain of 8 dB is reached at 60 GHz, the maximum power density is 0.5 W mm^{-1} at 60 GHz. For a gate length $l_{\text{g}} = 140 \text{ nm}$, a cut-off frequency $f_{\text{T}} = 91 \text{ GHz}$ is achieved in [2.164]. The f_{max} is as high as 122 GHz. Several results exist for the scaling of the gate length. Vertically scaled T-gated AlGaIn/GaN HEMTs are reported in [2.45]. An extrinsic transconductance of 500 mS mm^{-1} is reported for devices with $l_{\text{g}} = 100 \text{ nm}$. The cut-off frequencies are $f_{\text{T}} = 125 \text{ GHz}$ and $f_{\text{max}} = 174 \text{ GHz}$. The first GaN W-band MMICs in microstrip technology are demonstrated by HRL [2.291]. The devices deliver output power levels of 316 mW at 80.5 GHz which have been obtained in cw-operation. The power density is 2.1 W mm^{-1} , the associated power gain amounts to 17.5 dB for three stages. On sapphire substrates, AlGaIn/GaN HFETs with cut-off frequencies $f_{\text{T}} = 152 \text{ GHz}$ at $V_{\text{DS}} = 5 \text{ V}$ are reported for $l_{\text{g}} = 60 \text{ nm}$. Even higher cut-off frequencies $f_{\text{T}} = 181 \text{ GHz}$ and $f_{\text{max}} = 186 \text{ GHz}$ are reported in [2.143]. When changing the barrier material to InAlN, $f_{\text{T}} = 172 \text{ GHz}$ is achieved with a gate length of 60 nm [2.143]. These devices are not fully passivated. Passivated AlGaIn/GaN HEMTs on s.i. SiC yield $f_{\text{T}} = 153 \text{ GHz}$ for $l_{\text{g}} = 90 \text{ nm}$ [2.355] with the application of a Ge-spacer technology. More of such high-speed specific process modules will be required; however, the potential of III-N HEMTs for mm-wave operation is visible.

RF-Noise Performance

Low-noise operation of III-N HEMTs is attractive due to the combination of high-carrier velocities, good carrier confinement in the channel, and increased robustness with respect to high-input power levels relative to other high-speed devices such as InAlAs/InGaAs HEMTs, AlGaAs/InGaAs PHEMTs, or Si/SiGe HBTs. Various overviews [2.353] and reports are available on the low-noise performance of GaN FETs. A matched minimum noise figure $N_{\text{F,min}}$ as low as 0.72 dB at 8 GHz is reported in [2.262, 2.364] for a device with $l_{\text{g}} = 120 \text{ nm}$ and $W_{\text{g}} = 100 \mu\text{m}$. The associated gain is 12 dB at 8 GHz. The maximum G_{ass} is found for a drain current $I_{\text{D}} = 150 \text{ mA mm}^{-1}$, while the minimum noise figure is found for $I_{\text{D}} = 100 \text{ mA mm}^{-1}$. Minimum noise figures $N_{\text{F,min}}$ of AlGaIn/GaN HEMTs on s.i. SiC of 0.75 dB at 10 GHz and 1.5 dB

at 20 GHz are reported, respectively, in [2.220] for a $2 \times 60 \mu\text{m}$ device with $l_g = 150 \text{ nm}$. Fig. 2.19 gives the dependence of the noise figure $N_{F,\min}$ as a function of frequency for $I_{DS} = 100 \text{ mA mm}^{-1}$ in comparison to a GaAs PHEMT of the same gate length $l_g = 150 \text{ nm}$. The low-noise performance of GaN HEMTs on sapphire substrate as a function of aluminum concentration in the barrier layer on the device level is discussed in [2.261]. The intrinsic minimum noise figure $N_{F,\min}$ at a given frequency decreases nearly linearly with increasing Al-content between 20% (1.7 dB) and 35% (0.92 dB), measured at 12 GHz. GaN HFETs on s.i. SiC substrate with excellent low-noise performance at low DC-power levels and $V_{DS} = 1 \text{ V}$ are demonstrated in [2.153]. Devices with a thin AlGaIn Schottky barrier layers of 15 nm are compared to devices with 30 nm barrier thickness. The $N_{F,\min}$ is below 0.8 dB across the 2–12 GHz frequency-band with associated gains of better than 12.5 dB for the device with the thinner barrier. The associated gain G_{ass} increases by 2 dB and the minimum noise figure $N_{F,\min}$ is reduced by 0.2 dB for the devices with the thinner barrier. On silicon substrates, very promising noise figures $N_{F,\min}$ at 10 GHz are reported for $0.17 \mu\text{m}$ gate length devices in [2.295, 2.296]. The $N_{F,\min}$ amounts to 1.1 dB at 10 GHz with an associated gain of 12 dB, measured at $V_{DS} = 10 \text{ V}$. The $N_{F,\min}$ at 18 GHz amounts to 1.75 dB. Low-power linearity of GaN HFETs on s.i. SiC is discussed in [2.364]. Overdrive testing and studies for the use of GaN LNA in synthetic aperture radar applications are presented, e.g., in [2.31]. MMIC-based LNA circuit examples on s.i. SiC substrates are given, e.g., in [2.31, 2.102]. These are further discussed later and in Chapter 6.

Indium-Based (H)FETs

The use of indium is also investigated in III-N heterostructure devices. Improvements in speed and effective mass similar to the (In)GaAs material system are targeted when indium is used in the channel. Further, the use of indium is discussed in order to reduce some of the high surface-charge density and strain issues causing dispersion, e.g., in [2.85, 2.284, 2.327]. The piezoelectric effects can be omitted for certain material compositions in InAlN/GaN HFETs. Further, the conduction band off-set is increased as compared to typical $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ HFETs [2.231]. HFETs can be realized in the (Al)GaIn/InGaIn, InAlN/GaN, and InAlN/InGaIn systems. In addition, indium can further be used as a dopant in AlGaIn/GaN HFETs to reduce interface roughness, e.g., [2.228, 2.240].

InAlN/GaN Heterostructure FETs

$\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ HFETs provide strong spontaneous polarization with very high sheet carrier concentrations $\geq 2 \times 10^{13} \text{ cm}^{-2}$ while the piezoelectric contribution is suppressed as the strain is minimized, as repeatedly stated [2.126, 2.186]. InAlN/GaN HFETs promise larger bandgap energies in the InAlN

barrier, a larger conduction band off-set at the channel interface, and thinner barrier layers [2.284]. The latter may be useful for the realization of mm-wave devices with high aspect ratio [2.126]. Very high drain current densities of 4.5 A mm^{-1} are expected for the InAlN/GaN HFETs [2.230], based on the high-sheet carrier concentration already demonstrated [2.84]. $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ single heterostructure HFETs grown by MOCVD on c-sapphire substrate are reported in [2.187]. With In contents $x = 0.04$ to $x = 0.15$ sheet carrier concentrations of $4 \times 10^{13} \text{ cm}^{-2}$ have been reached. For gate lengths $l_g = 0.7 \mu\text{m}$, cut-off frequencies $f_T = 11 \text{ GHz}$ and $f_{\text{max}} = 13 \text{ GHz}$ are achieved. The performance of InAlN/GaN HFET with 60 nm gate length and f_T values of 170 GHz is already discussed above [2.143]. Unstrained $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ HEMTs on s.i. SiC are reported in [2.126]. With a gate length $l_g = 250 \text{ nm}$ a cut-off frequency $f_T = 43 \text{ GHz}$ is reached with a DC-transconductance of 355 mS mm^{-1} and a barrier thickness of 7.5 nm . The power densities at 10 GHz reach 2 W mm^{-1} with an associated PAE of 29%. The pinch-off voltage is -1.7 V .

InGaN/GaN Heterostructure FETs

On the device level, GaN/InGaN/GaN double heterostructure FETs are demonstrated in [2.85]. These DHHEMT structures are considered to be more stable with respect to device dispersion, as mentioned in [2.327]. Kelvin probe microscopy shows no change in the surface potential of InGaN DHHEMTs contrary to AlGaN/GaN HFETs. Device characteristics of GaN/ $\text{In}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$ doped-channel double heterostructure HFETs are shown in [2.150]. The devices yield a maximum transconductance $g_{m,\text{max}}$ of 65 mS mm^{-1} , a maximum drain current of 272 mA mm^{-1} , and current gain cut-off frequencies $f_T = 8 \text{ GHz}$ and $f_{\text{max}} = 20 \text{ GHz}$ for a gate length of $1 \mu\text{m}$. The output power at 1.9 GHz is 26 dBm for a gate width of 1 mm , i.e., 0.4 W mm^{-1} . P-channel InGaN HFET structures based on polarization doping without external acceptor doping are discussed in [2.534]. The channel sheet carrier concentration is 10^{11} cm^{-2} with a hole mobility of $700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $T_L = 66 \text{ K}$. The maximum drain currents measured at room temperature (RT) are extremely low. MOSFET InGaN structures are also reported. AlGaN/InGaN/GaN DHFETs using SiO_2 as a passivation layer and gate dielectric layer yield a saturated output power density of 6.1 W mm^{-1} at 2 GHz and $V_{\text{DS}} = 30 \text{ V}$ [2.426]. The maximum transconductance $g_{m,\text{max}}$ amounts to 110 mS mm^{-1} for the MOSDHFET structure, while the simple DHFET structure yields 170 mS mm^{-1} . Pure InN/AlN MISFETs on Si(111) substrates are reported in [2.251]. A 26 nm -thick InN layer is grown by RF-plasma-assisted MBE (PAMBE) on AlN. A current density of $\geq 500 \text{ mA mm}^{-1}$ is reached with a very low breakdown voltage of 3 V and a threshold voltage of -7 V . These examples show the promising principle operation of indium-based FETs so far. The main emphasis of In-based development focusses on material growth, while the device development requires the suppression of leakage currents and the stabilization of the InAlN interface toward the dielectric.

2.5.6 Heterojunction Bipolar Transistors (HBTs)

The family of III-N-based field-effect transistors has been heavily exploited, as discussed in the previous sections. The use of bipolar transistors has also been considered; however, substantial hurdles have delayed the development of III-N-based bipolar devices. At the same time, very few reports exist on bipolar devices in the SiC material system, e.g. [2.532].

AlGaIn/GaN Heterojunction Bipolar Transistors

Complications with the p-doping in GaN [2.218,2.225] in epitaxial design [2.23] and issues with the processing [2.283] known from the optoelectronic devices have interfered with the successful development of bipolar AlGaIn/GaN transistors.

Performance Predictions of PNP- and NPN-Devices

Various theoretical predictions have been made about the possible performance of AlGaIn/GaN heterojunction bipolar transistors. Performance predictions for npn-Al_xGa_{1-x}N/GaN HBTs are given in [2.374]. Spontaneous and piezoelectric polarization are shown to have only minor impact on the device performance. Incomplete ionization and reduced activation of the base dopant are shown to be the main issues. Limiting factors and optimum design of npn- and pnp-AlGaIn/GaN HBTs have been addressed and performances have been investigated by simulation in [2.311]. Again, the high-base resistance induced by the deep acceptor level is found to be one of the causes of limited current gain values for npn-bipolar devices. The analysis for pnp-devices indicates limited RF-performance caused by the reduced minority hole transport across the N-GaN base. Simulations of the characteristics of AlGaIn/GaN heterojunction bipolar transistors are given in [2.234]. The 2D-simulations show the great potential of AlGaIn/GaN HBT with high calculated β , high breakdown voltage BV_{CE0} of 55 V, and a maximum cut-off frequency $f_T = 18$ GHz. Similar optimistic predictions are given in [2.7]. Generally, AlGaIn/GaN HBTs are discussed also for high operation temperatures, e.g., 300°C in [2.382], since the activation of the acceptor Mg-doping and the performance increase for higher operation temperatures. The measured current gain amounts to 10 for a 90 μm^2 device at this temperature due to the reduction of the base resistance.

AlGaIn/GaN Heterojunction Bipolar Transistors Fabrication

GaN/AlGaIn HBT fabrication issues are discussed in [2.383]. A standard III-V HBT process is applied to material grown by both MBE and MOCVD, while the annealing temperature of the ohmic contacts is increased to 700–800°C. Current gain levels of 10 are reached at elevated temperatures of 300°C for both material types. At the same time, the junction leakage is significantly

increased at high temperature. However, remaining issues include these leakage currents and the reduced base conductivity. The main performance problem for HBTs is thus the reduced current amplification [2.283,2.514]. Both the lifetime of 25 ps and diffusivity of electrons in Mg-doped GaN are found to be low compared to practical base width of, e.g., 100 nm. The collector leakage is correlated with the threading dislocation density. The maximum operation bias is 70 V. Selective area growth of AlGaIn/GaN HBTs is used in [2.413] to analyze its potential advantages as compared to more traditional growth techniques by normal MOCVD. Both linear ohmic contacts and improved material quality and interfaces could be obtained by the use of this more complicated technique applying a two-step procedure for the base contact. Very high voltage operation ≥ 330 V with a high current gain of AlGaIn/GaN HBTs using selectively regrown emitters on sapphire substrates is given in [2.513]. The high-breakdown voltage is attributed to the low-background doping level in the 8 μm -thick GaN collector and the suppression of leakage in the lateral base/collector junction due to etch damage in the 2–3 μm spacing. Further, the use of ELO growth, reducing the number of threading dislocations, significantly reduces the collector leakage [2.283]. Further analysis of the leakage currents is given in [2.514]. Anomalously high current gains at low current levels in AlGaIn/GaN can be observed. The calculated extrinsic β of the devices can be misleading due to leakage and ohmic contacts parasitic contributions, while the intrinsic performance is low due to purely intrinsic effects. AlGaIn/GaN HBTs thus have promising theoretical performance; however, this performance still cannot be exploited due to epitaxial and technological issues.

InGaIn/GaN Heterojunction Bipolar Transistors

The problems of p-doping of binary GaN can be overcome by using InGaIn as a base material. NPN-GaN/InGaIn/GaN DHBTs on s.i. SiC substrates with current gains of 3,000 can be fabricated [2.270]. This is ascribed to the lower acceptor activation energies and higher overall doping activation, e.g., in $\text{In}_{0.14}\text{Ga}_{0.86}\text{N}$ [2.225,2.269]. Active carrier concentrations of 10^{18} cm^{-3} can be achieved. The InGaIn is regrown by MOVPE in this case.

Base transit time analysis in GaN/InGaIn/GaN HBTs is performed in [2.70]. The contribution of the base transit time decreases with increasing temperature, while the collector transit time remains nearly constant. Similar to AlGaIn/GaN devices, this behavior makes the devices more suitable for high-temperature operation [2.152]. Double heterostructure GaN/InGaIn/GaN HBTs on s.i. SiC substrate are presented in [2.269,2.271] and several of the doping and processing issues are resolved. The breakdown voltage of the DHBTs in [2.271] exceeds 50 V, while a low current gain is observed without the application of regrowth. Further improvements of the epitaxy by using base regrowth [2.270] and improved processing yield a current gain $\beta = 2,000$ in [2.271] for an emitter geometry of $50 \times 30 \mu\text{m}^2$. The maximum current is as high as 80 mA. Based on these developments, the further development of

the GaN/InGaN (D)HBT is a promising candidate to overcome some of the epitaxial and processing limitations.

2.5.7 MMIC HEMT Technology

Apart from demonstrations on the device level, the demonstration of microwave integrated circuits (MICs) and monolithic microwave integrated circuits (MMICs) is a core competence for any RF-technology. The state-of-the-art is discussed in the following with focus on the III-N issues.

High-Power MMIC Technologies

Coplanar-Waveguide High-Power MMICs

Initial coplanar AlGaIn/GaN HEMT MMICs on s.i. SiC substrates are reported in [2.133] for broadband applications. The transmission-lines have impedance levels between 30 and 80 Ω . MMICs with saturated output power levels beyond 37 dBm are realized between quasi-DC and 8 GHz. Several demonstrations of high-power coplanar MMICs on s.i. SiC are available for X-band. They are given in detail in Chapter 6. Coplanar K-band MMICs on sapphire substrate are reported in [2.332]. The devices exhibit a small-signal gain of 10 dB and a 3 dB bandwidth of more than 4 GHz between 20 and 24.5 GHz. A 200 μm -thick SiN is used for the MIM capacitances, while WSiN is used for the resistors. Further details on the passive components are given in Chapter 8.

Microstrip Transmission-Line High-Power MMICs

The first complete microstrip transmission-line high-power MMIC technology on s.i. SiC for SiC MESFETs and AlGaIn/GaN HEMTs is presented by Cree in [2.362]. A 24 W high-power amplifier at 16 GHz is presented. Specific via etching techniques are required, which will be detailed in Chaps. 4 and 8. Triquint announces a full GaN HEMT MMIC technology on s.i. SiC with a saturated power density of 12 W mm⁻¹ at 10 GHz and an associated PAE=50% [2.467]. A similar microstrip MMIC process on silicon substrate is presented by Triquint in [2.109]. The silicon substrates are thinned to 100 μm in this case. The vias can be etched by standard Si processing equipment. The other passive components are not modified compared to the GaAs process. Further MMIC details are given in Chapter 6. At Ka-band, a comparison of both coplanar and microstrip line HEMT MMICs on s.i. SiC has been presented by HRL in [2.290]. The coplanar MMIC yields an output power of 1.6 W at 33 with 4 GHz bandwidth, while the MSL MMIC yields 2.2 W at 27 GHz with 8 dB gain between 24 and 32 GHz. When additional external tuning is used, a PAE of 27% is reached. The substrates are thinned to 50 μm . The via geometry is 30 $\times$ 30 μm^2 . A recent report by NGST gives a dual-stage

MMIC power amplifier in microstrip technology with a pulsed-output power of 11 W at 34 GHz. The duty cycle is very low and unusual for the telecom application [2.436, 2.439].

Low-Noise MMIC Process Technologies

GaN HEMTs are attractive for LNA MMICs due to high sheet carrier densities n_{sheet} and high intervalley energy (≈ 1.5 eV). One of the first GaN LNA MMICs is presented in [2.102]. A coplanar-waveguide dual-stage broadband LNA yielding a minimum noise figure of 2.4 dB and a gain of 20 dB between 3 and 18 GHz is presented in [2.102]. The devices are biased at $2.5 \text{ V} \leq V_{\text{DS}} \leq 4 \text{ V}$. The third-order intercept point is better than 34 dBm at 8 GHz, which demonstrates the good input linearity of the MMIC. The impact of linearity, high-input power levels, and a discussion of typical destruction levels in GaAs is given in [2.60]. Typical catastrophic destruction levels of GaAs PHEMT LNA MMICs amount to 20 dBm without additional circuitry [2.60]. GaN HEMTs with similar gate periphery can be driven to input power levels of 30 dBm without degradation of the output power. Further the exceptional linearity with an output intercept point of 43 dBm is proven. A full investigation of single- and dual-stage X-band LNAs, including linearity investigations, is presented in [2.220]. The trade-off between minimum noise figure at low $V_{\text{DS}} = 7 \text{ V}$ and good input and output linearity at high $V_{\text{DS}} = 25 \text{ V}$ is discussed. The noise figure of the full MMIC at X-band is mainly determined by the passive components. A coplanar C-band high-dynamic-range LNA MMIC has been presented in [2.515]. The noise figure is as low as 1.6 dB at 6 GHz and does not exceed 1.9 dB between 4 and 8 GHz. The input port of the circuit can endure up to 31 dBm of input power. The MMIC shows noise figures comparable to other semiconductor technologies, while the dynamic range and the survivability are strongly enhanced. A microstrip transmission-line technology on s.i. SiC substrate is used to demonstrate wideband dual-gate LNAs between 0.1 GHz and 5 GHz in [2.60]. A linear gain of 15 dB is found with a saturated output power of 33 dBm at a compression level at 13 dB. Further MMIC examples and design consideration are discussed in Chapter 6.

2.6 Applications Issues

A large number of possible applications has been suggested for III-N devices. Without taking into account all possibilities, some key applications are systemized in this section. A large number of overview papers have been provided on this issue in the literature. The impact of wide-bandgap microwave devices on defense and naval systems is discussed in [2.105, 2.189]. Specific overview articles on radar applications are given, e.g., in [2.104, 2.147, 2.263, 2.272]. The application in power systems is discussed in [2.470, 2.494]. Future directions and technology requirements of wireless communication systems are discussed, e.g., in [2.116, 2.309].

2.6.1 Broadband Communication

The most important nonmilitary application of III-N devices is the partial replacement of Si LDMOS transistors in base-station applications for mobile communication. For such broadband/multiband communication applications the following advantages for wide bandgap semiconductors are typically named:

- The increase in relative bandwidth for a given power level
- The higher output impedance level to match, i.e., higher impedance and reduced C_{ds} per unit gate width for load matching
- Increased efficiency through new circuit and system concepts
- Improved linearity for the same output power
- Thus increased linear output power
- A Reduction of memory effects
- Potentially, less effort for the thermal management based on high-temperature operation

Examples for the development of device and amplifiers in L-band and S-band are given in Chaps. 2 and 6.

2.6.2 Radar Components

The particular application of III-N solid-state high-power amplifiers and low-noise amplifiers is discussed for radars for several reasons. The particular applications include:

- Active electronically scanned arrays (AESA)
 - For airborne radars [2.104, 2.272],
 - For ground-based air defense radars [2.272],
 - For naval radars [2.147]
- For airborne and spaceborne reconnaissance systems, e.g., [2.263]

Radar applications are the main drivers in the development of the III-N electronic materials. The fundamental improvements through the use of wide bandgap amplifiers involve on the system level:

- Better power×aperture gain [2.535]
- The possibility of high-power ultra-wideband (UWB) systems [2.147, 2.272]
- And higher reliability and survivability

The resulting improvements on the device and module level for defense applications include:

- Increasing power-added efficiency on system level by the increase of operation bias
- Elevated temperature operation allowing for reduced cooling [2.147]
- Reduced cooling through higher junction temperatures [2.124]

- Reduced limiter usage in the receiver path [2.272]
- Increased absolute output power levels [2.147]
- Improved reliability and increased system availability due to graceful degradation [2.263]
- Higher robustness with respect to supply voltage variations [2.263]
- Possibly the use of modulation schemes for increased functionality [2.147]

The frequency ranges involve S-band, C-band, X-band [2.104], and potentially Q-band [2.384]. Ultra broadband electronic warfare applications will further involve the range from 6–18 GHz [2.272]. In addition, Ka-band missile applications at 35 GHz are being discussed [2.179].

2.6.3 Electronics in Harsh Environments

As for other wide bandgap materials, nitride semiconductors have been suggested for their application in harsh environments, such as:

- Airborne operation [2.147]
- Space applications with high radiation levels, elevated temperatures, and strong temperature gradients [2.263]
- Space applications with requirements for reduced volume, reduced weight, and energy consumption [2.263]
- Car engines, i.e., microwave ignition [2.252] and energy-efficient DC–DC-conversion [2.470]

The particular functions include:

- RF-power sources and power generation [2.180]
- Highly linear RF-mixers [2.13]
- Robust RF-receivers [2.262, 2.364]
- DC–DC-conversion [2.470]
- Chemical sensors [2.365]
- Fluid sensors [2.285], biogen sensors [2.365], and (combustion) gas sensors [2.200, 2.365, 2.402, 2.458]
- Pressure sensors [2.175]
- Strain sensors [2.365]

A good overview of the sensor capabilities of GaN, especially with respect to its pyroelectric capabilities, is given in [2.10]. A sensor array using conventional semiconductor arrays for the operation regime between 200°C and 400°C is given in [2.461]. Various gaseous constituents can be discriminated. Gas sensors for hydrogen and propane are reported, based on MOSFETs in [2.176], and, based on n-type GaN and Pt-based Schottky contacts operating at 400°C, in [2.265]. Pressure sensors based on the pressure-induced conductivity changes in AlGaN/GaN HEMTs on Si substrates are reported in [2.175]. The pressure dependence can be used in pressure sensing applications; however, the pressure dependence poses also serious consequences on

the variation of the wafer bow and overall strain when dicing and handling the device.

2.7 Problems

1. Summarize the substrate situation for III-N electronic devices.
2. Given all the advantages named in the text, name at least three technical disadvantages of III-N semiconductors with respect to epitaxy and technology.
3. Name the advantages of double heterostructure devices relative to single heterostructure devices.
4. To this date, what are the shortcomings of AlGa_N/Ga_N heterostructure bipolar transistors?
5. Do you expect a difference for of unipolar and bipolar devices with respect to the influence of the substrate? Discuss!
6. Calculate the cross-section of a copper wire to be able to transport 1 W of DC-power for an operation bias at 5 V and at 50 V.

Epitaxy for III-N-Based Electronic Devices

Epitaxy is a core competency for the production of III-N devices. In this chapter, growth procedures for gallium-, aluminum-, and indium-based binary and ternary compounds are described with emphasis on AlGa_N/Ga_N-, InGa_N/Ga_N-, and (In)Ga_N/InAl_N-based heterostructure systems. Nitride-specific material characterization, doping, and material quality issues are analyzed. Unlike Chapter 2, this chapter systematically reviews substrate properties with respect to the requirements of electronic device growth. This chapter mainly addresses the growth of both metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). In general, MOCVD growth of Ga_N is performed at much higher temperatures (well above 1000°C) than MBE growth, which is typically performed at temperatures of about 700°C [3.205,3.206]. MBE growth enables the growth of very precise interfaces, which improve transport properties. The two methods can also be combined, e.g., to a methodology called migration-enhanced MOCVD, as described, e.g., in [3.44]. Other techniques such as hydride vapor phase epitaxy (HVPE) have also been mentioned, but do not play a dominant role for the fabrication of the active layers.

Surface Preparation

Specific surface preparation methods have been developed, which improve the surface roughness before epitaxial deposition and are used prior to the actual growth procedure. Further, specific procedures assure that the reactor spaces are not contaminated by extrinsic pollution. Standard surface-polishing techniques are based on plastic deformation by an abrasive, e.g., diamond. Electrochemical–mechanical polishing procedure (ECMP) improves the reproducibility of the epitaxial growth and is preferred to purely mechanical polishing (CMP), as the induced subsurface damage is reduced. A proprietary ECMP process of SiC applied by NovaSiC is mentioned in several publications, e.g., in [3.154,3.162,3.216]. A full description of a two-step ECMP procedure is given in [3.112]. The procedure is characterized by a balance of anodic oxidation and oxide removal [3.216] to obtain a defect-free surface of the substrate.

A high-temperature hydrogen etching process is used to further smooth the surface to atomic levels. On the device level, a correlation of the gate-leakage current and substrate defects in 2-in. SiC substrates is given in [3.126]. A clear correlation showing a reduced yield of the FETs for an increased defect density in a particular area is visible. The increased defect concentration in selected areas of the wafer leads to a statistical increase of the gate leakage current of about 100% measured at $V_{DS} = 20$ V.

Substrate Surface Cleaning and Backside Metallization

Further wafer preparation includes the deposition of a Ti layer on the backside of the transparent substrate prior to growth to provide an effective heat transfer [3.162], typically for MBE growth only. A sputtered Mo thermal-contact layer is used for ammonia MBE in [3.213]. Various surface heating procedures have been reported for the in-situ preparation of the substrates within the reactor chambers or preparatory chambers. Prolonged heating of Si(111) for up to 10 h at 600°C with subsequent oxide removal by rapid thermal annealing is reported, e.g., in [3.180]. An ex-situ exposure to hydrogen at 1,600°C is reported in [3.205] prior to an in-situ surface cleaning by Ga deposition and desorption within the reactor chamber. The impact of reactor loading leakage and the impact of the contamination of sapphire substrates is discussed in [3.94]. Various cleaning conditions and sequences with prebake and flush for moisture removal prior to growth are discussed. A potential reaction is the composition of H_2O from hydrogen and Al_2O_3 . Oxygen incorporation serving a shallow donor is considered a major obstacle for semi-insulating GaN. The investigation includes a prebake of the sapphire and a flush of the substrates by hydrogen between 10 min and 12 h. The optimized procedure includes both the prebake in-situ and no flush, and is critical in order to obtain semi-insulating GaN buffers.

3.1 The AlGaIn/GaN Material System

The growth of AlGaIn/GaN heterostructures is a basic technology for the production of high performance HEMT and HBT devices. General overview articles and comparisons between the various growth methods for the AlGaIn/GaN system are given, e.g., in [3.36, 3.39, 3.138]. An overview of MBE growth of AlGaIn/GaN heterostructures is given in [3.172].

3.1.1 Metal Organic Chemical Vapor Deposition (MOCVD)

Metal organic chemical vapor deposition (MOCVD) is the name of a growth technique that involves a dynamic flow in which gaseous reactants pass over a heated substrate and react chemically to form a semiconductor layer [3.36]. It is widely spread for the fast and precise growth of many III-V materials,

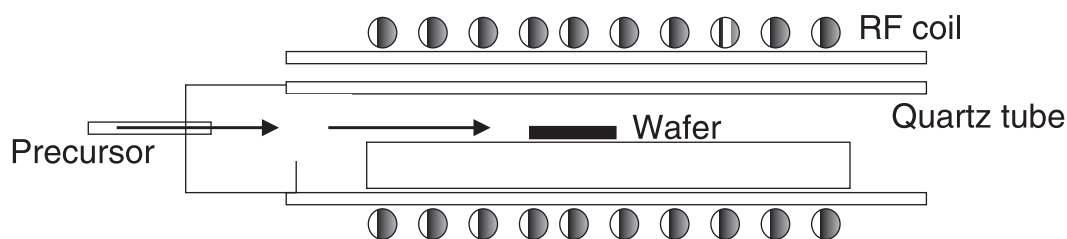
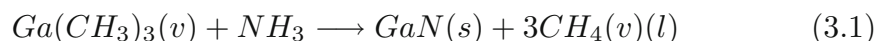


Fig. 3.1. Scheme of metal organic chemical vapor deposition (MOCVD) growth

e.g., for InGaP/GaAs [3.156] and In_{0.53}Ga_{0.47}As/InP [3.61]. III-N MOCVD-based material growth is very attractive due to the large amount of experience and success available from the growth of optoelectronic devices, e.g., [3.141], and the increased growth rates relative to molecular beam epitaxy (MBE). Thus, MOCVD is widely used for the growth of heterostructures for electronic applications [3.94]. Fig. 3.1 gives a schematic view of MOCVD growth of III-N materials. The precursors TriMethyl-Gallium (TMGa), TriMethyl-Aluminum (TMAI), and TriMethyl-Indium (TMIn) react with ammonia (NH₃) on the hot substrate surface to form semiconductor layers. Additional sources such as nitrogen, silane (SiH₄), disilane (Si₂H₆) [3.48], and Bis(cyclopentadienyl) magnesium (Cp₂Mg) sources [3.105,3.121] are needed. The substrate is located on top of a graphite susceptor. Various reactor concepts have been developed [3.1,3.142] to accomplish and optimize the laminar flow of gases on larger area surfaces [3.7] and within multi-wafer concepts, e.g., in [3.48,3.192,3.221]. Both reactor concept and geometries, often kept proprietary, influence the growth conditions to a high extent. This fact also limits the comparability of parameters such as growth temperature, gas flows, and others parameters, which are adjusted externally. However, a principal understanding of the requirements for III-N growth can be obtained.

Growth Chemistry

The growth kinetics and chemistry of III-N semiconductors by MOCVD are described in various publications which shall be briefly mentioned here [3.138,3.167,3.169,3.172]. The details of the complex reactions are not fully understood and especially the intermediate reactions are found to be very complex. The principal reaction to form GaN reads [3.142]:



A similar reaction occurs for AlN(s) replacing gallium by aluminum. The chemistry is governed by strong reactions of the precursors at room temperature. Further ammonia requires pyrolysis, which is not very efficient. Thus, high growth temperatures beyond 1000°C are used along with high V/III-ratios (>1000) and high gas velocities.

Optimized Conditions for MOCVD Growth

One of the key advantages for the AlGaIn/GaN material system is based on the fact that the complete range of solid solutions from GaN to pure AlN is available using MOCVD growth. Typical growth rates for GaN are about $2\text{ }\mu\text{m h}^{-1}$ [3.219]. Overview articles of the development of the growth conditions of AlGaIn/GaN heterostructures are reported, e.g., in [3.34, 3.92, 3.168]. The aluminum content or mole fraction x in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ /GaN heterostructures is varied between 0 and 0.6 in [3.92]. The defect density in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer on GaN is found to increase significantly for $x \geq 0.3$ for typical barrier thicknesses of 18 nm for AlGaIn/GaN HFETs. Further, the mobility in GaN channels along AlGaIn/GaN hetero-interfaces decreases with decreasing barrier-layer thickness and with increasing Si-doping concentrations. Sheet carrier concentrations of $1.8 \times 10^{13}\text{ cm}^{-2}$ are reached at $x = 0.44$. The AlGaIn-spacer thickness between the channel and the Si-doped barrier layer is varied between 0 and 3 nm. A mobility of $1,650\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at RT is found for 3 nm thickness. The sheet carrier concentration decreases from 1.5 to $0.8 \times 10^{13}\text{ cm}^{-2}$ with the increase of spacer thickness from 0 to 3 nm. Very good layer properties and reproducibilities have been reported for optimized growth conditions on two-inch and three-inch wafers, e.g., in [3.221]. The wafer-to-wafer variability of the sheet resistance mapping is $\leq 3\%$ on 3-in. s.i. (0001)SiC wafers. The critical growth parameters will now be discussed in detail.

Growth Temperature Schemes: Nucleation and Buffer for MOCVD

The growth temperatures critically determine the properties of the semiconductor layers. A typical temperature scheme for the growth of an AlGaIn/GaN heterostructure sequence is given in [3.94]. On sapphire substrates, a 15–25 nm thick AlN nucleation layer is used in a growth temperature range of 500°C to 700°C . The consequent growth of the main GaN buffer layers is performed at $\geq 1,000^\circ\text{C}$. For all temperatures, the changes of the growth temperature due to different thermal contacting at the backside of the substrate have to be considered. A GaN nucleation temperature of 550°C on 2-in. sapphire substrate is reported in [3.218]. A slightly misoriented grain morphology is obtained, which results in poor electrical properties. Growth at a temperature of 530°C for the nucleation layers is reported in [3.192] on 3-in. sapphire substrates. The growth of AlN as a nucleation layer on sapphire substrate with a temperature of 500 to 700°C is reported in [3.219]. Above the AlN nucleation layer, all layers are grown at much higher temperatures, especially the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ heterobarrier. AlGaIn-based nucleation layers for growth on s.i. SiC substrates are reported in [3.185]. Defect-poor surfaces on top of GaN buffer layers with thicknesses up to $5\text{ }\mu\text{m}$ can be observed optimizing the alloy composition and thickness of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ nucleation layers. The deposition temperatures of the $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ nucleation layer amount to $1,010^\circ\text{C}$ on s.i. SiC and $1,040^\circ\text{C}$ on sapphire for the same nucleation. The minimum Al-content is 6% for SiC nucleation and 15% for the nucleation on sapphire.

AlGaN nucleation on s.i. SiC substrates has also been reported in [3.102]. The thickness of the nucleation layer is 500 nm, followed by the GaN buffer. Growth of AlN nucleation layers on SiC is another standard procedure and has repeatedly been investigated, e.g., in [3.103]. The temperature is varied in [3.103] depending on the crystal structure of the n-type SiC substrate: A nucleation temperature of 1,080°C is used for the 6H-SiC substrates, while 980°C is used for 4H-SiC substrates. The thickness is 100 nm in both cases. The hotter growth for the 6H-SiC substrates shows smaller grains than for the growth on 4H-SiC, which means that the morphology of the AlN influences the quality of the subsequent layers. The specific nucleation of III-N materials on Si substrates is discussed below.

Growth Temperature Schemes: Channel and Barrier

The substrate temperatures reported for the growth of conducting GaN by MOCVD typically exceed 1,020°C [3.219]. The associated growth rate is $1.2 \mu\text{m h}^{-1}$. A growth temperature of 1,080°C for the growth of the main GaN layer is reported using hydrogen as a carrier gas in [3.93] on sapphire substrates. Growth temperatures of 1,180°C are reported for the GaN channel and the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ heterobarrier in [3.174] on sapphire substrates. An analysis introducing additional layers in the buffer layer is given. The growth temperature is chosen accordingly for Al-, In-, and Ga-based binary and ternary semiconductors within the interlayer. A temperature of 1,125°C for the growth of $\text{Al}_{0.33}\text{Ga}_{0.67}\text{N}$ in the heterostructure is reported in [3.93]. The impact of the variation of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ growth temperature between 1,060 and 1,125°C is reported in [3.92]. The Al-incorporation changes from 0.37 to 0.42 at otherwise constant conditions with the variation of the growth temperature from 1,060 to 1,125°C. Hot growth of the AlGaN layer is considered promising in [3.93] with respect to the output power, while a termination of the growth in the cool-down using nitrogen is found to be most suitable, again with respect to output power considerations of the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{N}/\text{GaN}$ HEMTs realized on SiC. Highly-resistive thick $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ layers grown by MOCVD at 1,150°C are reported in [3.23]. When the growth temperatures of $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ are reduced to 920°C and silicon and indium codoping are applied, highly conductive $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ layers are reported. Mobility values of $22 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and bulk carrier concentrations of $2.5 \times 10^{19} \text{ cm}^{-3}$ are reached. The termination conditions of the semiconductor surfaces are discussed below with the specific methodology, e.g., cap layers [3.30, 3.93], or in-situ passivation layers, see [3.133].

MOCVD Gas Flow and Group V/III Ratio

Similar to the growth temperature discussed in the previous section, the element group-V/group-III ratio is of critical importance for the material properties. A nitrogen-rich growth is necessary in general because of the very different

chemical bindings and, to a lesser extent, different atomic weights of the constituents N and group III-metals [3.142]. The absolute and relative gas flows and pressures are quantities that are strongly dependent on the susceptor and reactor geometries. Several reactor-specific investigations are available in the literature, e.g., in [3.1, 3.23, 3.92]. Optimization of the GaN nucleation layer on sapphire substrates as a function of nitridation conditions, group V/III ratio, growth temperature, and growth pressure is discussed in [3.218]. TMG flows of $32 \mu\text{mol min}^{-1}$ and NH_3 flows of $0.09 \text{ mol min}^{-1}$, i.e., N-rich conditions, are reported for GaN growth. The V/III ratio is thus 2,775. A group V/III ratio of 1,800 for GaN growth and 900–1,800 for AlGaIn growth by MOCVD are reported in [3.39] for $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}/\text{GaN}$ heterostructures on SiC and sapphire. A group V/III ratio of 2,000–2,600 is reported in [3.219] for the growth of GaN. In a comparison of two reactor concepts, a V/III ratio of 2,660 is reported for the growth of the GaN channel-layers on AlN nucleation layers in a so-called showerhead reactor in [3.219]. In a second quartz tube reactor, a group V/III ratio of 2,000 is used for the same TMG flow of $23 \mu\text{mol min}^{-1}$. A V/III ratio of 2,100 is reported for GaN growth at a growth temperature of $1,030^\circ\text{C}$ in [3.218]. The V/III ratio is increased to 2,775 for a growth temperature of $1,065^\circ\text{C}$ to accommodate for the increased N-desorption.

Growth Pressure

The pressure in MOCVD is the most fundamental parameter next to temperature and V/III ratio. It basically determines the incorporation of the various constituents like the group-V and group-III materials, including group-IV dopants like Si and C. The influence of growth pressure on the morphology and carrier compensation in GaN and related alloys is described, e.g., in [3.219]. For very low pressures of 40 Torr, the GaN layers are highly resistive and yield very low carrier mobility nearly independent of the growth temperature. Very high growth pressures at 200 Torr and beyond lead to the loss of the resistive nature of GaN, e.g., at atmospheric pressure [3.6]. In an intermediate growth pressure range, both high mobility and high resistivity (i.e., low nonintentional doping) can be reached in GaN Layers. Optimized growth pressures of 130 and 65 Torr are reported for GaN layers [3.219].

Similar reports of a pressure of 76 Torr are given in [3.39] for $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}/\text{GaN}$ heterostructures, and 100 mbar for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ HFET layers [3.48]. Further results at a growth pressure of 76 Torr are reported in [3.218] for the growth of the GaN nucleation layer on sapphire, while 150 Torr is used for the rest of the layers. This pressure, at which pressure prereactions occur, is strongly dependent on the reactor geometry. This critical pressure is found to be 150 Torr for GaN for the reactor used in [3.218]. For the growth of $\text{Al}_x\text{Ga}_{1-x}\text{N}$, the pressure dependence is modified depending on the Al mole-fraction [3.92]. For a given V/III ratio and growth temperature, the Al-mole fraction is particularly influenced by the partial pressures of Al and Ga, and their deviation from the equilibrium partial pressures, as further detailed in [3.92]. Thus, lower pressures than for optimized GaN layers

are needed for good Al-incorporation in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layers, as reported in [3.219]. A medium growth pressure of 76 Torr is reported in [3.94, 3.185] for the growth of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$, due to the tendency of TMAI to form adducts with ammonia. At this pressure of 76 Torr, such prereactions are still not fully suppressed. Again, their occurrence is again strongly reactor-dependent. Relatively high pressure of 300 mbar is reported for the growth of $\text{Al}_{0.33}\text{Ga}_{0.67}\text{N}/\text{GaN}$ heterostructures in [3.93]. The high pressure growth also leads to increased incorporation of nonintentional doping such as C and Si.

Crystal Misorientation

The control of the misorientation of the substrate as compared to the III-N layers is of further importance for the layer quality. Growth of GaN on both on-axis and off-axis 6H-SiC substrates is reported in [3.103]. A 3.5° off-axis 6-H substrate is used for comparison. A strong impact on the surface conditions has been repeatedly reported, e.g., [3.103]. However, the impact of the misorientation on electronic device performance is not yet fully understood. This is due to the lack of SiC substrates that are oriented according to tight specifications with respect to the misorientation.

The slight misorientation from c-plane (0001)-sapphire substrates is well investigated for optoelectronic applications [3.58]. The emission from the photoluminescence of material on misoriented substrates is higher than for the on-axis material. The impact on GaN LED output power is further investigated in [3.228]. For the misorientation of 0.17° the morphology changed to small-step-type morphology. However, the optical output powers of the GaN LEDs are nearly identical despite the misorientation. The impact of the different optical surface properties has also to be considered.

For 4H-SiC and 6H-SiC substrates reports on the impact of the misorientation on layer and device performance are available [3.145, 3.171, 3.189, 3.195]. MOCVD-grown GaN epitaxial layers show a good morphology for on-axis substrates, while the crack density increases with the increase of the misorientation in [3.171].

This effect can be overcompensated by other growth parameters, such as the growth temperature, as shown for GaN diodes on 4H- and 6H-SiC in [3.145] and for heterostructures in [3.103]. An increase of the mobility and a carrier reduction in Si-doped GaN films is obtained with a slight misorientation of 3.5° compared to the on-axis layer. Positron annihilation spectroscopy shows that with increasing misorientation on 4H-SiC the concentration of nitrogen vacancies in GaN increases, while the number of shallow traps decreases [3.195]. This can potentially have an impact on device isolation in the buffer layer, if the misorientation is not controlled. With the application of MBE growth the importance of the misorientation rises, as described in [3.189]. The morphology of GaN grown on 4H-SiC(0001) with a very strong misorientation of 8° is strongly affected by undulations, while this not the case for a misorientation of $\leq 0.3^\circ$. Deduced from that, a controlled misorientation

can be useful for the electronic device performance, if the growth parameters are properly matched.

Nucleation Layer

The conditions for the growth of the nucleation layer are critical for the defect concentrations, residual conduction, and the distribution of the defects and traps in all layers grown on top of it [3.103,3.185]. The nucleation layer is naturally highly dependent on the substrate choice. Several nucleation approaches have been suggested, both AlGa_N (on SiC and sapphire), Ga_N (on sapphire), and AlN (on SiC and sapphire) nucleation have already been mentioned. The use of insulating AlGa_N nucleation layers for the growth of AlGa_N/Ga_N heterostructures on s.i. SiC and sapphire substrates is described in [3.185]. The nucleation layer thickness is 180 nm in this case. The TDD is about $5 \times 10^9 \text{ cm}^{-2}$. The impact of the nitridation and nucleation conditions of the growth on the low-temperature Ga_N nucleation layer on the morphology on sapphire substrate is investigated in [3.218]. Dislocation densities estimated by XTEM of less than 10^8 cm^{-2} are reported for a 2 μm thick Ga_N layer. The grain orientation can be improved with increased nitridation temperatures. Further, the quality of the epitaxial Ga_N is improved by increased growth temperatures and pressures. In [3.219], AlN nucleation layers are grown on sapphire substrates. Thicknesses of 20 nm are fabricated at a growth temperature of 500–700°C. The TDD varied only slightly with values of $1\text{--}2 \times 10^9 \text{ cm}^{-2}$. The nucleation on s.i. SiC can also be performed with AlN nucleation. The thickness of the nucleation layer is 120 nm in [3.183], which is higher than that for AlN nucleation on sapphire. The temperature dependence of the nucleation with AlN on SiC has already been discussed [3.30]. The AlN thickness is 100 nm in this case. The optimization of the nucleation layer is further monitored by the drain-lag type of pulsed-measurements for processed HFETs, as discussed in Chapter 5.

Buffer Isolation

The growth of the buffer layer in an AlGa_N/Ga_N heterostructure is basically a trade-off between high isolation and surface morphology. For the buffer isolation, a minimum isolation requirement of $1 \times 10^7 \Omega \text{ cm}$ – $10^{11} \Omega \text{ cm}$ is suggested in [3.40,3.139]. Earlier examples include values of $10^5 \Omega \text{ cm}$ in [3.219] for high-resistivity Ga_N layers. The impact of the growth temperature of a Ga_N buffer between 1,070 and 1,150°C is discussed in [3.139]. Buffer isolation resistances between 10^4 and $10^{11} \Omega \text{ cm}$ are reached. Relatively higher growth temperature yield increased isolation in this regime. Further, it is mentioned that the isolation reduces by an order of magnitude when the test bias is switched from 2 to 40 V. The impact on surface morphology is also discussed in a trade-off, as hotter growth temperatures increase the surface roughness.

Buffer-Layer Thickness

The overall thickness of the epitaxial layers in the hetero-epitaxy is determined by the buffer layer, which varies between 350 nm [3.5], approximately 3 μm , e.g., in [3.139] and 5 μm in [3.132]. The impact of buffer layer thickness is discussed in more detail in [3.5]. A minimum thickness of 350 nm is used. The thickness is varied in the following trade-off. Thin buffer layers promise reduced thermal impedance and low growth time, while the growth of thicker layers reduces the effect of threading dislocation density TDD and the effect of the residual strain from the lattice-mismatch [3.132]. Further, the surface morphology improves for the buffer thickness between 2 and 3 μm on sapphire substrates, as mentioned in [3.40]. Ga_N buffer layers grown by MOCVD with thicknesses up to 5 μm are reported in [3.132]. Thicker buffer layers promise smoother growth fronts with improved interface roughness, reduced dislocation density, and further removal of the active region from the defective nucleation layers. The negative impact of thicker buffers on the thermal resistance to the substrate is further discussed in Chapter 8. The impact of various buffer materials and interlayers, such as InGa_N, AlGa_N, and Ga_N, on wafer bowing, grown in various ways by MOCVD, is discussed in [3.174]. In general, multi-layer structures are found to enhance wafer bowing, see [3.5]. Recent reports demonstrate the introduction of thin (3 nm) InGa_N layers in the buffer layer very close, i.e., at a distance of 10 nm, to the channel layer [3.154]. This is achieved in order to obtain a similar function as a real double heterojunction structure. A graded Al_{*x*}Ga_{1-*x*}N-buffer approach grown by MOCVD is presented in [3.78]. The mole fraction *x* is varied from 0.3 at the nucleation layer to 0.05 near at the buffer channel interface. The thickness of the graded layer is 1 μm , the Ga_N channel thickness is 10 nm.

Codoping of the Buffer Layers

Unintentional codoping is a major problem for nonoptimized growth conditions [3.23, 3.94] in III-N semiconductors. Codoping introduces nonintentional background carrier concentration and thus persistent nonintentional conductivity. This fact has been the reason for a number of publications [3.6, 3.23, 3.94]. Nitrogen vacancies and oxygen serve as shallow donors [3.94] typically considered for Ga_N layers. Carbon prevails in the MOCVD reactor due to the methyl-precursors [3.28]. Mg and Fe are intentional dopants of interest, which, however, can be residual from reactor memory effects. In a number of the high-performance single-heterostructure devices, Fe or C [3.6, 3.63] are used to control the isolation in the buffer by pinning and thus stabilizing the Fermi levels through deep acceptors [3.28]. This codoping is one method used to control the Fermi-level in the buffer and to overcome the need for a second heterojunction. In [3.64], the use of Fe doping for applications in AlGa_N/Ga_N HEMTs is described to improve the stability of the semi-insulating Ga_N layers and to reduce dispersion, especially the drain-lag. At the same time, the Fe doping does not modify the good structural quality of the layer. Thus the

improved isolation is achieved without a high TDD necessary to obtain good isolation without codoping. The impact of high-temperature rapid thermal annealing (RTA) on the properties of Fe-doped semi-insulating GaN is investigated in [3.164] at temperatures between 750 and 1,050°C. The Fe distribution is found to be nonuniform and to increase close to the interfaces. The Fermi-level is pinned at $E_C - 0.5$ eV. The paper also states a strong residual gradient and diffusion of the Fe concentration in the buffer layer, partly based on a memory effect [3.15]. The reduction of dislocation density on both sapphire and s.i. SiC substrates through intentional Fe codoping is investigated in [3.15]. High-resistivity layers are obtained by both modulation doping and continuous bulk Fe-codoping. The Ferrocene flux is modulated to overcome the maximum doping level of $1 \times 10^{19} \text{ cm}^{-3}$. A more detailed study of the Fe doping at the regrowth interface of GaN on a GaN on sapphire template is given in [3.111]. The Fe doping of the interface is found to be crucial for the quality of the transistor layers on top of a 2- μm thick buffer. These thick Fe-doped layer leads to good mobility and increased carrier concentrations in the active transistor layers while no charge is found at the regrowth interface.

The impact of the excess incorporation of carbon on the trap states in MOCVD-grown material is investigated in [3.6]. Low-pressure growth at 76 Torr, compared to 760 Torr, leads to increased C incorporation in the GaN layers grown at 1,040°C. Carbon is considered to supply shallow but also deep acceptor levels in n-type GaN. This carbon contributes to the compensation of free carriers. C-doped samples are found to be highly resistive, while codoping with both Si and C leads to highly compensated layers. This finding is of critical importance, as O and C are typically present in any MOCVD reactor chamber. Oxygen incorporation during MOCVD growth is investigated in [3.23]. Higher growth temperatures at 1,150°C lead to reduced oxygen and carbon incorporation at levels of 10^{17} cm^{-3} , while the incorporation of carbon and oxygen can be strongly correlated. Growth temperatures of 920°C for $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ lead to oxygen concentrations of up to $1.5 \times 10^{19} \text{ cm}^{-3}$ and carbon concentrations of $1 \times 10^{18} \text{ cm}^{-3}$. In-codoping further suppresses the formation of native defects with acceptor character. Doping compensation is further of critical importance for the device behavior at high voltages, as explained in Chapter 5.

Dislocations in MOCVD Material

The threading dislocation density (TDD) was already discussed with the lattice mismatch in Chapter 2. The TDD is naturally dependent on the substrate type and quality. TDDs of $\approx 5 \times 10^8 \text{ cm}^{-2}$ on s.i. SiC substrates and of low 10^9 cm^{-2} on sapphire substrates are reported for both MOCVD and MBE material in [3.39, 3.185]. These numbers are confirmed in a variety of publications, e.g., [3.36, 3.92]. MOCVD-grown material is analyzed by combined scanning capacitance microscopy and AFM measurements in [3.60]. Threading dislocations are found to be surrounded by a negative charge.

A TDD of $2 \times 10^9 \text{ cm}^{-2}$ is mentioned for optimized MOCVD-based epitaxy of AlGaIn/GaN on 4-in. silicon(111) substrate [3.204]. A good overview on the strain engineering on Si(111) is given in [3.34].

Epitaxial lateral overgrowth (ELOG) by MOVPE allows a reduction of the TDD below $\leq 10^9 \text{ cm}^{-2}$ on sapphire substrates, as reported, e.g., in [3.86]. The leakage in AlGaIn/GaN HBTs is reduced by an ELOG procedure with a concentration of threading dislocations of 10^8 cm^{-2} in the defect-reduced part. Areas with TDDs reduced to $\leq 10^6 \text{ cm}^{-2}$ in the defect reduced part are reported in [3.86]. However, these stripes are typically $10 \mu\text{m}$ wide only. The use of ELOG of GaN on conducting 6H-SiC substrates can yield dislocation densities as low as $2.2 \times 10^7 \text{ cm}^{-2}$ in the wings (i.e., the defect-reduced area) and $2 \times 10^9 \text{ cm}^{-2}$ in the windows (defect-rich area), as reported in [3.53]. GaN laser growth requires a TDD of 10^6 cm^{-2} obtained with an effective lattice mismatch of 0.01% to the heterosubstrate [3.34]. The TDD in bulk AlGaIn grown by MOCVD on SiC substrates for solar blind detectors is found to be higher than in GaN layers. The overall TDD (mostly edge type) reach $2\text{--}5 \times 10^{10} \text{ cm}^{-2}$ in the AlGaIn, as shown in [3.157].

Partial dislocation annihilation by Si- δ -doping in GaN grown by MOCVD on silicon substrates is described in [3.31]. Screw dislocations are bent to neighboring dislocations, whereas edge dislocations are not affected by the burst of silicon during the growth. Fig. 3.2 depicts a GaN layer grown on sapphire(0001) ($\alpha\text{-Al}_2\text{O}_3$) substrate to give a more qualitative image of the dislocation density. The GaN layer is etched by a photo-enhanced chemical (PEC) etching technique. The different etch rates in the area of the dislocations can be observed. Further, the extension of the dislocations is visible reaching 500 nm into the GaN layer. This fact requires a minimum buffer layer thickness to protect the actual device layers.

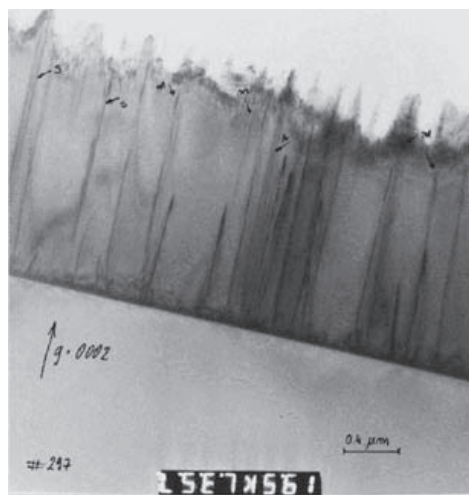


Fig. 3.2. SEM image of a PEC-etched GaN buffer on sapphire substrate

Impact of Growth on Carrier Mobility

Fig. 3.3 gives the temperature dependence of the drift mobility especially for temperatures lower than RT. Various mechanisms that influence the electron mobility can be separated. Data for both 2DEG AlGaN/GaN heterostructures and bulk GaN are given. The different contributions to the mobility lead to the overall mobility. The limiting effects dominating at different temperatures are the following:

- Impurity scattering dominating from below 70 K [3.144]
- Polar optical phonon scattering dominating above 70 K [3.21, 3.144]
- Acoustic phonon scattering [3.65, 3.101]
- Dislocation scattering
- Polar dipole scattering
- Interface scattering [3.4]

Impurity and polar optical scattering are the classical scattering mechanisms to reduce the mobility in the bulk, as described in [3.21], see Fig. 3.3. Acoustic phonon scattering is discussed in [3.65, 3.101] and found to be of significance. It can be distinguished from the other scattering mechanisms at temperatures below 20–50 K and plays a role in AlGaN/GaN heterostructures. Peak mobilities in 2DEGs of $80,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 4 K are observed for sheet carrier concentrations of $0.4 \times 10^{12} \text{ cm}^{-2} \leq n_{\text{sheet}} \leq 3 \times 10^{12} \text{ cm}^{-2}$ [3.65].

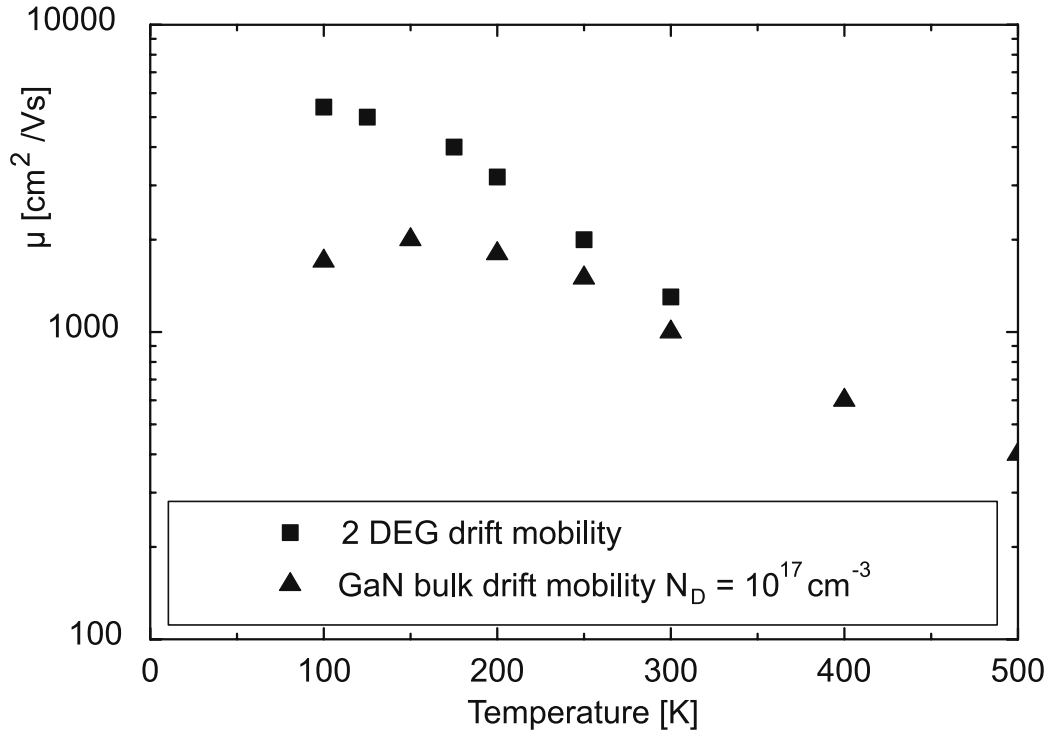


Fig. 3.3. Drift mobility as a function of lattice temperature in MOCVD material

Thus, for the III-N heterostructures, additional mechanisms prevail, which limit the mobility and which are discussed in [3.4, 3.80, 3.81]. Interface scattering is found to be relevant for carrier densities $\geq 7 \times 10^{12} \text{ cm}^{-2}$ [3.4]. For lower sheet carrier densities than $7 \times 10^{12} \text{ cm}^{-2}$, the mobility is limited by the interface charge and the related Coulomb scattering. Theoretical approaches to the additional dislocation scattering [3.80] and dipole scattering [3.81] are suggested. Dipole scattering of electrons in the heterostructures occurs due to the fluctuations from perfectly periodic dipole in highly polar semiconductors. Further, the high dislocation density of 10^8 cm^{-2} in AlGa_N/Ga_N 2DEGs leads to an additional scattering mechanism [3.81]. However, mobilities of $51700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 13 K are reached for carrier densities $\geq 2 \times 10^{12} \text{ cm}^{-2}$. The effect is different from the 3D-bulk impact of dislocations, as described in [3.120]. The drift mobility in heterostructure is further investigated, e.g., in [3.200]. The distinction of the carrier mobility between peak and the drift mobility in AlGa_N/Ga_N heterostructures is made in [3.200]. Peak values of the mobility of $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for low carrier densities of $0.4 \times 10^{13} \text{ cm}^{-2}$ are found on s.i. SiC substrates, while the actual drift mobility at high carrier densities of $1 \times 10^{13} \text{ cm}^{-2}$ amounts to $1,400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature. The peak mobility for layers on sapphire for comparable nominal barrier structures is only $1,300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature.

MOCVD-Grown Heterostructures

Nearly all electronic high-performance Ga_N FET and bipolar devices contain heterostructures of some kind. Thus, the specific growth of heterostructures and results are addressed in this section.

Heterostructure Transport in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$

Fig. 3.4 depicts the extracted heterostructure Hall mobility data taken from a more statistical point of view from various publications, e.g., [3.13, 3.39, 3.102, 3.139]. The data on the AlGa_N/Ga_N heterostructures are given for various substrates, including the channel resistivity contours. The Hall mobility values in general range between 500 and $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ depending on the substrate and material quality and some specific growth measures. The transport situation in heterostructures differs from a bulk approach, so that additional mechanisms influence the mobility, as is already discussed in chapter 2 and also further described in [3.82]:

- Alloy scattering mechanisms, especially at high sheet carrier densities
- Interface roughness
- Scattering for remote surface donors
- Scattering due to threading dislocations

Typical sheet resistances of $130\text{--}500 \Omega \text{ sq}^{-1}$ can be found for various compositions, as shown in Fig. 3.4. Numerous publications are available for the

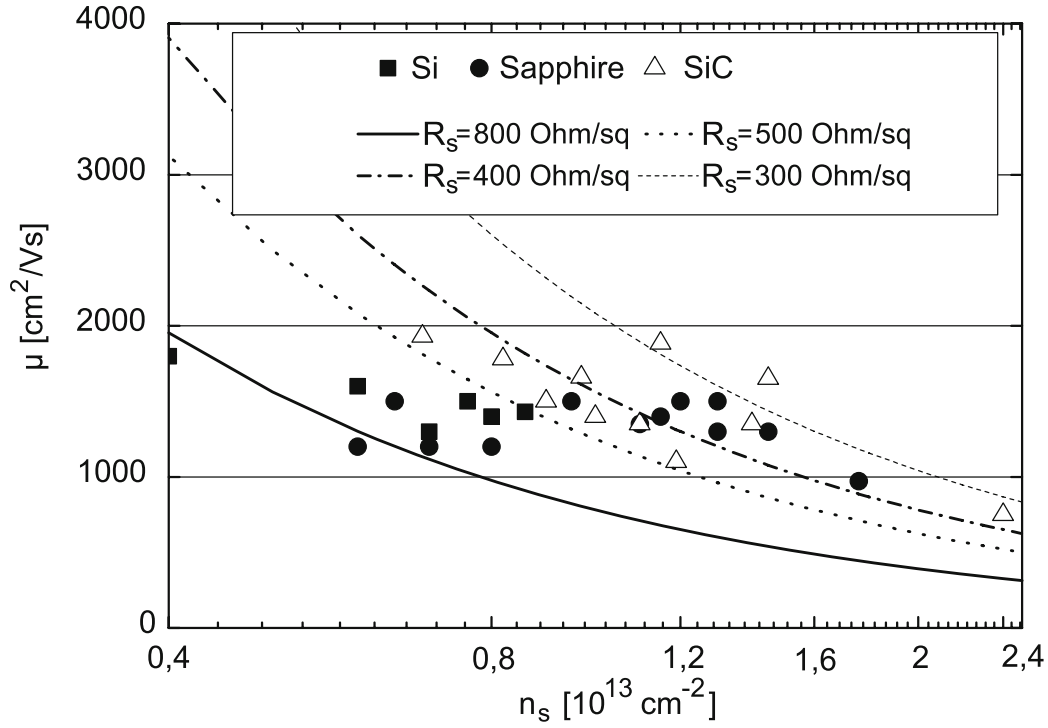


Fig. 3.4. Hall mobility as a function of sheet carrier concentration for AlGaIn/GaN heterostructures grown on various substrates in MOCVD material

Al-content range between 10 and 35% [3.13, 3.39, 3.102, 3.139]. Even higher Al-contents ($x \geq 0.35$) in AlGaIn/GaN MODFETs with Al-contents up to 52% are reported in [3.92, 3.136, 3.222]. The detailed influence of the MOCVD growth parameters will now be discussed.

Material Composition Dependence

The material dependence of the properties of the ternary materials is of great importance and determines several device parameters critically, as is already shown with the sheet resistance. Fig. 3.5 gives the Hall mobility data as a function of Al-content in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier in MOCVD-grown heterostructures for completely undoped structures with a constant barrier thickness. The mobility is only weak function of the sheet carrier concentration up to a concentration of approximately $1 \times 10^{13} \text{ cm}^{-2}$. Beyond that value, the Hall mobility decreases with increasing carrier concentration. Fig. 3.6 gives the Hall mobility as a function of carrier concentration in AlGaIn/GaN heterostructures on sapphire for a given Al-mole fraction and barrier thickness with the Si δ -doping varied. The values for the sheet carrier concentration range from $4.5 \times 10^{12} \text{ cm}^{-2}$ to about $1.2 \times 10^{13} \text{ cm}^{-2}$. The impact of doping of the $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier can be observed in Fig. 3.6 for a given experiment at otherwise constant growth parameters. We see that the Si δ -doping in the barrier in the range 10^{17} cm^{-3} (nid) to $3 \times 10^{19} \text{ cm}^{-3}$ has a significant impact on the sheet carrier concentration, and that the doping has also a strong impact on

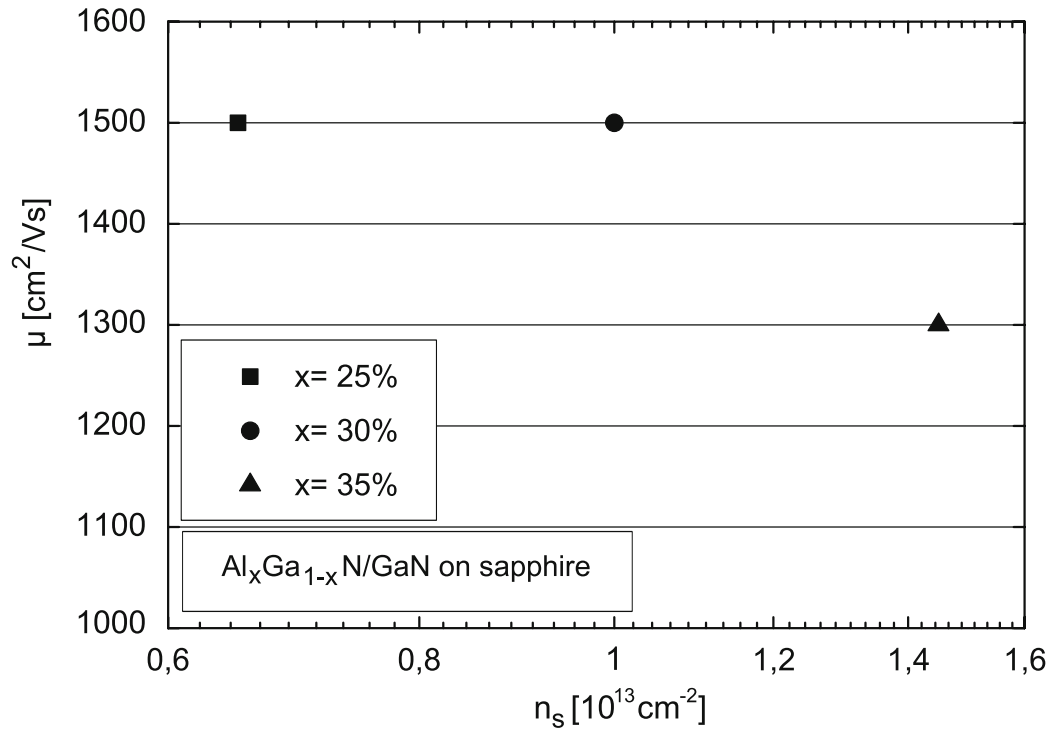


Fig. 3.5. Hall mobility as a function of sheet carrier concentration with the Al-content as a parameter in undoped MOCVD heterostructures on sapphire substrate

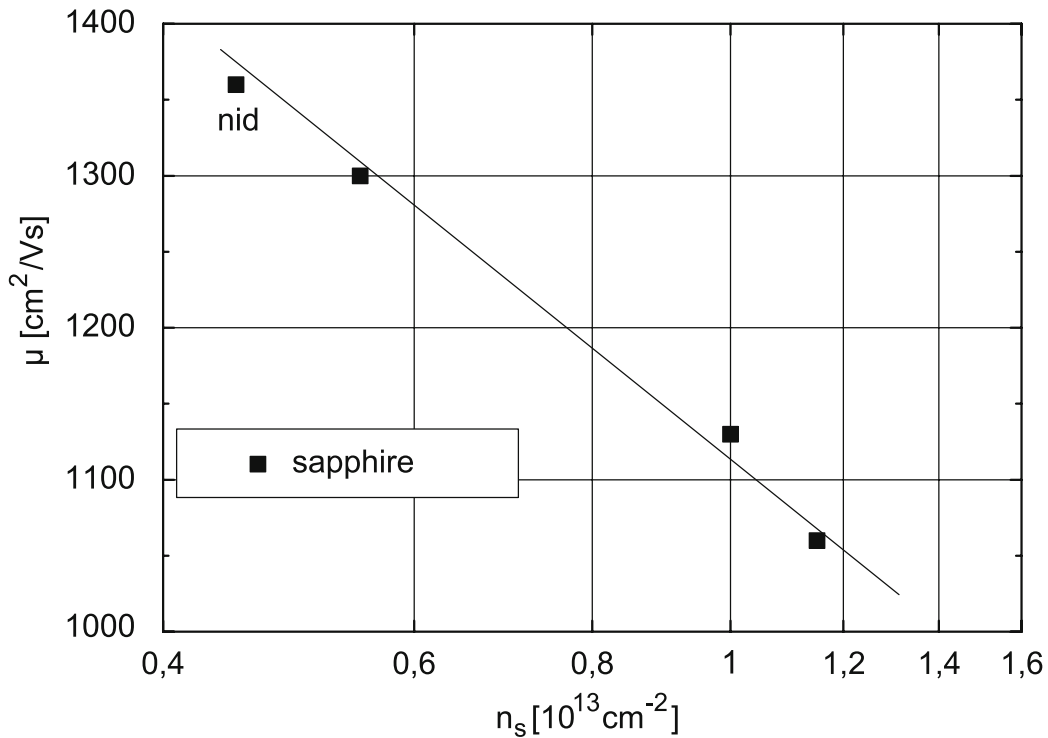


Fig. 3.6. Hall mobility as a function of sheet carrier concentration for different doping levels in the barrier for MOCVD material on sapphire and SiC substrates

the carrier mobility. Very similar data is found for growth on s.i. SiC in [3.48]. Additional effects arise from the introduction of AlN interlayers [3.139], as described further below. Depending on the growth parameters, sheet carrier densities of $2 \times 10^{13} \text{ cm}^{-2}$ can be reached [3.25, 3.92].

Uniformity

Epitaxial uniformity is a basic requirement for the reproducible device and MMIC production. The uniformity is currently given for 2-in. to 4-in. wafer sizes, e.g., [3.192]. For the average standard deviation of the sheet resistance, typically a value $\leq 1\%$ is specified for both 2-in. and 3-in. wafers on MOCVD material grown on sapphire and s.i. SiC substrates [3.192]. Fig. 3.7 shows the homogeneity of the sheet resistance within a multi-wafer growth reactor chamber for 2-in. s.i. SiC wafers, which achieves a standard deviation of 1%. The improvement in uniformity due to the transition from 2-in. to 3-in. s.i. SiC wafers is, e.g., investigated in [3.221]. The run-to-run reproducibility is significantly improved for the 3-in. growth, which is a prerequisite for reproducible device production. In a direct comparison, average standard deviations $\leq 3\%$ on 3-in. MBE-grown and MOCVD-grown material are reported in [3.221]. The substrate quality impact on the uniformity is strong, especially for SiC substrates with still evolving quality. Some general findings shall be listed here: With the increasing substrate diameter, improved substrate-related unifor-

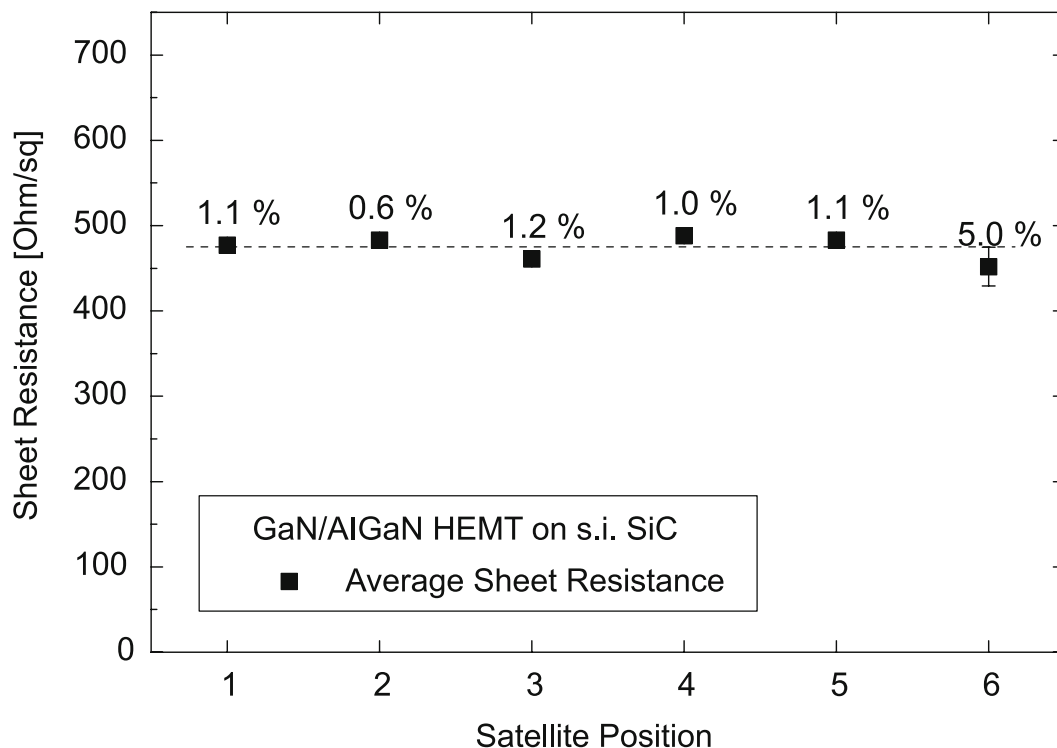


Fig. 3.7. Homogeneity of sheet resistance in MOCVD material within a $6 \times 2''$ reactor

mity and a wafer-to-wafer uniformity of AlGa_N/Ga_N HEMT epitaxial wafers on sapphire and s.i. SiC substrates are reported [3.193]. The typical standard deviation of the sheet resistance is 2% on 4-in. sapphire substrates. Very reproducible AlGa_N/Ga_N HEMTs are grown on n-type SiC with very low standard deviations of $\leq 1\%$ of the device parameters [3.96]. Typically, the substrate quality improves with the increase of the substrate diameter. This scaling benefit is similar to the findings of silicon technology and related substrate scaling. The contribution of the homogeneity of the material composition is investigated, e.g., in [3.161]. The material composition $x = 0.12$ of Al_{*x*}Ga_{1-*x*}N directly grown on s.i. SiC varied by $x \pm 0.005$ due to terrace steps on the growth surface.

Fig. 3.8 gives a topogram to demonstrate the on-wafer homogeneity of the sheet resistance on a 3-in. wafer. The homogeneity is very much influenced by the substrate quality, which is also visible in Fig. 3.8. The largest deviations of the sheet resistance can be correlated with substrate nonuniformities in the upper left edge shown in Fig. 3.8, resulting from substrate growth. Further particular growth issues to increase uniformity include the following:

- The uniform distribution of the defects such as micropipes and others in the substrates
- The uniformity of the temperature and of other growth parameters over the wafer
- The growth windows with respect to relative requirements and to relative deviations
- Such as the uniformity of the thermal contact of the substrate during growth

These issues are related to the particular reactor concepts, such as the wafer rotation during growth. These issues are now discussed in the following sections.

Material Analysis

Several state-of-the-art methods are used for the characterization of the III-N heterostructures. These advanced methods are necessary to optimize this complicated material system with regard to the great variety of effects. Atomic force microscopy (AFM) typically reveals surface roughness. The measurements are performed for areas with some 10 μm dimension, e.g., [3.204]. An example of an AFM image is given in Fig. 3.9 for the growth of Ga_N surface on sapphire substrate. A RMS roughness of 0.4 nm is observed. Structural topography by X-ray diffraction (XRD) and two-dimensional XRD maps reveal structural properties such as micropipes, dislocations, and grain boundaries of substrates and overgrown semiconductor layers [3.100]. The line widths in XRD measurements further allow the investigation of the lattice-mismatch and the Al-content in the barrier layer, as explained, e.g., in [3.204].

Photo-luminescence measurements at various temperatures reveal possible trap mechanisms, e.g., as stated in [3.219], between 2.25 and 3.0 eV. Fig. 3.10

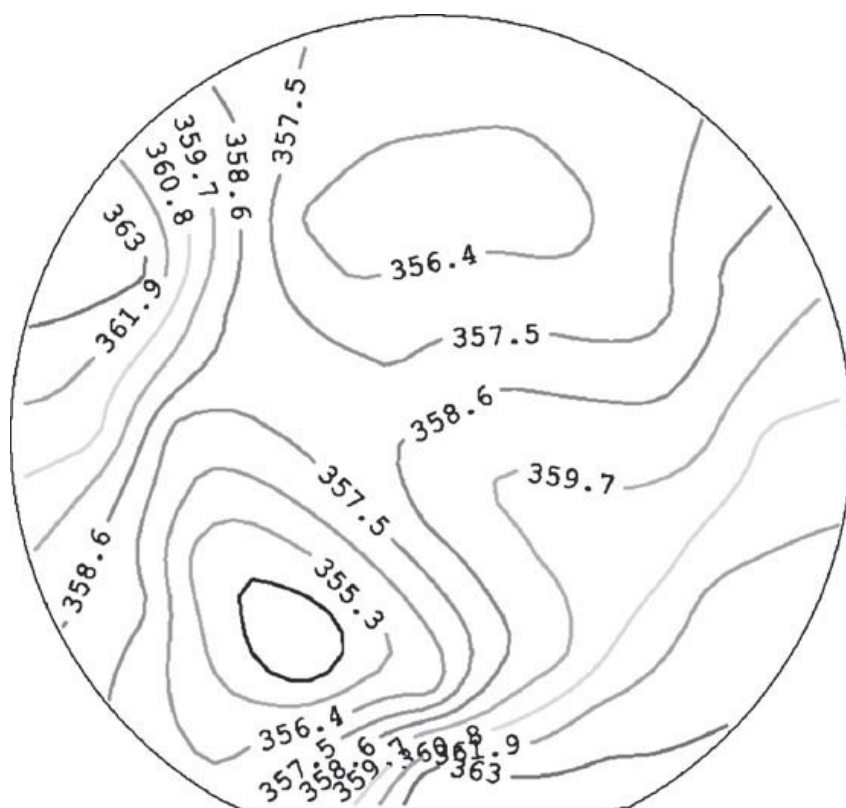


Fig. 3.8. On-wafer homogeneity of sheet-resistance of an AlGaIn/GaN MOCVD-grown heterostructure on 3-in. s.i. SiC substrate, average $359 \Omega \text{sq}^{-1} \pm 0.7\%$

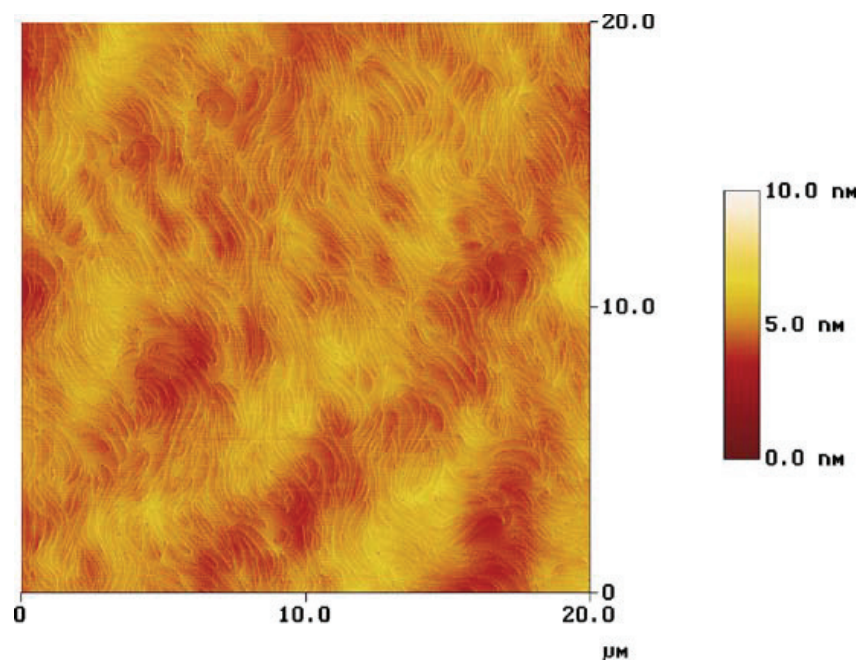


Fig. 3.9. Atomic force microscope image of a surface of a GaN layer MOCVD-grown on sapphire substrate

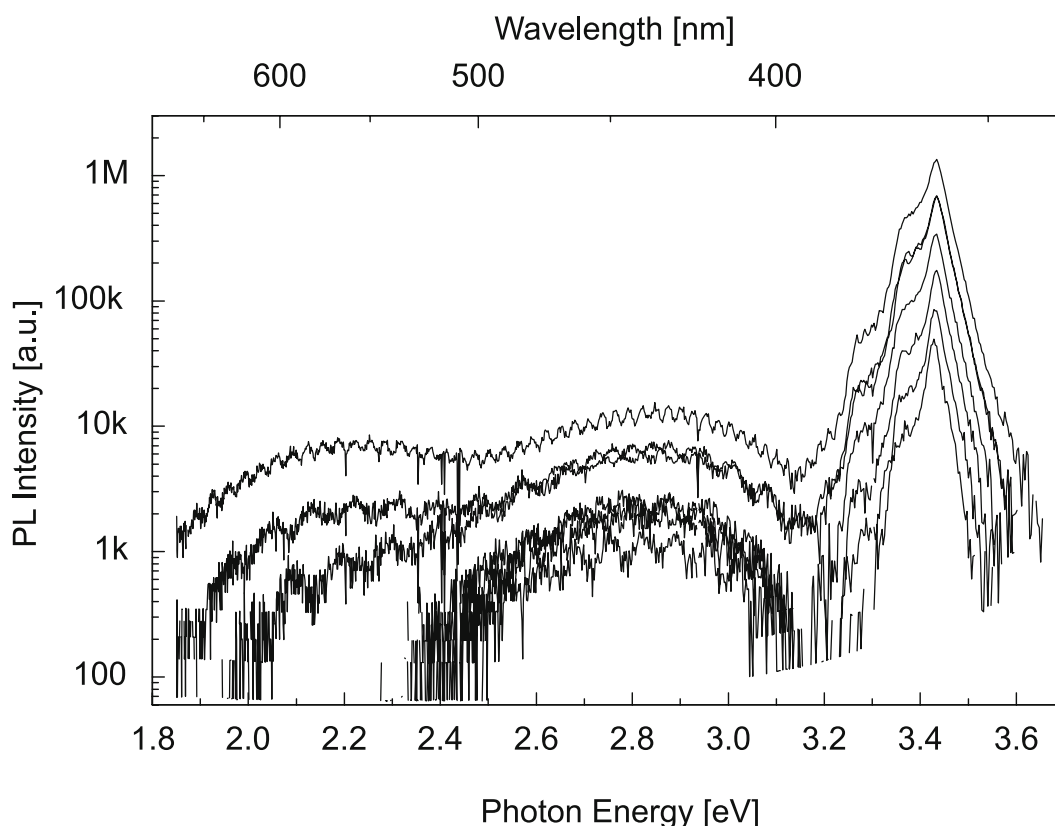


Fig. 3.10. Photoluminescence spectra of AlGa_N/Ga_N heterostructures for different excitation energies

gives a spectrum of an AlGa_N/Ga_N HEMT structure on s.i. SiC. There is yellow luminescence visible at a photon energy of ≈ 2.8 eV. The significance of this data is based on the electron recombination in high-resistivity films, potentially with edge-type threading dislocations [3.219] leading to high resistivity. An alternative explanation is the removal of a particular trap with changes of growth parameters.

MOCVD Growth on s.i. SiC(0001) Substrate

SiC(0001) requires the matching of the Ga_N layers to the 4H- or 6H-s.i. substrate. Direct growth of Ga_N on (0001) 6H-SiC leads to columnar grain with rough, faceted surfaces and high non-intentional net carrier concentrations [3.59]. Typical nucleation layers for growth on SiC are high-temperature Al_N layers [3.215, 3.222]. Further details are given below. An example of multi-wafer epitaxy of AlGa_N/Ga_N heterostructures on s.i. silicon carbide for power applications is given in [3.102]. Fig. 3.11 shows the sheet carrier concentration in Al_xGa_{1-x}N/Ga_N heterostructures as a function of Al-content on s.i. substrate for a mole fraction between 0 and 40%. A very linear dependence is visible for these samples from $x = 0.13$ to 0.35. As the Al-content defines the sheet carrier concentration at the interface, Fig. 3.12 gives the homogeneity of

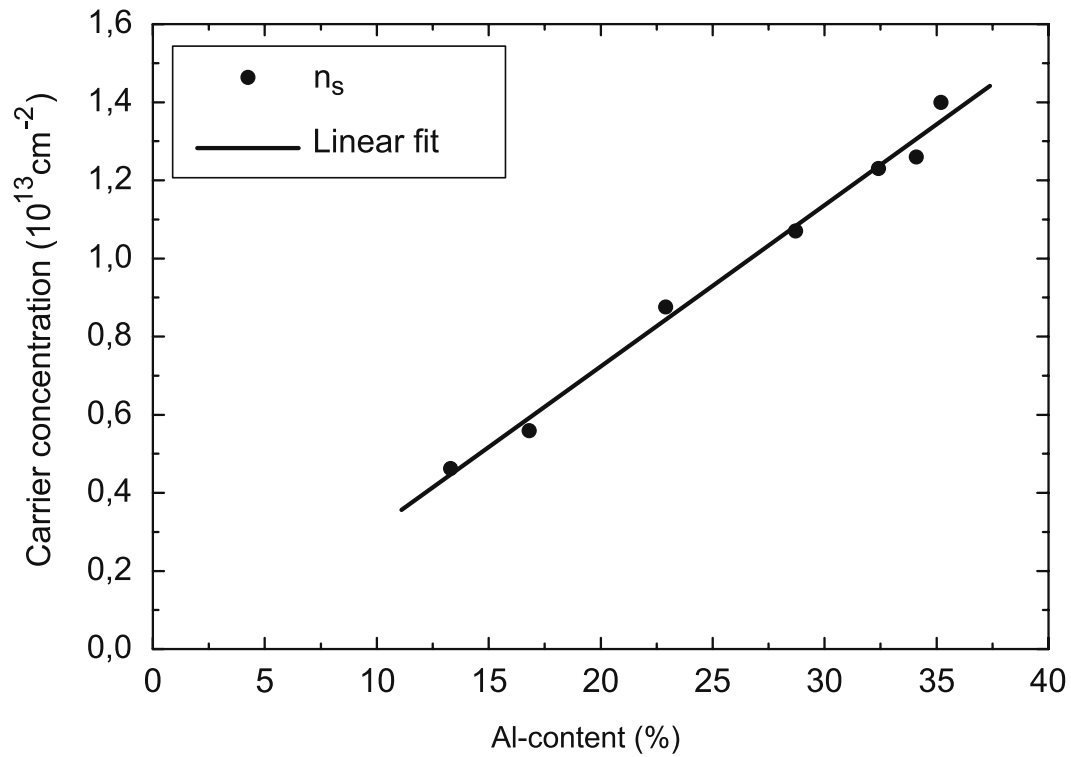


Fig. 3.11. Sheet carrier concentration as a function of Al-content for MOCVD-grown $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures on s.i. SiC substrate

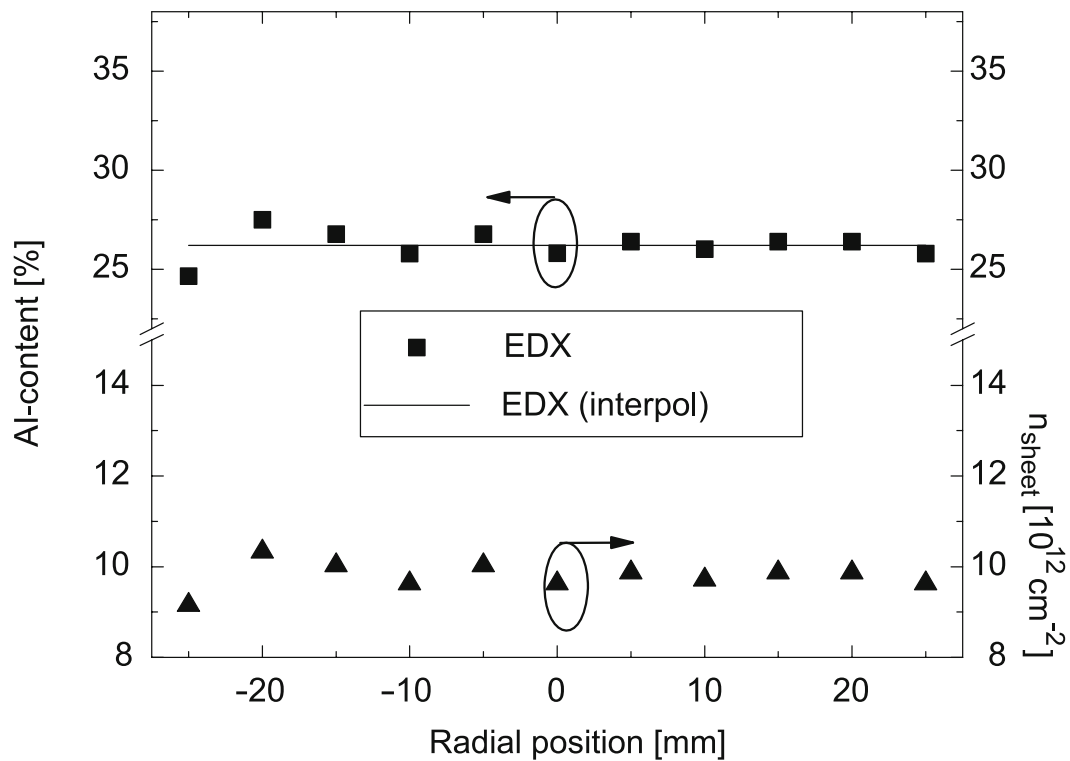


Fig. 3.12. Al-content and corresponding variation of the sheet carrier concentration as a function of radial position for a 2-in. s.i. SiC wafer

the Al-content determined by electron diffraction (EDX) and at the same time provides the calculated difference of the carrier concentration. Even a very small variation of $x \leq 0.2\%$ provides a significant variation in the sheet carrier concentration of $\approx 1 \times 10^{12} \text{ cm}^{-2}$ over the 2-in. diameter. The n_{sheet} is calculated from the $n_{\text{sheet}}(x)$ extrapolated relation in Fig. 3.11.

MOCVD Growth on Sapphire(0001) Substrate

One of the crucial advantages of sapphire relative to SiC is the lack of micropipes and the commercial availability of larger substrate formats up to at least 6 in., as used for CMOS on sapphire with a different crystal orientation [3.95]. MOCVD growth on 4-in. sapphire substrates is reported in [3.7, 3.96]. MOCVD growth issues on sapphire substrates are the increased lattice-mismatch and the difference in thermal expansion between sapphire and Ga_N. The latter results in increased wafer bow [3.96] when the wafer is cooled to room temperature after growth. As an example, the wafer bowing can be reduced to 22 μm on top of 630 μm thick Ga_N buffer, as reported in [3.193]. Epiready 2–4 in. sapphire substrates have been used in [3.192]. The standard deviation of the sheet resistance is $\leq 1\%$ for all diameters. The Al-composition varies by 0.2% over the 3 in. wafer. The AlGa_N thickness varies by $29.25 \pm 0.75 \text{ nm}$. Fig. 3.9 depicts the AFM image of a Ga_N surface on sapphire substrate. The surface root mean square (RMS) roughness on sapphire amounts to only 0.4 nm for an area of $20 \times 20 \mu\text{m}^2$. The peak-to-peak roughness can be as high as 15 nm, which has several implications for the scaling of the devices to small gate lengths.

MOCVD Growth on Silicon(111) Substrate

Growth on silicon substrates is very attractive as a cost effective method and also relates the III-N material system to the most successful semiconductor system. First demonstrations of MOCVD-grown AlGa_N/Ga_N HEMTs on silicon substrate have been claimed, e.g., in [3.29]. The results are obtained on p-type Si(111) substrates with a buffer layer of 500 nm thickness on top of a 30 nm Al_N nucleation layer. An overview of the MOCVD growth on silicon substrate is given in [3.34]. The silicon material can either be conductive or highly resistive (30 k Ω cm). Highly resistive silicon is more expensive than conductive substrates and available only in smaller diameters. However, highly resistive silicon is advantageous to reduce the substrate RF-losses, especially at frequencies higher than 2 GHz [3.42]. Buffer growth is of great importance due to the increased lattice-mismatch between silicon and the III-N material system. A critical thickness of the buffer growth of 1 μm is mentioned in [3.34]. Furthermore, the difference in thermal expansion is pronounced, as explained in Table 2.5. Mismatch engineering is thus of critical importance. Patterned substrate techniques are described, e.g., in [3.85]. AlGa_N/Ga_N HEMTs are fabricated on top of rectangular silicon ridges. The rectangular stripes have

a maximum size of $168 \times 52 \mu\text{m}^2$, which limits the application of this techniques to small devices. The stress distribution in patterned GaN films grown by MOCVD on (111) silicon is investigated in [3.208]. The intentional cracking of the layers grown reduces the tensile strain in small area stripes. Low-temperature (LT) AlN-interlayers are used for strain engineering [3.34]. The LT-AlN layers are combined with high-temperature layer stacks. These methods can be used to reduce the threading dislocation density in the heterostructure layers [3.37]. Crack-free GaN material is reported in [3.79] on 2-in. p-type silicon grown by MOCVD. The buffer thickness is $2.5 \mu\text{m}$, which further reduces the dislocation density on top of specially designed layer sequences used for nucleation. The RMS surface roughness reported amounts to 0.64 nm determined by AFM. A commercial GaN HFET process on 100 mm diameter silicon substrates is given in [3.204], using GaN epitaxial layers up to $2 \mu\text{m}$ thickness in the SiGaN_{tic}TM process. The standard deviation of the Al_{0.21}Ga_{0.79}N spectral-peak wavelength at 324 nm across a 100 mm wafer is as low as 0.6%. The Hall mobilities reach $1,430\text{--}1,500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at a sheet charge carrier concentration of $\approx 8 \times 10^{12} \text{ cm}^{-2}$. The difference in thermal expansion and lattice-mismatch have particular impact on the device reliability, which is further discussed in Chapter 7.

3.1.2 Molecular Beam Epitaxy (MBE)

MBE is the second attractive growth method for III-N semiconductors. The growth of semiconductors by MBE occurs via reactions between thermal-energy molecular, atomic, or ionized beams of the constituent elements on a heated substrate in an ultrahigh vacuum; see, e.g., in [3.36]. The advantage of MBE is a very precise definition of the interfaces and the increased flexibility of the polarity of the interfaces [3.87, 3.196]. These advantages are available at the expense of reduced growth rates relative to MOCVD growth. The growth rates of III-N MBE typically amount to $0.5\text{--}1 \mu\text{m h}^{-1}$ [3.132]. Fig. 3.13 gives the schematic of a MBE growth chamber. The molecular beam of Ga and Al originate from effusion cell sources. An elemental group-V N-source is impossible due to the very high binding energy of the N₂. N radicals are thus generated either by a RF-plasma source [3.17, 3.132, 3.166] or by an ammonia source, as reported, e.g., in [3.194, 3.213]. The background pressure amounts to $\leq 10^{-11} \text{ mbar}$ during MBE growth, as given, e.g., in [3.89]. The substrates are typically rotated during growth. Growth temperatures amount to 800°C for GaN growth. Growth conditions of MBE can be characterized by growth diagrams, given for III-V semiconductors, e.g., in [3.36, 3.88, 3.149].

State-of-the-Art of MBE Growth

Overviews on molecular beam epitaxial growth of III-N materials are given, e.g., in [3.50, 3.87, 3.172]. More general overviews of growth and doping of III-V nitrides including MBE growth are given in [3.39, 3.150]. AlN is typically used

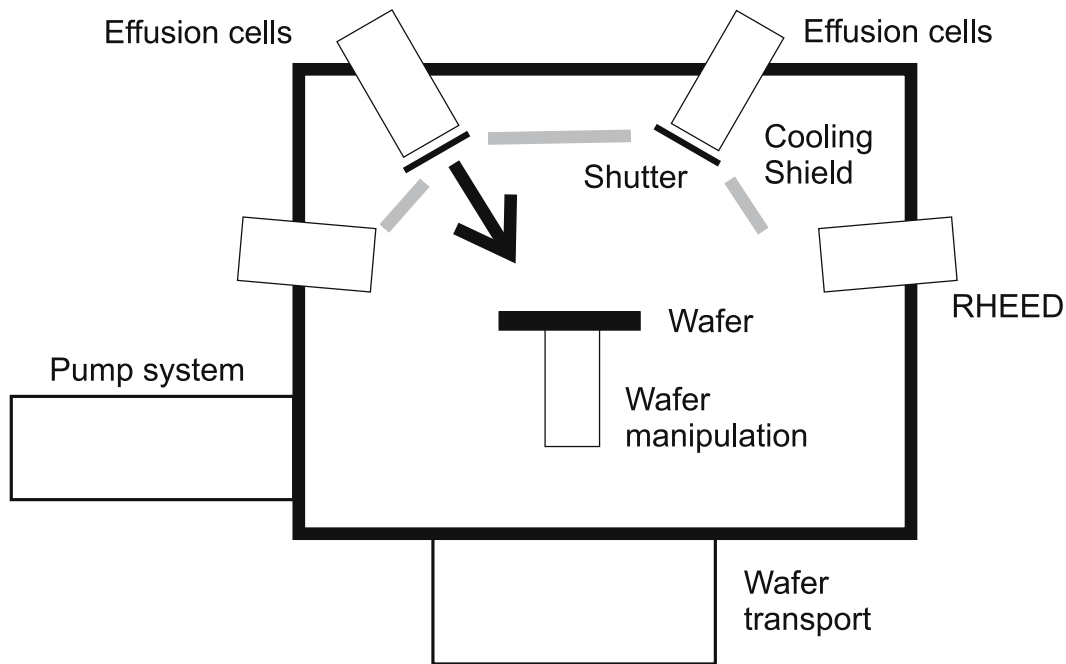


Fig. 3.13. Scheme of molecular beam epitaxial (MBE) growth

as a nucleation layer for MBE [3.90,3.132,3.216]. Issues in scaling nitride MBE systems to 4-in. single-wafer production are discussed in [3.188]. The scaling of the RF-plasma system is investigated, especially with respect to the small growth window in the Ga/N flux ratio. The second issue in wafer-size scaling is the growth temperature uniformity for increased wafer size. Compared to other III/V-MBE systems, the temperature control is more complicated due to the high growth temperatures of III-N materials, leading to high radiative losses. Further, the optical transparency of the substrates, such as SiC and sapphire, in the infrared complicates heat absorption. MBE-growth conditions are investigated in a number of publications, e.g., in [3.17, 3.41, 3.66, 3.67, 3.113, 3.165, 3.205, 3.213], and are detailed below. On the device level, high-power GaN/AlGa_N HEMTs grown by plasma-assisted MBE operating up to 25 GHz are described in [3.124, 3.125, 3.132, 3.216]. An X-band power amplifier is given featuring a cw-output power of 22.9 W using four hybrid 1 mm cells. The amplifier yields a PAE of 37%. Further impressive device examples and a comparison of HEMTs grown either by plasma-assisted MBE or MOCVD are given in [3.39, 3.166]. Device examples of ammonia-based Ga_N MBE are given in [3.10]. AlGa_N/Ga_N HEMTs with gate lengths of 130 nm feature very high drain current densities $\geq 1.3 \text{ A mm}^{-1}$ and a cut-off frequency $f_T = 103 \text{ GHz}$.

Optimized Growth Conditions for MBE Growth

Similarly, as in MOCVD growth, optimized growth conditions for MBE are very system- or machine-specific. However, general trends will be outlined here.

Growth Temperatures for III-N MBE Growth

Before the actual growth procedure, the substrates are typically inserted into the growth chamber via a preparation chamber. The substrates are outgassed in the preparation chamber. A typical substrate outgas temperature in the preparation chamber is reported to be 700°C in [3.90]. Further temperature steps for oxide removal reach 1,000°C. The reported nucleation temperature using AlN nucleation on sapphire substrate is 800°C, as reported in [3.150]. A nucleation temperature of 835°C on s.i. 6H-SiC substrates is used in [3.90]. The growth of the insulating GaN buffer layer on top of a nucleation layer is reported to be performed at 745°C in [3.90, 3.125] for Ga-rich conditions. The GaN channel layers are typically grown at 800°C using atomic nitrogen, as reported in [3.40]. The backside of the substrate is metalized by tungsten in this case. Thick bulk GaN layers are grown by plasma-assisted MBE between 600 and 800°C for different Ga/N flux ratios on SiC(0001), as reported in [3.205]. The threading dislocation density can be reduced from 10^{11} cm^{-2} for a growth temperature of 600°C and Ga-lean growth to 10^{10} cm^{-2} for a growth temperature of 800°C and Ga-rich growth. The nominal growth temperatures for GaN using ammonia-based MBE growth is 910–920°C and 880°C for AlN [3.10, 3.212]. A growth temperature for a bulk GaN layer of 860°C is reported in [3.194] for ammonia-based MBE on sapphire(0001). Magnetron sputter epitaxy is used in this case for the initial deposition of a AlN nucleation layer. The growth of quaternary $\text{Al}_x\text{Ga}_{1-x-y}\text{In}_y\text{N}$ materials by plasma-assisted MBE on GaN templates is described in [3.137]. Substrate growth temperatures range from 590 to 650°C. The use of the MBE technique increases the material composition range, which is ($0 \leq x \leq 0.5$, $0 \leq y \leq 0.2$) in this case.

N-Group-III Ratio for MBE Growth

Similar to MOCVD growth, the V/III ratio is a critical parameter for the MBE growth, however, for a very different material transport. A distinction is made for RF-plasma-assisted MBE (PAMBE) and ammonia-based MBE. The V/III-ratio determines the quality of the epitaxial layers. The impact of the Ga/N flux ratio on trap concentrations and morphology in GaN grown by plasma-assisted MBE is discussed in [3.67, 3.68]. The distinction of the Ga-rich, intermediate, and N-stable regime is made. N-stable-grown GaN films are semi-insulating. GaN layers grown with ratios in the intermediate regime yield fewer pits with an atomically flat surfaces. At high Ga/N-ratio Ga droplet formation occurs. However, the mobility decreases significantly. The best material is thus grown within the intermediate regime. The best combination of

surface morphology and material quality is achieved by a modulated technique varying alternately Ga-rich and Ga-lean growth, see, e.g., [3.33, 3.117]. The growth diagram for GaN, grown homoepitaxially by plasma-assisted MBE, is given in [3.67] for a growth temperature of 720°C. The surface morphology and GaN mobility are optimized for the various Ga-flux conditions. Similar surface structure diagrams between 550 and 700 K are given in [3.66].

The growth conditions such as V/III ratio and temperature for AlGaIn are investigated for plasma-assisted MBE in [3.41]. The $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ layers are grown at temperatures between 650 and 750°C. Particularly, the O_2 incorporation is investigated. It is found that the incorporation is minimized for the higher growth temperatures.

For ammonia-MBE, carbon-doped insulating GaN MBE layers are grown on s.i. SiC substrates at a temperature of 910°C [3.211, 3.212, 3.214]. For the AlN nucleation in [3.194], argon and ammonia fluxes are adjusted leading to growth rates of $3.4 \text{ nm min}^{-1} \equiv 204 \text{ nm/h}$ at a very high deposition pressure of 1.4 mTorr. GaN-layer deposition pressures of 3×10^{-6} Torr are reached during the growth. The growth rates reach $1\text{--}2 \mu\text{m h}^{-1}$ by the adjustment of the ammonia flow to 50 sccm.

Nucleation Layer Growth by MBE

The nucleation layer is of very high importance on various substrates, as this region with its polycrystalline inclusions contributes significantly to the quality of the MBE-grown active semiconductor layers and thus to device performance. The growth of an AlN nucleation layer by plasma-assisted MBE on s.i. 4H-SiC substrate is reported in [3.89]. The layer thickness is 100 nm, grown at a temperature of 835°C. The N_2 pressure is 2×10^{-5} Torr for the nucleation layer. A 60 nm thick AlN nucleation layer is used in [3.124] grown by PAMBE on s.i. SiC substrate under Al-rich growth conditions at 745°C. Similar thicknesses and conditions are reported in [3.125]. Hundred nanometer thick AlN nucleation layers are grown by RF-PAMBE at 835°C [3.90]. An AlN nucleation layer on sapphire with a thickness of 70 Å is used in [3.39] for RF-plasma-assisted MBE on sapphire substrate. Al-rich surfaces to obtain Ga-polarity are used. The GaN growth rate is $0.5 \mu\text{m h}^{-1}$ at a growth temperature of 800°C. On silicon substrate, a 50–60 nm thick AlN nucleation layer is used, grown by reactive MBE in combination with a 500 nm special layer sequence and a $1.5 \mu\text{m}$ thick GaN buffer [3.135]. The TDD amounts to $7\text{--}9 \times 10^9 \text{ cm}^{-2}$.

Growth and Isolation of the Buffer Grown by MBE

A large variety of buffer layers grown by MBE are reported for heteroepitaxy. The growth rate of GaN achieved by MBE in general is smaller than in MOCVD growth, e.g. $0.5 \mu\text{m}$ in [3.132]. This lower growth rate favors reduced layer thicknesses for MBE growth, especially for the buffer layer.

As an example for a optimized buffer sequence, after the growth of a 45 nm thick AlN nucleation layer on 4H-s.i. SiC, a 400 nm thick GaN two-layer sequence is used in [3.162, 3.166, 3.206] to improve the isolation, grown

with a flux variation stepping from a low Ga-flux regime to a high Ga-flux regime. Further, the AlN and the first 100 nm are C-doped with CBr_4 . This sequence is followed by a 1 μm thick undoped GaN buffer/channel-layer. Two micrometer GaN thick buffer layers grown by PAMBE on s.i. 4H-SiC substrate are reported in [3.132]. The growth rate is $0.5 \mu\text{m h}^{-1}$.

Grown by ammonia-MBE on s.i. 4H-SiC substrate, a 2 μm thick highly insulating C-doped GaN buffer layer is reported in [3.213]. The layer is followed by a 200 nm undoped GaN channel layer grown at a nominal temperature of 920°C . Beryllium-doped GaN buffer layers grown by RF-plasma-assisted MBE on n-type 6H-SiC are reported in [3.90]. The leakage through a 1 μm thick buffer is reduced by the Be-doping at concentrations between 10^{18} and 10^{19} cm^{-3} . Even the lowest doping concentration leads to significant reduction of the leakage by three orders of magnitude.

On high-resistivity silicon substrate, a 1.5 μm -thick GaN buffer is reported in [3.135], grown by MBE on a 50 nm-thick AlN nucleation layer. Crack-free GaN bulk buffer layers with thicknesses up to 3 μm grown on silicon substrate are reported in [3.180]. Ammonia is used as a nitrogen source for the MBE. Buffer layers with thicknesses between 1 and 2.5 μm are investigated for AlGaIn/GaN heterostructures. Hall mobility values up to $1,600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are achieved at room temperatures. The TDD range between 5×10^9 and 10^{10} cm^{-2} .

The interface the substrate is especially susceptible to isolation issues due to the high concentration of defects. Indications for conduction parallel to the GaN/sapphire interface in PAMBE-grown material are investigated in [3.3]. The buffer material is etched to different thicknesses. The results show that the apparent carrier concentration increases near the interface, while the mobility decreases. Both interface conduction and impurity band conduction near the interface are considered to explain this behavior.

Codoping in MBE Material

Similar to MOCVD-grown material, intentional codoping is of great importance for the isolation of the nucleation and buffer layers. During MBE growth, this codoping is achieved mostly by carbon and (non-intentional) oxygen, as Fe sources are not available. Carbon introduces a midgap state which helps to increase the isolation in buffer layers. Codoping by carbon for MBE-grown GaN buffer material in the buffer is reported, e.g., in [3.162, 3.163, 3.166]. A 45 nm-thick C-doped nucleation layer is grown by PAMBE on s.i. SiC. This layer is followed by a sequence of GaN buffer layers. By adjustments of the CBr_4 pressure linearly from 15 and 5 mTorr, the background C-doping concentration is varied linearly from 1.2×10^{18} , 8×10^{17} , and $4 \times 10^{17} \text{ cm}^{-3}$. A systematic investigation of carbon codoping via CBr_4 in PAMBE-grown material is reported in [3.162]. Doping levels of $2\text{--}6 \times 10^{17} \text{ cm}^{-3}$ significantly reduce the buffer leakage in AlGaIn/GaN single heterostructures on s.i. SiC substrate. Unintentional oxygen incorporation into GaN layers is a major problem in

MBE growth. Several sources such as the background vacuum pressure, the nitrogen source, and the metal source are potential candidates. A systematic investigation is given in [3.41] for AlGa_N layers grown by PAMBE on sapphire substrates. Ga-rich growth of AlGa_N reduces the oxygen incorporation by a factor of three. Temperature reduction from 750 to 650°C significantly increases the oxygen incorporation. The nitrogen source is considered as a main source of oxygen in the MBE growth system, which is operated at a background pressure of 10^{-11} Torr. Intentional oxygen incorporation into Ga_N grown by PAMBE has been investigated in [3.165]. The doping is found to be controllable and reproducible up to doping level of 10^{18} cm^{-3} . Oxygen is an effective donor with low compensation and the incorporation is found to be strongly dependent on the growth polarity. PAMBE-grown Ga_N layers with N-polarity incorporate about 50 times as much oxygen than Ga-face material. Oxygen doping levels of 10^{22} cm^{-3} can be achieved.

Channel and Barrier Layers Grown by MBE

The growth conditions for the Ga_N channel layers is of primary importance for the material quality. Several detailed suggestions are available. Ga_N channel layers are grown by PAMBE at 735°C at a growth rate of $0.37 \mu\text{m h}^{-1}$ in Ga-rich conditions [3.89]. The Al_{0.25}Ga_{0.75}N heterobarrier layers are grown at the same temperature and the same nitrogen flow as Ga_N in this case. The Ga_N channel layers in [3.124] are grown by PAMBE on s.i. 6H-SiC under Ga-rich conditions at 745°C near the border of Ga-droplet formation. The upper half of Al_{0.34}Ga_{0.66}N layers are doped by Si to $1 \times 10^{18} \text{ cm}^{-3}$. Similar growth temperatures for PAMBE on sapphire are used in [3.75, 3.77] with a growth temperature of 730°C for Ga_N, and 760°C for the subsequent AlN/Al_{0.4}Ga_{0.6}N growth. This temperature is significantly lower than the growth temperature for similar AlGa_N layers grown by MOCVD. For ammonia(NH₃)-based MBE growth on s.i. SiC, the Ga_N channel layers are typically grown at higher temperatures, i.e., 920°C, as reported in [3.213]. A similar temperature of 910°C for Ga_N is reported in [3.10, 3.214] on 4H-SiC(0001). A growth temperature of 790°C is mentioned in [3.180] for growth on conducting p-type silicon(111) substrates. The resulting mobility data and sheet carrier densities are detailed below.

Dislocations in MBE Material

The TDD in the MBE-grown layers can be reduced to densities similar to those achieved for MOCVD-grown material. On s.i. SiC substrate, the dislocation density can be reduced to $\leq 10^9 \text{ cm}^{-2}$, as observed by plan-view TEM in [3.17]. Plasma-assisted MBE (PAMBE) is used in this case.

Leakage current mechanisms in Schottky diodes are investigated in [3.133, 3.134] in plasma-assisted MBE material grown on Ga_N templates, which again are grown by MOCVD on sapphire substrates. A leakage mechanism is isolated during the investigation based on threading dislocations. The mechanism has

an exponential temperature dependence, and so either a trap-assisted tunneling or a one-dimensional hopping mechanism is considered for the physical origin. A similar investigation of the impact of different dislocation types such as edge-, screw-, and mixed -type in GaN grown by PAMBE on MOCVD templates on sapphire substrates is given in [3.184]. A combination of scanning Kelvin probe microscopy (SKPM) and conductive atomic force microscopy (C-AFM) is used. Edge- and mixed-type dislocation are found to be negatively charged with limited contribution to the leakage, while pure screw dislocations, on the contrary, provide a conductive leakage path. The TDD obtained for the GaN templates on sapphire is found to be maintained through the subsequent MBE growth and is determined by electron-beam current microscopy (EBIC) to be $8 \times 10^8 \text{ cm}^{-2}$.

On resistive silicon substrate, the threading dislocation density amounts to $5\text{--}7 \times 10^9 \text{ cm}^{-2}$ reported in [3.32, 3.135] for MBE-grown material and observed by TEM. The overall layer thickness is $2.6 \mu\text{m}$. Further investigations of p-type silicon(111) substrate in [3.180] demonstrate an increase of the threading dislocation density of GaN on silicon substrate relative to s.i. SiC or sapphire substrates by a factor of two in the same investigation.

MBE-Grown Heterostructures

The basic properties such as mobility and sheet carrier densities grown by MBE are very similar to those obtained by MOCVD growth. Fig. 3.14 gives the mobility as a function of Al-content in MBE-grown material. Similarly, Fig. 3.15 gives the sheet carrier concentration. The maximum sheet carrier concentrations reach $2 \times 10^{13} \text{ cm}^{-2}$. Similar tendencies for the MBE-grown material are observed as for MOCVD, compare Fig. 3.6.

Fig. 3.16 depicts the mobility as function of sheet carrier concentration for various substrates in MBE-grown material at 300 K. Again, very strong variations are observed for a given Al-content depending on the substrate type and the growth conditions, compare Fig. 3.7. The maximum Hall mobility is close to $2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at RT. The results presented in Fig. 3.16 are now analyzed in detail for the different substrate types.

MBE Growth on s.i. SiC

High-performance heterostructures are achieved using both RF-plasma-source MBE and ammonia MBE [3.132, 3.214, 3.217]. Low-field mobility values of GaN/AlGaN heterostructures on 6H-SiC as high as $75,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ measured at 4.2 K grown by PAMBE have been reported, while the RT mobility values amount to $1,400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [3.216]. An additional ECMP surface polish is reported to be crucial to the reproducibility of the heterostructure device results on the SiC substrate.

Sheet carrier densities of up to $2.1 \times 10^{13} \text{ cm}^{-2}$ have been obtained on s.i. SiC substrates using RF-PAMBE. The associated room temperature mobility is $1,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [3.16]. Very thin barrier AlGaN layers

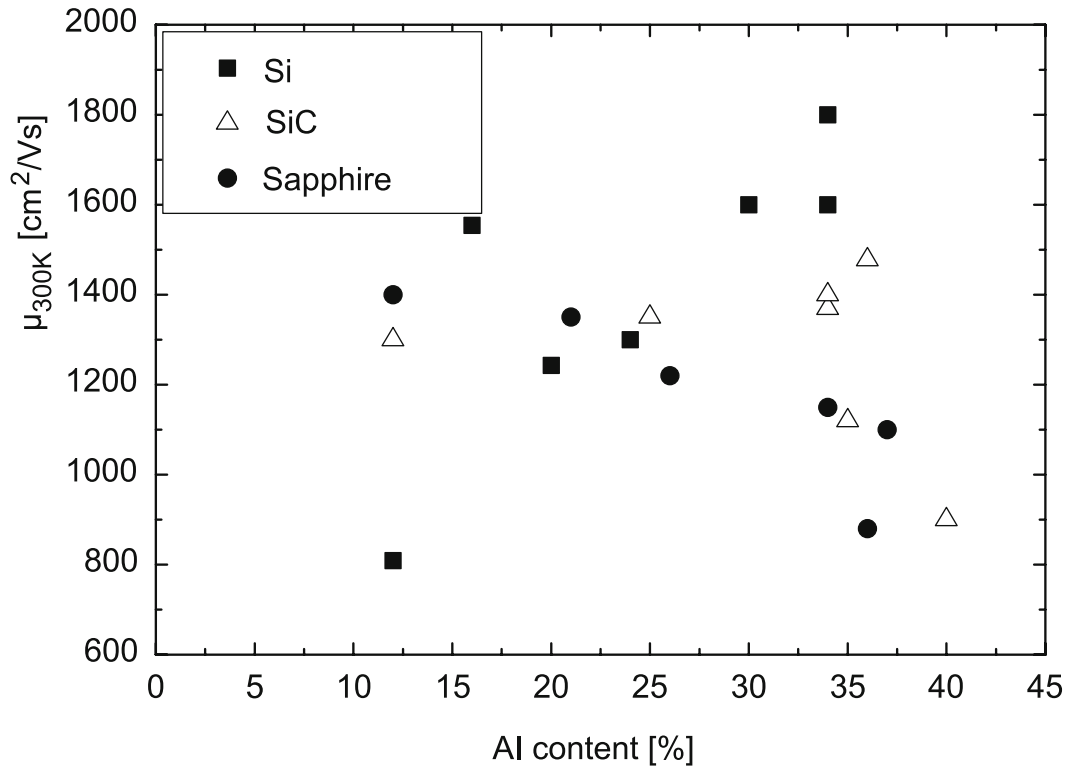


Fig. 3.14. Hall mobility as a function of Al-content in MBE-grown Al_xGa_{1-x}N/GaN heterostructures on various substrates

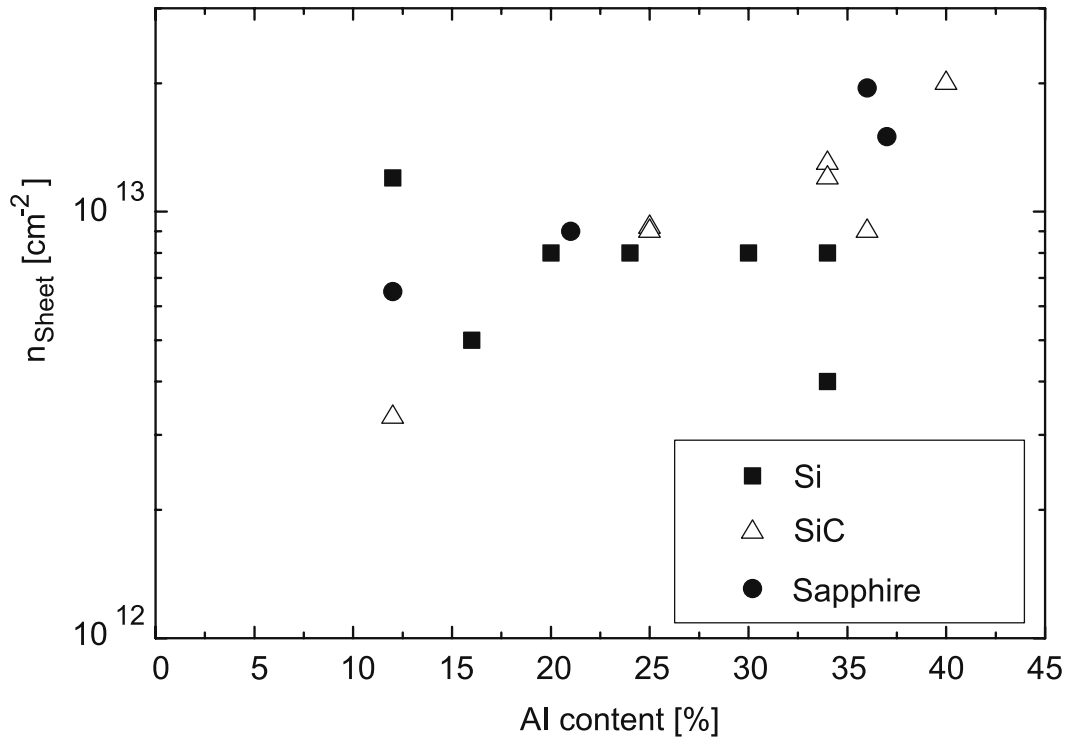


Fig. 3.15. Sheet carrier concentration as a function of Al-content in MBE-grown Al_xGa_{1-x}N/GaN heterostructures on various substrates

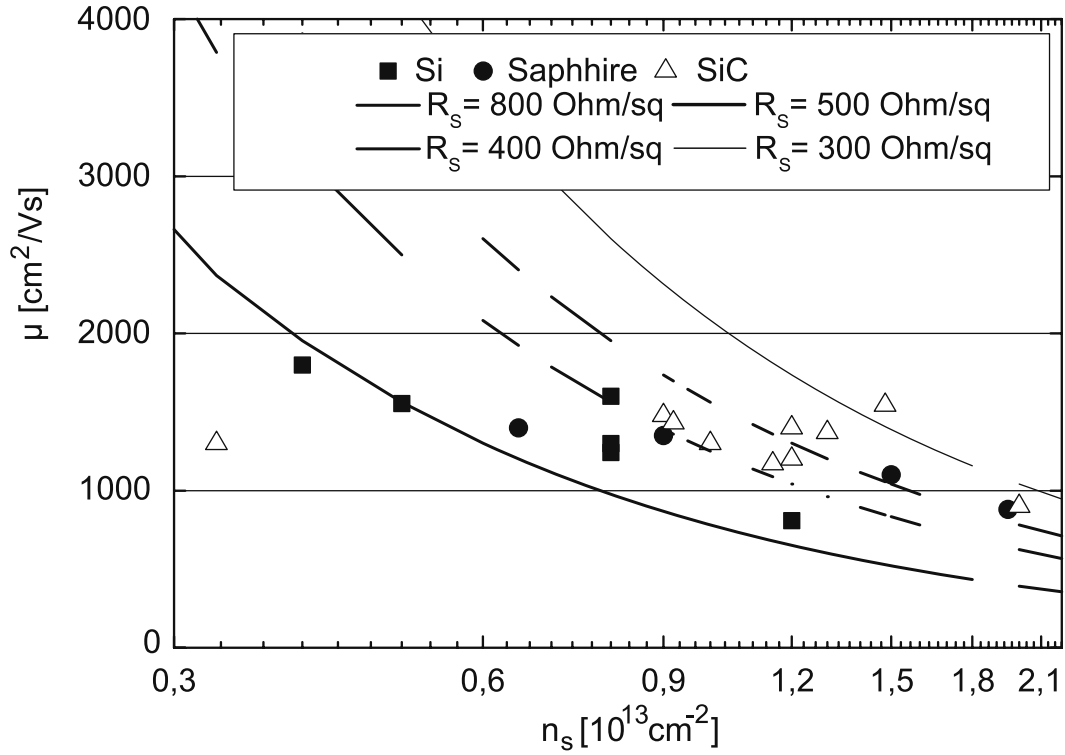


Fig. 3.16. Mobility in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures on various substrates as a function of sheet carrier concentration

of 8 nm thickness lead to reduced sheet carrier densities of $8 \times 10^{12} \text{ cm}^{-2}$ due to the reduced polarization effect [3.75]. Very high cut-off frequencies $\geq 100 \text{ GHz}$ of AlGaIn/GaN HFETs on s.i. SiC substrates grown by ammonia MBE are reported in [3.10]. The AlGaIn/GaN heterostructure mobility is $993 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, while a high sheet carrier density of $1.6 \times 10^{13} \text{ cm}^{-2}$ is measured. Inverted n-face $\text{AlGaIn}/\text{GaN}/\text{AlGaIn}$ HFETs on s.i. SiC substrates show a room-temperature mobility of $860 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The sheet carrier density amounts to $7.8 \times 10^{12} \text{ cm}^{-2}$ [3.26]. The latter result demonstrates the increased flexibility by MBE growth, as inverted polarization with N-face growth can be obtained.

MBE Growth on Sapphire

Most of the initial bulk material investigations and heterostructure results by MBE have been performed on sapphire substrates [3.39] or on GaN-templates grown on c-sapphire by MOCVD, e.g., [3.66–3.68, 3.133, 3.134, 3.137]. RT mobility values of $1,211 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are reported in [3.212] for $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures grown by ammonia-based MBE. The mobility is only a weak function of the Al-mole fraction at RT. The mobility at 77 K amounts to $5,660 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x = 10\%$, while it is $3,200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x = 20\%$, and $2,600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x = 30\%$. Further room temperature results for growth on sapphire are compiled in [3.214]. Using metal organic

sources, III-N MBE can be performed leading to metal organic molecular beam epitaxy (MOMBE) [3.113]. Metal organic species are used for the group-III elements, while the group-N elements are generated by plasma or ammonia.

MBE Growth on Silicon(111)

Several reports exist for the MBE growth on silicon(111) substrate. MBE growth of AlGa_N/Ga_N HEMTs on resistive Si(111) substrates using ammonia MBE are reported in [3.32, 3.179, 3.180]. The range for the resistivity in the substrate amounts to 4–20 k Ω cm for high resistivity [3.135] and 0.002 Ω cm [3.180] for p-doped substrates. The carrier densities reach $8 \times 10^{12} \text{ cm}^{-2}$ with room-temperature mobilities of $1,600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively [3.135]. The TDD is $5\text{--}7 \times 10^9 \text{ cm}^{-3}$. Mobilities of up to $2,100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ on Si(111) have been reported in [3.16] with Al-contents up to 50%. The report further claims no change in the surface morphology for such high Al-contents. The use of silicon substrates with substrate resistivities of 20 k Ω cm leads to very good noise performance using an AlGa_N/Ga_N HEMT structure on silicon with $\geq 2 \mu\text{m}$ thickness. Good mobility values of $1,300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are reported in [3.213] with an associated sheet carrier density of $3.3 \times 10^{12} \text{ cm}^{-2}$ grown by ammonia-based MBE. The mobility at 77 K amounts to $11,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Picogiga reports MBE growth with an ammonia source on high resistivity silicon substrates with up to 4-in. diameter in [3.16]. The typical RMS roughness is 3–5 nm and the TDD is in the range of 10^9 cm^{-2} . The typical isolation of the buffer amounts to $10^6 \Omega \text{ cm}$. Further, pseudomorphic growth of a AlGa_N/Ga_N/AlGa_N double heterostructure is reported to improve the buffer leakage.

3.1.3 MOCVD and MBE Growth on Alternative Substrates

Apart from the direct homo- and heteroepitaxial growth on a crystalline substrate, advanced alternative substrate methodologies have also been developed, e.g., [3.129]. A hybrid technique is used to fabricate AlGa_N/Ga_N HEMTs on diamond substrate [3.84, 3.229]. Al_{0.27}Ga_{0.73}N/Ga_N heterostructures are conventionally grown on 2-in. silicon(111) substrates. The wafers are then mechanically frontside-mounted on a mechanical substrate. The silicon substrate is then removed. A 25 μm thick CVD grown polycrystalline diamond substrate is then atomically bonded to the Ga_N buffer. The procedure potentially combines the very good thermal conductivity of diamond with III-N semiconductor devices, as detailed in [3.229]. Remaining issues include the additional need of another mechanical substrate to enable the processing of the wafers. SiC on insulator (SiC on SOI or SiCOI) composite substrates are another substrate alternative, combining the advantages of crystalline and poly-SiC substrates and facilitating the substrate thinning possibilities [3.46]. With the application of the Smart Cut[®] and cleaving technology, a 270 nm SiC layer is bonded onto the oxide of a silicon(100) handle substrate [3.16].

The MOCVD growth of GaN on SiC is facilitated, as the lattice-constant of the SiC material is decisive for the HEMT layers, as reported in [3.217]. A growth recipe for GaN HEMT on SiC can be used. AlGaIn/GaN HEMTs fabricated based on this procedure yield similar DC-characteristics and breakdown voltages as devices fabricated on silicon(111) substrates. The devices grown on the hybrid substrates show stronger thermal compression of the output characteristics. This is attributed to the increased thermal resistance R_{th} of the SiO₂ layer. The advantage of silicon and SiC are combined in the silicon on polycrystalline SiC (SopSiC) technology [3.108, 3.129]. A high resistivity silicon wafer is bonded on top of a polycrystalline SiC substrate. Smart-Cut splitting is used to remove some of the HR-silicon substrate, so that a crystalline substrate surface is maintained. The composite substrate has the good thermo-mechanical properties of polycrystalline SiC. This allows to increase the substrate diameter beyond the diameter of available s.i. SiC substrates. A MOCVD-based wafer technology on metallic nickel substrates is described in [3.209]. The metallic substrate is based on nickel electroplating and laser lift-off. Prior to lift-off, the Schottky diode epitaxial layers are grown by MOCVD on sapphire substrates. MBE growth of GaN on LiGaO₂ is described in [3.38]. Lithium gallate has limited thermal conductivity, while it has a very low lattice-mismatch relative to all other hetero-substrates available for III-N devices. As a true insulator, the RF-losses can be greatly reduced compared to compensated material. The material grown by MBE has a TDD of only $4\text{--}5 \times 10^8 \text{ cm}^{-2}$. AlGaIn/GaN HEMT on AlN templates on sapphire are reported in [3.8]. The TDD can be reduced to $1.5 \times 10^8 \text{ cm}^{-2}$ in this case.

3.1.4 Epitaxial Lateral Overgrowth (ELO)

Epitaxial lateral overgrowth (LEO) or (ELO(G)) is most important in the reduction of the dislocation density especially for III-N optoelectronic devices such as lasers [3.141]. A good overview of ELO is given in [3.51]. Threading dislocation densities as low as $2.2 \times 10^7 \text{ cm}^{-2}$ are reported in [3.53]. Several examples exist for ELO growth for electronic devices. The effect of threading dislocations on AlGaIn/GaN HBT performance is reported in [3.127]. Device results obtained on conventional substrates and ELO substrates are compared. The reduction of the threading dislocation is found crucial for the reduction of the emitter-collector leakage, which is reduced by four orders of magnitude. A comparison of AlGaIn/GaN HEMTs on sapphire substrates with and without grooves is provided in [3.45]. The devices with local grooves and increased crystalline quality yield an increase of drain current, transconductance, and output power. Further, the leakage currents are reduced.

3.1.5 Hydride Vapor Phase Epitaxy (HVPE)

HVPE is a very attractive option as a high-throughput and low-cost methodology for the growth of GaN quasi-substrates [3.159] due to its high growth

rate, which enables very thick III-N layers [3.198]. The growth rates for HVPE of device layers are typically adjusted to $0.05\text{--}0.3\mu\text{m min}^{-1}$, as reported in [3.109]. A good overview of the growth of GaN by HVPE is given in [3.198]. The principle of hydride vapor phase epitaxy for III-V element semiconductor is based on the flow of group-V hydride precursors and hydrogen chlorides in combination with nitrogen through a multizone furnace, typically consisting of quartz. The furnace has three functions and areas: a source zone, a mixing zone, and a deposition zone.

A quasi-substrate approach for epitaxial layer growth is presented in [3.159]. The HVPE layers are grown on GaN MOCVD templates on sapphire substrate. A detailed strain analysis is performed, which explains the strong wafer bending after removal of the sapphire substrate. Thicker sapphire substrates are suggested to reduce the wafer bending. On the device level, the fabrication and characterization of heterojunction GaN diodes is described in [3.35]. The active GaN layers are grown by HVPE on 4H-SiC substrates. Layers with thicknesses between 10 and $200\mu\text{m}$ grown by HVPE are investigated. GaN/AlGaIn HEMTs grown by HVPE on AlN/SiC substrates are described in [3.109]. A $30\mu\text{m}$ -thick insulating AlN layer is deposited on undoped conducting SiC substrates. The actual HEMT layer structure consists of a $3\mu\text{m}$ -thick GaN layer and a 40 nm -thick $\text{Al}_{0.28}\text{Ga}_{0.72}\text{N}$ layer grown by MOCVD. The device yields relatively low low-frequency dispersion, which is attributed to the reduction of the lattice-mismatch and the consequent dislocation reduction in the very thick AlN buffer layer. The use of HVPE-grown buffer layers on sapphire substrate is described in [3.52]. MBE is used to grow the epitaxial layers. The uniformity of the device DC-parameters despite the more complicated approach. Complete growth of AlGaIn/GaN HEMTs by HVPE on sapphire substrates is reported in [3.123]. Both buffer layers and epitaxial layers are grown by HVPE and yield an RMS surface roughness of $\leq 0.2\text{ nm}$. AlGaIn/GaN HEMTs with a gate length $l_g = 1\mu\text{m}$ are defined with a transconductance in excess of 110 mS mm^{-1} and $I_{\text{Dmax}} = 0.6\text{ A mm}^{-1}$.

3.2 Indium-Based Compounds and Heterostructures

The growth of (Al)In(Ga)N and related ternary and quaternary materials for electronic applications has not yet been as exploited as the growth of (Al)GaN [3.2]. The InGaIn/GaN heterostructures are essentially developed for optoelectronic applications, e.g., [3.176]. The promise of very low effective masses of InN down to $0.05m_e$, see [3.49], and the remarkable transport properties [3.177] motivate the development of growth for electronics, e.g., [3.116, 3.130, 3.151, 3.175, 3.224]. The growth kinetics of InN and InGaIn are reviewed, e.g., in [3.14, 3.225]. In general, the decomposition temperature of InN is relatively low, typically $\leq 600^\circ\text{C}$, as mentioned in [3.73]. The growth of InAlN is described, e.g., in [3.74, 3.91]. Thus, the growth temperatures of InN by MOCVD typically amount to $300\text{--}500^\circ\text{C}$. This temperature range is

typically too low for the growth of low-defect material, when MOCVD growth or ammonia-based MBE are being used. This is due to the decomposition rate of the ammonia gas in the reactor [3.73], as the temperature must satisfy the temperature conditions of NH_3 pyrolysis, while the dissociation of InN must be avoided [3.146]. The realization of double heterojunction FETs is very desirable, since the enhancement of the confinement effect in double heterojunction is favorable for device performance [3.115]. In-inclusion may help to increase the flexibility of the barrier definition at the frontside and the backside of the channel [3.116]. Further, increased sheet carrier densities can be achieved in InAlN/GaN heterostructures, as discussed below [3.91, 3.122].

3.2.1 MOCVD Growth of Indium-Based Layers

Early reports on MOCVD growth of InN on various substrates, such as Al_2O_3 or even GaAs, can be found in [3.226]. Growth is performed at atmospheric pressure on $\alpha\text{-Al}_2\text{O}_3$, and good conductive properties are reached with intrinsic concentrations $n = 5 \times 10^{19} \text{ cm}^{-3}$ and Hall mobility values of $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. In more recent reports, low-temperature MOCVD growth of InN is analyzed, e.g., in [3.173]. Thin InN films of 100 nm thickness are grown at 530°C on low-temperature (grown at 400°C) InN nucleation layers and on high-temperature GaN buffer layers. A near band-edge PL emission of 0.75 eV is observed already in this publication, which points to the revision of the bandgap energy of InN. On the device level a comparison of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}/\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ and $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{InGaN}/\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ double heterostructure HEMTs (DHHEMTs) grown by MOCVD on s.i. SiC substrates is given in [3.122]. The comparison of the devices at 77 K proves the superiority of the double heterostructure concept with respect to 2DEG mobility and sheet carrier density. AlGaN/GaN/AlGaN DHHEMTs show enhanced mobility relative to the AlGaN/GaN single heterostructures. The mobility amounts to $>8,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the DHHEMT at 77 K. The inclusion of a $\text{In}_x\text{Ga}_{1-x}\text{N}$ layer with $x = 6\%$ leads to an increase of the mobility for a given sheet carrier density.

Growth Conditions: Material Transport and Temperature

Growth conditions of InN by MOCVD are characterized by low growth-temperatures and high growth-pressures [3.14]. It is the most difficult among the III-nitrides because of the low dissociation temperature of InN and the high equilibrium N_2 pressure. A good overview on the growth parameters and the substrate situation is given there [3.14]. InN growth on sapphire substrate by MOCVD reported in [3.226] yields InN with carrier densities of $5 \times 10^{19} \text{ cm}^{-3}$ and a room-temperature Hall mobility of $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. A very high V/III ratio of 10^5 is used for MOCVD in this case. TMI and ammonia are used as precursors at growth temperatures of $450\text{--}550^\circ\text{C}$ and reactor pressures of 0.1–1 bar. The increase of the growth rate and the use of

nitrogen increase the In incorporation at a given temperature, as reported in [3.36]. The impact of reactant gas on the growth of InN by MOVPE is reported in [3.227]. Growth rates of InN as high as $2\mu\text{m h}^{-1}$ are reached. A $0.5\mu\text{m}$ thick InN layer yields intrinsic carrier concentrations of 10^{19} – 10^{20} cm^{-3} . The room-temperature Hall mobility range is 260 – $120\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$. Growth temperatures of 400 – 600°C have been used. A 1 nm thick $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}$ notch can be introduced into the GaN/AlGaIn SHHEMT layer sequence to form a double heterostructure composed of GaN/ $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}$ /AlGaIn [3.154, 3.224]. The GaN buffer growth is performed at 550°C . The temperature is then increased to 810°C for the growth of the InGaIn. A 11 nm -thick GaN channel is grown at 920°C , followed by an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier grown at $1,020^\circ\text{C}$ [3.153]. The devices yield excellent cut-off frequencies of $\geq 150\text{ GHz}$ for a gate length of 100 nm .

3.2.2 MBE Growth of Indium-Based Layers

Molecular beam epitaxy, especially plasma-assisted MBE, is advantageous for the growth of indium-based compounds, as the growth temperature can be modified significantly as compared to MOCVD growth. Nitrogen radicals can be generated in the plasma source independent from the growth temperature, which does not have to satisfy the requirements of NH_3 pyrolysis. This principal effect especially increases the material quality. A review of MBE growth of InN and InGaIn is given in [3.146].

Growth Conditions: Temperature and Material Transport

Reports on the growth of InN films and InAlIn/InN heterostructures similar to the InGaAs/InAlAs material system can be found in various publications, e.g., in [3.74, 3.76, 3.146, 3.199]. The bandgap energy of InN has been under constant investigation during the development of the material system. A good review of the recent material development and bandgap investigations of InN and InGaIn is given in [3.147]. Recent estimates of the bandgap energy of InN derived from photoluminescence properties of undoped and Si-doped InN films grown by PAMBE amount to 0.76 eV at RT [3.76]. The impact of the interface and crystalline effects is further detailed. In general, the material quality can be improved significantly by PAMBE growth, as compared to ammonia-based MBE and MOCVD. Indium incorporation and surface segregation during $\text{In}_x\text{Ga}_{1-x}\text{N}$ growth by PAMBE are discussed in [3.24]. The temperature for the growth of InGaIn on sapphire substrates is chosen between 580 and 620°C . A low-temperature GaN buffer is grown at 550°C . The growth rates for both GaN and InGaIn amount to 200 nm h^{-1} . The material fluxes are adjusted to match $\text{In}_x\text{Ga}_{1-x}\text{N}$ with an indium fractions of 0 – 0.5 . High-quality InN films based on plasma-assisted MBE are reported in [3.73]. The growth temperature for the low-temperature InN buffer layer amounts to 240 – 420°C , while the actual InN layers are grown at 380 – 520°C . Both an annealing step at growth

temperature and a rapid cooling at 200°C after the actual growth are applied. The mobility increases as a function of growth temperature between 380 and 490°C, whereas the intrinsic carrier concentration drops. The maximum Hall mobility at room temperature reaches $1,420 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at a background electron concentration of $1.4 \times 10^{18} \text{ cm}^{-3}$. The corresponding growth temperature is 490°C. Earlier reports in [3.71] show Hall mobilities of $1,420 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at electron concentrations of $1.6 \times 10^{18} \text{ cm}^{-3}$ for 350 nm thick films. PAMBE growth, characterization, and properties of InN and $\text{In}_x\text{Ga}_{1-x}\text{N}$ on sapphire substrates are further reported in [3.146]. The importance of the V/III ratio is pointed out in a trade-off between In-droplet formation (In-rich growth) and high N-partial pressure (to avoid dissociation). Considering both limitations the V/III ratio at the surface should be controlled to stoichiometry maintaining the the surface slightly N-rich [3.146]. The growth temperature is chosen between 460 and 550°C. Further, the importance of the nitridation procedure on the sapphire and the two-step growth with the low-temperature buffer are highlighted. The effects of atomic hydrogen irradiation on indium incorporation and ordering in $\text{In}_x\text{Ga}_{1-x}\text{N}$ grown by RF-MBE at 640–700°C are discussed in [3.152]. The indium incorporation and ordering are enhanced by the presence of H_2 . InAlN is grown by MBE at a temperature below 460°C for the incorporation of In due to the weak In-N bond [3.91]. The next paragraph addresses heterostructure growth.

3.2.3 Indium-Based Heterostructure Growth

Both (In)GaN/InAlN and InGaN/GaN heterostructures can be formed once indium sources are available in the growth system. Al-rich $\text{In}_y\text{Al}_{1-y}\text{N}$ can be used effectively as barrier material for heterostructures with high sheet carrier densities [3.91]. Growth temperatures of 400 and 480°C are reported in [3.72] for the growth of $\text{In}_{0.15}\text{Al}_{0.85}\text{N}$ barriers on GaN by PAMBE on sapphire substrates. Sheet carrier densities of $1.7 \times 10^{13} \text{ cm}^{-2}$ and associated Hall mobility values of $654 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature are reported using an additional AlN interlayer. After the growth of an AlN-nucleation layer at 900°C, the GaN buffer layer is grown at 730°C by PAMBE. The AlN interlayer with a nominal thickness of 1.3 nm is grown at 760°C. For the $\text{In}_{0.15}\text{Al}_{0.85}\text{N}$ barrier layer, the growth is performed at 400 and 480°C. Better mobility and surface quality are achieved for the higher growth temperature. The subsequent processing of InAlN/GaN HFETs is also reported.

$\text{In}_{0.2}\text{Al}_{0.8}\text{N}$ /GaN heterostructures grown by MOCVD on sapphire(0001) substrates are given in [3.107]. The layer sequence includes a low-temperature GaN nucleation layer, a 1.4 μm -thick GaN buffer layer, and a 10 nm $\text{In}_{0.2}\text{Al}_{0.8}\text{N}$ barrier layer grown between 800 and 850°C. The Hall mobility and sheet carrier concentration amount to $2 \times 10^{13} \text{ cm}^{-2}$ and $260 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. InAlN/GaN heterostructures grown by MOCVD on silicon(111) substrate are reported in [3.210]. A 300 nm-thick (Al)GaN nucleation layer is deposited on high-resistivity 3-in. n-silicon substrates. A 1 μm -thick GaN buffer is capped

by an $\text{In}_{0.16}\text{Al}_{0.84}\text{N}$ barrier layer. A 1 nm AlN layer can be included between channel and barrier. The barrier layer thickness is 20–25 nm. The Hall mobility amounts to $1,200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ without inclusion layer, and $1,800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with AlN-inclusion layer. The related sheet carrier densities are 0.8×10^{13} and $1.5 \times 10^{13} \text{ cm}^{-2}$. The findings in this section demonstrate the potential to increase the sheet carrier density in the heterostructures with the use of In and potentially to improve the associated mobility.

3.3 Doping and Defects

Doping and defects are fundamental for electronic device fabrication in any semiconductor system [3.202]. Defects in MOCVD- [3.143] and MBE-grown material [3.69] are found to be strongly growth-method dependent, as reported in various publications, e.g., [3.57, 3.118, 3.170]. Defects can be categorized in point, line, and areal defects [3.119, 3.170]. The important point defects are vacancies and interstitials, the line defects are threading dislocations, and areal defect are stacking faults [3.119]. These defects are thus discussed for each growth method. Good overview articles on defects in III-N materials are given in [3.118, 3.138, 3.160]. Early overview data for defect related donors, acceptors, and traps in GaN grown by MOCVD, MBE, and HVPE are given in [3.118]. The impact of surface stoichiometry and polarity on the defect structure for GaN is discussed in [3.178]. Point defects can be deliberately generated by various types of irradiation, such as electrons, protons, ions, γ -ray, and metal deposition by electron beam. The signatures obtained from the defect creation can then be compared to as-grown materials. It is stressed in [3.118] that shallow defects are dominating and that impurities such as Si and O are dominant in early as-grown GaN layers rather than defects. Threading dislocations in n-GaN are reported to have an acceptor-like behavior [3.118].

A very recent extensive review of the luminescence of defects in GaN, InN, and AlN is given in [3.170]. GaN is considered to break the long-standing paradigm that high defect densities precludes electronic device performance. Minimum nonintentional acceptor concentrations are found to be 10^{15} cm^{-3} even in the purest material. This also leads to a minimum of uncontrolled compensation in n-type material. Zn, Mg, C, Si, H, O, Be, Mn, and Cd are considered the most important impurities. The dominant role of extended defects such as threading dislocations and point defects such as nitrogen vacancies is also discussed in [3.160]. It has further been found in GaN and the related materials AlN, InN, InGa_{1-x}N_x, AlGa_{1-x}N_x, that hydrogen is present in relatively high concentrations in as-grown samples, especially in p-type GaN [3.148]. It has been shown experimentally that the amount of oxygen present during material growth can have a strong influence on the background conductivity, indicating that it is a shallow donor in GaN. Carbon can also be a significant residual impurity in MOCVD-grown nitrides. Its

source is typically the precursor. Typical characterization methods for defects include [3.118] the following:

- Temperature-dependent Hall measurements for the determination of the donor and acceptor concentrations
- X-ray diffraction (XRD)
- Transmission electron microscopy (TEM)
- Photoluminescence (PL)
- Atomic force microscopy (AFM)
- Positron annihilation spectroscopy (PAS)
- Magneto-resonance
- Deep-level transient spectroscopy (DLTS) [3.118]

The analysis of threading dislocations has already been mentioned. A more detailed analysis is presented in the following.

3.3.1 MOCVD Growth

Shallow- and deep-level defects in n-doped GaN grown by MOCVD are described in [3.54].

Doping in n-Doped and p-Doped MOCVD Material

Silicon introduces a shallow donor level in GaN at $E_C - 0.022$ eV [3.54, 3.56] and is found to be the dominant donor impurity in unintentionally (nid)-doped material. A deeper donor is also found at $E_C - 0.034$ eV. Oxygen is another donor for GaN [3.160]. It is found to have a strong impact on the n-type background conductivity. It is prevailing due to the precursor NH_3 in MOCVD-grown material. A donor state at $E_C - 0.078$ eV is mentioned.

Mg and Zn are the most important acceptors in a number of p-dopants for III-N semiconductors, such as C-, Mg-, and Be-. They generally are not very efficient acceptors. The p-doping of GaN is complicated by the following effects, which have been named repeatedly [3.143]:

- Large thermal activation energy of 120–200 meV [3.54]
- Hydrogen passivation of MOCVD-grown GaN:Mg [3.143, 3.160] and
- Significant Mg reactor memory leading to broad Mg profiles, reported, e.g., in [3.62, 3.186]

Early overviews of the compensation mechanisms of p-doping are given by Nakamura in [3.143] and further, e.g., in [3.105, 3.121]. Mg has been described early as an acceptor in GaN at an electronic level of approx. $E_V + 0.2$ eV, e.g., in [3.54]. It is the most important acceptor for GaN. A midgap trap level is isolated in p-type GaN with a photoionization energy of 1.8 eV. However, none of the deep levels is found to be of sufficient concentration to compensate the shallow acceptors. Mg accumulation effects in bulk samples at doping levels of 3×10^{19} to $9 \times 10^{19} \text{ cm}^{-3}$ due to surface treatment and air exposure

are reported in [3.62]. A strong surface band bending is observed of 1.2–1.6 eV for GaN:Mg. This is considered to be due to high-density surface states. Even strong wet etching by KOH and NH_4OH does not modify this high surface state density [3.62]. Hydrogen in general plays a dominant role for the passivation of acceptors [3.160]. Early reports of the activation of p-type GaN material by post-annealing steps at 800°C in nitrogen are given in [3.121, 3.143]. A more detailed overview on the impact of hydrogen is given in [3.160]. Carbon is a residual impurity in MOCVD-grown material. C is discussed to be both an acceptor and an amphoteric. Maximum hole concentrations of $3 \times 10^{17} \text{ cm}^{-3}$ are reached at a mobility of $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [3.160]. P-doping of AlGaIn is even more complicated than GaN, as reported, e.g., in [3.47]. The background is the even higher activation energy of Mg in AlGaIn, the increased compensation due to Si in the precursors, and the interaction with Si, C, and O. The measured hole concentrations in AlGaIn are even more strongly reduced than in GaN. Other p-dopants such as Ca, Zn, C, and Cd in the material have to be considered, as also reported in the overview on defects in GaN in [3.160].

Defects in MOCVD-Grown Material

Defect concentrations in the form of threading dislocations and other defects are of critical importance, as most of the electronic devices are grown by heteroepitaxy and a minimum mismatch relative to the semiconductor layers. A great number of reports exist on different defect types [3.138, 3.160, 3.170]. DLTS analysis of the barrier-layer material AlGaIn is of importance due to the impact on dispersion in III-N FETs, similar to that of AlGaAs in GaAs PHEMTs. A donor-like deep-level defect in $\text{Al}_{0.12}\text{Ga}_{0.88}\text{N}$ grown by MOCVD on SiC substrate is found by DLTS at $E_C - 0.77 \text{ eV}$, as reported in [3.55]. Deep levels are found by DLTS at threshold energies of 0.83 and 1.01 eV in n-doped GaN [3.54] grown by MOCVD. Further deep levels between $E_C - 0.87 \text{ eV}$ and $E_C - 1.59 \text{ eV}$ are reported. Luminescence, especially yellow luminescence, is of particular interest for electronic material analysis, e.g., by photoluminescence and surface photovoltage spectroscopy [3.181]. Yellow luminescence and related deep traps in undoped GaN grown by MOCVD are investigated in [3.22, 3.181]. For GaN layers the band energy of the luminescence is about 2.2 eV with a broad spectrum. It is present for different substrate types. The background of this emission are deep traps about 1 eV above the valence band which capture photoelectrons. Localized high current densities around screw dislocations in GaN films grown by MOCVD are investigated by ballistic electron emission spectroscopy (BEEM) in [3.18]. A correlation of the threading dislocations and charged traps is suggested, which leads to poor Schottky characteristics. Both donor- and acceptor-type behavior of threading dislocations are reported, as also stated in [3.118]. Apart from the detailed detection of single defects and traps, the correlation of defects with device performance is interesting. Deep traps in GaN MESFETs and their correlation with current

collapse are analyzed in [3.55]. Two electron trap energies are isolated for this n-channel device. The defect energies of 1.8 and 2.85 eV below the conduction band have also been reported in other publications, e.g., in [3.22]. Variation of the edge dislocation concentration with the AlN nucleation layer design is directly correlated with the AlGaN/GaN reliability [3.57]. Traps can also be created by device operation and related degradation, as reported in [3.187]. Further analysis is provided in Chaps. 4 and 7.

3.3.2 MBE Growth

Surveys on doping and defects for MBE-grown materials are given, e.g., in [3.160, 3.170, 3.203].

Doping of n-doped and p-doped MBE Material

The most important n-dopant in MBE material is silicon. N-doped GaN material grown by MBE is characterized by a number of particular defects. Deep-level transient spectroscopy (DLTS) investigations in MBE-grown GaN material are given in [3.69]. The n-type GaN material is grown by MBE on MOCVD-grown templates on sapphire substrate. The characteristic capture-time constant obtained amounts to $8.6\mu\text{s}$ for a line-type deep trap at $E_C - 0.91\text{ eV}$. A defect found at $E_C - 0.59\text{ eV}$ does not show the behavior of a line or point defect. A comparison of the MBE growth of thin wurtzite GaN on 6H-SiC, silicon(111), and sapphire substrates is given in [3.190]. Cross-sectional TEM measurements of the n-type GaN materials reveal the domination of threading defects at the substrate/buffer or buffer/film interfaces at residual concentrations of $10^8\text{--}10^9\text{ cm}^{-2}$.

N-doping is typically performed by standard silicon effusion cells, e.g., [3.68]. Silane can be used as a silicon source for ammonia-based MBE [3.194]. Next to silicon, oxygen is also considered as a donor for MBE grown material [3.160]. Residual water vapor in MBE chambers or oxygen impurities leaked from the quartz containment vessel often employed in N_2 plasma sources is considered as the source.

P-doping of MBE material is different from that of MOCVD material. Typical for MBE, the doping profiles of MBE III-N material can be very sharp. Mg p-doping of GaN by PAMBE on MOCVD-grown GaN templates on sapphire substrates is described in [3.186]. MBE growth can cure two further disadvantages of GaN:Mg growth by MOCVD. It avoids hydrogen passivation of the Mg, and no Mg reactor memory is observed during MBE growth. The GaN:Mg layers are grown by PAMBE at 650°C . Mobilities $\mu_p = 24\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at $p = 1.8 \times 10^{17}\text{ cm}^{-3}$ and $\mu_p = 7.5\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at $p = 1.4 \times 10^{18}\text{ cm}^{-3}$ are reached. The incorporation of Mg is uniform and very sharp profiles can be realized due to the low growth temperature, as verified by SIMS measurements. The sharp profiles further allow very precise superlattice engineering and Mg profiling, as reported in [3.106]. Superlattice dimensions are varied

between 2 and 14 nm in order to enhance the active hole concentration in the superlattice beyond 10^{18} cm^{-3} , especially at low temperatures.

Defects in MBE Material

Deep level defects in n-type GaN material grown by MBE are described, e.g., in [3.207] found by DLTS. Five deep traps are reported between $E_C - 0.23 \text{ eV}$ and $E_C - 0.96 \text{ eV}$. The capture cross-sections amount to $2 \times 10^{-15} \text{ cm}^2$ (0.59 eV) and $3 \times 10^{-14} \text{ cm}^2$ (0.91 eV). Similar point defect serving as electron traps are found at $E_C - 0.06 \text{ eV}$ and at $E_C - 0.9 \text{ eV}$. Capture cross-sections of 5.0×10^{-15} and $7.4 \times 10^{-17} \text{ cm}^2$ are determined for electron levels of 0.21 and 0.23 eV in PAMBE-grown AlGaIn/GaN/AlGaIn heterostructure material [3.158]. The 0.21 eV defect is related to a nitrogen vacancy, while 0.23 eV is associated with extended defects.

Defect microstructure of thin wurtzite GaN films grown by MBE on SiC substrates, silicon substrates, and sapphire substrates are analyzed by TEM in [3.190]. Threading dislocations are line defects along the growth direction. The defect microstructure is dominated by threading defects that originated at the buffer/substrate or buffer/epialyer interface. A defect density of 10^8 – 10^9 cm^{-2} is found to be prevailing depending on the substrate. This density is residual despite the reduction of defects by the use of a 1 μm -thick buffer layer. HVPE-grown material has also been investigated in several publications, e.g., in [3.170, 3.223]. Three traps are isolated in [3.223] at energies $E_C - 0.65 \text{ eV}$, $E_C - 0.61 \text{ eV}$, and $E_C - 0.27 \text{ eV}$.

The previous section has demonstrated the impact of impurities and defects; however, the most important requirement for electronics is their avoidance and control during material growth, which is part of this chapter. Control of processed-induced defect creation will be addressed in Chapter 4.

3.4 Epitaxial Device Design

In the previous sections, a number of specific growth features and their characteristic methodologies have been discussed for the InGaIn/AlGaIn/InAlN/GaN material system. This section addresses particular features for device growth. As an example, Fig. 3.17 gives the layer sequence of advanced HFETs for both the III-As and the III-N material system. Fig. 3.17 visualizes and compares the concept of a double heterojunction and the specific device features with respect to epitaxial growth, as also proposed, e.g., in [3.104]. These features are detailed in the following sections and compared, where necessary, to III-As devices.

3.4.1 Geometrical Considerations

Geometrical considerations are numerous in the design of III-N devices. Most data are available on the fabrication of HFETs.

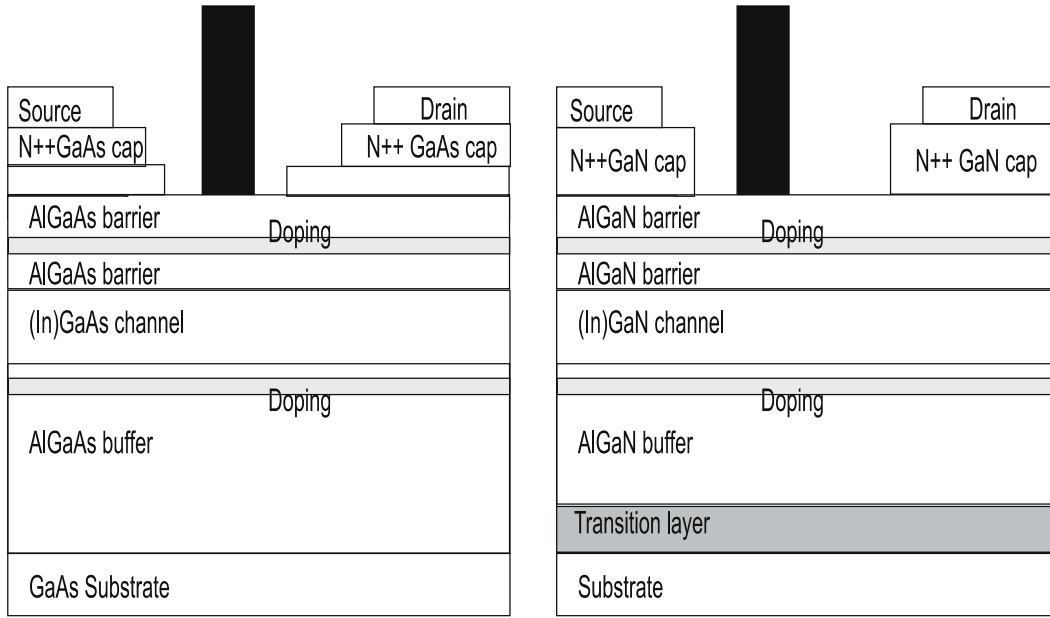


Fig. 3.17. Schemes of advanced double-heterojunction HFETs: (*left*) GaAs, (*right*) GaN

Barrier-Layer Design: Thickness

The barrier-layer thickness in HEMTs is a principal design feature. It is evaluated in [3.197]. Nonrecessed AlGaN/GaN HEMTs with barrier thicknesses of 10 and 20 nm are compared. As expected, the device with the thinner barrier layer shows reduced current due to the reduced polarization effects and higher transconductance. Further, a reduced saturated power density is obtained. RF-loadline measurements show the reduction of RF-full channel current as compared to DC full channel current and the increase in the RF-knee voltage for the devices with a smaller gate-to-channel separation. Thus there is a reduction in output power due to these surface-induced dispersive effects. The second effect on the output power at a given voltage is the expected reduced polarization effect, as also argued in [3.75]. The barrier thickness and mole fraction also strongly influence the vertical field distribution in the barrier, as measured by photoreflectance spectroscopy in [3.20]. The polarization effects lead to electrical fields $\geq 1 \text{ MV cm}^{-1}$ [3.220]. A systematic investigation of the gate-to-channel-separation is performed in [3.75] for AlGaN/GaN HEMTs with a gate-length of $1 \mu\text{m}$ grown by PAMBE on sapphire substrates. The gate-to-channel separation is varied between 8 and 25 nm. The reduction of the gate-to-channel separation leads to a significant increase of the transconductance from 185 to 360 mS mm^{-1} . At the same time, the drain current at $V_{\text{GS}} = 1 \text{ V}$ is reduced from 1.1 to 0.68 A mm^{-1} . The positive threshold voltage shift is about 0.23 V per 1 nm change of the layer thickness. For very-high operation frequencies, a gate-to-channel separation of 11.3 nm is used in [3.77] for an HFET with a gate length of 60 nm . Very

thin $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ layers in MOSHFETs are reported in [3.70]. A 7 nm-thick AlGa N layer leads to a threshold voltage of -0.3 V . The situation is close to a normally-off device. Al_2O_3 gate layers are used. The MOSHFET allows the overdrive of the device up to gate voltages of $+4\text{ V}$. Theoretical estimates for the impact of the barrier-layer thickness and the Al-content on the power performance and corresponding gain compression are discussed in [3.43]. An increase in output power is predicted with increasing barrier thickness and Al-content. Further geometrical issues for the design of (H)FETs include the following:

- The distance of δ -doping layers to the channel [3.48]
- The position of the (backside) InGa N layer to the channel [3.26, 3.153, 3.154]
- The thickness of doped Ga N layers in recess processes, e.g., in [3.98]

The distance of the δ -doping of AlGa N /Ga N HEMTs is optimized in a similar procedure as for GaAs PHEMTs, as reported in [3.48]. The considerations include scattering of the carrier in the channel and also doping efficiency. The optimum value amounts to 3–6 nm. The thickness of Ga N cap layers needs to be optimized with respect to the surface depletion, as performed in [3.98]. In recess structures, the layer depth needs to be adjusted to the Ga N etch process, as further described below and in Chapter 4.

Barrier-Layer Design: Mole Fraction

The Al-mole fraction in the barrier is a critical parameter in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ /Ga N and $\text{In}_x\text{Al}_{1-x}\text{N}$ /Ga N HFETs. Increased Al-contents promise higher sheet carrier concentrations in the channel at nearly constant mobilities. Devices with Al-concentrations of $\geq 35\%$ are reported, e.g., in [3.94, 3.222]. The findings with an increase of the mole fraction in the barrier layer include the following:

- Eventually a saturation of the sheet carrier concentration due to relaxation of the AlGa N barrier layer, and grain formation, which both reduce the polarization effects
- Reduced doping efficiency of the Si doping
- Increased ohmic contact resistances

Typically, optimized single heterostructure FETs have Al-contents of 20–30% [3.204]. Al-contents between 26 and 52% are investigated on 4-in. sapphire substrates in [3.136]. The increase in Al-content leads to reduced surface quality and increased gate leakage, especially for Al-contents of 52%. The geometrical considerations have already been discussed above.

3.4.2 Growth of Cap Layers

Cap layers are introduced to moderate the transition at the semiconductor-passivation interface. In many publications, thin undoped Ga N layers are

reported for improved contact formation, e.g., in [3.12, 3.216]. The thicknesses are 1 nm in [3.32, 3.135], 3 nm in [3.12], and up to 5 nm in [3.166, 3.216]. The specific formation of electron and hole gases in cap layers can be investigated by photorefectance spectroscopy [3.19, 3.191]. It becomes obvious, that small variation in the cap layers thickness in the nm-range have strong impact to the field distribution. Highly n-doped caps are generally used in any semiconductor system to facilitate ohmic contact formation in order to increase the density of states at the metal semiconductor interface. This is especially necessary for wide bandgap semiconductor devices, which require very high annealing temperatures to reach ohmic-type contacts. Highly-doped GaN caps have further repeatedly been suggested to reduce dispersive effects, e.g., in [3.12, 3.75, 3.97]. The resulting devices show reduced dispersion even for the unpassivated situation [3.182]. However, the high doping levels lead to prohibitive gate-leakage currents, which unfortunately reduce the operation voltage without the applications of further steps such as recessing to $V_{DS} = 15$ V only [3.182]. P-doped GaN caps with very high nominal Mg concentrations of $1 \times 10^{20} \text{ cm}^{-3}$ have been used to minimize RF- and DC-dispersion in AlGaIn/GaN HEMTs, as reported in [3.12, 3.30]. The physical effect of high n- and p-type doping concentration is similar and is based on the compensation of traps and related charge at the semiconductor/passivation interface. The effect of MOCVD growth-termination conditions at the top cap layer above the barrier layer and the impact of wafer cool-down on the performance of the total GaN FETs is further investigated in [3.93]. A modest improvement in the device power density is observed for wafers, if, after deposition of the AlGaIn layer under constant growth conditions, the samples are cooled down to room temperature in pure nitrogen. Insulating low-temperature-grown GaN-cap layers are used for the reduction of the dark currents in Schottky-barrier photodetectors [3.110]. The low-temperature GaN is grown at 560°C and reduces the dark current by four orders of magnitude. Superlattice cap layers have been recently proposed in order to reduce the source resistance of AlGaIn/GaN HFETs [3.140]. Fifty nanometer thick superlattice-cap layers followed by a 20 nm n^+ -doped GaN cap are proposed. The layer thicknesses of the AlGaIn barrier and of the superlattice layers are optimized with the aim to reduce the potential barrier at the AlGaIn/GaN channel interface below the ohmic contacts. This leads to on an overall reduction of the access resistances.

3.4.3 Doping

III-N devices are intrinsically doped by unintentional impurities and by polarization doping. In several reports, the intentional doping is completely based on the polarization mechanism, e.g., [3.39]. However, conventional impurity doping is used repeatedly in both HEMT [3.48] and HBT [3.128] structures for several reasons. On the device level, the impact of barrier doping on the performance of unpassivated AlGaIn/GaN/SiC HEMTs grown by MOCVD is

reported on in [3.13]. Conventionally doped unpassivated AlGaIn/GaN heterostructures are found to be less sensitive to dispersive mechanisms due to shielding of the channel from the barrier/dielectric interface. The effects of the variation of δ -doping and geometry in AlGaIn/GaN HEMTs on SiC substrate are described in [3.48]. Both the position and the nominal doping concentration of the δ -doping are varied for spacer thicknesses of 3–9 nm. The sheet charge is optimized for a spacer thickness of 6 nm, while the mobility increases with increased distance. A doped-channel AlGaIn/GaN HFET with isoelectronic doping in the channel is described in [3.83]. The thickness of the doped channel layer is 70 nm in this case, which is much larger than the typical extension of an AlGaIn/GaN channel layer, which is estimated to be ≤ 10 nm.

3.4.4 AlN Interlayer

The channel-barrier interface in HFETs has been optimized with respect to several aspects, e.g., interface roughness [3.139, 3.155] and trap reduction [3.9, 3.82]. To that end, AlGaIn/GaN high-power microwave HEMTs have been optimized by the introduction of a thin AlN interlayer with a thickness of a few monolayers, e.g., in [3.183]. The concept has repeatedly been published with different focuses [3.9, 3.11, 3.139]. The insertion of the thin AlN layer produces a larger effective conduction band discontinuity ΔE_C . This increase in effective ΔE_C is due to the polarization-induced dipole in the AlN [3.183]. This AlN interlayer concept implies the following advantages:

- Increased effective bandgap discontinuity [3.183]
- Decreased alloy scattering [3.9, 3.183] and thus increased channel mobility
- Increased mobility for a given sheet carrier concentration [3.139]
- Increased sheet carrier density [3.139]
- Reduced interface trapping [3.9]

Additional issues to be considered are the following:

- The introduction of an additional tunneling barrier near the ohmic contacts
- Potentially a diode-like access resistance [3.99], similar to RTD

This kind of diode-like behavior is caused by the potentially strong band bending at various bias conditions. If additionally an AlN interlayer is introduced to serve as a barrier layer, a resonance is possible between the contact and the diode. Fig. 3.18 gives the sheet carrier concentration and Hall mobility of AlGaIn/AlN/GaN heterostructures as a function of AlN interlayer thickness, as shown in [3.139]. An optimized mobility is found for the thickness of ≈ 1 nm with mobility values of $1,700 \text{ V s cm}^{-2}$. The sheet carrier concentration increases steadily from 0.9 to $1.4 \times 10^{13} \text{ cm}^{-2}$. Fig. 3.19 further gives the sheet resistance as a function of AlN-interlayer thickness. A minimum is found at an interlayer thickness of about 1 nm. Further analysis of the drift mobility as a function of carrier concentration in [3.9] shows that the effect of the AlN layer specifically enhances the mobility at high carrier concentrations. In another

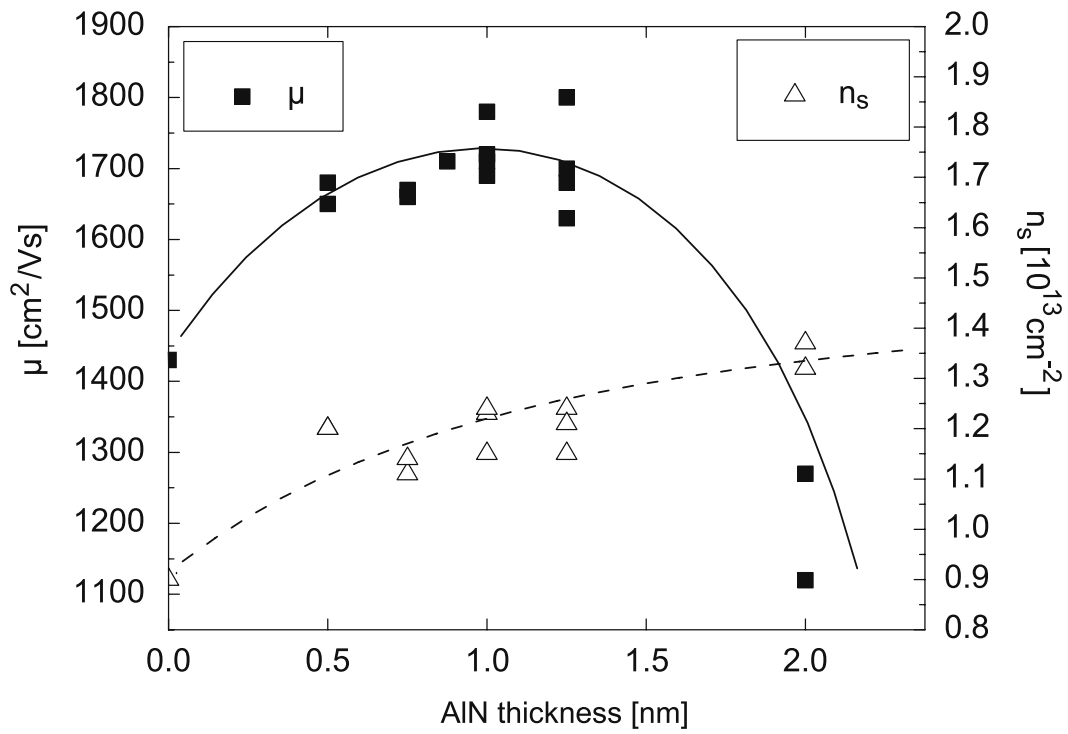


Fig. 3.18. Sheet-carrier concentration and mobility as a function of AlN interlayer thickness

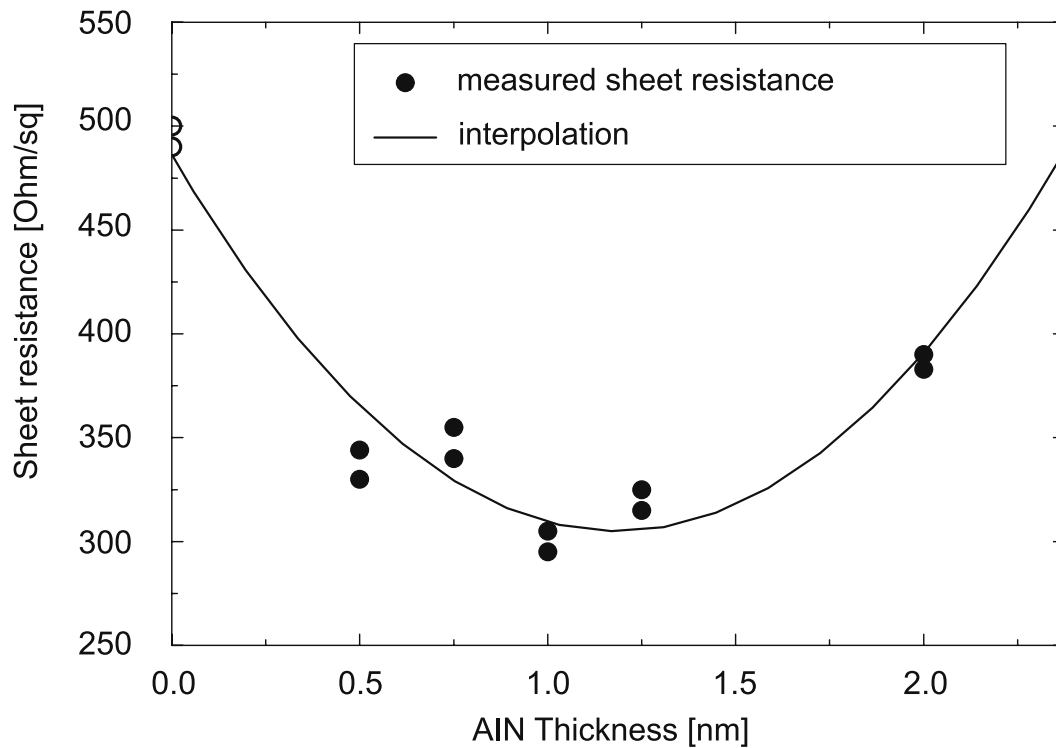


Fig. 3.19. Sheet resistance as a function of AlN interlayer thickness

device concept the AlGa_N barrier layer can also be completely removed and the effect of the barrier is then performed entirely by the AlN-interlayer, as reported in [3.155].

3.4.5 Channel Concepts

Simple planar HFET structures use the extended buffer layers under the barrier as channel layers. Near the interface, the GaN is highly conductive. Nominally, the channel layer is grown at a similar temperature to that used for the buffer layer, e.g., [3.92]. More advanced composite-channel concepts with varying Al-mole fractions in the channel/barrier have been introduced in [3.114]. The first channel forms at the Al_{0.3}Ga_{0.7}N/Al_{0.05}Ga_{0.95}N interface, while the second channel forms at the Al_{0.05}Ga_{0.95}N/GaN interface. It has further been suggested that this graded-channel concept enhances linearity at 2 GHz; however, the improvements in linearity claimed are within the statistical scattering of the measurement data. Doped HFET channels with isoelectronic Al-doping in the channel have been described in [3.83]. The Al-doping is used to improve the crystalline quality of the channel layer by reducing the amount of threading dislocations serving as acceptors. This leads to an overall enhancement of the mobility. However, the absolute values of the Hall mobility reported can also be achieved by other means. Further channel concepts are based on double heterostructures. The layers for this concept can be grown by both MOCVD and MBE. Al_{0.3}Ga_{0.7}N/GaN/Al_{0.05}Ga_{0.95}N based on MBE growth are described in [3.131]. The Al-fraction in the buffer has to be optimized with similar care as a GaN buffer with respect to unintentional doping, lattice mismatch, and defect mitigation. The Al-fraction thus cannot be chosen as freely as for a conventional AlGaAs/GaAs/AlGaAs HEMT layer structure.

3.4.6 Epitaxial In-Situ Device Passivation

Typically, the dielectric passivation in III-N devices is introduced by process-technological means, e.g., [3.136, 3.204]. This procedure is sometimes called ex-situ passivation. SiN can further be deposited in-situ, i.e., directly in the reactor growth chamber during MOCVD growth, as reported, e.g., in [3.201]. A thin SiN layer (4 nm) is deposited in the MOCVD chamber by flowing disilane and ammonia. The deposition is performed at a temperature of 980°C with a deposition rate of 0.1 Å s⁻¹ [3.27]. The growth temperature of the SiN is thus lower than that typically used for the AlGa_N barrier. MBE layers can also be passivated in-situ; however, this is not done in the same MBE reactor chambers, but using subsequent MOCVD growth. Such a procedure thus includes an interruption of the growth process, as reported, e.g., in [3.166]. The more technologically based features of device design, such as recesses, contacts, implantation, and device passivation issues, are discussed in Chapter 4.

3.5 Problems

1. *Discuss the major differences of III-N growth by MOCVD, HVPE, and MBE with respect to relative advantages/drawbacks!*
2. *For which kind of devices does MBE growth have unique properties?*
3. *Discuss the possible advantages and drawbacks of indium-based FETs!*
4. *Discuss epitaxial measures for dispersion control!*
5. *What are typical growth issues for III-N HBT layers?*
6. *Which particular improvements/drawbacks can be found for GaN heteroepitaxy of HFET layers on GaN substrates?*

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