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ENGINEERING MATERIALS AND PROCESSES

Gallium Nitride Processing for Electronics, Sensors and Spintronics

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With 241 Figures



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1 Advanced Processing of Gallium Nitride for Electronic Devices

1.1 Abstract

This chapter focuses on understanding and optimization of several key aspects of GaN device processing. For example, to activate ion-implanted dopants it is necessary to preserve the surface during the required high temperature anneal. A novel rapid thermal processing up to 1500°C, in conjunction with AlN encapsulation, is capable of activating high dose implants, although for most applications an anneal temperature of 1100–1150°C is sufficient to achieve reasonable activation. The activation processes of implanted Si or Group VI donors and common acceptors in GaN by using this ultrahigh temperature annealing, along with its effects on surface degradation, dopant redistribution and damage removal are discussed. 1400°C has proven to be the optimum temperature to achieve high activation efficiency and to repair the ion-induced lattice defects. Ion implantation can also be employed to create high resistivity GaN. Damage-related isolation with sheet resistances of $10^{12} \Omega/\square$ in n-GaN and $10^{10} \Omega/\square$ in p-GaN have been achieved by implanting O and transition metal elements. Effects of surface cleanliness on characteristics of GaN Schottky contacts have been investigated, and the reduction in barrier height was correlated with removing the native oxide that forms an insulating layer on the conventionally cleaned surface. W alloys have been deposited on Si-implanted samples and Mg-doped epilayers to achieve ohmic contacts with low resistance and better thermal stability than the existing non-refractory contact schemes. Dry etching damage in GaN has been studied systematically using Schottky diode measurements. Wet chemical etching and thermal annealing processes have been developed to restore the ion-degraded material properties.

1.2 Introduction

For the last three decades or so, the III–V semiconductor material system has been viewed as highly promising for semiconductor device applications at blue and UV wavelengths in much the same manner that its highly successful As-based and P-based counterparts have been exploited for infrared, red and yellow wavelengths. As members of the III–V nitrides family, AlN, GaN, InN and their alloys are all wide band-gap materials, and can crystallize in both wurtzite and zincblende polytypes. Wurtzite GaN, AlN and InN have direct room-temperature bandgaps of 3.4 eV, 6.2 eV and 1.9 eV, respectively (Figure 1.1). In cubic form, GaN and InN have direct bandgaps, while AlN is indirect. In view of the available wide range of direct bandgaps, GaN alloyed with AlN and InN may span a continuous range of direct bandgap energies throughout much of the visible spectrum well into the UV wavelengths. This makes the nitride system attractive for optoelectronic device applications, such as LEDs, laser (LDs), and detectors, which are active in the green, blue or UV wavelengths.[1] Although similar applications based on InGaAlP heterostructures have

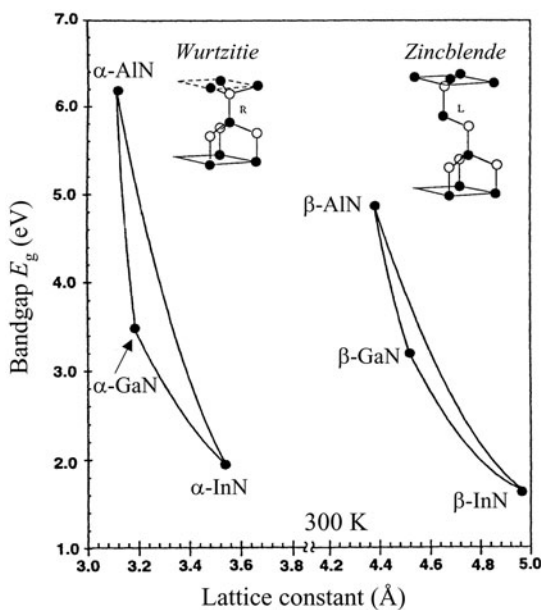


Figure 1.1. Bandgap of hexagonal (α -phase) and cubic (β -phase) InN, GaN, and AlN and their alloys versus lattice constant a_0

been successfully demonstrated, this material system is limited to about 550 nm. The addition of III–V nitrides to the family of device-quality semiconductors is essential for developing full-color displays (Figure 1.2) and coherent sources for high-density optical storage technologies, and very likely devices for signal and illumination application. In particular, the combination of GaN-based blue and green LEDs with GaAs-based red LEDs forms the basis for large-scale full displays and white light illumination. The solid-state white light source generated by mixing the primary colors in a light scrambling configuration would provide not only compactness and high lifetime, but also would reduce power consumption by 80–90% compared with incandescent or fluorescent light sources.

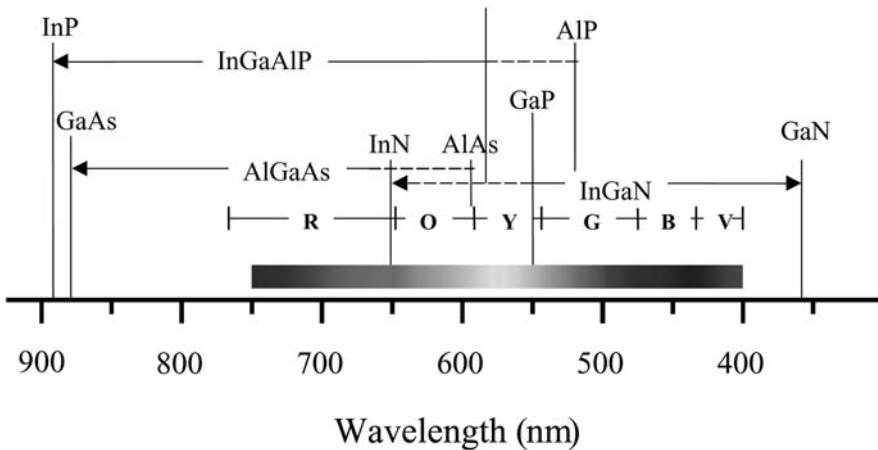


Figure 1.2. The various ternary and quaternary materials used for LEDs with the wavelength ranges indicated

Another area gaining a lot of attention for III–V nitrides is high temperature/high power electronics.[2] The interest stems from two intrinsic properties of this group of semiconductors. The first is their wide bandgap nature. The wide bandgap materials, such as GaN and SiC, are promising for high temperature applications because they go intrinsic at much higher temperatures than materials like Ge, Si and GaAs. This means that GaN power devices can operate with less cooling and fewer high-cost processing steps associated with complicated structures designed to maximize heat extraction. The second attractive property of III–V nitrides is that they have high breakdown fields. The critical electric field of the breakdown scales roughly with the square of the energy band gap, and is estimated to

be >4 MV/cm for GaN,[3] compared with 0.2 MV/cm and 0.4 MV/cm for Si and GaAs respectively. Figure 1.3 is a plot of avalanche and punch-through breakdown of GaN Schottky diodes calculated as a function of doping concentration and standoff layer thickness. It can be seen that a 20 kV device may be obtained with an ~ 100 μm thickness GaN layer with doping concentration $<10^{15}$ cm^{-3} .

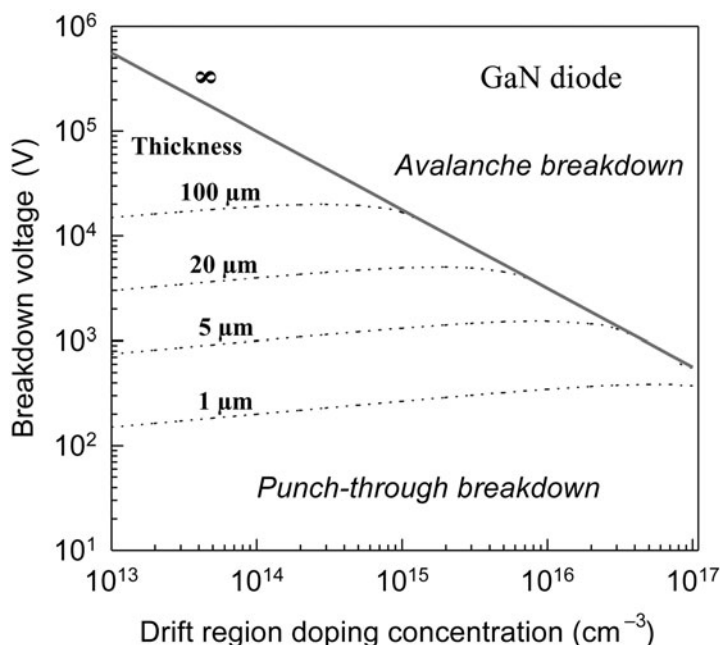


Figure 1.3. Calculated breakdown voltage as a function of doping concentration and thickness of the drift region in GaN M–n[–]–n⁺ diodes

GaN also has excellent electron transport properties, including good mobility, and high saturated drift velocity, as shown in Figure 1.4.[4] This makes it adequate for general electronics, and particularly promising for microwave rectifiers, particularly. The material properties associated with high temperature, high power, and high frequency application of GaN and several conventional semiconductors are summarized in Table 1.1. It is anticipated that GaN may eventually prove to be superior to SiC in this area.

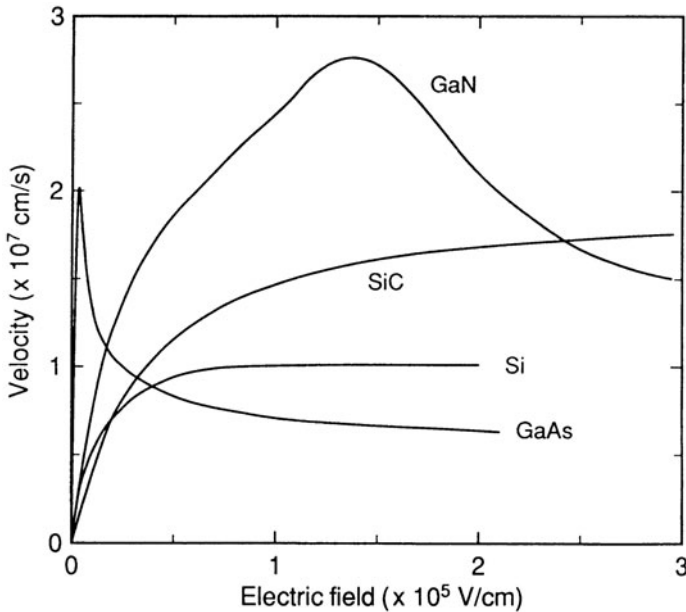


Figure 1.4. Electron drift velocity at 300 K in GaN, SiC, Si and GaAs computed using the Monte Carlo technique

The strongest feature of the III–V nitrides compared with SiC is the heterostructure technology it can support. Quantum well, modulation-doped hetero-interface, and heterojunction structures can all be made in this system, giving access to new spectral regions for optical devices and new operation regimes for electronic devices. From this point of view, III–V nitrides can be considered the wide band-gap equivalent of the AlGaAs–InGaAs system, which has set the modern benchmark for microwave device performance.

Other advantageous properties of III–V nitrides include high mechanical and thermal stability, large piezoelectric constants and the possibility of passivation by forming thin layers of Ga_2O_3 or Al_2O_3 with band gaps of 4.3 eV and 9.2 eV respectively. In addition, AlN has received considerable attention for its insulating property,[5] particularly as a potential isoelectronic insulator for GaAs FETs.

Table 1.1. Comparison of 300 K semiconductor material properties

Property	Si	GaAs	4H-SiC	GaN
Bandgap E_g (eV)	1.12	1.42	3.25	3.25
Breakdown field E_B (MV/cm)	0.25	0.4	3.0	3.0
Electron mobility μ (cm ² /V·s)	1350	6000	800	800
Maximum velocity v_s (10 ⁷ cm/s)	1.0	2.0	2.0	2.0
Thermal conductivity χ (W/cm·K)	1.5	0.5	4.9	4.9
Dielectric constant ϵ	11.8	12.8	9.7	9.7
CFOM = $\chi\epsilon\mu v_s E_B^2 / (\chi\epsilon\mu v_s E_B^2)_{Si}$	1	8	458	458

(CFOM=Combined figure of merit for high temperature/high power/high frequency applications)

Substantial research on III–V nitrides growth was initiated in the early 1960s. However, they have trailed way behind the easier-to-grow Si and GaAs semiconductors on the development curve. Nearly 30 years later, Si and GaAs have been pushed to their theoretical limits, while nitrides are just beginning to show their promise. The technological spin-offs came late because ideal substrates could not be found and the consequent growth of GaN thin films contained substantial concentrations of defects and had high n-type backgrounds. Even in films having relatively small background electron concentration, p-type doping could not be achieved until recently.

One particular difficulty in the growth of GaN thin films is the unavailability of sufficiently large (>1 cm) single crystals for use as substrate for homoepitaxial growth. Thus, up to now, heteroepitaxial growth has been a practical necessity and the choice of substrate is critical. Possible substrate materials should have low thermal expansion and lattice mismatch with the crystals grown. Also, they should be unaffected by the growth chemistries (such as NH₃ or H₂) at high growth temperatures (in excess of 1000°C in some cases). Under these presuppositions, sapphire and SiC are the most popular substrate materials used currently. When hexagonal GaN is grown on the (0001) basal plane of Al₂O₃, a lattice misfit of ~13% at the growth temperatures can generate a high density of dislocations and defects in the thin film. In the practical case, a large part of the misfit is relaxed through three-dimensional (3D) island growth. The residual strain is comparable to the lattice misfit between 6H-SiC and GaN, and the result is that comparable dislocation densities are observed.[6] Today, SiC substrates, though more costly, are of increasing interest for high temperature, high power devices like transistors due to their good thermal conductivity and possibility of n- and p-type doping. The materials with a close lattice match with GaN, such as LiAlO₂ [7] and LiGaO₂ [8], were also used for epitaxial

substrates. However, the GaN grown lacked the desired electronic properties due to either the rough growth or unintentional contamination from the substrates. The ideal candidate substrate is clearly a GaN wafer. Several research groups are investigating the growth of the bulk GaN crystals and very thick films through various techniques.[9–11] However, commercially available large-area GaN wafers appear to be several years away. The nitride community is, therefore, challenged with growth of heteroepitaxial films.

Many epitaxial thin film growth processes have been developed, including molecular beam epitaxy (MBE),[12,13] hydride vapor phase epitaxy (HVPE),[9–11,14] metalorganic chemical vapor deposition (MOCVD),[15–20] and derivatives of these methods. In the past few years, MOCVD has evolved into a leading technique for production of III–V-nitride optoelectronic and microelectronic devices. One remarkable application worthy mention is the achievement of super-bright blue LEDs.[18] Characteristics of this method include the use of high purity chemical sources, a high degree of composition control and uniformity, high growth rates, large-scale manufacturing potential and the ability to grow abrupt junctions.

Initially, the growth of GaN was performed directly on sapphire and SiC substrate, with large crystalline defects threading vertically from the substrate interface through the newly deposited thin film. The wafer usually had rough surfaces, mainly caused by the 3D growth mode. In 1986, Amano *et al.*[16] succeeded in remarkably improving the GaN surface morphology, as well as the electrical and optical properties, by deposition of a thin low-temperature AlN buffer layer prior to the high temperature growth of GaN. The essential role of this buffer is both to supply nucleation and promote lateral growth of the GaN film due to the decrease in interfacial free energy between the film and the substrate. Although the buffer layer has reduced the effects of the lattice mismatch, the densities of the threading defects in these thin films are still in the range of 10^9 – 10^{10} cm^{-2} , and on the order of one million times higher than in other semiconductor systems. These defect-laden materials, to date, have had a surprisingly small effect on the performance of both optical and electronic devices, but they may raise major questions as to the long-term stability of these devices. It is unlikely that the full promise of GaN and related alloys can be realized without a major reduction in the defect densities in the as-grown materials.

In 1994, the lateral epitaxial overgrowth (LEO) technique was employed to further improve the quality of the heteroepitaxially grown GaN by a marked reduction in defect density.[19] In this method, a layer of GaN grown by MOCVD is covered with 100–200 nm of amorphous SiO_2 and

Si_3N_4 with *ex situ* techniques. Small circular or rectangular "windows" are then etched through to the underlying GaN. A GaN film is subsequently regrown under conditions such that growth occurs epitaxially only in the windows and not on the mask. If growth continues, then lateral growth over the mask eventually occurs. Since most of the extended dislocations propagate in the growth direction through GaN, very few threading dislocations are visible in the regrown GaN that extends laterally over the mask. Marchand *et al.*[20] observed that the density of dislocation reaching the surface of LEO GaN was in the 10^4 – 10^5 cm^{-2} range, while the film over the window regions still contained high levels of the threading defects. Figure 1.5 compares the cross-section transmission electron microscopy (TEM) of a typical MOCVD growth and LEO GaN.

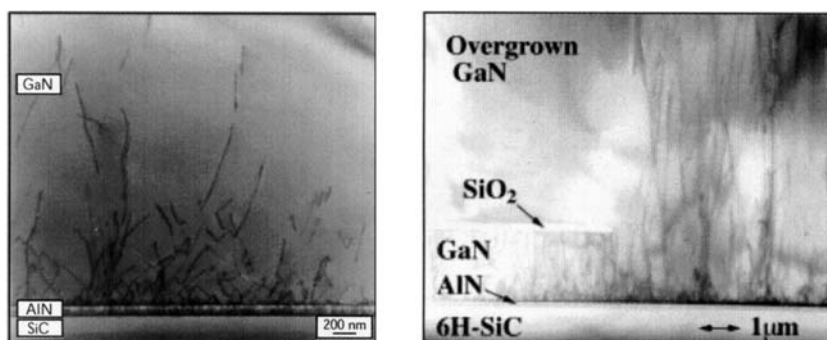


Figure 1.5. Cross-section TEM of typical MOCVD-grown GaN using an AlN buffer layer on SiC (left) and typical LEO GaN (right) (after Ref. [20])

A refined approach to a nearly dislocation-free GaN substrate for devices can be employed by two successive LEO steps with the mask of the second step positioned over the opening defined by the mask of the first step, thus blocking the defects that have grown out of the first windows. This complicated procedure offers the possibility of eliminating the disadvantages of heteroepitaxy, and will be important until GaN substrates become available.

In addition to growing GaN films with low defect densities, another key requirement for fabricating devices is the ability to control the desired electrical properties of the thin film precisely. In general, wide bandgap semiconductors are difficult to dope due to native defects. When the enthalpy for defect formation is lower than the band gap energy, the probability of generating a defect increases with the bandgap, *i.e.* the energy released by a donor-to-acceptor transition. Particularly for GaN, MOCVD-grown material is commonly n-type conductive, and N-vacancy

was long believed to be the dominant donor. Many attempts have been made to avoid N-vacancy formation by growing GaN at high pressures and high temperatures.[21,22] Efficient n-type doping of GaN through incorporation of Si during the growth proved relatively easy to achieve. Highly doping can also be created by implantation of Si or Group VI donors. Recently, Burm *et al.*[23] have shown a shallow Si implant at high dose to produce a doping density of $4 \times 10^{20} \text{ cm}^{-3}$, resulted in an extremely low ohmic contact resistance of $4 \times 10^{-8} \Omega \cdot \text{cm}^2$ using Ti–Au contacts.

Since conductivity is proportional to the product of carrier concentration and Hall mobility, another goal for GaN used in device applications is to obtain the highest Hall mobilities possible. Figure 1.6 summarizes the measured electron mobility in n-type GaN, along with the results obtained from Monte Carlo simulation.[24,25] As can be seen, the experimental data is roughly half of the calculated value, possibly due to significant scattering from impurities and defects in the state-of-the-art materials.

The III–V nitrides are expected to be made p-type by inserting column II elements such as Zn, Mg Be and Ca substitutionally for Ga to form single acceptors. However, all of these divalent elements form deep acceptors, the shallowest being Mg with an ionization level of 0.17 eV, which is still many kT above the valence band edge of GaN.[26] At this acceptor level, one should only expect <10% of the Mg atoms to be ionized at room temperature, which means the Mg concentration needs to be approximately two orders of magnitude larger than the desired hole concentration. When MOCVD is used as the growth method, it has been difficult to obtain p-type conductivity. It was later found that hydrogen plays a crucial role in passivating the Mg acceptors, and creates a neutral complex Mg–H that prevents the formation of holes in GaN.[27] It was first shown by Amano *et al.*[28] that p-type conductivity can be achieved by activating Mg-doped GaN using low-energy electron irradiation. Nakamura *et al.* demonstrated subsequently that the activation of Mg can also be realized by thermal annealing at $\sim 700^\circ\text{C}$.[29] Note that MBE-grown GaN doped with Mg may be p-type without a thermal activation process, because of the absence of hydrogen and H–N radicals during growth. In addition, p-type doping was also achieved by implanting Ca or Mg into GaN, followed by high temperature annealing ($\sim 1100^\circ\text{C}$).[30,31] The highest hole concentration reported so far is $\sim 10^{18} \text{ cm}^{-3}$, and the typical hole mobility is very low, often $10 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ or below, but allowing the realization of p–n junctions. Achieving low resistance ohmic contacts to the GaN layers with poor p-type doping concentrations has proved to be troublesome. Recently, Brandt *et al.*[32] found that by compensating Be with O a neutral dipole is formed that does not scatter the holes. Hence, a record high hole mobility

of $150 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ was obtained. This may be the ideal contact layer for GaN-based devices.

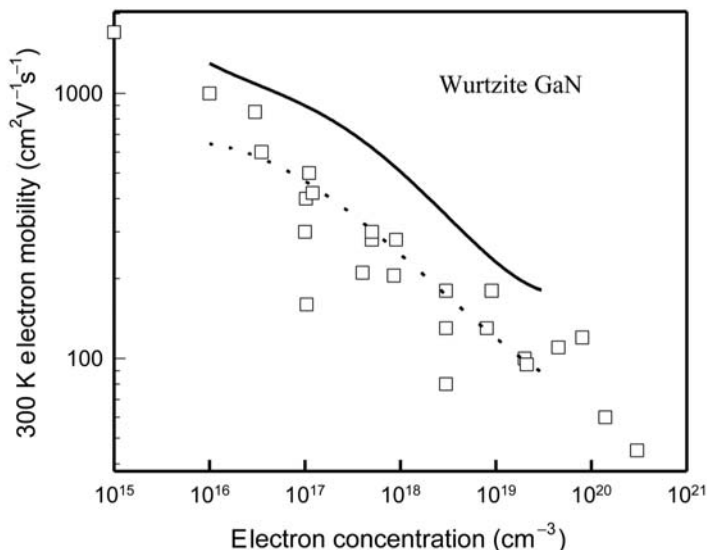


Figure 1.6. A survey of 300 K GaN electron Hall mobility values as reported by various groups. The solid line shows the calculated results for uncompensated n-GaN (after Ref. [24, 25])

The current level of the progress in the development of GaN commercially viable devices, namely GaN-based LEDs, LDs and UV detectors, has been the direct result of the realization of high quality crystals of GaN, AlGaIn, InGaIn, and the relatively recent achievement of p-type conduction in GaN. The first p–n junction LED was demonstrated by Amano *et al.*[28] in 1989. Following this, Nichia Chemical Industries announced the commercial availability of blue LEDs with high efficiency and luminous intensities over 1 cd.[18] In the subsequent years, high-brightness single quantum-well-structure blue, green, and yellow InGaIn LEDs with luminous intensities above 10 cd have been commercialized.[33,34] In 1996, Nakamura *et al.*[35] reported the first current-injection GaN-based LDs with separate confinement heterostructure, and subsequently achieved continuous-wave (CW) lasing at room temperature.[36] Figure 1.7 schematically shows the cross-section of the nitride-based laser diode. The active layer is an InGaIn multiquantum well with a large number of well layers. GaN and AlGaIn were used as the waveguide and cladding layers respectively. The mirror facet was formed by numerous methods, including dry etching, polishing or cleaving.

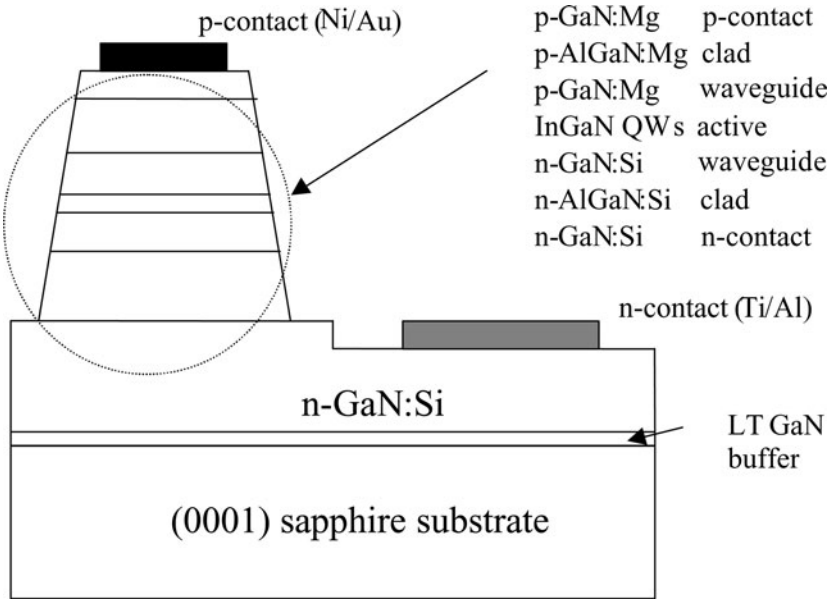


Figure 1.7. Cross-sectional view of a typical structure of GaN-based LD

Surprisingly, the high-density dislocations resulting from the heteroepitaxial growth on sapphire in these optical devices did not appear to be efficient nonradiative centers, as they are in other III–V materials. However, the crystalline defects do affect the device reliability. Nichia employed the LEO growth technique for their blue LDs and achieved an increase in device lifetime from a few hundred hours to an estimated 10,000 h.[37] Another major problem limiting diode performance is high specific contact resistance of the ohmic contact on the p-GaN side of the junction. Present lateral GaN lasers suffer significant IR drops due to poor p-type doping and ohmic metallization.

The nitride material growth technology that supports the optical device efforts has also proven to be compatible with the development of electronic devices. In the past several years, the electronic device development has emphasized FET structures, because this important class of devices puts smaller demands on the growth and fabrication technique compared with bipolar transistors. The rapid progress that has been made, especially in modulation-doped FETs (MODFETs), has been sufficient to show that GaN and related alloys will play a significant role in the future develop-

ment of high temperature, high power, and high frequency electronic devices.[38–41]

Figure 1.8 presents a schematic representation of a GaN–AlGaN heterostructure. Owing to the large conduction band discontinuity, the electrons diffusing from the large bandgap AlGaN into the smaller bandgap GaN form a two-dimensional (2D) electron gas (2DEG) in the triangle quantum well at the interface, which is the hallmark of a MODFET. The sheet carrier density of the 2DEG was found to be further enhanced by the strong piezoelectronic effect in GaN. Piezoelectronic coefficients in nitrides were measured to be about an order of magnitude higher than in traditional Group III–V semiconductors.[42] Theoretical simulations have predicted a high peak electron velocity of $\sim 3 \times 10^7$ cm/s [25] and an electron mobility of ~ 2000 $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ in the GaN channel at room temperature at a carrier concentration of 10^{17} cm^{-3} . [43] Gaska *et al.* [4] showed that the highest measured Hall mobility at room temperature was 2019 $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, and this increased approximately fivefold to $10,250$ $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ below 10 K for growth on 6H-SiC substrate.

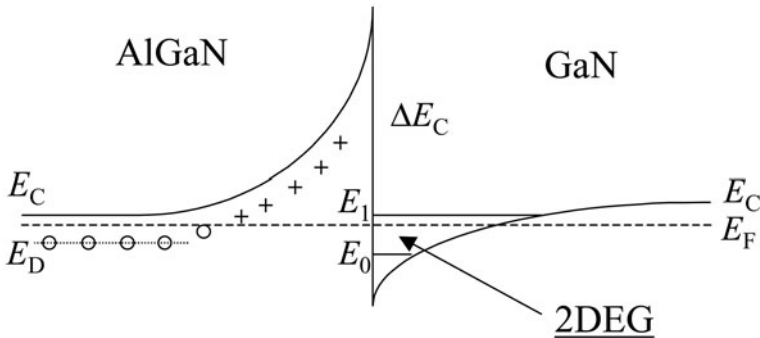


Figure 1.8. Conduction band structure of a modulation-doped structure

In 1993, Khan *et al.* [38] demonstrated the first AlGaN–GaN MODFET, with a g_m of 23 mS/mm and 2DEG mobility of 563 $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ at 300 K. They also reported the first microwave results, with f_t of 11 GHz and $f_{\max}$ of 14 GHz.[39] In the early stages, the MODFETs exhibited very low transconductances and relatively poor frequency response. This is consistent with the defect-laden nature of the early GaN and AlGaN layers. With improvements in the materials quality, the transconductance, current capacity, and drain breakdown voltage are all increased to the point that GaN-based MODFETs are now strong contenders in the arena of high power devices/amplifiers. To date, the highest power density achieved for

a $0.45 \times 125 \text{ } \mu\text{m}^2$ GaN MODFET is 6.8 W/mm at 10 GHz and associated gain of 10.65 dB.[40] The operation temperature has been pushed to 750°C by employing a thermally stable Pt–Au gate contact.[41]

The published performances of epitaxial GaN-based Metal Semiconductor Field reflect Transistor (MESFETs) demonstrate that all the required components for a MESFET-based technology are in place,[44,45] *i.e.* an appropriate high resistivity buffer–substrate combination has been developed for doped-layer epitaxial growth, FET channels can be grown with thin n^+ contact layers on which ohmic contact with adequate contact resistances have been achieved, gate metalizations which can pitchoff the channel and support a high drain bias have been demonstrated, and it has shown that both mesa etch and implant isolation can be used to define the active device area. Recently, an all implanted GaN junction FET,[46] an Si_3N_4 -gated GaN Metal Insulator Semiconductor Field reflect Transistor (MISFET),[47] and a $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_4)$ gated GaN MOSFET [48] with reasonable performance were also reported. These types of devices potentially have advantage over MESFET, especially at high temperatures due to low reverse leakage currents.

So far, there are only several reports of development of GaN-based bipolar transistors.[49,50] Basically, the device performance is limited by the difficulty in growth and processing related to the buried p-type layer and the small minority carrier lifetime. Commercialization of these devices, is still far away but their developments will follow the material improvements in the new decade, and much impetus comes from defense applications where ultrawide bandwidth and linearity are desired.

Group III–V nitrides offer a valuable combination of electrical, optical and piezoelectrical behavior, and enable the fabrication of LEDs, LDs, detectors, and transistors. In the past, the poor quality of the materials, the lack of p-type doping, and the absence of reliable processing procedures thwarted engineers and scientists from fabricating these useful devices. However, the 1990s have brought significant advances in the sophistication of growth techniques, the purity of the chemicals used for film deposition, the controlled introduction and activation of selected impurities, and progress in processing techniques. Most of the aforementioned obstacles have been sufficiently overcome, and the electronic and optical devices have been demonstrated and partially commercialized. Market projections show that GaN-based blue and green LEDs will represent the majority of the estimated \$3 billion per year GaN-based device market by 2006. In transistors, GaN can go where no other semiconductors have gone before. The future development in this area will definitely be fueled by the increasing demand for high temperature, high power applications. From materials science to device engineering, from laboratory research to com-

mercial products, III–V nitride technologies have shown a late but exciting blooming.

While further improvements in the III–V nitride materials quality can be expected to enhance device operation, further device advances will also require improved processing technology. Owing to their wide bandgap nature and chemical stability, GaN and related materials present a host of device processing challenges, including poor p-type doping (by implantation), difficulty in achieving reliable low-resistance p-ohmic contacts, high temperatures needed for implant activation, lack of efficient wet etch process, generally low dry etch rates and low selectivity over etching masks, and dry etch damage. These problems constitute a major obstacle to successful demonstration and commercialization of some GaN-based devices, such as bipolar transistors and power switches, whose performance is affected much more by the immature fabrication techniques. To fully exploit these device applications, a number of critical advances are necessary in the areas of implantation doping and isolation, high temperature thermal processing, ohmic contact to p-type material, dry etching process, and device passivation.

Ion implantation is an enabling technology for creating selective-area doping and forming high-resistance regions in device structures. For the development of ion implantation doping for advanced GaN-based electronics, it is important to understand the dopant activation process, and implantation-induced damage generation and removal. Recent studies have showed that quite good activation efficiency can be obtained by annealing at 1100°C, [30,51] but implantation damage cannot be significantly removed at this temperature. Annealing at temperatures >1300°C is suggested to fully remove the damage and further optimize the transport properties of implanted regions in GaN.[51] Since these temperatures are beyond the capability of most rapid thermal annealing systems, new annealing apparatus must be developed. Consequently, there is an urgent need to carry out detailed studies on the dopant activation, impurity redistribution, defect removal, and surface degradation at these elevated temperatures. Efficient surface protection must be developed to prevent material decomposition and N₂ loss from the GaN surfaces.

Ion implantation is also attractive for inter-device isolation and producing current guiding. Efficient compensation has been achieved in the GaN materials by using N or He implantation.[30,52] However, the isolation is not stable at high temperatures, *i.e.* typical implant damage compensation. Implantation in In-containing III–V nitrides has shown that InGaN, as used in LEDs, laser cavities, or transistor channels, is difficult to render highly resistive.[53] The defect level is usually high in the energy gap, not near midgap, as is ideal for implant isolation. There is a strong need for an un-

derstanding of the implant isolation process and mechanism in III–V nitride materials because of the emerging applications for high temperature, high power electronics based on this material system. In particular, attempts need to be made to explore thermally stable implant isolation in GaN, and significant compensation must be achieved in the In-containing nitrides.

Considerable progress in the development of contacts to GaN has been made in the past several years.[54] Nevertheless, it is necessary still to improve upon the electrical performance of these contacts, particularly to achieve low contact resistances to p-GaN, and to develop contacts with greater thermal stability, which is critical for high current density devices. It has proven challenging to obtain acceptable low specific contact resistances on p-GaN. Values $\leq 10^{-5} \Omega \cdot \text{cm}^2$ would be desirable in general for electronics, but more typical numbers are 10^{-1} – $10^{-3} \Omega \cdot \text{cm}^2$. The high contact resistances can be attributed to several factors, including: (1) The absence of a metal with a sufficiently high work function (the bandgap of GaN is 3.4 eV, and the electron affinity is 4.1 eV, but metal work functions are typically ≤ 5 eV). (2) The relatively low hole concentrations in p-GaN due to the deep ionization level of the Mg acceptor (~ 170 meV). (3) The tendency for the preferential loss of nitrogen from the GaN surface during processing, which may produce surface conversion to n-type conductivity. In order to lower the contact resistances to p-GaN further, it will be necessary to further increase p-type conductivity or to lower the barrier height of the metal contacts, perhaps by growing a more readily contacted compositionally graded semiconductor alloy on the p-GaN.

The thermal stability of the contacts is also noteworthy. Annealing at $\sim 700^\circ\text{C}$ resulted in interfacial reaction, along with serious morphological degradation of the conventional Ti-based or Ni-based contacts.[55,56] In the case of contact to p-GaN, the metalization will heat up as current flows across the interface due to the high series resistance, leading to metal migration down threading dislocations and eventual shorting of the devices. Thermally stable Schottky contacts are also required for power amplifiers and optoelectronics that operate at high temperatures, but the electrical characteristics of the metal–n-GaN diodes have been reported to suffer degradation upon exposure to temperatures as low as 300°C (Pd),[57] 400°C (Pt),[58] 575°C (Au)[59] and 600°C (Ni).[54]

Furthermore, there is a large scatter in the measured results of Schottky barrier height (SBH) and the ohmic contact resistance, suggesting that our understanding of the interface reactions, surface preparation, and non-idealities associated with the metal–GaN contacts is far from complete.

Dry etching has become the dominant patterning technique for the Group III nitrides due to the shortcomings in wet chemical etching. The

etch rates in reactive ion etch (RIE) systems are generally low.[60] High density plasma etching, *i.e.* inductively coupled plasma (ICP)[61,62] and electron cyclotron resonance (ECR)[63] etching have been developed in a variety of chlorine- and methane-based chemistries. The etch rates of GaN were reported as high as 9800 Å/min in a Cl₂-H₂-Ar mixture.[62] However, surface roughening, N depletion, and degradation in electrical and optical properties were observed. Some device etching applications, such as gate recessing for FETs and base mesa formation for Heterojunction Bipolar Transistors (HBTs), can be particularly susceptible to ion-induced damage. In order to minimize the deleterious effects of energetic ions during dry etching, it will be necessary to develop effective low-damage etching processes that utilize ion energies well below 100 eV. At this point, it is also important to determine the nature of the plasma-induced damage in GaN, and to explore the procedures for damage removal.

GaN-based amplifiers and switches are attractive for high power applications in hostile environments. Reliable edge termination and passivation processes are critical to fully exploit these types of devices. There is not much work to date in this area. In addition, as discussed earlier, thermally stable doping, isolation, and metal contacts are all key issues for these special applications.

1.3 Results and Discussion

1.3.1 Ultra-High-Temperature Activation of Implant Doping in Gallium Nitride

Ion implantation is an enabling technology for selected-area doping or isolation of advanced semiconductor devices. Implantation of donors at high doses can be used to decrease source and drain access resistance in FETs, at lower doses to create channel regions for FETs, while sequential implantation of both acceptors and donors may be used to fabricate p-n junctions. In addition, ion implantation is a suitable technological tool to explore doping, compensation effects, and redistribution properties of the potential dopant species.

The first work on implantation in GaN was performed by Pankove and Hutchby in the earlier 1970s.[64] They reported primarily on the photoluminescence properties of a large array of implanted impurities in GaN. The work was successful in identifying Mg as the shallowest acceptor found to date for GaN. In 1995, Pearton *et al.*[30] achieved electrically

active n- and p-type dopants in GaN by implantation of Si and Mg respectively. Subsequently, implanted O was also shown to be a donor and implanted Ca an acceptor in GaN.[31] Two different GaN-based device structures have been demonstrated using implant doping, namely a junction FET [46] and a planar homojunction LED.[65]

Tan *et al.*[66] have observed that low dose ($\leq 5 \times 10^{14} \text{ cm}^{-2}$) implants in GaN anneal poorly up to 1100°C , leaving a coarse network of extended defects, while high dose ($\geq 2 \times 10^{15} \text{ cm}^{-2}$) implants may lead to amorphization. Amorphous layers recrystallize in the range $800\text{--}1000^\circ\text{C}$ to form defective polycrystalline material. Quite good activation efficiencies have been obtained for n-type implanted dopants in spite of high residual damage.[30,51] It is also clear that annealing temperatures above 1300°C are desirable for optimal electrical properties in the implanted layers.[51] At these temperatures, the equilibrium N_2 pressure over GaN is very high; thus, surface protection is necessary to prevent dissociation of the GaN. The most effective and convenient approach is use of an AlN encapsulant that can be removed selectively in KOH after annealing. This technique is attractive for processing of GaN devices in a conventional fabrication-line environment, without the need for specialized high-pressure furnaces.

In this section we first introduce a novel rapid thermal processing (RTP) up to 1500°C to the GaN material system, used in conjunction with AlN cap layers. The high temperature activation characteristics of implanted Si and Group VI donors are then examined. The activation of Mg, Be and C for p-type doping has also been investigated, along with the redistribution of all these species in GaN. Finally, the effectiveness of the new RTP for removing lattice damage in implanted GaN was studied by TEM.

1.3.1.1 High-Temperature Annealing and Aluminum Nitride Encapsulation

In the development of advanced electronic devices, the technology of RTP plays a critical role at numerous points, such as implant activation of dopant species, implantation-induced damage removal, alloying of ohmic contacts, maximization of sheet resistance in implant isolation regions, *etc.* The existing commercial RTP equipment typically relies on a series of tungsten-halogen lamps as heat sources to rapidly heat up the semiconductor wafers, and only has modest temperature capacity ($<1100^\circ\text{C}$), primarily because of the point-like nature of the sources and large thermal mass of the systems. Recent interest in developing wide bandgap compound semiconductors such as SiC and GaN has pushed the processing temperature requirements to much higher values (up to 1500°C).

To realize higher temperature capacity, novel molybdenum intermetallic composite heat sources have been employed, which may be used in air at temperatures up to 1900°C. These heaters have high emissivity (up to 0.9) and allow heat-up times of the order of seconds and heat fluxes up to 100 W/cm². The ZapperTM unit relies on wafer movement (in/out of the furnace horizontally) to achieve rapid ramp-up or ramp-down rates (~50 °C /s and 25 °C /s respectively). Excellent temperature uniformity ($\leq \pm 4^\circ\text{C}$ over a 9"×6" area at 1500°C), good reproducibility can be obtained. Figure 1.9 shows the typical temperature–time profiles for annealing cycles at 1400°C and 1500°C. To examine the thermal stability of the nitrides, a variety of undoped GaN and AlN wafers were sealed in quartz ampoules under N₂ gas, and annealed in ZapperTM unit at different time–temperature combinations. The GaN layers ~ 3 μm thick were grown at ~1050°C by MOCVD using trimethylgallium and ammonia. Growth was preceded by low-temperature deposition of thin (~200 Å) AlN buffers on Al₂O₃ substrates. Some AlN layers were deposited by reactive sputtering of pure AlN targets in 300 mTorr of 20% N₂Ar at 400°C. The others were grown by metal organic MBE (MOMBE) at 750°C using dimethylamine alane and plasma-dissociated nitrogen.[67] The N₂ pressure in the quartz ampoules was ~15 psi. This negative pressure was necessary to prevent blowout of the ampoule at elevated annealing temperatures. The samples were then annealed at 1100–1500°C for a dwell time of ~10 s.

Figure 1.10 (top) shows scanning electron microscopy (SEM) micrographs of the GaN surfaces annealed at 1200–1500°C. The 1200°C annealing does not degrade the surface, and the sample retains the same appearance as the as-grown material. After 1300°C annealing, there is a high density (~10⁸ cm⁻²) of small hexagonal pits due to incongruent evaporation from the surface. The 1400°C treatment produces complete dissociation of the GaN, and only the underlying AlN buffer survives. Annealing at 1500°C also causes loss of this thin buffer layer, and a smooth exposed Al₂O₃ substrate is evident. The corresponding root-mean-square (RMS) surface roughness of these samples measured by atomic force microscopy (AFM) scans is shown in Figure 1.10 (bottom).

In sharp contrast, both the sputtered and MOMBE-grown AlN were found to survive annealing up to 1400–1500 °C. However, for the sput-

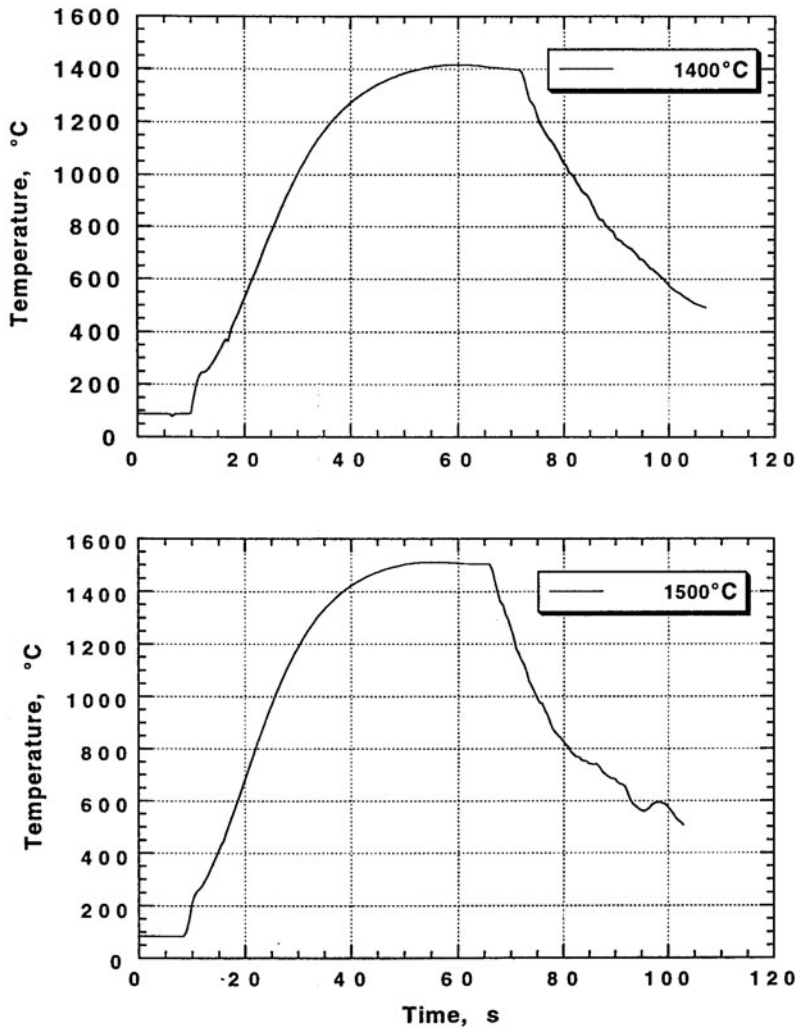


Figure 1.9. Time–temperature profiles for Zapper™ RTP annealing at 1400°C and 1500°C

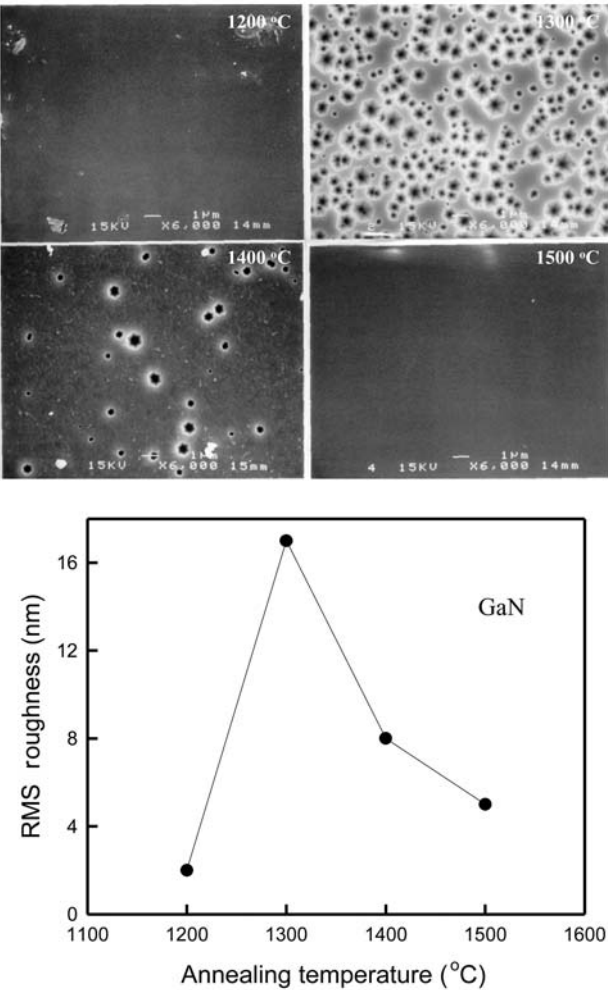


Figure 1.10. SEM micrographs (top) and RMS roughness (bottom) of GaN surfaces annealed at 1200–1500°C

tered materials, we often observed localized failure of the film (Figure 1.11 (top)), possibly due to residual gas (Ar or H₂) agglomeration to form bubbles. The surface roughness tends to go through a maximum at ~1300°C, partially due to some initial localized bubbling, followed by the film densification at temperatures ≥1400°C, as shown in Figure 1.11 (bottom). The film retains its integrity even at 1450°C, and appears to be more thermally

stable than the AlN buffer layer under the GaN (Figure 1.10). This can be attributed to the fact that the AlN was deposited at higher temperature (400°C compared with 300°C for the buffer layers) and, therefore, is denser and contains less residual entrapped gas. For the MOMBE grown films, the localized material failure was basically absent.

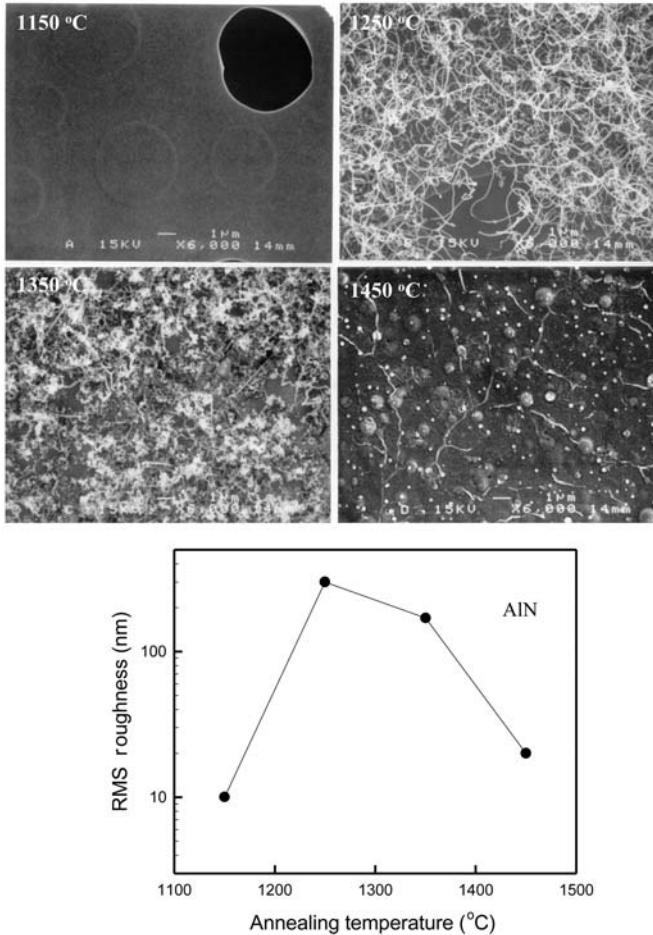


Figure 1.11. SEM micrographs (top) and RMS roughness (bottom) of AlN surfaces annealed at 1150–1450°C

There is clear evidence from previous work that temperatures above 1300°C are required to completely remove implantation damage and to achieve the optimal dopant activation in GaN. However, the above results

show that a premium is placed on prevention of loss of nitrogen or even surface dissociation under those conditions. AlN encapsulation can preserve the surface quality to 1500°C, which is quite promising for the high temperature activation processes.

1.3.1.2 *n-Type Implant Doping*

Nominally undoped ($n \approx 5 \times 10^{16} \text{ cm}^{-3}$) GaN was grown on *c*-plane Al_2O_3 substrates by MOCVD. Samples were implanted at room temperature in a non-channeling direction with 150 keV $^{28}\text{Si}^+$ ions at a dose of $5 \times 10^{15} \text{ cm}^{-2}$, 200 keV $^{32}\text{S}^+$ and 600 keV $^{128}\text{Te}^+$ ions at doses of $5 \times 10^{14} \text{ cm}^{-2}$ for *n*-type doping. The Si implant is a standard condition for producing very high *n*-type doped regions in GaN when combined with high temperature RTA. All samples were capped with $\sim 1000 \text{ \AA}$ reactively sputtered AlN, and annealed at 1200–1500 °C under a N_2 ambient in the ZapperTM furnace for a dwell time of $\sim 10 \text{ s}$. Following annealing, the AlN was removed in aqueous KOH at $\sim 80^\circ\text{C}$, and the samples were characterized. For measurement of the electrical properties, HgIn ohmic contacts were alloyed to the corners of $3 \times 3 \text{ mm}^2$ sections, and Hall effect data was recorded at 25°C in all cases.

Figure 1.12(a) shows an Arrhenius plot of sheet carrier concentration in Si^+ -implanted material. As a comparison, the electrical results for the unencapsulated samples are also shown. In these uncapped wafers, the sheet electron density increases with annealing temperature up to 1300°C , but this was the highest temperature we would obtain data due to loss of the film. By contrast, the AlN encapsulated samples show a peak in the sheet electron density and the 300 K electron mobility (Figure 1.12(b)) at 1400°C . The activation occurs with an activation energy of $\sim 5.2 \text{ eV}$, which we interpret as the average required to move the interstitial Si atom to a vacant substitutional site by short-range diffusion and to simultaneously remove compensating point defects so that the Si is electrically active. Note that both the electron density and the mobility decreases at 1500°C , indicating that the material is becoming more compensated. This behavior is fairly typical of Si implant activation in III–V materials, and is usually ascribed to self-compensation through Si site-switching, *i.e.* some of the Si_{Ga} donors move to Si_{N} sites, producing self-compensation. A peak Si activation efficiency of $\sim 90\%$ is obtained at 1400°C (with the ionization level of $\sim 30 \text{ meV}$, Si was fully ionized at room temperature), which corresponds to a peak electron concentration of $\sim 5 \times 10^{20} \text{ cm}^{-3}$. This very high doping level can enhance emission over the barrier on metal contacts de-

posited on the material and reduce contact resistances in GaN electronic devices.

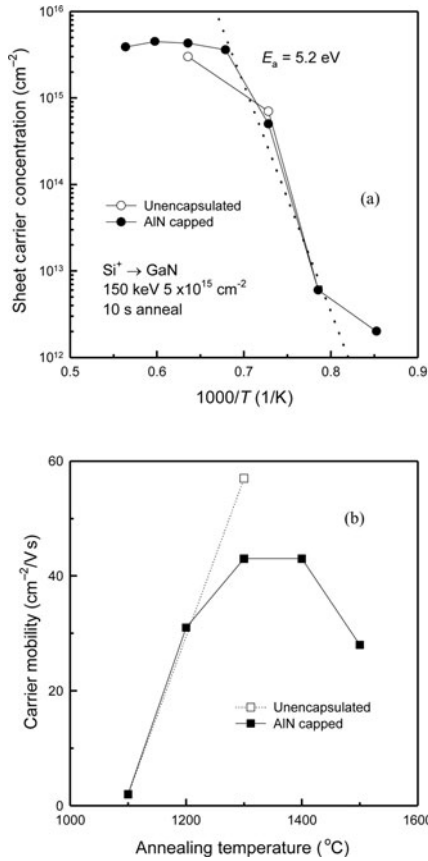


Figure 1.12. Sheet carrier concentration (a) and electron mobility (b) in Si-implanted GaN after uncapped and AlN-capped annealing

There is clear evidence from previous work that temperatures above 1300 $^{\circ}\text{C}$ are required to completely remove implantation damage and to achieve the optimal dopant activation in GaN. However, the results in Figure 1.13(a) show an Arrhenius plot of S^+ activation in GaN. The sheet carrier concentration measured at 25 $^{\circ}\text{C}$ shows an activation energy of 3.2 eV for the annealing temperature range between 1000 and 1200 $^{\circ}\text{C}$, and the physical origin of this energy is essentially same as that of Si implant activation. The sheet carrier concentration is basically saturated thereafter. The maximum sheet electron density, $\sim 7 \times 10^{13} \text{ cm}^{-2}$, corresponds to a peak

volume density of $\sim 5 \times 10^{18} \text{ cm}^{-3}$. This is well below that achieved with Si^+ implantation and annealing ($> 10^{20} \text{ cm}^{-3}$). Even though implanted Si^+ at the same dose showed evidence of site-switching and self-compensation, it still produces a higher peak doping level than the non-amphoteric donor S, which is only slightly heavier (^{32}S vs ^{28}Si). From temperature-dependent Hall measurements, we find an S^+ donor ionization level of $48 \pm 10 \text{ meV}$, so that the donors are fully ionized at room temperature.

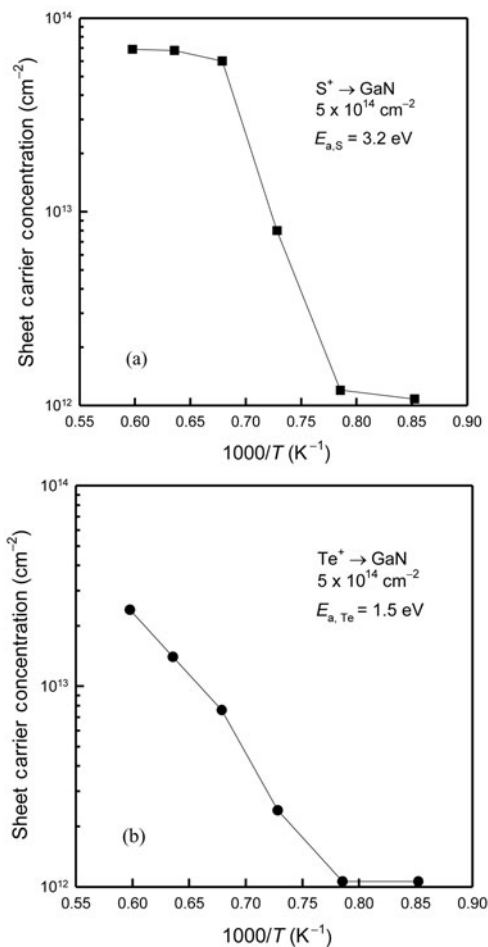


Figure 1.13. Arrhenius plots of sheet electron density in S (a) and Te (b) implanted GaN as a function of annealing temperature

Similar data are shown in Figure 1.13(b) for Te⁺ implantation. The activation starts around the same temperature as for S, but much lower sheet electron densities are obtained, the activation energy is significantly lower (1.5 eV) and the carrier concentration does not saturate, even at 1400°C. It is likely that because of the much greater atomic weight of ¹²⁸Te, even higher annealing temperatures would be required to remove all its associated lattice damage, and that the activation characteristics are still being dominated by this defect removal process. Residual lattice damage from the implantation is electrically active in all III–V semiconductors, producing either high resistance behaviors (GaAs) or residual n-type conductivity (InP, GaN). The only data available on Group VI doping in epitaxial material is from Se-doped MOCVD material, where maximum electron concentrations of 2×10^{18} – 6×10^{19} cm⁻³ were achieved. These are also below the values reported for Si-doping, and suggests that the Group VI donors do not have any advantage over Si for creation of n-type conductivity in GaN. From limited temperature-dependent Hall data, we estimate the Te ionization level to be 50 ± 20 meV.

1.3.1.3 p-Type Implant Doping

Similar GaN samples were implanted with 80 keV ⁹Be⁺, 80 keV ¹²C⁺, or 150 keV ²⁴Mg⁺ at doses of 3 – 5×10^{14} cm⁻² for p-type doping. Post-implant annealing was performed at 1000–1400°C under a N₂ ambient in the ZapperTM furnace for ~10 s in conjunction with ~1000 Å AlN encapsulation.

The effects of the annealing temperature on the sheet carrier concentrations in Mg⁺ - and C⁺ -implanted GaN are shown in Figure 1.14. There are two important features of the data: first, we did not achieve p-type conductivity with carbon; second, only ~1% of the Mg produces a hole at 25°C. Carbon has been predicted previously to have a strong self-compensation effect,[68, 69] and it has been found to produce p-type conductivity only in MOMBE where its incorporation on a N-site is favorable.[70] Based on an ionization level of ~170 meV, the hole density in Mg-doped GaN would be calculated to be ~10% of the Mg acceptor concentration when measured at 25°C. In our case we see an order of magnitude less holes than predicted. This should be related to the existing n-type carrier background in the material and perhaps to residual lattice damage, which is also n-type in GaN. At the highest annealing temperature (1400°C), the hole density falls, which could be due to Mg coming out of solution or to the creation of further compensating defects in the GaN. The results of Be implant are similar with those of C implant, *i.e.* remaining n-

type after annealing, probably also due to a strong compensation effect. This data indicates that ion implantation is not so efficient for creating p-type conductivity in state-of-the-art GaN as epitaxial growth doping.

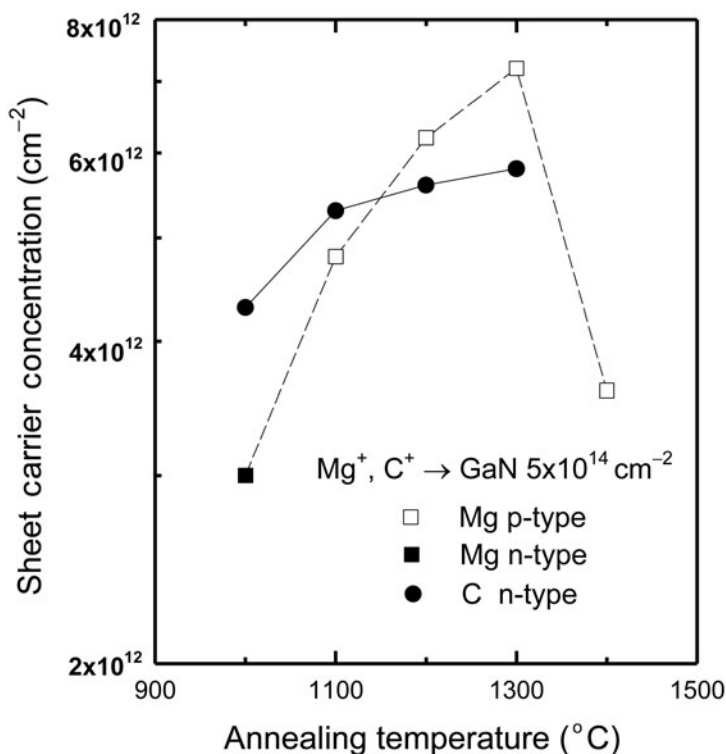


Figure 1.14. Sheet carrier concentrations in Mg^+ - and C^+ -implanted GaN as a function of annealing temperature

1.3.1.4 Dopant Redistribution

Figure 1.15 shows the calculated, as-implanted Si atomic profile and the secondary ion mass spectroscopy (SIMS) profiles of as-implanted and 1400°C annealed samples. The calculated profile does not produce a good match to the experimental profile, and some work will need to be done to obtain better stopping power data for the ions in GaN. There is little redistribution of the Si at 1400°C, with the diffusivity $\leq 10^{-13} \text{ cm}^2 \cdot \text{s}^{-1}$ calculated from the change in width at half-maximum. This result emphasizes the extremely stable nature of Si dopant in GaN even at very high processing temperatures.

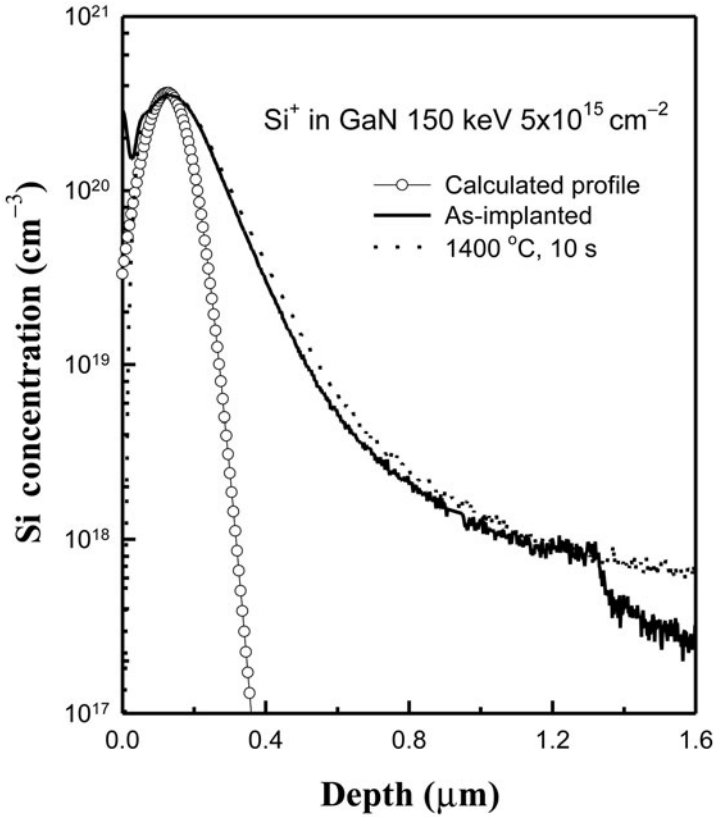


Figure 1.15. Calculated and experimentally measured (by SIMS) profiles of implanted Si (150 keV, $5 \times 10^{15} \text{ cm}^{-2}$) in GaN

Figure 1.16 (top) shows SIMS profiles before and after 1450°C annealing of implanted S in GaN. There is clearly no motion of the sulfur under these conditions and the profiles are essentially coincident. Wilson *et al.* [71] reported some redistribution of implanted S after annealing at 700–1000°C in relatively thin layers of GaN, which might have been influenced by the high crystalline defect density in the material. The samples in the present experiment are much thicker and the extended defect density will be correspondingly lower in the implanted region ($\sim 5 \times 10^8 \text{ cm}^{-2}$ compared with $\sim 10^{10} \text{ cm}^{-2}$ in the thin samples). The other Group VI donors, Se and Te, have low diffusion coefficients in all compound semiconductors (e.g. $D_{\text{Se}} = 5 \times 10^{-15} \text{ cm}^2 \cdot \text{s}^{-1}$ at 850°C in GaAs), and we find a similar result for these species implanted into GaN, as shown in Figure 1.16 (bottom).

Given the resolution of SIMS measurement (~ 200 Å under these conditions), we can obtain the diffusivity at this temperature $\leq 2 \times 10^{-13} \text{ cm}^2 \cdot \text{s}^{-1}$ using a simple $2\sqrt{Dt}$ estimation.

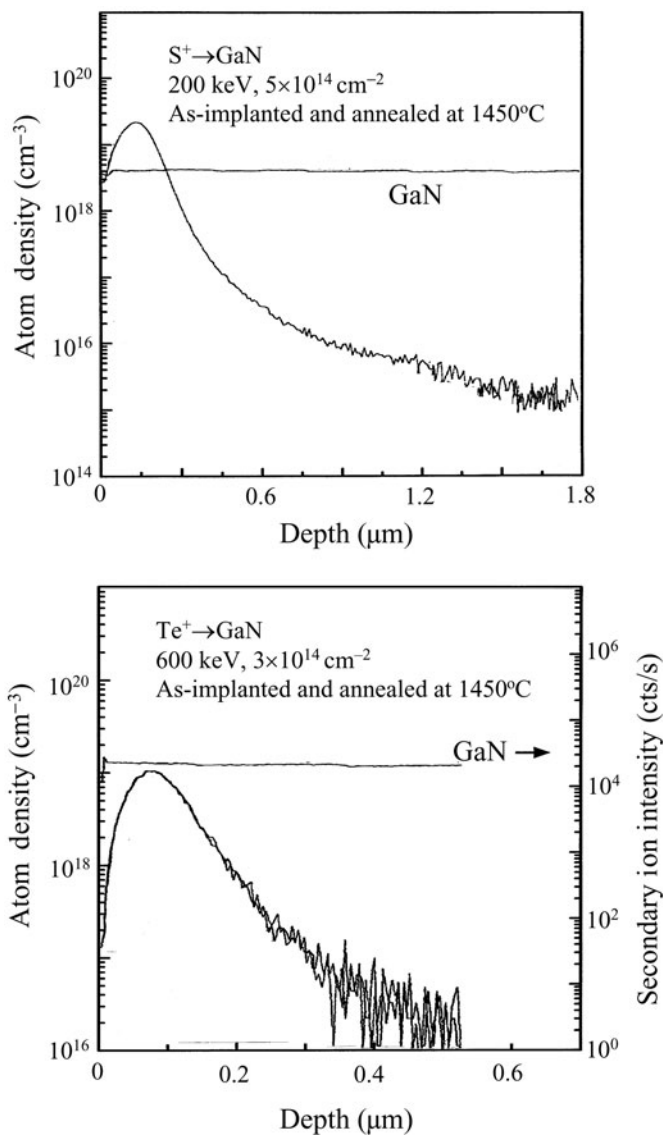


Figure 1.16. SIMS profiles of S^+ (top) and Te^+ (bottom) implanted GaN before and after annealing at 1450°C (the profiles are essentially coincident)

Figure 1.17 (top) shows the SIMS profiles of implanted Mg in GaN before and after annealing at 1450°C. Again, within the resolution of SIMS, there is no motion of the Mg. This is in sharp contrast to its behavior in GaAs,[72,73] where the rapid diffusion of the Ga-site acceptors during annealing can only be suppressed by co-implanting a Group V element to create a sufficient number of vacant sites for the initially interstitial acceptor ions to occupy upon annealing. This reduces the effective diffusivity of the acceptor and increases its electrical activation. In addition, implanted Mg in GaAs often displays out-diffusion toward the surface (in most cases up, rather than down, the concentration gradient), leading to loss of dopant into the annealing cap.[74] This has been suggested to be due to non-equilibrium levels of Ga interstitials created by the implantation process. This mechanism is clearly absent for implanted Mg in GaN.

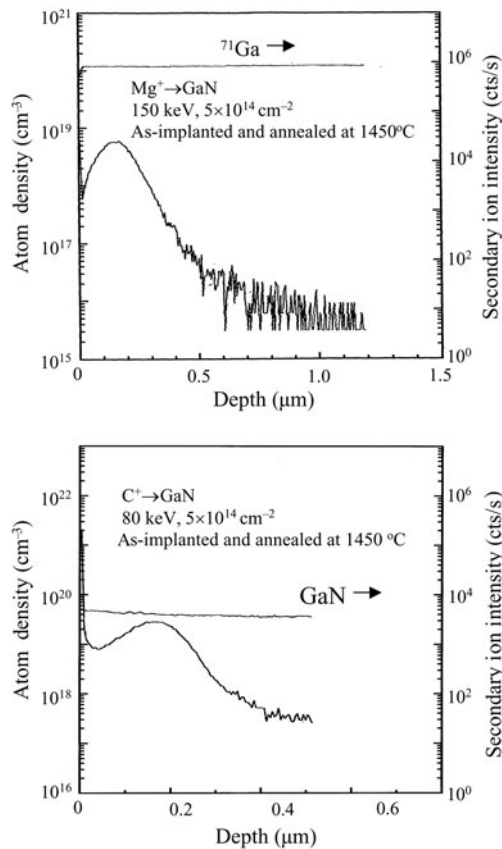


Figure 1.17. SIMS profiles of Mg⁺ (top) and C⁺ (bottom) implanted GaN before and after annealing at 1450°C (the profiles are essentially coincident)

Carbon is typically a very slow diffuser in all III–V compounds, since it strongly prefers substitutional lattice sites.[74,75] In general, carbon occupies both Ga and N sites in GaN, and the material containing high concentrations of carbon is found to be self-compensated. Figure 1.17 (bottom) shows that it is also an extremely slow diffuser when implanted into GaN, with $D_{\text{eff}} \leq 2 \times 10^{-13} \text{ cm}^2 \cdot \text{s}^{-1}$ at 1400°C .

Figure 1.18 shows a series of profiles for ^9Be before and after annealing up to 1200°C . Note that there is an initial broadening of the profile at 900°C , corresponding to an effective diffusivity of $\sim 5 \times 10^{-13} \text{ cm}^2 \cdot \text{s}^{-1}$ at this temperature. However, there is no subsequent redistribution at temperatures up to 1200°C . It appears that, in GaN, the interstitial Be undergoes a type of transient-enhanced diffusion until these excess point defects are removed by annealing, at which stage the Be is basically immobile. Implanted Be shows several types of anomalous diffusion in GaAs, including up-hill diffusion and movement in the tail of the profile, in addition to normal concentration-dependent diffusion,[76] which also result from the non-equilibrium concentrations of point defects created by the nuclear stopping process of the implanted ions.

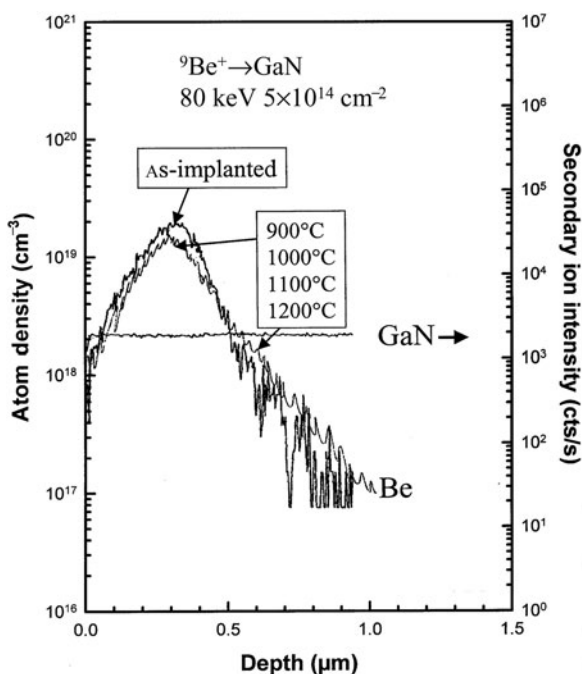


Figure 1.18. SIMS profiles of Be^+ implanted GaN before and after annealing at different temperatures

The above results show that most of the common acceptor and donor species implanted into GaN, with the exception of Be, are extremely slow diffusers at high temperatures. This bodes well for the fabrication of GaN-based power devices, such as thyristors and insulated gate bipolar transistors, that will require creation of doped well or source/drain regions by implantation. The low diffusivities of implanted dopants in GaN means that junction placement should be quite precise and there will be less problems with lateral diffusion of the source/drain regions towards the gate. In addition, these results also show the effectiveness of the AlN cap in protecting the GaN surface from dissociation, since if any of the surface was degraded during annealing, then the implant profiles would no longer overlap.

1.3.1.5 Residual Damage

Figure 1.19 shows a plan view TEM micrograph and selected-area electron diffraction pattern from an Si-implanted sample (150 keV , $5\times 10^{15}\text{ cm}^{-2}$) after annealing at 1100°C for 10 s. This is a high-dose implant of the type used for making n^+ ohmic contact regions, and represents a worst-case scenario in terms of damage removal. It also allows comparison with damage expected with other dopants such as S, Ca and Mg due to the representative mass number of Si. The sample is still single crystal as determined by the diffraction pattern, but contains a high density of extended defects ($\sim 10^{10}\text{ cm}^{-2}$). This is consistent with past reports of high backscattering yields in implanted GaN annealed at these conditions.[77] We ascribe these defects to the formation of dislocation loops in the incompletely repaired lattice.

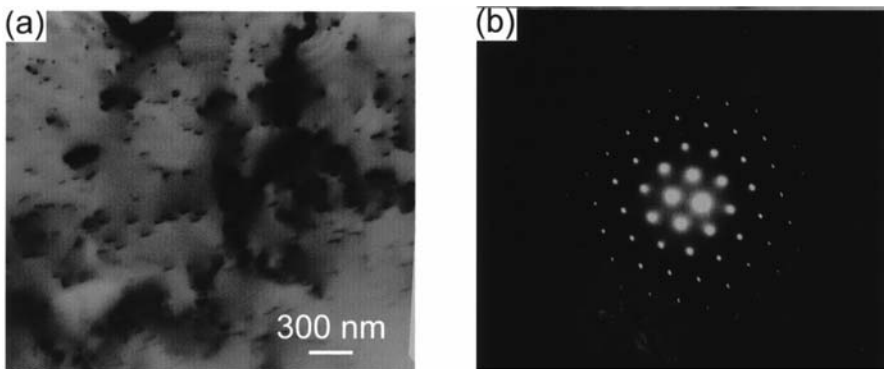


Figure 1.19. TEM plan view (a) and selected-area diffraction pattern from Si^+ -implanted GaN after 1100°C , 10 s annealing

By sharp contrast, annealing at 1400°C for 10 s brings a substantial reduction in the implant-induced defects, as shown in Figure 1.20. The sample is again single-crystal, but the only contrast in the TEM plan view is due to the lower density ($\sim 10^9 \text{ cm}^{-2}$) of threading dislocations arising from lattice mismatch in the heteroepitaxy. This appears to correlate well with the fact that the highest electron mobility and carrier density in these samples was observed for 1400°C annealing. Clearly, the ultra-high temperature annealing is required to completely remove lattice damage in GaN implanted with high doses. However, it may not be needed for the material implanted with lower dose ($\leq 5 \times 10^{13} \text{ cm}^{-2}$), where the amount of damage created is correspondingly less.

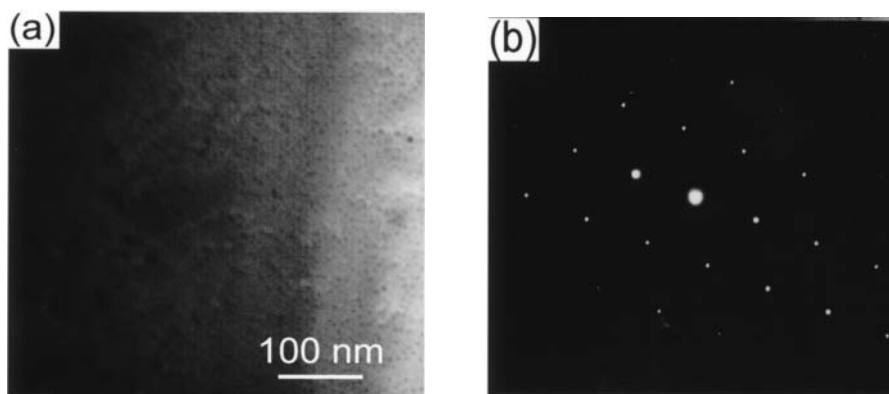


Figure 1.20. (a) TEM plan view and (b) selected-area diffraction pattern from Si^+ -implanted GaN after 1400°C, 10 s annealing

1.4 Implant Isolation

Implant isolation has been widely used in compound semiconductor devices for inter-device isolation, such as in transistor circuits, or to produce current channeling, such as in lasers. The implantation process can compensate the semiconductor layer either by a damage or chemical mechanism, maintaining a planar device morphology without the need for etched mesa isolation. For the former compensation, high resistivity is created due to introduction of midgap, damage-related levels, which trap the free

carriers in the materials. This effect is stable only to the temperature at which the damage is annealed out. For the latter case, the implanted species occupy the substitutional sites and create chemically induced deep levels in the middle of the bandgap. The compensation is thermally stable in the absence of out-diffusion or precipitation of the species. There is a strong need for an understanding of the implant isolation process in GaN because of the emerging applications for high temperature, high power electronics based on this material and its alloys.

To date in the GaN materials system there has only been an examination of damage-induced isolation. Binari *et al.*[52] investigated H^+ and He^+ isolation of n-GaN, with the material remaining compensated to over 850°C with He^+ and 400°C with H^+ . Subsequent work focused on N^+ implantation into both n- and p-type GaN, producing defect levels of 0.83 eV and 0.90 eV respectively.[30] The implantation damage was annealed out at 850°C in n-type material and 950°C in p-type material. Very effective isolation of AlGaIn heterostructure FET structures has been achieved with a combined P^+/He^+ implantation leading to sheet resistances of $\geq 10^{12} \Omega/\square$ and an activation energy of 0.71 eV for the resistivity.[78] Some work has also been reported for isolation of In-containing nitrides using O^+ , F^+ or N^+ .[53] Basically, the implantation in InN and InGaIn ternaries produced only one or two orders of magnitude increase in sheet resistance after an optimum anneal. The relatively low sheet resistance ($\sim 10^4 \Omega/\square$) achieved is not sufficient for inter-device isolation in electronic circuits.

To create chemically induced isolation, it is necessary to implant impurities with electronic levels in the GaN bandgap, and usually a minimum dose (dependent on the doping level of the sample) is required. In other compound semiconductors, species such as Fe, Cr, Ti and V have been employed, with other examples being O in AlGaAs (where Al–O complexes are thought to form)[79] and N in GaAs (C) (where C–N complexes are thought to form).[80]

In this section, multi-energy O^+ , Ti^+ , Fe^+ or Cr^+ were implanted into n- and p-type GaN to create high resistivity. The annealing temperature dependence of the sample sheet resistance was measured up to 900°C. The defect levels in the materials of both types were determined by temperature-dependent Transmission Line Method (TLM) measurements. The thermally stable, electrically active concentration of deep states produced by these species was found to be $< 7 \times 10^{17} \text{ cm}^{-3}$ in both conductivity types of GaN, with the sample resistivity approaching its original, unimplanted value by $\sim 900^\circ\text{C}$ in all cases. The defect levels created in the implanted material are within 0.5 eV of either bandedge.

1.4.1 Oxygen Implantation for Selective Area Isolation

0.3 μm thickness n- (Si-doped) or p-type (Mg-doped) GaN layers were grown on 1 μm thickness undoped GaN on (0001) sapphire substrates by radio frequency (rf) plasma activated MBE. The carrier concentration in the doped layers was $7 \times 10^{17} \text{ cm}^{-3}$ in each case. Ohmic contacts were formed in a transmission line pattern (gap spacings of 2, 4, 8, 16 and 32 μm) by e-beam evaporation and lift-off of Ti–Au (n-type) and Ni–Au (p-type) annealed at 800°C and 700°C respectively for 30 s under N_2 . The total metal thickness was 4000 Å, so that these regions could act as implanted masks. A schematic of the resultant structure is shown in Figure 1.21.

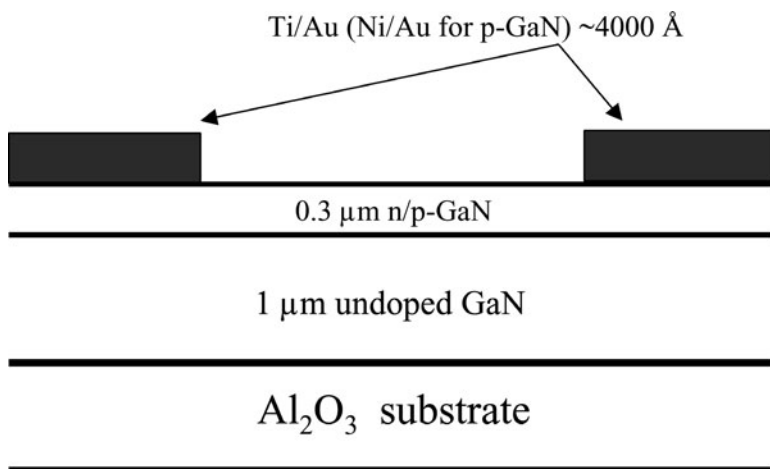


Figure. 1.21. Schematic of GaN structure for measurement of sheet resistance after ion implantation

The samples were then implanted at 25°C using multiple-energy O^+ ions at different doses: 50 keV, $1 \times 10^{14} \text{ cm}^{-2}$; 100 keV, $2 \times 10^{14} \text{ cm}^{-2}$; 200 keV, $3 \times 10^{14} \text{ cm}^{-2}$. The total dose was therefore $6 \times 10^{14} \text{ cm}^{-2}$. The sheet resistance was obtained from TLM measurements for both the as-implanted sample and those annealed at increasing temperatures to 900°C. Measurement temperatures in the range of 25–200°C were employed to determine the defect levels in the material.

In the case where the implanted species is chemically active in the GaN it is the ion profiles that are the important feature, since it is the electrically active fraction of these implanted species that determines the isolation behavior. In the case where the isolation simply results from damage-related

deep levels, then it is the profile of ion damage that is important. Figure 1.22 shows both the calculated ion profiles (top, from P-CODETM simulations) and damage profiles (bottom, from transport-of-ions-in-matter (TRIM) simulations) for the multiple-energy O⁺ implant scheme. Note that the defect density is generally overstated in these calculations due to recombination of vacancies and interstitials. In any case, the doses are below the amorphization threshold for GaN.

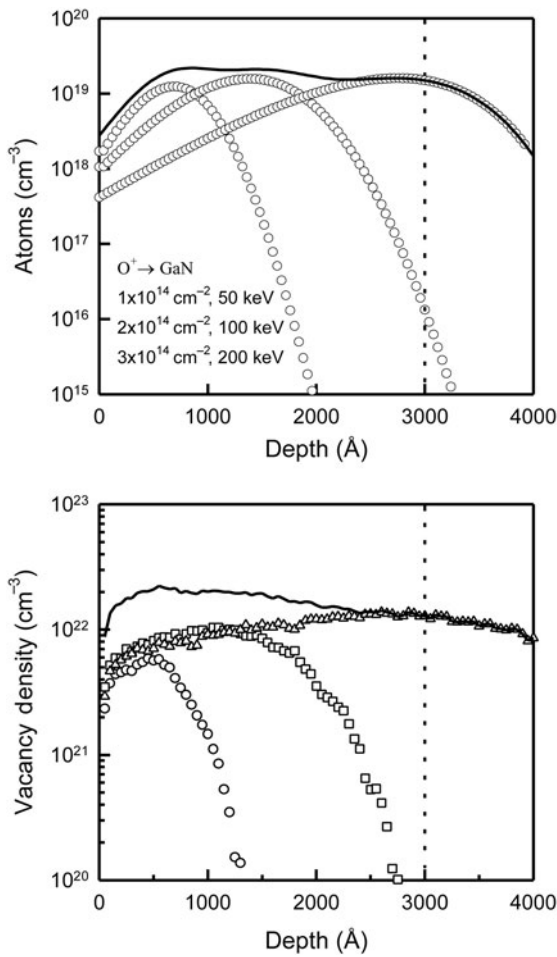


Figure 1.22. Ion (top) and damage (bottom) profiles for multiple-energy O⁺ implant sequence into GaN

Figure 1.23 (top) shows the evolution of the sheet resistance for O^+ implanted n- and p-type GaN with annealing temperature. For the n-type sample, the as-implanted sheet resistance was $4 \times 10^9 \Omega/\square$, and gradually decreased over the entire annealing temperature range. We do not believe this is a result of O-related shallow donor states because these are not activated until annealing temperatures above 1100°C . [30] By contrast, the trend in the sheet resistance in p-type GaN is typical of those observed with damage-related isolation. The as-implanted resistance is five orders of magnitude higher than that of the unimplanted material due to creation of deep traps that remove holes from the valence band. Subsequent annealing tends to further increase the sheet resistance, by reducing the probability for hopping conduction as the average distance between trap sites is increased. [81] Beyond a particular annealing temperature (600°C in this case) the trap density begins to fall below the carrier concentration and holes are returned to the valence band. This produces a decrease in sheet resistance toward the original, unimplanted values. Note that even after a 900°C anneal the sheet resistance is still two orders of magnitude above the unimplanted value. A general rule of thumb for achieving acceptable device isolation is that the implanted region should have a sheet resistance $\geq 10^7 \Omega/\square$. [82] In this implant process, sheet resistances above this value were achieved for annealing temperatures up to 600°C for n-type and 800°C for p-type.

Figure 1.23 (bottom) shows Arrhenius plots of the sheet resistance of the implanted n- and p-type GaN annealed at either 300°C (n-type) or 600°C (p-type). The annealing temperature for the p-type sample was chosen to be close to the point where the maximum in the sheet resistance occurs. The activation energies derived from these plots represent the Fermi level positions for the material at the particular annealing temperatures employed. Note that the values are far from midgap (1.7 eV for hexagonal GaN). In particular, the defects created in n-GaN are much shallower and could not produce efficient compensation in this material.

From Figure 1.22 we find that there is a region at the immediate surface ($<300 \text{ \AA}$) that receives a much lower concentration of cumulative damage, simply because the projected range of the 50 keV O^+ ions is $\sim 400 \text{ \AA}$. Inadequate coverage of this near-surface region is a common problem in implant isolation processes, because conventional implant systems typically have minimum operating voltages in the 20–30 keV range. One solution to this problem is to implant through a surface layer, which acts to move the projected range of the lowest energy implant closer to the semiconductor surface. Titanium is a good choice, since it can be readily removed after the implant step with HF solutions. To achieve good compensation in the near-surface region, $\sim 500 \text{ \AA}$ Ti was deposited on top of the GaN. The

implantation performed under same conditions through this Ti overlayer produced a maximum sheet resistance 50 times higher than that without the implant overlayer. The subsequent evolution of the resistance with annealing temperature was similar.

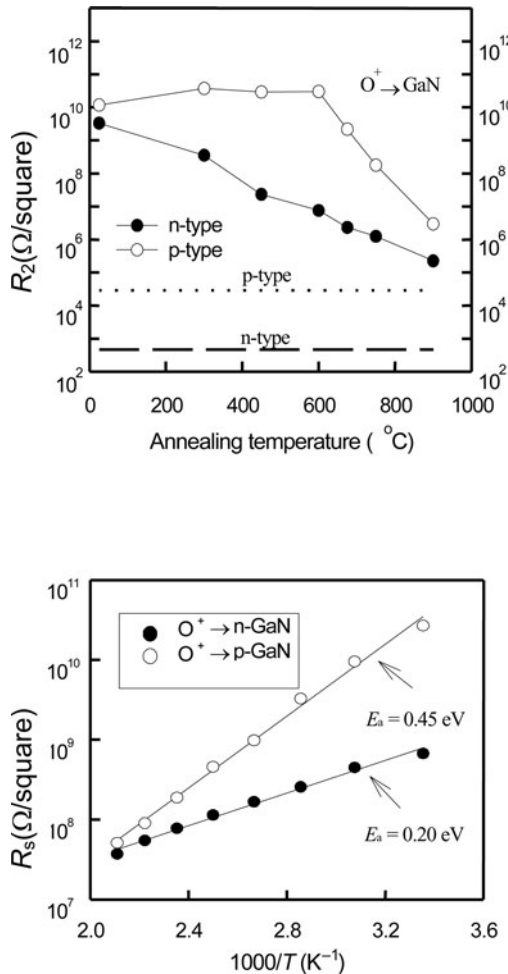


Figure 1.23. Evolution of sheet resistance of n- and p-type GaN with annealing temperature after O^+ implantation (top), and Arrhenius plots of sheet resistance after either 300°C (n-type) or 600°C (p-type) annealing (bottom)

1.4.2 Creation of High-Resistivity Gallium Nitride by Ti, Iron, and Chromium Implantation

For a better understanding of the implant isolation mechanism in GaN, Ti^+ , Fe^+ and Cr^+ were implanted into n- and p-type samples at 100 keV (10^{14} cm^{-2}), 300 keV ($2 \times 10^{14} \text{ cm}^{-2}$) and 500 keV ($3 \times 10^{14} \text{ cm}^{-2}$). The wafer structure is the same as shown in Figure 1.21. The doses and energies were chosen to create an average ion concentration of $\sim 10^{19} \text{ cm}^{-3}$ throughout the $0.3 \mu\text{m}$ thickness doped GaN layers. Both the ion and vacancy profiles for the Fe^+ implants are shown at the top and bottom, respectively, of Figure 1.24. It is very clear that implanting with these heavier ions produced much more cumulative damage than the O^+ implantation.

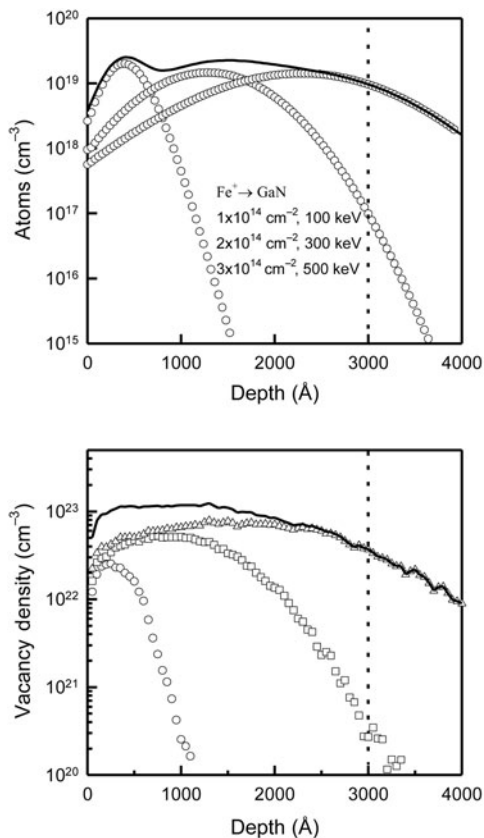


Figure 1.24. Ion (top) and damage (bottom) profiles for multiple-energy Fe^+ implant sequence into GaN

Figure 1.25 shows the annealing temperature dependence of sheet resistance for Cr^+ (top) and Fe^+ (bottom). The as-implanted resistance is six to seven orders of magnitude higher than that of the unimplanted material. The sheet resistances peak at some particular annealing temperatures (500–600°C). There is a significant improvement in the maximum R_s in the n-type sample compared with the O^+ implantation described earlier ($\sim 10^{12}$ vs $\sim 10^{10} \Omega/\square$), because of the higher vacancy and interstitial concentrations created. The trends in the sheet resistance show that the isolations are all typically damage related. If Cr or Fe produced electrically active deep states related to their chemical nature in the bandgap with concentrations greater than the carrier density in the material, then the sheet resistance would remain high for annealing temperatures above 600°C. For these two impurities it is clear that the electrically active concentration of deep states is $< 7 \times 10^{17} \text{ cm}^{-3}$, otherwise all the carriers would remain trapped beyond an annealing temperature of $\sim 600^\circ\text{C}$.

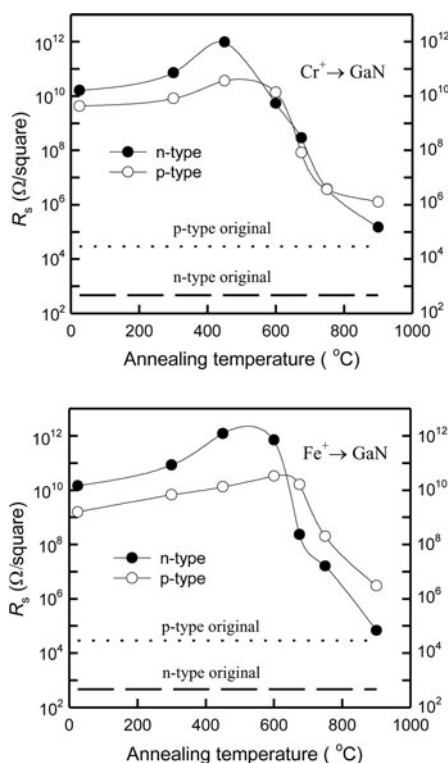


Figure 1.25. Evolution of sheet resistance of GaN with annealing temperature after Cr^+ (top) and Fe^+ (bottom) implantation

Figure 1.26 shows the sheet resistance of Cr^+ - (top) or Fe^+ implanted (bottom) n- and p-type GaN annealed at either 450°C (n-type) or 600°C (p-type), as a function of the measurement temperature. The activation energies derived from these plots are 0.49 eV and 0.45 eV in n-type and p-type GaN respectively, which give rough estimates of the positions of the Fermi levels. These implant-induced defect states, although relatively shallow, efficiently compensated the wide bandgap material.

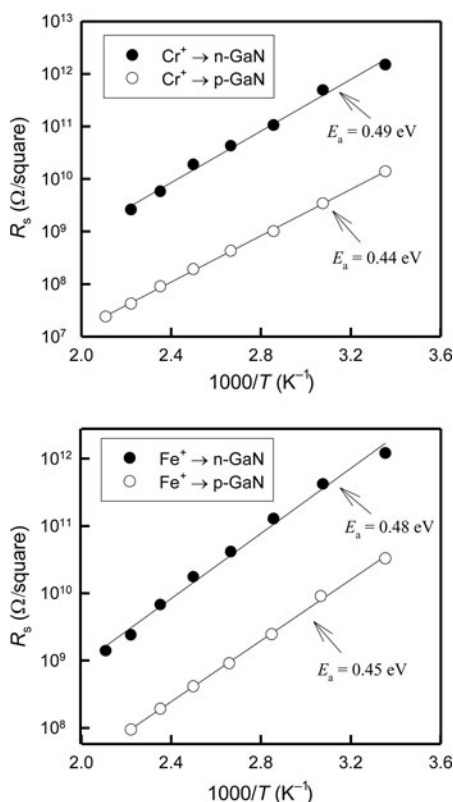


Figure. 1.26. Arrhenius plots of sheet resistance in Cr^+ - (top) and Fe^+ -implanted (bottom) n- and p-type GaN after annealing at either 450°C (n-type) or 600°C (p-type)

Similar results were obtained from Ti^+ implantation in both n- and p-GaN. Within the experimental error ($\pm 0.04 \text{ eV}$), the activation energies are the same for all these implants for both conductivity types. This again suggests that the defect states created are damage related and not chemical in nature. Note that the activation energy obtained with O^+ implant into n-GaN is much smaller. This difference may be related to the lower damage

density with O^+ implantation. The defect states in the gap are most likely due to point defect-complexes of vacancies and/or interstitials, and the exact microstructures of these complexes and their resultant energy levels are expected to be very dependent on damage density and creation rate.[83] This might also explain the differences reported in the literature for the activation energies obtained with different implant species.

Figure 1.27 shows a schematic of the energy level positions found in this work for Ti-, Cr-, Fe- and O-implanted p- and n-type GaN annealed to produce the maximum sheet resistance. Although the levels are not at midgap, as is ideal for optimum compensation, they are sufficiently deep to produce high resistivity material ($\sim 10^{12} \Omega/\square$ in n-GaN and $\sim 10^{10} \Omega/\square$ in p-GaN). In GaN contaminated with transition metal impurities, non-phonon-assisted photoluminescence lines attributed to Fe^{3+} at 1.3 eV and Ti^{2+} at 1.19 eV have been reported,[84] but to date there are no electrical measurements.

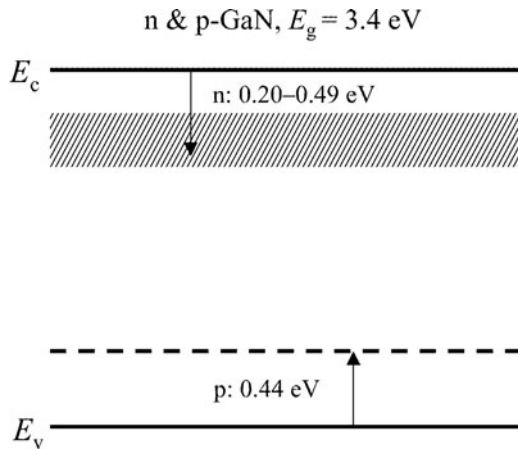


Figure 1.27. Schematic representation of the positions in the energy band gap of defect levels created by O, Fe, Cr and Ti implantation into GaN

1.5 Electrical Contacts to Gallium Nitride

GaN is attractive for optical devices with blue or ultraviolet wavelengths, as well as for high power and high temperature electronics. Critical to the success of these devices, however, are the ohmic contacts, and in some cases Schottky contacts to the semiconductors. In general, making low-

resistance ohmic contact is difficult for wide bandgap materials, especially for p-type GaN due to the difficulty in doping. This creates a large voltage drop across the GaN–metal interface for ohmic contacts, which leads to poor device performance and reliability. For most devices, ohmic contacts with resistances lower than $10^{-5} \Omega\cdot\text{cm}^2$ are desired.

Ti-based contacts with contact resistances of 10^{-6} – $10^{-5} \Omega\cdot\text{cm}^2$ have been demonstrated on n-type GaN.[23,55,85] These contacts are found to take advantages of the formation of a thin interfacial TiN layer (which is refractory), exhibit metallic conductivity, and possess a low work function (<4 eV).[86] However, no satisfying ohmic contact to p-type GaN has been developed so far. In the search for improved contact characteristics, a wide variety of metallizations have been investigated on p-GaN besides the standard Ni–Au,[18,56,87,88] including Ni,[87,88] Au,[87,89] Pd,[87] Pd–Au,[90] Pt–Au,[91] Au–Mg–Au,[92] and Pd–Pt–Au.[91] Typically, metals with a large work function, such as Ni, Pd or Pt, are in direct contact with the GaN, and the structure is annealed at 400–750°C. This produces contact resistances in the 10^{-1} – $10^{-3} \Omega\cdot\text{cm}^2$ range. Reports have also appeared on the effect of annealing in O_2 ambient in reducing contact resistance (r_c),[93] oxidation of Ni–Au metallization and its role in improving contact quality,[94] the role of surface treatments in determining contact quality [95,96], and the use of Ta–Ti contacts with low, but unstable contact resistances.[97]

Another approach to achieve low-resistance contact is through semiconductor bandgap engineering. Schubert *et al.*[98] proposed the use of Al–GaN–GaN superlattices as a technique to increase the average hole concentration. The periodic oscillation of the valence band edge is superimposed with the oscillation generated by the piezoelectric field; this significantly reduces the Mg acceptor ionization energy and, therefore, increases the hole concentration. Ti–Pt–Au contacts with specific contact resistance of $\sim 4 \times 10^{-4} \Omega\cdot\text{cm}^2$ have been achieved on this structure.[99] However, this scheme may not easily be applied to real devices, since the free carriers are separated into parallel sheets.

The Schottky contacts to n-GaN for a variety of elemental metals have been studied extensively. The reported SBH increases monotonically, but does not scale proportionally with metal work function, with a considerable amount of scatter in the experimental results for a given metal. The I – V ideality factor is usually significantly larger than unity, and the measured values of the Richardson constant A^{**} are quite small.[54] This non-ideal behavior of GaN Schottky diodes appears to result from the presence of several transport mechanisms, and to materials and process factors such as defects present in these films, the effectiveness of surface cleans prior to

metal deposition, local stoichiometry variations, and variations in surface roughness.

There is not much information on Schottky contacts on p-GaN. Measurement of the barrier height is very difficult, due to the general difficulty in growing high quality p-type material, and the lack of low resistance ohmic contact. The experimental values from conventional I - V and C - V methods are usually inconsistent, but also appear to be affected by the work function of the metals.[87]

One of the important issues in making high quality Schottky and ohmic contacts to GaN is the surface cleanliness. The ideal metal-semiconductor interface should be oxide- and defect-free, atomically smooth, uniform, and thermally stable, with the metal epitaxial. Analysis by spectroscopic ellipsometry showed that >30 Å of overlayer consisting organic and inorganic, and native oxide is present on air-exposed GaN.[90] *In situ* treatments, such as N-ion sputtering, were reported to remove the oxide layer on the GaN surface without significant modification of the N-to-Ga atomic ratio.[87:101] For practical contacts, the samples are treated with various acidic or basic solutions before deposition of metal layers. It was found that HCl-based solution is more effective in removing oxides and leaves less oxygen residue, but HF is more effective in removing carbon and hydrocarbon contamination.[102] These *ex situ* treatments can remove a significant part of the surface overlayer, but cannot produce atomically clean surfaces. The residual oxide layer is expected to act as a barrier to current flow through the metal-GaN interface and, therefore, has a profound influence on the electrical characteristics of contacts to GaN.

The thermal stability of metal-GaN contacts is also critically important for practical device operation (especially power electronics). The thermal limits of most of the metal-GaN combinations are between 300°C and 600°C.[54] At higher temperatures, severe degradation in contact morphology is observed, usually resulting from the formation of new interfacial phases, such as metal gallides.

In this section, as a first step to explore the improved ohmic contact to p-GaN, the effects of $(\text{NH}_4)_2\text{S}$ treatment of the GaN surface on the electrical properties were studied. Reductions in SBH by ~ 0.2 eV were observed. This reduction in SBH was ascribed to removal of the native oxide of thickness 1–2 nm that was present after conventional cleaning, and formed an interfacial insulating layer at the metal-GaN interface. In the second part, the thermal stability of W and WSi contacts on n- and p-type GaN was examined. Specific contact resistances in the range $10^{-5} \Omega \cdot \text{cm}^2$ were obtained for W on high-dose Si-implanted GaN, while true ohmic characteristics could only be achieved at elevated temperatures for contacts on p-GaN.

1.5.1 Effects of Interfacial Oxides on Schottky Contact

Three different types of samples were employed with n-type doping of either $8 \times 10^{16} \text{ cm}^{-3}$ or 10^{18} cm^{-3} , or p-type doping (hole concentration) of 10^{17} cm^{-3} . These GaN layers were 1–3 μm thick and were grown on *c*-plane Al_2O_3 substrates by rf plasma-assisted MBE. Each of the samples was treated in one of two different ways. The first involved a conventional cleaning process that involved sequential rinsing in acetone, isopropyl alcohol and deionized water prior to lithography for defining the contact areas. After lithography, the samples were rinsed 60 s in 30% HCl (25°C) and 30 s in buffered HF to remove the native oxide and then immediately loaded into the e-beam evaporator. The second cleaning process was the same as the first, but the last step was a 20 min boil in $(\text{NH}_4)_2\text{S}$. This solution does not affect the photoresist mask. The $(\text{NH}_4)_2\text{S}$ solution is effective in removing native oxide and prevention of immediate reoxidation, since a Ga–S monolayer is formed on the surface. This should be far less of a hindrance to current flow than the presence of a much thicker native oxide. The samples had Ti–Al or Ni–Au for ohmic contacts, each annealed at 750°C for 30 s to produce low r_c . The Pt (400 Å)–Au (1500 Å) rectifying contacts were e-beam deposited with diameters 50–200 μm . The effective barrier heights were obtained from the forward current–voltage (*I*–*V*) characteristics, according to the equation (see Equation (1.1)).

$$J = A^{**} T^2 \exp\left(-\frac{\phi_b}{kT}\right) \left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \quad (1.1)$$

where A^{**} is $26.4 \text{ A}\cdot\text{cm}^{-2}\cdot\text{K}^{-2}$ for n-GaN and $96.1 \text{ A}\cdot\text{cm}^{-2}\cdot\text{K}^{-2}$ for p-GaN and *J* is current density, ϕ_b is barrier height.

Figure 1.28 shows forward (top) and reverse (bottom) *I*–*V* characteristics from the n^+ GaN diodes, either with or without the $(\text{NH}_4)_2\text{S}$ treatment prior to Schottky contact deposition. There are several key points in this data. First, the forward current increases as a result of the $(\text{NH}_4)_2\text{S}$ treatment due to a decrease in barrier height from 0.81 eV on the control diode to 0.58 eV on the treated diode. Second, in the linear region of the forward characteristics, the scaling of current with contact diameter is much greater than a power of two. This suggests that there is a non-uniform concentration of defects, which are generation–recombination centers. Finally, the reverse leakage current is also increased by the $(\text{NH}_4)_2\text{S}$ treatment.

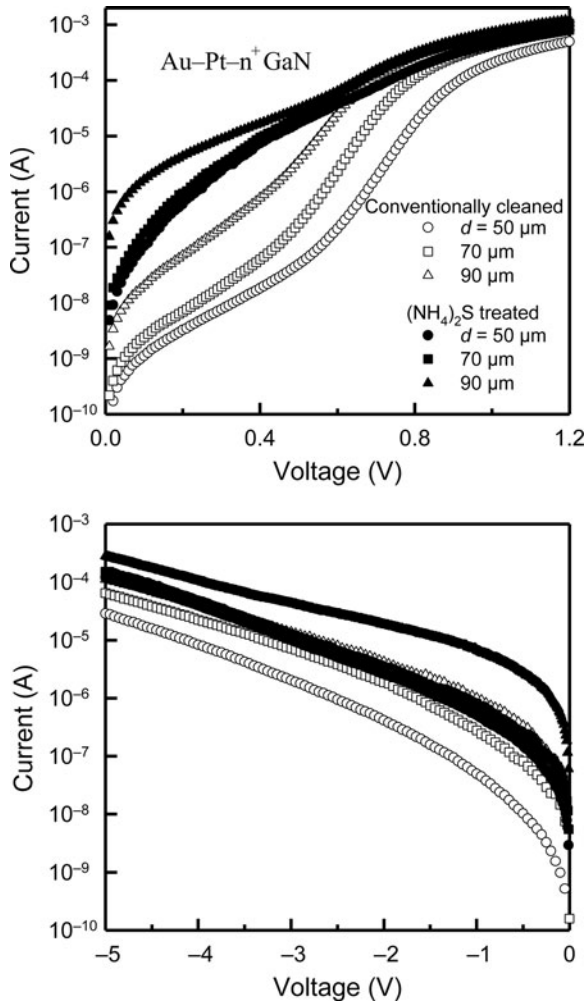


Figure 1.28. Forward (top) and reverse (bottom) I-V characteristics from AuPt-n⁺-GaN diodes of different diameters, either cleaned in a conventional fashion prior to metal deposition or with an additional (NH₄)₂S treatment

Similar data are shown in Figure 1.29 for the n-GaN diodes, at two different rectifying contact diameters. The average barrier height decreased from ~0.99 eV on the control diodes to ~0.83 eV on the (NH₄)₂S-treated samples. Both the forward and reverse currents increased as a result of the (NH₄)₂S step.

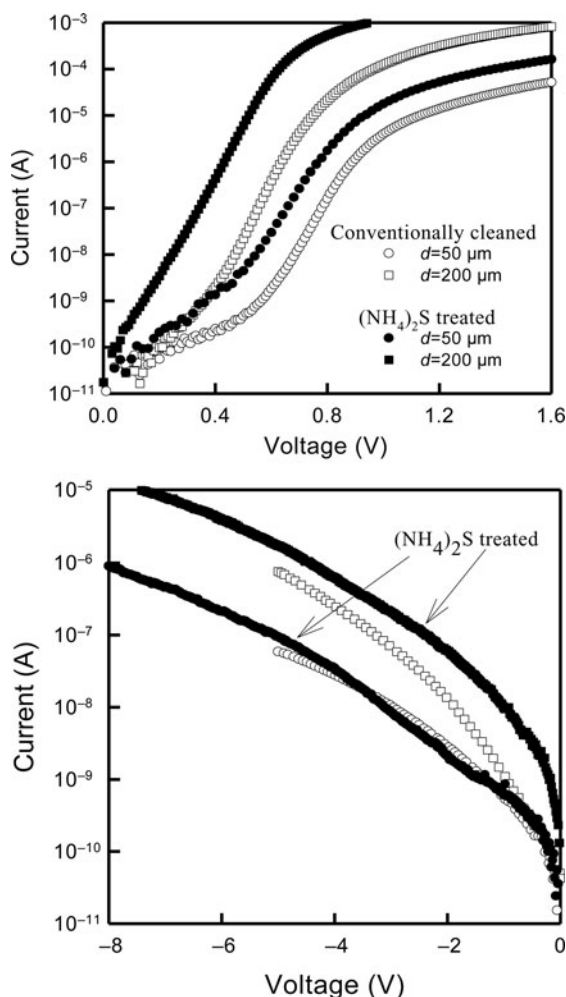


Figure 1.29. Forward (top) and reverse (bottom) I-V characteristics from AuPt-n⁻GaN diodes of different diameters, either cleaned in a conventional fashion prior to metal deposition or with an additional $(\text{NH}_4)_2\text{S}$ treatment

Figure 1.30 shows I-V characteristics from the p-GaN diodes. These structures showed high currents due to the difficulty in forming high barriers to p-GaN. The control diodes showed average barrier heights of 0.49 eV, which was slightly reduced to 0.47 eV as a result of the $(\text{NH}_4)_2\text{S}$ treatment. In these diodes, the low bias current scaled with contact diameter, indicating that surface leakage is important. We did not passivate the perimeters of the devices in this work.

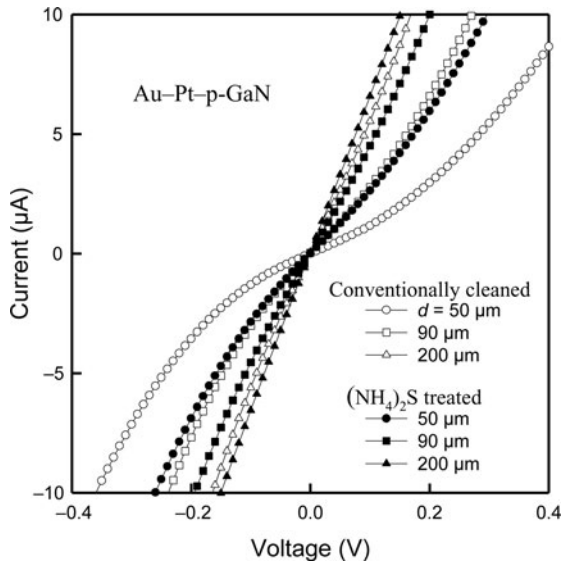


Figure 1.30. I–V characteristics from AuPt–p–GaN diodes of different diameters, either cleaned in a conventional fashion prior to metal deposition or with an additional $(\text{NH}_4)_2\text{S}$ treatment

Table 1.2 shows a compilation of the barrier heights and ideality factors for the n^+ , n and p diodes. The clear effect of the boiling $(\text{NH}_4)_2\text{S}$ exposure is to decrease ϕ_b , suggesting that it could be promising for fabrication of high quality ohmic contacts on GaN. $(\text{NH}_4)_2\text{S}$ solution was also employed to treat completed GaN mesa Schottky diodes. Figure 1.31 shows the I–V characteristics from the control and the passivated devices. Both the forward and reverse current densities increase slightly after the treatment. This probably can be ascribed to the same reason as described earlier, *i.e.* $(\text{NH}_4)_2\text{S}$ passivation reduced the barrier height, and the leakage current on the periphery increased. The forward section of the I–V characteristics shows only a slight improvement in ideality factor, and little change in this parameter is also shown in Table 1.2. Note that the $2kT$ leakage current in a diode of this type has contributions from both the bulk space-charge region and the mesa surface, and that sulfide passivation would only affect the latter. The fact that the diode ideality factors did not improve suggests that the problem for the conventional III–V compound semiconductors, *i.e.* high density of surface states, is absent for GaN, and $(\text{NH}_4)_2\text{S}$ does not passivate the surface of GaN electronically, as it does for the GaAs or InP surfaces. This is consistent with the fact that no Fermi level pinning has been observed on the GaN surface. However, we generally got ideality factors much larger than unity, which indicates high dislocation densities

and high compensation levels in the current state of GaN materials. Particularly for diodes fabricated on MBE-grown wafers, high leakage currents were typically observed, due to the relatively low epi thickness of this growth method.

Table 1.2. Summary of electrical data for test diodes

Sample	n		ϕ_b (eV)	
	Conventionally cleaned	(NH ₄) ₂ S treated	Conventionally cleaned	(NH ₄) ₂ S treated
AuPt–n ⁺ -GaN	1.6–1.8	1.8–1.9	0.81	0.58
AuPt–n-GaN	1.4–1.6	1.3–1.8	0.99	0.83
AuPt–p-GaN	~2	~2	0.49	0.47

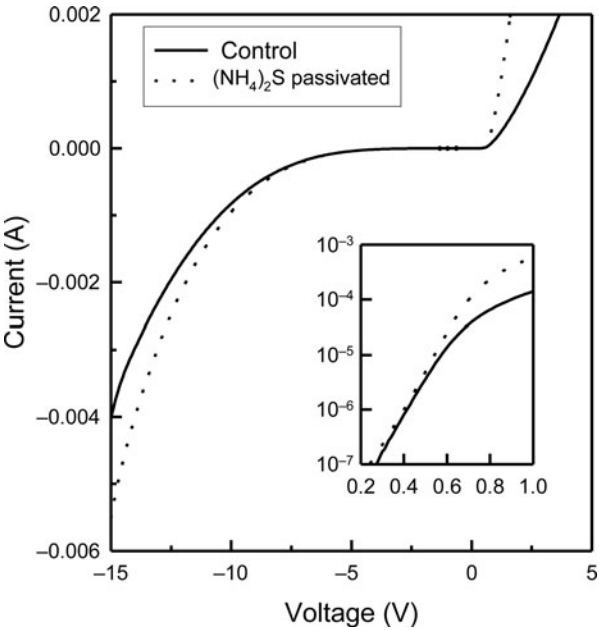


Figure.1.31. I–V characteristics from complete GaN mesa diodes before and after (NH₄)₂S treatment

1.5.2 Interfacial Insulator Model

A contamination layer such as a thin oxide at the metal–semiconductor interface usually behaves as an insulator, and provides energy barrier for carrier injection. It is assumed that the thickness and the mean tunneling barrier height of this thin oxide layer are δ and χ respectively. According to quantum mechanics, the transmission coefficient of an electron with energy E through this barrier is given by

$$T \approx \exp\left\{-\frac{2}{\hbar} \int_0^\delta (2m)^{1/2} [\chi - E]^{1/2} dx\right\} = \exp\left[-\frac{2}{\hbar} (2m)^{1/2} (\chi - E)^{1/2} \delta\right] \quad (1.2)$$

where m is the tunneling effective mass. Therefore, the current density across the interface can be expressed as (the zero of electron energy is chosen as the conduction band edge at the semiconductor surface)

$$J = \frac{qm_t}{2\pi^2 \hbar^3} \exp\left[-\frac{2}{\hbar} (2m\chi)^{1/2} \delta\right] \int_0^\infty \int_0^\infty (f_s - f_m) dE_t dE_x \quad (1.3)$$

where E_x and E_t are the electron energy components normal and parallel to the Schottky barrier; f_s and f_m are the Fermi-Dirac distribution functions for electron states in the semiconductor and metal respectively; and m_t is the effective mass component in the semiconductor transverse to the barrier. In the nondegenerate case, the current density for forward biases $V > 3kT/q$ is given by

$$J = A^{**} T^2 \exp\left[-\frac{2}{\hbar} (2m\chi)^{1/2} \delta\right] \exp(-q\phi_{b0}/kT) \exp(qV/nkT) \quad (1.4)$$

The effective SBH ϕ_b can be obtained from

$$\phi_b = \phi_{b0} + \Delta\phi \quad (1.5)$$

where ϕ_{b0} is the barrier height without the interfacial layer and $\Delta\phi$ is the additional barrier due to the oxide. The parameter $\Delta\phi$ is given by $2kT/\hbar(2m\chi)^{1/2} \delta$. The χ value for the oxide on GaN is calculated to be ~ 0.2 eV using the free electron mass.[87] In this work we typically observed $\Delta\phi$ to be 0.16–0.23 eV for Pt–Au on n-GaN, which yields an estimate for the oxide layer thickness of 1–2 nm left on the GaN surface after conventional cleaning. Previous work on the effect of different surface treatments

on the r_c of ohmic contacts on p-GaN has shown that wet chemical solutions that remove the native oxide improve the contact resistance. For example, solutions of 1.3 HNO₃:HCl were found to produce r_c values of $4.1 \times 10^{-4} \Omega \cdot \text{cm}^2$ for Pd–Au ohmic contacts on p-GaN, whereas untreated samples had values two orders of magnitude larger.[95] Similarly, the use of buffered HF and boiling (NH₄)₂S, followed by a final dip in buffered HF prior to metal deposition, was able to lower r_c by three orders of magnitude relative to untreated diodes.[103] The oxide can also be removed by annealing the contact metal at elevated temperatures. Ishikawa *et al.*[87] observed that, for Ni–GaN or Ta–GaN contacts, Ni or Ta diffused into the contamination layer after annealing at 500°C, and grew epitaxially on the GaN surface. However, Au and Pd did not react efficiently with the oxide layer. Our work suggests that the conventional *ex situ* surface treatments using HCl and HF cannot completely remove the native oxide on GaN. This oxide has a strong influence on the contact characteristics on both n- and p-type GaN, and appears to be responsible for some of the wide spread in contact properties reported in the literature.

Figure 1.32 shows the band diagrams for metal–n- or n⁺-GaN structures either with an interfacial oxide (top) or after boiling in (NH₄)₂S to remove this oxide (bottom). In the case of n-GaN, the dominant current conduction mechanism probably remains as thermionic field emission (albeit with low barrier height), while for n⁺-GaN there may also be a contribution from field emission. Alternative explanations for the increased current in (NH₄)₂S-treated samples would be an increase in contact area due to surface roughening. However, AFM measurements showed no significant change in the RMS surface roughness in our samples.

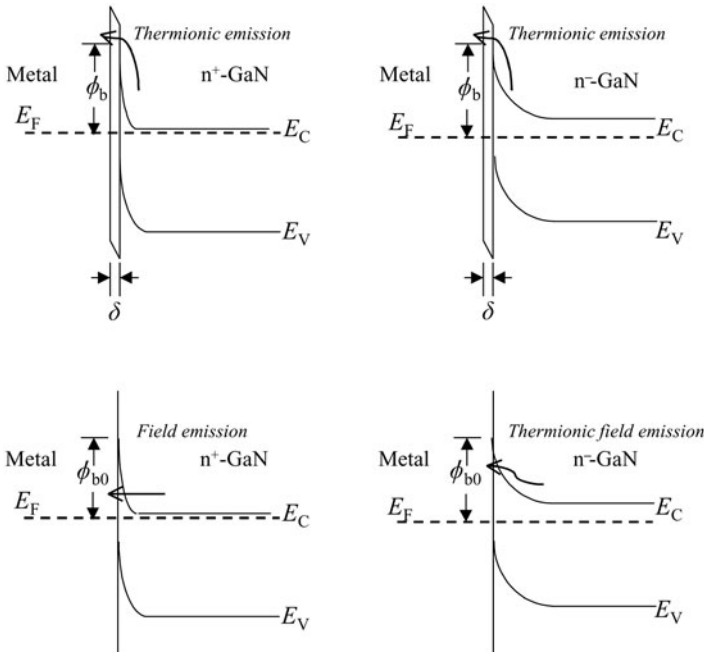


Figure 1.32. Energy band diagrams at the interface of n^+ -GaN–metal and n^- -GaN–metal with or without an interfacial oxide layer

1.5.3 Thermally Stable Tungsten-Based Ohmic Contact

Undoped GaN layers $\sim 3 \mu\text{m}$ thickness were grown on Al_2O_3 by MOCVD. These samples were implanted with 150 keV Si^+ ions at a dose of $5 \times 10^{15} \text{ cm}^{-2}$ and annealed with AlN caps in place to 1400°C for 10 s. W or $\text{WSi}_{0.45}$ layers $\sim 1000 \text{ \AA}$ thickness were deposited using an MRC501 sputtering system. The sample position was biased at 90 V with respect to the Ar discharge. Prior to sputtering, the surface contamination was removed by a rinse in HCl and buffered HF solutions. Transmission line patterns were defined by dry etching the exposed metal with SF_6 –Ar, and forming mesas around the contact pads using BCl_3/N_2 dry etching to confine the current flow. The samples were annealed for 60 sn at 500 – 1100°C under flowing N_2 .

The Si implantation followed by high-temperature activation yielded a peak n-type doping concentration of $\sim 5 \times 10^{20} \text{ cm}^{-3}$. For as-deposited metal contacts on this highly doped layer, tunneling current dominates the

total current. The specific contact resistance is roughly determined by the tunneling mechanism. Figure 1.33 shows the annealing temperature dependence of r_c for W contacts on Si-implanted GaN. The specific contact resistance improves with annealing up to $\sim 950^\circ\text{C}$, and degrades at high temperatures. Cole *et al.*[104] observed the formation of the $\beta\text{-W}_2\text{N}$ phase at the W–GaN interface at annealing temperatures between 600 and 1000°C , as demonstrated by the x-ray results in Figure 1.34. The as-deposited sample displays a well-oriented (110) W film overlaying a well-oriented (002) GaN epilayer. The samples annealed at 800°C and 1000°C exhibit well-developed face cubic $\beta\text{-W}_2\text{N}$ phase, as indicated by diffraction peaks from, the (111) in the x-ray results in Figure 1.34. The as-deposited sample displays a well-oriented (110) W film overlaying a well-oriented (002) GaN epilayer. The onset of the formation of this thin compound was first detected after annealing at 600°C . Annealing at 1000°C caused this phase to disorder, as reflected by the broadening of the W_2N (111) as well as the disappearance of the other W_2N peaks. The $\beta\text{-W}_2\text{N}$ phase was no longer stable and subsequently transformed into the defect structure of W–N after annealing at higher temperatures.

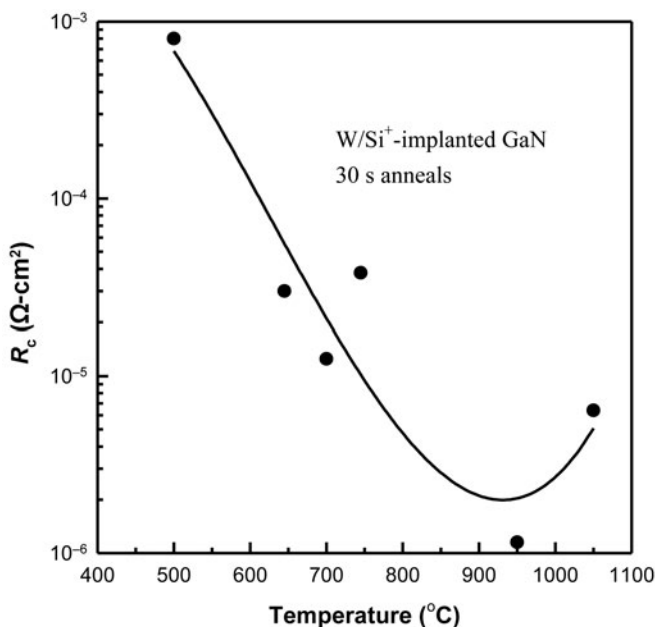


Figure 1.33. Specific contact resistance for W on Si^+ -implanted GaN, as a function of post-metallization annealing temperature

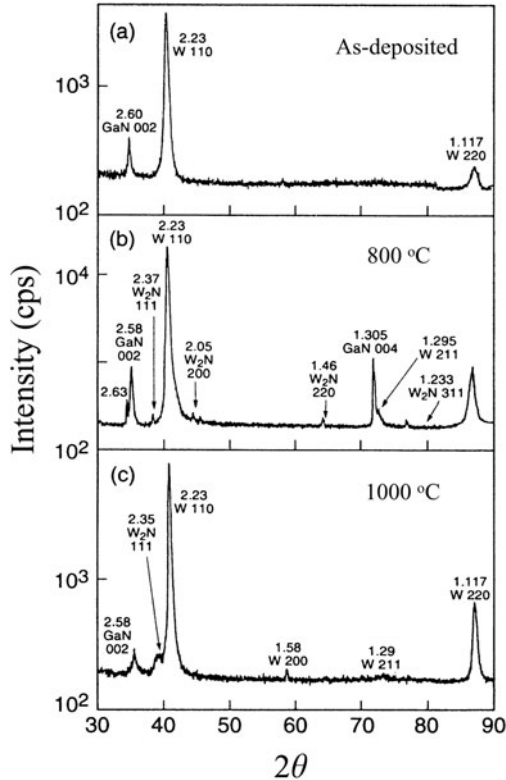


Figure 1.34. The x-ray diffraction results for the (a) as-deposited, (b) 800°C annealed, (c) 1000°C annealed W on n⁺-GaN samples

The formation of the β -W₂N phase paralleled the low specific contact resistance, and is very likely to be critical for achieving the low resistance W ohmic contacts on GaN. If the N needed to form this interfacial compound has out-diffused from the GaN without decomposing the original structure, then there would exist an accumulation of N vacancies near the GaN surface, which act as donors. Thus, the surface GaN would be highly n-type and the carrier tunneling is enhanced. Another possibility is that the N out-diffusion aids in the formation of a Ga-enriched highly conductive layer at the GaN surface, and results in a lower barrier height.

The near-surface GaN crystal quality is of particular importance, and could directly influence the uniformity and stability of the W contacts. TEM results showed that the defect-laden regions were directly associated with contact spiking into the GaN epilayer, which in turn inhibited the formation and development of the β -W₂N interfacial phase with its associated smooth metal–semiconductor interface.[105] Protrusion of the metal-



1.5.4 Behavior of Tungsten and Tungsten Silicide Contacts on p-Gallium Nitride

The 1 μm thickness GaN layers were grown on Al_2O_3 substrates by MBE using solid Ga and rf-activated N_2 from a plasma source. The Mg acceptor concentration was 10^{18} cm^{-3} . Cathodoluminescence revealed a strong peak at 383–385 nm, with very little deep-level emission. W or $\text{WSi}_{0.45}$ layers $\sim 1000 \text{ \AA}$ thickness were deposited using an MRC501 sputtering system using an Ar discharge and an acceleration voltage of 90 V. Prior to sputtering, the samples were cleaned in HCl and buffered HF solutions. TLM patterns were defined by dry etching the exposed metal with SF_6 -Ar, and

forming mesas around the contact pads using $\text{BCl}_3\text{-N}_2$ dry etching to confine the current flow. For comparison $\text{Au}(1000 \text{ \AA})\text{-Ni}(500 \text{ \AA})$ was deposited by e-beam evaporation, defined by lift-off and mesas formed by dry etching. The samples were annealed for 1 min at temperatures from 400–1100°C under a flowing N_2 ambient.

Figure 1.36 shows I–V characteristics for WSi, W and Ni–Au metallization on p-GaN, as a function of post-deposition annealing temperature. It is clear that annealing at low temperatures improves the intimate contact between the metals and GaN, and hence, the contact quality. However, even at the optimum annealing temperatures for each metal scheme (700°C for Ni–Au and W; 800°C for WSi_x) there is not true ohmic behavior, and the contacts are better described as leaky Schottky diodes. At annealing temperatures above these optimum conditions, the contact characteristics worsen and become more rectifying. Note that the formation of the W_2N phase at these temperatures could result in a decrease in hole concentration at the GaN surface, and degrade the contact properties.

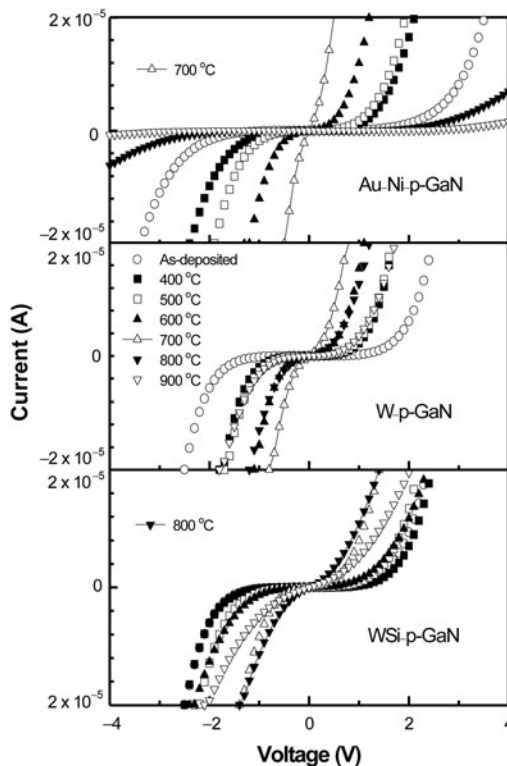


Figure 1.36. Annealing temperature dependence of I–V characteristics of WSi, W and Ni–Au contacts on p-GaN (60 s anneal times)

It is instructive to examine the contact morphology for different annealing temperatures. Figure 1.37 shows SEM micrographs of Ni–Au after annealing at 400°C (top left) and 700°C (top right), and of W after annealing at 400°C (bottom left) and 900°C (bottom right). In the former case the Ni–Au becomes strongly islanded, as reported by Venugopalan *et al.* [106], due to dissociation of the GaN by the reaction with the Ni.[56] The rate of the reaction becomes increasingly rapid above ~600°C, and in our contacts a 5 min anneal at 700°C produced extremely poor results both from an electrical and structural view point. The reacted nature of the Ni–Au contact will definitely be a problem in electronic devices such as heterojunction bipolar transistors or junction FETs, where the contact size is much smaller than in photonic devices, and need to be uniform for large numbers of devices. By sharp contrast, both the W and WSi did not show any loss of dimensional stability or surface morphology degradation even at >900°C. In addition, there is not a strong dependence of the electrical characteristics on annealing time, as shown in Figure 1.38. There is little change in the contact properties for 30 s–2 min, and contacts become slightly more rectifying for longer times, indicating that the interfacial reaction is very limited. In conjunction with the low defect density material grown by epitaxial overgrowth, the use of WSi and W metallization should prove useful in improving the thermal stability of p-ohmic contacts on GaN.

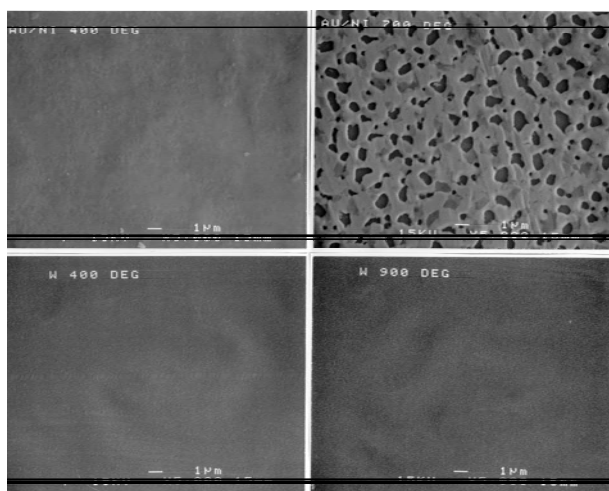


Figure 1.37. SEM micrographs of Ni–Au contacts on p-GaN after 60 s anneals at 400°C (top left) and 700°C (top right), and W contacts after annealing at 400°C (bottom left) and 900°C (bottom right)

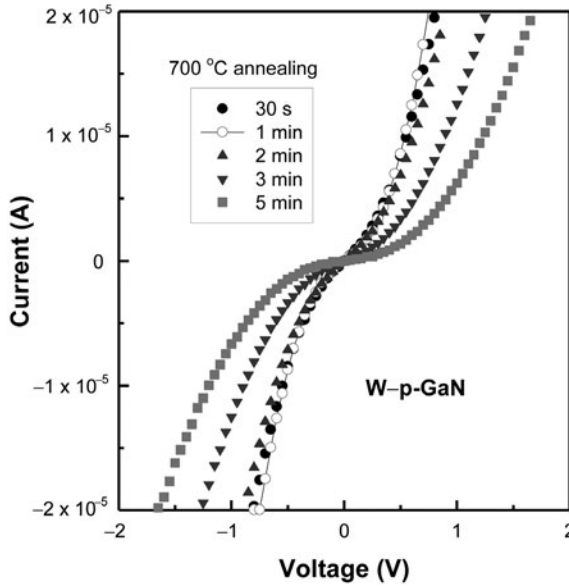


Figure 1.38. Annealing time dependence at 700°C of I–V characteristics from W contacts on p-GaN

From Fermi-Dirac statistics we can calculate the Fermi level position E_F for p-GaN containing 10^{18} acceptors as a function of absolute temperature T

$$N_A \frac{1}{1 + 2 \exp[(E_a - E_F)/kT]} = N_V \exp(-(E_F - E_V)/kT) \quad (1.6)$$

where N_A is the acceptor concentration, $E_a = 171$ meV for Mg in GaN and N_V is the valence band density of states. Using this relation, we calculated the ionization efficiency for Mg as a function of sample temperature, as shown in Figure 1.39. At 25°C, only ~10% of the Mg is ionized, whereas the efficiency increases to ~57% at 300°C. Given the acceptor concentration in our films, this means the hole density rises from $\sim 10^{17} \text{ cm}^{-3}$ at 25°C to $\sim 5.7 \times 10^{17} \text{ cm}^{-3}$ at 300°C. Past investigations have shown a combination of thermionic emission and thermionic field emission as the dominant conduction mechanisms in contacts to p-GaN.[91,107] At elevated operating temperatures, the hole density in the material increases rapidly, leading to a decrease in material sheet resistance. Concurrently, there should be more

efficient thermionic emission and tunneling of holes across the metal-GaN barrier, leading to a decrease in specific contact resistance.

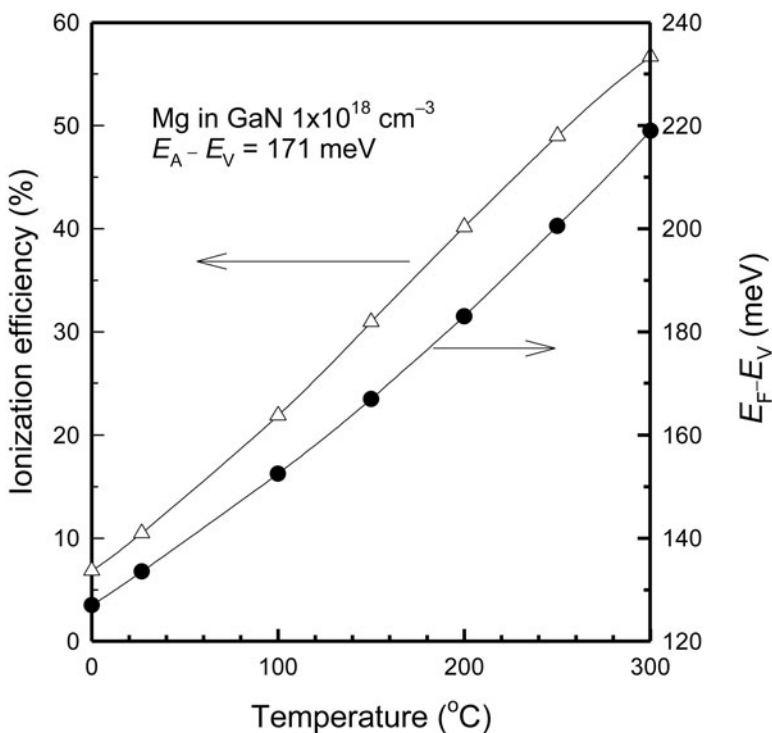


Figure 1.39. Ionization efficiency of Mg acceptors in GaN, and Fermi level position for GaN doped with 10^{18} cm^{-3} Mg acceptors as a function of temperature

Figure 1.40 shows I–V characteristics from the three different metallization schemes on p-GaN, as a function of measurement temperature. At 250°C the Ni–Au is truly ohmic, whereas the W and WSi_x have linear characteristics at 300°C. Table 1.3 shows the r_c values at 300°C are $9.2 \times 10^{-2} \Omega\text{-cm}^2$ (Ni–Au), $6.8 \times 10^{-1} \Omega\text{-cm}^2$ (W) and $2.6 \times 10^{-2} \Omega\text{-cm}^2$ (WSi). The substrate sheet resistance decreases with increasing temperature, indicating that the increased hole concentration plays a major role in decreasing r_c . Whilst device operation at elevated temperatures clearly would improve the p-contact resistance, it remains to be seen how much of a trade-off this entails in terms of degraded reliability.

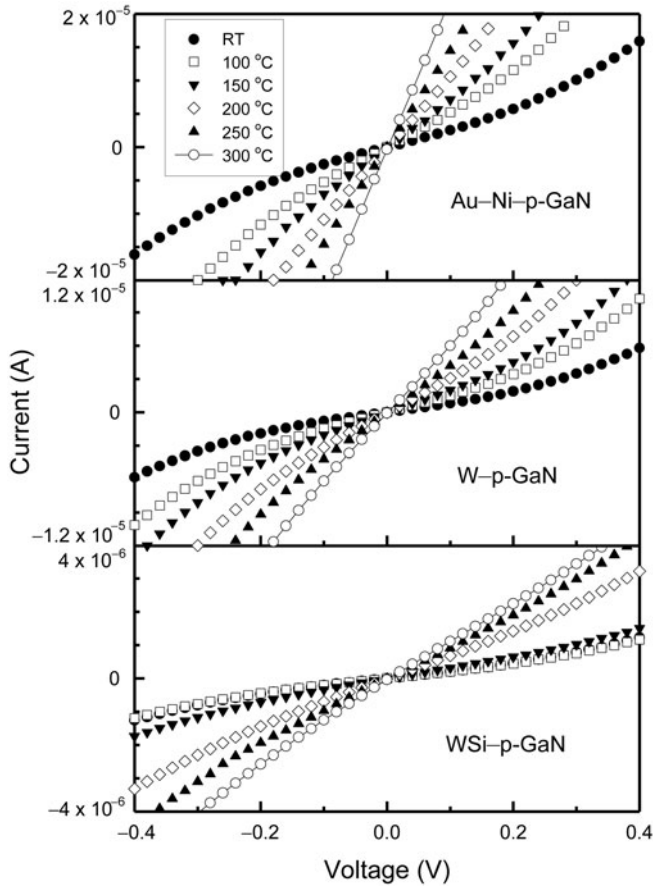


Figure 1.40. Measurement temperature dependence of I–V characteristics of Ni–Au, W and WSi contacts on p-GaN

Table 1.3. Temperature-dependent contact data for p-GaN

Contact	Measurement temperature (°C)	Specific contact resistance ($\Omega \text{ cm}^2$)	Contact resistivity ($\Omega \text{ mm}$)	Sheet resistance ($\Omega/$)
Ni–Au	200	0.125	415.7	13900
Ni–Au	250	0.121	319.5	8470
Ni–Au	300	0.092	205.9	4600
W	300	0.682	758.4	–

1.6 Dry Etch Damage in Gallium Nitride

Dry etching has proven an effective technique for the formation of mesas in GaN devices. However, exposure to the energetic ions may result in significant damage, which often degrades the material properties and device performance. The ICP technique uses lower ion energies than RIE, and thus in general has lower damage levels as a result. At high source powers, however, ion flux incidence on the surface is so high that substantial damage can be detected to depths of a few hundred angstroms. Plasma-induced damage to GaN may take several forms, all of which lead to changes in its electrical and optical properties, as follows ion-induced creation of lattice defects, which generally behave as deep-level states and thus produce compensation, trapping or recombination in the material. Owing to channeling of the low energy ions that strike the sample, and rapid diffusion of the defects created, the effects can be measured as deep as 1000 Å from the surface, even though the projected range of the ions is only ≤ 10 Å.

1. Unintentional passivation of dopants by atomic hydrogen. The hydrogen may be a specific component of the plasma chemistry, or may be unintentionally present from residual water vapor in the chamber or from sources such as photoresist mask erosion. The effect of the hydrogen deactivation of the dopants is a strong function of substrate temperature, but may occur to depths of several thousand angstroms.
2. Creation of non-stoichiometric surfaces through preferential loss of one of the lattice elements. This can occur because of strong differences in the volatility of the respective etch products, leading to enrichment of the less volatile species, or by preferential sputtering of the lighter lattice element if there is a strong physical component to the etch mechanism. Typical depths of this non-stoichiometry are < 100 Å.
3. Deposition of polymeric film from plasma chemistries involving CH_x radicals, or from reaction of photoresist masks with Cl_2 -based plasma.

In GaN-based photonic devices, the constraints placed on dry etching are minimal. Usually, these structures are heavily doped and etch depths are comparatively large, and thus are fairly resistant to damage. Moreover, the etch proceeds to an n^+ -GaN layer, onto which an ohmic contact is subsequently deposited. Preferential loss of N_2 from the near-surface region during the etch step is actually beneficial in this case because it leads to increased n-type doping levels, and hence lower contact resis-

tances.[85,100,108,109] By sharp contrast, in electronic devices such as HBTs or Bipolar Junction Transistors (BJTs), the etching requirements are much more demanding. Low-damage processes are required to form mesas for the base and collector contacts without increasing recombination in the base-emitter junction or surface leakage in the base-collector junction.

To date, much less is known about the electrical effects of dry etch damage and its subsequent removal by chemical treatment or annealing in the GaN system than for other compound semiconductors. Most past work in this area has focused on n-type material. The sheet resistances of GaN, InGaN, InAlN and InN samples were found to increase in proportion to ion flux and ion energy in an ECR Ar plasma.[110,111] Ren *et al.*[112] examined the effect of ECR $\text{BCl}_3\text{-N}_2$ and $\text{CH}_4\text{-H}_2$ plasmas on the electrical performance of InAlN and GaN channel FET. They found that hydrogen passivation of the Si doping in the channel may occur if H_2 is a part of the plasma chemistry and that preferential loss of N_2 degraded the rectifying properties of Schottky contacts deposited on plasma-exposed surfaces. Saotome *et al.*[113] found pure Cl_2 plasma treatment decreased near band-edge (Photo luminescence) intensity of the GaN samples by a factor of approximately five through introduction of non-radiative levels, whereas subsequent photo-assisted wet etching restored this to about half of the original value.

There is very little information available on the electrical effects of plasma damage in p-type GaN. Shul *et al.*[114] reported that the sheet resistance of p-GaN increased upon exposure to pure ICP Ar discharge. The increases were almost linearly dependent on ion energy, but weakly dependent on ion flux.

In this section, we studied systematically the effects of ICP N_2 , H_2 , Ar or $\text{Cl}_2\text{-Ar}$ discharge exposure under various conditions on the properties of n- and p-GaN Schottky diodes. The choice of these plasma chemistries enabled us to differentiate between ion mass effects and the role of physical versus chemical components of the etching. The depth and thermal stability of the damage have been determined. Wet etching and thermal annealing were employed to restore the electrical properties of the damaged materials.

1.6.1 Plasma Damage in n-Gallium Nitride

The layer structure and contact metals are shown schematically in Figure 1.41. The GaN was grown by rf plasma-assisted MBE on *c*-plane Al_2O_3 substrates. The Ti-Au ohmic contacts were patterned by lift-off and annealed at 750°C , producing contact resistances in the $10^{-4} \Omega\text{-cm}^{-2}$ region.

Samples were exposed to either pure N_2 or H_2 discharges in a Plasma-Therm 790 ICP system at a fixed pressure of 5 mTorr. The gases were injected into the ICP source at a flow rate of 15 standard cubic centimeters per minute (sccm). The experimentally varied parameters were source power (300–1000 W) and rf chuck power (40–250 W), which control ion flux and ion energy respectively. The Pt–Au Schottky metallization was then deposited through a stencil mask by e-beam evaporation. I–V characteristics were recorded on an HP4145A parameter analyzer, and the reverse breakdown voltage V_B was defined as the voltage at which the leakage current was 5×10^{-3} A. We found in all cases that plasma exposure caused significant increases in forward and reverse currents, with ideality factors increasing from typical values of 1.4 to 1.7 on control samples to >2 . For this reason, we were unable to extract meaningful values of either ideality factor or barrier height.

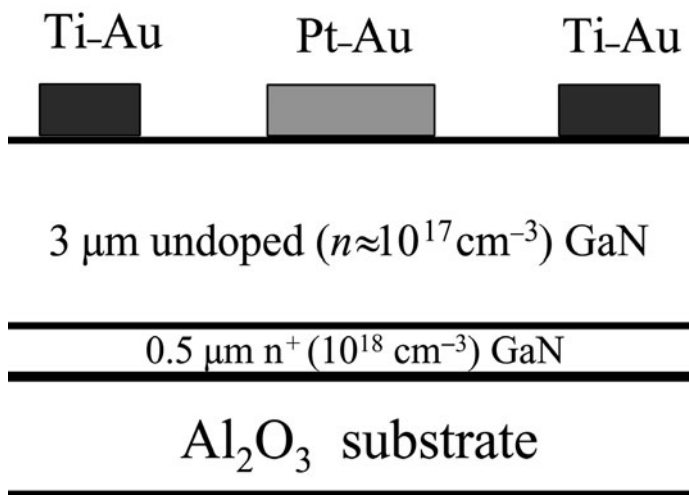


Figure 1.41. Schematic of GaN Schottky diode structure

Figure 1.42 shows a series of I–V characteristics from the GaN diodes fabricated on samples exposed to either H_2 or N_2 discharges at different source powers. It is clear that N_2 plasma exposure creates more degradation of the diode characteristics than does H_2 exposure. This implicates the ion mass ($^{28}N_2^+$, $^2H_2^+$ for the main positive ion species) as being more important in influencing the electrical properties of the GaN surface than a chemical effect, since H_2 would be likely to preferentially remove nitrogen from the GaN as NH_3 .

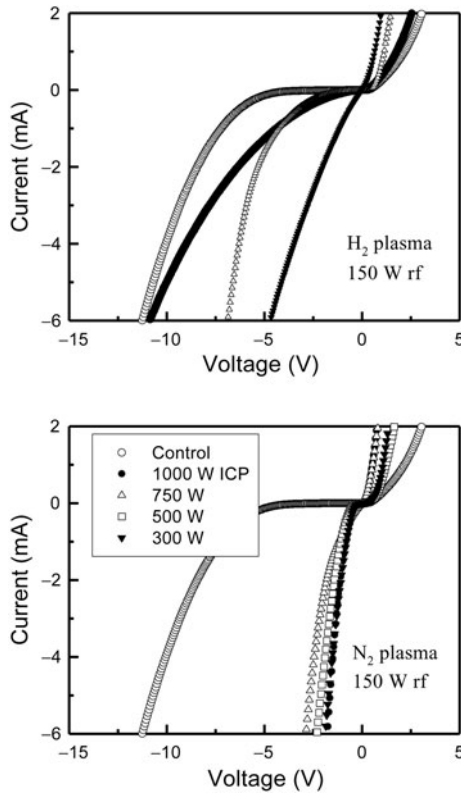


Figure 1.42. I–V characteristics from GaN diodes before and after H_2 (top) and N_2 (bottom) plasma exposure (150 W rf chuck power, 5 mTorr) at different ICP powers

The variations of V_B of the diodes with the source power during plasma exposure are shown in Figure 1.43. For any exposure to the N_2 discharges, V_B is severely reduced. By contrast, there is less degradation with the H_2 plasma exposures at higher source powers. This is likely related to the lower average ion energy at those conditions, as shown at the bottom of Figure 1.43. The average ion energy is approximately equal to the sum of dc self-bias and plasma potential, with the latter being in the range -22 to -28 V as determined by Langmuir probe measurements. Ion-induced lattice damage in GaN may display n-type conductivity, due to more N atoms being displaced. In addition, the heavy N_2^+ ions are also more effective in preferential sputtering of the N relative to Ga and creating N vacancies, compared with the H_2^+ ions. The net result is that N_2^+ ions will lead to more degradation of the surface electrical properties of GaN than do H_2^+ ions of similar energy.

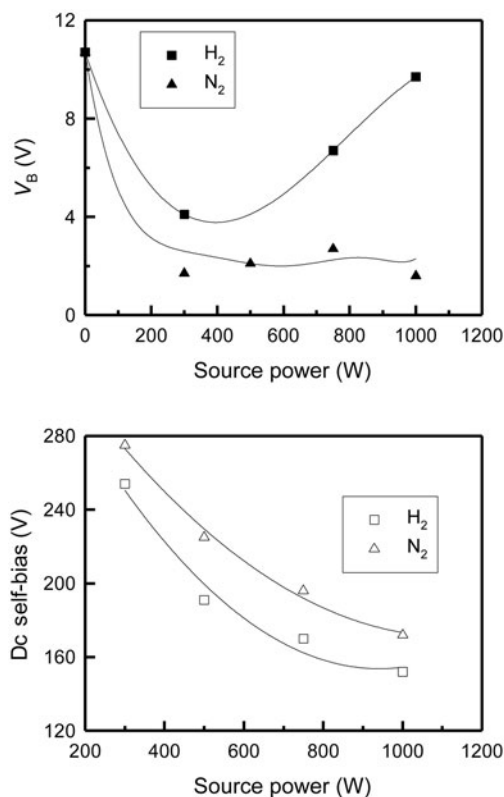


Figure 1.43. Variation of V_B in GaN diodes (top) and dc chuck self-bias (bottom) as a function of ICP source power in H_2 or N_2 plasmas (150 W rf chuck power, 5 mTorr)

Similar conclusions can be drawn from the data on the effect of increasing rf chuck power. Figure 1.44 shows the diode I–V characteristics from H_2 or N_2 plasma-exposed samples at fixed source power (500 W) but varying rf chuck power. There are once again very severe decreases in breakdown voltage and increases in leakage current. The dependence of V_B on rf chuck power during the plasma exposures is shown in Figure 1.45, along with the dc self-bias. The V_B values fall by more than a factor of two even for very low self-biases, and emphasize how sensitive the GaN surface is to degradation by energetic ion bombardment. The degradation saturates beyond ~ 100 W chuck power, corresponding to ion energies of ~ 175 eV. We assume that, once the immediate surface becomes sufficiently damaged, the contact properties basically cannot be made any worse and the issue is then whether the damage depth increases with the

different plasma parameters. Since ion energy appears to be a critical factor in creating the near-surface damage, damage depth would be expected to increase with ion energy in a non-etching process. In the case of simultaneous etching and damage creation (*e.g.* in Cl_2 -Ar etch processing), higher etch rates would lead to smaller depth of residual damage because the disordered region would be partially removed.

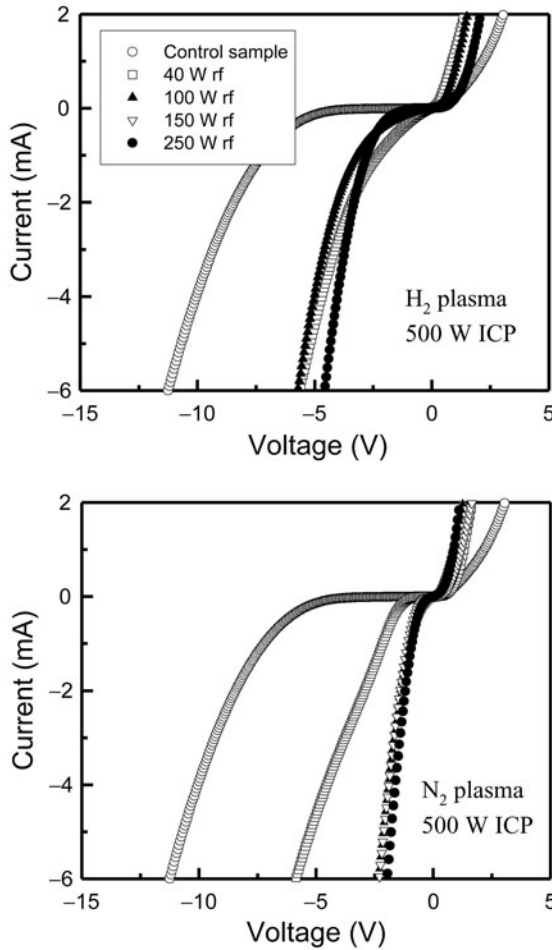


Figure 1.44. I–V characteristics from GaN diodes before and after H_2 (top) or N_2 (bottom) plasma exposure (500 W source power, 5 mTorr) at different rf chuck powers

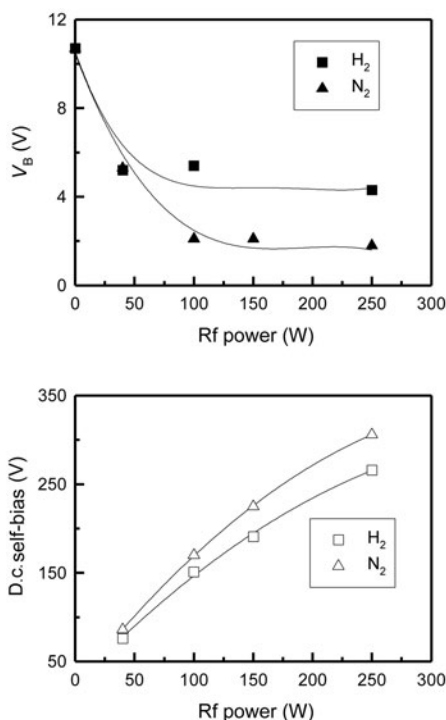


Figure 1.45. Variation of V_B in GaN diodes (top) and dc chuck self-bias (bottom) as a function of rf chuck power in H_2 or N_2 plasmas (500 W source power, 5 mTorr)

For completed n-GaN diodes exposed to ICP discharges we observed that the changes in the electrical properties were much less severe than those above. However, the low bias forward currents of the damaged devices were still increased by up to two orders of magnitude. Auger electron spectroscopy (AES) showed that plasma exposure created a N_2 -deficient region around the periphery of the rectifying contact, which reduced the barrier to current conduction. By contrast, the reverse I–V is more strongly dependent on the bulk doping in the GaN under the contact and is less affected by the plasma damage.

1.6.2 Effect of Etching Chemistries on Damage

It would be expected that exposure to etching chemistries such as Cl_2 –Ar create less and shallower damage, on the basis of the fast etching rate and hence improved damage removal. In this section we compare the effects

of Cl_2 -Ar and Ar ICP exposure on the electrical properties of n-GaN Schottky diodes. The layer structure consisted of $0.5\text{ }\mu\text{m n}^+$ (10^{18} cm^{-3}) GaN grown on *c*-plane Al_2O_3 substrate by MBE, followed by $1\text{ }\mu\text{m}$ of nominally doped ($n\approx 5\times 10^{16}\text{ cm}^{-3}$) GaN. The mesas were etched with Ar- Cl_2 ICP discharges at low powers, and ohmic contacts were formed by e-beam evaporation and lift-off of Ti-Al-Pt-Au, followed by annealing at 800°C to remove dry etch damage and alloy the contacts. The samples were exposed to either $10\text{Cl}_2/5\text{Ar}$ or 15Ar (where the numbers denote the gas flow rate in standard cubic centimeters per minute) ICP discharges in a Plasma-Therm ICP reactor at a fixed pressure of 3 mTorr. We investigated a range of rf chuck powers (25–250 W) and etch times (4–100 s), with a fixed source power of 500 W. The Schottky metallization Pt-Au ($\phi=50, 70$ or $90\text{ }\mu\text{m}$) was then deposited on the damaged surface by e-beam evaporation, followed by lift off. As schematic of the mesa diodes and an SEM micrograph are shown in Figure 1.46.

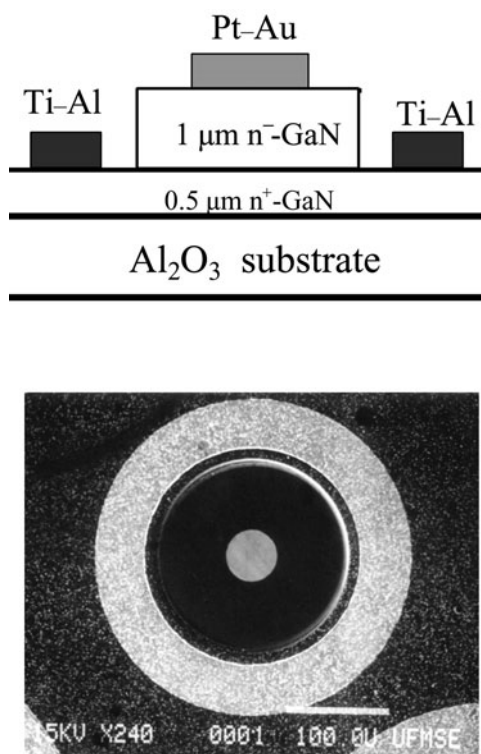


Figure 1.46. Schematic of the diode structure (top) and SEM of a complete device (bottom)

Figure 1.47 shows a series of I–V characteristics from n-type GaN diodes fabricated on samples exposed to either Cl_2 –Ar (top) or Ar (bottom) discharges at different rf chuck powers. There is a significant reduction in V_B under all conditions, with Ar producing less damage at low chuck powers. This is probably related to two factors: the slightly higher chuck bias with Cl_2 –Ar due to the lower positive ion density in the plasma (Cl is more electronegative than Ar) and the heavier mass of the Cl_2^+ ions compared to Ar^+ . This is consistent with data on the relative effects of N_2 and H_2 plasma exposure, *i.e.* ion mass was more important in influencing the electrical properties of the GaN surface than any chemical effects.

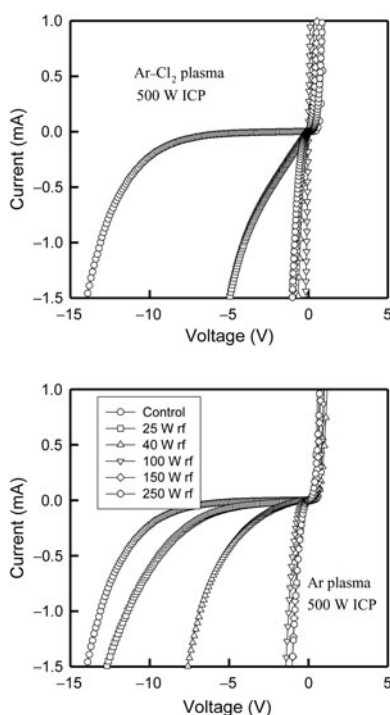


Figure 1.47. I–V characteristics from n-GaN samples exposed to ICP Cl_2 –Ar (top) or Ar (bottom) discharges (500 W source power) as a function of rf chuck power prior to deposition of the rectifying contact

The variations of V_B and V_F with the rf chuck power during plasma exposure are shown in Figure 1.48 (top). At powers ≤ 100 W (this correspond to ion energies $< \sim 150$ eV), the Cl_2 –Ar creates more degradation of V_B , as discussed above, while at higher powers the damage saturates. This is also reflected in the variation of the forward on-voltage V_F with rf chuck

power. Note that the etch rate in Cl_2 -Ar discharges increases rapidly with the rf chuck power (shown at the bottom of the figure). The amount of the etch damage is the direct result of competition between defect introduction and etching processes.

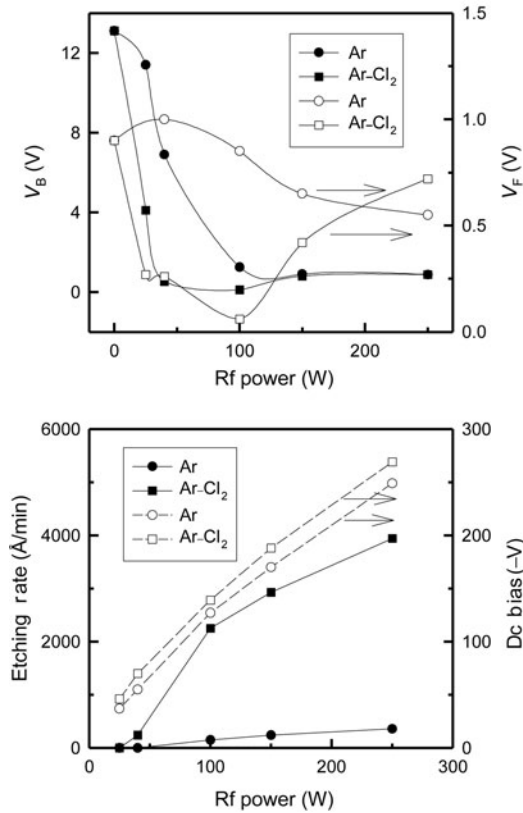


Figure 1.48. Variations of V_B and V_F (top), and n-GaN etching rate or dc self-bias (bottom) as a function of rf chuck power for n-GaN diodes exposed to ICP Ar and Cl_2 -Ar discharges (500 W source power)

Figure 1.49 shows a series of I-V characteristics from n-type GaN diodes fabricated on samples exposed to the two different plasmas for different times at fixed rf chuck power (150 W) and source power (500 W). It is clear that the damage accumulates rapidly, with the I-V characteristics becoming linear at longer times. The breakdown voltages are <1 V for basically all plasma exposure times for both Cl_2 -Ar and Ar. Figure 1.50 shows the variations in V_B and V_F in these diodes with plasma exposure,

together with the etch depth versus etch time (bottom). As is readily apparent, V_B decreases dramatically after even short plasma exposures (4 s) and then tends to recover slightly up to ~25 s. It should be remembered that this is damage accumulating ahead of the etch front. The V_B values are saturated after some points due to the etching or sputtering effect. Since the etch rate with $\text{Cl}_2\text{-Ar}$ is much faster (Figure 1.50, bottom), the damage accumulation in this chemistry should reach the saturation point much earlier, as shown in Figure 1.50 (top).

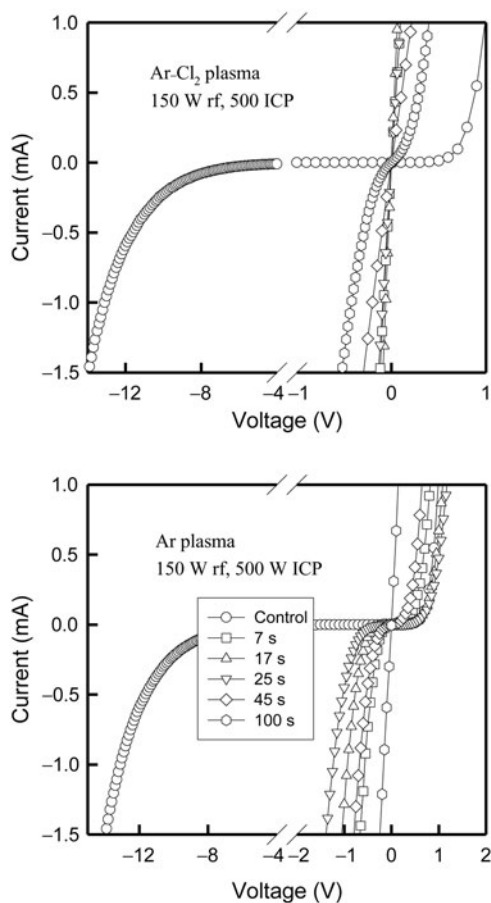


Figure 1.49. I–V characteristics from n-GaN samples exposed to ICP $\text{Cl}_2\text{-Ar}$ (top) or Ar (bottom) discharges (150 W rf chuck power, 500 W source power) as a function of plasma exposure time prior to deposition of the rectifying contact

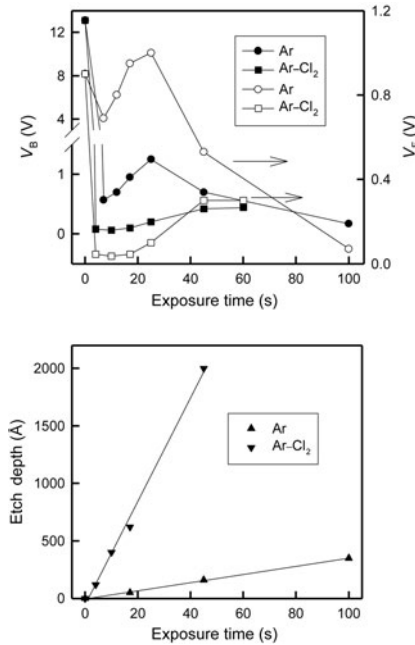


Figure 1.50. Variation of V_B and V_F (top) and of n-GaN etch depth (bottom) as a function of plasma exposure time for n-GaN diodes exposed to ICP Cl₂-Ar discharges (500 W source power 150 W rf chuck power)

The rapid accumulation could explain why Cl₂-Ar discharges produce more damage than pure Ar. Significant damage could be created in the near-surface region in this high-density plasma after even a very short exposure. The Schottky contact is most sensitive to the electrical properties of the immediate surface layer. For these reasons it is possible that Cl₂-Ar discharges, containing ions with higher energy and heavier mass, produce more degradation in the electrical properties of the GaN Schottky diodes than pure Ar discharges, even though the damage depth may be smaller due to high etch rate. Note that we have studied a worst-case scenario for damage introduction during ICP etching. In a real etch process of GaN device, damage would be less severe because much lower power conditions are employed.

1.6.3 Thermal Stability of Damage

To examine the thermal stability of the etch damage, the n-type GaN samples were exposed to the 500 W source power, 150 W rf chuck power (dc

self-bias -221 V), 5 mTorr N_2 discharge, and then annealed in N_2 for 30 s at 300 – 850°C prior to deposition of the rectifying contact. Figure 1.51 (top) compares the AFM data from the control sample, the as-exposed sample and samples annealed at 550°C or 750°C . The fact that plasma exposure severely degraded the surface is clear, as the RMS surface roughness increases from 0.8 nm to 4.2 nm. Subsequent annealing essentially restored the initial morphology. I–V data from annealed samples are shown in Figure 1.51 (bottom). These samples show that increasing the annealing temperature up to 750°C brings a substantial improvement in V_B . However, for annealing at 850°C the diode began to degrade, and this is consistent with the temperature at which N_2 begins to be lost from the surface.[59]

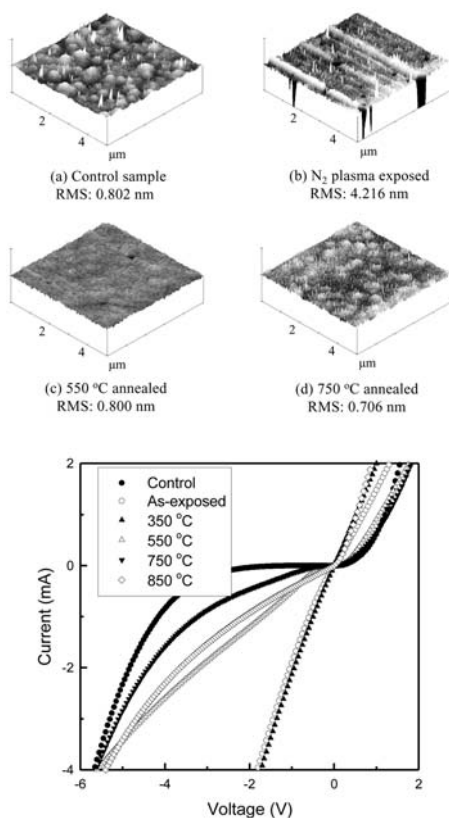


Figure 1.51. AFM scans of GaN surfaces (top) and I–V characteristics from GaN diodes (bottom) before and after N_2 plasma exposure (500 W source power, 150 W rf power, 5 mTorr) and subsequent annealing at different temperatures prior to deposition of the Schottky contacts

It is instructive to compare the thermal stability of Pt–Au contacts on the damaged and undamaged GaN. The metal was deposited on a control sample and a sample which was plasma exposed (N_2 , 500 W source power, 150 W rf chuck power, 5 mTorr), then annealed at different temperatures for 30 s. The I–V characteristics are shown in Figure 1.52. The Pt–Au contact is stable to 700°C on unetched samples, whereas in the case where the samples were exposed to the N_2 plasma the I–V characteristics show continued worsening upon annealing. The poorer stability in etched samples could be related to the surface damage enhancing interfacial reaction between the Pt and GaN, and ohmic contact on the damaged materials can take advantage of this enhanced alloying process.

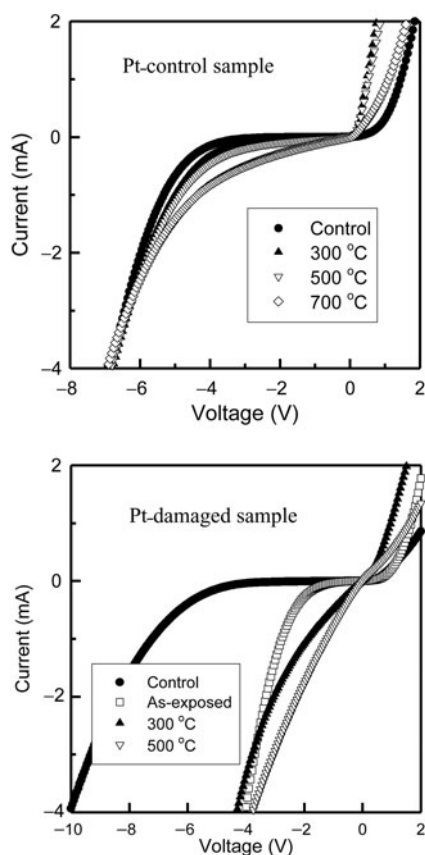


Figure 1.52. I–V characteristics from GaN diodes with Schottky metal deposited on control samples (top) and plasma-exposed samples (bottom) followed by annealing at different temperatures

Figure 1.53 shows I–V characteristics from control, samples which were exposed to Ar or Cl_2/Ar discharges at a fixed source power (500 W) and rf chuck power (150 W rf), and annealed in N_2 . Again, the annealing produced a significant recovery of the electrical properties, and more restoration was achieved for samples exposed to the Ar plasma. The V_B values are shown in Figure 1.54, as a function of post-plasma exposure annealing temperature. Annealing temperatures between 700–800°C restored >70% of the original V_B value, but clearly annealing alone cannot remove all of the dry etch induced damage. Annealing temperatures above 800°C were found to lead to preferential loss of N_2 from the surface, with a concurrent degradation in V_B .

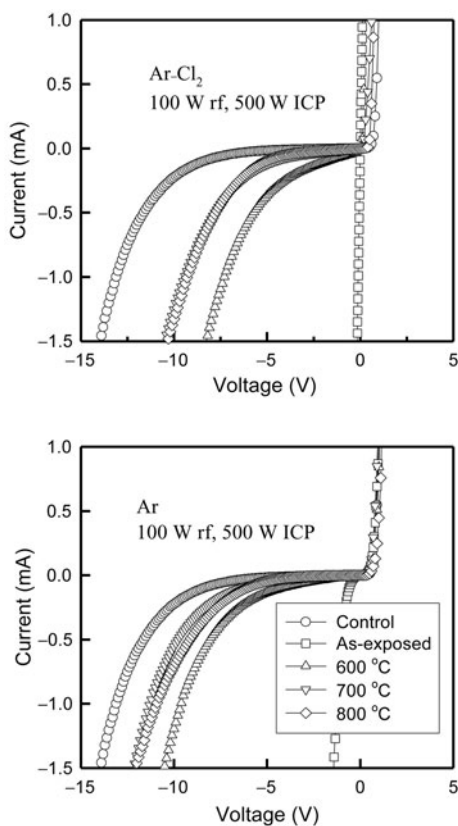


Figure 1.53. I–V characteristics from n-GaN samples exposed to ICP Cl_2 –Ar (top) or Ar (bottom) discharges (500 W source power, 100 W rf chuck power) as a function of annealing temperature prior to deposition of the rectifying contact

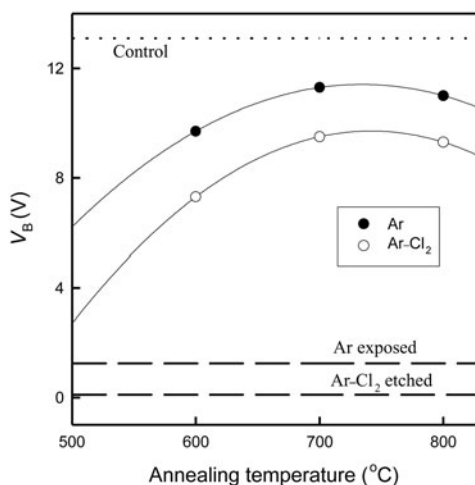


Figure 1.54. Variation of V_B in n-GaN diodes exposed to ICP Cl_2 -Ar or Ar discharges (500 W source power, 100 W rf chuck power) with annealing temperature prior to deposition of the rectifying contact

1.6.4 Plasma Damage in p-Gallium Nitride

The layer structure consisted of 1 μm of undoped GaN ($n \approx 5 \times 10^{16} \text{ cm}^{-3}$) grown on a c -plane Al_2O_3 substrate, followed by 0.3 μm of Mg doped ($p \approx 5 \times 10^{17} \text{ cm}^{-3}$) GaN. The samples were grown by rf plasma-assisted MBE. Ohmic contacts were formed with Ni-Au deposited by e-beam evaporation, followed by lift-off and annealing at 750°C. The GaN surface was then exposed for 1 min to ICP H_2 or Ar plasmas in a Plasma-Therm 790 System. The 2 MHz ICP source power was varied from 300 to 1400 W, while the 13.56 MHz rf chuck power was varied from 20 to 250 W. The former parameter controls the ion flux incident on the sample, while the latter controls the average ion energy. Ti-Pt-Au contacts with 250 μm diameter were deposited through a stencil mask. The I-V characteristics of the diodes were recorded on an HP 4145A parameter analyzer. The unetched control diodes have reverse breakdown voltages of ~ 2.5 –4 V depending on the wafer – these values were uniform ($\pm 12\%$) across a particular wafer.

Figure 1.55 shows the I-V characteristics from samples exposed to either H_2 (top) or Ar (bottom) ICP discharges (150 W rf chuck, 2 mTorr) as

a function of source power. In both cases there is an increase in both the reverse breakdown voltage and the forward turn-on voltage, with these parameters increasing monotonically with the source power during plasma exposure.

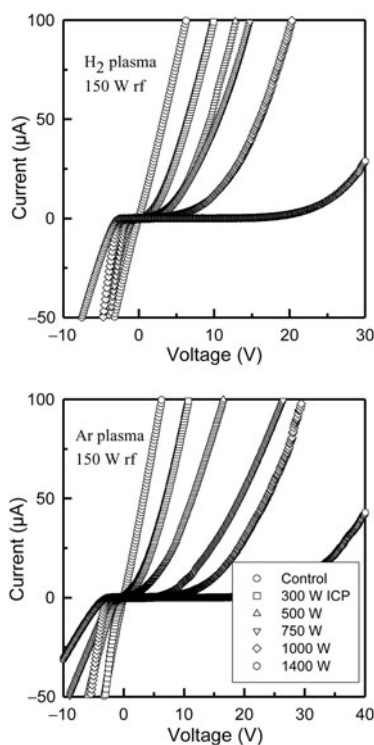


Figure 1.55. I-V characteristics from samples exposed to either H₂ (top) or Ar (bottom) ICP discharges (150 W rf chuck power) as a function of ICP source power prior to deposition of the Ti-Pt-Au contact

Figure 1.56 shows this increase in breakdown voltage as a function of source power, and also the variation of the chuck dc self-bias. As the source power increases, the ion density also increases and the higher plasma conductivity suppresses the dc bias developed. Note that the breakdown voltage of the diodes continues to increase even as this bias (and hence ion energy, which is the sum of this bias and the plasma potential) decreases. These results show that ion flux plays an important role in the change of diode electrical properties. The other key result is that Ar leads to consistently more of an increase in breakdown voltage, indicating

that ion mass is important, rather than any chemical effect related to removal of N_2 or NH_3 in the H_2 discharges.

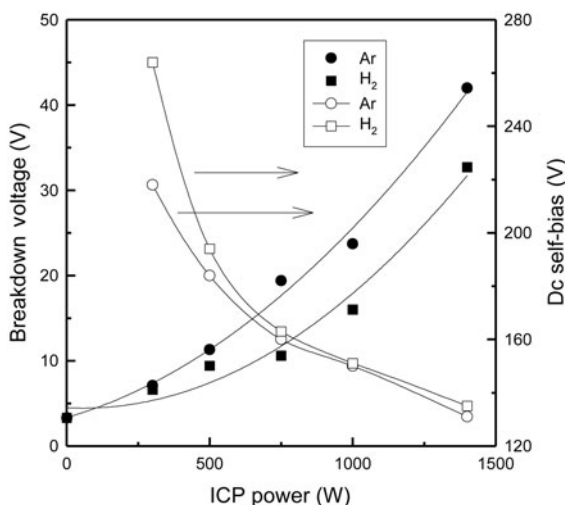


Figure 1.56. Variation of diode breakdown voltage in samples exposed to H_2 or Ar ICP discharges (150 W rf chuck power) at different ICP source powers prior to deposition of the Ti–Pt–Au contact. The dc chuck self-bias during plasma exposure is also shown

The increase in breakdown voltage on the p-GaN is due to a decrease in hole concentration in the near-surface region through the creation of shallow donor states. The key question is whether there is actually conversion to an n-type surface under any of the plasma conditions. Figure 1.57 (top) shows the forward turn-on characteristics of the p-GaN diodes exposed to different source power Ar discharges. At low source power (300 W), the turn-on remains close to that of the unexposed control sample, *i.e.* the surface remains p-type with no significant reduction in conductivity. However, there is a clear increase in the turn-on voltage at higher source powers, and in fact at ≥ 750 W the characteristics are those of an n–p junction, *i.e.* the surface has converted to n-type. The turn-on voltage at the highest flux conditions is ~ 3.3 V (Figure 1.57 (bottom)), which is close to the built-in potential of a GaN n–p diode. Since the hole concentration in the GaN is $\sim 10^{17} \text{ cm}^{-3}$, the Mg acceptor concentration is $\sim 10^{19} \text{ cm}^{-3}$ based on the ionization level of ~ 170 meV. This means the plasma exposure at high flux conditions produces $>10^{19} \text{ cm}^{-3}$ shallow donor states and there is surface conversion. According to our previous study [111], the obvious conclusion is that nitrogen vacancies create these shallow donor levels. We

found that N_2 loss from the p-GaN surface during thermal annealing at temperatures $>900^\circ\text{C}$ also produced significantly decreased p-type conduction.

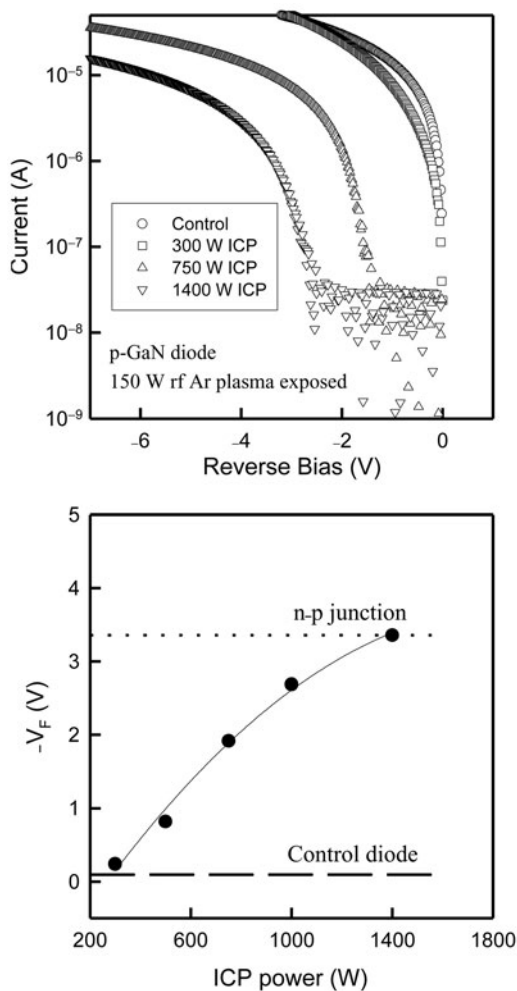


Figure 1.57. Forward turn-on characteristics (top) and turn-on voltage (bottom) of diodes exposed to ICP Ar discharges (150 W rf chuck power) at different ICP source powers prior to deposition of the Ti–Pt–Au contact

The influence of rf chuck power on the diode I–V characteristics is shown in Figure 1.58 for both H_2 and Ar discharges at fixed source power (500 W). A similar trend is observed as for the source power experiments, namely the reverse breakdown voltage increases, consistent with a reduc-

tion in p-doping level near the GaN surface. Surface type conversion also occurred at high powers.

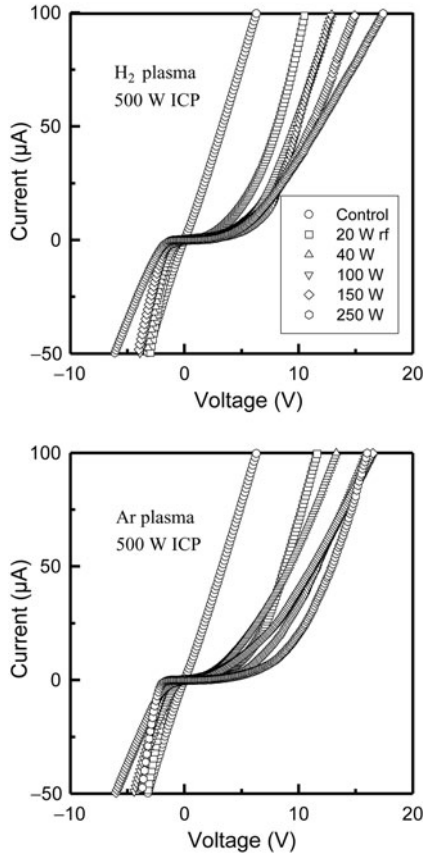


Figure 1.58. I–V characteristics from samples exposed to either H_2 (top) or Ar (bottom) ICP discharges (500 W source power) as a function of rf chuck power prior to deposition of the Ti–Pt–Au contact

Figure 1.59 plots breakdown voltage and dc chuck self-bias as a function of the applied rf chuck power. The breakdown voltage initially increases rapidly with ion energy (the self-bias plus ~ 25 V plasma potential) and saturates above ~ 100 W probably due to the fact that sputtering yield increases and some of the damaged region is removed. Note that there are very large changes in breakdown voltage even for low ion energies, emphasizing the need to control both flux and energy carefully.

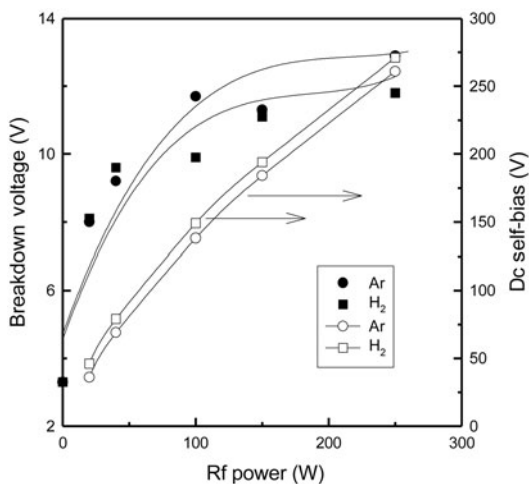


Figure 1.59. Variation of diode breakdown voltage in samples exposed to H₂ or Ar ICP discharges (500 W source power) at different rf chuck powers prior to deposition of the Ti–Pt–Au contact. The dc chuck self-bias during plasma exposure is also shown

1.6.5 Thermal Stability of Damage

One important method of removing plasma-induced damage is annealing. In these experiments we exposed the samples to the same type of plasma (Ar, 750 W source power, 150 W rf chuck power) and then annealed under N₂ at different temperatures. Figure 1.60 (top) shows the I–V characteristics of these different samples, and Figure 1.60 (bottom) shows the resulting breakdown voltages as a function of annealing temperature. On this wafer, plasma exposure caused an increase in breakdown voltage from ~2.5 to ~18 V. Subsequent annealing at 400°C initially decreased the breakdown voltage, but higher temperatures produced a large increase. In some cases, the samples were found to be highly compensated after annealing at 600–700°C. At temperatures above 700°C, the diode characteristics returned toward their initial values and were back to the control values by 900°C. This behavior is similar to that observed in implant-isolated compound semiconductors, where ion damage compensates the initial doping in the material, producing higher sheet resistances. In many instances the damage site density is larger than that needed to trap all of the free carriers, and trapped electrons or holes may move by hopping conduction. Annealing at higher temperatures removes some of the damage sites, but there are still enough to trap all the conduction electrons/holes. Under these conditions the hopping conduction is reduced and the sample

sheet resistance actually increases. At still higher annealing temperatures, the trap density falls below the conduction electron or hole concentration and the latter are returned to their respective bands. Under these conditions the sample sheet resistance returns to its pre-implanted value. The difference in the plasma-exposed samples is that the incident ion energy is a few hundred electron-volts compared to a few hundred kilo-electron-volts in implant-isolated material. In the former case the main electrically active defects produced are nitrogen vacancies near the surface, whereas in the latter case there will be vacancy and interstitial complexes produced in far greater numbers to far greater depths. We did not examine the time dependence of the damage removal, but expect it would show a square-root power of annealing time.

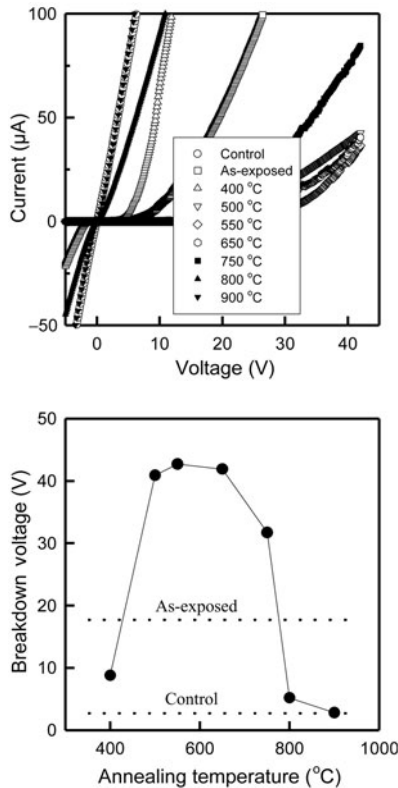


Figure 1.60. I–V characteristics from samples exposed to ICP Ar discharges (750 W source power, 150 W rf chuck power) and subsequently annealed at different temperatures prior to deposition of the Ti–Pt–Au contact (top) and breakdown voltage as a function of annealing temperature (bottom)

In our previous work on plasma damage in n-GaN [111] we found that annealing at $\sim 750^\circ\text{C}$ almost returned the electrical properties to their initial values. If the same defects are present in both n- and p-type materials after plasma exposure, then this difference in annealing temperature may be a result of a Fermi level dependence on the annealing mechanism.

1.6.6 Determination of Damage Profile in Gallium Nitride

An important concern is the depth of the plasma-induced damage. We found we were able to etch p-GaN very slowly in boiling NaOH solutions, at rates that depended on the solution molarity (Figure 1.61) even without any plasma exposure of the material. This enabled us to directly measure the damage depth in plasma exposed samples in two different ways.

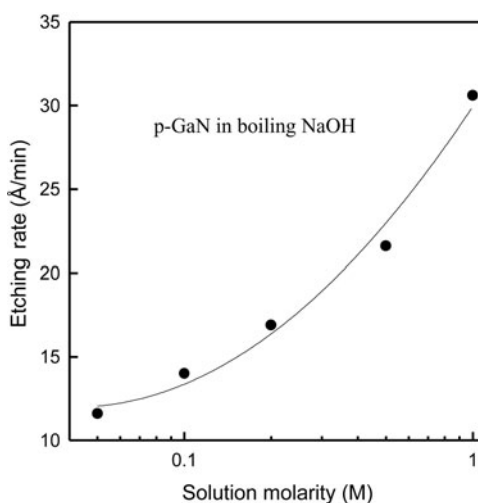


Figure 1.61. Wet etching rate of p-GaN in boiling NaOH solutions as a function of solution molarity

The first method involved measuring the etch rate as a function of depth from the surface. Defective GaN resulting from plasma, thermal or implant damage can be wet chemically etched at rates much faster than undamaged material because the acid or base solutions are able to attack the broken or strained bonds present. Kim *et al.* [115] reported that the wet etch depth on thermally or ion-damaged GaN was self-limiting. Figure 1.62 shows the GaN etch rate as a function of depth in samples exposed to a 750 W source power, 150 W rf chuck power Ar discharges (-158 V dc

bias). The etch rate is a strong function of the depth from the surface and saturates between ~ 425 and 550 Å. Within this depth range the etch rate is returned to the “bulk” value characteristic of undamaged p-GaN.

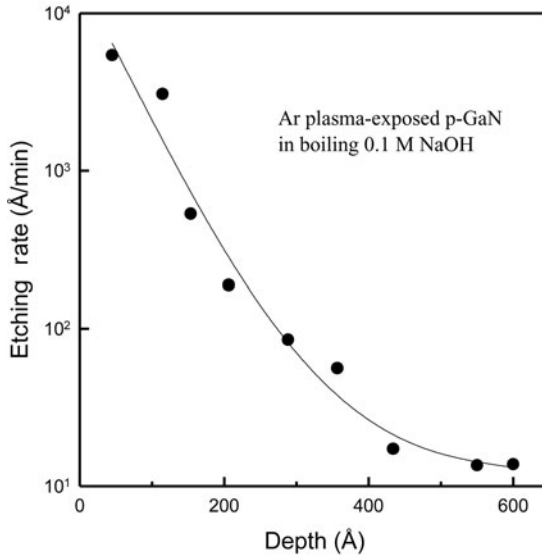


Figure 1.62. Wet etching rate of Ar plasma-exposed (750 W source power, 150 W rf chuck power) p-GaN as a function of depth into the sample

The second method to establish damage depth, of course, is simply to measure the I–V characteristics after removing different amounts of material by wet etching prior to deposition of the rectifying contact. Figure 1.63 (top) shows the I–V characteristics from samples exposed to 750 W source power, 150 W rf chuck power (-160 V dc chuck bias) Ar discharges and subsequently wet etched to different depths using 0.1 M NaOH solutions before deposition of the Ti–Pt–Au contact. Figure 1.63 (bottom) shows the effect of the amount of material removed on the diode breakdown voltage. Within the experimental error of $\pm 12\%$, the initial breakdown voltage is re-established in the range 400 – 450 Å. This is consistent with the depth obtained from the etch-rate experiments described above, and corresponds to an ion energy of ~ 180 eV.

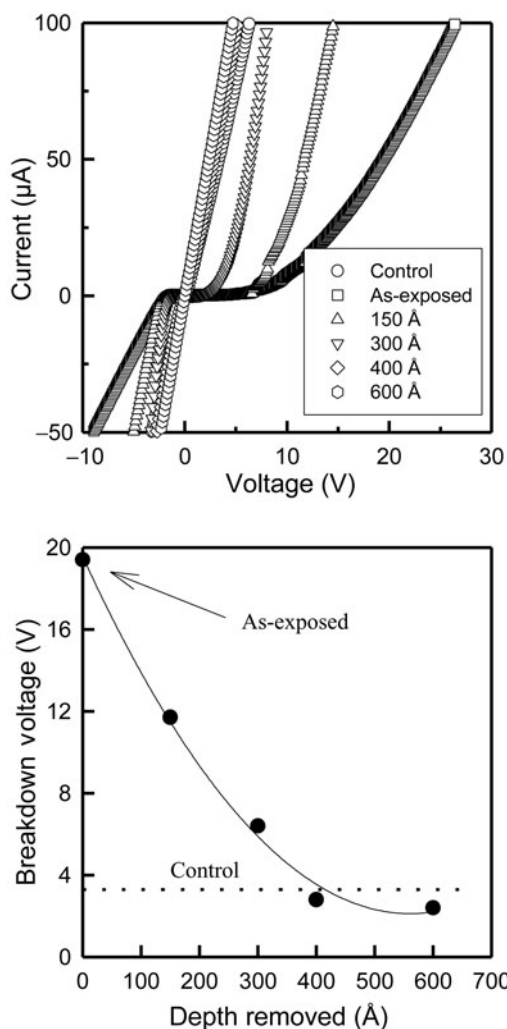


Figure 1.63. I–V characteristics from samples exposed to ICP Ar discharges (750 W source power, 150 W rf chuck power) and subsequently wet etched to different depths prior to deposition of the Ti/Pt/Au contact (top) and breakdown voltage as a function of depth removed (bottom)

It would be instructive to determine and compare the damage depth created after exposure to Cl_2 –Ar and Ar discharges (500 W source power, 150 W rf chuck power, 1 min, -192 V or -171 V dc chuck bias). For these plasma conditions, we did not observe type conversion of the surface. The values of forward turn-on voltage increased after plasma exposure, due to the lowered net hole concentration. The electrical properties are almost re-

stored after depths of 500–600 Å were removed by NaOH etching, as can be seen in Figure 1.64. This data can also be obtained from Figure 1.65, where the wet etch depth in plasma-damaged p-GaN is plot as a function of etching time. What is clear from this data is that the damage depth produced in Cl_2 -Ar discharges is only slightly smaller than that in Ar discharges, even though the etch rate of GaN in the former plasma is almost 30 times higher.

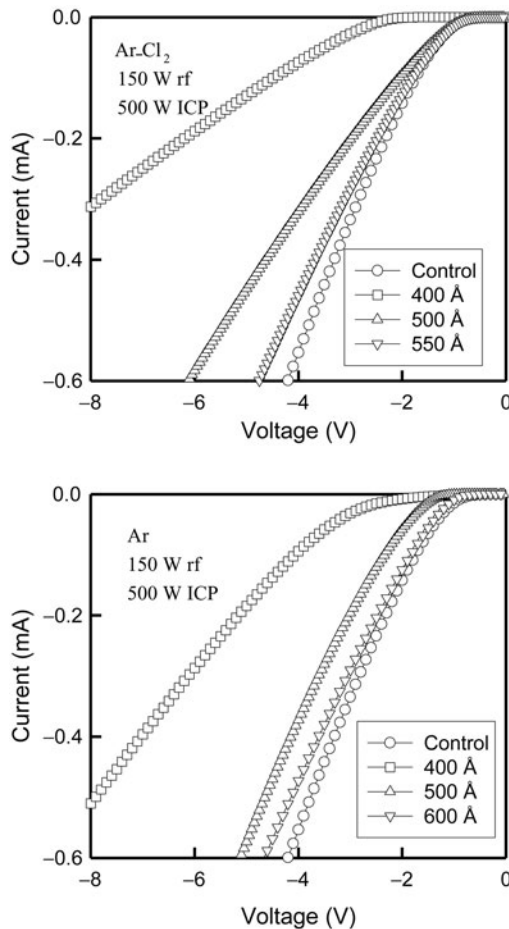


Figure 1.64. Forward I-V characteristics from p-GaN samples exposed to ICP Cl_2 -Ar (top) or Ar (bottom) discharges (500 W source power, 150 W rf chuck power) and wet etched in boiling NaOH to different depths prior to deposition of the rectifying contact

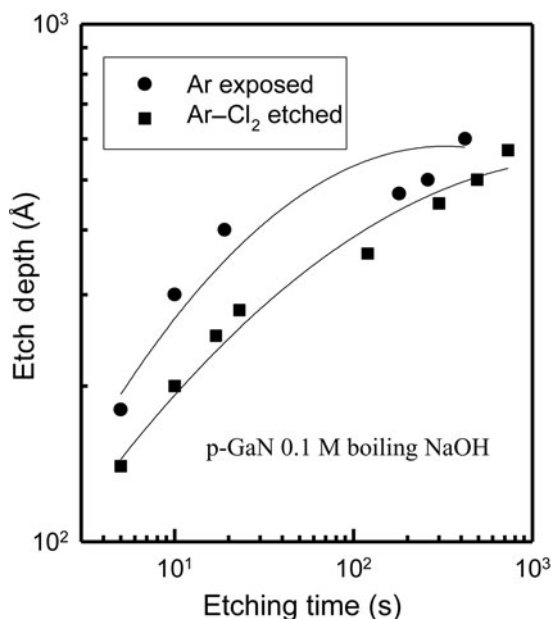


Figure 1.65. Wet etch depth versus etch time in boiling NaOH solutions for plasma-damaged p-GaN

The damage depth in n-type GaN can be established by photoelectrochemically (PEC)[116] wet etching different amounts of the plasma-exposed material, and then measuring the electrical properties of the GaN surfaces. For samples exposed to a 500 W source power, 150 W rf chuck power N₂ discharge, the reverse breakdown voltage was restored to about half of its initial value after removal of ~260 Å damaged layer. However, increasingly rough surfaces of PEC etching for larger removal depths were usually observed. The estimated damage depth for the N₂ plasma conditions mentioned above could be similar to that established in p-type GaN samples exposed to similar plasma conditions.

1.7 Conclusions and Future Trends

Recognized for their stability in harsh environments and their unique optical and electronic properties, the III–V nitrides have become one of the few select classes of materials being engineered into optoelectronics and

microelectronic devices demanded by today's technologically advancing society. Although early progress was slowed by the lack of ideal substrates and p-type doping ability, the pace of successful GaN-based device fabrication has accelerated within the last few years. The commercialization of blue and green LEDs and the achievement of long lifetime LDs have been followed by the realization of UV photodetectors and numerous different electronic devices. However, the scientific understanding necessary to routinely reproduce these results and advance device performance is still lacking in many critical areas. While further improvement in heteroepitaxial growth is currently gaining considerable attention, a reliable processing procedure is another critical factor for GaN to reach its full potential, especially for microwave power electronics. This dissertation has focused on several important aspects of GaN processing, with efforts directed towards optimizing GaN technology and improving GaN-based device performance.

A novel RTP at temperatures up to 1500°C has been developed for GaN and related materials. High quality AlN has proven to be an efficient encapsulant at these temperatures, and can be removed selectively in KOH solutions. High-dose Si implantation followed by 1400°C annealing produced metallic doping levels ($\sim 5 \times 10^{20} \text{ cm}^{-3}$) in GaN. Post-implant annealing at 1100°C was found to be insufficient to remove the lattice damage, while 1400°C produced much lower defect densities. The implantation and activation of other common donors and acceptors in GaN have also been examined. The Group VI donors, though free of the potential drawback of being amphoteric, did not show any advantages over Si for creation of n-type doping in GaN. Only Mg was found to produce p-type conductivity, while C- and Be-implanted samples remained n-type due to strong compensation effects. None of the implanted species showed measurable diffusion at high temperatures, but Be did display an apparent defect-assisted redistribution at 900°C. A summary of these results is shown in Table 1.4.

To fully develop the potential of ion implantation in advanced electronics, there is still a need to examine further the possible implanted dopants in GaN, especially to improve p-type doping efficiency in GaN or AlGaN. One attractive technique is to improve the occupation of dopants on the desirable lattice sites through co-implantation, such as co-implantation of C, Ge or Sn with Group III species for more conducting p-type nitrides, and co-implantation of Si and Group VI dopants to get even better n-type conductivity.

Table 1.4. Ion implantation doping in GaN

	Max achievable doping level (cm ⁻³)	Diffusivity (cm ² ·s ⁻¹)	Ionization level (meV)
Donors			
Si	5×10 ²⁰	<2×10 ⁻¹³ (1500°C)	28
S	5×10 ¹⁸	<2×10 ⁻¹³ (1400°C)	48
Se	2×10 ¹⁸	<2×10 ⁻¹³ (1450°C)	–
Te	1×10 ¹⁸	<2×10 ⁻¹³ (1450°C)	50
Si	5×10 ²⁰	<2×10 ⁻¹³ (1500°C)	28
S	5×10 ¹⁸	<2×10 ⁻¹³ (1400°C)	48
Se	2×10 ¹⁸	<2×10 ⁻¹³ (1450°C)	–
O	3×10 ¹⁸	<2×10 ⁻¹³ (1200°C)	30
Acceptors			
Mg	~5×10 ¹⁷	<2×10 ⁻¹³ (1450°C)	170
Be	n-type	Defect-assisted	165
C	n-type	<2×10 ⁻¹³ (1400°C)	–

High sheet resistances of ~10¹² Ω/square in n-GaN and 10¹⁰ Ω/square in p-GaN have been achieved by implantation of O, Cr, Fe and Ti. The concentration of electrically active deep energy levels related to the chemical nature of these species was found to be <7×10¹⁷ cm⁻³, and the implanted GaN displayed typical damage-related isolation behavior. Temperature-dependent measurements showed that the defect levels are in the range 0.2–0.49 eV in n-GaN and are ~0.44 eV in p-GaN, which are far from midgap, but sufficient to produce high resistivity materials. Future work in the area of implant isolation includes searching for high compensation in InGaN and thermally stable isolation for use at elevated temperatures.

W-based contacts deposited on Si-implanted GaN produced ohmic contacts with low resistance of 10⁻⁶ Ω·cm². Minimal reaction at the W–GaN interface was observed even at 1000°C. The behavior of W and WSi on p-type GaN has been compared with that of Ni–Au. True ohmic characteristics were obtained only at elevated temperatures. The refractory contact schemes offer superior thermal stability to the standard metallization used in photonic devices, *i.e.* Ti–Al and Ni–Au, and, therefore, are very promising for GaN-based ultra-high-power electronics. At this point, difficulty in achieving low resistance p-type ohmic behavior is still one of the major obstacles in fabricating efficient photonic devices. Further improvements in this area must be achieved at the next stage, including better understanding of metal–GaN reactions and use of these reactions for tunneling and/or lowering barrier height, exploring and incorporating a graded structure or superlattice layer, or highly doped material with a narrower band gap for ohmic contacts.

Dry etch damage is another key issue for optimization of GaN processing. In this work, plasma damage in n- and p- GaN has been studied systematically using Schottky diode measurements. ICP discharges (including real etching chemistries) produced large changes in diode characteristics. The results are consistent with creation of nitrogen vacancy – related shallow donors in the near-surface region ($<600 \text{ \AA}$), which decrease the doping concentration in p-GaN and increase electron density in n-GaN. Surface type conversion was observed in p-GaN at high ion fluxes and high ion energies. The damage was found to accumulate rapidly, and ion mass appeared to be a key parameter in determining the magnitude in degradation of material properties. Annealing at $\sim 750^\circ\text{C}$ for n-GaN and 850°C for p-GaN, or wet chemical etching have proven to be efficient for damage removal. For GaN-based microelectronics, other promising low-damage, etching such as low energy electron-enhanced etching [117–122] or photo-assisted vapor etching,[124] could become alternative techniques and attract more and more attention in the future.

GaN and related materials provide exciting opportunities in material research and device engineering, and are perhaps a model system for the interplay between science and technology. In the photonics arena, device applications have appeared before there was a complete understanding of the growth and defect issues. Today, research regarding the III–V nitride materials is focused on the optimization of these and other devices, and realization of their theoretical potential; thus, methods to improve heteroepitaxial growth and critical advances in processing technology are once again at the forefront.

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