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**Enhancement-Mode GaN-Based HEMTs
for High-Voltage Switching Applications**

A Dissertation submitted in partial satisfaction

of the requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

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March 2008

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*Dedicated to my parents,
Yugap and Soohee*

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- Method to Fabricate III-N Semiconductor Devices on the N-face of Layers which are Grown in the III-face Direction Using Wafer Bonding and Substrate Removal (Pending)

PUBLICATIONS

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Abstract

Enhancement-Mode GaN-Based HEMTs for High-Voltage Switching Applications

by Chang Soo Suh

High-voltage switching applications require normally-off or enhancement-mode devices because safety is the primary concern. Although AlGaN/GaN HEMTs are capable of delivering breakdown voltage and on-resistance beyond the material limits of other semiconductors used for high-voltage switching applications, these devices are typically normally-on or depletion-mode devices due to the large polarization-induced charge in AlGaN/GaN heterostructures. This dissertation focuses on development of enhancement-mode AlGaN/GaN HEMTs for high-voltage switching applications.

The barrier created by the gate between the source and drain-side access regions was identified as an important design parameter for minimizing off-state leakage and operation at high temperatures. The design space of gate-recessed AlGaN/GaN enhancement-mode HEMTs showed that in order to obtain enhancement-mode devices with sufficiently low on-resistances, very thin AlGaN barriers are needed below the gate and AlN interlayers cannot be used to improve device performance. Although fabricated devices showed

positive threshold voltages, devices showed significant off-state leakage due to a low source-to-drain barrier height.

The effects of fluorine-based plasma treatment on AlGa_N/Ga_N HEMTs were systematically studied and a self-aligned low-damage treatment for enhancement-mode operation was developed. With the integration of self-aligned integrated field-plates, true enhancement-mode AlGa_N/Ga_N HEMTs with low off-state leakage were developed. Although these devices exhibited record breakdown voltage of 1400 V and good switching characteristic, negative shift of threshold voltage at moderately high temperatures were observed.

The design space of AlGa_N/Ga_N HEMTs with a full-depleted p-Ga_N layer below the gate showed that it is possible to get a relatively low on-resistance with a reasonably thick AlGa_N layer. In addition, Al_N interlayers can be used to further improve device performances in this approach. Although enhancement-mode devices with low off-state leakage were developed, DC-to-RF dispersion was observed in these devices even after passivation. The cause of this dispersion is yet unclear and this issue needs to be resolved. Although AlGa_N/Ga_N HEMTs have the potential to deliver low on-resistance and high breakdown voltages, several challenges remain for high-voltage switching applications.

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1

Introduction

Over the past two decades, monumental progress has been made in the research and development of gallium nitride (GaN) for a broad range of applications. GaN and its family of III-V nitride semiconductors exhibit several distinctive and complimentary properties that make them the most complete semiconductor family available at present. With the recent commercialization of GaN-based light emitting diodes (LEDs), laser diodes, and microwave high-electron-mobility-transistors (HEMTs), GaN has firmly established its place in the semiconductor industry.

Indium gallium nitride ($\text{In}_x\text{Ga}_{1-x}\text{N}$) and aluminum gallium nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$) alloys cover a broad range of direct-bandgap energy, allowing for use of these semiconductors in light emitting devices. Spanning 0.7 eV to 6.2

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eV, the bandgap energy range of this system enables output in the entire visible spectrum and even deep ultraviolet (UV) wavelengths. Through improvements in material growth, device designs and process technology, record performances in green, blue, and UV light emitters are rapidly transforming the lighting and display industry [1]. Nitride-based photodetectors are also receiving interest as candidates for detection of UV and infrared waves. Among a very wide range of UV detector applications, AlGaIn-based photoconductive detectors [2] are drawing interest for low cost applications such as fire detection and solar UV monitoring due to their simplicity, responsivity, and relatively low cost. Moreover, detection of infrared spectrum, including the 1.55 μm -wavelength used in optical communications, has been demonstrated in GaN/AlN-based quantum-well infrared photodetectors (QWIP) that utilize intersubband transitions [3].

Nitride semiconductors grown in the [0001] direction of a wurtzite crystal structure or in the [111] direction of a zinc-blend crystal structure exhibit extremely large piezoelectric polarization constants and thus have found applications in micro-electromechanical systems (MEMs) [4]. Due to high surface acoustic wave (SAW) velocity, AlN-based SAW filters with 1-GHz-band have already been demonstrated [5]. Furthermore, demonstration of

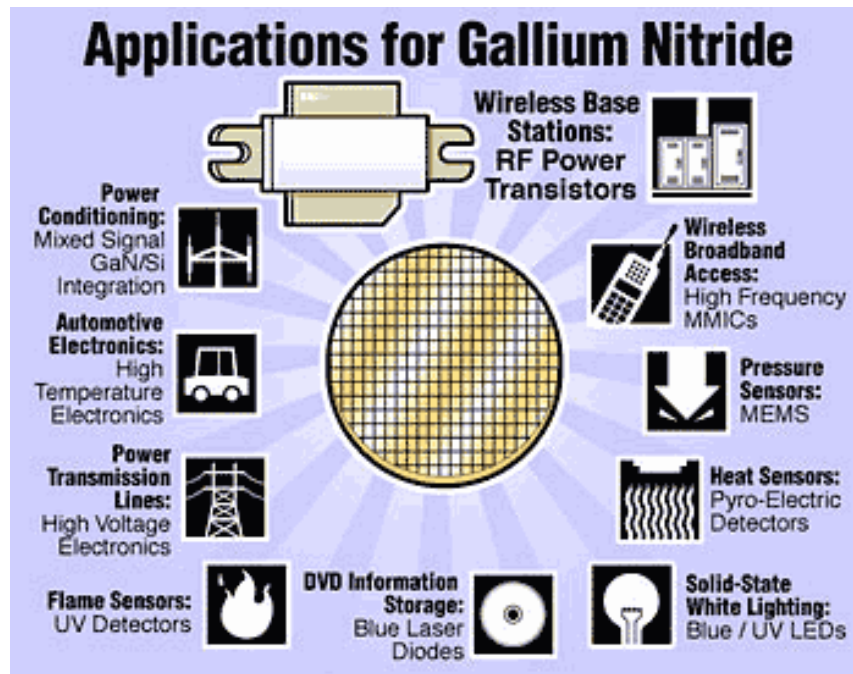


Figure 1.1: Applications being pursued by GaN and its family of nitride semiconductors (from www.nitronex.com)

room temperature ferromagnetism in transition-metal-doped GaN has sparked efforts even in spintronics applications [6].

GaN is also attractive for a large variety of electronics applications due to excellent electron transport and electrical properties. Among numerous GaN-based electronic devices, the AlGaIn/GaN HEMTs have garnered major part of the focus due to the excellent performances at microwave and mm-wave frequencies. AlGaIn/GaN HEMTs exhibit electron velocity of 2.5×10^7 m/s, polarization-induced 2-dimensional-electron-gas (2DEG) density and

Characteristic (unit)	Si	4H-SiC	GaN (AlGaN/GaN)
E_G (eV)	1.1	3.26	3.39
μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	1500	700	2200
v_S ($\times 10^7$ cm/s)	1	2	2.5
E_C (MV/cm)	0.3	3	3.5
θ_K (W/cm $\cdot$ K)	1.5	4.5	1.3
ϵ_r	11.8	10	9

Table 1.1: Physical properties of Si, SiC and AlGaN/GaN

mobility of $1 \times 10^{13} \text{ cm}^{-2}$ and $2200 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, respectively. High breakdown fields associated with wide-bandgap (2.4 and 3.5 MV/cm for GaN and $\text{Al}_{0.22}\text{Ga}_{0.78}\text{N}$, respectively) also makes AlGaN/GaN HEMTs an excellent candidate for power electronics. Figure 1.1 shows variety of applications that are being pursued by GaN and its family of nitride semiconductors [7].

In recent years, interest in AlGaN/GaN HEMTs for high-voltage switching applications has drastically increased due to numerous demonstrations of high breakdown voltage (V_{BD}) and low on-resistance (R_{ON}) [8, 9]. Owing to excellent material properties, AlGaN/GaN HEMTs are capable of delivering V_{BD} and R_{ON} beyond the material limits of silicon (Si) and silicon carbide (SiC), semiconductors used today for high-voltage switching applications. Table 1.1 lists some material properties of Si, SiC and AlGaN/GaN HEMT structure that are relevant to high-voltage switching applications. The AlGaN/GaN HEMT structure is superior in just about every

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property except thermal conductivity (θ_k), typically mitigated by epitaxial growth on SiC substrates.

AlGaN/GaN HEMTs are typically normally-on or depletion-mode devices due to the large polarization-induced charge in AlGaN/GaN heterostructures. However, normally-off or enhancement-mode devices with positive threshold voltages (V_{TH}) are necessary for high-voltage switching application because safe operation is the primary concern in this application. This dissertation describes the development and evaluation of various GaN-based enhancement-mode HEMTs for potential application in high-voltage switching applications. The aim of the work was to identify design parameters critical to enhancement-mode devices for high-voltage switching applications, establish the design spaces, develop processing techniques for the fabrication of devices, and resolve the roadmap towards large-scaled enhancement-mode HEMTs with low R_{ON} , high V_{TH} and V_{BD} .

1.1 Switching Device Figures of Merit

There are numerous analyses of the impact of material parameters on the performance of semiconductor devices. Johnson's figure of merit [10]

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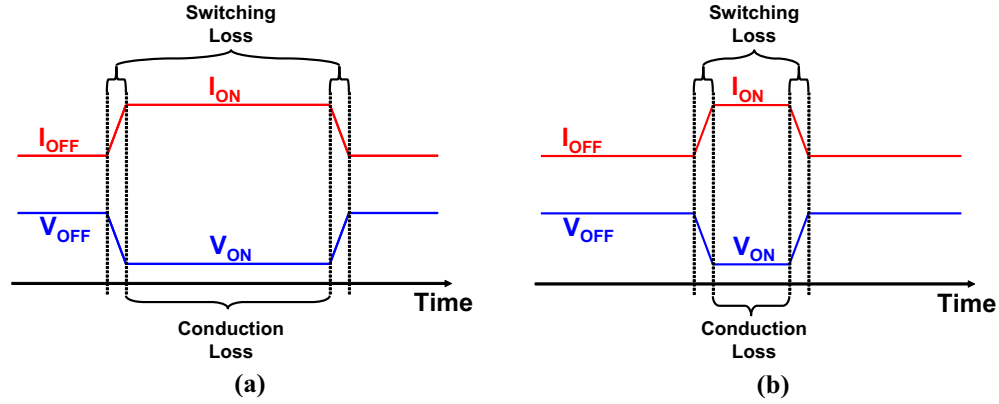


Figure 1.2: The ratio of switching time to conduction time is low at (a) low frequencies where conduction loss is dominant and high at (b) high frequencies where switching loss becomes increasingly important

$$JFOM = \frac{E_C \cdot v_s}{2\pi} \quad (1.1.1)$$

defines the power-frequency product for a low-voltage transistor. E_C is the critical electric field for breakdown and v_s is the saturated drift velocity.

Keye's figure of merit [11]

$$KFOM = \Theta_K \left(\frac{c \cdot v_s}{4\pi\epsilon} \right)^{1/2} \quad (1.1.2)$$

accounts for thermal (Θ_K) limitations to the switching behavior of transistors used in integrated circuits. Based on the assumption that power losses in switching devices are exclusively due to conduction losses or power dissipation during the on-state of a power field-effect transistor (FET), Baliga's [12] figure of merit

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$$BFOM = \varepsilon \cdot \mu \cdot E_G^3 \quad (1.1.3)$$

defines material parameters to minimize losses in power FETs switching at low frequencies. Here, μ is the charge mobility and E_G is the bandgap energy of the semiconductor. At low frequencies, switching losses associated with rise and fall (switching) times can be ignored since time-length of the on-state (conduction time) is much greater than the rise and fall times.

The rise and fall times become increasingly important for high-voltage switching applications at higher frequencies. As shown in Figure 1.2, with increasing switching frequency, the ratio of switching time to conduction time increases. Increasing the device area reduces conduction losses but simultaneously increases switching losses due to increased input capacitances. Therefore, for a given switching frequency, the total power loss must be minimized by choosing the optimum area of the device, which leads to equal conduction and switching losses. Then, the minimum power loss follows

$$P_{loss,min} \propto \frac{\sqrt{f}}{\sqrt{\mu E_C}} \quad (1.1.4)$$

and thus the denominator of equation 1.1.4 becomes the high frequency figure of merit [21-22]. Alternatively, Baliga's high frequency figure of merit (BHFOM)

$$BHFOM = \mu E_C^2 \quad (1.1.5)$$

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is given by the square of the denominator of equation 1.1.4 [15]. Although power loss increases with increasing switching frequency, since passive components scale down in size, operation at higher frequency is desired in applications where compact packaging is needed. Hence, it is important for devices operating at high frequencies to have short switching times.

Along with fast switching times, high V_{BD} and low R_{ON} are two of the most important requirements for high-voltage switching devices. For a vertical device with a uniform doping profile, if low R_{ON} is desired, device doping-level should be increased. However, with increasing doping-level, V_{BD} decreases. Since V_{BD} is twice the integration of the doping level along the depletion region, it decreases at a square rate with decreasing R_{ON} . Hence, the relation V_{BR}^2/R_{ON} given by

$$\frac{V_{BD}^2}{R_{ON}} = \frac{\epsilon \mu E_C^3}{4} \quad (1.2.1)$$

should be used to compare devices with different V_{BR} and R_{ON} [16]. The V_{BR}^2/R_{ON} term is the power device figure of merit (PDFOM) and it compares semiconductors directly from the material point of view. The BFOM also originates from this equation. However, this equation is only for a vertical device. AlGaIn/GaN HEMTs are lateral devices and the relationship between its V_{BR} and R_{ON} is given by

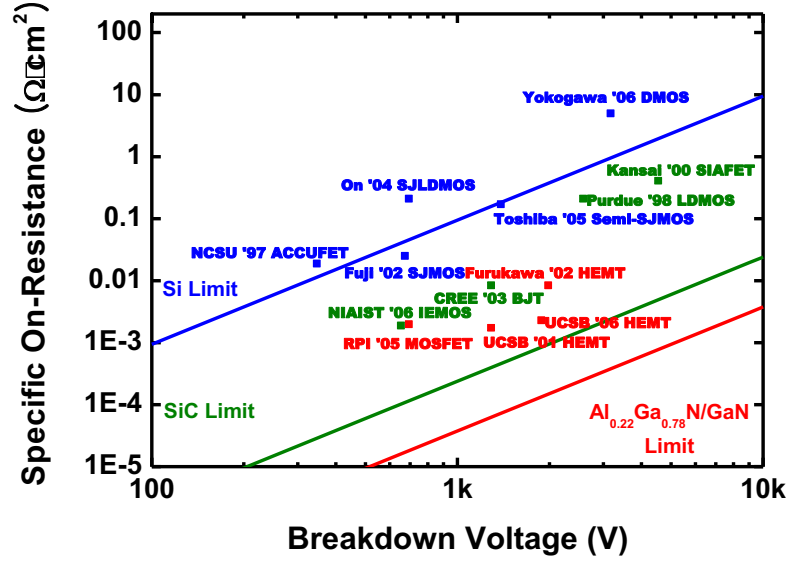


Figure 1.3: The theoretical limits of power device figure of merit (PDFOM) for Si, SiC and $\text{AlGa}_{0.22}\text{Ga}_{0.78}\text{N/GaN}$ HEMTs

$$\frac{V_{BD}^2}{R_{ON}} = q\mu n_S (E_C^2 - E_P^2) \quad (1.2.2)$$

where n_S is the 2DEG density of the channel and E_P is the polarization field [16].

1.2 Advantages of AlGaN/GaN Structure

Figure 1.3 shows the theoretical limits of PDFOM for Si, SiC and $\text{Al}_{0.22}\text{Ga}_{0.78}\text{N/GaN}$ HEMT structure. Silicon has long been the most dominant

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Figure of Merit	Si	4H-SiC	AlGaIn/GaN
JFOM	1	20	29.2
KFOM	1	4.6	1.6
BFOM	1	10.3	32.7
BHFOM	1	46.7	200
PDFOM	1	39500	251000

Table 1.2: Normalized (to Si) figure of merit of various semiconductors

semiconductor for high voltage power switching devices. However, the performances of Si-based devices are approaching the theoretical limits and in many cases, there have been demonstrations of performance beyond its material limits through novel device structures. As a result, wide bandgap materials such as SiC and GaN have attracted significant attention because they offer numerous advantages over silicon devices in the areas of switching (faster with lower losses), operating temperature, and blocking voltage.

The advantages of AlGaIn/GaN structure over SiC and Si are apparent from Figure 1.3 and the figures of merits listed in Table 1.2. HEMTs can be fabricated on AlGaIn/GaN structures to take advantage of the 2DEG at the hetero-junction. Mobilities exceeding $2200 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ can be obtained by insertion of AlN interlayers and high 2DEG densities near the $1 \times 10^{13} \text{ cm}^{-2}$ range can be realized due to polarization doping. The resulting high $n_s \cdot \mu$ product contributes to reduction of R_{ON} . The high E_C enables higher voltage operation for a given device dimensions or alternatively, enables reduction of

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device dimensions for a given operating voltage, thus reducing the R_{ON} . Although GaN has a low thermal conductivity, this problem is mainly mitigated by epitaxial growth of GaN on SiC substrates and the wide bandgap of the AlGaN/GaN structure makes high-temperature operation possible.

1.3 Research Background of GaN HEMTs for Power Switching Applications

The preliminary work on high breakdown voltage AlGaN/GaN HEMTs were done at UCSB by Zhang *et al.* where overlapping gate or field-plate technology was used to increase the V_{BD} [16]. Through their work, gate leakage was identified as the major factor limiting the V_{BD} of AlGaN/GaN HEMTs. Various gate dielectrics were implemented to achieve higher V_{BD} and reduce gate leakage. Although very high V_{BD} was achieved, devices suffered from DC-to-RF dispersion. Dora *et al.* then developed device technologies that enabled high V_{BD} and low R_{ON} without losing the large signal frequency performance [17]. In their work, multiple field-plates and different field-plate shapes were studied for high V_{BD} in dispersion-free devices. The origin of gate leakage was studied further and new gate processes were developed to minimize gate leakage with insulators and field-plates. Highly resistive

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buffers necessary for high V_{BD} were also studied and in the process, alloyed ohmic contacts were identified as another source of buffer leakage. Devices with record V_{BD} and low R_{ON} with fast switching times were developed. However, those devices were all depletion-mode devices. Achieving enhancement-mode operation, which is essential for high-voltage switching applications, was the ensuing issue that needed to be addressed.

1.4 Overview of the Dissertation

This dissertation focuses on the development of enhancement-mode AlGaIn/GaN HEMTs for high-voltage switching applications. The main objective of this work was to explore different methods of achieving enhancement-mode operation in AlGaIn/GaN HEMTs for the realization of dispersion-free, normally-off device with high V_{BD} and low R_{ON} . Through evaluation of various methods, the benefits and the limitations of each approach was identified.

Chapter 2 describes design elements of an enhancement-mode HEMT and identifies the important parameters for switching devices. The design space of gate-recessed AlGaIn/GaN HEMTs is presented. Here, the gate is recessed below the thickness of AlGaIn where no 2DEG is present (t_c). The

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results of devices fabricated by gate recessing are presented.

In chapter 3, the effects of fluorine-based plasma treatment on the AlGa_N/Ga_N heterostructure and its application to enhancement-mode devices were studied. Several treatment conditions were tried to find the appropriate treatment for enhancement-mode operation and other effects resulting from fluorine-based plasma treatment are described. The fabrication of high- V_{BD} devices with slant field-plates and its results are presented. The temperature stability of this treatment is also characterized.

In chapter 4, modification of surface barrier height by insertion of a p-GaN cap layer is described. The design space of a p-GaN capped AlGa_N/Ga_N HEMT is presented. Insertion of a thin, fully depleted p-GaN cap layer below the gate was tried to deplete the 2DEG below for enhancement-mode operation. The fabrication and the performances of high- V_{BD} devices with source-connected field-plates are presented. The design, fabrication and the performance of devices scaled to large dimensions are also presented. Performances of p-GaN capped devices were improved by using an AlN interlayer and the design space of p-GaN/AlGa_N/AlN/GaN HEMTs is also presented.

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4.1 Introduction

Enhancement-mode operation in AlGa_N/Ga_N HEMTs can also be accomplished by increasing the AlGa_N barrier height which lifts up the potential at the AlGa_N/Ga_N hetero-interface to deplete the 2DEG. Adding a p-type capping layer to an AlGa_N/Ga_N HEMT structure increases the AlGa_N barrier height and depletes the 2DEG. In addition, increasing the AlGa_N barrier height is useful for enhancement-mode devices since it also increases the gate turn-on voltage. Enhancement-mode operation in AlGa_N/Ga_N HEMTs with a p-type gate was first demonstrated by Hu *et al.* in 2000 [1]. In these devices, enhancement-mode operation was achieved by selectively regrowing p-GaN (100 nm-thick) on an AlGa_N/Ga_N structure with a SiO₂

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mask. Ohmic gate contacts were used to modulate the channel and the gate turn-on voltage of these devices were +3 V, but low channel conductance from very large gate lengths (L_G) limited the peak transconductance ($g_{m,peak}$) to 10 mS/mm. While this process was successful in shifting the V_{TH} and increasing the gate turn-on voltage, this process has several limitations and low manufacturability associated with regrowth technology.

Alternatively, Tsuyukuchi et al. [2] demonstrated a new process that avoids the regrowth process, but the device performances were limited by gate turn-on voltage of approximately +1 V which is lower than the gate turn-on voltage of normal Schottky contacts on AlGaIn/GaN HEMTs. Through the use of a p-AlGaIn cap layer, improved performances were later reported by Uemoto *et al.* [3]. These devices also used ohmic gate contacts and true enhancement-mode operation and high breakdown voltage (V_{BD}) was demonstrated. Although operation principles of these devices are slightly different due to utilization of hole injection from the p-AlGaIn to the underlying AlGaIn/GaN structure, enhancement-mode operation in these devices were achieved based on the same principle of increasing the AlGaIn barrier height.

Although true enhancement-mode operation and high V_{BD} has been demonstrated, increasing the V_{TH} of these devices, as required for high-voltage

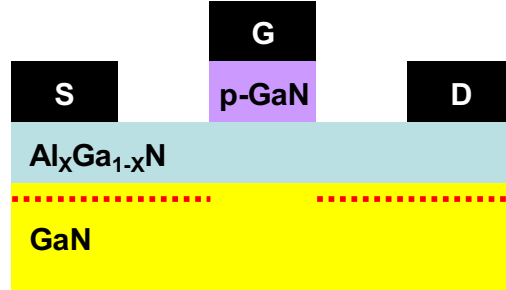


Figure 4.1: Schematic cross-section of a p-GaN capped enhancement-mode AlGaIn/GaN HEMT

switching applications, is still a difficult task. Because the gate contacts used in these devices are ohmic, gate insulators cannot be used to increase the V_{TH} . However, by using a thin, fully-depleted p-GaN cap layer with a Schottky gate contact, realization of enhancement-mode devices are possible, and V_{TH} can be increased through insertion of gate insulators. In this chapter, the design space, fabrication, and performance of AlGaIn/GaN HEMTs with a thin p-GaN capping layer are presented.

4.2 Design Space

Figure 4.1 shows the schematic cross-section of a p-GaN capped enhancement-mode AlGaIn/GaN HEMT. In order to achieve enhancement-mode operation with the addition of a p-GaN cap layer, the thickness and/or

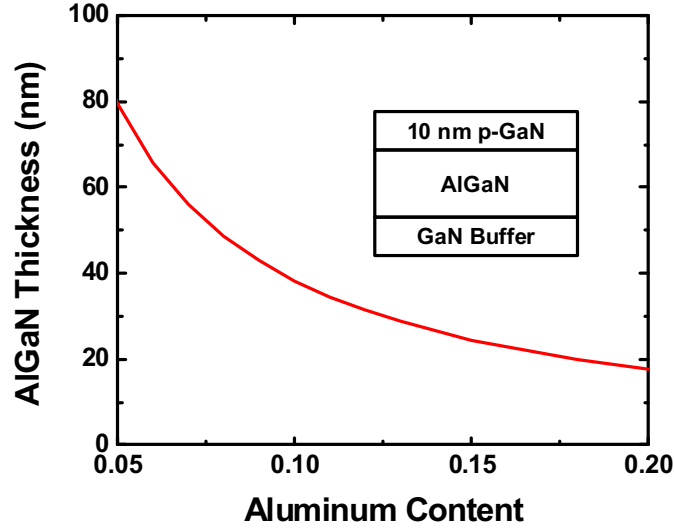


Figure 4.2: The aluminum composition of the AlGaN layer versus the t_{AlGaN} required for a V_{TH} of zero volts

the aluminum composition of the AlGaN layer has to be carefully designed since the 2DEG density that can be depleted by a p-GaN cap layer is limited. Given a p-GaN/AlGaN/GaN structure, the thickness of AlGaN (t_{AlGaN}) needed to remove all of the 2DEG (for V_{TH} of zero volts) is given by

$$t_{AlGaN} = \frac{\frac{\epsilon\epsilon_0}{q}\phi_B}{\sigma_{AlGaN/GaN}} \quad (4.2.1)$$

where $\sigma_{AlGaN/GaN}$ is the net polarization charge density at the AlGaN/GaN interface, and ϕ_B is the surface barrier height of the p-GaN. This equation assumes that the band-bending in the thin p-GaN layer and the distance of

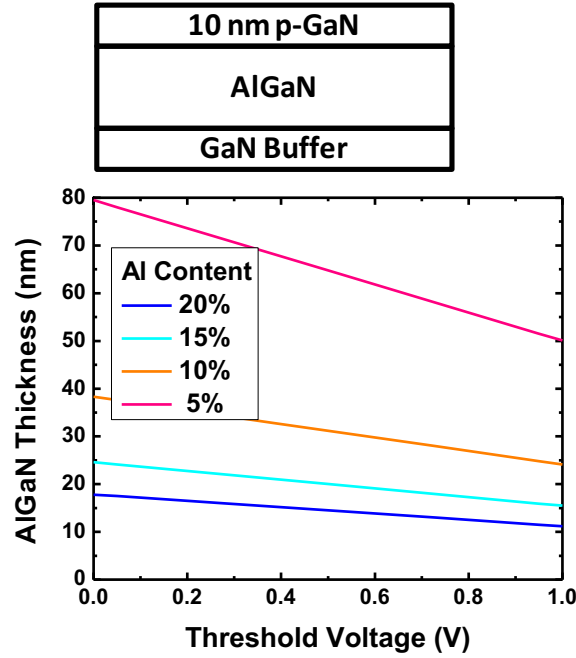


Figure 4.3: The V_{TH} versus the required t_{AlGaIn} for p-GaN capped AlGaIn/GaN HEMTs

2DEG from the AlGaIn/GaN interface is negligible. Equation 4.2.1 can be modified to

$$t_{AlGaIn} = \frac{\frac{\epsilon_0}{q} \phi_B V_{TH}}{\sigma_{AlGaIn/GaN}} \quad (4.2.2)$$

to calculate the t_{AlGaIn} needed to achieve a given V_{TH} .

Figure 4.2 shows the aluminum composition of the AlGaIn layer versus the t_{AlGaIn} required for a V_{TH} of zero volts in p-GaN/AlGaIn/GaN structures.

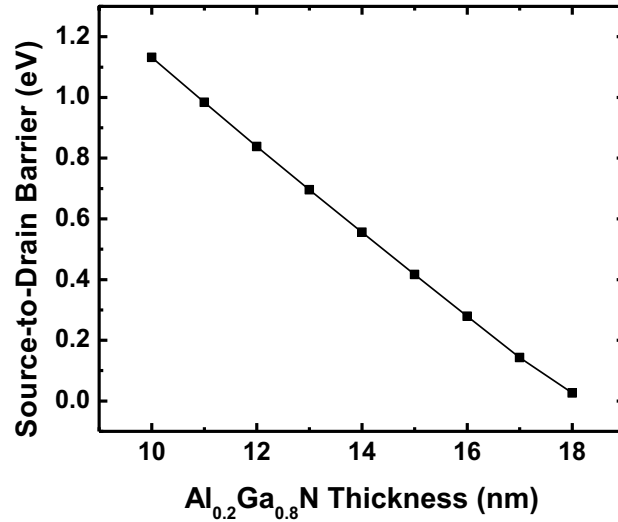


Figure 4.4: The source-to-barrier height of p-GaN capped Al_{0.2}Ga_{0.8}N/GaN HEMTs with and without an AlN interlayer

The p-GaN layer was 10 nm-thick and Schottky barrier height of 2.7 eV was used [4]. Compared to the t_{AlGaN} needed to deplete the 2DEG in gate-recessed structures (Figure 2.3), the 2DEG in p-GaN capped structures can be depleted with much thicker AlGaN layers.

Figure 4.3 shows the dependence of t_{AlGaN} on the V_{TH} for various aluminum compositions. Although V_{TH} as high as +2 V can be obtained with thinner AlGaN layers, it is important to keep in mind that the t_{AlGaN} in the access regions are the same as the gate region. Hence, increasing the V_{TH} by decreasing the AlGaN thickness comes at the cost of decreasing 2DEG charge

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in the access regions. In order to obtain a V_{TH} of +0.5 V in p-GaN capped AlGaIn/GaN HEMTs, approximately 14.5 nm-thick AlGaIn layer is needed. At this thickness, 2DEG density of approximately $5 \times 10^{12} \text{ cm}^{-2}$ can be obtained in the access regions (Figure 2.2).

As shown in Figure 4.4, the source-to-drain barrier height of p-GaN capped $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$ HEMTs can reach as high as 1 eV. Although raising the barrier height comes at the cost of decreasing 2DEG charge in the access regions, the source-to-drain barrier that can be obtained with p-GaN cap layers are much higher than the barrier heights that can be obtained in gate-recessed devices (Figure 2.7). Hence, lower off-state leakage is expected from p-GaN capped AlGaIn/GaN HEMTs and operation at high temperatures should be possible.

4.3 Device Fabrication

The p-GaN/AlGaIn/GaN structures studied in this work was grown by RF plasma-assisted molecular beam epitaxy (MBE) on semi-insulating 4H-SiC. The structure consisted of 40 nm-thick AlN nucleation layer followed by a carbon-free, 0.6 μm -thick unintentionally doped (UID) GaN buffer. The cap consisted of 12 nm of UID AlGaIn followed by 10 nm GaN:Mg doped at a

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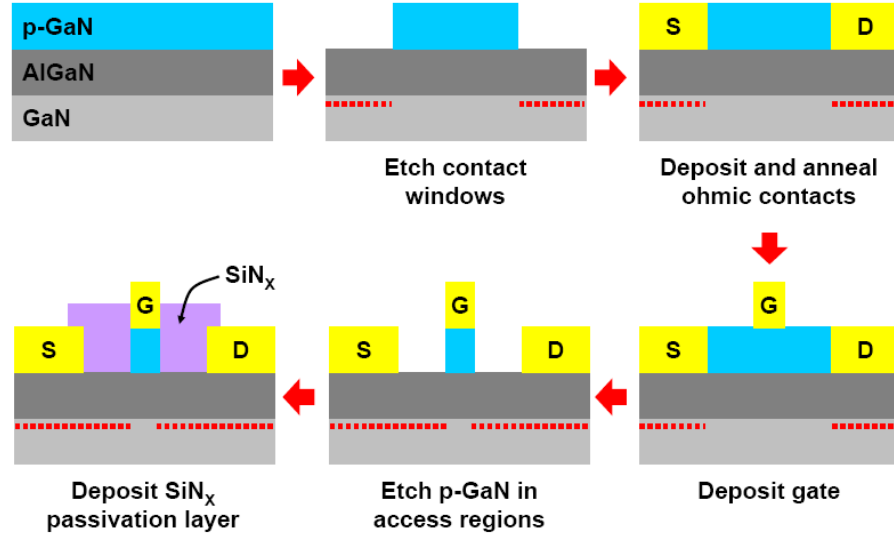


Figure 4.5: Process flow of p-GaN/AlGaN/GaN HEMTs

level of $1 \times 10^{18} \text{ cm}^{-3}$. The aluminum compositions of the AlGaN layer were 19, 22, and 25%. The MBE growth was optimized for low buffer leakage utilizing N-rich AlN growth conditions during nucleation [5] and for uniformity utilizing a modulated gallium flux during growth [6]. The cap layers were grown in the Ga-droplet regime to suppress the formation of inversion domains in the GaN:Mg layer [7]. The absence of inversion domains was confirmed by atomic force microscopy.

The source and drain ohmic contacts were formed by depositing Ti/Al/Ni/Au (20/120/30/50 nm) multilayer ohmic stack and annealing at 870 °C for 30 seconds in a N₂ atmosphere. Prior to the deposition of the ohmic

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stack, a low-power BCl_3/Cl_2 -based dry etch was used to remove the p-GaN layer below the contacts. Devices were then isolated using a Cl_2 -based mesa etch. The ohmic contact resistance was typically measured to be between 0.2 and 0.4 $\Omega\cdot\text{mm}$ by transfer length measurements (TLM). Schottky gate contacts were formed by depositing Ni/Au/Ni (30/250/50 nm) multilayer stack. Using the gate contacts and ohmic contacts as self-aligned etch masks, the p-GaN in the access regions were etched away by low-power BCl_3/Cl_3 -based dry etch. SiN_x passivation layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) to eliminate DC-to-RF dispersion. Finally, contact pad windows were formed by etching the SiN_x with CF_4 plasma. The process flow is shown in Figure 4.5. The detailed process procedures are in Appendix C.

4.4 Device Performance

The DC current-voltage characteristics and the gate-transfer characteristics (in linear and log scale) of the p-GaN capped device with 19% aluminum composition at V_{DS} of 5 V are shown in Figure 4.6. The source-to-gate distance (L_{SG}) was 1 μm and the gate length (L_G) was 2 μm . The gate-to-

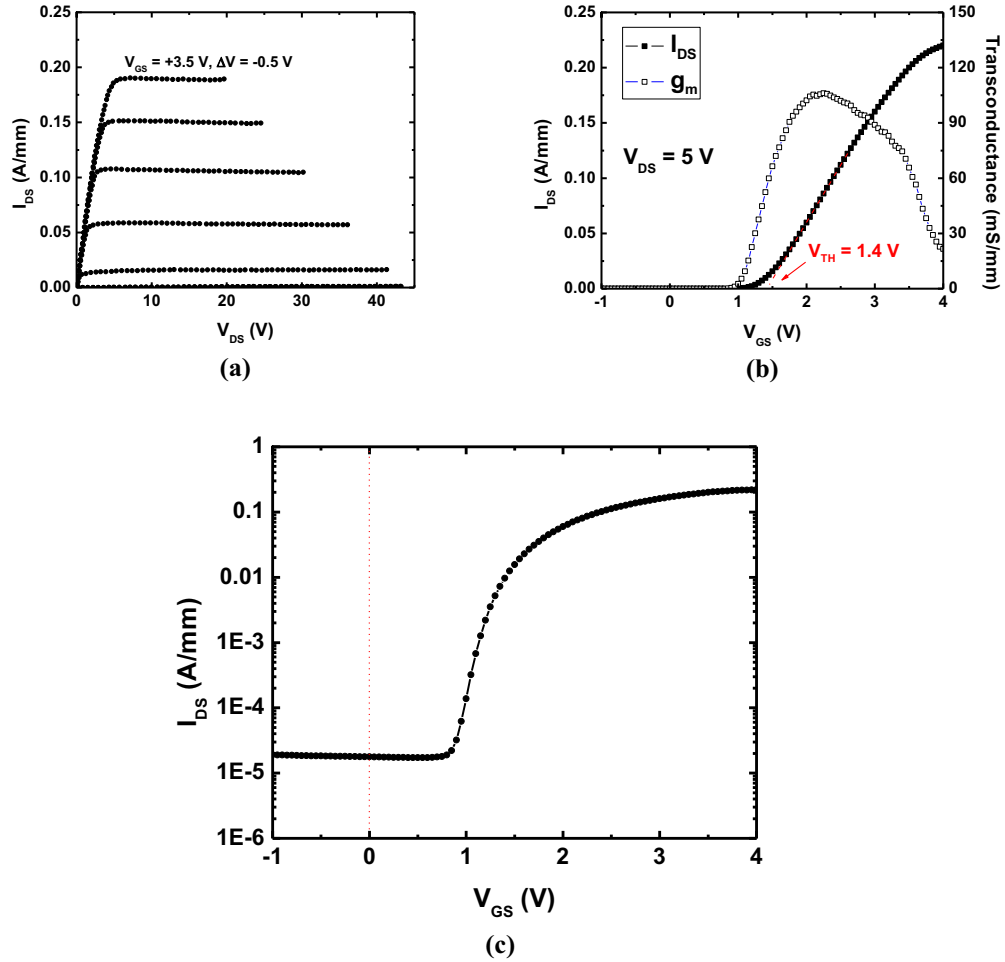


Figure 4.6: (a) The DC current-voltage characteristics, (b) the gate-transfer characteristics of the p-GaN capped device with 19% aluminum composition at V_{DS} of 5 V, in linear and (c) log scale

drain spacing (L_{GD}) was 5 μm and the gate width (W_G) was $2 \times 75 \mu\text{m}$. The device exhibited a peak transconductance ($g_{m,peak}$) of 105 mS/mm at V_{GS} of 2.3 V. The device exhibited true enhancement-mode operation with a V_{TH} of +1.4 V. Due to the increased surface barrier height, the gate turn-on voltage

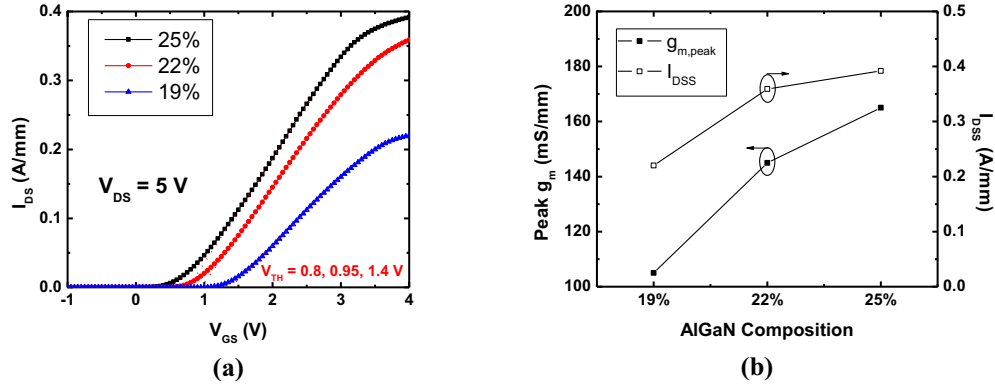


Figure 4.7: The V_{TH} , $g_{m,peak}$, and I_{DSS} of devices with different aluminum compositions

increased and the maximum gate voltage increased to +3.5 V. The device exhibited I_{DS} of approximately 0.2 A/mm.

Figure 4.7 compares the V_{TH} , $g_{m,peak}$, and I_{DSS} of devices with different aluminum compositions. True enhancement-mode operation was observed in all three samples, and as expected, the sample with 19% aluminum composition exhibited the highest V_{TH} of 1.4 V but exhibited the lowest $g_{m,peak}$ and I_{DSS} . The sample with 25% aluminum composition exhibited the lowest V_{TH} of 0.8 V but exhibited the highest $g_{m,peak}$ and I_{DSS} .

Figure 4.8 shows the DC and 80 μ s-pulsed current-voltage characteristics of a device fabricated on the sample with 19% aluminum composition. Despite deposition of SiN_x passivation layer, the device exhibited significant current collapse at 80 μ s. This behavior was seen in all of

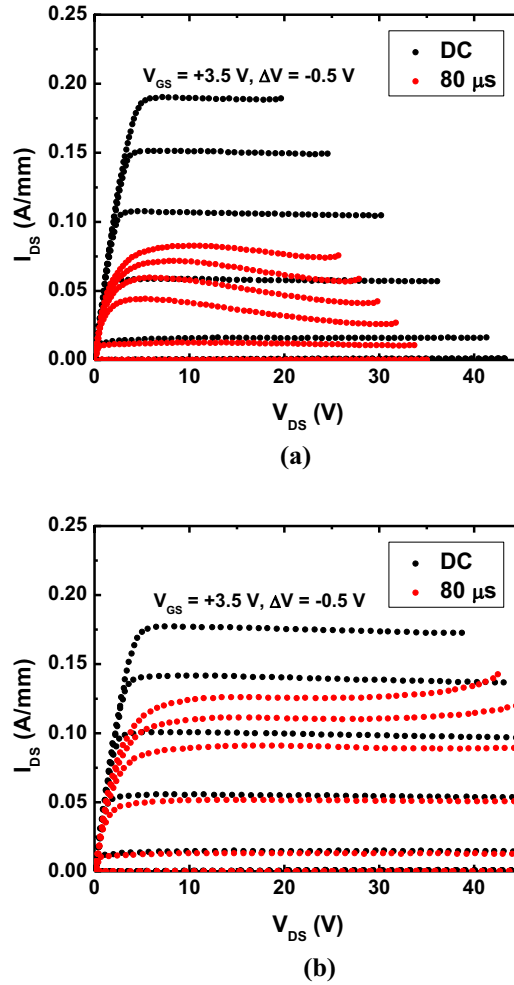


Figure 4.8: The DC and 80 μ s-pulsed current-voltage characteristics of the device fabricated on the 22% sample (a) without and (b) with source connected field-plates

the samples used for this study. If the source of dispersion was on the drain-side of the gate, the knee voltage should have walked out. Typically, dispersion without knee-walkout stems from the source side or from below the gate [8]. Preliminary investigation via current-deep-level-transient-

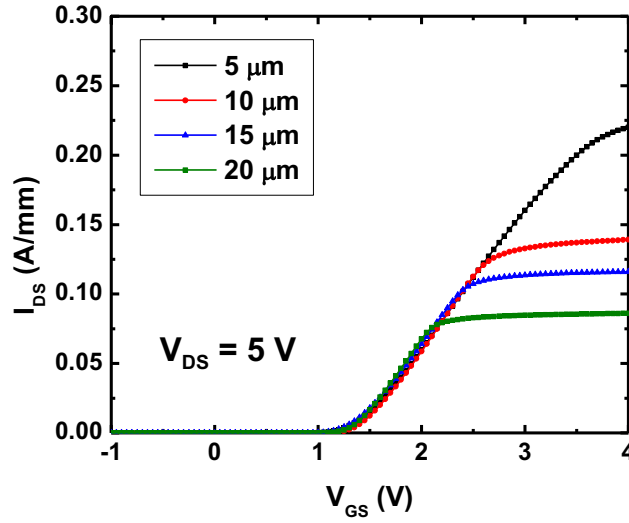


Figure 4.9: Gate-transfer characteristics of devices fabricated on the sample with 19% aluminum composition with different L_{GD} spacing

spectroscopy (I-DLTS) [9] indicated that the presence of two different hole-traps at the p-GaN/AlGaN interface may be contributing to dispersion. The energy levels of these traps were +0.11 eV and +0.26 eV relative to the p-GaN valence-band edge. However, the dispersion was partially alleviated by adding source-connected field-plates to these devices. In some devices, the dispersion at 80 μs was almost completely alleviated. If the source of the dispersion was beneath the gate, the addition of a source-connected field-plate should have had no effect. Further investigation is needed to determine the cause of this dispersion. The length of the field-plate (L_{fp}) was 2 μm .

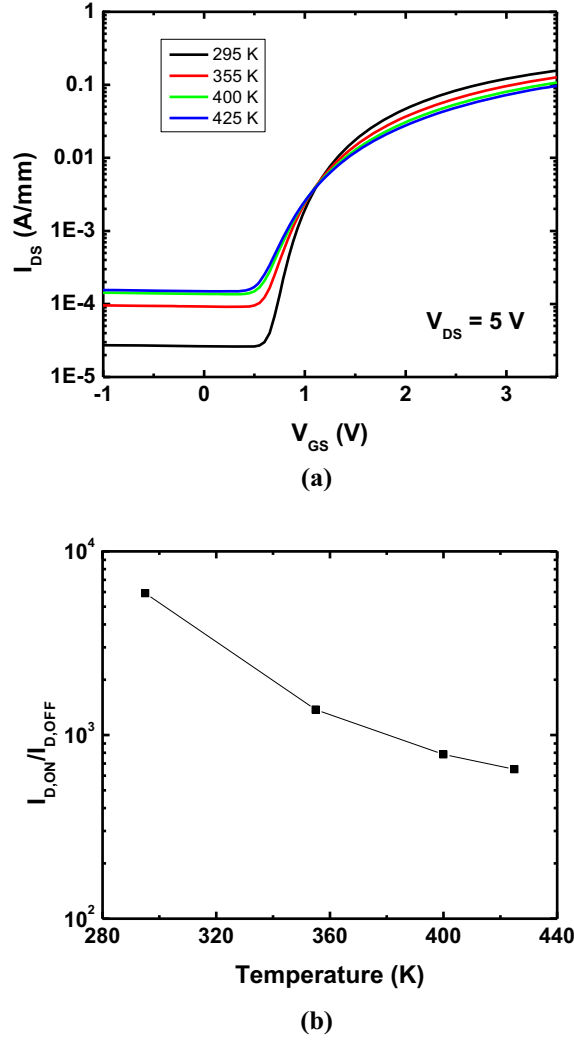


Figure 4.10: (a) Gate-transfer characteristics of the device fabricated on the 22% sample at different temperatures and (b) the on-to-off ratio of drain currents

Figure 4.9 shows the gate-transfer characteristics of devices fabricated on the sample with 19% aluminum composition with different L_{GD} values. Due to low 2DEG charge in this sample (approximately $4 \times 10^{12} \text{ cm}^{-2}$), the drain

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currents at V_{GS} of 5 V decreased significantly with increasing L_{GD} . This translates to high R_{ON} in devices with large L_{GD} required for high V_{BD} .

Figure 4.10a shows the gate-transfer characteristics of the device fabricated on the sample with 22% aluminum composition at different temperatures. The device with L_{GD} of 5 μm was initially tested at room temperature (295° K) and heated on a thermal chuck. As shown in Figure 4.10b, the drain current on-to-off ratio (at +3.5 and 0 V) decreased significantly with increasing temperature. At 425° K, the on-to-off ratio decreased almost by an order of magnitude. This indicates the importance of good heat-sinking and high source-to-drain barrier.

4.5 Large Periphery Devices

High-voltage switching devices are operated in the linear region during the on-state. Thus, devices are typically operated at a third or quarter of its maximum current levels. To achieve devices capable of switching large currents, large periphery devices capable of handling twice or three times the switching current are needed. In order to maximize on-wafer device area, large periphery devices are typically laid out with inter-digitated multi-finger

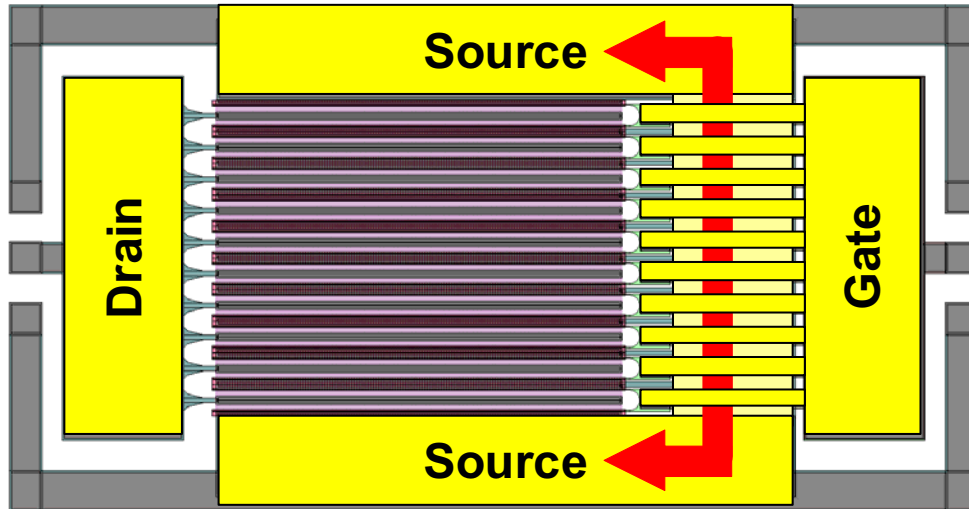


Figure 4.11: The mask layout of the 20×1 mm-wide device

geometries with air-bridges or dielectric-assisted-bridges connecting the gate fingers to a larger pad located away from the active area. In order to test large current switching capabilities of p-GaN capped devices, 20×1 mm-wide device was designed and fabricated.

The mask layout of the 20×1 mm-wide device is shown in Figure 4.11. The pads were designed to accommodate ground-signal-ground (GSG) coplanar probes for various on-wafer tests. The drain fingers were directly connected to the large pad and the source fingers were connected to the large pads on the two sides of the device through a bus (path shown with the red arrow). The gate fingers were connected to the gate pad with a dielectric-assisted bridge over the source bus (Figure 4.12). Photosensitive

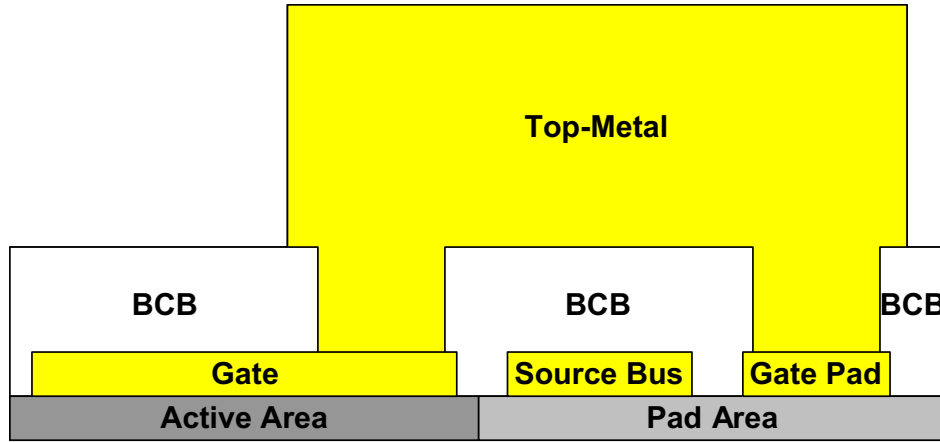


Figure 4.12: Schematic cross-section of the dielectric-assisted bridge between the gate fingers and the gate pad

benzocyclobutene-based (BCB) dielectric was spun on the wafer and vias to the gate fingers/pad were patterned by photolithography. The BCB dielectric was developed and cured in a vacuum oven.

A Ti/Au (30 nm/2 μm) top-metal stack was deposited and lifted off using a triple-layer PMGI process. The top-metal stack was deposited with the sample angled and rotating to ensure complete coverage of the sidewalls. The details of bridge processing are presented in Appendix C. The fabricated device is shown in Figure 4.13. The device had a L_{GS} of 1 μm , L_G of 2 μm , and L_{GD} of 15 μm . The device also had a 2 μm -long source-connected field plate. The DC and 80 μs -pulsed current-voltage characteristics of the large periphery device fabricated on the sample with 19% aluminum composition

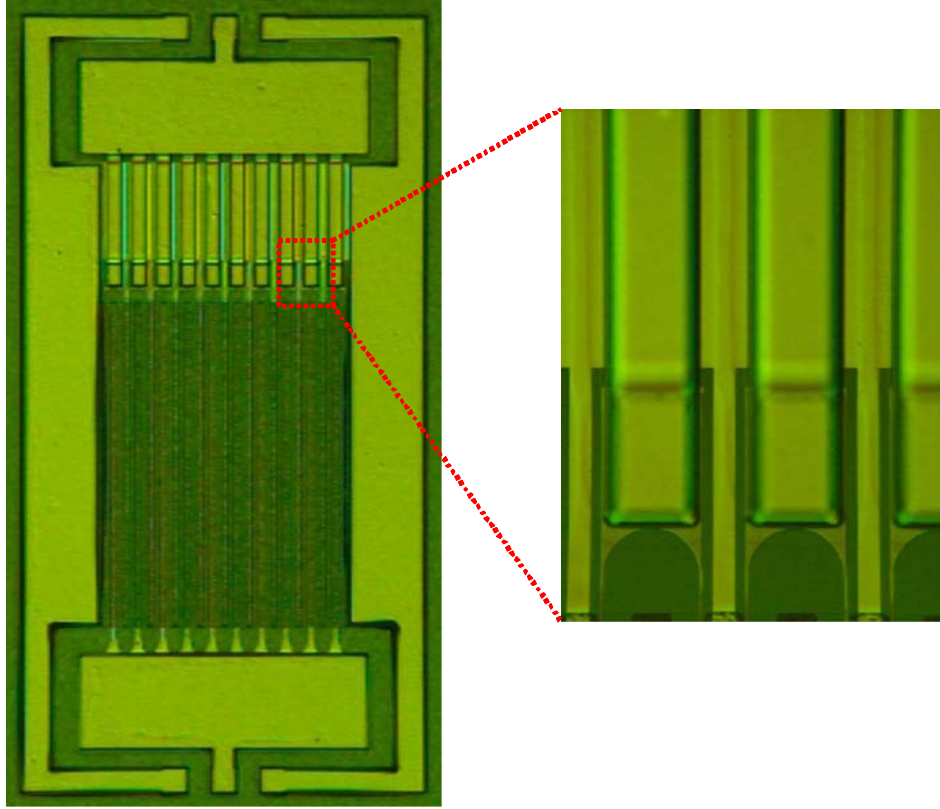


Figure 4.13: Microscope image of the fabricated 20× 1 mm-wide device

are shown in Figure 4.14. Unlike the earlier devices, the large device showed no dispersion at 80 μm . The I_{DS} of the device was approximately 2 A or 100 mA/mm with +3.5 V on the gate.

Even in 2×75 μm -wide devices, similar current densities were observed, indicating good scaling with multiple 1 mm-wide gate fingers. However, this current density was approximately half of the current densities observed in 2×75 μm -wide devices prior to the BCB bridge process. Stress caused by the

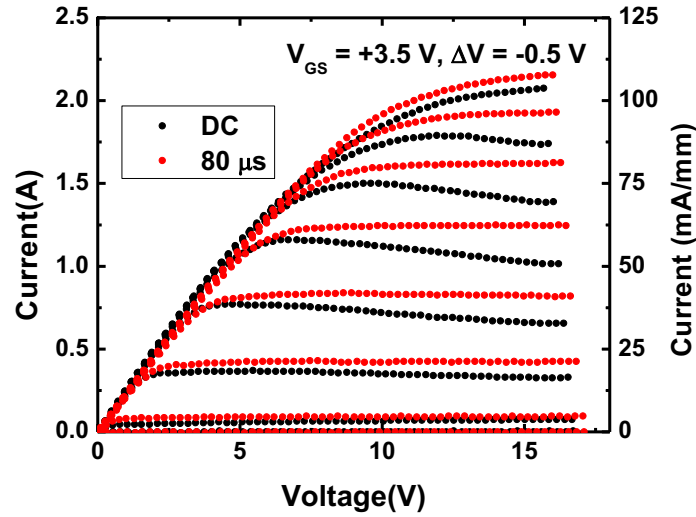


Figure 4.14: The DC and 80 μ s-pulsed current-voltage characteristics of the large periphery device

BCB layer may be the cause of this degradation, but further investigation is needed to resolve this issue.

The results of on-wafer 12 μ s-switching measurements with a resistive load ($R_L = 100 \Omega$) are shown in Figure 4.15. Devices at V_{DS} of 50 to 100 V (in 10 V steps) were switched from 0 V to +3 V. The details of the switching measurement setup are located in Appendix B. The on-resistances of these devices were calculated from the average on-state voltage and average on-state current switched from each off-state V_{DS} values. These values were much higher than the on-resistance calculated from the DC current-voltage

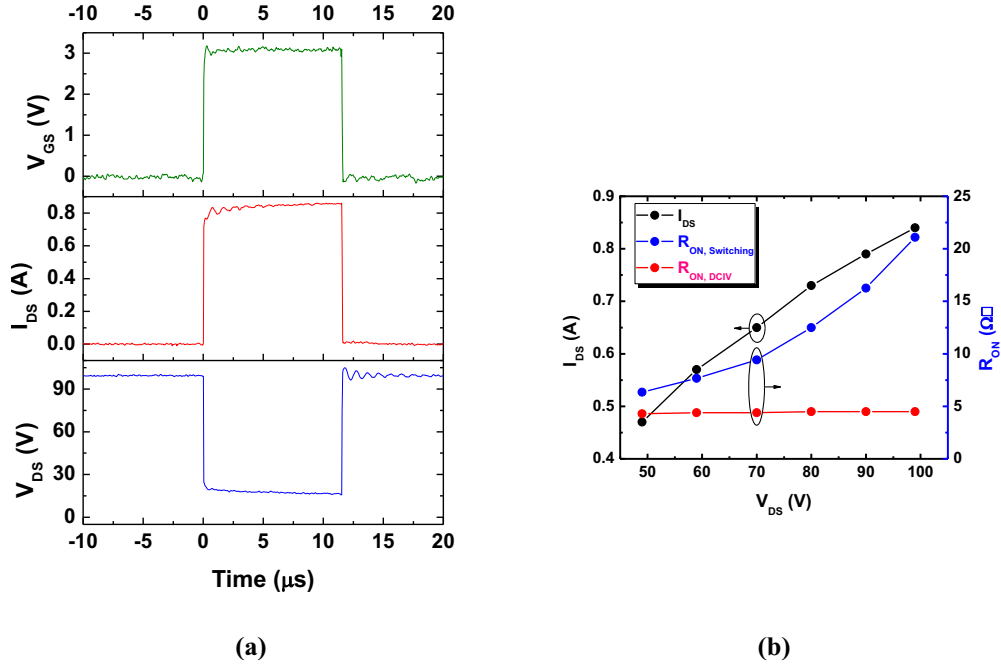


Figure 4.15: (a) On-wafer switching measurements with a load resistance of 100 Ω at V_{DS} of 100 V and (b) I_{DS} and on-resistance vs. $V_{DS, \text{off}}$

characteristics and the differences increased at higher voltages. Although dispersion was not observed at 80 μs -pulsed measurements, this indicates presence of dispersion but the true cause is still unclear. Accurate switching times could not be measured because the switching speed of the device was limited by gate-drive circuit, which had a rise time of approximately 40 ns. As shown in Figure 4.17, the large-periphery device showed V_{BD} of 800 V and R_{ON} of 4.3 Ω (1 A at 4.3 V). Based on an active area (footprint excluding large pads) of 0.8 $\times$ 1 mm, the specific on-resistance of the device was 34.4 $\text{m}\Omega\cdot\text{cm}^2$.

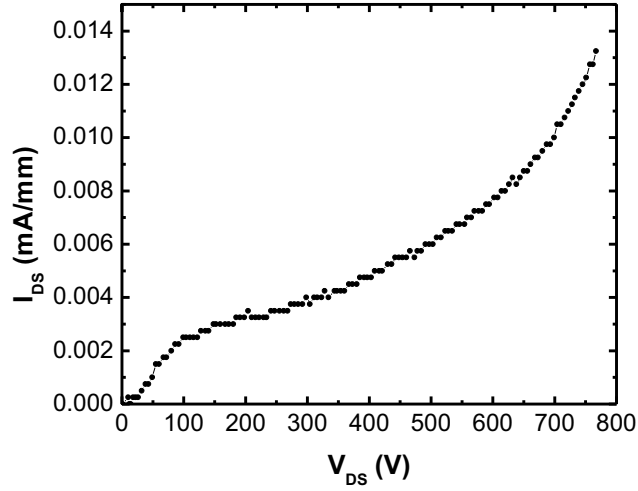


Figure 4.17: DC breakdown characteristic of the 20 mm-wide device

4.6 Evaluating the Use of an AlN Interlayer

Because increasing the V_{TH} in a p-GaN capped device comes at the cost of decreasing the 2DEG density, increasing the 2DEG density and mobility is extremely important. The use of an AlN interlayer in AlGaN/GaN HEMTs increases the 2DEG density and mobility. Alternately, with an AlN interlayer, the same 2DEG density can be obtained with thinner AlGaN caps. With a thinner AlGaN layer, the p-GaN capping layer can deplete more charge due to increased gate capacitance. Hence, realization of enhancement-mode

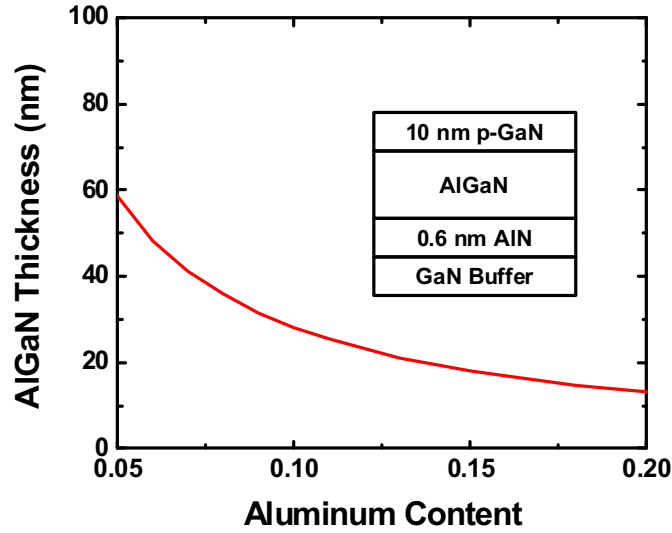


Figure 4.18: The aluminum composition of the AlGaN layer versus the t_{AlGaN} required for a V_{TH} of zero volts

operation should be possible with more charge and higher mobility by implementing an AlN interlayer.

With the insertion of an AlN interlayer, the t_{AlGaN} required for a given V_{TH} is given by

$$t_{AlGaN} = \frac{\frac{\epsilon\epsilon_0}{q}(\phi_B - V_{TH}) - t_{AlN}\sigma_{AlN/GaN} - t_p(\sigma_{AlN/GaN} - \sigma_{AlN/AlGaN} - \sigma_{AlGaN/GaN})}{\sigma_{AlN/GaN} - \sigma_{AlN/AlGaN}} \quad (4.6.1)$$

where t_{AlN} is the thickness of the AlN interlayer and t_p is the thickness of the p-GaN layer. Figure 4.18 shows the aluminum composition of the AlGaN layer

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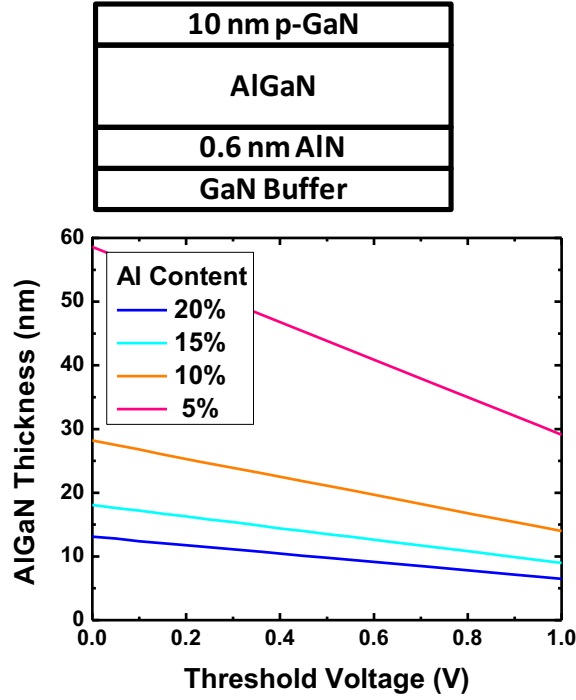


Figure 4.19: The V_{TH} versus the required t_{AlGaIn} for p-GaN capped AlGaIn/GaN HEMTs with an AlN interlayer

versus the t_{AlGaIn} required for a V_{TH} of zero volts in p-GaN/AlN/AlGaIn/GaN structures. The AlN interlayer was 0.6 nm-thick and the p-GaN layer was 10 nm-thick. Schottky barrier height of 2.7 eV was used again. Compared to the t_{AlGaIn} needed to deplete the 2DEG in gate-recessed structures (Figure 2.3), the 2DEG in p-GaN capped structures with AlN interlayer can be depleted with reasonable AlGaIn thicknesses. Figure 4.19 shows the dependence of t_{AlGaIn} on the V_{TH} for various aluminum compositions. In order to obtain a V_{TH} of +0.5 V

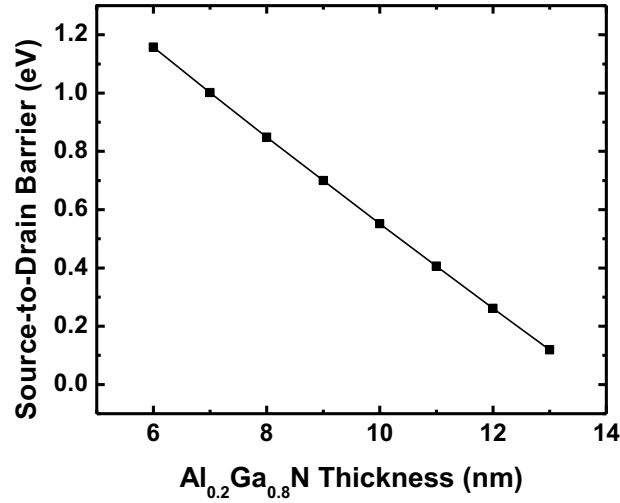


Figure 4.20: The source-to-barrier height of p-GaN capped Al_{0.2}Ga_{0.8}N/GaN HEMTs with an AlN interlayer

in p-GaN capped HEMTs with an AlN interlayer, a 9.7 nm-thick AlGa_{0.2}N layer is needed. At this thickness, 2DEG density of $7 \times 10^{12} \text{ cm}^{-2}$ (20% increase) can be obtained the access regions (Figure 2.2). As shown in Figure 4.20, similar source-to-drain barrier heights can be obtained with the insertion of an AlN interlayer.

4.7 Device Performance (p-GaN/AlGa_{0.2}N/AlN/GaN)

The p-GaN/AlGa_{0.2}N/AlN/GaN structure studied in this work was grown by metal-organic chemical vapor deposition (MOCVD) on semi-insulating 4H-

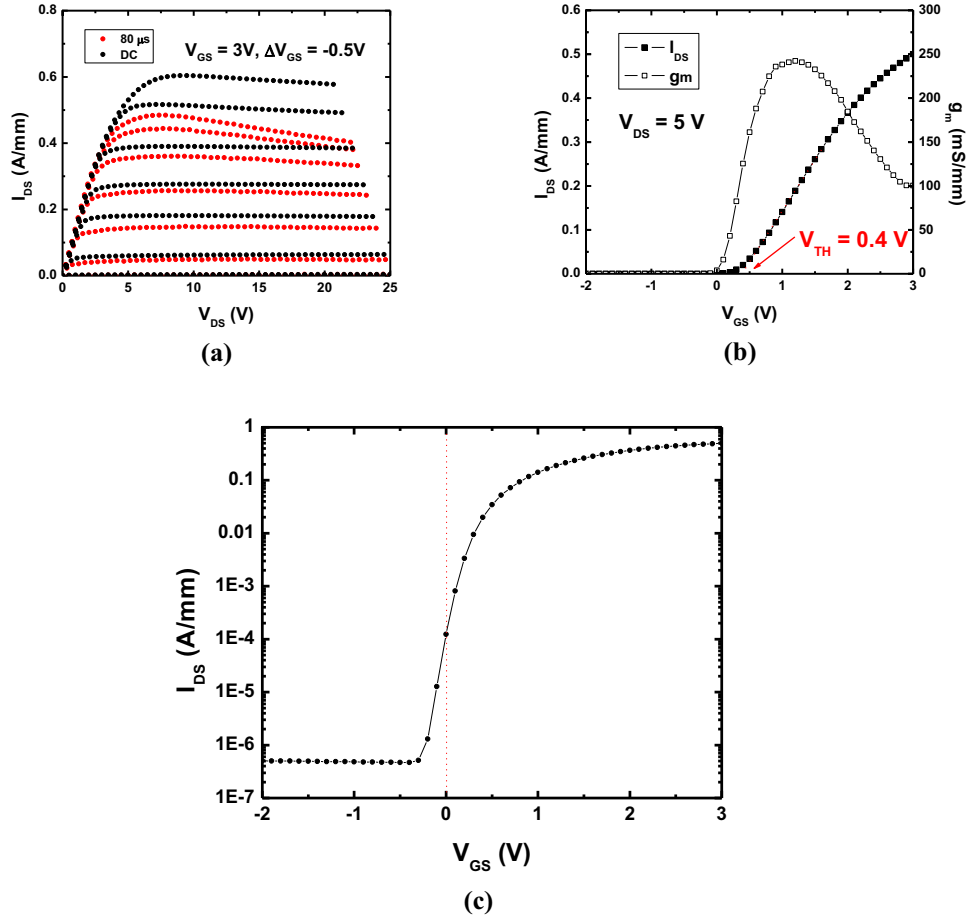


Figure 4.21: (a) The DC, 80 μ s-pulsed current-voltage characteristics, (b) the gate-transfer characteristics of the p-GaN capped device with an AlN interlayer at V_{DS} of 5 V, in linear and (c) log scale

SiC substrate. The epitaxial structure consisted of a thin AlN nucleation layer, 0.3 μ m-thick Fe-doped GaN layer, 1.4 μ m-thick undoped GaN buffer layer, 0.6 nm-thick AlN layer, 12 nm-thick $Al_{0.23}Ga_{0.77}N$ followed by 10nm-thick Mg-doped p-GaN layer. Aluminum composition of 20% was intended but

CHAPTER 4: P-GAN CAPPED DEVICES

drift in the growth resulted in a slightly higher aluminum composition (23%). The devices were fabricated using the same procedure as the samples without AlN interlayers. The L_{SG} , L_G , and L_{GD} of the device were 0.5, 0.6, and 2.3 μm respectively.

Figure 4.21 shows the DC, 80 μs -pulsed current-voltage characteristics and gate-transfer characteristics at V_{DS} of 5 V in linear and log scales. The device exhibited I_{DS} of approximately 600mA/mm at V_{GS} of +3 V and a V_{TH} of +0.4 V. At V_{GS} of +1.2 V, peak g_m of 240 mS/mm was observed. As before, dispersion was observed. Although the device had a very high on-to-off ratio (approximately 1×10^6), the device did not exhibit true enhancement-mode operation due to the unintended higher aluminum composition. Hall measurement in the access regions yielded a 2DEG density of $5.6 \times 10^{12} \text{ cm}^{-2}$ and mobility of 2160 $\text{cm}^2/\text{V}\cdot\text{s}$. The resulting sheet resistance of the access regions was 533 $\Omega/$. With a 23% aluminum composition, 2DEG density in the access regions should have been close to $8 \times 10^{12} \text{ cm}^{-2}$. The lower 2DEG density is due to over-etching of the p-GaN in the access regions to ensure complete removal. At AlGaIn thicknesses below 20 nm, the 2DEG density of an AlGaIn/AlN/GaN structure decreases significantly with decreasing AlGaIn thicknesses (Figure 2.2). Hence, in order to keep the access resistances low,

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the use of a selective etch is necessary to ensure complete removal of the p-GaN without etching the AlGaN.

4.8 Summary and Conclusion

The design space of p-GaN/AlGaN/GaN enhancement-mode HEMTs was presented. Through the use of a fully-depleted thin p-GaN cap layer and Schottky gate contacts, true enhancement-mode devices were fabricated. Large periphery devices packaged in TO-220-style packages exhibited maximum current of 2 A, V_{BD} of 800 V and R_{ON} of 4.3 Ω (1 A at 4.3 V). Presence of dispersion was observed in pulsed current-voltage and switching measurements. I-DLTS measurements identified hole-traps at the p-GaN/AlGaN interface as possible cause of these traps but contradicting results were observed during pulsed current-voltage measurements of field-plated devices.

While further investigation is necessary to determine the cause and remedy for dispersion in these devices, device design and back-end processing also need to be improved for lower R_{ON} . Feasibility of using an AlN interlayer, for higher 2DEG density and mobility, was confirmed and the design space of p-GaN/AlGaN/AlN/GaN HEMTs was also presented. Higher 2DEG density

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and mobility were observed in the fabricated devices, but due to drift in aluminum conditions, devices exhibited current flow at V_{TH} of zero volts. Nonetheless, the use of an AlN interlayer was identified as a path to lower R_{ON} .

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Conclusions and Future Work

5.1 Conclusions

The work presented in this dissertation dealt with the development of enhancement-mode AlGaIn/GaN HEMTs for high-voltage switching applications. Different methods of achieving enhancement-mode operation in AlGaIn/GaN HEMTs were explored for the realization of dispersion-free, normally-off device with high V_{BD} and low R_{ON} .

The design space of gate-recessed AlGaIn/GaN HEMTs was presented. In order to obtain enhancement-mode devices with sufficiently large 2DEG density in the access regions, it was found very thin AlGaIn barriers are needed below the gate. Moreover, AlN interlayers cannot be used because the required AlGaIn thicknesses become too thin. Devices with positive threshold

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

voltages were fabricated by dry-etching the AlGa_N layer below the gate contact but devices still exhibited some current flow with zero volts on the gate. While it is possible to eliminate the current flow at zero volts with more aggressive gate-recessing, the lack of an etch-stop layer and relatively low source-to-drain barriers make this approach unattractive.

The effects of CF₄-based plasma treatment on AlGa_N/Ga_N HEMT structures were studied. Decrease in 2DEG densities and positive-shift in threshold voltages were observed due to etching of the AlGa_N and presumably implantation of negatively charged fluorine ions. Reduction of gate leakage and increase in gate turn-on voltage was also observed after the plasma treatment. True enhancement-mode operation and record breakdown voltages were observed with integration of slant field-plates, but negative-shift in threshold voltages were observed at moderately high temperatures indicating escape or redistribution of fluorine ions.

The design space of a p-Ga_N capped AlGa_N/Ga_N HEMTs were presented. Through the use of a fully-depleted thin p-Ga_N cap layer and Schottky gate contacts, true enhancement-mode devices were fabricated. The use of an AlN interlayer for higher 2DEG density and mobility in the access regions was demonstrated. The device performances were limited by dispersion and large-periphery devices with BCB-based dielectric-assisted

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

bridges showed degradation of DC performances. Exact causes of these effects are still unclear.

5.2 Future Work (p-GaN Capped Devices)

The exact cause(s) and remedy for the dispersion in p-GaN capped devices needs to be investigated. If the dispersion can be eliminated, p-GaN capped devices with AlN interlayers have the potential to deliver enhancement-mode devices with low on-resistances and breakdown voltages beyond the limits of Si and SiC. The p-GaN cap layer in the access regions need to be etched away using the selective etch [1] to maximize the charge in the access regions. Due to the self-aligned process of access-region etch, the slant field-plate process can not be applied to p-GaN capped devices. Hence, optimization of the field-plate(s) (gate-connected, source-connected, and combination) is needed to maximize breakdown voltages. Another factor that limits breakdown voltages is leakage at the mesa side-walls/gate-metal interface. This leakage typically occurs after the deposition of SiN_x passivation layer. Through the use of implant isolation, this leakage can be reduced significantly. In the next generation of devices, implant isolation should be used.

5.3 Future Work (N-Polar HEMTs)

Due to the reversed direction of polarization in N-polar GaN, new device structures, including new enhancement-mode devices that offer superior performances are possible [2]. Opposite to structures grown in Ga-polar direction, increasing the AlGaN cap in structures grown in the N-polar direction depletes the channel charge. This allows a more robust enhancement-mode device with a relatively thick AlGaN barrier between the channel and the gate electrode. Additionally, devices with higher source-to-barrier height are possible, enabling operation at higher temperatures. Although Ga-polar devices currently dominate the research industry, interest in N-polar devices should increase in the light of recent breakthroughs in N-polar growth technology [3].

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

References

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E-mode Slant Field-Plate Process Procedures

Ohmic Contacts

- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 2. Double Layer PR Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply HMDS directly on the sample and wait 20 sec
 - 30 sec spin at 5 krpm
 - Apply OCG825
 - 30 sec spin at 5 krpm
 - 60 sec bake at 95 °C
 - 60 sec cool
 - Apply SPR950-0.8
 - 30 sec spin at 3.5 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool

APPENDIX A: E-MODE SLANT FIELD-PLATE PROCESS PROCEDURES

3. Ohmic Layer Lithography (Autostep200)

0.675 sec exposure
120 sec post-exposure bake at 100 °C
100 sec develop (MF701:DI 2:1)
60 sec DI rinse
15 sec descum (100 W O₂ plasma at 300mT)
60 sec DI rinse
60 sec oxide removal (HCl:DI 1:3)
60 sec DI rinse

4. Ohmic Metal Deposition (E-Beam#4)

15 sec descum (100 W O₂ plasma at 300mT)
60 sec DI rinse
60 sec oxide removal (HCl:DI 1:3)
60 sec DI rinse
Deposit Ti/Al/Ni/Au (20/120/30/50 nm)
5 min soak in Acetone and blow off metal with pipette
3 min Acetone soak in ultrasonic bath (face down/tilted)
3 min Acetone soak in ultrasonic
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse

5. Alloying Step (RTA)

30 sec anneal at 870 °C under N₂ atmosphere

APPENDIX A: E-MODE SLANT FIELD-PLATE PROCESS PROCEDURES

Device Isolation

- 1. Standard Solvent Clean**
3 min Acetone soak in ultrasonic bath
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse
- 2. PR Spin**
3 min dehydration bake at 120 °C
1 min cool
Apply HMDS directly on the sample and wait 20 sec
Apply SPR950-0.8
30 sec spin at 3.5 krpm
60 sec bake at 90 °C
60 sec cool
- 3. Mesa Etch (RIE#5)**
15 sec descum (100 W O₂ plasma at 300mT)
1 min sample etch (100 W BCl₃ 10 sccm at 5 mT)
2 min chamber etch (100 W Cl₂ 10 sccm at 5 mT)
- 4. Standard Solvent Clean**
3 min Acetone soak in ultrasonic bath
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse

APPENDIX A: E-MODE SLANT FIELD-PLATE PROCESS PROCEDURES

Passivation

1. Standard Solvent Clean

- 3 min Acetone soak in ultrasonic bath
- 3 min Isopropanol soak in ultrasonic bath
- 1 min DI water rinse

2. SiN_x Deposition

- CHIN_A01 chamber clean (use CHIN_A14 if the chamber is dirty)
- 15 sec descum (100 W O₂ plasma at 300mT)
- 60 sec DI rinse
- 60 sec oxide removal (HCl:DI 1:3)
- 60 sec DI rinse
- CHIN_A09 SiN_x deposition ($\approx$ 160 nm)

APPENDIX A: E-MODE SLANT FIELD-PLATE PROCESS PROCEDURES

Schottky Gate Contacts (Slant Gates)

- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 2. Double Layer PR Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply HMDS directly on the sample and wait 20 sec
 - 30 sec spin at 5 krpm
 - Apply OCG825
 - 30 sec spin at 5 krpm
 - 60 sec bake at 95 °C
 - 60 sec cool
 - Apply SPR950-0.8
 - 30 sec spin at 3.5 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool

- 3. Gate Layer Lithography (Autostep200)**
 - 0.675 sec exposure (0.9 sec for 0.7 µm opening from 0.5 µm pattern)
 - 120 sec post-exposure bake at 100 °C
 - 100 sec develop (MF701:DI 2:1)
 - 60 sec DI rinse
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse

APPENDIX A: E-MODE SLANT FIELD-PLATE PROCESS PROCEDURES

4. SiN_x Etch (RIE#3)

30 min chamber clean (500 V O₂ 20 sccm at 50 mT)
2 min chamber etch (100 V CF₄/O₂ 20/2 sccm at 20 mT)
15 sec descum (100 W O₂ plasma at 300mT)
60 sec oxide removal (HCl:DI 1:3)
60 sec DI rinse
14 min sample etch (100 V CF₄/O₂ 20/2 sccm at 20 mT)
15 sec descum (100 W O₂ plasma at 300mT)
60 sec DI rinse
60 sec oxide removal (HCl:DI 1:3)
60 sec DI rinse

5. Gate Metal Deposition (E-Beam#1)

Deposit Ni/Au/Ni (30/500/50 nm) with 15° angled rotation
5 min soak in Acetone and blow off metal with pipette
3 min Acetone soak in ultrasonic bath (face down/tilted)
3 min Acetone soak in ultrasonic
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse

APPENDIX A: E-MODE SLANT FIELD-PLATE PROCESS PROCEDURES

Bond Pads

- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 2. Double Layer PR Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply OCG825
 - 30 sec spin at 5 krpm
 - 60 sec bake at 95 °C
 - 60 sec cool
 - Apply SPR950-0.8
 - 30 sec spin at 3.5 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool

- 3. Bond Pad Layer Lithography (Autostep200)**
 - 0.675 sec exposure
 - 120 sec post-exposure bake at 100 °C
 - 100 sec develop (MF701:DI 2:1)
 - 60 sec DI rinse
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 3 min SiN_x etch (200 W CF₄ plasma at 300mT)
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse

- 4. Bond Pad Metal Deposition (E-Beam#3)**
 - Deposit Ti/Au (30/500 nm)
 - 5 min soak in Acetone and blow off metal with pipet
 - 3 min Acetone soak in ultrasonic bath (face down/tilted)
 - 3 min Acetone soak in ultrasonic
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse



P-GaN Cap Process Procedures

Ohmic Contacts

- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 2. Double Layer PR Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply HMDS directly on the sample and wait 20 sec
 - 30 sec spin at 5 krpm
 - Apply OCG825
 - 30 sec spin at 5 krpm
 - 60 sec bake at 95 °C
 - 60 sec cool
 - Apply SPR950-0.8
 - 30 sec spin at 3.5 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

- 3. Ohmic Layer Lithography (Autostep200)**
 - 0.675 sec exposure
 - 120 sec post-exposure bake at 100 °C
 - 100 sec develop (MF701:DI 2:1)
 - 60 sec DI rinse
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse
- 4. p-GaN Etch (RIE#5)**
 - 30 min chamber clean (200 W O₂ 50 sccm at 50 mT)
 - 2 min chamber etch (100 W BCl₃/Cl₂ 20/5 sccm at 10 mT)
 - 5 min chamber etch (15 W BCl₃/Cl₂ 20/5 sccm at 10 mT)
 - 2 min chamber etch (15 W BCl₃ 10 sccm at 10 mT)
 - 2 min sample etch (15 W BCl₃ 10 sccm at 10 mT)
 - 1 min sample etch (15 W BCl₃/Cl₂ 20/5 sccm at 10 mT)
- 5. Ohmic Metal Deposition (E-Beam#4)**
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse
 - Deposit Ti/Al/Ni/Au (20/120/30/50 nm)
 - 5 min soak in Acetone and blow off metal with pipette
 - 3 min Acetone soak in ultrasonic bath (face down/tilted)
 - 3 min Acetone soak in ultrasonic
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse
- 6. Alloying Step (RTA)**
 - 30 sec anneal at 870 °C under N₂ atmosphere

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

Device Isolation

- 1. Standard Solvent Clean**
3 min Acetone soak in ultrasonic bath
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse
- 2. PR Spin**
3 min dehydration bake at 120 °C
1 min cool
Apply HMDS directly on the sample and wait 20 sec
Apply SPR950-0.8
30 sec spin at 3.5 krpm
60 sec bake at 90 °C
60 sec cool
- 3. Mesa Etch (RIE#5)**
15 sec descum (100 W O₂ plasma at 300mT)
1 min sample etch (100 W BCl₃ 10 sccm at 5 mT)
2 min chamber etch (100 W Cl₂ 10 sccm at 5 mT)
- 4. Standard Solvent Clean**
3 min Acetone soak in ultrasonic bath
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

Schottky Gate Contacts and Access Region Etch

- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 2. Double Layer PR Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply HMDS directly on the sample and wait 20 sec
 - 30 sec spin at 5 krpm
 - Apply OCG825
 - 30 sec spin at 5 krpm
 - 60 sec bake at 95 °C
 - 60 sec cool
 - Apply SPR950-0.8
 - 30 sec spin at 3.5 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool

- 3. Gate Layer Lithography (Autostep200)**
 - 0.675 sec exposure (0.9 sec for 0.7 μm opening from 0.5 μm pattern)
 - 120 sec post-exposure bake at 100 °C
 - 100 sec develop (MF701:DI 2:1)
 - 60 sec DI rinse
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

4. Gate Metal Deposition (E-Beam#4)

Deposit Ni/Au/Ni (30/500/50 nm)
5 min soak in Acetone and blow off metal with pipette
3 min Acetone soak in ultrasonic bath (face down/tilted)
3 min Acetone soak in ultrasonic
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse
15 sec descum (100 W O₂ plasma at 300mT)
60 sec DI rinse
60 sec oxide removal (HCl:DI 1:3)
60 sec DI rinse

4. p-GaN Etch (RIE#5)

30 min chamber clean (200 W O₂ 50 sccm at 50 mT)
2 min chamber etch (100 W BCl₃/Cl₂ 20/5 sccm at 10 mT)
5 min chamber etch (15 W BCl₃/Cl₂ 20/5 sccm at 10 mT)
2 min chamber etch (15 W BCl₃ 10 sccm at 10 mT)
2 min sample etch (15 W BCl₃ 10 sccm at 10 mT)
1 min sample etch (15 W BCl₃/Cl₂ 20/5 sccm at 10 mT)

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

Passivation

1. **Standard Solvent Clean**
3 min Acetone soak in ultrasonic bath
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse

2. **SiN_x Deposition**
CHIN_A01 chamber clean (use CHIN_A14 if the chamber is dirty)
15 sec descum (100 W O₂ plasma at 300mT)
60 sec DI rinse
60 sec oxide removal (HCl:DI 1:3)
60 sec DI rinse
CHIN_A09 SiN_x deposition ($\approx$ 160 nm)

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

Bond Pads

- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 2. Double Layer PR Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply OCG825
 - 30 sec spin at 5 krpm
 - 60 sec bake at 95 °C
 - 60 sec cool
 - Apply SPR950-0.8
 - 30 sec spin at 3.5 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool

- 3. Bond Pad Layer Lithography (Autostep200)**
 - 0.675 sec exposure
 - 120 sec post-exposure bake at 100 °C
 - 100 sec develop (MF701:DI 2:1)
 - 60 sec DI rinse
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 3 min SiN_x etch (200 W CF₄ plasma at 300mT)
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse

- 4. Bond Pad Metal Deposition (E-Beam#3)**
 - Deposit Ti/Au (30/500 nm)
 - 5 min soak in Acetone and blow off metal with pipet
 - 3 min Acetone soak in ultrasonic bath (face down/tilted)
 - 3 min Acetone soak in ultrasonic
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

Source-Connected Field-Plates

- 0. Repeat Passivation and Bond Pads**
- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse
- 2. Double Layer PR Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply HMDS directly on the sample and wait 20 sec
 - 30 sec spin at 5 krpm
 - Apply OCG825
 - 30 sec spin at 5 krpm
 - 60 sec bake at 95 °C
 - 60 sec cool
 - Apply SPR950-0.8
 - 30 sec spin at 3.5 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool
- 3. Field-Plate Layer Lithography (Autostep200)**
 - 0.675 sec exposure (0.9 sec for 0.7 µm opening from 0.5 µm pattern)
 - 120 sec post-exposure bake at 100 °C
 - 100 sec develop (MF701:DI 2:1)
 - 60 sec DI rinse
 - 15 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

4. Field-Plate Metal Deposition (E-Beam#4)

Deposit Ni/Au/Ni (30/500/50 nm)
5 min soak in Acetone and blow off metal with pipette
3 min Acetone soak in ultrasonic bath (face down/tilted)
3 min Acetone soak in ultrasonic
3 min Isopropanol soak in ultrasonic bath
1 min DI water rinse
15 sec descum (100 W O₂ plasma at 300mT)
60 sec DI rinse
60 sec oxide removal (HCl:DI 1:3)
60 sec DI rinse

4. p-GaN Etch (RIE#5)

30 min chamber clean (200 W O₂ 50 sccm at 50 mT)
2 min chamber etch (100 W BCl₃/Cl₂ 20/5 sccm at 10 mT)
5 min chamber etch (15 W BCl₃/Cl₂ 20/5 sccm at 10 mT)
2 min chamber etch (15 W BCl₃ 10 sccm at 10 mT)
2 min sample etch (15 W BCl₃ 10 sccm at 10 mT)
1 min sample etch (15 W BCl₃/Cl₂ 20/5 sccm at 10 mT)

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

BCB-assisted Bridge

- 1. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 2. BCB Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply AP3000 (Cyclotene adhesion promoter)
 - 30 sec spin at 3.5 krpm
 - 120 sec bake at 110 °C
 - 60 sec cool
 - Apply Cyclotene
 - 10 sec spin at 0.5 krpm (ramp 800 rpm/sec)
 - 45 sec spin at 6 krpm (ramp 2000 rpm/sec)
 - Edge bead removal with DS2100
 - 60 sec bake at 65 °C
 - 60 sec cool

- 3. Post Layer Lithography (Autostep200)**
 - 0.55 sec exposure
 - 55 sec post-exposure bake at 55 °C
 - Spin develop (DS2100, ramp 300 rpm/sec)
 - 15 sec spin at 150 rpm (while spraying)
 - 45 sec puddle
 - 15 sec spin at 500 rpm (while spraying)
 - 30 sec spin-dry at 4000 rpm
 - 60 sec bake at 55 °C

- 4. BCB Curing (Blue Oven)**
 - Turn up N₂ to 100
 - Turn on the oven
 - Run recipe P5
 - Removed the sample after the oven has cooled (5-6 hours)
 - Turn off N₂, oven
 - 120 sec descum (200 W O₂ plasma at 300mT)

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

- 5. Standard Solvent Clean**
 - 3 min Acetone soak in ultrasonic bath
 - 3 min Isopropanol soak in ultrasonic bath
 - 1 min DI water rinse

- 6. PMGI Lift-Off Layer Spin**
 - 3 min dehydration bake at 120 °C
 - 1 min cool
 - Apply HMDS directly on the sample and wait 20 sec
 - 30 sec spin at 5 krpm
 - Apply SF15
 - 40 sec spin at 2 krpm
 - 120 sec bake at 200 °C
 - 60 sec cool
 - Apply SF15
 - 40 sec spin at 2 krpm
 - 120 sec bake at 200 °C
 - 60 sec cool
 - Apply 5214
 - 30 sec spin at 6 krpm
 - 60 sec bake at 90 °C
 - 60 sec cool

- 7. Bridge Layer Lithography (Autostep200)**
 - 0.25 sec exposure
 - 110 sec post-exposure bake at 60 °C
 - 60 sec develop (4:1 AZ400K)
 - 60 sec DI rinse
 - 300 sec Deep UV exposure
 - 60 sec develop (SAL101)
 - 60 sec DI rinse
 - Repeat DUV/101 expose/develop 4 more times
 - 60 sec descum (100 W O₂ plasma at 300mT)
 - 60 sec DI rinse
 - 60 sec oxide removal (HCl:DI 1:3)
 - 60 sec DI rinse

APPENDIX C: P-GAN CAP PROCESS PROCEDURES

8. Bridge Metal Deposition (E-Beam#1)

Load sample approximately 8 inches from the source

Deposit Ti/Au (30/500 nm) tilted and rotating

5 min soak in Acetone and blow off metal with pipette

3 min Acetone soak in ultrasonic bath (face down/tilted)

3 min Acetone soak in ultrasonic

3 min Isopropanol soak in ultrasonic bath

1 min DI water rinse

3 min 1165 soak in ultrasonic

3 min Isopropanol soak in ultrasonic bath

1 min DI water rinse