

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01381
U.S. Patent No. 8,350,294

PATENT OWNER'S PRELIMINARY RESPONSE

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37 C.F.R. § 42.107	1
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PATENT OWNER’S EXHIBIT LIST

Exhibit No.	Description
2001	Jorg Neugebauer et al., “Role of Hydrogen Complexes in Doping of GaN,” Material Research Society Symposium Proceedings, Vol. 423 (1996), pp. 619-24 (“Neugebauer-MRS1”)
2002	Jorg Neugebauer et al., “Theory of Point Defects and Complexes in GaN,” Material Research Society Symposium Proceedings, Vol. 395 (1996), pp. 645-56 (“Neugebauer-MRS2”)
2003	EPC’s Responsive Claim Construction Brief: Inv. No. 337-TA-1366, dated October 6, 2023
2004	IEEE Dictionary definition for “compensated”
2005	U.S. Patent No. 6,498,111 (“the ‘111 patent”)
2006	Translation of Innoscience’s Invalidation Request to the Chinese Patent Office for the Chinese Counterpart to the ‘294 Patent

I. INTRODUCTION

In accordance with 37 C.F.R. § 42.107, Patent Owner Efficient Power Conversion Corporation (“EPC” or “Patent Owner”) submits this preliminary response to the Petition (the “Petition” or “Pet.”) filed by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (“Petitioner”) for *Inter Partes* Review of claims 1-12 of U.S. Patent No. 8,350,294 (the “’294 patent”). Patent Owner respectfully requests that the Board deny the Petition for at least the reasons set forth below.

The ‘294 patent relates to a compensated gate MISFET (title). Claim 1 specifically recites “a compensated GaN layer” beneath the gate contact. As explained below, the compensated GaN layer in the gate allows the claimed transistor of the ‘294 patent to operate in a normally OFF (enhancement) mode, while also rendering the gate semi-insulating, thereby reducing undesirable gate leakage.

Compellingly, none of the prior art relied upon in the Petition even mentions the word “compensated” or remotely suggests a transistor with a compensated gate. This is because the compensated gate invention of the ‘294 patent, which achieves two technical effects having opposite requirements for electrical conductivity, was entirely unexpected and went in a direction completely contrary to conventional wisdom at the time of the invention.

Accordingly, for the reasons explained below, Petitioner has not established that there is a reasonable likelihood that at least one of the challenged claims of the ‘294 patent is unpatentable, and the Petition should be denied.

II. BACKGROUND

A. The ‘294 Patent

The ‘294 patent describes and claims a GaN (Gallium Nitride) MISFET (Metal Insulator Semiconductor Field Effect Transistor). GaN FETs are known for their ability to carry greater current and withstand higher voltages than their silicon counterparts. ‘294 patent at 1:21-24.

GaN transistor devices may be categorized into two different categories: (1) depletion-mode FETs and (2) enhancement-mode FETs. *See* ‘294 patent at 1:42-54. *See id.* Depletion-mode FETs maintain an “ON” state at zero gate-source voltage (normally ON), while enhancement mode FETs maintain an “OFF” state at zero gate source voltage (normally OFF). *See id.* Depletion-mode FETs deplete the 2DEG located near the junction of two layers having different band gaps. *See id.* In the depletion-mode FETs, an electron channel that exists at zero gate voltage is depleted by applying a negative gate voltage, thereby turning the FET OFF. *See id.* Conversely, enhancement-mode FETs have no electron channel at zero gate voltage, but an electron channel can be induced by applying a positive gate voltage, thereby turning the FET ON. *See id.*

The structure of a conventional GaN FET generally includes a substrate, a transition layer or layers (including a nucleation layer) that transitions the crystal growth from the substrate to the III-N epitaxial layers (e.g., AlGa_N), a III-N buffer layer (e.g., GaN), a III-N barrier layer (e.g., AlGa_N), and an optional p-type gate semiconductor material (e.g., GaN). *See* '294 patent at 1:55-2:2. A FET further includes three metal contacts: source, gate, and drain. *See id.*

As shown in Fig.1 of the '294 patent, an enhancement-mode transistor in the prior art has a conductive p-type GaN gate semiconductor. '294 patent at 1:55-2:2. When the p-type doping concentration in the GaN gate semiconductor (e.g., doping with Mg) is sufficiently high and the layer is sufficiently thick, the acceptors in the gate layer accept electrons, specifically electrons of the 2DEG, thereby depleting the 2DEG and interrupting the electron channel formed between source and drain. *Id.* at 1:42-2:2.

In the enhancement mode embodiment of Figs. 2-9, the '294 patent discloses a GaN transistor in which “a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the gate contact 37.” *Id.* at 3:8-9. The '294 patent explains that the compensated GaN gate material “leads to low gate leakage during device operation,” (*id.* at 3:18-19) and “reduces the gate capacitance of the device.” *Id.* at 3:20-21. The '294 patent further notes that “the high doping level of the compensated layer 38 leads to enhancement mode devices.” *Id.* at 3:16-17.

The '294 patent identifies several improvements achieved by its invention over preexisting transistors, including that “(1) the capacitance from gate to channel layer when the device is on is lower than in the prior art; (2) the gate bias can be driven much more positive without significant current through the gate...; and (3) hole injection from the gate into the channel layer is dramatically reduced relative to the prior art.” *Id.* at 3:22-29.

The compensated GaN layer of the '294 patent achieves two opposing effects related to electrical conductivity requirements. First, as the p-type GaN layer is grown, the Mg acceptors accept electrons from the 2DEG, thereby depleting the 2DEG and creating a normally-OFF (enhancement-mode) transistor. *See id.* at 3:10-17. Second, during the growth process, the remaining Mg acceptors are passivated by hydrogen, so that the p-type conductivity in the p-doped GaN is substantially reduced, and the p-doped GaN is in fact semi-insulating. *See id.* at 3:15-21, 43-52. As a result, the undesirable gate bulk leakage current through the bulk (not surface) of the p-doped GaN becomes small. *See id.* This is in accordance with the teaching of the '294 patent: “the compensated semiconductor layer 38 is a highly compensated semi-insulating material” '294 patent at 3:47-48.

These two opposite effects were entirely unexpected according to the conventional wisdom. Based on the teachings of the prior art technical literature, a

POSA (person of skill in the art) would have concluded that passivated p-doped GaN cannot be used to deplete the 2DEG and cannot create enhancement transistors. Ex. 1018; Ex. 2001; Ex. 2002. The prior art at the time of the '294 patent disclosed that passivated Mg-H complexes are neutral. Being neutral means that there is no electrical effect and a POSA would thus not have found passivation of p-doped GaN to be useful in the design of enhancement-mode transistors. The invention of the '294 patent fundamentally altered this thinking.

B. Grounds of Challenge

The petitioner challenges the patentability of claims 1-12 of the '294 patent on three grounds:

Ground 1: Claims 1-12 are challenged as being obvious over Smith, either alone (Ground 1A), in view of Kigami (Ground 1B), or in view of Uemoto (Ground 1C).

Ground 2: Claims 1-12 are challenged as being obvious over Uemoto in view of Smith.

III. CLAIM CONSTRUCTION

Petitioner correctly sets forth Petitioner's proposed claim construction from a related matter but misstates Patent Owner's construction, which was modified during responsive briefing of the related matter. Ex. 2003 at 6. Patent Owner proposes that the term "a compensated GaN layer" in claim 1 should be construed

as “a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).”

Patent Owner’s construction applies the plain meaning to a POSA of “GaN layer” and “compensated” consistent with the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005). Petitioner’s incorrect construction - “a doped GaN layer formed with a step to passivate its impurities” - fails to recognize that a POSA would understand the claimed “GaN layer” to be a GaN **gate** material. Moreover, Petitioner improperly seeks to have the limitation construed as a product-by-process limitation, contending that “compensated” refers to a process. As discussed below, however, a POSA would understand the term “compensated” in the context of the claim to be referring to and connoting a specific structure and electrical characteristics in the claimed “GaN layer,” not a process to create a GaN layer.

But regardless of whether Petitioner’s or Patent Owner’s claim construction is applied, the result is the same. The prior art relied upon by Petitioner simply does not disclose or suggest a transistor with a “compensated GaN layer”.

A. “GaN Layer” Refers to GaN Gate Material

A POSA would understand the plain meaning of the term “compensated GaN layer” in view of both the claim and the specification to be referring to a

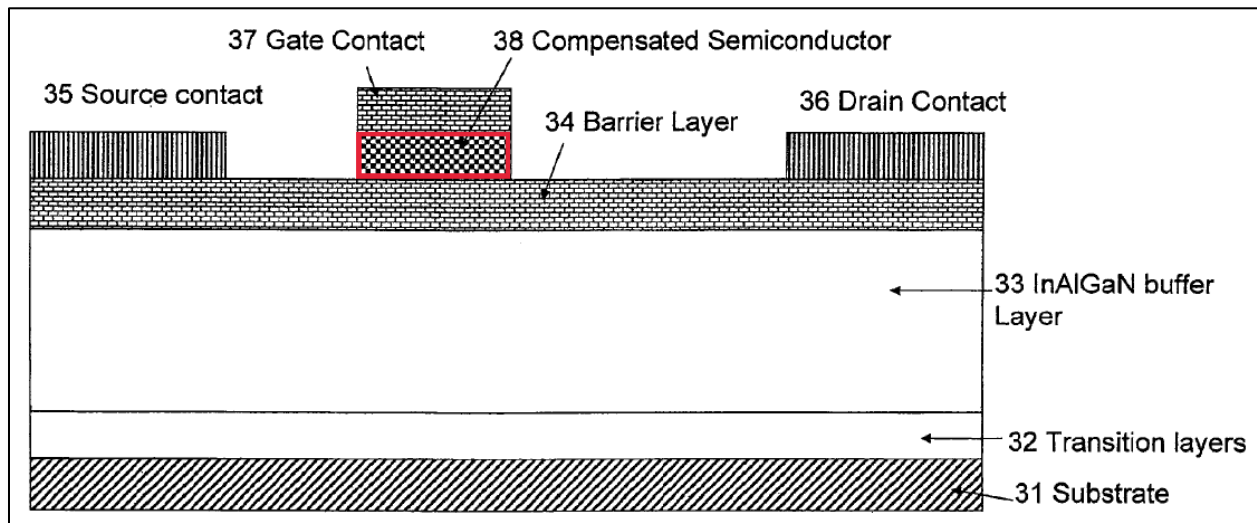
“compensated GaN gate material.” No claim term should be construed in a vacuum, out of context with the other words in a claim. *Phillips*, 415 F.3d at 1314

Claim 1 of the '294 patent describes a transistor where the “compensated GaN layer” is formed “above the barrier layer” and that “a gate contact” is formed “above the compensated GaN layer.” A POSA would understand from the placement of the “compensated GaN layer” between the barrier and the gate contact that the “GaN layer” is a GaN gate material.

The POSA’s interpretation and understanding of this fundamental claim term based on the claim language itself is confirmed by the specification. “[T]he specification is always highly relevant to the claim construction analysis . . . [and] it is the single best guide to the meaning of a disputed term.” *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Here, the entirety of the specification refers solely to a compensated GaN gate material. The '294 patent is titled “Compensated **Gate** MISFET and Method for Fabricating Same.” The specification details the problems with prior art GaN transistors having unfavorable **gate** leakage (see '294 patent at 1:55-2:6) and identifies a solution to that problem by creating a compensated **gate** “with low **gate** leakage.” *Id.* at 2:13-14 (emphasis added).

The figures and Summary of Invention further confirm the POSA’s understanding of the meaning of “compensated GaN layer” based on the claim

itself. Indeed, in describing Figure 2, the specification explains that “a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the **gate** contact 37.” *Id.* at 3:7-9 (emphasis added). Figure 2 (excerpted below with the compensated GaN layer annotated in red) has the same structure as recited in claim 1.



A POSA would understand that the layer between the gate contact and the barrier layer - in Figure 2 just as in claim 1 - refers to a GaN gate material. Indeed, the Summary of Invention explains that the claimed inventions are directed to using a material “below the gate contact and above the barrier layer” to “reduce[]” “gate leakage.” *Id.* at 2:14-16; *see also id.* at 3:18-21 (“using a compensated semiconductor layer **38** leads to low **gate** leakage during device operation”) (emphasis added). A POSA would understand that it is the gate material between these layers that contributes to reducing gate leakage, not some other type of GaN

layer. Moreover, the specification provides a method of making the device depicted in Figure 2 (a transistor) and recites the step of “etch[ing] away the compensated semiconductor layer 38, except the portion beneath the gate contact layer 37.” *See id.* at 3:35-38. A POSA reading the claim in light of the specification would have understood the ’294 patent to be describing the manufacturing of a gate stack, where the gate material is beneath the gate contact, and serves the purpose of turning the transistor on or off.

In short, the intrinsic evidence confirms that a POSA would have understood the term “compensated GaN layer” as used in claim 1 to be referring to a compensated GaN gate material, which is the only structure described in the intrinsic evidence as providing the advantages to the claimed transistor over the prior art and which the applicant identified as being at the heart of the claimed inventions.

B. Compensated Describes a Semiconductor with Modified Electrical Characteristics

A POSA would have understood the term “compensated” to have its plain and ordinary meaning in the art. The IEEE dictionary defines “compensated semiconductor” as “[a] semiconductor in which one type of impurity or imperfection (for example, donor) partially cancels the electric effects of the other type of impurity or imperfection (for example, acceptor).” Ex. 2004. Patent Owner’s construction is consistent with that definition.

The description of “compensated” in the specification of the ’294 patent is consistent with the plain and ordinary meaning of “compensated.” For example, the specification explains that the compensated GaN gate material includes a p-type impurity (e.g., Mg, Zn, Be, Cd, or Ca) that imparts an electric effect (i.e., conductivity), and a second impurity, e.g., hydrogen, that partially cancels the electric effect of the p-type impurity by rendering it semi-insulating. ’294 patent at 3:10-13, 3:43-45. The specification explains further that by having the electrical effect of the p-type impurity cancelled out by another impurity, the p-type gate material is differentiated from the prior art by having modified electrical characteristics—specifically, by being more resistive than the conductive structures found in the prior art. *See id.* at 3:46-49 (“the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material.”). A more resistive p-type GaN gate material has improved functional characteristics compared to the prior art, including “low gate leakage during device operation,” *id.* at 3:16-19, reduced gate capacitance, and the ability to act as an enhancement mode device (where the transistor is activated only when a positive voltage is applied to the gate contact). Indeed, nowhere does the ’294 patent refer to a compensated GaN material anywhere other than in connection with the compensated GaN gate. In fact, a POSA reading the ’294 patent – beginning with its title – would have

understood the compensated GaN as part of the gate structure to be the novel feature that distinguished the claimed transistor from the prior art by reducing gate leakage.

Because the term “compensated” has a plain meaning in the art and because the intrinsic evidence describes a “compensated GaN layer” consistent with the plain meaning of the term, Patent Owner’s plain-meaning construction should be adopted.

C. Petitioner’s Construction Should be Rejected

Petitioner’s construction of “compensated GaN layer” as “a doped GaN layer formed with a step to passivate its impurities” is incorrect for several reasons.

First, Petitioner’s construction does not apply the plain and ordinary meaning of “compensated GaN layer” to a POSA as “compensated **GaN gate material**.” As discussed above, the claimed structure is not referring to any GaN layer, but rather a gate material. Thus, Petitioner’s non-construction renders the term impermissibly broader than its plain meaning in view of the intrinsic evidence.

Second, Petitioner’s failure to construe GaN layer consistent with the intrinsic evidence by limiting the GaN layer to the gate material would encompass transistor designs in which the compensated GaN layer does not serve as gate semiconductor material and does not reduce the gate leakage current, as taught in

the '294 patent. For example, a transistor with a compensated GaN layer that is separate from the gate structure and in contact with the source and the drain would fall under Petitioner's expansive construction. In such a transistor, the gate structure would consist only of the metal, and as a result, the compensated GaN layer would not prevent gate leakage, as taught by the '294 patent. Petitioner's reading of the claim term in isolation is therefore incorrect.

But even if there was an equal choice between Petitioner's broad construction and Patent Owner's narrower construction - which there is not for the reasons discussed above - the proper choice would be the narrower construction proposed by EPC. *See Takeda Pharm. Co. v. Zydus Pharms. USA, Inc.*, 743 F.3d 1359, 1365 (Fed. Cir. 2014) ("We long ago established that '[w]here there is an equal choice between a broader and a narrower meaning of a claim, and there is an enabling disclosure that indicates that the applicant is at least entitled to a claim having the narrower meaning, we consider the notice function of the claim to be best served by adopting the narrower meaning.'") (quoting *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996)).

Third, Petitioner's proposed construction improperly limits the scope of the claim to a single type of compensation – i.e., passivation. Petitioner's proposed construction is incorrect, because it improperly limits the term "compensated"

based on the specification's reference to passivation as the "critical step" in achieving the claim "compensated GaN layer."

Fourth, "compensated GaN layer" is not a product-by-process limitation. Indeed, nothing in the claim defines the "compensated GaN layer" in terms of the processes used to compensate. The purpose of the product-by-process "doctrine is to prevent foreclosing inventors 'from the benefits of the patent system simply because a product is difficult to describe in words, or its structure is insufficiently understood.'" *In re Biogen* 335 F. Supp. 3d 688, 712 (D.N.J. 2018) (quoting *SmithKline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312 (Fed. Cir. 2006)), *rev'd and remanded sub nom. Biogen MA Inc. v. EMD Serono, Inc.*, 976 F.3d 1326 (Fed. Cir. 2020). In this case, claim 1 of the '294 patent is not directed to a product that the inventors were unable to describe in words or where the product's structure was not sufficiently understood. *Id.* As discussed above, the IEEE dictionary itself underscores that the term is well understood in the field and a POSA would have readily understood that the term "compensated GaN" layer refers to a GaN layer having certain structural and electric characteristics, not a GaN layer made according to a particular process.

Petitioner argues that "while the claim uses 'compensated as an adjective, that adjective derives from a past-tense verb" and that "[t]he past-tense form of 'compensated' suggests that the step of compensating had occurred." Petition at

14. Even if Respondents were correct that the term “compensated” derives from a past-tense verb, that does not transform the term “compensated” into a process term. Indeed, in *In re Garnero*, the predecessor court to the Federal Circuit recognized that past-tense verbs such as “‘intermixed,’ ‘ground in place,’ ‘press fitted,’ ‘etched,’ and ‘welded’ all . . . at one time or another have been separately held capable of construction as structural, rather than process, limitations.” 412 F.2d 276, 279 (C.C.P.A. 1969); *see also* *3M Innovative Prop. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (“‘[S]uperimposed’ . . . neither transforms claim 1 into a product-by-process claim nor even limits the scope of the claim to a serial method of manufacture; it describes only the structural relationship between the embossing patterns.”); *Hazani v. U.S. Int’l Trade Comm’n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997) (“‘chemically engraved’ not a process term). As discussed above, “compensated GaN layer” is not merely “capable of construction as [a] structural, rather than a process, limitation,” *In re Garnero*, 412 F.2d at 279, a POSA would understand the term to be a structural term.

But even if the Court believes that “compensated” can be interpreted as both a structural limitation (as Patent Owner proposes) and as a process limitation (as Petitioner proposes), the term still would not be a product-by-process limitation. “[W]ords of limitation that can connote with equal force a structural characteristic

of the product or a process of manufacture are commonly and **by default** interpreted in their structural sense, unless the patentee has demonstrated otherwise.” *In re Nordt Dev. Co.*, 881 F.3d 1371, 1375 (Fed. Cir. 2018) (emphasis added). Here, Patent Owner has clearly demonstrated that “compensated” is to be interpreted in its structural sense as allowing for modified electric characteristics in a GaN gate material that were otherwise possible in a material that was not compensated. *See Hazani*, 126 F.3d at 1479 (“chemically engraved” limitation not a product-by-process limitation because the limitation, “read in context, describes the product more by its structure than by the process used to obtain it”).

IV. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1A (SMITH ALONE)

In Ground 1A, Petitioner asserts that *Smith* alone “discloses the allegedly inventive elements, including the “compensated GaN” and “semi-insulating” layers recited in independent claims 1, 4, 7 and 10 of the ‘294 patent. Petition, pp. 21-22, 38, 46, 50 and 53. As explained below, Petitioner misinterprets and misrepresents the teachings of *Smith*.

Smith discloses a HEMT device with a cap layer 34 that extends completely between the ohmic contacts 30. As described in para [0070], a doped region 40 is provided over the cap layer.

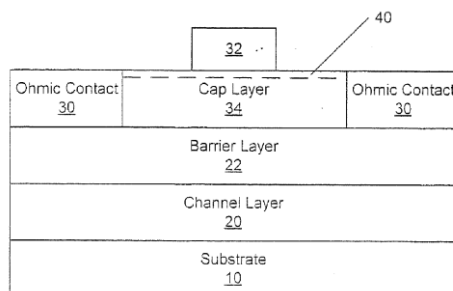


Figure 2A

Per *Smith*, paragraph [0085]:

In some embodiments of the present invention, the **doped region 40 is doped with p-type dopant, such as Mg**, Be, Zn, Ca and/or C. In other embodiments of the present invention, the doped region 40 is doped with an n-type dopant, such as Si, Ge and/or O. In further embodiments of the present invention, the doped region 40 is doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co. The dopant may be incorporated into the cap layer 34 during deposition or growth of the cap layer 34, 34' or may be subsequently implanted, for example, using ion implantation. In some embodiments of the present invention, the cap layer 34 has a dopant incorporated throughout the cap layer 34, 34'. In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34'. [Emphasis added.]

In other embodiments, e.g., Figs. 3B/4B, without a doped region 40, a passivation layer (BN Layer 100' or SiC layer 110') is provided above the cap layer:

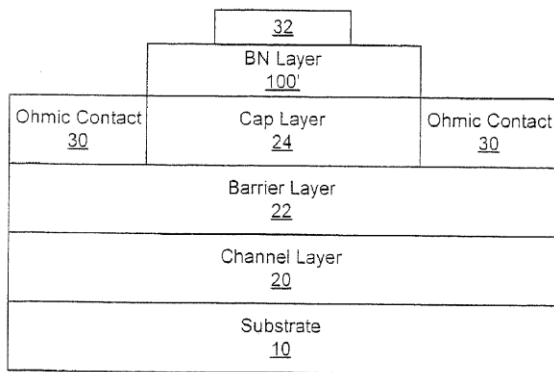


Figure 3B

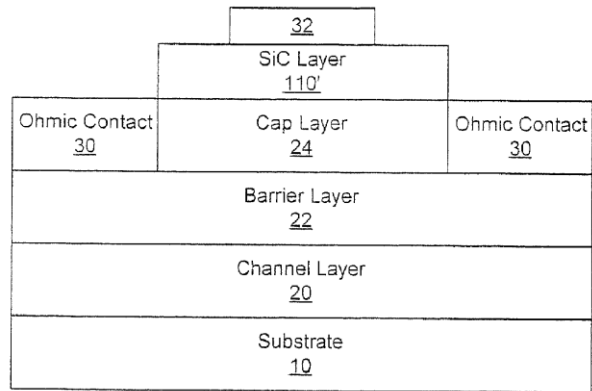


Figure 4B

A. Smith does not disclose the “compensated GaN layer” of independent claim 1.

Petitioner asserts that the cap layer 34 shown in Figure 2A may be a GaN layer or a GaAlN layer (which is correct) and that **doped region 40** may be doped with p-type dopant, e.g., Mg (also correct). However, Petitioner asserts (incorrectly) that **the cap layer 34**, in the embodiment of Figure 2A, is **necessarily** a compensated layer because “by 2009 it was well-known that hydrogen would be naturally present in such layers,” and “[i]t was known that hydrogen would be present even in as-grown GaN materials, forming acceptor-H neutral complexes that passivate the impurity.” Petition, p. 42. “And because it was well-known that as-grown GaN films are naturally hydrogen passivated, ... *Smith’s* cap layer 34 has passivated impurities.” Petition, p. 39.

Petitioner’s assertion is based on a false premise and is incorrect for at least three important interrelated reasons:

1. *Smith* provides little detail regarding the formation of the cap layer.

Smith discloses in [0077]: “The cap layer 24, 24’ may be blanket formed on the barrier layer 22 and may be epitaxially grown and/or formed by deposition.” Petitioner makes no argument that, if the cap layer is formed by deposition rather than epitaxial growth, hydrogen would be incorporated in the cap layer. With respect to an epitaxial growth process, *Smith* discloses in [0064]: “The cap layer 24, 24’ may be provided by conventional epitaxial growth techniques where a higher Al concentration is provided during termination of growth of the cap layer 24, 24’. Thus, for example, the cap layer 24, 24’ may be provided by MOCVD growth with an increase in the Al source just prior to and during termination of growth.” **However, importantly, there is no indication in *Smith* that the “conventional epitaxial growth techniques” that *Smith* references are carried out in the presence of hydrogen.**

2. U.S. Patent No. 6,498,111 (“the ‘111 patent”), which *Smith* incorporates by reference in [0083], indicates that there are processes which remove hydrogen prior to cool down. Ex. 2005 at 2:1-3.
3. Importantly, even if hydrogen was present during epitaxial growth in the particular “conventional growth technique” chosen by a skilled person

seeking to produce a device according to *Smith*'s teachings, that skilled person, following conventional wisdom (as set forth in the '111 patent) would have included an anneal/activation step to remove hydrogen ('111 patent, lines 13-28) as was conventional (see the '111 patent, col. 2, lines 13-17). Indeed, in [0083], *Smith* explicitly suggests that "an anneal of the structure including the passivation layer may be carried out in an oxygen environment **to remove hydrogen** from the layer."¹

Petitioner also posits that a POSA would have been motivated to passivate *Smith*'s cap layer to result in the claimed "compensated GaN layer."

Specifically, at pages 26-27 of the Petition, Petitioner asserts:

A POSITA would have been motivated to adjust *Smith*'s doping by using hydrogen passivation because *Smith* recognizes level of doping as a result-effective variable controlling transistor characteristics, and a POSITA would have known that hydrogen passivation adjusted the doping level. *Smith* discloses that the level of doping in cap layers is a result-effective variable to control leakage, explaining that "[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant 'surface' state but not so high as to provide introduce traps or leakage paths." By 2009, a POSITA was intimately familiar with acceptor doping and hydrogen passivation. A POSITA would have known that incorporating hydrogen in GaN layers would passivate acceptor dopants affecting the level of doping.

¹ The '111 patent **teaches away** from passivation with hydrogen. A skilled person reading the '111 patent would have been led in the opposite direction of the invention of the '294 patent, and would have sought to **avoid compensation** of p-GaN by passivation of hydrogen.

Petitioner confuses the “level of doping” with the level of compensation of dopants. Passivating a doped GaN layer does not affect the level of doping of that GaN layer. Rather, passivation with hydrogen affects to what extent the dopants in a p-GaN layer are compensated, not the level of doping (which is based on the concentration of dopants in the layer). Accordingly, absent hindsight, a POSA would not have looked to hydrogen passivation as a way to alter *Smith*’s level of doping.

Moreover, *Smith* requires active, rather than compensated, p-type dopants: “P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and or minimize trapping effects.” Ex. 1005 at ¶ [0072]. *Smith* even discloses a preferred p-type dopant level: “With p-type dopants, the doped region 40 may provide a dopant concentration of from about 10^{16} to about 10^{22} cm^{-3} .” Ex. 1005 at ¶ [0087]. Given *Smith*’s teaching requiring active p-type dopants in region 40, a POSA would not contemplate doing the opposite and compensating the very dopants that are necessary for the *Smith* device to function effectively.

Even the above quoted passage at ¶ [0087] of *Smith* regarding the “level of doping” states only that it “should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths.” Thus, in paragraph

[0087], *Smith* simply reiterates that a specific **concentration of dopants** is necessary, **not that those dopants should be compensated**. *Smith* therefore provides no motivation for a POSA to compensate.

In summary, the portions of *Smith* relied upon in the Petition relate to methods for achieving a desired level of **doping** in a semiconductor material, not a desired level of passivation/compensation of the dopants. Compensating *Smith*'s doped layer 40 would negate the effects of the doping of that layer. *Smith* would not dope layer 40 only to subsequently compensate the doping. Doing so would be completely counterintuitive and runs completely counter to *Smith*'s stated intentions. *Smith*'s disclosure thus goes in **the exact opposite** direction of the compensated gate of the '294 patent.

***Smith* therefore does not disclose compensation**, under either party's construction, and it cannot be implied or rendered obvious from the disclosure of *Smith* for the reasons stated above. If compensation occurred naturally in *Smith* during the "conventional growth techniques", as assumed by Petitioner, *Smith* would have taken steps to remove the hydrogen, so that region 40, if p-doped, would work as intended. ***Smith* thus does not disclose or suggest the "compensated layer" of independent claim 1, and a POSA would not be motivated to compensate *Smith*'s cap layer.**

B. Smith does not disclose the "semi-insulating III-N layer" of independent claims 4, 7 and 10.

At page 46 of the Petition, Petitioner asserts that “*Smith* discloses that cap layer can be a ‘semi-insulating III-N layer.’” Specifically, on page 47 of the Petition, Petitioner incorrectly refers to Figure 2A of *Smith* as disclosing “*Smith*’s **semi-insulating cap layer 34** above barrier layer 22.” [Emphasis in original.]

In fact, *Smith* never states or even remotely implies that the cap layer 34 is “semi-insulating.” Petitioner effectively concedes that the term “semi-insulating” is actually not associated with *Smith*’s cap layer, but rather comes from *Smith*’s incorporation by reference of *Saxler874* (Ex. 1016). Petition at 46.

Petitioner’s argument appears to focus on *Smith*’s disclosure in [0085] that, “[i]n further embodiments of the present invention, the doped region 40 is doped with a deep level dopant” and that “in some embodiments, doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34.” Invoking *Smith*’s subsequent incorporation by reference of *Saxler874*, Petitioner combines these disclosures in *Smith* with the disclosure in *Saxler874* “that co-doping “provide[s] semi-insulating Group III nitride layers.” Ex. 1016 at [0005]. But there is a fundamental flaw in Petitioner’s argument.

The portion of *Saxler874* on which the Petitioner relies does not state or suggest that *any* type of co-doping results in a semi-insulating Group III nitride layer, as Petitioner implies. Rather, in [0005], *Saxler874* discloses:

“Embodiments of the present invention provide semi-insulating Group III nitride semiconductor layers and methods of fabricating semi-insulating Group III nitride layers. In certain embodiments of the present invention, fabrication of a semi-insulating Group III nitride layer includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.” To the extent this disclosure teaches creating a semi-insulating layer using co-doping, a POSA would understand this disclosure to mean that co-doping a shallow level p-type dopant and a deep level dopant is what would result in the semi-insulating layer.

Conversely, in the context of paragraph [0085], where *Smith* incorporates *Saxler*⁸⁷⁴ by reference, *Smith* at most teaches co-doping regions of different dopant concentrations (“In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34’”). There is no suggestion in *Smith* that region 40, if p-doped, should be co-doped with a deep level dopant. And Petitioner has provided no motivation as to why a POSA would use that type of co-doping in *Smith*. Accordingly, Petitioner has not established that *Smith* discloses or renders obvious a **“semi-insulating III-N layer above the barrier layer”** as recited in independent claims 4, 7 and 9.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 1A.

V. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1B

In Ground 1B, Petitioner asserts that *Smith* in view of *Kigami* renders obvious the “compensated GaN layer” recited in independent claim 1. Petition, p. 24-31. As explained above, Petitioner misinterprets and misrepresents the teachings of *Smith* with regard to the claimed features recited in independent claim 1. As explained below, *Kigami* does not rectify the deficiencies of *Smith*.

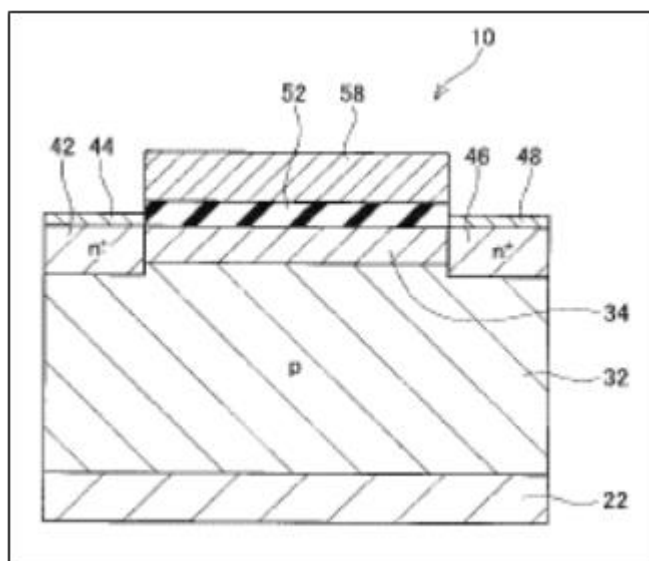
A. Kigami does not rectify the deficiencies of Smith with respect to the “compensated GaN layer” of independent claim 1.

At page 28 of the Petition, Petitioner asserts that a “POSITA would have been motivated to apply *Kigami*’s hydrogenation processing step(s) to passivate impurities in *Smith*’s cap layers.” Petitioner also contends that the motivation for modifying *Smith* is provided in *Kigami*: “A POSITA would have been motivated to use *Kigami*’s hydrogen incorporation techniques to form a region with passivated impurities in *Smith*’s cap layer.” *Id.* Patent Owner disagrees.

In *Kigami*, hydrogen is present in the local region 34, above the semiconductor layer 32, and purportedly “forms a composite” with the magnesium in the local region 34. Ex. 1008 at [0022]. The semiconductor layer 32 is formed directly on the substrate 22. That semiconductor layer corresponds to a buffer

and/or a transition layer with regard to claim 1. A gate-insulating film 52 is formed *above* the local region 34 of the semiconductor layer 32, and a gate electrode is formed above that gate-insulating film 52. *Id.* at ¶[0020].

The *Kigami* device, as shown in Figure 1 below, thus has a gate insulator 52 that is *above* the insulating barrier (local region 34). Hydrogen is introduced to lower the threshold voltage and form a channel *under* the gate insulator 52. A fully activated (not compensated) p-GaN layer (semiconductor layer 32) *below* the local region 34 depletes the 2DEG from the channel.



***Kigami* at FIG. 1**

Kigami discloses a different device from the device recited in claim 1 of the '294 patent and is cumulative to *Bowers*, which was considered for its discussion of passivation by hydrogen in GaN material during prosecution of the '294 patent. Ex. 1002 at 87-88; Ex. 1020.

Kigami uses an entirely different layer as the “gate insulating film” below the gate contact and incorporates a fully-activated p-type GaN layer and a GaN layer with magnesium and hydrogen to form the channel. Nothing in *Kigami* discloses or suggests that its hydrogen-treated p-type GaN layer would be suitable below the gate contact or that a compensated GaN layer including Mg dopants and hydrogen would be acceptable or functional in place of the cap layer 34 of *Smith*. In fact, as explained above, hydrogen is introduced to the GaN layer in *Kigami* in order to form a channel, not to reduce gate leakage. A POSA would therefore not seek to combine the teachings of *Smith* with *Kigami*, to “apply *Kigami*’s hydrogenation techniques to *Smith*’s cap layer 34,” absent impermissible hindsight.

Furthermore, there is no motivation to combine *Smith* with *Kigami* because a POSA would find the doping of a gate semiconductor followed by the cancellation of the effects of the dopant to be highly counterintuitive. *Smith* makes clear the purpose of the dopants it utilizes: “The dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations.” *Smith* at [0064]. Passivating those dopants would void their purpose in *Smith*, rendering the *Smith* device inoperable for its stated purpose.

Smith in view of *Kigami* therefore do not render obvious the claimed “compensated GaN layer,” under either party’s construction.

B. Kigami does not rectify the deficiencies of Smith with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10.

Petitioner does not contend that *Kigami* is relevant or combinable with *Smith* with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10. Pet. at pp. 46-47, 49-50 and 56.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 1B.

VI. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1C

In Ground 1C, Petitioner asserts that *Smith* in view of *Uemoto* renders obvious the “compensated GaN layer” recited in independent claim 1. Petition at 25-26. As explained above, Petitioner misinterprets and misrepresents the teachings of *Smith* with regard to this claimed feature. As explained below, *Uemoto* does not rectify the deficiencies of Smith in this regard.

A. Uemoto does not rectify the deficiencies of Smith with respect to the “compensated GaN layer” of independent claim 1.

At page 31 of the Petition, Petitioner asserts that a “POSITA would have been motivated to apply *Uemoto*’s hydrogen diffusion technique to selectively increase the resistivity of Smith’s cap layers.” More specifically, Petitioner asserts that a POSA would have been motivated to use *Uemoto*’s “hydrogen diffusion film 17” in *Smith* to form the “high resistive region 15b,” “to similarly inactivate

impurities in *Smith*'s cap layer, generate the highly resistive regions, and reduce leakage."

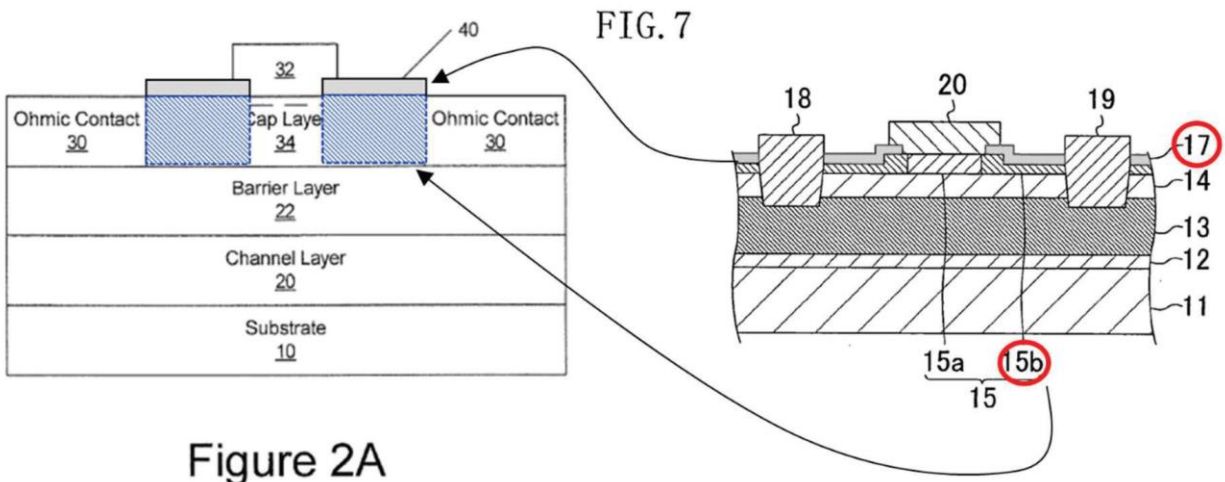


Figure 2A

Petitioner is incorrect. Absent hindsight, there would have been no motivation for a POSA to modify *Smith* to incorporate the teachings of *Uemoto*, and even if the two were combined as Petitioner proposes, the resultant device would still not have a compensated layer under the gate contact as claimed.

Petitioner argues that *Uemoto* suggests and motivates the combination of *Smith* and *Uemoto*. Petition at 32. Specifically, Petitioner posits that inactivating impurities increases resistivity and reduces leakage, which would assist *Smith* with its concern with fabrication methods that reduce transistor leakage. But *Smith*'s focus is on adjusting the level of doping, not inactivating impurities. Petitioner has provided no motivation as to why, given *Smith*'s concern with doping level adjustments, a POSA would seek to inactivate impurities in *Smith*.

Moreover, Petitioner does not argue or provide any proof that the alleged compensated GaN layer of the *Smith-Uemoto* combination is under the gate contact. See Petition at 31-33, 43. Even if Petitioner did so, the resultant combined *Smith-Uemoto* device would not have “a gate contact above the compensated GaN layer,” as recited in claim 1 of the ’294 patent. For example, on page 43 of the Petition, Petitioner asserts that “applying *Uemoto*’s technique to diffuse hydrogen would result in cap layer 34 being “compensated,” as the term is used in the ’294 patent. But as is evident from Petitioner’s above illustration of the proposed combination of *Smith* and Fig. 7 of *Uemoto*, the alleged “compensated” region of *Smith* is NOT under the gate contact 32 of *Smith*, as required by claim 1. Thus, the proposed combination, even if attempted, would not result in a GaN transistor as claimed, with a compensated layer under the gate contact.

Smith in view of *Uemoto* therefore do not render obvious the claimed “compensated GaN layer,” under either party’s construction.

B. Uemoto does not rectify the deficiencies of Smith with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10.

Petitioner does not contend that *Uemoto* is relevant or combinable with *Smith* with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10. Pet. at 46-47, 49-50 and 56.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 1C.

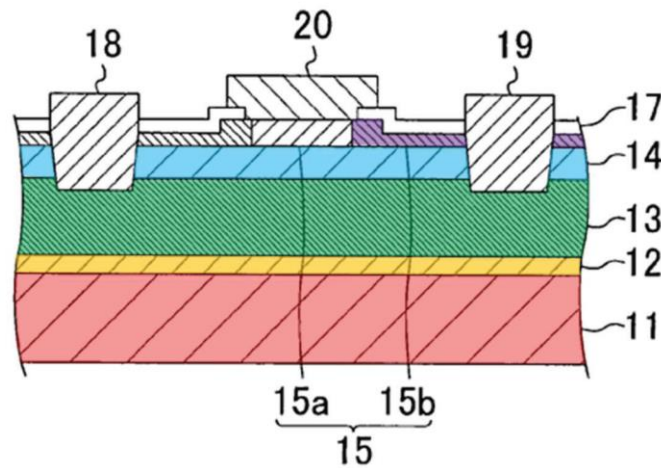
VII. THE BOARD SHOULD DENY INSTITUTION OF GROUND 2

In Ground 2, Petitioner reverses the order of the prior art as compared to Ground 1C, and asserts that *Uemoto* in view of *Smith* meets independent claims 1, 4, 7 and 10 of the ‘294 patent. Petition, p. 61-67. As explained below, Petitioner misrepresents the teachings of *Uemoto* with respect to the “compensated GaN layer” of claim 1, and the “semi-insulating III-N layer” of independent claims 4, 7, and 10.

A. Uemoto does not disclose the “compensated GaN layer” of independent claim 1.

At page 61 of the Petition, Petitioner asserts that *Uemoto* discloses the compensated GaN layer of independent claim 1, because *Uemoto* discloses that “a third nitride semiconductor layer 15” is formed with GaN doped with magnesium.” Petitioner asserts that “layer 15 is compensated,” “because *Uemoto* discloses that the impurities in region 15b of the layer 15 are inactivated when ‘hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment.’” *Id.*

FIG. 7



***Uemoto* at FIG. 7.**

Importantly, Petitioner conflates two separate elements of *Uemoto* in its analysis: element 15a, which is a p-doped *conductive*, activated AlGaIn/GaN region, and element 15b, which is a resistive p-doped AlGaIn/GaN region. *Uemoto* at ¶ [0033], [0063]. Petitioner conflates those two distinct elements of *Uemoto* to obscure the fact that it is the *conductive*, activated p-doped AlGaIn region 15a, not the resistive region 15b, which is situated above the barrier layer 14 and below the gate electrode 20, as recited in independent claim 1 of the '294 patent.

As shown in Figure 2B of *Uemoto*, there is always a 2DEG under p-doped high resistive region 15b. See Ex. 1006 at Fig. 2B, [0038]. Upon application of a positive gate voltage, the activated p-type material of region 15a operates like the “highly doped p-GaN 106” shown in prior art Figure 1 of the '294 patent, such that the *Uemoto* device depletes the 2DEG under the gate and conducts with a high gate

leakage current relative to the device of the '294 patent. See Ex. 1006 at Fig. 2A, 2B, [0038]; '294 patent at Fig. 1, 2:3-6.

Thus, a fundamental issue with Petitioner's argument is that region **15b** is not under the gate, nor is the overlying hydrogen passivation film 17 that supplies hydrogen to inactivate the acceptors (e.g., magnesium) in region 15b under the gate. Region 15b serves absolutely no function in depleting the underlying 2DEG and turning the device on or off. Rather, that function is carried out by gate contact 20 and underlying region 15a, which is conductive, not inactivated.

It is clear that the conductive control region 15a of *Uemoto* contains activated (conductive) rather than passivated (semi-insulating) p-type material because *Uemoto* intentionally activates the Mg dopants in the control region:

“When a thermal treatment is performed in an inert gas atmosphere at 800° C. for about 20 to 60 minutes, the hydrogen atom is desorbed from Mg. Then, the Mg is activated, and **thus the nitride semiconductor layer shows p-type conductivity.**”

Id. at ¶ [0049] (emphasis added). *Uemoto* specifically notes that this activation process is performed in a nitrogen atmosphere. *Id.* at ¶ [0048]. That is in contrast to *Uemoto*'s discussion of the high resistive region 15b, “in which the p-type impurity is not activated to offer a high resistive layer.” *Id.* at ¶ [0051]. *Uemoto* discloses: “The third nitride semiconductor layer doped with Mg is composed of: a control region **15 a** in which Mg is activated to exhibit a p-type conductivity; and

a high resistive region **15 b** in which Mg is not activated to offer a higher resistance than the control region **15 a**.” *Id.* at ¶ [0033]. *Uemoto* thus reflects the conventional understanding prior to the ’294 patent, that passivation below the gate is unfavorable to the formation of an enhancement mode transistor.

Notably, in a parallel invalidation request to the Chinese Patent Office relating to the Chinese counterpart of the ’294 patent proceeding, Petitioner relied upon the p-doped conductive region 15a, not high resistive region 15b, as purportedly disclosing the “compensated GaN layer.” *See* Ex. 2006 at 23-25. That inconsistency demonstrates that Petitioner itself recognizes that it is unreasonable to identify region 15b as meeting the “compensated GaN layer” of independent claim 1, because region 15b is not under the gate electrode 20, as required by claim 1 of the ’294 patent.

Furthermore, it would not have been obvious to adjust *Uemoto*’s gate electrode 20 and region 15b such that region 15b was under the gate because such a modification would run counter to *Uemoto*’s stated goal of having a control region under the gate with much lower resistivity than the high resistive region 15b. *See* Ex. 1006 at [0033]. *Uemoto* highlights the importance of activation in the control region below the gate, stating “in the control region, as shown in Figure 2A, the p-type impurity contained in the third nitride semiconductor layer **15** is

activated” and that this activation “results in obtaining the normally-off characteristics of nitride semiconductor transistors.” *Id.* at [0038].

Moreover, *Uemoto* does not disclose “a compensated GaN layer,” as recited in claim 1 of the ’294 patent because the p-doped high resistive region 15b is not a part of the gate material (that is, region 15b is not under the metal gate). As shown in Figure 7 above, it is the conductive control region 15a that “comes into ohmic contact with” and is part of the gate structure along with gate electrode 20. *Id.* at [0034]. But *Uemoto* discloses no such contact between the gate electrode and the p-doped high resistive region 15b, and Figure 7 shows that it is: (1) separated from the gate electrode by the hydrogen diffusion film 17, and (2) extends well beyond the structure of the gate.

Because *Uemoto* does not disclose a “compensated GaN layer,” for at least the reasons outlined above, *Uemoto* cannot disclose “a gate contact above the compensated GaN layer,” as recited in claim 1 of the ’294 patent. The gate contact and compensated GaN layer, as recited in claim 1 of the patent, together form the gate structure of the transistor of claim 1. *Uemoto* does not disclose, teach, or suggest that element, and therefore the element, “a gate contact above the compensated GaN layer,” of claim 1 is not disclosed by *Uemoto*.

Uemoto in view of *Smith*² therefore do not render obvious the claimed “compensated GaN layer,” under either party’s construction.

B. Uemoto in view of Smith does not disclose the “semi-insulating III-N layer” of independent claims 4, 7 and 10.

At page 78 of the Petition, Petitioner concedes that *Uemoto* does not disclose layer 15 as being “semi-insulating.” Petitioner thus relies upon *Smith* for this teaching, referring to the arguments at VIII.G.6 (pp. 46-47) of the Petition.

Petitioner asserts that *Smith*’s cap layer 34 can be formed with “[t]echniques for co-doping Group III-nitride materials,” Ex. 1005 at [0085], and that *Saxler*⁸⁷⁴ (Ex. 1016), which *Smith* incorporates by reference, explains that co-doping “provide[s] semi-insulating Group III nitride semiconductor layers.” Ex. 1016, [0005].

But, as explained above, there is a fundamental flaw in Petitioner’s argument. *Smith* never states or even remotely implies that the cap layer 34 is “semi-insulating.” Petitioner effectively concedes that the term “semi-insulating” is actually not associated with *Smith*’s cap layer, but rather comes from *Smith*’s incorporation by reference of *Saxler*⁸⁷⁴. Petition at 46.

² Petitioner does not rely on *Smith* to provide an alleged teaching of “compensated GaN layer” in Ground 2.

Petitioner's argument appears to focus on *Smith*'s disclosure in [0085] that, "[i]n further embodiments of the present invention, the doped region 40 is doped with a deep level dopant" and that "in some embodiments, doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34." Invoking *Smith*'s subsequent incorporation by reference of *Saxler874*, Petitioner combines these disclosures in *Smith* with the disclosure in *Saxler874* "that co-doping "provide[s] semi-insulating Group III nitride layers." Ex. 1016 at [0005]. But there is a fundamental flaw in Petitioner's argument.

The portion of *Saxler874* on which the Petitioner relies does not state or suggest that *any* type of co-doping results in a semi-insulating Group III nitride layer, as Petitioner implies. Rather, in [0005], *Saxler874* discloses:

Embodiments of the present invention provide semi-insulating Group III nitride semiconductor layers and methods of fabricating semi-insulating Group III nitride layers. In certain embodiments of the present invention, fabrication of a semi-insulating Group III nitride layer includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.

To the extent this disclosure teaches creating a semi-insulating layer using co-doping, a POSA would understand this disclosure to mean that co-doping a shallow level p-type dopant and a deep level dopant is what would result in the semi-insulating layer.

Conversely, in the context of paragraph [0085], where *Smith* incorporates *Saxler*⁸⁷⁴ by reference, *Smith* at most teaches co-doping regions of different dopant concentrations (“In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34’’”). There is no suggestion that a p-type dopant be co-doped with a deep level dopant. And Petitioner has provided no motivation as to why a POSA would use that type of co-doping in *Smith*.

Accordingly, for the reasons set forth above, *Smith* thus does not rectify the admitted deficiency of *Uemoto* with respect to a **“semi-insulating III-N layer above the barrier layer”** as recited in independent claims 4, 7 and 10.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 2.

VIII. RESERVATION OF RIGHTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if IPR is instituted. Similarly, Patent Owner does not concede any underlying contentions in the Petition and reserves the right to rebut any such contention later. Further, Patent Owner is not limited to the arguments presented in this Preliminary Response, but

expressly reserves the right to raise further arguments, including claim construction arguments, not presented herein.

IX. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

Dated: December 21, 2023

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

walter.davis@blankrome.com

Blank Rome LLP

1825 Eye St NW

Washington, DC 20006

Tel: 202-420-2200

Fax: 202-420-2201

Counsel for Patent Owner

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER's PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 8,034 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

Dated: December 21, 2023

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

Innoscience-EPC-IPRs@finnegan.com

Dated: December 21, 2023

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner