

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before the Honorable Clark S. Cheney
Chief Administrative Law Judge**

In the Matter of

**CERTAIN SEMICONDUCTOR DEVICES,
AND METHODS OF MANUFACTURING
SAME AND PRODUCTS CONTAINING
THE SAME**

Investigation No. 337-TA-1366

COMPLAINANT'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Claims must be construed in a way that “most naturally aligns with the patent’s description of the invention.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005). And their construction must be consistent with the “overall object of the invention” and based on the specification’s descriptions of the invention “as a whole.” *See, e.g., Praxair v. ATMI*, 543 F.3d 1306, 1323-24 (Fed. Cir. 2008). These canons of construction are the heart of much of the dispute here. EPC consistently adheres to these central canons across all of its proposed constructions. Respondents do not.

Respondents’ constructions and supporting arguments expose an unprincipled and self-serving approach, calculated to avoid infringement and bolster Respondents’ invalidity positions. On the one hand, they reduce the entire invention to exemplary embodiments, impermissibly limiting its scope. On the other hand, they ignore the essence of the invention and the specification as whole to improperly broaden the claims.

The sections below detail Respondents’ problematic approach.

II. CLAIM CONSTRUCTION OF ASSERTED PATENTS

A. “A COMPENSATED GAN LAYER” (’294 PATENT, CLAIM 1)

As to the term “compensated GaN layer,” reading the specification and the intrinsic evidence as a whole makes clear that this limitation can be nothing but *the gate material*. As to the word “compensated” in that term, EPC is aligned with the Staff and is now conforming its proposed construction accordingly. Respondents’ construction, however, improperly imports isolated statements from preferred embodiments as unnecessary limitations.

1. The Invention as a Whole Refers Only to a GaN Gate as Being the Compensated Structure

Respondents and the Staff are both incorrect that “GaN layer” as used in claim 1 of the ’294 patent is not referring specifically to a GaN **gate material**. Neither Respondents nor the Staff explain how it can be anything else while staying true to the invention. Their positions fail to account for two claim construction principles:¹ (1) that a disputed term cannot be construed “in a vacuum, devoid of the context of the claim as a whole,” EPC Br. at 5 (quoting *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1347 (Fed. Cir. 2008)); and (2) that the meaning of a claim term must be construed based on the description of the invention “as a whole” in the specification and to give effect to the “overall object of the invention.” *Praxair*, 543 F.3d at 1323-24 (requiring that the claimed “flow restriction must be sufficient to achieve the overall object of the invention—that is, to prevent a hazardous release of gas,” which is described as the invention “as a whole”); *see also Alloc, Inc. v. Int’l Trade Comm’n*, 342 F.3d 1361, 1370 (Fed. Cir. 2003) (looking to “whether the specification read as a whole suggests that the very character of the invention requires the limitation be part of every embodiment”); *Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1313-14 (Fed. Cir. 2007) (construing claims to include limitations where doing so “most naturally aligns with the patent’s description of the invention”); *Phillips*, 415 F.3d at 1316 (same).

The entire specification makes clear that the claimed compensated GaN layer can only be the gate material. *See* Declaration of Dr. Eric Fred Schubert in Support of Complainant’s Opening Claim Construction Brief (“Schubert Decl.”) ¶ 45; *see also* Declaration of Dr. Eric Fred

¹ The Staff’s reliance on *Thorner v. Sony Computer Entm’t Am., LLC*, 669 F.3d 1362, 1368 (Fed. Cir. 2012) is misplaced. Staff Br. at 26. The passage on which the Staff relies is directed to limiting a claim based on lexicography. EPC is not relying on lexicography in proposing that “GaN layer” be construed as “GaN gate.”

Schubert in Support of Complainant’s Responsive Claim Construction Brief (“Schubert Responsive Decl.”) ¶¶ 8-25. It is the only material located just below the gate metal contact and is thus the crux of the invention because it is the only described solution for solving the problem of gate leakage current and gate capacitance. *See, e.g.*, ’294 patent at 3:16-21. Unlike Respondents, EPC is not attempting to limit the scope of the claims based on “isolated statements . . . pertain[ing] to specific embodiments of the invention rather than to the invention as a whole.” *Praxair*, 543 F.3d at 1324. As made clear in EPC’s opening brief and supporting declarations, a POSA would only understand the patent disclosure as a whole to be referring to a compensated GaN *gate*.

Because EPC’s construction “most naturally aligns with the patent’s description of the invention,” and does not seek to constrain the claim to a selected embodiment, EPC’s construction should be adopted. *Ormco*, 498 F.3d at 1313-14.

2. Respondents’ Proposed Construction Improperly Limits the Scope of the Claim to a Single Type of Compensation

Respondents’ proposed construction is incorrect because it improperly limits the term “compensated” based on the specification’s reference to passivation as the “critical step” in achieving the claimed “compensated GaN layer.” But Respondents do not explain why they require the passivation of all of the p-type dopants in the compensated GaN layer. As explained below, such a requirement is incorrect and renders the invention inoperable for its intended purpose.

As explained in EPC’s opening brief, construing “compensated” as “passivation” is not sufficiently accurate to describe the invention and its inner workings. The specification teaches that compensation differentiates the claimed compensated GaN gate from the prior art by transforming the conductive p-type GaN material into one that is semi-insulating. ’294 patent at

3:45-49. The result is that the compensated GaN layer exhibits novel properties—specifically reduced gate leakage current and reduced gate capacitance—which EPC discovered is critical to the functionality of GaN transistors. See Schubert Decl. ¶ 32; Schubert Responsive Decl. ¶¶ 14-15. As the patent and Dr. Schubert explain, not *all* of the p-type dopant atoms (*e.g.*, magnesium) are passivated by the other impurity (hydrogen). And, in fact, doing so would render the invention unworkable. Rather, it is crucial for some of the p-type acceptor dopants to deplete the 2DEG electrons from the buffer layer so the invention can work. Schubert Responsive Decl. ¶ 19.

Thus, Respondents’ proposed construction is incorrect because it suggests that the “compensated GaN layer” must have *all the p-type dopants completely* passivated to exclude the “conductive p-type material” of the prior art. Respondents’ Br. at 20. As Dr. Schubert explains, if Respondents were correct, the claimed GaN gate would not function correctly. Schubert Decl. ¶ 45. GaN gates that are p-type doped are used to create enhancement mode transistors that are “off” when no gate voltage is applied. Schubert Responsive Decl. ¶¶ 11-13. But if all of the p-type dopants were passivated as Respondents’ proposed construction requires, none of the p-type dopants can serve as “acceptors” which are essential for proper enhancement mode functionality. *Id.* ¶ 19. Accordingly, Respondents’ construction would exclude the preferred enhancement mode embodiments and is thus impermissible. See *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (constructions excluding preferred embodiments are “rarely, if ever, correct”).

3. EPC’s Construction Applies a POSA’s Understanding of “Compensated” In View of the Intrinsic Evidence

Respondents complain that the words “electrical effects” in EPC’s proposed construction are ambiguous, Respondents’ Br. at 19, and that the phrase “partially cancels” in EPC’s proposed

construction is improper because it would render the claim indefinite. Respondents' Br. at 18-19. EPC disagrees, as does the Staff.

As Dr. Schubert explains, Schubert Responsive Decl. ¶ 17, a POSA would readily understand from the '294 patent specification that the electrical effect at issue is electrical conductivity. See '294 patent at 2:4-6 ("One problem is that the leakage current of the gate contact during device conduction is very high due to gate charge injection."); see also *id.* 3:17-19 ("In addition, using a compensated semiconductor layer 38 leads to low gate leakage during device operation.").

The Staff agrees that EPC's proffered "partially cancels" is consistent with the specification of the patent and comes directly from IEEE's definition," Staff Br. at 8-9, but suggests that "the word 'partially' should be removed." *Id.* at 9. EPC agrees with the Staff that omitting the term "partial" from the construction is the better approach. Relying on Dr. Schubert, the Staff explains that '294 patent differentiates between a semi-insulating compensated p-type GaN from a conductive p-type GaN. Staff Br. at 9. EPC agrees with the Staff's assessment that the claims of the '294 patent would not permit "a GaN layer with any compensation whatsoever." *Id.* Rather, such compensation must be enough such that the claimed GaN gate is semi-insulating as the stated goal of the patent is to reduce gate capacitance and gate leakage, which is achieved through the use of a semi-insulating gate structure. '294 patent at 3:17-21; Schubert Responsive Decl. ¶¶ 18-24. EPC's proposed construction that included the term "partially cancels" was meant to align with this stated goal but agrees that the exclusion of that term as the Staff suggests "more accurately captures the meaning of this disputed limitation." Staff Br. at 9. EPC also agrees with the Staff that using the word

“impurity” in lieu of reciting “dopant” suffices, and that for the purposes of this invention, it is not necessary to include the word “imperfection.”

Accordingly, EPC is amenable to revising its proposed construction to make it consistent with the Staff’s construction, as indicated below:

“a semiconductor GaN gate material in which one type of ~~dopant~~, impurity, or ~~imperfection~~ (for example, donor) ~~partially~~ cancels the electrical effects of the other type of ~~dopant~~, impurity, or ~~imperfection~~ (for example, acceptor)”

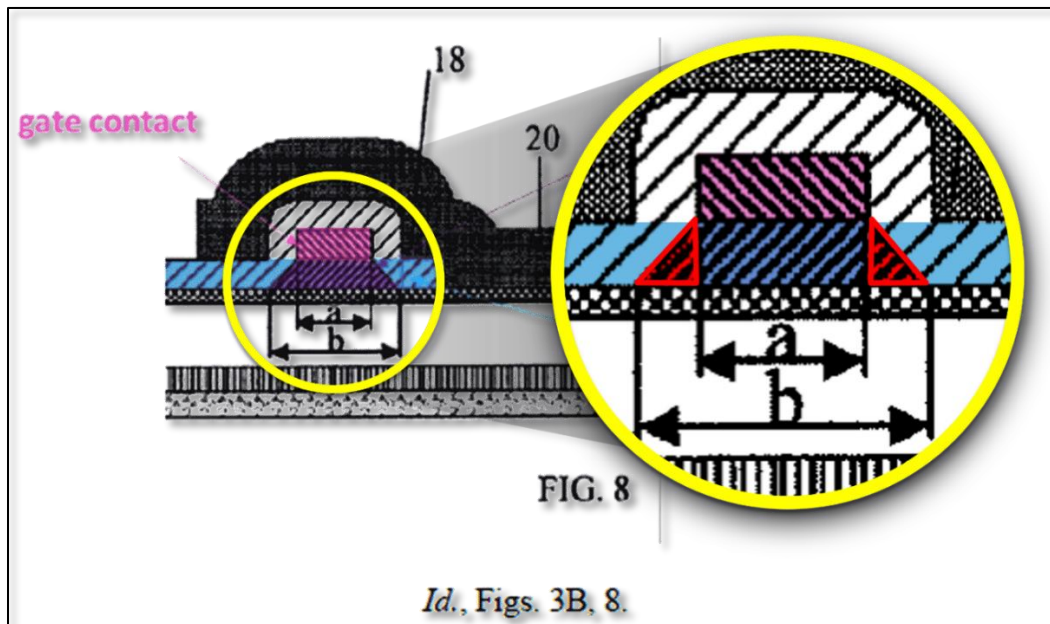
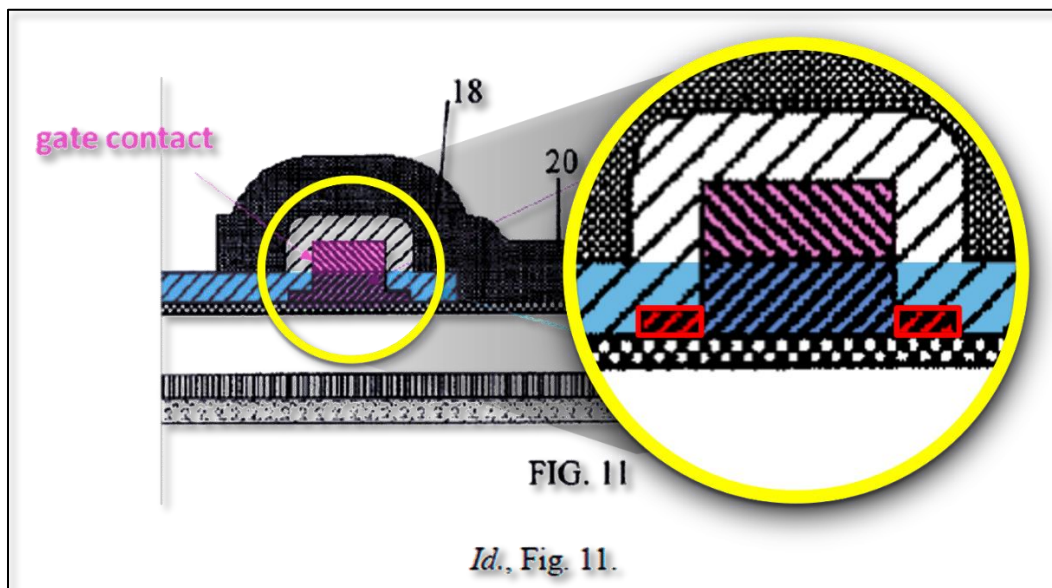
4. “Compensated GaN layer” Is Not a Product-by-Process Limitation

Relying on grammatical sleight-of-hand, Respondents contend that the compensated GaN layer “requires a deliberate compensation process.” Respondents’ Br. at 15-16. If Respondents were correct, then any use of a past-tense verb as an adjective to describe the properties of structures in a claim would transform those structures into process limitations. Both the Federal Circuit and its predecessor court have rejected the same argument that Respondents advance here. See EPC Br. at 10-11. Respondents’ further reliance on the Examiner’s rejection of the “compensated GaN layer” limitation over Bowers, Respondents’ Br. at 17, is inapposite. The Staff agrees. Staff Br. at 10-11. As Respondents’ own characterization of the rejection makes clear, the applicant overcame the rejection by pointing out that Bowers—although it discloses knowledge about passivation of p-type dopants—did not disclose forming a GaN layer. Nothing in the applicant’s response suggests that the applicant traversed the rejection based on Bowers because the claimed “compensated GaN layer” was formed, unlike Bowers, with a specific deliberate process of compensation.

B. “ETCHING AWAY THE DOPED GAN LAYER, EXCEPT A PORTION OF THE DOPED GAN LAYER BENEATH THE GATE CONTACT” (’508 PATENT, CLAIM 1)

Respondents’ construction should be rejected because it does not comport with the plain meaning of the term as describing an area to avoid with respect to the claimed etching and

because it excludes the preferred embodiments. The patent's own Figures 8 and 11, on which Respondents themselves rely, negate Respondents' contention that "every embodiment of the specification make[s] clear that the doped GaN layer is etched away in all regions extending outside the gate contact." Respondents' Br. at 23. Both figures clearly show that the regions of the GaN gate outside the gate contact (shown here with red borders) are clearly not etched.



Respondents' Br. at 25, 27 (red annotations added). Respondents nevertheless contend that these embodiments support their proposed construction because "the doped GaN layer in all regions outside the gate contact is at least ***partially etched***." Respondents' Br. at 26 (emphasis added). But Respondents' proposed construction requires that "***all regions*** [of the gate material] extending outside the gate contact" be etched away. The regions of gate material highlighted above in red are clearly not etched away and Respondents' proposed construction must be rejected. *Vitronics*, 90 F.3d at 1583 (constructions excluding preferred embodiments are "rarely, if ever, correct").

C. '508 PATENT, CLAIM 1

The dispute concerning this term is two-fold: First, whether all of the claimed steps must be performed in the order in which they are listed; and second, whether the "photo resistant pattern" step must be imported into subsequent etching steps. The law favors EPC on both issues.

Nothing in the claims or specification "directly or implicitly requires" that the step of removing the gate photo resistant pattern occurs after the second-listed etching step. *Mformation Techs., Inc. v. Rsch. In Motion Ltd.*, 764 F.3d 1392, 1398 (Fed. Cir. 2014). And nothing in the intrinsic evidence mandates that the pattern removal step must occur after the second-listed etching step.² The Staff contends that Dr. Schubert failed to identify any evidence supporting that a POSA need not use the photo resistant pattern itself for the second etching step. Staff Br. at 18. Dr. Schubert's extensive experience in the field, including with respect to photo masking,

² The Staff correctly notes that the only exemplary embodiment performs the distinct claim steps in the order listed. But, as EPC articulated in its opening brief, limiting a method claim to a particular order based on a preferred embodiment is improper. EPC Br. at 3-4.

is itself proper evidence on this point. And Dr. Schubert's responsive declaration now identifies multiple references supporting his earlier point. See Schubert Responsive Decl. ¶ 32-35.

Second, the intrinsic evidence does not mandate Respondents' requirement to "using the gate photo resistant pattern" for etching the compensated gate material. Respondents' Br. at 28. Respondents are correct that the specification describes the "present invention" as "using a single photo mask to etch both the gate contact and doped GaN layer." *Id.* But Respondents' proposal ignores this essential self-alignment element—the use of a **single photo mask**—and instead, limits the invention to using a single *photoresist* pattern/mask. To clarify, the single photo mask is used to pattern a photoresist pattern/mask, and that photoresist pattern may then be used to etch *one or more* layers of the gate structure. But nothing in the patent requires that the *photoresist pattern/mask* must be used to etch *all the layers*. The '508 patent is entirely directed to single photo masking process, not the limitation of using a single photoresist to etch multiple layers. See, e.g., '508 patent at 3:4-6, 3:45-47, 4:6-9, 4:41-42, 4:55-59. In one manner, a single photo mask can be used to pattern a photoresist mask which is then used to etch the metal, the photoresist mask is removed, and the metal is used as a hard mask subsequently etch the gate material. See Schubert Responsive Decl. ¶¶ 27-35. Alternatively, a single photo mask can be used to pattern a photoresist mask which is used as the mask for both the gate metal and the gate material. The point is that the claim covers at least both of these embodiments, and the photoresist mask need not remain through the etching of the entire gate structure. As Dr. Schubert explains, using metal masks, was well-known in the art and a POSA would have known to select such methods instead of using the same photoresist mask. See *id.* ¶¶ 27-29.

Indeed, Dr. Schubert clarifies that there are at least two ways of performing the process using one photo mask—including one in which the photoresist pattern is used for etching the

gate metal and then removed prior to etching the compensated gate material. Schubert Responsive Decl. ¶¶ 32-35. Respondents seek to limit the scope of the claims only to the former process, which is tantamount to limiting the scope of the claims to the preferred embodiments. *Praxair*, 543 F.3d at 1324 (importing limitations based on “isolated statements . . . pertain[ing] to specific embodiments of the invention rather than to the invention as a whole” is improper).

**D. “WHEREIN THE PAIR OF HORIZONTAL LEDGES
OF THE P-TYPE GATE MATERIAL ARE SELF-ALIGNED” (’335 PATENT, CLAIM 2) /
“A PAIR OF SELF-ALIGNED LEDGES” (’335 PATENT, CLAIM 5)**

Because the term “self-aligned” connotes structural characteristics to ledges and to the claimed transistor as a whole, the limitation is not a product-by-process limitation. EPC Br. at 11, 21 (discussing standard under *In re Nordt Dev. Co., LLC*, 881 F.3d 1371, 1375 (Fed. Cir. 2018)).

Nonetheless, Respondents ignore that the specification teaches that the self-aligned manufacturing process also “enable[s] the creation of a p-type gate with a minimum critical dimension (‘CD’).” EPC Br. at 23 (citing ’335 patent at 3:65 – 4:3). Because minimum CD is not a requirement of claim 1, the principle of claim differentiation is not at issue. And Respondents cannot rely on this principle “to overcome the specification’s description” of “self-aligned” as connoting structure, in addition to function. *Laitram LLC v. Ashworth Bros.*, No. 2022-1044, 2023 WL 3449148, at *4 (Fed. Cir. May 15, 2023). Indeed, a POSA would have readily understood minimum CD not only to be a structural feature of the claimed GaN transistor, but also one that would have resulted in improved functional characteristics that differentiated the claimed transistor over prior art not created with a self-aligned manufacturing process that utilized a single photo mask. See Schubert Decl. ¶¶ 78-80, 87. Accordingly, the term “self-aligned ledges” is not a product-by-process limitation.

E. Side Surface Terms ('335 PATENT, CLAIMS 1 & 5; '347 PATENT, CLAIM 1)

Respondents' construction as requiring the base of the GaN gate to be more than 10% wider than the top improperly limits the claims to an exemplary structure describe in the specification.³

EPC agrees that the construction of a claim term must give effect to the “overall object of the invention.” Respondents' Br. at 44 (relying on *Praxair*, 543 F.3d at 1324). At the same time, however, a construction that limits the scope of the claim based on “isolated statements . . . pertain[ing] to specific embodiments of the invention rather than to the invention as a whole,” *Praxair*, 543 F.3d at 1323, cannot be correct.

A GaN transistor having a p-type gate material that has a base that is 10% wider than the top is an exemplary structure described in ***one of twelve exemplary embodiments*** discussed in the '508 patent. See '508 patent at 5:23-28 (referring to Figure 8 and describing the fourth embodiment). This embodiment is not part of any description of the invention ***as a whole***. Rather, the shared specification of the '335 and '347 patents makes clear that the invention—as a whole—is an enhancement-mode GaN transistor with reduced gate leakage current. See '335 patent at 1:23-26; 2:34-38. A POSA would understand this goal is achieved by extending the path over which current travels from the gate, not by identifying any set of optimal proportions for the geometric shape of the p-type material. Schubert Responsive Decl. ¶¶ 38-39.

Thus, because EPC's construction (as well as the Staff's) only requires the side walls to be ***elongated*** towards the source and drain contacts without importing a specific exemplary

³ Respondents' construction cannot be correct for the additional reason that their construction, which would limit the claimed side surfaces only to “sloped” side surfaces, would exclude preferred embodiments from the scope of the claims, specifically the stepped side surfaces described in the specification of the '508 patent. EPC Br. at 29-31.

geometry, EPC's construction "most naturally aligns" with the '335 and '347 patents' "description of the invention." *Ormco*, 498 F.3d at 1313-14; *Praxair*, 543 F.3d at 1324.

Respondents are incorrect that limiting the construction of the side surfaces terms to structures that have a base that is 10% wider than the top is necessary to give effect to the overall object of the invention or to ensure that the claim is not "broaden[ed] . . . beyond what the intrinsic record describes" with respect to the problem addressed by EPC's invention.

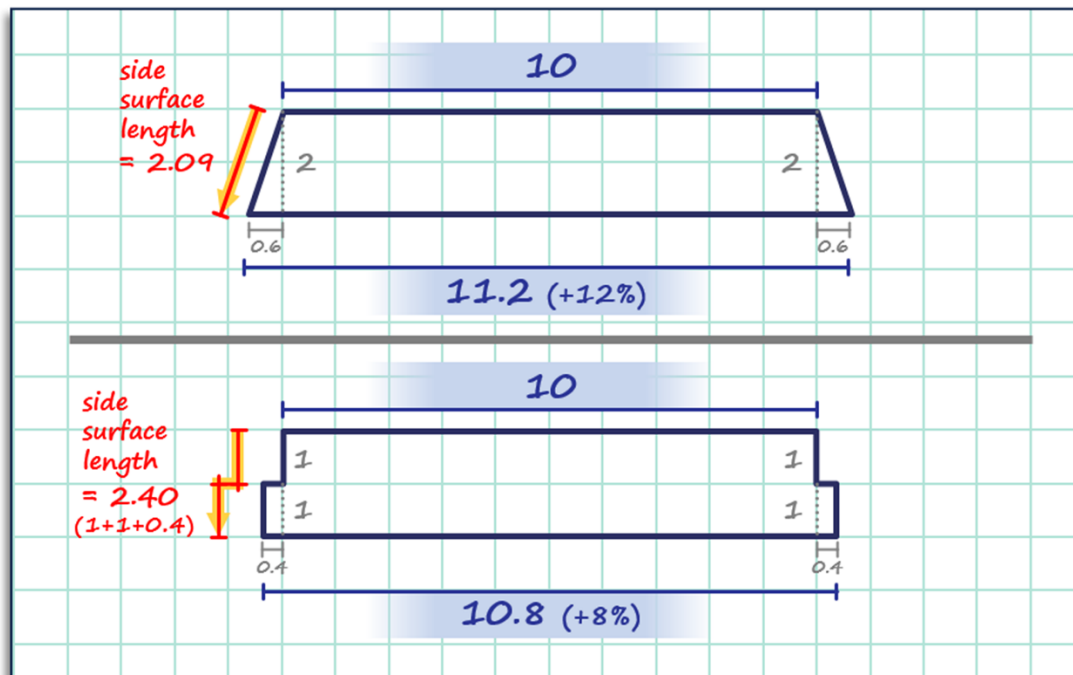
Respondents' Br. at 43. Respondents are concerned that unless the claims are restricted in the manner they propose, the claims could capture structures with vertical sidewalls that nevertheless "have a slightly larger base than top" due to purported limitations in the etching process that results in tapered, or rounded or curved features, at the base of a rectangular structure.

Respondents' Br. at 43-44 (citing Ex. 28 ¶ 0042).

Such concerns are unsubstantiated and cannot serve to limit the claimed side walls. As reflected in the '335 and '347 patents, EPC discovered a way to reduce leakage current emanating from the gate by elongating the path that such current takes to get to the source and drain. Moreover, a POSA understood that, at the time of the '335 and '347 patents, etching processes were available that allowed such tapers, rounded, and curved features to be avoided. Schubert Responsive Decl. ¶¶ 40-41. The claim does not exclude a structure resulting from utilizing an etching process that results in tapers, rounded, or curved features at the base of the p-type gate material, such that sidewalls are extended horizontally, thus elongating the current path from the gate to the source and drain.

Respondents' construction would also exclude structures that have longer side surfaces despite having a narrower base. Shown below are two exemplary gate structures with the same height (2 units)—one having a base that is 12% wider than the top with single, sloped edges (top

structure), and one having a base that is 8% wider than the top with stepped side surfaces (bottom structure). Based on the width of the base alone, the top structure would fall within the scope of the claim according to Respondents' position, whereas the bottom structure would not.



As the images above depict, despite the bottom structure having a base that is less than 10% wider than the top, it has a longer side surface than the structure where the base is proportionally wider (2.40 units compared to 2.09 units). Respondents' construction is arbitrary because there is no reason to exclude the bottom structure from the scope of the claims, which are directed to structures that elongate the gate current path.

**F. “ETCHING THE GATE METAL AND THE P-TYPE GATE MATERIAL” /
“ETCHING THE GATE METAL TO FORM A PAIR OF LEDGES” (’347 PATENT, CLAIM 1)**

As claim 1 of the ’347 patent makes clear, the two etching steps are directed to formation of certain structures. The first listed step is directed to formation of side surfaces (the “side-surfaces etching” term) whereas the second listed step is directed to formation of ledges (the “ledges-etching” term). Claim 1 also requires “forming a photoresist over the gate metal.”

The sole dispute with respect to the side surfaces-etching term is whether the claimed “photoresist” must be used to etch both the gate metal and the p-type gate material to achieve the claimed side surfaces. Respondents contend that limiting the term to require the use of the photoresist in the etching of both materials—the metal and the gate material—is necessary so that “the double-mask process disparaged by the ’347 patent” does not become encompassed within the scope of the claim. Respondents’ Br. at 47.

The problem with Respondents’ construction is that it once again unduly limits the claim to requiring the use of a single photoresist pattern for etching both the gate metal and the compensated p-type GaN material and thus impermissibly limits the single photo masking processes properly within the scope of the claims to one type of process—i.e., the process described in the exemplary embodiments.⁴ For the same reasons discussed above with respect to the ’508 patent, *supra* Section C, Respondents’ attempt to limit claim 1 based on a process described in the exemplary embodiments should be rejected. *Praxair*, 543 F.3d at 1324.

⁴ Contrary to the Staff’s position, the fact that the side surfaces etching step refers to etching of both the gate metal and p-type gate material does not suggest that the applicant “intended that the etching of both layers be done in a single etching step.” Staff Br. at 29. Rather, the fact that the gate metal and p-type gate material are referenced in the same etching step suggests merely that both materials must be etched to achieve the claimed side surfaces.

With respect to the ledges-etching term, Respondents incorrectly impute an order in the claim requiring that the ledges-etching step occur *after* the side-surfaces etching step. Respondents' sole basis for doing so is because the exemplary embodiment describes the steps in this order. But, as EPC discussed in its Opening Brief, nothing in the intrinsic evidence explicitly or implicitly requires that the ledges-etching step occur before, during, or after the side-surfaces etching step, and nothing in the specification *requires* such an order. The mere fact that this order is followed by the exemplary embodiments is not enough for that order to be imported into the claims. EPC Br. at 14-15.

Moreover, nothing about EPC's construction would render the ledges-etching step meaningless, as Respondents suggest. Respondents' Br. at 49. When read together, EPC's proposed construction mandates what the claim requires—an etching step that results in formation of side surfaces and an etching step that results in formation of ledges. Just as the claim language reflects, EPC's proposed construction is agnostic as to how or when each of the materials in the transistor, including the claimed gate metal and p-type gate material are etched. The specification describes an example of first etching the gate metal and p-type gate material to form the side surfaces followed by a second etching step whereby the gate metal is further etched to form ledges. But such an etching process is not described anywhere in the specification as comprising the whole invention. Accordingly, the claims cannot be limited to this exemplary process. *Praxair*, 543 F.3d at 1324. So long as two etching steps are performed—one to create side surfaces, and one to create ledges—the object of the invention is satisfied.

III. CONCLUSION

For the reasons stated above, the Court should adopt Complainant's proposed constructions.

WORD COUNT CERTIFICATION

Pursuant to Ground Rules 1.6 and 7.2, I hereby certify that the foregoing Complainant's Opening Claim Construction Brief complies with the word count limitation of Ground Rule 7.2. The brief contains 4,288 words, excluding those portions exempted by Ground Rule 1.6, as calculated by the word count indicated by the word-processing system used to prepare this brief.

Dated: October 6, 2023

Respectfully submitted,

/s/ Dipu A. Doshi

Dipu A. Doshi

R. Paul Zeineddin

Megan R. Wood

Walter D. Davis Jr.

Ameya V. Paradkar

Jonathan W.S. England

Sydney A. Salters

Benjamin R. Reyes

BLANK ROME LLP

1825 Eye Street, NW

Washington, DC

Tel: (202) 420-2604

Fax: (202) 420-2201

Email: EPC-ITC@BlankRome.com

Domingo M. Llagostera

BLANK ROME LLP

717 Texas Ave, Suite 1400

Houston, TX 77002

Tel: (713) 632-8682

Fax: (713) 228-6605

Stephanie C. Chomentowski

BLANK ROME LLP

One Logan Square

130 North 18th Street

Philadelphia, PA 19103

Tel: (215) 569-5344

Fax: (215) 569-5555

Cory R. Edwards

BLANK ROME LLP

444 West Lake Street, Suite 1650

Chicago, IL 60606
Tel: (312) 776-2589
Fax: (312) 776-2601

Cheryl S. Chang
Ping Zhang
BLANK ROME LLP
2029 Century Park East
Los Angeles, CA 90067
Tel: (424) 239-3472
Fax: (424) 239-3434

Joshua S. Reisberg
Peiran Zhang
BLANK ROME LLP
1271 Avenue of the Americas
New York, NY 10020
Tel: (212) 885-5553
Fax: (212) 885-5001

Benjamin Levi
Rett Snotherly
Tom Schaumberg
**LEVI SNOTHERLY &
SCHAUMBERG, PLLC**
1101 Connecticut Avenue, NW, Suite 450
Washington DC 20036
Tel: (202) 997-3711
Fax: (202) 331-1325
Email: EPCC-LSS-1366@LeviSnotherly.com

*Counsel for Complainant Efficient Power
Conversion Corporation*

CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing ***Complainant's Responsive Claim Construction Brief*** was served upon the following as indicated below on October 6, 2023:

The Honorable Lisa R. Barton Secretary to the Commission U.S. INTERNATIONAL TRADE COMMISSION 500 E Street, S.W. Washington, DC 20436	VIA ELECTRONIC FILING EDIS
The Honorable Clark S. Cheney Administrative Law Judge U.S. INTERNATIONAL TRADE COMMISSION 500 E Street, S.W. Washington, DC 20436	VIA BOX, NOTIFICATION VIA EMAIL Cheney1366@usitc.gov
Commission Investigative Attorney: R. Whitney Winston, Esq. Office of Unfair Import Investigations U.S. INTERNATIONAL TRADE COMMISSION 500 E Street, S.W. Washington, DC 20436	VIA ELECTRONIC MAIL Whitney.Winston@usitc.gov
Respondent Innoscience (Zhuhai) Technology Company, Ltd.: Lionel M. Lavenue FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, LLP 1875 Explorer Street, Suite 800 Reston, VA 90190	VIA ELECTRONIC MAIL Innoscience-ITC@Finnegan.com
Respondent Innoscience America, Inc.: Lionel M. Lavenue FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, LLP 1875 Explorer Street, Suite 800 Reston, VA 90190	VIA ELECTRONIC MAIL Innoscience-ITC@Finnegan.com

/s/ Dipu A. Doshi
Dipu A. Doshi