

Text of Request for Invalidation of the Patent Right

Part II Overview of reasons and evidence for request for invalidation

I. Overview of reasons for invalidation

Claims	Related article of law	Reason for invalidation
Claims 1-3	Article 26.3 of the Patent Law	Said claims are insufficiently disclosed by the description
Claims 1-2	Article 26.4 of the Patent Law	Said claims are not supported by the description
Claim 1	Rule 20.1 of the Implementing Regulations of the Patent Law	Said claim is unclear
Claims 1-3	Article 22.2 of the Patent Law	Said claims lack novelty
Claims 1-3	Article 22.3 of the Patent Law	Said claims do not involve an inventive step

II. Evidence used in this request for invalidation and using manners of evidence

Attachment 1: *Semiconductor Physics and Devices*, edited by LV, Shuyuan et al., Xidian University Press, February 2017;

Attachment 2: *Semiconductor and Thin Film Physics*, edited by YUN, Zhengzhong et al., University of Electronic Science and Technology of China, National Defense Industry Press, August 1981;

Attachment 3: Decision of reexamination No. 104791, decision date: January 15, 2016;

Attachment 4: *Behaviour of impurities and defects in GaN*, SHI, jinxing, Semiconductor Information, vol. 35, no. 1, February 1998;

Attachment 5: *Fundamentals of Solid-State Electronics*, edited by Chih-Tang Sah (USA), translated by RUAN, Gang et al., Fudan University Press, April 2003;

Attachment 6: *The Physics of Semiconductors*, edited by LIU, Enke, ZHU, Bingsheng, Xi'an Jiaotong University Press, National Defense Industry Press, December 1979;

Attachment 7: *Operation Principle and Manufacturing Process of Power Semiconductor Device*, edited by GHANDHI, S.K., translated by ZHANG, Guanghua, ZHONG, Shiqian et al., China Machine Press, September 1982;

Attachment 8: *Property and Test of Insulating Material (Accompanied by High-Voltage Test Devices)*, edited by LIU, Shaojun, Dadong Press, July 1954;

Attachment 9: US6498111B1, the date of publication: December 24, 2002;

Attachment 10: *p-type Doping of GaN*, XIE, Shiyong et al., Research & Progress of SSE, vol. 21, no. 2, May 2001;

Attachment 11: *Research progress based on GaN Material p-type doped*, LIU, Yibing, HUANG, Xinmin, LIU, Anning, et al., Infrared Technology, vol. 30, no. 3, March 2008;

Attachment 12: A comparative table of infringements filed by the patentee in the USITC Section 337 procedure and a translation thereof;

Attachment 13: CN102365747B, main contents of evidence of the reasons for the lack of novelty,

inventive step and industrial applicability, and instructions thereof;

Attachment 14: reference document 1 (D1): CN101107713, the date of publication: January 16, 2008;

Attachment 14-1: US2005145874A1 cited in D1 and a Chinese translation thereof;

Attachment 15: reference document 2 (D2): US2008/0087915A1 and a Chinese translation thereof, the date of publication: April 17, 2008;

Attachment 16: reference document 3 (D3): TW200414540A, the date of publication: August 01, 2004;

Attachment 17: the granted and announced document of the present patent: CN102365747B;

Attachment 18: business license of the applicant; and

Attachment 19: power of attorney.

Attachments 1-11 are used for proving the understanding of technical terms by those skilled in the art, and the background art of the patent at issue. Attachment 12 is used for proving the claiming of infringement of the patentee in 337 Survey involving a US family patent (claims 1-3 thereof correspond to claims 1-3 of the present patent). In attachment 13, proof purposes of attachments 1-12 and the mainly used paragraphs and contents thereof are summarized.

Attachments 14-16 are reference documents 1-3 for assessing novelty and inventive step, and the dates of publication thereof are all earlier than the date of priority of the present patent. In D1, the contents of attachment 14-1 and attachment 9 are incorporated in the present patent by reference in its entirety.

Part III Specific statement of reasons for invalidation

Claim 1 seeks to protect a Group III Nitride transistor. For the ease of analysis, the technical features of claim 1 are now numbered as follows.

“1-1 A Group III Nitride transistor comprising:

1-2 a substrate,

1-3 a set of III-N transition layers above the substrate,

1-4 a III-N buffer layer above the set of transition layers,

1-5 a III-N barrier layer above the buffer layer,

1-6 a compensated GaN layer above the barrier layer, and

1-7 a gate contact above the compensated GaN layer”.

Claim 2 further defines the compensated GaN layer in claim 1 to “the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen”.

Claim 3 further defines the acceptor type atoms in claim 2 to “the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca”.

I. Claims 1-3 are insufficiently disclosed in the description, which fails to comply with the provisions of Article 26.3 of the Patent Law.

The technical solution of claims 1-3 corresponds to the first embodiment of the description (paragraphs [0025]- [0029] in the description). The illustration in the description regarding the composition, implementation and technical effect of the “compensated GaN layer” in claim 1 has obvious contradiction and unclarity (section 1). In addition, the first embodiment intends to disclose a MISFET in the form of GaN transistor, and the functions implemented by the transistor and the functions implemented by various layers (e.g., a buffer layer) forming the transistor are also obviously unclear (section 2).

1. The “compensated GaN layer” in claim 1 corresponds to “compensated semiconductor layer 38” in the description, and the illustration in the description regarding the composition, implementation and technical effect of the compensated GaN layer has obvious contradiction and unclarity.

The main reasons are as follows.

First, through a conventional growth preparation procedure (e.g., MOCVD, MOVPE, etc.) of p-GaN (with the acceptor being Mg, Zn, C, etc.) with or without an additional hydrogen passivation, p-GaN that can be obtained is a deep level passivated highly-compensated semi-insulator, that is, the preferred/unique implementation of the compensated semiconductor 38 (the compensated GaN layer) of the present patent is obviously prior art. Therefore, the technical solution of claims 1-3 obviously covers the prior art, and thus those skilled in the art cannot clearly distinguish the present patent and the prior art (see section 1.1).

Second, according to the disclosure of the description, those skilled in the art are unclear about why “an additional hydrogen passivation” is provided, and the purpose of “the additional hydrogen passivation is to form a GaN layer of what resistivity (see section 1.2).

Third, the patentee does not clearly specify how the compensated GaN layer of the present patent can achieve two technical effects having opposite requirements for conductive electron density/resistivity at the same time (see section 1.3).

To facilitate the panel in understanding related opinions of the petitioner, the petitioner provides explanations of related terms in the patent at issue (see section 1.0).

1.0 Term Interpretation

Involved: compensated semiconductor, highly compensated semiconductor, enhancement-type devices (enhancement-type HEMT)

(1) The conventional definition of “compensated semiconductor” and “highly compensated semiconductor” in the art and the meaning of “compensated GaN layer” in this patent.

First, according to attachments 1-3, the definition of the compensated semiconductor in the art is that there are both donor impurities and acceptor impurities in a semiconductor, and according to attachment 3, the definition of a highly compensated semiconductor in the art is that, when a donor density and an acceptor density are equal ($N_A \approx N_D$), neither electrons nor holes provides an electrical conduction function.

According to attachment 1 (“Semiconductor Physics and Devices”, see Page 60), “the compensated semiconductor refers to a semiconductor containing both a donor impurity and an acceptor impurity therein. The compensated semiconductor can be formed by doping the acceptor impurity in an N-type semiconductor in which the donor impurity has been doped in advance, or by doping the donor impurity in a P-type semiconductor in which the acceptor impurity has been doped in advance. The compensated semiconductor can be classified according to the size relationship of the two impurities doped in the compensated semiconductor. If $N_A > N_D$, it is referred to as the P-type compensated semiconductor; if $N_D > N_A$, it is referred to as the N-type compensated semiconductor. If $N_A = N_D$, it is referred to as a fully compensated semiconductor. The conductive electron density of the fully compensated semiconductor is the same as that of an intrinsic semiconductor”.

According to attachment 2 (“Semiconductor and Thin Film Physics”, see Page 9), “The above-mentioned case where both the donor impurity and the acceptor impurity are present in the semiconductor so that the conduction effects are offset each other is referred to as the compensation effect of the impurities. The semiconductor with impurity compensation is referred to as the compensated semiconductor. For the highly compensated semiconductor ($N_A \approx N_D$), since neither electrons nor holes provide the conduction effect, although the resistivity of this material is very high as measured, it does not represent a very pure material. In this case, only supplemented by the measurement of other parameters such as the mobility and the like, its purity can be identified.”

As for the determination of compensated semiconductors, attachment 3 (Re-examination Decision No. 104791) is consistent with attachments 1-2, “**the compensated semiconductor is defined as a semiconductor containing both donor impurity atoms and acceptor impurity atoms in the same region**. Since the acceptor energy level is much lower than the donor energy level, electrons on the donor energy level first need to fill those on the acceptor energy level, so that the ability of a donor to provide electrons to a conduction band and the ability of an acceptor to provide holes to a valence band are weakened due to the fact that they are offset each other. Typically, N_d represents the donor density, and N_a represents the acceptor density. When $N_d > N_a$, the semiconductor is the n-type compensated semiconductor, and the electron density in the conduction band is $n = N_d - N_a$, which is called the equivalent donor density. Conversely, when $N_d < N_a$, the semiconductor is the p-type compensated semiconductor, and when $N_d = N_a$, electrons on all donors just ionize the acceptors, and conductive electrons in an energy band can only be generated by intrinsic excitation. At this time, the semiconductor is referred to as the fully compensated semiconductor, which exhibits the property of the intrinsic semiconductor. Typically, in the semiconductor fabrication technology, a method of compensation doping is used for obtaining the desired Fermi energy level”.

Second, the compensated GaN layer/the compensated semiconductor layer 38 in the present patent refers to passivation or compensation of Mg, etc. (a p-type acceptor impurity having the characteristic of tending to be combined with hydrogen) by hydrogen (serving as a donor) in the GaN layer.

As a specific semiconductor, GaN confronts an important problem in the development process that it is difficult to obtain p-type conductance, because when doped as the acceptor, Mg will be passivated by hydrogen in the semiconductor growth process to generate MgH. Therefore, the p-type conductance can be obtained typically only after doping followed by low energy electron beam

irradiation or thermal annealing (See attachment 4 “Properties of Impurities and Defects in GaN”, Section 2 “Doping of GaN and Properties of Various Impurities”)

It is recorded in attachment 4 Section 2.1 “Effect of Hydrogen in Doping” that **“H can be used as a donor H+ in p-type GaN, ... The conclusion that for Mg-doped GaN, if it grows at high temperatures above 1200 K, it is always highly compensated,** and the compensation center may be N vacancy or H (if H₂ is present) is consistent with the experimental fact. In molecular beam epitaxy (MBE) growth, the only way to obtain p-type GaN without treatment after growth is realized through low-temperature growth below 1000 K and the absence of H. **If H is present, the concentration of H is substantially equal to that of Mg,** the H donor and Mg acceptor actually form an electrically neutral complex with the binding energy of 0.7 eV. For the dissolution of the complex at the growth temperature, the binding energy is low enough, **whereas Mg and H will form an Mg-H pair when samples are cooled to room temperature”**.

In addition, “A compensated semiconductor layer 38 preferably includes AlGa_N or Ga_N having a deeply passivated p-type impurities, such as Mg, Zn, Be, Cd or Ca” as recorded in the description; and the claims of the patentee in the U.S. litigation (claims 1-3 completely correspond to claims 1-3 of this patent), according to SIMS data, if a certain level of hydrogen and Mg are detected in an accused infringing product, it is considered that the GaN layer is a compensated GaN layer.

According to the characteristics of the GaN semiconductor itself, in combination with the records of the description and the relevant claims of the patentee, it can be determined that the compensated GaN layer in the patent implicated refers to the passivation or compensation of hydrogen (acting as the donor) in the GaN layer for magnesium and the like (p-type acceptor impurity having the quality of being prone to bind with hydrogen).

(2) Higher resistivity (or lower conductive electron density) corresponding to a “semi-insulator” in this field, but there is no unified standard for the range of the corresponding resistivity (or conductive electron density) in the art.

According to attachment 5 (“Fundamentals of Solid-State Electronics”), conductors, semi-insulators and insulators are distinguished according to the resistivity/conductive electron density, with the resistivity of the conductor, the resistivity of the semi-insulator and the resistivity of insulator increasing sequentially and the conductive electron densities decreasing sequentially.

Material Category	Resistivity ($\Omega \cdot \text{cm}$)	Conductive electron density (cm^{-3})
Conductor	10^{-2} - 10^9	10^6 - 10^{17}
Semi-insulator	10^{10} - 10^{14}	10 - 10^5
Insulator	10^{14} - 10^{22}	1 - 10

According to attachment 5, the resistivity of the semiconductors is the minus second to ninth power of $10 \Omega \cdot \text{cm}$, the resistivity of the semi-insulator is the **tenth to fourteenth power of $10 \Omega \cdot \text{cm}$** , and the resistivity of the insulator is the fourteenth to twenty-second power of $10 \Omega \cdot \text{cm}$.

However, as recorded in attachment 6 (“Physics of Semiconductors”), the semi-insulators are those with the resistivity greater than the sixth to seventh power of $10 \Omega \cdot \text{cm}$.

As recorded in attachment 7 (“Working Principle and Fabrication Process of Power Semiconductor Devices”), materials with a resistivity exceeding $100 \Omega \cdot \text{cm}$ are often classified as semi-insulating materials.

As recorded in attachment 8 (“Properties and Tests of Insulating Materials: High-Voltage Testing Equipment Attached”), the resistivity of the semi-insulator is between the sixth to twelfth power of $10 \Omega \cdot \text{cm}$, and the resistivity of the insulator is above the twelfth power of $10 \Omega \cdot \text{cm}$.

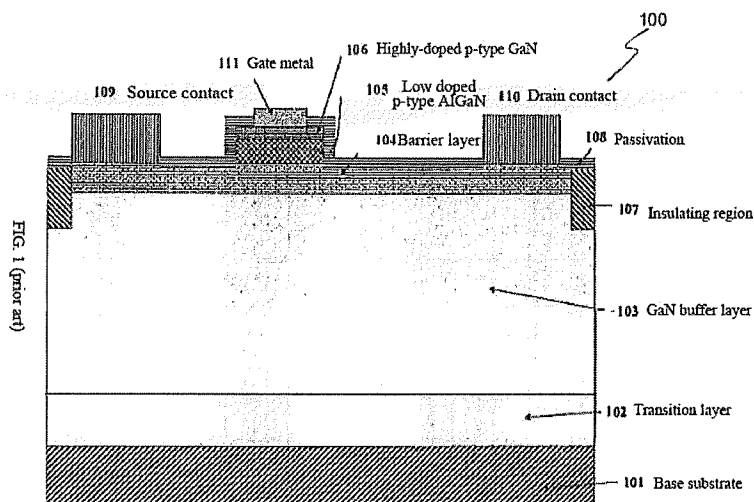
As can be seen, a semi-insulator is distinguished according to resistivity/conductive electron density. However, there is a relatively large difference between ranges of the resistivity/conductive electron density of the semi-insulator as defined in the prior art, and thus, when the semi-insulator is a key property for those skilled in the art to distinguish the present patent and the prior art, it is necessary to define a range of resistivity/conductive electron density corresponding to the semi-insulator in the present patent.

(3) p-GaN enhancement-type device (enhancement-type HEMT)

There are multiple implementations for the enhancement-type HEMT, one of which is a p-GaN enhancement-type device, that is, a p-GaN layer is provided between a barrier layer and gate metal (i.e., the position where the compensated GaN layer is located in this patent), and a certain density of p-type conductive electrons are required to make the device normally closed.

A general high-electron-mobility transistor (HEMT) is of a normally-open type or a depletion type, which achieves a high electron mobility by using a two-dimensional electron gas (2DEG) generated by arranging an AlGaN layer (i.e., a barrier layer 104 in FIG. 1) on a GaN layer (i.e., a buffer layer 103 in FIG. 1) (See Paragraphs 0003 to 0004 of this patent description).

Unlike normally-open or depletion type devices, the enhancement-type device (See Paragraph 0005 of this patent description) has p-GaN layers (105, 106) provided between the barrier layer 104 and the gate metal 111. Only when p-type carriers in the p-GaN layer have a certain concentration can the device be normally closed.



(4) MISFET

MISFET is a field effect transistor (FET) having an MIS (metal-insulator-semiconductor) structure.

1.1 Through a conventional growth preparation procedure (e.g., MOCVD, MOVPE, etc.) of p-GaN (with the acceptor being Mg, Zn, C, etc.) with or without an additional hydrogen passivation, p-GaN obtained may be a deep level passivated highly-compensated semi-insulator, that is, the preferred/unique implementation of the compensated semiconductor 38 (the compensated GaN layer) of the present patent is obviously prior art. Therefore, the technical solution of claims 1-3 obviously covers the prior art, and thus those skilled in the art cannot clearly distinguish the present patent and the prior art.

First, in the conventional growth process (e.g., MOCVD, MOVPE) of p-GaN, hydrogen passivation of p-type acceptors such as magnesium is unavoidable, and at this time, a highly compensated semi-insulator with deep hydrogen passivation is obtained. It can be seen that in a preferred (and only) implementation as recorded in the description, the highly compensated semi-insulator with deep hydrogen passivation is a natural result from the conventional growth process of p-GaN.

It is recorded in attachment 9 (US6498111B1) submitted by the petitioner that receptor passivation of a reactor cooling device cannot be avoided when the receptors are magnesium, zinc, carbon and the like, when p-GaN is grown by MOCVD: "During growth of the GaN material and subsequent reactor cooling, hydrogen is common in an MOCVD reactor and typically comes from two sources. In the growth process, hydrogen is typically used as a carrier gas for a growth source gas. Furthermore, ammonia (NH₃) is used as a source gas for nitrogen (N) during growth of the GaN material and is also used for stabilizing the GaN material during reactor cooling. Hydrogen is a by-product of ammonia in the growth and cooling processes. In the conventional GaN growth process, there is sufficient hydrogen in the reactor to cause passivation of a p-type region during cooling." (See Column 2, Paragraph 1 of the translation of attachment 9). The p-type acceptor that is easily passivated by hydrogen include magnesium, zinc, carbon and the like (See Column 1, Paragraph 3 of the translation of attachment 9). It is impractical to remove all hydrogen sources and passivation during reactor cooling is unavoidable (See Column 2, Paragraph 2 of the translation of attachment 9).

In addition, hydrogen passivation of the acceptors such as magnesium (forming an Mg-H complex) causes the acceptors such as magnesium to lose activity, resulting in that the material becomes an insulating or weak p-type in a growth state. In general, the purpose of doping is to obtain certain conductive electrons; and the difficulty in obtaining low-resistivity p-GaN due to hydrogen passivation is a major factor that has hampered the development of p-GaN (See attachment 9 and attachment 10 "p-type doping of GaN materials", and attachment 11 "Research progress based on p-type doping of GaN materials).

For example:

A common problem as recorded in attachment 9 (See Column 1, Paragraph 3 of the translation of attachment 9) is that the acceptors such as Mg, zinc (Zn), carbon (C) and others are electrically passivated by hydrogen atoms. The smaller hydrogen atoms diffuse into the GaN material, where

they neutralize the Mg acceptors and holes generated by Mg. The passivation process causes the Mg receptor to lose activity, resulting in that the material becomes an insulating or weak p-type in a growth state".

It is recorded in attachment 10 (See P206, Section 3, Paragraph 2): "However, the initial progress was not smooth. When GaN is grown by MOCVD, even if Mg up to 10^{19} to 10^{20} cm⁻³ is doped, GaN is still semi-insulating, with a resistivity up to 10^8 $\Omega \cdot \text{cm}$, and this phenomenon is referred to as passivation of Mg. Mg can be activated only by retreatment after growth to obtain p-type GaN".

Second, to obtain lower resistivity, it is necessary to reduce the level of hydrogen passivation in p-GaN by means of an additional process of activating p-type carriers (e.g., annealing) or designing a special structure (e.g., a passivation layer). However, hydrogen passivation in p-GaN is hardly eliminated completely. Therefore, even if the patentee claims that the scope of protection of claim 1 is larger than the scope of the preferred embodiment, that is, the degree of hydrogen passivation of an acceptor (e.g., Mg) is not defined, claim 1 obviously covers the residual hydrogen passivation in p-GaN in the prior art even after hydrogen passivation is reduced by means of an additional activation process or a special structure design.

It can be known from attachments 9-11 provided by the petitioner that the degree of hydrogen passivation can be reduced by means of an additional activation process (e.g., annealing), thereby obtaining p-GaN with relatively low resistivity, but only a part of hydrogen passivation can be removed, and a certain degree of hydrogen passivation still remains.

For example, it is recorded in attachment 10 (See P208, the last paragraph to P209, Paragraph 1, i.e., the last paragraph of Section 4) that "However, even after LEEBI or RTA treatment, the hole concentration of Mg-doped GaN usually does not exceed 10^{18} cm⁻³, and the doping efficiency is only 0.1% to 1%, which cannot meet the device requirements very well. On the one hand, there is still a large amount of H [13] remaining in the treated Mg-doped GaN, and these H compensate for part of the receptor Mg".

1.2 According to the disclosure of the description, those skilled in the art is unclear about why "an additional hydrogen passivation" is provided, and the purpose of "the additional hydrogen passivation is to form a GaN layer of what resistivity.

The patent at issue specifies, in paragraph [0028] in the description, that "an additional hydrogen passivation" is executed after the growth of the compensated semiconductor 38:

"Referring to FIG. 7, the next step is to grow a compensated semiconductor layer 38 over the barrier layer 34. Referring to FIG. 8, the next step is to deposit a gate contact 37 on the compensated semiconductor layer 38... The gate photo resist mask is then removed. An additional hydrogen passivation can be performed by exposing the device to ammonia or hydrogen plasma at a high temperature."

First, the description does not clearly specify the rationality and necessity of the "additional hydrogen passivation".

According to the evidences provided by the petitioner, it can be seen that, in the art, a highly compensated semi-insulating GaN layer can be obtained during the growth of the p-GaN layer

without an additional annealing process (with the acceptor being Mg, etc.) (see attachment 4 and attachments 11-13). That is, a compensated semiconductor 38 formed by natural growth can meet the requirements of the preferred embodiment of the present patent for the attributes of the p-GaN before the execution of the additional hydrogen passivation.

The purpose of the “additional hydrogen passivation” is obviously to improve the degree of hydrogen passivation. According to the preparation method corresponding to the transistor of claim 1 provided in the description, the rationality and necessity of the execution of the “additional hydrogen passivation” are difficult to understand for those skilled in the art.

Second, semi-insulation does not correspond to a certain range of resistivity, and thus those skilled in the art do not know when the “additional hydrogen passivation” is required, and cannot determine the degree of the “additional hydrogen passivation”.

Regarding the preferred embodiments disclosed in the present patent, “semi-insulation” corresponds to a very vague resistivity range (point (2) in section 1.0 of this opinion), and according to this, those skilled in the art cannot know when the “additional hydrogen passivation” is required, and also cannot know the purpose of the “additional hydrogen passivation” is to form a GaN layer of what resistivity.

Assuming that the patentee claims the scope of protection of claim 1 is larger than the scope of the preferred embodiment, that is, the degree of hydrogen passivation of an acceptor (e.g., Mg) is not defined, since those skilled in the art can generate p-GaN of different resistivity by means of changing annealing parameters such as annealing temperature, and a certain amount of residual hydrogen passivation is still present even after an annealing process, at this time, those skilled in the art cannot determine when the “additional hydrogen passivation” is required, and cannot determine the degree of the “additional hydrogen passivation”.

1.3 The patentee does not clearly specify how the compensated GaN layer of the present patent achieves two technical effects having opposite requirements for conductive electron density/resistivity at the same time.

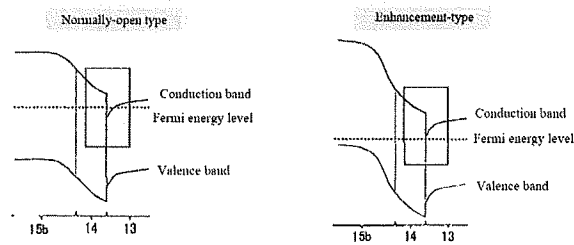
Require low resistivity	Require high resistivity
The enhancement mode device requires p-type carriers in p-GaN having certain density	Conductive electrons in p-GaN are highly compensated, and the p-GaN becomes a semi-insulating material.
Disclosure of the patent at issue [0026] “... compensated layer 38 leads to <u>enhancement mode devices</u> ”.	Disclosure of the patent at issue [0026] “using a compensated semiconductor layer 38 leads to low gate leakage during device operation”, and “the insulating nature of compensated layer 38 reduces the gate capacitance of the device”. [0029] “the passivation of a p-type impurity using hydrogen”. The passivation leads to two differences. First, in GaN transistor 1, the

	compensated semiconductor layer 38 is a <u>highly compensated semi-insulating material</u> , ... Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art".
Technical effect 1	Technical effect 2
First, when the resistivity is high enough to make the compensated semiconductor layer 38 "a highly compensated semi-insulating material", the density of the conductive p-type electrons and the density of hydrogen ions are equal ($NA \approx ND$), almost all the conductive p-type electrons are passivated by the conductive p-type electrons, and thus the device cannot serve as an enhancement mode device. Second, it is assumed that the patent right emphasizes the compensated GaN in the present patent does not have to have the resistivity to become "the highly compensated semi-insulating material", and it is only necessary to have resistivity higher than general p-GaN. However, due to a different process and a different application scenario, the resistivity of the general p-GaN does not have an explicit range, and those skilled in the art cannot determine what is the higher resistivity, and therefore cannot determine what compensated GaN layer is a compensated GaN layer belonging to the technical contribution of the present invention.	

The operation principle of the enhancement mode device determines that p-type carriers in the p-GaN must have a certain density.

The conduction bands of the normally-open device (as shown in the left panel of the figures below) have discontinuity at a heterogenous interface between a first nitride semiconductor layer 13 (GaN) and a second nitride semiconductor layer 14 (AlGaN). At the heterogenous interface, the conduction bands are located at a lower energy level than the Fermi energy level (there is a triangular region where the conduction bands are below the Fermi energy level in the red box), thus generating 2DEG.

As for the enhancement-type device (as shown in the right panel of the figures below), a third nitride semiconductor layer 15 is provided on the second nitride semiconductor layer 14, and only if the p-type impurity of the layer is activated (namely, having a certain concentration) can the energy levels of the second nitride semiconductor layer 14 and the first nitride semiconductor layer 13 be increased until the conduction bands at the heterogenous interface between the first nitride semiconductor layer 13 and the second nitride semiconductor layer 14 are located at an energy level higher than the Fermi energy level (the conduction bands in the red box are all above the Fermi energy level). At this time, 2DEG will not be generated at the heterogenous interface, thus obtaining the normally-off property of a nitride semiconductor transistor. It can be seen that when the p-type impurity in the semiconductor layer 16 is not activated or is deeply passivated, the normally-off function cannot be realized, that is, the transistor is no longer the enhancement-type device (the above-mentioned principle is correspondingly described in Page 3, Paragraph 0038 of the description of reference document 2)



2. As recorded in the description, the first embodiment implements a transistor which is both an MISFET and the enhancement-type device (HEMT). However, according to technical knowledge of the persons skilled in the art, the structure of the first embodiment hardly forms the transistor which is both the MISFET and the enhancement-type device (HEMT). Since the functions implemented by the device determine the functions implemented by each layer, the persons skilled in the art also cannot clearly understand what is meant by “a buffer layer 33 separates a transition layer 32 from a barrier layer 34” emphasized in the description.

Background art	First embodiment
Paragraph [0005] of the description: “a device 100 includes... a base substrate 11, a transition layer 102 with a thickness of about 0.1 to about 1.0 μm typically formed from AlN and AlGaIn, a buffer material 103 with a thickness of about 0.5 to about 10 μm typically formed from <u>GaN</u>, a barrier material 104 with a thickness from about 0.005 to about 0.03 μm typically formed from <u>AlGaIn</u> (where the ratio of Al to Ga is about 0.1 to about 0.5), p-type AlGaIn 105, highly-doped p-type GaN106, an insulating	Paragraph [00025] of the description: “FIG. 2 shows an <u>MISFET in the form of a GaN transistor 1</u> according to one embodiment of the present invention. A base substrate 31 for example.... The transition layer 32 is located on and in contact with the base substrate 31. The transition layer 32 may include, for example, AlN or AlGaIn, and has a thickness of between 0.1 and 1.0 μm. <u>The buffer layer 33 separates the transition layer 32 from the barrier layer 34.</u> The buffer layer 33 is preferably

region 107, passivation region 108, ohmic contact metals 109 and 110, and a gate metal 111 formed from nickel (Ni) and gold (Au) metal contacts located above a p-type GaN gate”. [Description] The structure in the background art is a typical structure of the <u>enhancement-type device (HEMT)</u>. The GaN layer (buffer layer) and the AlGaN layer (barrier layer) form a heterojunction to generate the two-dimensional electron gas, and the setting of the p-type GaN makes the device normally closed.	formed from InAlGa_N, has any concentration of In and Al (including 0% In and/or Al), and has a thickness of 0.5 to 3 μm. The barrier layer 34 is formed from AlGa_N, has a thickness of between 0.005 to 0.03 μm, and has a percentage of Al of about 10% to 50%. A gate contact 37 is for example formed from Ta, Ti, TiN, W or WSi₂, ... In accordance with the present invention, the compensated semiconductor layer 38 is formed over the barrier layer 34 and located below the gate contact 37.....”. [Description] The first embodiment is <u>an MISFET</u>, and the description only emphasizes that the effect of the buffer layer is the effect that “the buffer layer 33 separates the transition layer 32 from the barrier layer 34”.
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The device functions are different, as well as the requirements for each layer. The persons skilled in the art have a different understanding of the device functions which can be implemented by the first embodiment, because the effect of the buffer layer emphasized therein cannot be understood.

According to “The high doping level of the compensated layer 38 leads to the formation of the enhancement-type device” as recorded in Paragraph 0026 of the description, Embodiment 1 is a transistor which is both an MISFET and an enhancement-type device. However, according to the technical knowledge, it is difficult to form the transistor which is both the MISFET and the enhancement-type (HEMT) by simply increasing the resistivity of the p-type GaN in the enhancement-type device, that is, the structure of the embodiment is relatively difficult to form the transistor which is both the MISFET and the enhancement-type (HEMT).

Since there is different understanding of the functions implemented by the device, and there is

also a different understanding of the functions that can be implemented by each layer, for example, as for the enhancement-type (HEMT) in the background art, the persons skilled in the art generally considers that the transition layer is provided for nucleation or lattice matching, and the buffer layer (GaN layer) and the barrier layer (AlGaN layer) are provided to form the heterojunction to generate the two-dimensional electron gas. However, the first embodiment emphasizes that the transistor is the MISFET. According to the comparison between the description of each layer in the background art and the description of each layer in the first embodiment in the above table, there are many differences between the description of each layer in the first embodiment and the description of each layer in the background art, in particular, the first embodiment additionally emphasizes that “the buffer layer 33 separates the transition layer 32 from the barrier layer 34”, and what is meant by the above difference and the emphasized “the buffer layer 33 separates the transition layer 32 from the barrier layer 34” is unclear to the persons skilled in the art.

II. Claims 1-2 are not supported by the description, and are not in conformity with the provisions of Article 26, Clause 4 of the Patent Law

1. The “compensated GaN layer” in claim 1 generalizes a wider scope, and the description only gives a specific “preferred” implementation. The persons skilled in the art cannot clearly understand whether other implementations besides the preferred implementation can also solve the same technical problem and achieve the same technical effect.

With regard to the superordinate concept “compensated GaN layer”, the description only gives a “preferred” implementation (See Paragraphs 0025 and 0029 of the description) “FIG. 2 shows an **MISFET** in the form of a GaN transistor 1 according to one embodiment of the present invention. The compensated semiconductor layer 38 preferably includes **AlGaN or GaN having deeply passivated p-type impurities**, such as Mg, Zn, Be, Cd or Ca.” and “**passivation of p-type impurities with hydrogen**”. Passivation results in two differences. First, in the GaN transistor 1, the compensated semiconductor layer 38 is a **highly compensated semi-insulating material**”.

In the preferred embodiment, the acceptor is “Mg, Zn, Be, Cd or Ca”, hydrogen acts as the donor to passivate or compensate for the acceptors such as Mg, and the concentration of hydrogen is equivalent to that of Mg ($N_A \approx N_D$), forming high compensation, that is, neither the electrons nor the holes provide a conduction effect (See attachment 3 for the definition of the highly compensated semiconductor). At this time, the p-GaN is an insulator or semi-insulator with high resistivity.

Those skilled in the art does not know whether there is other “compensated GaN layer” implementation methods than this preferred embodiment to solve the technical problem of the present invention and achieve the same technical effect.

2. Claim 2 further defines the “compensated GaN layer”, but is still summarization of the preferred embodiment. Those skilled in the art cannot be clear about whether there are other implementation methods than the preferred method to solve the same technical problem and achieve the same technical effect.

Claim 2 further defines the “compensated GaN layer” to “the compensated GaN layer contains acceptor type dopant atoms **passivated with hydrogen**”.

2.1 Claim 2 does not define the type of the “acceptor type dopant atoms”, which comprise “acceptor type dopant atoms” of types that cannot solve the technical problem of the present invention and cannot achieve the same technical effect, for example, “the group consisting of C, Fe, Mn, Cr and V”.

2.2 Claim 2 does not define the degree of the “hydrogen passivation”, and therefore obviously comprises the technical solutions that cannot solve the technical problem of the invention and cannot achieve the same technical effect (e.g., the solution in FIG. 1 (prior art)).

The description merely discloses a method for implementing an insulator or a semi-insulator using hydrogen passivation: the corresponding implementation method involves that the transistor having the structure of “metal-insulator-semiconductor” is MISFET, a compensated semiconductor layer 38 “comprising AlGa_N or Ga_N with a deep level passivated p-type impurity” is below a gate contact (metal) (see paragraph [0025]), and the compensated semiconductor layer 38 is “a highly compensated semi-insulating material” (see paragraph [0029]).

Claim 2 does not make any definition to the degree or result of the “hydrogen passivation”. Since the acceptor is an impurity such as Mg, the hydrogen passivation is inevitable, and therefore, said claim obviously comprises the technical solution of the prior art, and the solution cannot solve the technical problem to be solved by the present invention and cannot achieve the same technical effect.

III. The scope of protection of claim 1 is unclear, which fails to comply with the provisions of Rule 20.1 of the Implementing Regulations of the Patent Law.

The scope of protection of “compensated Ga_N layer” in claim 1 is unclear. In the art, hydrogen passivation of p-Ga_N (with the acceptor being Mg, etc.) is inevitable during growth, that is, the p-Ga_N (with the acceptor being Mg, etc.) obtained through a conventional preparation procedure is a “compensated Ga_N layer”, and Mg is one of the acceptors that are earliest used for implementing the p-Ga_N. As can be seen, those skilled in the art even cannot distinguish the technical solution of claim 1 and the technical solution of the background art according to the “compensated Ga_N layer” of claim 1, and therefore, claim 1 obviously defines an unclear scope of protection.

IV. claims 1-3 lack novelty and fail to comply with the provisions of Article 22.2 of the Patent Law

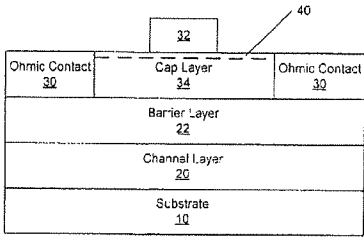
1. Independent claim 1 lacks novelty with respect to D1, D2 or D3, and fails to comply with the provisions of Article 22.2 of the Patent Law.

1.1 Claim 1 lacks novelty with respect to D1.

The correlation between the features of claim 1 of the present patent and the disclosure of D1 (CN101107713A) is as shown in the following table. It should be noted that the following table is only an exemplary example, and the technical content disclosed in D1 is not limited to the text and images listed in the table below.

1-1 A Group III Nitride transistor comprising:	[Explanations] <u>Feature 1-1 has been disclosed in D1:</u> D1 discloses a Group III Nitride transistor. [The specific content disclosed in D1] <u>[See page 2, the penultimate paragraph in Description of D1]</u> “Some embodiments of the present invention provide <u>Group III-nitride high electron mobility transistors</u> and methods of <u>fabricating Group III-nitride high electron mobility transistors...</u>” <u>[See page 9, the last paragraph in Description of D1]</u> “Embodiments of the present invention may be particularly well suited for use in nitride-based devices such as Group III-nitride based HEMTs). As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In)”.
1-2 a substrate,	[Explanations] <u>Feature 1-2 has been disclosed in D1:</u> The substrate disclosed in D1 is equivalent to the substrate in claim 1. [The specific content disclosed in D1] <u>[See FIG. 2A and page 12, the last paragraph in Description of D1]</u> Figure 2A “Turning to Figures 1A and 1B, a substrate 10 is provided on which nitride based devices may be formed. In particular embodiments of the present invention, the substrate 10 may be a semi-insulating silicon carbide (SiC) substrate that may be, for example, 4H polytype of silicon carbide. Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes.” <u>[See page 13, the penultimate paragraph in Description of D1]</u> “Although silicon carbide may be used as a substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like.”

1-3 a set of III-N transition layers above the substrate,	[Explanations] <u>Feature 1-3 has been disclosed in D1:</u> The AlN buffer layer (not shown in the figures) disclosed in D1 is equivalent to the transition layer in claim 1. According to the disclosure of the description (see paragraph [0025] of the present patent), the transition layer of the present patent may comprise AlN. [The specific content disclosed in D1] <u>[See page 13, paragraph 2 in Description of D1]</u> “Optional buffer, nucleation and/or transition layers (not shown in the figures) may be provided on the substrate 10. For example, <u>an AlN buffer layer may be provided</u> to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device.”
1-4 a III-N buffer layer above the set of transition layers,	[Explanations] <u>Feature 1-4 has been disclosed in D1:</u> The channel layer 20 (the channel layer 20 is a Group III-nitride) disclosed in D1 is equivalent to III-N buffer layer in claim 1. [The specific content disclosed in D1] <u>[See FIG. 2A, page 13, the last paragraph and page 14, paragraph 2 in Description of D1]</u> Figure 2A “Returning to Figures 1A and 1B, a channel layer 20 is provided on the substrate 10. The channel layer 20 may be deposited on the substrate 10 using buffer layers, transition layers, and/or nucleation layers as described above... In some embodiments of the present invention, <u>the channel layer 20 is a Group III -nitride</u>, such as $\text{Al}_x\text{Ga}_{1-x}\text{N}$ where $0 \leq x < 1$, provided that the energy of the conduction band edge of the channel layer 20 is less than the energy of the conduction band edge of the barrier layer 22 at the interface between the channel and barrier layers. In certain embodiments of the present invention, $x = 0$, indicating that the channel layer 20 is GaN. The channel layer 20 may also be other Group III-nitrides such as InGa₂N, AlInGa₂N or the like. The channel layer 20 may be undoped

	(“unintentionally doped”) and may be grown to a thickness of greater than about 20 Å.”
1-5 a III-N barrier layer above the buffer layer,	[Explanations] <u>Feature 1-5 has been disclosed in D1:</u> The barrier layer 22 (the barrier layer 22 may be a Group III-nitride) disclosed in D1 is equivalent to the III-N barrier layer in claim 1. [The specific content disclosed in D1] <u>[See FIG. 2A and page 14, paragraphs 1-2 from the bottom in Description of D1]</u>  Figure 2A “A barrier layer 22 is provided on the channel layer 20. The channel layer 20 may have a bandgap that is less than the bandgap of the barrier layer 22 and the channel layer 20 may also have a larger electron affinity than the barrier layer 22. The barrier layer 22 may be deposited on the channel layer 20. In certain embodiments of the present invention, the barrier layer 22 is AlN, AlInN, AlGaIn or AlInGaIn with a thickness of between about 0.1 nm and about 40 nm. <u>The barrier layer 22 may be a Group III-nitride</u> and has a bandgap larger than that of the channel layer 20 and a smaller electron affinity than the channel layer 20.”
1-6 a compensated GaN layer above the barrier layer, and	[Explanations] <u>Feature 1-6 has been disclosed in D1:</u> The cap layer 34 disclosed in D1 is based on a GaN layer or a GaAlN layer, the doped region 40 is doped with p-type dopant (e.g., Mg), and the cap layer 34 in the embodiment in which no passivation layer is provided has a highly compensated semi-insulating property, which corresponds to the compensated GaN layer in claim 1. <u>The specific reasons are as follows:</u> In D1, attachment 14-1 (US2005145874A1) and attachment 9 (US6498111) are incorporated by reference in their entireties. When the dope region 40 is doped with a p-type dopant (e.g., Mg), hydrogen passivation is inevitable or is an intrinsic defect and impurity. According to attachment 9, the purpose of the provision of a passivation layer is to

replace an annealing process to reduce the degree of hydrogen passivation in p-GaN. Regarding the embodiment in which no passivation layer is provided, i.e., corresponding to a cap layer p-GaN in the embodiment in which no passivation layer is provided, according to the disclosure of D1, no other technical means for reducing the degree of hydrogen passivation is provided in the solution, therefore, the cap layer p-GaN in the embodiment obviously has a highly compensated semi-insulating property.

[Contents specifically disclosed in the reference document]

[See FIG. 2A of reference document 1, and the superscript, Page 18, Paragraph 2 of the description]

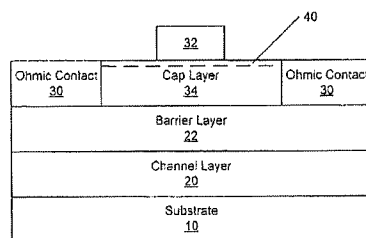


Figure 2A

“FIGS. 2A and 2B illustrate an electron mobility transistor having a cap layer 34, 34’ according to further embodiments of the present invention. As previously discussed with reference to FIGS. 1A and 1B, a substrate 10, a channel layer 20, a barrier layer 22, an ohmic contact 30, and a gate contact portion 32 may be provided. As shown in FIGS. 2A and 2B, the cap layer 34, 34’ includes a doped region 40 at or near its outer surface. The cap layers 34, 34’ may be a GaN based cap layer (such as GaN and/or GaAlN, etc.), for example, as discussed in the patents and patent applications incorporated herein by reference. In some embodiments of the present invention, the doped region 40 is doped with a p-type dopant (such as Mg, Be, Zn, Ca, and/or C, etc.). The technology for co-doping Group III nitride materials is described, for example, in U.S. Patent Application No. 10/752970, entitled “CO-DOPING FOR FERMI LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES”, filed on January 7, 2004, which is incorporated herein by reference, as if set forth in its entirety.”

[See the superscript, Page 19, the last paragraph to Page 20, Paragraph 1 of the description of reference document 1]

“In other embodiments, the doped region 40 is a region doped with the p-type dopant. In particular embodiments of the present invention without a grid recess, the doped region 40 extends into the cap layer 34 from 2.5A to

about 100A. With the p-type dopant, the doped region 40 can provide a dopant concentration from about 10^{16} to about 10^{22} cm⁻³. The p-type dopant may be Mg, Be, Zn, Ga, and/or C. The doping level should be high enough **to reduce leakage current in embodiments without a recessed grid** and to be a dominant “surface” state, but not so high as to provide introduce traps or leakage paths by becoming a conductive layer.”

[See the superscript, Page 17, Paragraph 3 of the description of reference document 1]

A conventional passivation layer or a BN passivation layer as described below may also be formed on the structure shown in FIGS. 1A and 1B. For example, a SiN layer, and a very thin SiN layer in other embodiments may be formed in situ. MgN passivation layers may also be utilized, and **are described in U.S. Patent No. 6498111**, entitled “FABRICATION OF SEMI CONDUCTOR MATERIALS AND DEVICES WITH CONTROLLED ELECTRICAL CONDUCTIVITY”, **which is incorporated herein by reference, as if set forth in its entirety**”.

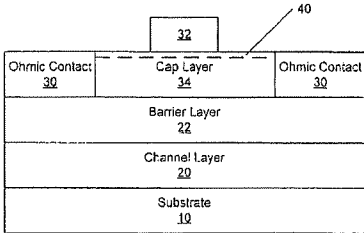
[Incorporated by reference into Paragraph [0032] of attachment 14-1 in reference document 1]

“For example, the group III nitride layer may also be annealed to remove **intrinsic defects and impurities, such as hydrogen**, which may result from co-doping of the semi-insulating group III nitride layer. For example, post-growth nitrogen annealing may be performed on the group III nitride layer”.

[Incorporated by reference into Column 1, Paragraph 1, Paragraph 3, and Column 2, Paragraph 1 of the translation of attachment 9 in reference document 1]

“The present invention relates to a method for achieving a desired conductivity in a doped semiconductor material affected by dopant passivation. The present invention specifically teaches a method for fabricating a passivation barrier layer to prevent or reduce passivation of dopant in the growth process of the semiconductor, thereby eliminating the need for in-situ or ex-situ annealing steps.

“In growing a GaN p-n junction diode by using metal-organic chemical vapor deposition (MOCVD), it is difficult to grow a p-type material with good structural, optical, and electrical integrity. A p-type region of a GaN junction diode is typically grown in the MOCVD reactor by adding magnesium (Mg) to obtain the desired conductivity. However, **a common problem is that the acceptors such as Mg, zinc (Zn) carbon (C) and others are electrically passivated by hydrogen atoms**. The smaller hydrogen atoms diffuse into the GaN material, where they neutralize the Mg acceptors and holes generated by Mg. **The passivation process causes**

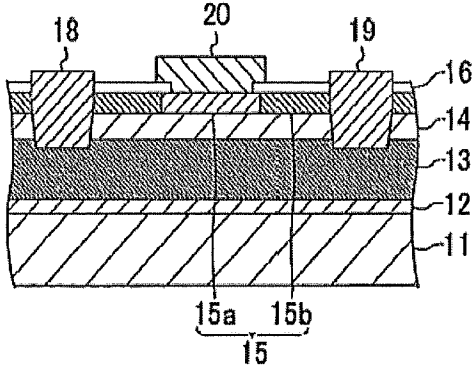
	<u>the Mg receptor to lose activity, resulting in that the material becomes an insulating or weak p-type in a growth state”.</u> “The presence of NH₃ in the reactor cooling process produces hydrogen and leads to passivation. Therefore, <u>it is believed that it is impractical to remove all hydrogen sources and passivation during reactor cooling is unavoidable.”</u>
1-7 a gate contact above the compensated GaN layer.	[Explanations] <u>Feature 1-7 has been disclosed in D1:</u> The gate contact 32 disclosed in D1 is equivalent to the gate contact in claim 1. [Contents specifically disclosed in the reference document] <u>[See FIG. 2A of reference document 1, and the superscript, Page 18, Paragraph 2 of the description]</u>  Figure 2A “FIGS. 2A and 2B illustrate an electron mobility transistor having cap layers 34, 34’ according to some other embodiments of the present invention. As previously discussed with reference to FIGS. 1A and 1B, a substrate 10, a channel layer 20, a barrier layer 22, an ohmic contact portion 30, and a <u>gate contact portion 32</u> may be provided. As shown in FIGS. 2A and 2B, the overlay layers 34, 34’ include a doped region 40 at or near its outer surface. The overlay layers 34, 34’ may be a GaN based cap layer (such as GaN and/or GaAlN, etc.), for example, as discussed in the patents and patent applications incorporated herein by reference. In some embodiments of the present invention, the doped region 40 is doped with a p-type dopant (e.g., Mg, Be, Zn, Ca, and/or C, etc.)

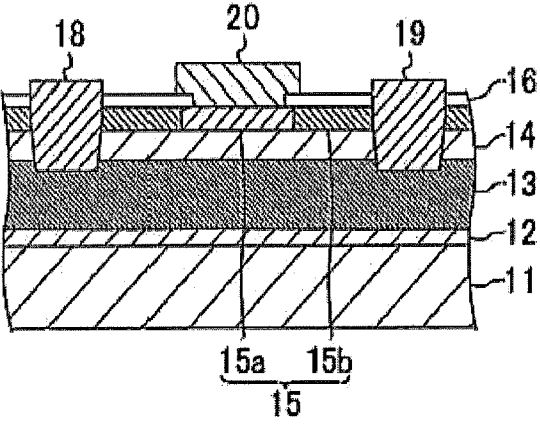
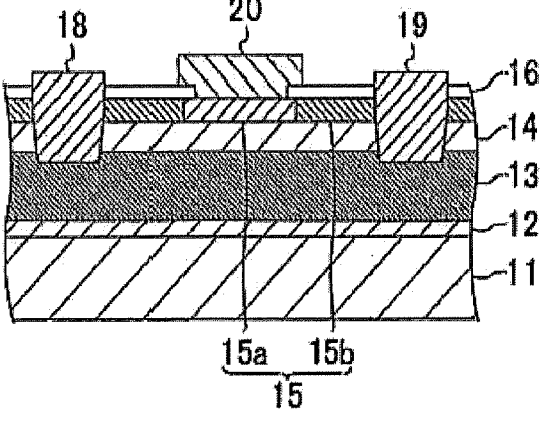
Therefore, D1 has disclosed all the technical features of claim 1, and the two fall within the same technical field, can solve the same technical problem, and can also achieve the same technical effect. Therefore, the claimed technical solution of claim 1, with respect to D1, lacks novelty as specified in Article 22.2 of the Patent Law.

1.2 Claim 1 lacks novelty with respect to D2.

The correlation between the features of claim 1 of the present patent and the disclosure of D2 (US2008087915A1) is as shown in the following table. It should be noted that the following table is only an exemplary example, and the technical content disclosed in D2 is not limited to the text

and images listed in the table below.

1-1 A Group III Nitride transistor comprising:	[Description] <u>Feature 1-1 is disclosed in reference document 2:</u> Reference document 2 discloses a group III nitride transistor. <u>[Contents specifically disclosed in the reference document]</u> <u>[See Paragraph 0003 of the translation of reference document 2]</u> “The present invention relates to a nitride semiconductor transistor and a fabrication method thereof. In particular, the present invention relates to a normally-closed nitride semiconductor transistor suitable for a power switching device and a fabrication method thereof.” <u>[See Paragraph 0005 of the translation of reference document 2]</u> “In recent years, the application of the field effect transistor (FET) made of a gallium nitride (GaN)-based material in high-frequency and high-power devices has been widely studied”.
1-2 a substrate,	[Description] <u>Feature 1-2 is disclosed in reference document 2:</u> The substrate 11 disclosed in D2 is equivalent to the substrate in claim 1. <u>[Contents specifically disclosed in the reference document]</u> <u>[See FIG. 1 of reference document 2, and Paragraph 0031 of the translation]</u> FIG. 1  “As shown in FIG. 1, the substrate 11 is made of silicon, and its main plane is a (111) plane. An AlN buffer layer 12 with a thickness of 100 nm is formed on the main plane of the substrate”.
1-3 a set of III-N transition layers above the substrate,	[Description] <u>Feature 1-3 is disclosed in reference document 2:</u> The buffer layer 12 of AlN disclosed in D2 is equivalent to the transition layer in claim 1. According to the disclosure of the description (see paragraph [0025]

	of the present patent), the transition layer of the present patent may comprise AlN. [Contents specifically disclosed in the reference document] [See FIG. 1 of reference document 2, and Paragraph 0031 of the translation] FIG. 1  “As shown in FIG.1, the <u>substrate 11</u> is made of silicon, and its main plane is a (111) plane. An <u>AlN buffer layer 12</u> with a thickness of 100 nm is formed on the main plane of the substrate”
1-4 a III-N buffer layer above the set of transition layers,	[Description] Feature 1-4 is disclosed in reference document 2: The first nitride semiconductor layer 13 of undoped GaN on the buffer layer 12 disclosed in D2 is equivalent to the III-N buffer layer in claim 1. [Contents specifically disclosed in the reference document] [See FIG. 1 of reference document 2, and Paragraph 0032 of the translation] FIG. 1  “An un-doped GaN <u>first nitride semiconductor layer 13</u> having a thickness

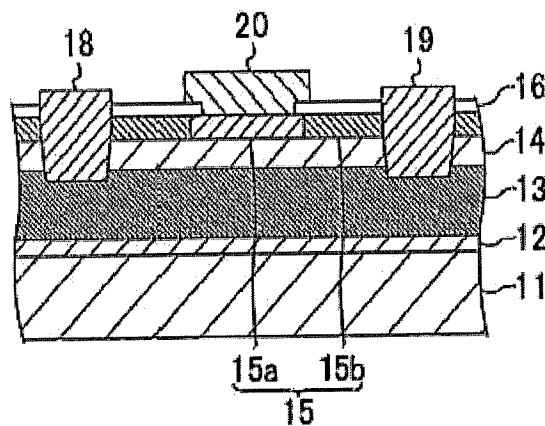
	of 2 μm and an un-doped $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ second nitride semiconductor layer 14 having a thickness of 25 nm are formed on the buffer layer 12. A channel region of the transistor to be described later is formed in an interface region between the first nitride semiconductor layer 13 and the second nitride semiconductor layer 14”.
1-5 a III-N barrier layer above the buffer layer,	[Description] <u>Feature 1-5 is disclosed in reference document 2:</u> The second nitride semiconductor layer 14 of undoped $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ on the first nitride semiconductor layer 13 disclosed in D2 corresponds to the III-N barrier layer in claim 1. [Contents specifically disclosed in the reference document] <u>[See FIG. 1 of reference document 2, and Paragraph 0032 of the translation]</u> FIG. 1 “An un-doped GaN first nitride semiconductor layer 13 having a thickness of 2 μm and an un-doped $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ second nitride semiconductor layer 14 having a thickness of 25 nm are formed on the buffer layer 12. A channel region of the transistor to be described later is formed in an interface region between the first nitride semiconductor layer 13 and the second nitride semiconductor layer 14”.
1-6 a compensated GaN layer above the barrier layer, and	[Description] <u>Feature 1-6 is disclosed in reference document 2:</u> The third nitride semiconductor layer 15 formed on the second nitride semiconductor layer 14 disclosed in D2 is equivalent to the compensated GaN layer in claim 1. A third nitride semiconductor 15 includes a high resistance region 15b, in which Mg is not activated (in hydrogen passivation) so that the resistance is higher than that of a region 15a in which Mg is activated. Although partial hydrogen passivation in 15a is eliminated by activation, hydrogen passivation cannot be completely eliminated (Section 1.1, Point 2, Part 1 of this request). Alternatively, as recorded in Paragraph 0039, after activation in 15a, the

concentration of Mg is set to about $1 \times 10^{19} \text{ cm}^{-3}$, while the concentration of the carrier is set to about $1 \times 10^{18} \text{ cm}^{-3}$, the doping efficiency is 10%, and there is obviously a large amount of hydrogen passivation. Therefore, assuming that the degree of hydrogen passivation in a compensated GaN is not specifically defined according to the claiming of the patentee in the U.S. Lawsuit, then 15a is also a compensated GaN layer.

[Contents specifically disclosed in the reference document]

[See FIG. 1 of reference document 2, and Paragraph 0033 of the translation]

FIG. 1



“On the second nitride semiconductor layer 14, a **third nitride semiconductor layer 15** with a thickness of 200 nm made of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ doped magnesium (Mg) is formed. The Mg-doped third nitride semiconductor layer includes: a control region 15a, in which Mg is activated to embody the P-type conduction property; and a high resistance region 15b in which Mg is not activated to provide a higher resistance than that of the control region 15a. The control region 15a is formed into, for example, bands each having a width of $1 \mu\text{m}$ ”.

[See Paragraph 0039 of the translation of reference document 2]

The concentration of Mg doped into the third nitride semiconductor layer 15 is set to about $1 \times 10^{19} \text{ cm}^{-3}$, and the concentration of the carrier in the control region 15a is set to about $1 \times 10^{18} \text{ cm}^{-3}$ ”.

[See Paragraph 0046 of the translation of reference document 2]

“A method for fabricating the transistor of the first embodiment will be described below. First, the AlN buffer layer 12, the un-doped GaN first nitride semiconductor layer 13, and the un-doped $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ second nitride semiconductor layer 14 are sequentially grown on the substrate 11 by a process of metal-organic chemical vapor deposition (MOCVD). Subsequently, the $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ third nitride semiconductor layer 15 doped with Mg as the P-type impurity is grown. Next, an AlN hydrogen diffusion barrier layer 16 is formed”.

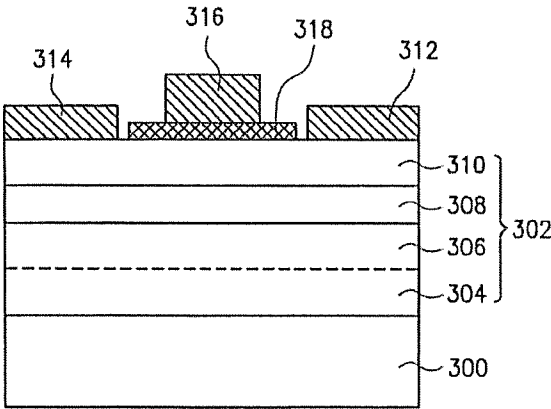
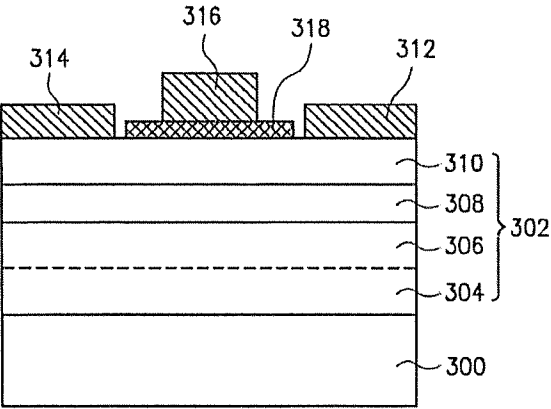
	[See Paragraph 0049 of the translation of reference document 2] “For example, when Mg is doped as the P-type impurity in the crystal growth process of the nitride semiconductor layer by using the MOCVD process, Mg is introduced into the nitride semiconductor. However, <u>Mg introduced into the nitride semiconductor binds with hydrogen atoms therein to lose activity.</u> When heat treatment is performed in an inert gas atmosphere at 800°C for about 20 to 60 min, the hydrogen atoms are desorbed from Mg. Then, Mg is activated, and therefore, the nitride semiconductor exhibits the P-type conduction property”.
1-7 a gate contact above the compensated GaN layer.	[Description] <u>Feature 1-7 is disclosed in reference document 2:</u> The gate electrode 20 disclosed in D2 is equivalent to the gate contact in claim 1. [Contents specifically disclosed in the reference document] <u>[See FIG. 1 of reference document 2, and Paragraph 0034 of the translation]</u> FIG. 1 “On the hydrogen diffusion barrier layer 16, a <u>gate 20</u> is formed to overlay the opening. The gate 20 is made of palladium (Pd) and is in ohmic contact with the control region 15a.

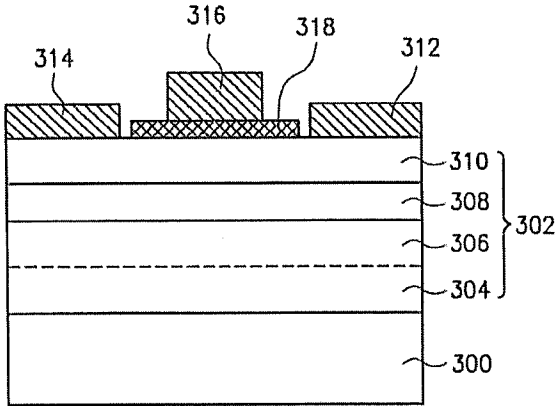
Therefore, reference document 2 discloses all technical features of claim 1, both falling within the same technical field, solving the same technical problem and achieving the same technical effect. Therefore, the technical solution claimed in claim 1 does not possess the novelty as defined in Article 22.2 of the Patent Law with respect to the reference document 2.

1.3 Claim 1 lacks novelty with respect to D3.

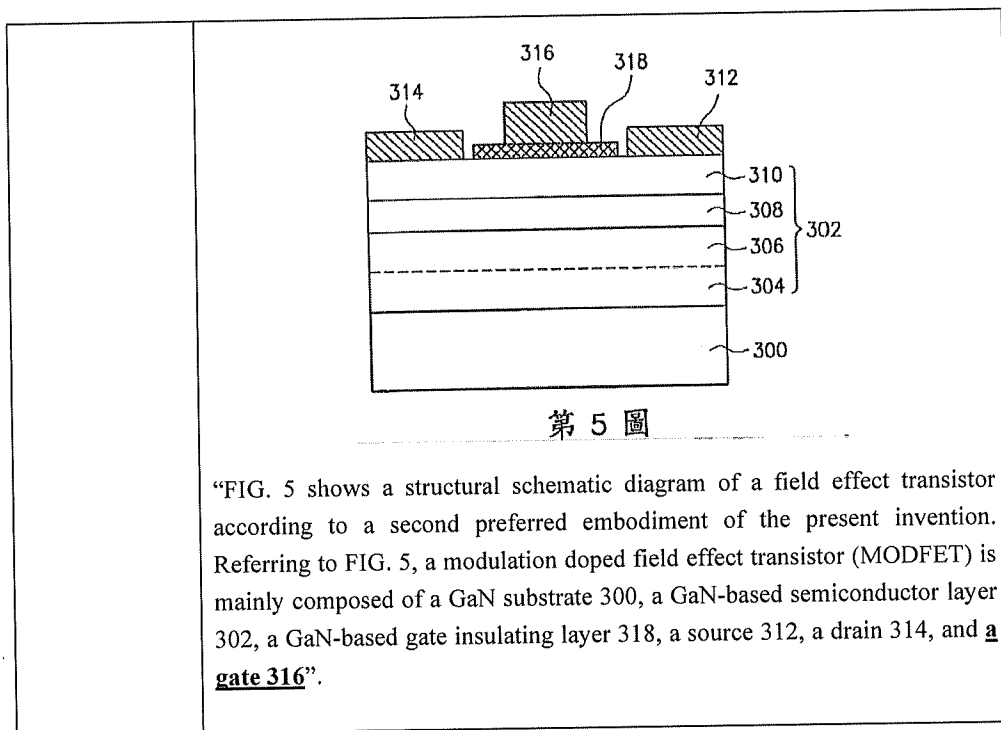
The correlation between the features of claim 1 of the present patent and the disclosure of D3 (TW200414540A) is as shown in the following table. It should be noted that the following table is only an exemplary example, and the technical content disclosed in D3 is not limited to the text and images listed in the table below.

1-1 A Group III Nitride transistor comprising:	[Description] Feature 1-1 is disclosed in reference document 3: D3 discloses a Group III Nitride transistor. Reference document 3 discloses: [Contents specifically disclosed in the reference document] <u>[See the subscript, Page 5, Paragraph 1 of the description of reference document 3]</u> “The present invention is related to a field effect transistor (FET) structure, and in particular to <u>a field effect transistor structure with a GaN-based gate insulating layer</u>”.
1-2 a substrate,	[Description] Feature 1-2 is disclosed in reference document 3: The substrate 300 disclosed in D3 is equivalent to the substrate in claim 1. [Contents specifically disclosed in the reference document] <u>[See FIG. 5 of reference document 3, and the subscript, Page 12, penultimate Paragraph 2 of the description]</u> FIG. 5 “FIG. 5 shows a structural schematic diagram of a field effect transistor according to a second preferred embodiment of the present invention. Referring to FIG. 5, a modulation doped field effect transistor (MODFET) is mainly composed of a GaN substrate 300, a GaN-based semiconductor layer 302, a GaN-based gate insulating layer 318, a source 312, a drain 314, and a gate 316”.
1-3 a set of III-N transition layers above the substrate,	[Description] Feature 1-3 is disclosed in reference document 3: Reference document 3 discloses the buffer layer 304, and when the layer b = 0, the buffer layer 304 is AlGaIn, which is equivalent to the transition layer in claim 1. As recorded in the description (See Paragraph 0025 of this patent), the

	transition layer of this patent may include AlGa_N. [Contents specifically disclosed in the reference document] <u>[See FIG. 5 of reference document 3, and the subscript, Page 12, the last paragraph to Page 13, Paragraph 1 of the description]</u>  FIG. 5 Still referring to FIG. 5, in the architecture of the modulation doped field effect transistor, the GaN-based layer 302 is composed of, for example, a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310. The buffer layer 304 and the channel layer 306 are, for example, an un-doped Al_aIn_bN_bGal_{a-b}N layer, and $a \geq 0, b \geq 0, 1 \geq a + b, x > a;$
1-4 a III-N buffer layer above the set of transition layers,	[Description] <u>Feature 1-4 is disclosed in reference document 3:</u> The channel layer 306 disclosed in D3 is equivalent to the III-N buffer layer in claim 1. [Contents specifically disclosed in the reference document] <u>[See FIG. 5 of reference document 3, and the subscript, Page 12, the last paragraph to Page 13, Paragraph 1 of the description]</u>  FIG. 5

		“Still referring to FIG. 5, in the architecture of the modulation doped field effect transistor, the GaN-based layer 302 is composed of, for example, a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310. The buffer layer 304 and the channel layer 306 are, for example, an un-doped Al_aIn_bGa_{1-a-b}N layer, and $a \geq 0$, $b \geq 0$, $1 \geq a + b$, $x > a$,”
1-5	a III-N barrier layer above the buffer layer,	[Description] <u>Feature 1-5 is disclosed in reference document 3:</u> The gap layer 308 and the barrier layer 310 disclosed in D3 correspond to the III-N barrier layer in claim 1. [Contents specifically disclosed in the reference document] <u>[See FIG.5 of reference document 3, and the subscript, Page 12, the last paragraph to Page 13, Paragraph 1 of the description]</u>  “Still referring to FIG. 5, in the architecture of the modulation doped field effect transistor, the GaN-based layer 302 is composed of, for example, a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310. The buffer layer 304 and the channel layer 306 are, for example, an un-doped Al_aIn_bGa_{1-a-b}N layer, and $a \geq 0$, $b \geq 0$, $1 \geq a + b$, $x > a$,” the gap layer 308 is, for example, an un-doped Al_xIn_yGa_{1-x-y}N layer, and $x \geq 0$, $y \geq 0$, and $1 \geq x + y$; and the barrier layer 310 is, for example, a silicon-doped Al_xIn_yGa_{1-x-y}N layer, and $x \geq 0$, $y \geq 0$, and $1 \geq x + y$”.
1-6	a compensated GaN layer above the barrier layer, and	[Explanations] <u>Feature 1-6 has been disclosed in D3:</u> D3 discloses disposing a GaN-based gate insulating layer 318 doped with Mg on a barrier layer 310, which is equivalent to the compensated GaN layer in claim 1. The high-resistivity p-GaN layer doped with Mg obviously uses the compensation or passivation effect of hydrogen on Mg, that is, D3 implicitly discloses a p-GaN having the insulating or semi-insulating property due to hydrogen passivation, i.e., the compensated GaN layer in the preferred embodiment of the present patent.

	[The specific content disclosed in D3] <u>[See FIG. 5, and page 12, the last paragraph to page 13, paragraph 2 in Description of D3]</u> 第 5 圖 “Still referring to FIG. 5, in the architecture of the modulation doped field effect transistor, the GaN-based layer 302 is composed of, for example, a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310. The buffer layer 304 and the channel layer 306 are, for example, an un-doped Al_aIn_bGa_{1-a-b}N layer, and $a \geq 0$, $b \geq 0$, $1 \geq a + b$, $x > a$,” the gap layer 308 is, for example, an un-doped Al_xIn_yGa_{1-x-y}N layer, and $x \geq 0$, $y \geq 0$, and $1 \geq x + y$; and the barrier layer 310 is, for example, a silicon-doped Al_xIn_yGa_{1-x-y}N layer, and $x \geq 0$, $y \geq 0$, and $1 \geq x + y$. Similarly to the previous embodiment, <u>the GaN-based gate insulating layer 318</u> in the present embodiment <u>may also has a dopant</u> to increase the resistance of the GaN-based gate insulating layer 318 (between about 10⁹ and about 10¹² Ω/□), the dopant is C, a metal such as <u>Mg</u> and Fe, or a combination of them, and these dopants (C and a metal such as Fe and Mg) are doped during, for example, an epitaxy process”.
1-7 a gate contact above the compensated GaN layer.	[Explanations] <u>Feature 1-7 has been disclosed in D3:</u> The gate electrode 316 disclosed in D3 is equivalent to the gate contact in claim 1. [The specific content disclosed in D3] <u>[See FIG. 5 and page 12, the penultimate paragraph in Description of D3]</u>



Therefore, D3 has disclosed all the technical features of claim 1, and the two fall within the same technical field, can solve the same technical problem, and can also achieve the same technical effect. Therefore, the claimed technical solution of claim 1, with respect to D1, lacks novelty as specified in Article 22.2 of the Patent Law.

2. Claims 2-3 lack novelty as specified in Article 22.2 of the Patent Law.

Claim 2 refers to claim 1, and the additional technical feature thereof is “the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen”.

Claim 3 refer to claim 2, and the additional technical feature thereof is “the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca”.

2.1 The additional technical features of claims 2-3 are disclosed in D1.

D1 discloses the following technical features (see page 18, paragraph 2 in Description of D1): “in some embodiments of the present invention, the doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C.”

D1, using attachment 9 (see column 1, paragraph 3) incorporated therein by reference, discloses the following contents: “during growth of GaN p-n junction diodes using Metal-Organic Chemical Vapor Deposition (MOCVD), it is difficult to grow a p-type material with good structural, optical, and electrical integrity. The p-type region of a GaN junction diode is commonly grown in a MOCVD reactor by adding magnesium (Mg) to achieve the desired conductivity. However, a common problem is electrical passivation of acceptors like Mg, zinc (Zn), carbon (C) and others

by hydrogen atoms. The smaller hydrogen atoms diffuse into the GaN material, where they neutralize the Mg acceptors and the holes produced by the Mg. The passivation process leaves the Mg acceptors inactive, resulting in the material becoming insulating or weakly p-type in its as grown state".

As can be seen, when the GaN layer is doped with an acceptor such as Mg, Be, Zn and Ca, there must be hydrogen passivation of the acceptor by hydrogen.

D1 provides different embodiments, for example, the technical solution with a passivation layer and the technical solution without a passivation layer, where the purpose of the passivation layer (e.g., a hydrogen absorption layer) as an alternative solution of the annealing process is to reduce the hydrogen passivation of Mg as the acceptor. Obviously, with regard to no passivation layer being provided and no annealing operation being performed on the p-GaN cap layer, actually disclosed is the solution "acceptor type dopant atoms such as Mg passivated with hydrogen".

In addition, assuming that the degree of hydrogen passivation in a compensated GaN is not specifically defined according to the claiming of the patentee in the U.S. Lawsuit, then even if the passivation layer is provided or an annealing operation is performed on the p-GaN cap layer, there is still residual hydrogen passivation, which is equivalent to disclosing the solution "acceptor type dopant atoms such as Mg passivated with hydrogen".

2.2 The additional technical features of claims 2-3 are disclosed in D2.

D2 discloses (see paragraph [0049] of the translation of D2): when Mg is introduced into the nitride semiconductor, Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom (i.e., the acceptor type dopant atoms passivated with hydrogen). "When, for example, Mg is doped as a p-type impurity during crystal growth for the nitride semiconductor layer by a MOCVD method, Mg is introduced into the nitride semiconductor. However, Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom".

2.3 The additional technical features of claim 2-3 are disclosed in D3.

D3 discloses (see page 13, paragraph 2 in Description of D3): when Mg is introduced into the nitride semiconductor, Mg introduced into the nitride semiconductor has an insulating or semi-insulating high-resistivity characteristic, and for those skilled in the art, the high-resistivity characteristic is from hydrogen passivation. "Similarly to the previous embodiment, the GaN-based gate insulating layer 318 in the present embodiment may also has a dopant to increase the resistance of the GaN-based gate insulating layer 318 (between about $10^9 \Omega/\square$ and about $10^{12} \Omega/\square$), the dopant is C, a metal such as Mg and Fe, or a combination of them, and these dopants (C and a metal such as Fe and Mg) are doped during, for example, an epitaxy process".

In summary, the additional technical features of dependent claims 2-3 have been disclosed in D1-D3, and when claim 1 they refer to lacks novelty with respect to D1-D3, dependent claims 2-3 also lack novelty as specified in Article 22.2 of the Patent Law with respect to D1.

V. Claims 1-3 lack inventive step as specified in Article 22.3 of the Patent Law.

1. Independent claim 1 lacks inventive step as specified in Article 22.3 of the Patent Law.

1.1 D1 is taken as the closest prior art

1.1.1 Claim 1 lacks inventive step with respect to D1 and a combination of D1 and common general knowledge.

According to section 1.1 in Chapter IV, D1 has disclosed all the technical features of claim 1, and claim 1 lacks novelty with respect to D1. When claim 1 lacks novelty with respect to D1, claim 1 also lacks inventive step with respect to D1. Assuming that the patentee claims there are subtle differences between claim 1 and D1, the differences are common general knowledge in the art.

1.1.2 Claim 1 lacks inventive step with respect to a combination of D1 and D2/D3, or further a combination of D1, D2/D3 and common knowledge.

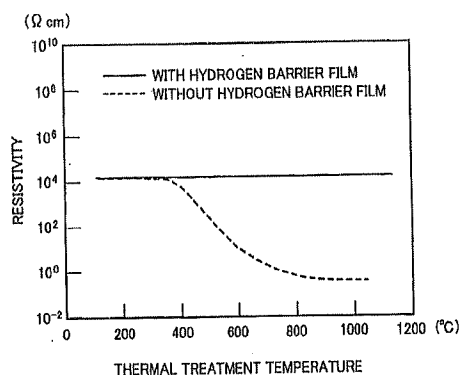
It is assumed that the patentee claims D1 does not disclose provide a compensated GaN layer between a barrier layer and a gate contact, that is, it is assumed that features 1.6-1.7 are distinguishing technical features. The described distinguishing technical feature are disclosed in D2/D3, or can be obtained by combining the motivation of D2/D3 with common general knowledge.

1.1.2.1 D2 discloses the distinguishing technical features, or a combination of D2 and common general knowledge discloses the distinguishing technical features.

The distinguishing technical features are disclosed in D2 (see the comments in section 1.2 of Chapter IV).

In addition, D2 further discloses the setting of different temperatures of thermal treatment (also referred to as activation and annealing) leads to different resistivity (see paragraph [0050] of the translation of D2): "FIG. 4 shows the correlation between the temperature of the thermal treatment and the resistivity in the case where an $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ layer doped with Mg to have a concentration of about $1 \times 10^{19} \text{ cm}^{-3}$ is subjected to a thermal treatment. The thermal treatment was performed in a nitrogen atmosphere for 20 minutes. As shown in FIG. 4, in the case of forming no hydrogen diffusion barrier film of AlN, the resistivity of the Mg doped $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ layer decreases with an increasing temperature of the thermal treatment, and becomes almost constant at around 800 degrees centigrade".

FIG. 4



When Mg is doped as a p-type impurity during crystal growth for the nitride semiconductor by a conventional preparation procedure (e.g., MOCVD), Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom, and thus presents a high-resistivity state first (an insulator or semi-insulator). Then, those skilled in the art can adjust subsequent annealing/activation/heating parameters according to needs, or perform no annealing/activation/heating, so as to obtain a nitride semiconductor of an expected resistivity. As can be seen, Mg introduced into the nitride semiconductor is passivated by hydrogen, and it is well known to those skilled in the art before the date of priority that reducing or reserving a hydrogen passivation can enable the nitride semiconductor to present different resistivity, which is not a contribution of the present patent to the prior art.

1.1.2.2 D3 discloses the distinguishing technical features, or a combination of D3 and common general knowledge discloses the distinguishing technical features.

The distinguishing technical features are disclosed in D3 (see the comments in section 1.3 of Chapter IV).

Alternatively, D3 discloses that when Mg is doped as a p-type impurity during crystal growth (an epitaxy preparation process) for the nitride semiconductor, the doping results in that the nitride semiconductor presents a high-resistivity state (an insulator or semi-insulator). Therefore, when those skilled in the art hope to dispose an insulator or semi-insulator between a gate electrode and a barrier layer (a semiconductor) (i.e., forming an MISFET), under the motivation of D3, it is totally possible to dope Mg as a p-type impurity during crystal growth (an epitaxy preparation process) of a nitride semiconductor layer to obtain a high-resistivity nitride semiconductor, and those skilled in the art know the reason for the high resistivity at this time is the passivation of Mg by hydrogen.

1.2 D2 is taken as the closest prior art.

1.2.1 Claim 1 lacks inventive step with respect to D2 and a combination of D2 and common general knowledge.

According to section 1.2 of Chapter IV herein, D2 has disclosed all the technical features of claim 1, and thus claim 1 lacks novelty with respect to D2. When claim 1 lacks novelty with respect to D2, claim 1 also lacks inventive step with respect to D2. Assuming that the patentee argues there are subtle differences between claim 1 and D2, the differences are common general knowledge in the art.

1.2.2 Claim 1 lacks inventive step with respect to a combination of D2 and D1/D3, or further a combination of D2, D1/D3 and common general knowledge.

It is assumed that the patentee claims D2 does not disclose provide a compensated GaN layer between a barrier layer and a gate contact, that is, it is assumed that features 1.6-1.7 are distinguishing technical features. The described distinguishing technical features are disclosed in D1/D3, or can be obtained by combing the motivation of D1/D3 with common general knowledge.

1.2.2.1 D1 discloses the distinguishing technical features, or a combination of D1 and common general knowledge discloses the distinguishing technical features.

The distinguishing technical features are disclosed in D1 (see the comments in section 1.1 of Chapter IV).

D1 discloses that, when Mg is doped as a p-type impurity during crystal growth for the nitride semiconductor by a conventional preparation procedure (e.g., MOCVD), hydrogen passivation is inevitable. D1 discloses that those skilled in the art can reduce the degree of passivation of Mg by hydrogen by means of providing a passivation layer or by means of an annealing process. However, D1 actually also discloses the solution without annealing and the passivation layer. According to the solution disclosed in D1, those skilled in the art can clearly know the reason for high resistivity when Mg is doped as a p-type impurity during crystal growth for the nitride semiconductor, and a different method for obtaining expected resistivity.

1.2.2.2 D3 discloses the distinguishing technical features, or a combination of D3 and common general knowledge discloses the distinguishing technical features (see the contents in section 1.1.2.2 of this Chapter).

1.3 D3 is taken as the closest prior art.

1.3.1 Claim 1 lacks inventive step with respect to D3 and a combination of D3 and common general knowledge.

According to section 1.3 of Chapter IV, D3 has disclosed all the technical features of claim 1, and thus claim 1 lacks novelty with respect to D3. When claim 3 lacks novelty with respect to D1, claim 1 also lacks inventive step with respect to D3. Assuming that the patentee argues there are subtle differences between claim 1 and D3, the differences are common general knowledge in the art.

1.3.2 Claim 1 lacks inventive step with respect to a combination of D2 and D1/D3, or further a combination of D2, D1/D3 and common general knowledge.

It is assumed that the patentee claims D3 does not disclose provide a compensated GaN layer between a barrier layer and a gate contact, that is, it is assumed that features 1.6-1.7 are distinguishing technical features. The described distinguishing technical features are disclosed in D1/D2, or can be obtained by combining the motivation of D1/D2 with common general knowledge.

1.3.2.1 D1 discloses the distinguishing technical features, or a combination of D1 and common general knowledge discloses the distinguishing technical features (see section 1.2.2.1 of this Chapter for details).

1.3.2.2 D3 discloses the distinguishing technical features, or a combination of D2 and common general knowledge discloses the distinguishing technical features (see the contents in section 1.1.2.1 of this Chapter).

2. Claims 2-3 lack inventive step as specified in Article 22.3 of the Patent Law.

The additional technical features of claims 2-3 are disclosed in D1/D2/D3 (see section 2 of Chapter IV). Therefore, when the claim they refer to lacks inventive step, claims 2-3 also lack inventive step as specified in Article 22.3 of the patent Law.