

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01381
U.S. Patent No. 8,350,294

**PATENT OWNER'S SUR-REPLY TO PETITIONER'S REPLY TO
PATENT OWNER'S PRELIMINARY RESPONSE**

I. PATENT OWNER DOES NOT CONSTRUE “ABOVE” TO REQUIRE DIRECT CONTACT AND ALIGNMENT

Petitioner insists that Patent Owner narrowly construes the term “above” to require that the claimed “gate contact” be centered and in direct contact with the claimed “compensated GaN layer.” That is inaccurate. Rather, Patent Owner argued that *Uemoto* does not disclose “a gate contact above the compensated GaN layer,” as recited in claim 1 of the ’294 patent, because the alleged compensated GaN layer (p-doped high resistive region 15b) is not a part of the gate structure and does not function, together with the gate contact, to control the on/off state of the transistor. Preliminary Response at 9, 30-33. That argument is not tantamount to requiring direct contact and centering.

The intrinsic evidence makes it clear that in order to meet the claimed “gate contact above the compensated GaN layer,” the alleged compensated GaN layer must be part of the gate structure and serve the purpose of turning the transistor on and off. For example, claim 1 describes a “transistor” where the “compensated GaN layer” is formed “above the barrier layer” and “a gate contact” is formed “above the compensated GaN layer.” A POSA would understand that a “compensated GaN layer” between the barrier and the gate contact is part of the gate structure.

The entirety of the specification is directed to GaN gate material. The specification details the problems with prior art GaN transistors having

unfavorable **gate** leakage (*see* '294 patent at 1:55-2:6) and identifies a solution to that problem by creating a compensated **gate** “with low **gate** leakage.” *Id.* at 2:13-14 (emphasis added). Indeed, the Summary of Invention explains that the claimed inventions are directed to using a material “below the gate contact and above the barrier layer” to “reduce[]” “gate leakage.” *Id.* at 2:14-16; *see also id.* at 3:18-21 (“using a compensated semiconductor layer **38** leads to low **gate** leakage during device operation”), as well as “reduce[d] [] **gate** capacitance of the device” (emphasis added). A POSA would understand that it is the gate material under the gate contact that contributes to reducing gate leakage and capacitance. Thus, a POSA would also understand that in order for an alleged “gate contact” to be considered above an alleged “compensated GaN layer,” the alleged “compensated GaN layer” must be part of the gate structure.

Moreover, the specification explains that “the high doping level of compensated layer 38 leads to enhancement mode devices.” ‘294 patent at 3:16-17. An enhancement mode device is one where the 2DEG region is depleted below the gate at zero applied gate bias. *Id.* at 1:47-53. Accordingly, the 2DEG region below a gate which includes a compensated GaN layer (such as compensated layer 38) is depleted at zero applied gate bias.

Conversely, a positive bias applied at the gate enables the enhancement mode device to conduct current. ‘294 patent at 1:53-54. That is, the positive bias

applied at the gate turns the transistor on. Thus, a POSA reading the claim in light of the specification, would understand that the compensated GaN layer, by virtue of causing the 2DEG region to be depleted at zero applied gate bias and enabling the device to conduct current when a positive bias is applied, functions with the gate contact to control the on/off state of the transistor.

II. UEMOTO DOES NOT DISCLOSE THE CLAIMED “GATE CONTACT ABOVE THE COMPENSATED GAN LAYER”

In order for *Uemoto*’s gate electrode 20 and high resistive region 15b to correctly correspond to the claimed “gate contact” and “compensated GaN layer,” respectively, high resistive region 15b would need to function with gate electrode 20 to control the on/off state of *Uemoto*’s transistor. It does not.

Uemoto discloses that there is always a 2DEG under high resistive region 15b (“In the region other than the control region, as shown in FIG. 2B, at the heterointerface the conduction band is located at a lower level than the Fermi level, and thus 2DEG is created.”) *Uemoto* at [0038]. As such, high resistive region 15b has nothing to do with turning the transistor on and off. Rather, it is control region 15a, in conjunction with gate electrode 20, that turns the transistor on and off.

For example, *Uemoto* discloses that the activated p-type impurity in layer 15 (e.g., control region 15a) lifts up the energy levels of semiconductor layers 13 and 14 so that “when non bias voltage is applied to the control region, 2DEG is not created at the heterointerface.” *Uemoto* at [0038]. This results in the transistor

turning off. *See id.* On the other hand, when a positive voltage is applied to control region 15a, the transistor is turned on. *See Uemoto* at [0040].

While control region 15a is part of the gate structure and functions with gate electrode 20 to control the on/off state of the transistor, it is decidedly not a “compensated GaN layer.” Nor is it alleged to be by Petitioner. Unlike a “compensated GaN layer,” control region 15a has activated p-type impurities. Accordingly, control region 15a is a conductive p-type material. In that sense, control region 15a operates like p-type layer 105 shown in the admitted prior art of the ‘294 patent, described by the ‘294 patent as “a conductive p-type material.” ‘294 patent at 43-49.

Perhaps because high resistive region 15b is not part of the gate structure and does not function to turn the transistor on and off, Petitioner, in a parallel invalidation request relating to the Chinese counterpart of the ‘294 patent proceeding, relied upon control region 15a, not high resistive region 15b, as purportedly teaching the “compensated GaN layer.” *See Ex. 2006* at 23-25. Indeed, as shown below in a snapshot of a portion of Petitioner’s claim chart in its China invalidation request, Petitioner relies on the ohmic contact of gate electrode 20 with control region 15a to provide an alleged teaching of “a gate contact above the compensated GaN layer.” *Ex. 2006* at 25.

III. CONCLUSION

For the foregoing reasons and those submitted in Patent Owner's Preliminary Response, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing
PATENT OWNER'S SUR-REPLY TO PETITIONER'S REPLY TO
PATENT OWNER'S PRELIMINARY RESPONSE is being served on counsel
of record by filing this document through the Patent Review Processing System,
with a copy served via electronic mail to the following email address, as authorized
in the Petition:

Innoscence-EPC-IPRs@finnegan.com

Dated: January 23, 2024

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