

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Innoscence (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc. (collectively “Petitioner”) filed a Petition requesting *inter partes* review of claims 1–12 of U.S. Patent No. 8,350,294 B2 (Ex. 1001, “the ’294 patent”). Paper 1 (“Pet.”). Efficient Power Conversion Corporation (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 7 (“Prelim. Resp.”). With authorization, Petitioner subsequently filed a Preliminary Reply (Paper 8, “Prelim. Reply”) and Patent Owner filed a Preliminary Sur-reply (Paper 10, “Prelim. Sur-reply”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail on at least one of the challenged claims of the ’294 patent. Accordingly, we institute an *inter partes* review as to all of the challenged claims of the ’294 patent on all of the grounds of unpatentability set forth in the Petition.

II. BACKGROUND

A. Related Matters

The parties indicate that the ’294 patent is at issue in the following proceedings: (1) *Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd.*, 2:23-cv-04026-AB-AS (C.D. Cal., filed May 24, 2023), and (2) *Certain Semiconductor Devices, and Methods of*

Manufacturing Same and Products Containing the Same, 337-TA-1366
(USITC, filed May 26, 2023). Pet. 90; Paper 5, 2.

B. Real Parties-in-Interest

Petitioner identifies itself (the two parties identified in the caption) and Innoscience (Suzhou) Technology Company, Ltd. as the real parties-in-interest. Pet. 90. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1–2.

C. The '294 patent

The '294 patent is titled “Compensated Gate MISFET and Method for Fabricating the Same” and issued January 8, 2013. Ex. 1001, codes (45), (54). The '294 patent is directed to “field enhancement mode gallium nitride (GaN) transistors” and, in particular, to “an enhancement mode GaN transistor with a compensated GaN layer or semi-insulating GaN layer below the gate contact and above the barrier layer.” *Id.* at 1:14–18.

Figure 1 of the '294 patent is reproduced below.

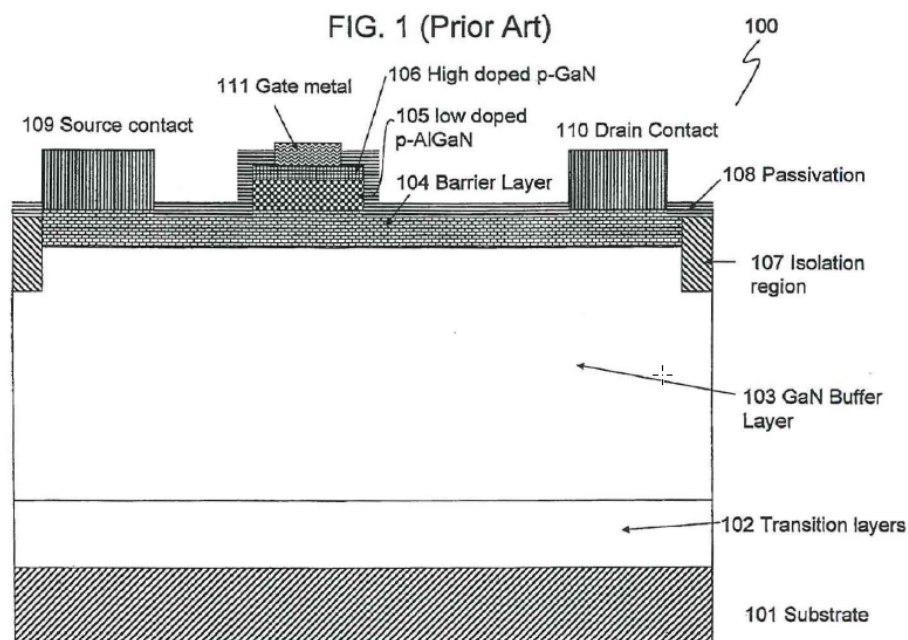


Figure 1 is a cross-section of conventional enhancement mode GaN transistor device 100. *Id.* at 1:55–56, 2:23. As shown in Figure 1, transistor device 100 includes substrate 101, transition layers 102, buffer material 103, barrier material 104, p-type AlGaN layer 105, heavily doped p-type GaN layer 106, isolation region 107, passivation region 108, ohmic contact metals 109 and 110 (source and drain, respectively), and gate metal 111 that resides over the p-type GaN gate. *Id.* at 1:56–2:2. The '294 patent reports that this conventional GaN transistor has several disadvantages, including “very high” “leakage current of the gate contact” due to gate charge injection. *Id.* at 2:3–6.

Figure 2 of the '294 patent is reproduced below.

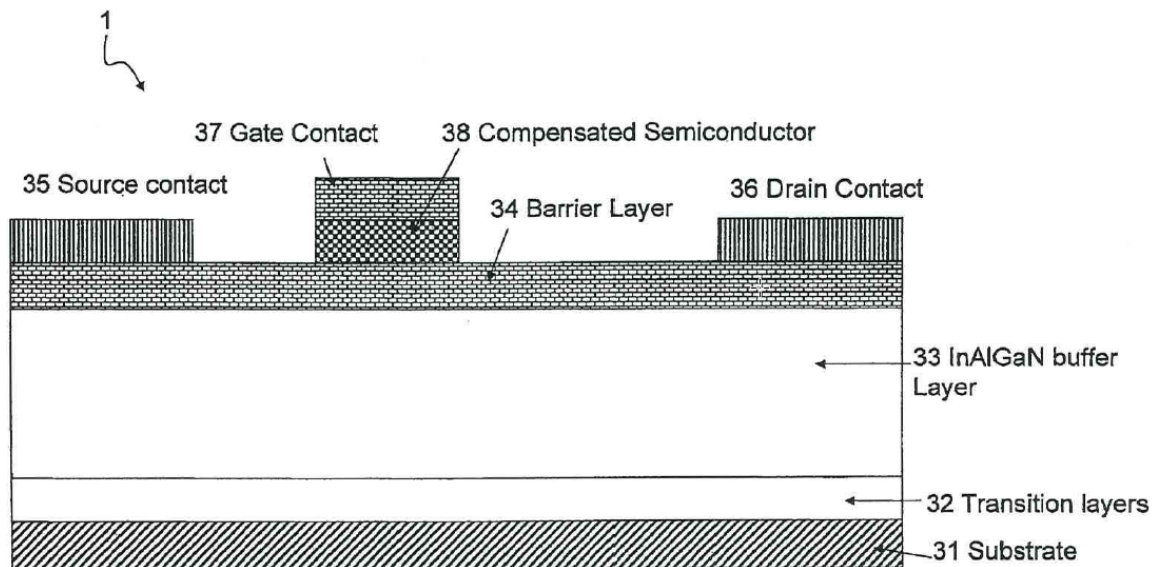


Figure 2 shows a MISFET in the form of GaN transistor 1. *Id.* at 2:24–25, 2:56–57. Transistor 1 is formed on substrate 31, which may be silicon, silicon carbide, or sapphire. *Id.* at 2:57–59. “Over and in contact with the substrate 31 are transition layers 32.” *Id.* at 2:59–60. Buffer layer 33 separates transition layers 32 from barrier layer 34 and is preferably formed of InAlGaN. *Id.* at 2:62–64. Source contact 35 and drain contact 36 are

disposed over barrier layer 34. *Id.* at 3:1–2. Gate contact 37 is provided between the source and drain contacts. *Id.* at 3:4–7. Compensated semiconductor layer 38 is formed over barrier layer 34 and under gate contact 37 and preferably comprises “AlGaN or GaN with a deep level passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca.” *Id.* at 3:7–12.

The ’294 patent explains that “the high doping level of compensated layer 38 leads to enhancement mode devices,” which are devices that “are normally off” and require “a positive bias applied at the gate in order to conduct current.” *Id.* at 1:47–54, 3:16–17. Use of a compensated semiconductor layer 38 also “leads to low gate leakage during device operation” and “reduced gate capacitance of the device.” *Id.* at 3:17–21. The ’294 patent further explains that

The critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen. The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material. Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art.

Id. at 3:43–52.

D. Illustrative Claims

Claims 1, 4, 7, and 10 are independent. Claims 1 and 4 are representative of the challenged claims and are reproduced below.

1. [1p] A column III Nitride transistor comprising:
[1a] a substrate,
[1b] a set of III-N transition layers above the substrate,
[1c] a III-N buffer layer above the set of transition layers,

- [1d] a III-N barrier layer above the buffer layer,
- [1e] a compensated GaN layer above the barrier layer, and
- [1f] a gate contact above the compensated GaN layer.

Ex. 1001, 5:12–18 (identifiers have been added to align with Petitioner’s arguments (Pet. at Claim Appendix)).

- 4. [4p] A column III Nitride transistor comprising:
 - [4a] a substrate,
 - [4b] a set of III-N transition layers above the substrate,
 - [4c] a III-N buffer layer above the set of transition layers,
 - [4d] a III-N barrier layer, and
 - [4e] a semi-insulating III-N layer above the barrier layer.

Id. at 5:24–29 (identifiers have been added to align with Petitioner’s arguments (Pet. at Claim Appendix)).

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 11):¹

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–12	103(a)	Smith ²
1–12	103(a)	Smith, Kigami ³
1–12	103(a)	Smith, Uemoto ⁴
1–12	103(a)	Uemoto, Smith

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. The ’294 patent issued January 8, 2013. Ex. 1001, code (45). Thus, we apply the pre-AIA version of §103.

² US Patent Publ. 2007/0164315, published July 19, 2007. Ex. 1005 (“Smith”).

³ JP Publ. JP2006-253224A, published September 21, 2006. Ex. 1008 (“Kigami”) (certified translation). The original Japanese language version of Kigami is provided at Exhibit 1007.

⁴ US Patent Publ. 2008/0087915 A1, published April 17, 2008. Ex. 1006 (“Uemoto”).

III. ANALYSIS

A. Legal Standard

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In order to determine whether an invention would have been obvious at the time the application was filed, we consider the level of ordinary skill in the pertinent art. *Graham*, 383 U.S. at 17. In assessing the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation omitted).

Petitioner contends a person of ordinary skill in the art “would have possessed at least a four-year degree in electrical engineering, chemical engineering, physics, or material science, or a closely related field, and at least two years of experience in semiconductor device design or fabrication,

including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies.” Pet. 5–6.

Patent Owner does not address the knowledge or education of a person of ordinary skill in the art.

On this record, we adopt Petitioner’s unopposed definition of the person of ordinary skill in the art as it appears consistent with the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (holding that the prior art itself can reflect the appropriate level of ordinary skill in the art).

C. Claim Construction

In an *inter partes* review proceeding, a patent claim is construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (as amended Oct. 11, 2018). This rule adopts the same claim construction standard used by Article III federal courts, which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. Under this standard, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *See Phillips*, 415 F.3d at 1312–13.

Petitioner contends the terms “compensated GaN layer” and “above” require construction. Pet. 12–17; Prelim. Reply 1–5. Patent Owner contends only the term “compensated GaN layer” requires construction. Prelim. Resp. 5–15; Prelim. Sur-reply 1–3.

Upon review of the parties’ arguments and evidence, we determine that only the term “compensated GaN layer” requires construction. *See*

Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”)).

Compensated GaN Layer

Claim 1 recites “A column III Nitride transistor comprising: . . . a compensated GaN layer above the barrier layer, and a gate contact above the compensated GaN layer.” Ex. 1001, 5:12–18. Petitioner contends a “compensated GaN layer” is a “doped GaN layer formed with a step to passivate its impurities which is a ‘product-by-process’ limitation.” Pet. 12–13. Given this construction, Petitioner contends “the prior art only need show a material with passivated impurities to show unpatentability, not the step to achieve it.” *Id.* at 16.

Petitioner notes that Patent Owner previously argued before the ITC that this term is properly construed to mean “[a] semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor),” but contends that it was known in the art that hydrogen is naturally present in GaN and will passivate p-type dopants. *Id.* at 13–15 (citing Ex. 1019 (ITC Proposed Constructions⁵) 1, 9). Petitioner also contends that during prosecution, Patent Owner argued a “compensated GaN layer” requires a step of

⁵ Petitioner cites to “*ITC Constructions*, 1, 9.” Pet. 13. It appears that Petitioner is referring to Ex. 1019, which includes both Complainant’s and Respondents’ proposed constructions before the ITC. Pet. xi.

“forming” the compensated layer, “not merely presence of hydrogen in as-grown layers.” *Id.* at 14–15 (citing Ex. 1002 (Prosecution History), 106).

Petitioner also contends that Patent Owner’s proposed construction includes the terms “imperfection,” “partially cancels,” and “electrical effects” that are not used in the claims and introduce ambiguities. Pet. 16. For example, Petitioner contends that in a real crystal there will always be imperfections, so Patent Owner’s construction would cover any GaN material, an interpretation Petitioner contends conflicts with the prosecution history of the ’294 patent. *Id.* at 16–17 (citing Ex. 1003 ¶¶ 78–81; Ex. 1024 (Excerpts of Ph.D. Dissertation, Matias) § 3.1).

Patent Owner contends the IEEE dictionary defines “compensated semiconductor” as “[a] semiconductor in which one type of impurity or imperfection (for example, donor) partially cancels the electric effects of the other type of impurity or imperfection (for example, acceptor).” Prelim. Resp. 9 (quoting Ex. 2004). Patent Owner further contends the term “compensated GaN layer” is not a product-by-process limitation, but rather “refers to a GaN layer having certain structural and electrical characteristics.” *Id.* at 13. Patent Owner further contends that a “compensated GaN layer” is a “compensated GaN gate material,” i.e., the compensated GaN layer is part of the gate structure and functions, “together with the gate contact, to control the on/off state of the transistor.” Prelim. Sur-reply 1; Prelim. Resp. 11.

With respect to the question of whether the term “compensated GaN layer” is a product-by-process limitation, we note that Petitioner contends the challenged claims would have been obvious regardless of whether “compensated GaN layer” is construed to be a product-by-process limitation or not. *See* Pet. 23–27 (asserting that the challenged claims would have been

obvious under either Petitioner's or Patent Owner's constructions), 39–42, 73 (“*Uemoto*, thus, teaches region 15b is ‘a compensated GaN layer’ under both parties’ proposed constructions.”). As Petitioner has provided sufficient evidence and argument to map the asserted art to the “compensated GaN layer” regardless of whether the term is construed to be a product-by-process limitation, it is not necessary to address this issue at this time.

With respect to the question of whether a compensated layer may be provided by any “dopant, impurity, or imperfection,” both parties appear to agree that a GaN layer in which hydrogen partially cancels the effect of a dopant will create a compensated GaN material. Pet. 39, 41–42; Prelim. Resp. 19–20. And, because Petitioner relies only upon the presence or addition of hydrogen in GaN materials in its grounds, we need not determine what other processes or structures could create a “compensated GaN” layer.

In addressing the question of whether a “compensated GaN layer” requires a “compensated GaN gate material,” we look to the intrinsic record to determine the correct meaning of the claim term. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

Claims

Claim terms are generally given their ordinary and customary meaning, which is the “meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Phillips*, 415 F.3d at 1313. Patent Owner does not present evidence that the ordinary meaning in the art of a “GaN layer” is “GaN gate material.” Indeed, the prior art of record discloses multiple GaN layers that do not appear to be “gate material.” Ex. 1006 ¶ 32; Ex. 1005 ¶ 74 (“the channel layer 20 is GaN”); Ex. 1008 ¶¶ 24–25 (noting that the buffer layer and semiconductor

layer are GaN). Nor does Patent Owner contend that the term “compensated” requires or implies a particular orientation or location with respect to the gate contact. Thus, by itself, the term “compensated GaN layer” does not require a “compensated GaN gate material.”

Rather, Patent Owner contends that given the placement of the “compensated GaN layer” above the barrier layer and below the gate contact, one of ordinary skill in the art would have understood that the claimed “compensated GaN layer” is a “compensated GaN gate material.” Prelim. Resp. 7. We are not persuaded by this argument, at this stage of the proceeding, because the prior art (Uemoto) discloses a compensated GaN layer that is above a barrier layer and below a gate contact, as recited in claim 1, and Patent Owner contends this layer is not a “compensated GaN layer.” Ex. 1006, Fig. 7; Prelim. Resp. 31–32. This tends to suggest that the placement of a “compensated GaN layer” above a barrier layer and below a gate contact, without more, does not necessarily indicate that said layer is part of the gate.

In view of the foregoing, on this record, we determine that the language and structure of claim 1 does not support a construction requiring that the “compensated GaN layer” be a “compensated GaN gate material.”

Written Description

Patent Owner contends the written description supports its construction requiring that the “compensated GaN layer” be a “compensated GaN *gate* material.” Prelim. Resp. 7–9. Patent Owner reasons that the title of the ’294 patent is “Compensated **Gate** MISFET and Method for Fabricating the Same,” “[t]he entirety of the specification is directed to GaN gate material,” and the identified inventive step is using a compensated GaN material in a transistor gate to improve gate leakage. Prelim. Resp. 7.

There are two exceptions to the general rule that we apply the ordinary and customary meaning of a claim term: (1) when a patentee sets out a definition and acts as his own lexicographer, or (2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution. *See Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). The standards for lexicography and disclaimer are “exacting.” *Id.* at 1366.

Here, there is no suggestion that the patentees acted as their own lexicographer to redefine the term “compensated GaN layer.” Thus, on this preliminary record, the lexicography exception does not apply.

A “patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.” *Thorner*, 669 F.3d at 1366 (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002)). As noted by Patent Owner, the title of the ’294 patent is “Compensated Gate MISFET” and much of the discussion of the ’294 is of a compensated GaN layer that is directly below the gate contact and above a barrier layer and operates in conjunction with the gate contact to control the on/off state of the transistor. Prelim. Sur-reply 1. On this record, we are presented with insufficient argument or evidence to conclude that these disclosures rise to the level of a disclaimer. First, although the title of the ’294 patent is directed to a “Compensated Gate MISFET,” claim 1 is more broadly directed to “[a] column III Nitride transistor.” Ex. 1001, 5:12, code (54). Second, we are directed to no disclosure or suggestion in the ’294 patent that the invention is limited to a “compensated GaN layer” that serves a particular function or is part of the gate, or a disclosure that a “compensated

GaN layer” is only useful in a column III Nitride transistor when it is directly below the gate and functions in concert with the gate electrode to control the on/off state of the transistor. *See Thorner*, 669 F.3d at 1366 (“It is likewise not enough that the only embodiments, or all of the embodiments, contain a particular limitation. We do not read limitations from the specification into the claims; we do not redefine words.”).

As also noted by Patent Owner, one of the primary purposes of the compensated GaN layer of the ’294 patent is to reduce gate leakage. Ex. 1001, 2:13–19, 3:18–21 (“using a compensated semiconductor layer 38 leads to low gate leakage during device operation.”). The prior art of record, however, indicates that a compensated GaN layer that is below the gate contact and above a barrier layer, but not part of the gate material, may also “decrease the leakage current between the gate and the drain.” Ex. 1006 ¶¶ 44 (“Even when a positive bias of 5 V or higher is applied to the gate electrode, no significant gate-leakage current is observed.”), 61. As such, evidence of record suggests that a person of ordinary skill in the art would have understood that one of the primary goals disclosed in the ’294 patent is achieved regardless of whether the compensated GaN layer is part of the gate, or simply in close vicinity to the gate.

In view of the foregoing, and on this preliminary record, we determine that the written description of the ’294 patent does not support construing “compensated GaN layer” as a “compensated GaN gate material.”⁶

⁶ The parties may address during trial whether the specification makes clear that the claimed invention is limited to a compensated GaN layer that is part of the gate.

Prosecution History

Neither party asserts that the prosecution history provides helpful guidance on the question of whether a “compensated GaN layer” requires a “compensated GaN gate material.” Pet. 13–17; Prelim. Resp. 6–15; Prelim. Reply 1–5; Prelim. Sur-Reply 1–5.

Conclusion

For the reasons set forth above, and after review of the claims, written description, and prosecution history cited by the parties, we do not construe “compensated GaN layer” to require a “compensated GaN gate material.” And, for the reasons discussed above, we need not address at this time whether a “compensated GaN layer” is a product-by-process limitation or includes materials that are compensated using methods other than hydrogen passivation.

D. Claims 1–12 over Smith

Petitioner contends the subject matter of claims 1–12 would have been obvious over the disclosures of Smith. Pet. 21–27, 34–60.

1. *Smith*

Smith discloses transistors that incorporate nitride-based active layers. Ex. 1005 ¶ 2. Smith explains that silicon (Si) and gallium arsenide (GaAs) have found wide application in low power semiconductor devices, but are not well suited for higher power and/or high frequency applications due to their relatively small bandgaps (e.g., 1.12 eV for Si and 1.42 for GaAs at room temperature) and/or relatively small breakdown voltages. *Id.* ¶ 3. In light of these difficulties, interest in high power, high temperature, and/or high frequency applications has turned to semiconductors with wide bandgaps, such as silicon carbide and Group III nitrides. *Id.* ¶ 4.

One application of these materials is in a High Electron Mobility Transistor (HEMT), which may offer operational advantages due to the formation of a two-dimensional electron gas (2DEG) at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity. *Id.* ¶ 5.

Figure 2A of Smith is reproduced below.

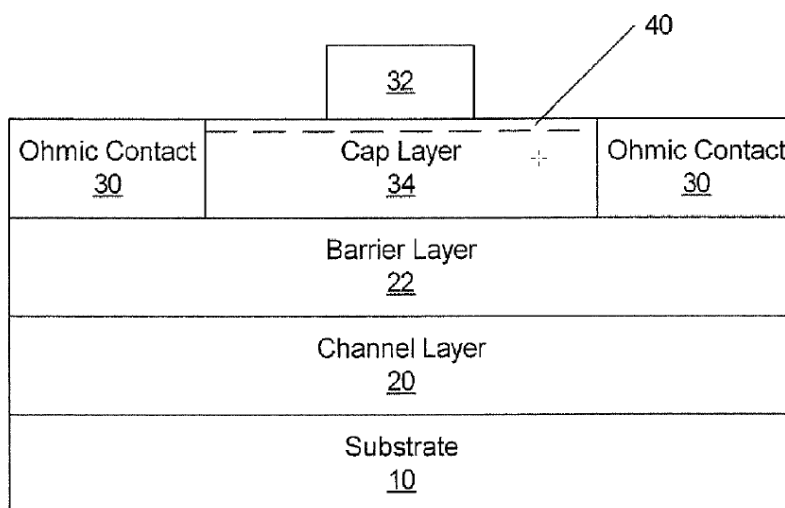


Figure 2A

Figure 2A is a cross-sectional schematic illustrating transistors having a cap layer. *Id.* ¶ 41. In the embodiment schematically depicted in Figure 2A, substrate 10 may be a semi-insulating silicon carbide layer. *Id.* ¶ 69.

“Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate 10.” *Id.* ¶ 70. Channel layer 20 is formed above substrate 10 and barrier layer 22 is formed above channel layer 20. *Id.*

¶¶ 73, 85. Channel layer 20 may be composed of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ where $0 \leq x < 1$ (which allows for GaN when $x=0$). *Id.* ¶ 74. Barrier layer 22 is composed of AlN, AlInN, AlGa_{0.5}In_{0.5}N, or AlInGa_{0.5}N and has a smaller electron affinity and greater bandgap than channel layer 20. *Id.* ¶ 75. Cap layer 34 may be a

GaN layer and includes a doped region 40 at or near its outer surface. *Id.*

¶ 85. Cap layer 34 may be blanket formed on barrier layer 22 and may be epitaxially grown and/or formed by deposition. *Id.* ¶ 77. Doped region 40 may be doped with a p-type dopant, such as Mg, Be, Zn, Ca and/or C. *Id.* ¶¶ 85, 87. The “[p]-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents.” *Id.* ¶ 87. “Gate contact 32 is provided directly on the doped region 40 so as to provide a Junction HEMT (JHEMT).” *Id.* ¶ 88.

2. Analysis—Claim 1

Petitioner contends that under either party’s construction of “compensated GaN layer,” Smith discloses, or renders obvious, the subject matter of claim 1. Pet. 34–39. In particular, Petitioner contends that Smith discloses a column III nitride transistor (limitation [1p]) comprising a substrate 10 (limitation [1a]), a set of transition layers on substrate 10 (not shown in Figure 2A) (limitation [1b]), a buffer layer in the form of channel layer 20 (limitation [1c]), a barrier layer in the form of barrier layer 22 (limitation [1d]), a compensated GaN layer in the form of cap layer 34 (limitation [1e]), and a gate contact 32 (limitation [1f]). *Id.* at 34–44. Petitioner further contends that barrier layer 22 is above channel layer 20, cap layer 34 is above barrier layer 22, and gate contact 32 is above cap layer 34, as recited in claim 1. *Id.*

Petitioner contends that under either parties’ construction, cap layer 34 is a compensated GaN layer because it is doped with p-type dopants that are passivated by hydrogen that is naturally present in the GaN layer. *Id.* at 39–40 (asserting that the product-by-process claims are met

“regardless of the specific compensation process”), 42 (asserting that this claim limitation is met under Patent Owner’s proposed construction requiring that a dopant or impurity (hydrogen) partially cancel the electrical effects of another type of dopant (magnesium)). This position is supported by the testimony of Dr. Shealy, who testifies that “as-grown” GaN materials contain hydrogen that will interact with and inactivate magnesium dopants. Ex. 1003 ¶ 62 (citing Ex. 1011, § 3.3 (“hydrogen is present in relatively high concentrations in as-grown samples, especially in p-type GaN”)); Ex. 1012 § 1.2 (“hydrogen plays a crucial role in passivating [] Mg acceptors, and creates a neutral complex Mg–H that prevents the formation of holes in GaN”); Ex. 1017, § I.1.c)).

Patent Owner contends Petitioner’s ground based on Smith fails because cap layer 34 is not a “compensated GaN layer.” Prelim. Resp. 17–21. Patent Owner acknowledges that Smith discloses that cap layer 34 may be formed by “conventional epitaxial growth techniques,” but contends “there is no indication in *Smith* that the ‘conventional epitaxial growth techniques’ that *Smith* references are carried out in the presence of hydrogen.” *Id.* at 18. The evidence presented by Petitioner, however, suggests that “hydrogen is present in relatively high concentrations in as-grown samples, especially in p-type GaN.” Ex. 1011, 127 (§ 3.3); Ex. 1003 ¶ 62. Moreover, as discussed below, Smith discloses an optional annealing step to remove hydrogen. Ex. 1005 ¶ 83. In combination, this evidence suggests that Smith’s “conventional epitaxial growth techniques” would result in the presence of hydrogen in the GaN layer, and Patent Owner presents no persuasive evidence or argument to suggest otherwise.

To the extent hydrogen is naturally present in cap layer 34 of Smith, Patent Owner contends one of ordinary skill in the art would have used

existing methods to remove this hydrogen from cap layer 34, with Smith explicitly disclosing an annealing step conducted in the presence of oxygen to remove hydrogen from the embodiments depicted in Figures 1A and 1B. Prelim. Resp. 18–19 (citing Ex. 1005 ¶ 83; Ex. 2005, 2:1–3).

As noted by Patent Owner, Smith discloses embodiments in which a passivation layer, such as the MgN passivation layer disclosed in U.S. Patent No. 6,498,111, is provided on the transistors depicted in Figures 1A and 1B of Smith and an optional annealing step is performed in the presence of oxygen to remove hydrogen. Ex. 1005 ¶ 83. Smith’s disclosure that the annealing step to remove hydrogen is optional, however, tends to cut against Patent Owner’s argument that one of ordinary skill in the art would have necessarily sought to remove any hydrogen present in cap layer 34 from the embodiments depicted in Figures 2A and 2B. *Id.*

In view of the foregoing, Petitioner demonstrates sufficiently for purposes of institution that Smith teaches or suggests a “compensated GaN layer” under either parties’ construction of that term. Petitioner also sufficiently demonstrates for purposes of institution that Smith teaches or suggests every other limitation of claim 1. Thus, Petitioner demonstrates a reasonable likelihood that the subject matter of claim 1 would have been obvious over Smith.

3. Analysis: Claims 4, 7, 10

Claims 4, 7, and 10 are independent and differ from independent claim 1, in relevant part, in requiring “a semi-insulating III-N layer above the barrier layer” (claims 4 and 7) or “a semi-insulating III-N layer between the barrier layer and the gate contact” (claim 10). Ex. 1001, 5:24–29, 6:11, 6:22–23. Petitioner contends that Smith discloses that cap layer 34 may

include deep level dopants and may be formed using “[t]echniques for co-doping Group III-nitride materials,” incorporating-by-reference US Patent Publication No. 2005/0145874 A1 (Ex. 1016 ¶ 5 (“Saxler ’874”)). Pet. 46 (citing Ex. 1005 ¶ 85). According to Petitioner, co-doping cap layer 34 of Smith using the method of Saxler ’874 would result in a semi-insulating III-N layer. *Id.* at 46–47, 49, 56–57.

Patent Owner contends that, in the context of paragraph 85 of Smith that incorporates Saxler ’874 by reference, Smith at most teaches co-doping regions of different dopant concentrations, but does not suggest that region 40, if p-doped, should be co-doped with a deep level dopant. Prelim. Resp. 23. Patent Owner further contends that Smith “never states or even remotely implies that the cap layer 34 is ‘semi-insulating,’” and Petitioner provides no other motivation for one of ordinary skill in the art to use the co-doping method of Saxler ’874 in Smith. *Id.* at 22–23. Thus, Patent Owner contends Petitioner has not demonstrated that Smith discloses or renders obvious the “semi-insulating III-N layer” recited in claims 4, 7, and 10. *Id.* at 23.

Referencing the embodiments depicted in Figures 2A and 2B, Smith discloses that cap layer 34 may be doped with a p-type dopant, such as Mg, Be, Zn, Ca and/or C, or doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co. Ex. 1005 ¶ 85. Smith then discloses that in some embodiments cap layer 34 may have a dopant incorporated throughout the cap layer, with doped region 40 having a region of increased dopant concentration over the concentration of the dopant in the remainder of cap layer 34. *Id.* Immediately after this disclosure, Smith states that “[t]echniques for co-doping Group III-nitride materials are described, for example, in [Saxler ’874] . . . entitled ‘CO-DOPING FOR FERMI LEVEL

CONTROL IN SEMI-INSULATING GROUP III NITRIDES,’ the disclosure of which is incorporated herein as if set forth in its entirety.” *Id.*

On this record, Petitioner sufficiently explains for purposes of institution why Smith’s express disclosure of co-doping using the techniques of Saxler ’874 would at least suggest to one of ordinary skill in the art that such techniques were contemplated for use in Smith. The invention disclosed in Saxler ’874 involves forming “semi-insulating Group III nitride semiconductor layers” by doping a Group III nitride layer with a shallow level p-type dopant *and* a deep level dopant. Ex. 1016 ¶¶ 1, 5, code (57). Thus, on this preliminary record, Petitioner sufficiently explains why one of ordinary skill in the art would have understood Smith to teach or suggest using Saxler ’874’s method of co-doping both a shallow level p-type dopant and a deep level dopant in cap layer 34 to result in a semi-insulating III-N layer.

Upon review of the parties’ arguments and supporting evidence, we determine that Petitioner demonstrates sufficiently for purposes of institution that Smith teaches or suggests the subject matter of claims 4, 7, and 10.

4. Analysis: Claims 2–3, 5–6, 8–9, and 11–12

Petitioner contends that Smith discloses the subject matter of claims 2–3, 5–6, 8–9, and 11–12. Pet. 44–45, 48, 52, 57–60.

Patent Owner does not address Petitioner’s arguments with respect to claims 2–3, 5–6, 8–9, and 11–12, apart from its arguments related to independent claims 1, 4, 7, and 10.

Upon review of the parties’ arguments and supporting evidence, we determine that Petitioner demonstrates sufficiently for purposes of institution

that Smith teaches or suggests the subject matter of claims 2–3, 5–6, 8–9, and 11–12.

E. Claims 1–12 over Smith and Kigami

Petitioner contends the subject matter of claims 1–12 would have been obvious over the combined disclosures of Smith and Kigami. Pet. 28–31, 34–60.

1. *Kigami*

Kigami discloses a semiconductor device that contains a p-type impurity wherein the concentration of the activated p-type impurity is locally adjusted to be low. Ex. 1008 ¶ 1. Kigami explains that one technique for forming a switching semiconductor device includes forming a gate electrode that is opposed, through an insulating film, by a semiconductor that contains a p-type impurity. *Id.* ¶ 4. “In this situation, there is a demand to lower the concentration of the p-type impurity contained in the semiconductor,” as the region opposing the gate electrode “becomes easy to invert, and thereby the gate voltage required to turn the switching semiconductor device ON and OFF can be made small.” *Id.* “[O]n the other hand, there is also a demand to raise the concentration of the p-type impurity,” “because, when the concentration of the p-type impurity is lowered, the withstand voltage of the switching semiconductor device decreases.” *Id.*

Kigami explains that “[t]he region in which it is desired to lower the concentration of the p-type impurity . . . is a local region that opposes the gate electrode” and the “region in which it is desired to raise the concentration of the p-type impurity is the entire region of the semiconductor.” *Id.* Kigami notes, however, that “in actuality, it is difficult

to obtain a III-V group compound semiconductor in which the concentration of a p-type impurity is lowered locally.” *Id.* ¶ 5.

Kigami notes that hydrogen atoms will inactivate p-type impurities in III-V group semiconductors. *Id.* ¶ 7. Kigami utilizes this phenomenon to locally lower the concentration of the activated p-type impurity in the region opposing the gate electrode, while retaining sufficient activated p-type impurities in the majority of the III-V group compound semiconductor. *Id.*

Figure 1 of Kigami is reproduced below.

FIG. 1

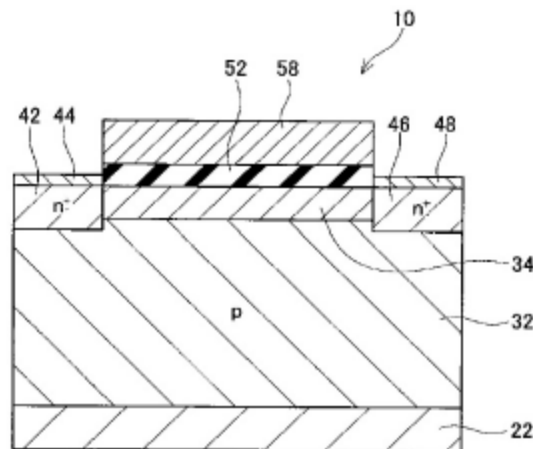


Figure 1 “schematically shows a longitudinal, cross-sectional view of the principal parts” of the semiconductor device. *Id.* ¶ 38. As shown in Figure 1, semiconductor device 10 has a substrate 22, GaN layer 32, gate insulating film 52, gate electrode 58, source region 42, and drain region 46. *Id.* ¶ 20. A magnesium dopant is added to GaN layer 32 and then an ionized hydrogen gas is introduced to the front-surface side of GaN layer 32 to form a local region 34 in which substantially all of the magnesium is inactivated. *Id.* ¶¶ 20, 22, 26. Kigami explains that “semiconductor device 10 has the characteristics of being able to operate at a low threshold voltage, having low loss, and having a high withstand voltage.” *Id.* ¶ 23.

2. *Analysis—Claim 1*

Petitioner contends that one of ordinary skill in the art would have sought to use Kigami's method of passivating impurities to improve the transistor of Smith. Pet. 24–25. In particular, Petitioner contends that one of ordinary skill in the art would have sought to employ Kigami's ionized gas hydrogenation method to passivate impurities in Smith's doped cap layer 34 because Kigami teaches that introducing hydrogen into GaN transistor layers "improves performance" by providing a transistor with "a low threshold voltage" and "high withstand voltage." *Id.* at 28–29 (citing Ex. 1008 ¶ 7). According to Petitioner, this modification would result in a "compensated GaN layer above the barrier layer" under either parties' construction of "compensated GaN layer." *Id.* at 24–25.

We question Petitioner's proposed combination. In the embodiment depicted in Figure 2A of Smith, dopants are added to cap layer 34 to form doped region 40, in which the concentration of dopants is higher than in the rest of cap layer 34. Ex. 1005 ¶¶ 85, 87. This increased concentration of dopants is "used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents." *Id.* ¶ 87. Petitioner's proposed combination would intentionally passivate the very dopants that Smith seeks to add to cap layer 34 to alter its electrical characteristics. We question whether Petitioner adequately explains why one of ordinary skill in the art would have used Kigami's methods to produce a cap layer with the opposite dopant configuration than desired in Smith.

F. Claims 1–12 over Uemoto and Smith

Petitioner contends the subject matter of claims 1–12 would have been obvious over the combined disclosures of Uemoto and Smith. Pet. 61–88.

1. *Uemoto*

Uemoto is titled “Nitride Semiconductor Device and Method for Fabricating the Same” and published April 17, 2008. Ex. 1006, codes (43), (54). The nitride semiconductor device of Uemoto

is characterized in that it includes: a first nitride semiconductor layer; a second nitride semiconductor layer; a third nitride semiconductor; and a gate electrode. The first nitride semiconductor layer is formed over a substrate. The second nitride semiconductor layer is formed on the first nitride semiconductor layer and has a wider band gap than the first nitride semiconductor layer. The third nitride semiconductor layer is formed on the second nitride semiconductor layer and includes a control region with a p-type conductivity and a high resistive region formed around the control region and having a higher resistance than that of the control region. The gate electrode is formed on the control region.

Id. ¶ 13. According to Uemoto, the disclosed semiconductor device “has a large operating current with normally-off operation and excellent switching characteristics.” *Id.* ¶ 11.

Figure 7 of Uemoto is reproduced below.

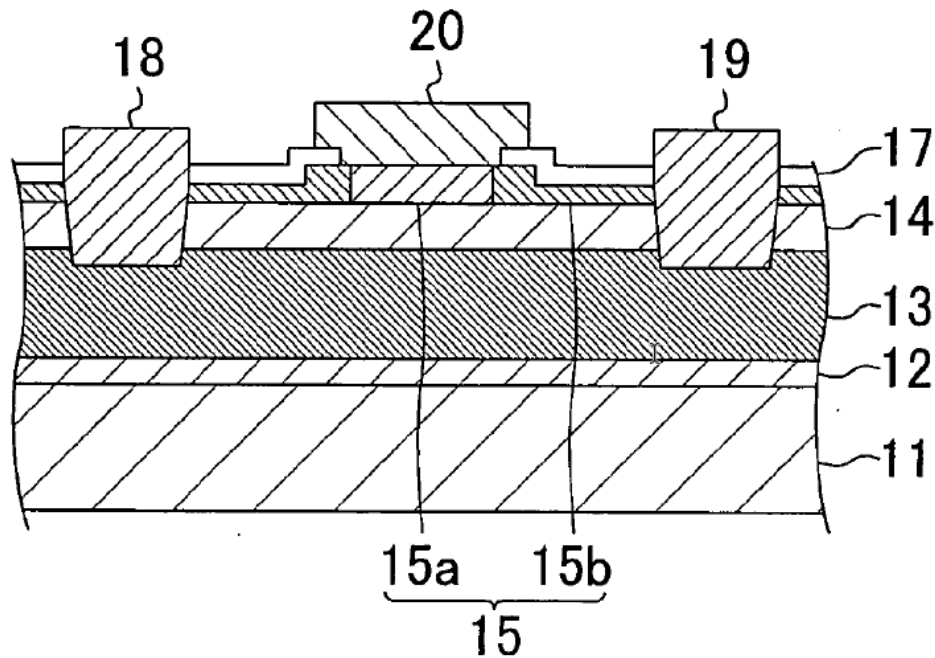


Figure 7 of Uemoto is “a cross sectional view showing a nitride semiconductor transistor according to a third embodiment” of Uemoto. *Id.* ¶ 23. The transistor depicted in Figure 7 is composed of substrate 11, buffer layer 12, first nitride semiconductor layer 13, second nitride layer 14, third nitride layer 15, hydrogen diffusion film 17, source electrode 18, drain electrode 19, and gate electrode 20. *Id.* ¶¶ 31–35, 57, 62–63.

Uemoto explains that the third nitride layer 15 is doped with Mg. *Id.* ¶¶ 33, 46. Hydrogen diffusion film 17 is made of silicon nitride (SiN) and contains at least $1 \times 10^{20}/\text{cm}^3$ hydrogen. *Id.* ¶ 63. During thermal treatment, hydrogen from hydrogen diffusion film 17 selectively inactivates impurities in region 15b, whereas impurities in control region 15a, which is not covered by hydrogen diffusion film 17, are activated to selectively form a region having p-type conductivity. *Id.* According to Uemoto, the high resistance of region 15b reduces the leakage current between the gate and the drain. *Id.* ¶ 59.

2. Analysis—Claim 1

Petitioner contends that Uemoto and Smith teach or suggest every limitation of independent claim 1. Pet. 61–76. In particular, Petitioner contends that Uemoto discloses a “nitride semiconductor transistor[.]” [limitation 1p] that contains a substrate 11 [limitation 1a], a buffer layer 12 [limitation 1b], a first nitride semiconductor layer 13 [limitation 1c], a second nitride semiconductor layer 14 [limitation 1d], a compensated GaN layer 15b [limitation 1e], and a gate electrode 20 [limitation 1f]. *Id.* Although buffer layer 12 is depicted as a single layer, and not as “a set of transition layers,” Petitioner contends that one of ordinary skill in the art would have sought to use a set of transition layers in Uemoto to achieve “strain balancing,” as taught in Smith. *Id.* at 62–64, 69–70. With respect to the requirement that the compensated GaN layer reside under the gate electrode, Petitioner contends that Figure 7 depicts a portion of region 15b under gate electrode 20. *Id.* at 75.

Patent Owner contends it is only region 15a of Uemoto that is above barrier layer 14 and below the gate electrode 20. Prelim. Resp. 31. According to Patent Owner, region 15b “serves absolutely no function in depleting the underlying 2DEG and turning the device on or off. Rather, that function is carried out by gate contact 20 and underlying region 15a, which is conductive, not inactivated.” *Id.* at 31–32. As region 15b is allegedly not part of the gate, Patent Owner contends it is not a “compensated GaN layer.” *Id.* at 34; Prelim. Sur-reply 5 (asserting that “because region 15b is not part of the gate structure and has nothing to do with turning the transistor on and off,” it is “unreasonable to identify region 15b as a ‘compensated GaN layer’”).

We do not construe “compensated GaN layer” to require a layer that is part of the gate, or operates in conjunction with gate electrode 20 to turn the transistor on and off. And, as shown in Figure 7 of Uemoto, a portion of element 15b is above second nitride layer 14 and below gate contact 20. Ex. 1006, Fig. 7. Accordingly, on this record, Petitioner demonstrates sufficiently for purposes of institution that Uemoto discloses a “compensated GaN layer.”

For the reasons set forth above, Petitioner sufficiently identifies for purposes of institution where Uemoto and Smith disclose every limitation of claim 1. Petitioner also provides an explanation, supported by factual underpinning, as to why one of ordinary skill in the art would have used a set of transition layers, as disclosed in Smith, in the transistor of Uemoto. Pet. 62–64. Thus, Petitioner demonstrates a reasonable likelihood that the subject matter of claim 1 would have been obvious over Uemoto and Smith.

3. Analysis: Claims 4, 7 and 10

Independent claims 4, 7, and 10, each require a “semi-insulating III-N layer.” Ex. 1001, 5:24–29, 6:11, 6:22–23. Petitioner contends that Smith discloses co-doping cap layers with a deep level dopant in order to improve transistor characteristics and that one of ordinary skill in the art would have sought to substitute the magnesium doping of Uemoto with the co-doping method of Saxler ’874 and Smith. Pet. 64–66.

Patent Owner disagrees, generally repeating its arguments recited above regarding the scope of Smith’s co-doping disclosure. Prelim. Resp. 35–37.

For the reasons discussed above with respect to the “semi-insulating III-N layer” in Smith, we determine that Patent Owner’s arguments

regarding the scope of Smith's disclosures raise, at most, a material issue of fact that is best resolved on a complete trial record. Thus, on this record, Petitioner sufficiently explains for purposes of institution where Uemoto and Smith teach or suggest the limitations of claims 4, 7, and 10.

4. Analysis: Claims 2–3, 5–6, 8–9, and 11–12

Petitioner contends the subject matter of claims 2–3, 5–6, 8–9, and 11–12 would have been obvious over the combined disclosures of Uemoto and Smith. Pet. 76–77, 79–80, 82, 86–88.

Patent Owner does not directly address Petitioner's arguments with respect to these claims, apart from its arguments discussed above directed to independent claims 1, 4, 7, and 10.

Upon review of the parties' arguments and evidence, we determine that Petitioner identifies sufficiently for purposes of institution where Uemoto and Smith teach or suggest every limitation of claims 2–3, 5–6, 8–9, and 11–12. As such, Petitioner demonstrates a reasonable likelihood that claims 2–3, 5–6, 8–9, and 11–12 would have been obvious over Uemoto and Smith.

G. Claims 1–12 over Smith and Uemoto

Petitioner contends the subject matter of claims 1–12 would have been obvious in view of the combined disclosures of Smith and Uemoto. Pet. 31–33.

As we determine a reasonable likelihood exists that claims 1–12 would have been unpatentable as obvious over the combination of Uemoto and Smith, we do not address the combination of Smith and Uemoto in this Decision. To the extent necessary, however, we will address this combination at trial.

IV. CONCLUSION

For the foregoing reasons, we determine that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We, therefore, institute an *inter partes* review.

V. ORDER

For the foregoing reasons, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review of claims 1–12 of the '294 patent is instituted on all ground of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, notice is given of institution of trial commencing on the entry date of this Decision.

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