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Title:

COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

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COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

FIELD OF THE INVENTION

[0001] The present invention relates to the field of enhancement mode gallium nitride (GaN) transistors. More particularly, the invention relates to an enhancement mode GaN transistor with a compensated GaN layer or a semi-insulating GaN layer below the gate contact and above the barrier layer.

DETAILED DESCRIPTION OF THE INVENTION

[0002] Gallium nitride (GaN) semiconductor devices are increasingly desirable for power semiconductor devices because of their ability to carry large current and support high voltages. Development of these devices has generally been aimed at high power/high frequency applications. Devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFET), high electron mobility transistors (HMET), or modulation doped field effect transistors (MODFET). These types of devices can typically withstand high voltages, e.g., 100 Volts, while operating at high frequencies, e.g., 100 kHz-10 GHz.

[0003] A GaN HEMT device includes a nitride semiconductor with at least two nitride layers. Different materials formed on the semiconductor or on a buffer layer causes the layers to have different band gaps. The different material in the adjacent nitride layers also causes polarization, which contributes to a conductive two dimensional electron gas (2DEG) region near the junction of the two layers, specifically in the layer with the narrower band gap.

[0004] The nitride layers that cause polarization typically include a barrier layer of AlGaN adjacent to a layer of GaN to include the 2DEG, which allows charge to flow through the device. This barrier layer may be doped or undoped. Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted, i.e. removed, below the gate at zero applied gate bias, the device can be an

enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

[0005] FIG. 1 illustrates a conventional GaN transistor device 100. Device 10 includes substrate 11 that can be composed of silicon (Si), silicon carbide (SiC), sapphire, or other material, transition layers 12, typically composed of AlN and AlGaN that is about 0.1 to about 1.0 μm in thickness, buffer layer 13, typically composed of GaN (which can include varying amounts of In and/or Al as well) that is about 0.5 to about 10 μm in thickness, primary channel layer 14 that is the region that conducts current and is typically composed of GaN or indium gallium nitride (InGaN) that is about 0.01 to about 0.1 μm thick, ohmic contact region 15, typically composed of AlGaN, Al and titanium (Ti) that may have Si, that is about 0.01 to about 0.03 μm thick, barrier material 16 typically composed of AlGaN where the Al to Ga ratio is about 0.1 to about 0.5, with thickness from about 0.01 to about 0.03 μm , gate structure 17 typically composed of p-type GaN, with a nickel (Ni) and gold (Au) metal contact, and ohmic contact metals 18 and 19 typically composed of Ti and Al, with a capping metal such as Ni and Au.

[0006] Similarly, FIG. 2 illustrates another conventional GaN transistor device 100. Device 100 includes gate metal 111, heavily doped p-type GaN 106, p-type AlGaN 105, drain ohmic contact metal 109, source ohmic contact metal 110, un-doped AlGaN barrier 104, un-doped GaN 103, buffer layer 102, and silicon substrate 101.

[0007] There are several disadvantages of the conventional GaN transistors shown in FIGS. 1 and 2. One problem is that the leakage current of the gate contact during device conduction is very high due to gate charge injection. In addition, the conductive layer (p-AlGaN layer 105 in FIG. 2) can become inactive during processing and limits the steps and order of device manufacture.

[0008] It therefore would be desirable to provide a MISFET, particularly a GaN transistor, that does not leak current during device conduction and that is easier to manufacture.

SUMMARY OF THE INVENTION

[0009] The present invention is directed to a MISFET, such as a GaN transistor, with low gate leakage. In one embodiment, the gate leakage is reduced with a compensated GaN layer below the gate contact and above the barrier layer. In another embodiment, the gate leakage is reduced by employing a semi-insulating layer below the gate contact and above the barrier layer..

BRIEF DESCRIPTION OF THE DRAWINGS

- [0010]** FIG. 1 is a cross-section of a prior art transistor.
- [0011]** FIG. 2 is a cross-section of a prior art transistor.
- [0012]** FIG. 3 is a transistor according to an embodiment described herein.
- [0013]** FIG. 4 is a cross-sectional view at a stage of processing.
- [0014]** FIG. 5 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 4.
- [0015]** FIG. 6 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 5.
- [0016]** FIG. 7 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 6.
- [0017]** FIG. 8 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 7.
- [0018]** FIG. 9 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 8.
- [0019]** FIG. 10 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 9.
- [0020]** FIG. 11 is a transistor according to an embodiment described herein.

[0021] FIG. 12 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 7.

[0022] FIG. 13 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 12.

[0023] FIG. 14 is a cross-sectional view at a stage of processing subsequent to that shown in FIG. 13.

DETAILED DESCRIPTION OF THE INVENTION

[0024] FIG. 3 shows a MISFET in the form of GaN transistor 1 according to an embodiment of the present invention. GaN transistor 1 is formed on a substrate 31 that may comprise, for example, silicon Si, silicon carbide SiC or sapphire. Over and in contact with the substrate 31 are transition layers 32. Transition layers 32 may comprise, for example, AlN or AlGa_N, with a thickness of between 0.1 to 1.0 μm. A buffer layer 33 separates the transition layers 32 from a barrier layer 34. The buffer layer 33 is preferably formed of InAlGa_N with any concentration of In and Al (including 0% In and/or Al) and has a thickness between 0.5 and 3 μm. The barrier layer 34 is formed of AlGa_N and has a thickness between 0.01 and 0.03 μm and an Al percentage of about 10% to 50%. Source and drain contacts 35, 36 are disposed over the barrier layer. Source and drain contacts are formed of Ti or Al with a capping metal such as Ni and Au or Ti and TiN. A gate contact 37, formed of for example, Ta, Ti, TiN, W, or WSi₂, and having a thickness of between 0.05 and 1.0 μm, is provided between the source and drain contacts. In accordance with the present invention, a compensated semiconductor layer 38 is formed over the barrier layer 24 and under the gate contact 37. Compensated semiconductor layer 38 preferably comprises AlGa_N or Ga_N with a deep level passivated p-type impurity such as, for example, Mg, Zn or Ca.

[0025] Advantageously, the high doping level of compensated layer 38 leads to enhancement mode devices. In addition, using a compensated semiconductor layer 38 leads to low gate leakage during device operation. Finally, the insulating nature of compensated layer 38 reduces the gate capacitance of the device.

[0026] Figures 4-10 describe an example method of manufacturing the GaN transistor 1 shown in FIG. 3. Referring to FIG. 4, the first step is to provide a substrate 31. Referring to FIG. 5, the next step is to nucleate and grow transition layers 32 on top of the substrate 31. Referring to FIG. 6, the next step is to grow a buffer layer 33 over the transistor layer 32. Referring to FIG. 7, the next step is to grow a barrier layer 34 over the buffer layer 33.

[0027] Referring to FIG. 8, the next step is to grow a compensated semiconductor layer 38 over the barrier layer 34. Referring to FIG. 9, the next step is to deposit a gate contact 37 on the compensated semiconductor layer 38. Referring to FIG. 10, the next step is to etch away the compensated semiconductor layer 38, except the portion beneath gate contact 37. An additional hydrogen passivation can be performed by exposing the device to ammonia or hydrogen plasma at a high temperature. The final step is to provide the source and drain ohmic contacts 35, 36 over the barrier layer 34, which results in the finished GaN transistor 1 shown in FIG. 3.

[0028] The critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 2) is the passivation of a p-type impurity using hydrogen. The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in MISFET 100 of the prior art, layer 105 is a conductive p-type material. Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art.

[0029] FIG. 11 shows a GaN transistor 2 according to a second embodiment of the present invention. GaN transistor 2 is similar to GaN transistor 1 (FIG. 3), except that GaN transistor 2 has a semi-insulating layer 39 in place of the compensated semiconductor layer 38 (FIG. 3). Semi-insulating layer 39 may comprise, for example, AlGa_N or Ga_N, with deep level impurity atoms, for example, C, Fe, Mn, V or Ni.

[0030] The second embodiment of the invention has the same advantages as the first embodiment. The high doping of semi-insulating layer 39 leads to enhancement mode devices, the semi-insulating layer 39 leads to low gate leakage during device operation, and the insulating nature of semi-insulating 39 reduces the gate capacitance of the device. In addition, the performance of the

device of the second embodiment is not as sensitive to future processing steps involving hydrogen and/or high temperatures.

[0031] The method of manufacturing GaN transistor 2 is the same as the method of manufacturing GaN transistor 1 for the steps shown in FIGS. 4-7. Referring to FIG. 12, the next step in the production of the second embodiment, after the step shown in FIG. 7, is the growth of semi-insulating layer 39 incorporating impurity atoms.

[0032] Referring to FIG 13, the next step is to deposit a gate contact 37 on the semi-insulating layer 39. Referring to FIG. 14, the next step is to etch away the semi-insulating layer 39, except the portion under gate contact 37. The next step is to provide the source and drain ohmic contacts 35, 36 over the barrier layer 34 which results in the finished device 2 shown in FIG. 11.

[0033] The device of the present invention has the following characteristics that distinguish it over the prior art: (1) the capacitance from gate to channel layer when the device is on is lower than in the prior art; (2) the gate bias can be driven much more positive without significant current through the gate (typically, in the prior art, the gate begins to conduct current between 2.5B to 3.5V, which the present invention can be driven to 6V without dramatic gate leakage occurring; and (3) hole injection from the gate into the channel layer does not occur.

[0034] The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described herein. Modifications and substitutions to specific process conditions can be made. Accordingly, the embodiments of the invention are not considered as being limited by the foregoing description and drawings.

ABSTRACT

A MISFET, such as a GaN transistor, with low gate leakage. In one embodiment, the gate leakage is reduced with a compensated GaN layer below the gate contact and above the barrier layer. In another embodiment, the gate leakage is reduced by employing a semi-insulating layer below the gate contact and above the barrier layer.

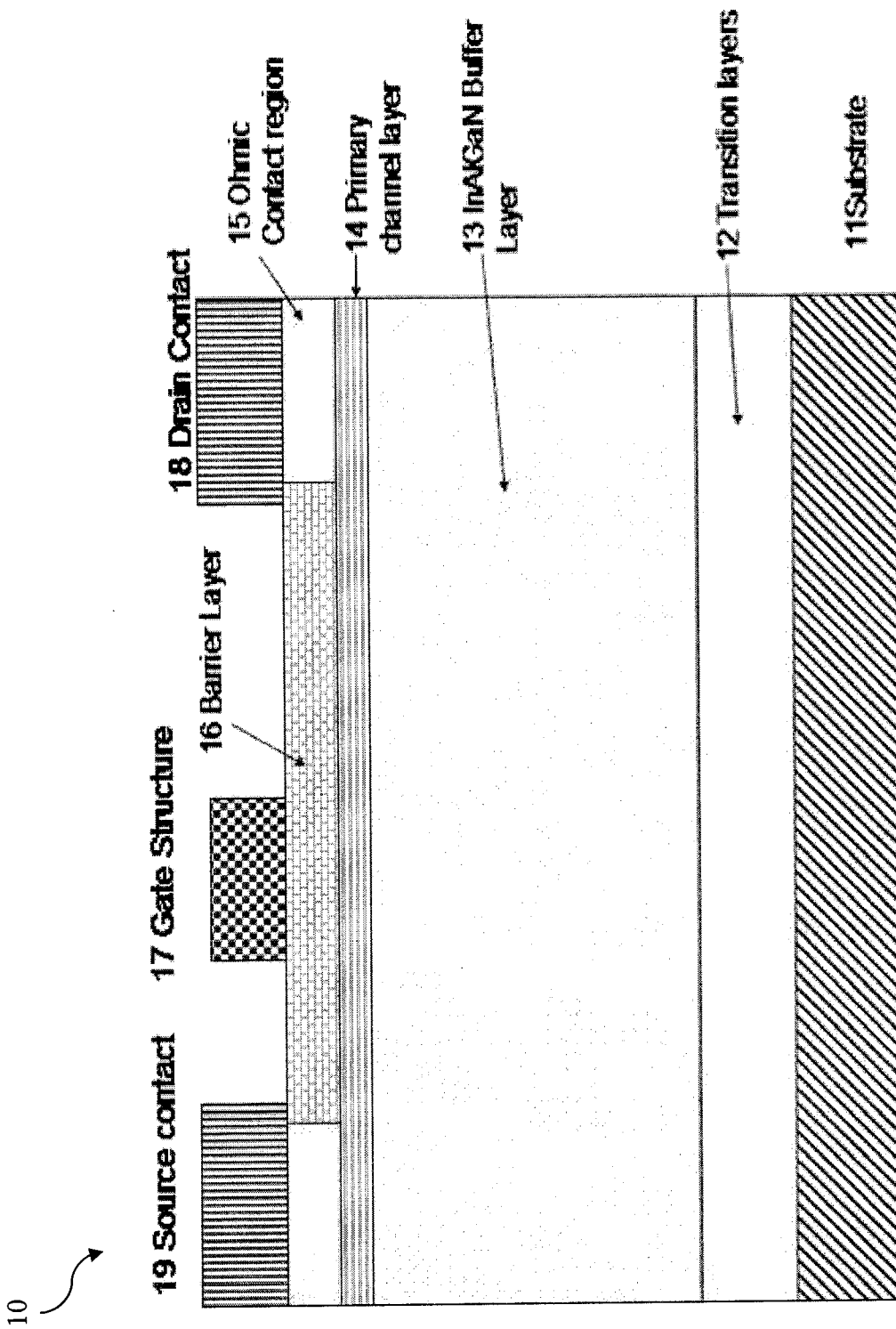


FIG. 1
Prior Art

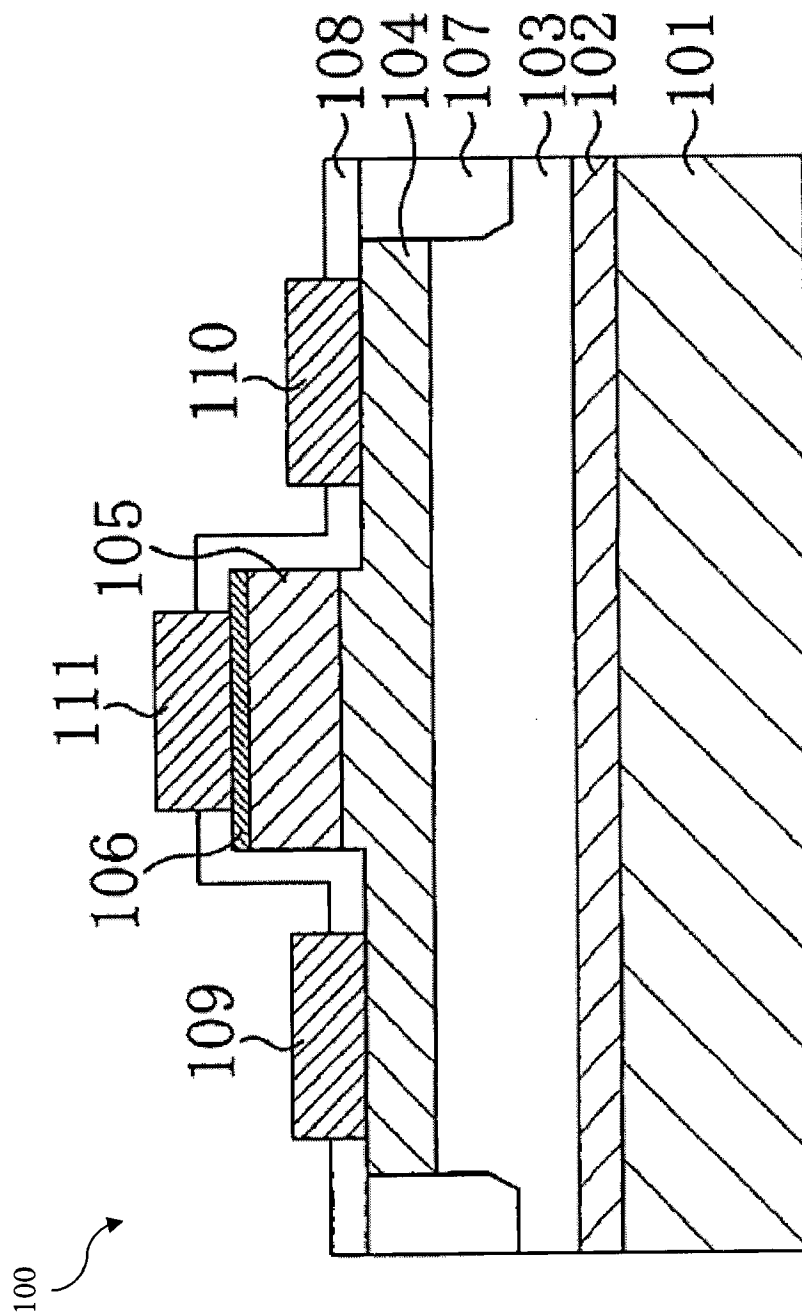


FIG. 2
Prior Art

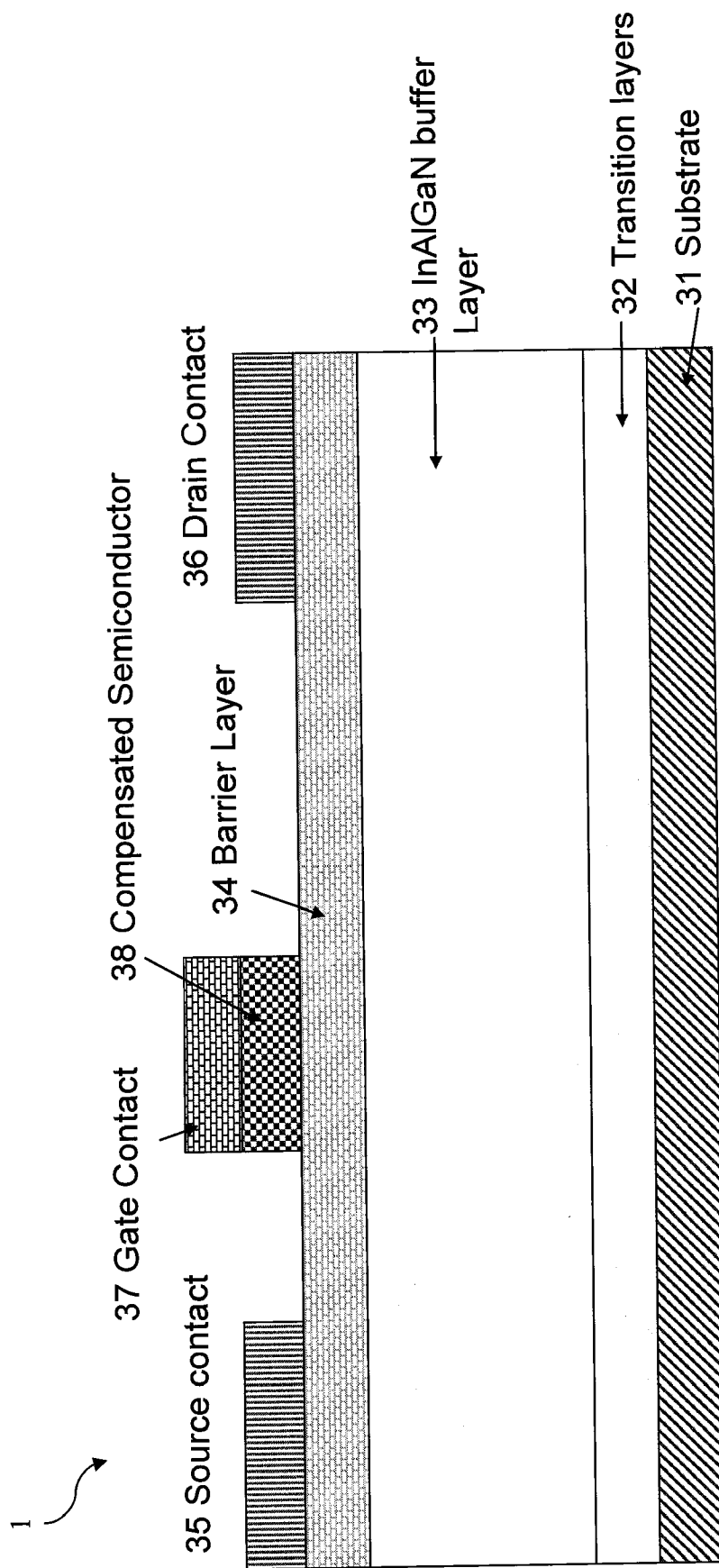


FIG. 3

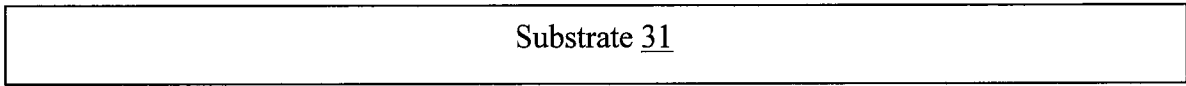


FIG. 4

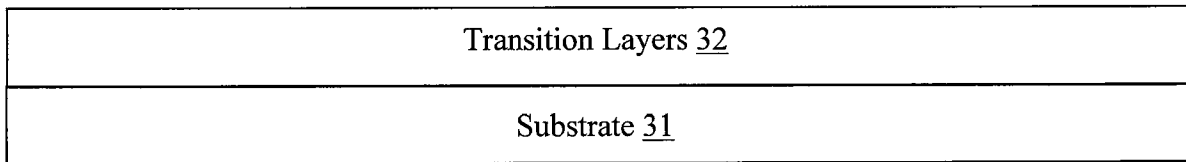


FIG. 5

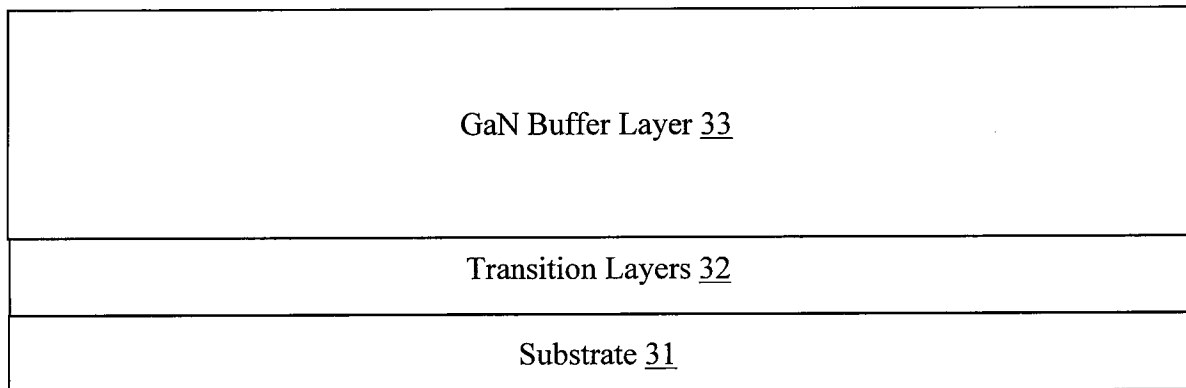


FIG. 6

Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 7

Compensated Semiconductor <u>38</u>
Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 8

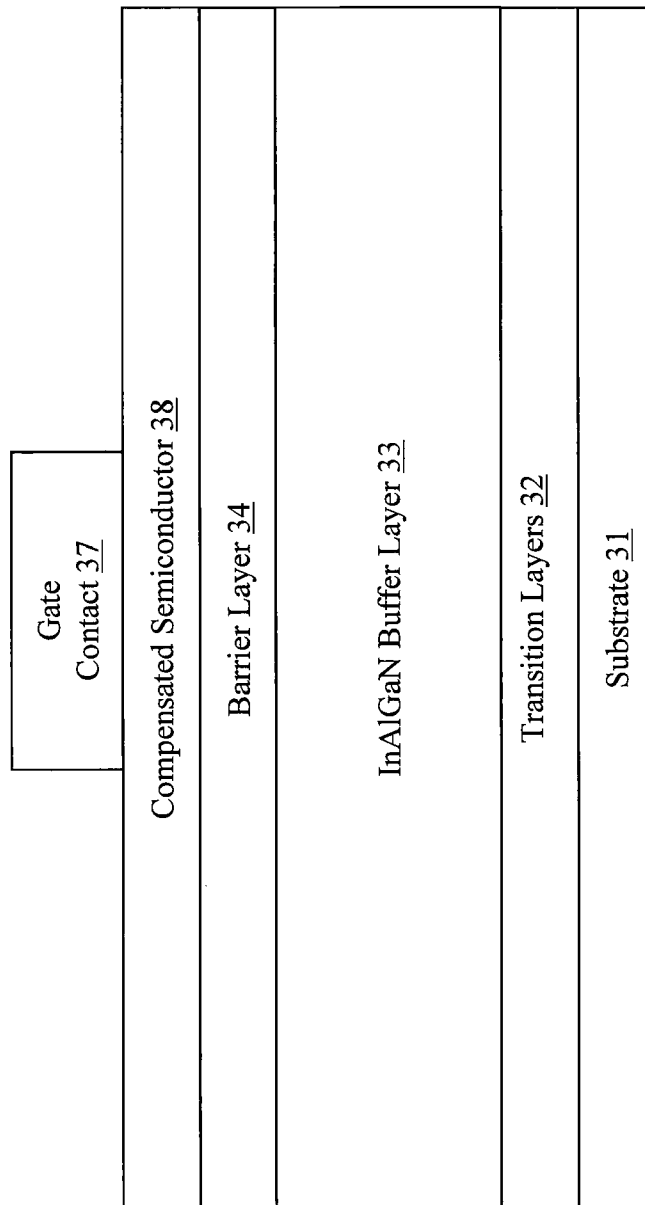


FIG. 9

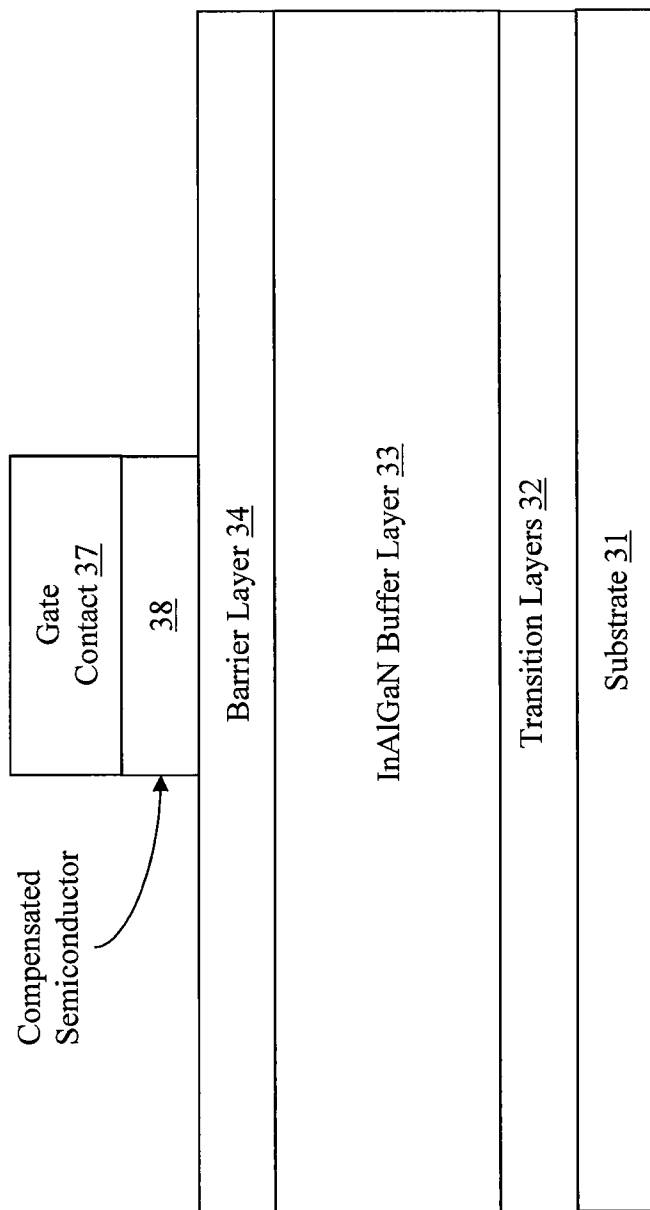


FIG. 10

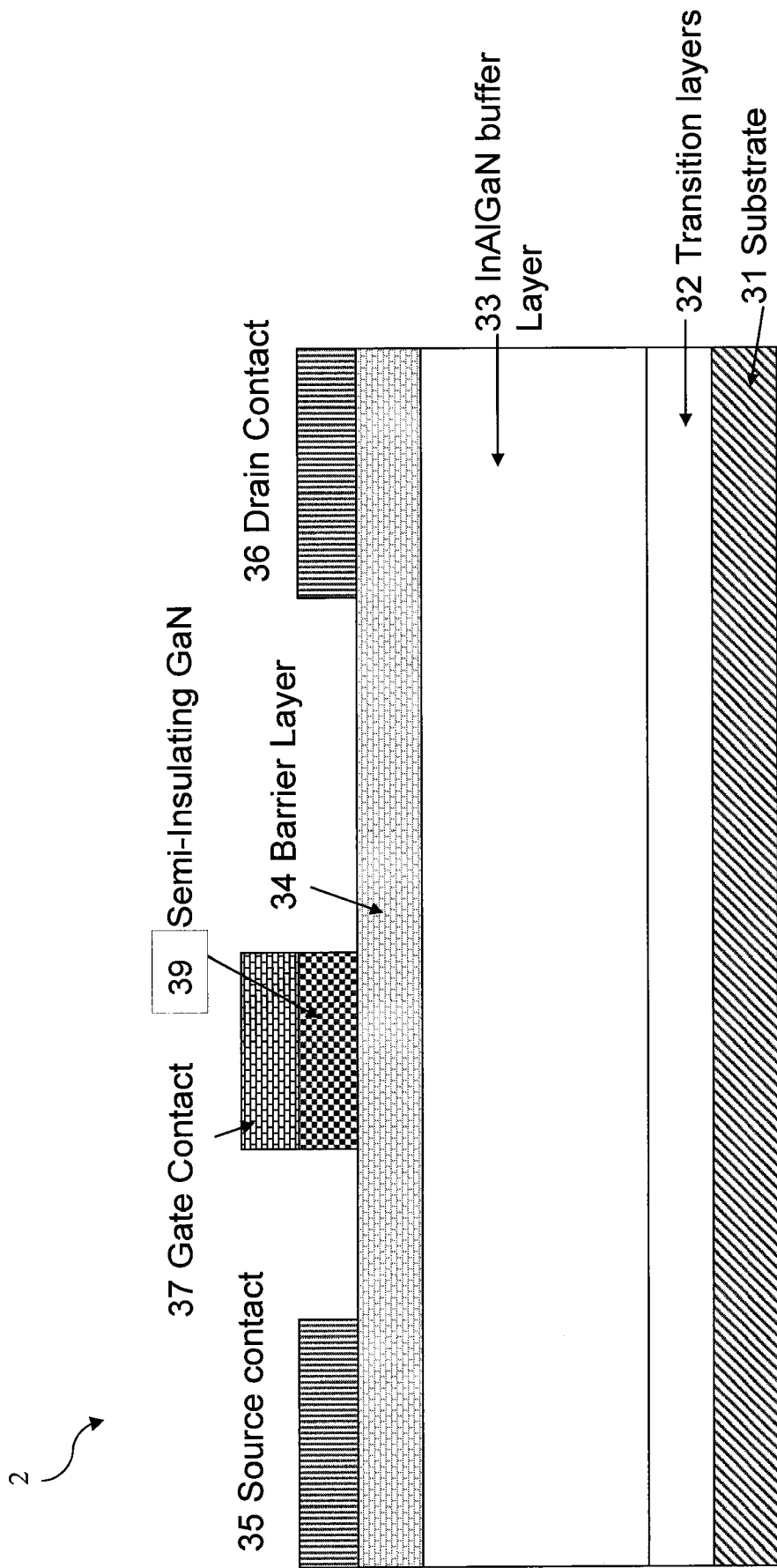


FIG. 11

Semi-insulating Semiconductor <u>39</u>
Barrier Layer <u>34</u>
InAlGaN Buffer Layer <u>33</u>
Transition Layers <u>32</u>
Substrate <u>31</u>

FIG. 12

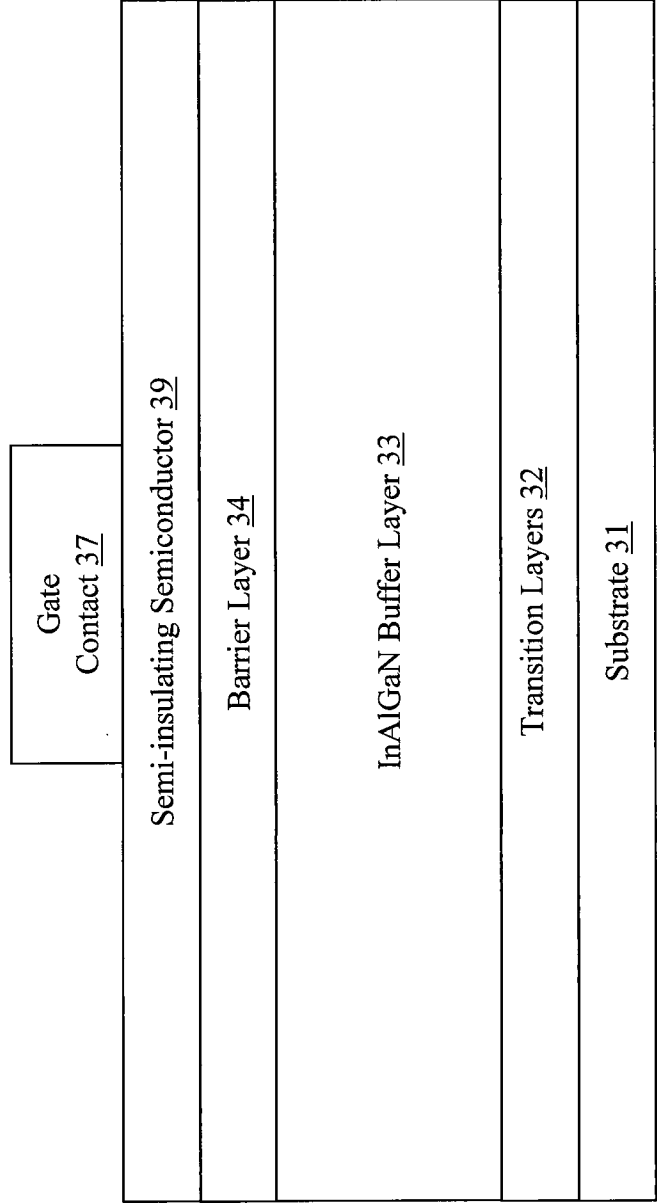


FIG. 13

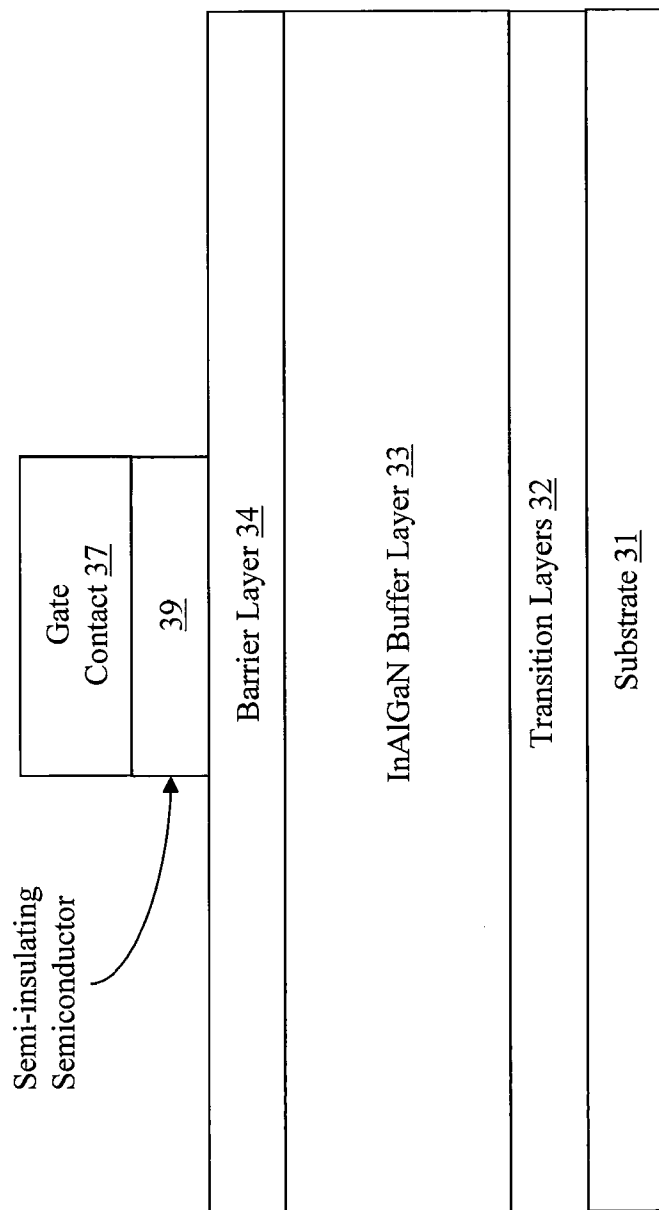


FIG. 14