

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01381
U.S. Patent No. 8,350,294

PATENT OWNER'S RESPONSE

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PATENT OWNER’S EXHIBIT LIST

Exhibit No.	Description
2001	Jorg Neugebauer et al., “Role of Hydrogen Complexes in Doping of GaN,” Material Research Society Symposium Proceedings, Vol. 423 (1996), pp. 619-24 (“Neugebauer-MRS1”)
2002	Jorg Neugebauer et al., “Theory of Point Defects and Complexes in GaN,” Material Research Society Symposium Proceedings, Vol. 395 (1996), pp. 645-56 (“Neugebauer-MRS2”)
2003	EPC’s Responsive Claim Construction Brief: Inv. No. 337-TA-1366, dated October 6, 2023
2004	IEEE Dictionary definition for “compensated”
2005	U.S. Patent No. 6,498,111 (“the ‘111 patent”)
2006	Translation of Innoscience’s Invalidation Request to the Chinese Patent Office for the Chinese Counterpart to the ‘294 Patent
2007	U.S. Patent App. No. 12/756, 906, filed on April 8, 2010
2008	U.S. Provisional App. No. 61/167,792, filed on April 8, 2009
2009	Declaration of Dr. E. Fred Schubert
2010	Respondents’ Post-Hearing Initial Brief (Inv. No. 337-TA-1366)
2011	Declaration of Dr. James Richard Shealy (IPR2023-01384)
2012	Deposition Transcript of Dr. Shealy (IPR2023-01381)
2013	Deposition Transcript of Dr. Shealy (IPR2023-01382, -01384)
2014	Evidentiary Hearing Transcript, pages 1-238 (Inv. No. 337-TA-1366) (Public)(
2015	Evidentiary Hearing Transcript, pages 239-506 (Inv. No. 337-TA-1366) (Public)
2016	Evidentiary Hearing Transcript, pages 741-984 (Inv. No. 337-TA-1366) (Public)
2017	Evidentiary Hearing Transcript, pages 985-1270 (Inv. No. 337-TA-1366) (Public)
2018	Certified Translation of Innoscience’s Invalidation Request to the Chinese Patent Office for the Chinese Counterpart to the ‘294 Patent
2019	Certified Translation of Decision on Innoscience’s Invalidation Request to the Chinese Patent Office for the Chinese Counterpart to the ‘294 Patent

2020	“About Efficient Power Conversion Corporation,” https://epc-co.com/epc/about-epc , printed Mar. 2, 2023
2021	“SEMI Awards Honors Process and Technology Integration Achievements,” https://www.semi.org/en/semi-awards-honor-process-and-technology-integration-achievements , Jan. 13, 2016

I. INTRODUCTION

In accordance with 37 C.F.R. § 42.107, Patent Owner Efficient Power Conversion Corporation (“EPC” or “Patent Owner”) submits this response to the Petition (the “Petition” or “Pet.”) filed by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (“Innoscience” or “Petitioner”) for *Inter Partes* Review of claims 1-12 of U.S. Patent No. 8,350,294 (the “’294 patent”) (Exhibit 1001). Patent Owner respectfully requests that the Board find the claims not unpatentable for at least the reasons set forth below.

The ‘294 patent relates to a compensated gate MISFET (title). Claim 1 specifically recites “a compensated GaN layer” beneath the gate contact. As explained below, the compensated GaN layer in the gate allows the claimed transistor of the ‘294 patent to operate in a normally OFF (enhancement) mode, while also rendering the gate semi-insulating, thereby reducing undesirable gate leakage and gate capacitance.

Compellingly, none of the asserted prior art remotely suggests a transistor with a compensated gate. This is because the compensated gate invention of the ‘294 patent, which achieves two technical effects having opposite requirements for electrical conductivity, was entirely unexpected and went in a direction completely contrary to conventional wisdom at the time of the invention.

Accordingly, for the reasons explained below, Petitioner has not established that the challenged claims are unpatentable.

II. BACKGROUND

A. The '294 Patent

The '294 patent is innovative, novel, and fundamental. It is the product of laborious research and experimentation by brilliant scientists who set out to create a new type of semiconductor. The inventors, including Drs. Alex Lidow and Robert Beach, engaged in years of diligent research and endured numerous failures before achieving their “a-ha” moment. *See* Ex. 2014 at 91:25-93:22 (Lidow) (explaining research done), 96:18-101:5 (detailing first attempts to design a novel GaN device), 106:10-111:13 (detailing experiments), 111:14-140:7 (detailing failures and progress towards “a-ha” discovery), 151:23-153:15 (detailing “body of knowledge” developed), 155:20-157:12 (explaining perfecting device with low leakage current “100,000 times better” than conventional devices and other benefits). The inventors went outside conventional wisdom to arrive at something “that was completely different than what we expected.” Ex. 2014 at 134:6-7 (Lidow).

The '294 Patent describes a novel enhancement mode transistor including a semi-insulating compensated GaN layer located in the gate structure between the gate contact and the 2DEG layer that not only allows the 2DEG to be depleted, but

also reduces gate leakage and gate capacitance—significant deficiencies of the prior art.

GaN transistor devices may be categorized into two different categories: (1) depletion-mode FETs and (2) enhancement-mode FETs. *See* Ex. 1001 at 1:42-54; Ex. 2009 at ¶[27]. *See id.* Depletion-mode FETs maintain an “ON” state at zero gate-source voltage (normally ON), while enhancement mode FETs maintain an “OFF” state at zero gate source voltage (normally OFF). *See id.* Depletion-mode FETs deplete the 2DEG located near the junction of two layers having different band gaps. *See id.* In the depletion-mode FETs, an electron channel that exists at zero gate voltage is depleted by applying a negative gate voltage, thereby turning the FET OFF. *See id.* Conversely, enhancement-mode FETs have no electron channel at zero gate voltage, but an electron channel can be induced by applying a positive gate voltage, thereby turning the FET ON. *See id.*

The structure of a conventional GaN FET generally includes a substrate, a transition layer or layers (including a nucleation layer) that transitions the crystal growth from the substrate to the III-N epitaxial layers (e.g., AlGa_N), a III-N buffer layer (e.g., GaN), a III-N barrier layer (e.g., AlGa_N), and an optional p-type gate semiconductor material (e.g., GaN). *See* Ex. 1001 at 1:55-2:2. A FET further includes three metal contacts: source, gate, and drain. *See id.*

As shown in Fig.1 of the '294 patent, an enhancement-mode transistor in the prior art has a conductive p-type GaN gate semiconductor. Ex. 1001 at 1:55-2:2. GaN is a piezoelectric material, which means that its crystal produces an electric field when strained. Ex. 2009 at ¶ [26]. When a thin layer of aluminum gallium nitride (AlGa_N) is added to the surface of the GaN, substantial strain can be created, resulting in an electrical field that attracts electrons to the GaN surface. *Id.* That attraction of electrons results in the formation of a two-dimension electron gas (2DEG) that is highly conductive and able to carry a large current. *Id.* When the p-type doping concentration in the GaN gate semiconductor (e.g., doping with Mg) is sufficiently high and the layer is sufficiently thick, the acceptors in the gate layer accept electrons, specifically electrons of the 2DEG, thereby depleting the 2DEG and interrupting the electron channel formed between source and drain. Ex. 1001 at 1:42-2:2.

The 2DEG is a thin sheet of free electrons located at the interface between the two semiconductor layers, typically a GaN buffer layer and an AlGa_N barrier. Ex. 2009 at ¶ [26]. The barrier and buffer layers extend from the source to the drain of the HEMT, so that the 2DEG can serve as an electron channel between the source and drain of the field-effect transistor. *Id.*

The compensated GaN layer of the '294 patent achieves two opposing effects related to electrical conductivity requirements. First, as the p-type GaN

layer is grown, the Mg acceptors accept electrons from the 2DEG, thereby depleting the 2DEG and creating a normally-OFF (enhancement-mode) transistor. *See* Ex. 1001 at 3:10-17; Ex. 2009 at ¶ [53, 68]. The magnesium acceptors in the p-GaN preferentially deplete electrons from the 2DEG before accepting electrons from any hydrogen in the p-GaN, because taking electrons from the 2DEG is energetically more favorable—on the order of 2 to 3 electron volts. *Id.*

Second, also during the growth process, the remaining Mg acceptors are passivated by hydrogen, so that the p-type conductivity in the p-doped GaN is substantially reduced, and the p-doped GaN is, in fact, semi-insulating. *See* Ex. 1001 at 3:15-21, 43-52. As a result, the gate capacitance and undesirable gate bulk leakage current through the bulk (not surface) of the p-doped GaN becomes small. *See* Ex. 1001; Ex. 2009 at ¶ [53, 69]. This is in accordance with the teaching of the '294 patent: “the compensated semiconductor layer 38 is a highly compensated semi-insulating material” Ex. 1001 at 3:47-48.

In the enhancement mode embodiments of Figs. 2-9, the '294 patent discloses a GaN transistor in which “a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the gate contact 37.” Ex. 1001 at 3:8-9. The '294 patent explains that the compensated GaN gate material offers at least **two** benefits over the prior art, in that it (1) “leads to **low gate leakage** during device operation,” (*id.* at 3:18-19) and (2) “**reduces the gate capacitance** of the

device.” *Id.* at 3:20-21. The ’294 patent further notes that “the high doping level of the compensated layer 38 leads to enhancement mode devices.” *Id.* at 3:16-17.

These effects were entirely unexpected according to the conventional wisdom. Ex. 2009 at [71]. Based on the teachings of the prior art technical literature, a POSA (person of skill in the art) would have concluded that passivated p-doped GaN cannot be used to deplete the 2DEG and cannot create enhancement transistors. Ex. 1018; Ex. 2001; Ex. 2002; Ex. 2009 at [71]. The prior art at the time of the ’294 patent disclosed that passivated Mg-H complexes are **neutral**. *Id.* Being neutral means that there is no electrical effect and a POSA would thus not have found passivation of p-doped GaN to be useful in the design of enhancement-mode transistors. *Id.* The invention of the ’294 patent fundamentally altered this thinking.

B. Grounds of Challenge

The petitioner challenges the patentability of claims 1-12 of the ’294 patent on three grounds:

Ground 1: Claims 1-12 are challenged as being obvious over Smith, either alone (Ground 1A), in view of Kigami (Ground 1B), or in view of Uemoto (Ground 1C).

Ground 2: Claims 1-12 are challenged as being obvious over Uemoto in view of Smith.

For purposes of the present response, Patent Owner specifically responds to the challenges of claims 1-3 and 7-9. The remaining claims are cancelled by way of Patent Owner's Motion to Amend filed concurrently herewith.

III. LEVEL OF ORDINARY SKILL IN THE ART

Based on the description in the '294 patent and the relevant art discussed during the prosecution history and cited on the patent, EPC submits that a person of ordinary skill in the art in the contact of the '294 patent would have possessed at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN. Ex. 2009 at ¶ [82]. Relevant graduate education could substitute for the professional work experience. *Id.* Dr. Schubert opines, however, that the difference between Innoscience's proposed POSA and EPC's proposed POSA would not affect the outcome of this proceeding or change his opinion in any material manner. *Id.* at ¶ [83].

IV. CLAIM CONSTRUCTION

A. "A Gate Contact Above the Compensated GaN Layer"

Patent Owner asserts that "a gate contact above the compensated GaN layer," when read in view of the intrinsic evidence, should be construed as "a gate comprised of a gate contact and the compensated GaN layer." The proper

construction of a claim term must “capture the scope of the actual invention,” rather than allowing the claim language to become “divorced from what the specification conveys is the invention.” *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1304 (Fed. Cir. 2011). Here, the misapplication of the prior art to the claims by Petitioner contorts the plain meaning of “a gate contact above the compensated GaN layer,” so that the claims cover transistors that do not meet the goals of the invention, make it clear that a proper construction specifying that the gate contact and compensated GaN layer are part of a gate structure, is necessary. Ex. 2009 at ¶ [89].

The '294 patent explains that the compensated GaN layer offers **two** primary goals, in that it (1) “leads to **low gate leakage** during device operation,” (Ex. 1001 at 3:18-19) and (2) “**reduces the gate capacitance** of the device” due to “the insulating nature” of the compensated GaN layer. *Id.* at 3:19-21.

Petitioner attempts to divorce the claim language from the disclosed goals of the invention and impermissibly broadens the claim to include devices with a purported compensated GaN layer that does not reduce the gate capacitance of the device. The only way for a compensated GaN layer to reduce gate capacitance is for the compensated GaN layer to be part of the gate. A compensated GaN layer that is not part of the gate has no effect on the gate capacitance. Ex. 2009 at ¶ [90]

Capacitance can be calculated using the formula, $C = Q/V$, where Q is charge, and V is voltage. Gate capacitance is the capacitance between the gate and the 2DEG channel. If a transistor has primarily conductive material directly underneath the gate contact, the charge carried by the conductive material will make the corresponding gate capacitance relatively high, like the prior art transistor depicted in the '294 patent or the *Uemoto* reference used by Petitioner to challenge the claims. Conversely, if a transistor has the compensated GaN layer of the '294 patent directly underneath the gate contact, the insulating nature of the compensated GaN layer greatly drives down the charge running through the gate, thus making the gate capacitance low. Accordingly, Patent Owners's proposed construction – that “a gate contact above the compensated GaN layer” should be construed as “a gate comprised of a gate contact and the compensated GaN layer” – is consistent with the inventors' identified invention goals.

Indeed, proper construction is to “capture the scope of the actual invention,” rather than allowing the claim language to become “divorced from what the specification conveys is the invention. *Retractable Techs.*, 653 F.3d at 1305. Patent Owner's construction is necessary to “tether the claims to what the specifications indicate the inventor actually invented.” *Retractable Techs.*, 653 F.3d at 1305; *see also Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1346 (Fed. Cir. 2018) (“the claim must be read ... in order to be faithful to the invention

disclosed in the specification”); *Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296, 1305 (Fed. Cir. 2017) (restricting the claim to a specific process to avoid “the impermissible result of extending [the] monopoly beyond the invention disclosed, and potentially to the prior art.”) (internal quotations omitted); *Gemalto S.A. v. HTC Corp.*, 754 F.3d 1364, 1369-71 (Fed. Cir. 2014) (affirming narrow construction based on purpose of invention and distinctions over prior art because “the claims cannot be of broader scope than the invention that is set forth in the specification.”) (internal quotations omitted); *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998) (“construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.”).

Moreover, the specification provides important context for the claim language. For example, the specification provides a method of making the device depicted in Figure 2 (a transistor) and recites the step of “etch[ing] away the compensated semiconductor layer 38, except *the portion beneath the gate contact layer 37.*” (emphasis added) *See* Ex. 1001 at 3:35-38. Here, it is clear that the specification is describing a process to make a transistor with a gate structure that includes a gate contact and compensated GaN. A POSA reading the claim in light of the specification would have understood the claimed “gate contact *above* the compensated GaN layer” to be referring to the structure that results from etching

away the compensated GaN layer except the portion *beneath* the gate contact, detailed above in the specification. That is, “above” means more than merely “higher than”; it implies a gate structure that includes a gate contact and compensated GaN layer. Ex. 2009 at ¶ [91].

B. “Compensated GaN Layer”

Petitioner correctly sets forth Petitioner’s proposed claim construction from a related matter but misstates Patent Owner’s construction, which was modified during responsive briefing of the related matter. Ex. 2003 at 6. Patent Owner proposes that the term “a compensated GaN layer” in claim 1 should be construed as “a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).” Ex. 2009 at ¶ [92].

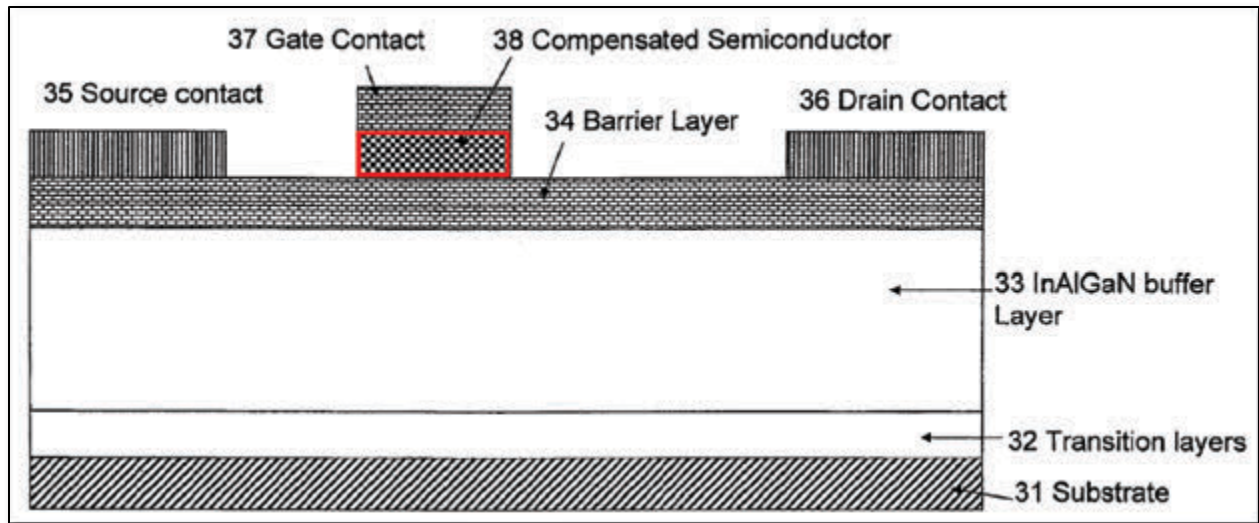
1. “GaN Layer” Refers to GaN Gate Material

Claim 1 of the ’294 patent describes a transistor where the “compensated GaN layer” is formed “above the barrier layer” and that “a gate contact” is formed “above the compensated GaN layer.” A POSA would understand from the placement of the “compensated GaN layer” between the barrier and the gate contact that the “GaN layer” is a GaN gate material. Ex. 2009 at ¶ [93].

The POSA’s interpretation and understanding of this fundamental claim term based on the claim language itself is confirmed by the specification. “[T]he

specification is always highly relevant to the claim construction analysis . . . [and] it is the single best guide to the meaning of a disputed term.” *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Here, the entirety of the specification refers solely to a compensated GaN gate material. The ’294 patent is titled “Compensated **Gate** MISFET and Method for Fabricating Same.” The specification details the problems with prior art GaN transistors having unfavorable **gate** leakage (*see* Ex. 1001 at 1:55-2:6) and identifies a solution to that problem by creating a compensated **gate** that leads to “low **gate** leakage” and “reduce[d] [] **gate** capacitance.” Ex. 1001 at 3:17-20 (emphasis added). Ex. 2009 at ¶ [94].

The figures and Summary of Invention further confirm the POSA’s understanding of the meaning of “compensated GaN layer” based on the claim itself. Indeed, in describing Figure 2, the specification explains that “a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the **gate** contact 37.” Ex. 1001 at 3:7-9 (emphasis added). Figure 2 (excerpted below with the compensated GaN layer annotated in red) has the same structure as recited in claim 1. Ex. 2009 at ¶ [95].



A POSA would understand that the layer between the gate contact and the barrier layer - in Figure 2 just as in claim 1 - refers to a GaN gate material. Indeed, the Summary of Invention explains that the claimed inventions are directed to using a material “below the gate contact and above the barrier layer” to “reduce[]” “gate leakage.” *Id.* at 2:14-16; *see also id.* at 3:18-21 (“using a compensated semiconductor layer **38** leads to low *gate* leakage during device operation”) (emphasis added). A POSA would understand that it is the gate material between these layers that contributes to reducing gate leakage, not some other type of GaN layer. Ex. 2009 at ¶ [96].

Moreover, the '294 patent explains that the compensated GaN layer offers **two** primary goals, in that it (1) “leads to **low gate leakage** during device operation,” (*id.* at 3:18-19) and (2) “**reduces the gate capacitance** of the device” due to “the insulating nature” of the compensated GaN layer. *Id.* at 3:19-21. Ex.

2009 at ¶ [97].

In short, the intrinsic evidence confirms that a POSA would have understood the term “compensated GaN layer” as used in claim 1 to be referring to a compensated GaN gate material, which is the only structure described in the intrinsic evidence as providing the advantages to the claimed transistor over the prior art and which the applicant identified as being at the heart of the claimed inventions. Ex. 2009 at ¶ [98].

2. “Compensated” Describes a Semiconductor with Modified Electrical Characteristics

A POSA would have understood the term “compensated” to have its plain and ordinary meaning in the art. The IEEE dictionary defines “compensated semiconductor” as “[a] semiconductor in which one type of impurity or imperfection (for example, donor) partially cancels the electric effects of the other type of impurity or imperfection (for example, acceptor).” Ex. 2004. Patent Owner’s construction is consistent with that definition. Ex. 2009 at ¶ [99].

The description of “compensated” in the specification of the ’294 patent is consistent with the plain and ordinary meaning of “compensated.” For example, the specification explains that the compensated GaN gate material includes a p-type impurity (e.g., Mg, Zn, Be, Cd, or Ca) that imparts an electric effect (i.e., conductivity), and a second impurity, e.g., hydrogen, that partially cancels the electric effect of the p-type impurity by rendering it semi-insulating. Ex. 1001 at

3:10-13, 3:43-45. The specification explains further that by having the electrical effect of the p-type impurity cancelled out by another impurity, the p-type gate material is differentiated from the prior art by having modified electrical characteristics—specifically, by being more resistive than the conductive structures found in the prior art. *See id.* at 3:46-49 (“the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material.”). A more resistive p-type GaN gate material has improved functional characteristics compared to the prior art, including “low gate leakage during device operation,” *id.* at 3:16-19, reduced gate capacitance, and the ability to act as an enhancement mode device (where the transistor is activated only when a positive voltage is applied to the gate contact). Indeed, nowhere does the ’294 patent refer to a compensated GaN material anywhere other than in connection with the compensated GaN gate. In fact, a POSA reading the ’294 patent – beginning with its title – would have understood the compensated GaN as part of the gate to be the novel feature that distinguished the claimed transistor from the prior art by reducing gate leakage. Ex. 2009 at ¶ [100].

Because the term “compensated” has a plain meaning in the art and because the intrinsic evidence describes a “compensated GaN layer” consistent with the

plain meaning of the term, Patent Owner’s plain-meaning construction should be adopted. Ex. 2009 at ¶ [101].

3. Petitioner’s Construction Should be Rejected

Petitioner’s construction of “compensated GaN layer” as “a doped GaN layer formed with a step to passivate its impurities” is incorrect for several reasons.

First, Petitioner’s construction does not apply the plain and ordinary meaning of “compensated GaN layer” to a POSA as “compensated ***GaN gate material***.” As discussed above, the claimed structure is not referring to any GaN layer, but rather a gate material. Thus, Petitioner’s non-construction renders the term impermissibly broader than its plain meaning in view of the intrinsic evidence, resulting in an inoperable transistor. Ex. 2009 at ¶ [103].

Second, Petitioner’s failure to construe GaN layer consistent with the intrinsic evidence by limiting the GaN layer to the gate material would encompass transistor designs in which the compensated GaN layer does not serve as gate semiconductor material and does not reduce the bulk gate leakage current and gate capacitance, as taught in the ’294 patent. For example, a transistor with a compensated GaN layer that is separate from the gate structure and in contact with the source and the drain would fall under Petitioner’s expansive construction. In such a transistor, the gate structure would consist only of the metal, and as a result, the compensated GaN layer would not prevent gate leakage and gate capacitance,

as taught by the '294 patent. Petitioner's reading of the claim term in isolation is therefore incorrect. Ex. 2009 at ¶ [104].

Third, “compensated GaN layer” is not a product-by-process limitation. Indeed, nothing in the claim defines the “compensated GaN layer” in terms of the processes used to compensate. The purpose of the product-by-process “doctrine is to prevent foreclosing inventors ‘from the benefits of the patent system simply because a product is difficult to describe in words, or its structure is insufficiently understood.’” *In re Biogen* 335 F. Supp. 3d 688, 712 (D.N.J. 2018) (quoting *SmithKline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312 (Fed. Cir. 2006)), *rev'd and remanded sub nom. Biogen MA Inc. v. EMD Serono, Inc.*, 976 F.3d 1326 (Fed. Cir. 2020). In this case, claim 1 of the '294 patent is not directed to a product that the inventors were unable to describe in words or where the product's structure was not sufficiently understood. *Id.* As discussed above, the IEEE dictionary itself underscores that the term is well understood in the field and a POSA would have readily understood that the term “compensated GaN” layer refers to a GaN layer having certain structural and electric characteristics, not a GaN layer made according to a particular process. Ex. 2009 at ¶ [105].

Petitioner argues that “while the claim uses ‘compensated as an adjective, that adjective derives from a past-tense verb” and that “[t]he past-tense form of ‘compensated’ suggests that the step of compensating had occurred.” Petition at

14. Even if Respondents were correct that the term “compensated” derives from a past-tense verb, that does not transform the term “compensated” into a process term. Indeed, in *In re Garnero*, the predecessor court to the Federal Circuit recognized that past-tense verbs such as “‘intermixed,’ ‘ground in place,’ ‘press fitted,’ ‘etched,’ and ‘welded’ all . . . at one time or another have been separately held capable of construction as structural, rather than process, limitations.” 412 F.2d 276, 279 (C.C.P.A. 1969); *see also* *3M Innovative Prop. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003); *Hazani v. U.S. Int’l Trade Comm’n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997). As discussed above, “compensated GaN layer” is not merely “capable of construction as [a] structural, rather than a process, limitation,” *In re Garnero*, 412 F.2d at 279, a POSA would understand the term to be a structural term. Ex. 2009 at ¶ [106].

But even if the Court believes that “compensated” can be interpreted as both a structural limitation (as Patent Owner proposes) and as a process limitation (as Petitioner proposes), the term still would not be a product-by-process limitation. “[W]ords of limitation that can connote with equal force a structural characteristic of the product or a process of manufacture are commonly and **by default** interpreted in their structural sense, unless the patentee has demonstrated otherwise.” *In re Nordt Dev. Co.*, 881 F.3d 1371, 1375 (Fed. Cir. 2018) (emphasis added). Here, Patent Owner has clearly demonstrated that “compensated” is to be

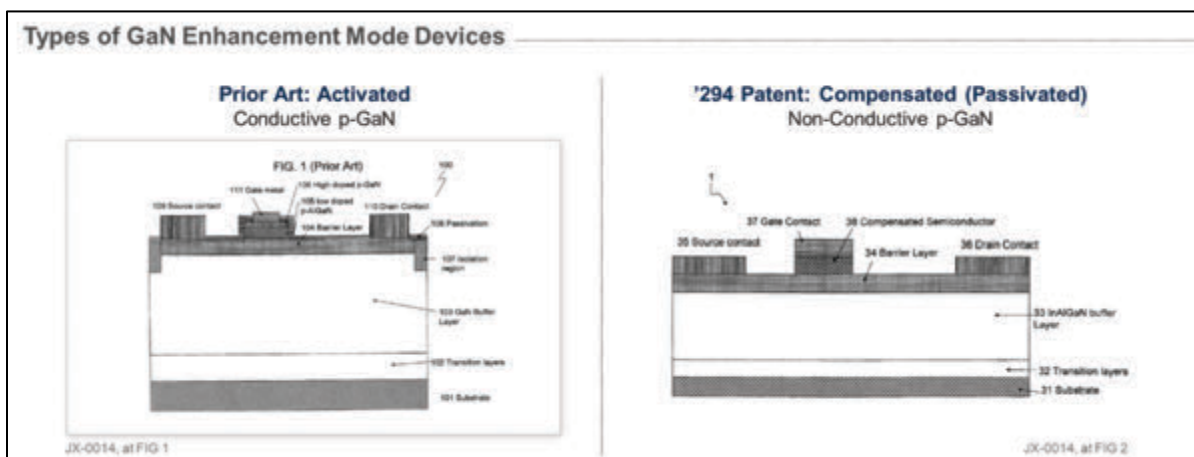
interpreted in its structural sense as allowing for modified electric characteristics in a GaN gate material that were otherwise possible in a material that was not compensated. *See Hazani*, 126 F.3d at 1479 (“chemically engraved” limitation not a product-by-process limitation because the limitation, “read in context, describes the product more by its structure than by the process used to obtain it”). Ex. 2009 at ¶ [107].

C. Claim 1 is Directed to an Enhancement-Mode Transistor

Claim 1 of the '294 Patent is directed to an enhancement mode transistor. The “Field of the Invention” section of the '294 Patent confirms that the invention “relates to the field of enhancement mode gallium nitride (GaN) transistors.” Ex. 1001 at 1:13-14. Ex. 2009 at ¶ [108].

The specification of the '294 Patent explains that the compensated semiconductor GaN layer 38, which is recited in claim 1, is formed over the barrier layer 34 and under the gate contact 37, and further discloses that “the high doping level of the compensated layer 38 leads to enhancement mode devices.” *See id.* at 3:8-9, 16-17. The '294 Patent describes the compensated semiconductor gate, in particular, a compensated GaN gate material, as the element that “leads to low gate leakage during device operation” and “reduces the gate capacitance of the device,” which remedies deficiencies in the prior art enhancement-mode GaN transistor described in FIG. 1. *Id.* at 3:18-21, 2:3-6 (referring to FIG. 1). Ex. 2009 at ¶ [109].

At the evidentiary hearing of the related ITC proceeding set forth in Patent Owner’s Mandatory Notice (Investigation No. 337-TA-1366), EPC’s expert, Dr. Schubert, further confirmed that the compensated GaN layer of claim 1 results in an enhancement-mode transistor, stating: “The high doping of the semi-insulating [compensated] layer 38 leads to enhancement-mode devices. The 2DEG region is depleted, that is, removed.” Ex. 2015 at 436:5-17, 442:20-443:18 (Schubert). Moreover, in his comparison of the prior art enhancement-mode device to the compensated GaN transistor disclosed by the ’294 Patent, Dr. Schubert explained that both devices were enhancement-mode, but the difference between the two was the non-conductive nature of the compensated p-GaN layer of the inventive device. *Id.* at 433:5-22. Thus, as Innoscience agrees, the p-doping of the p-GaN that is required for forming the compensated GaN layer recited in claim 1 results in an enhancement-mode transistor. Exhibit 2016 at 936:17-937:2 (Lebby) (“If you design a device with p-type material as we’ve heard in this litigation, it’s enhancement-mode.”). Ex. 2009 at ¶ [110].



'294 Patent at FIGS. 1 & 2 (Annotated)

The '294 Patent discloses (and must use) p-type dopants in its compensated GaN gate material, in order to deplete the 2DEG, as explained above, and thereby forms an enhancement-mode device. See Exhibit 2016 at 926:1-22 (Lebby) (admitting that p-type doping is necessary for a device to be enhancement-mode). Indeed, the '294 Patent states that its “[c]ompensated semiconductor layer 38 preferably comprises AlGaN or GaN with a deep level passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca.” Ex. 1001 at 3:10-12. Experts for both parties agree that p-type dopants are necessary for depletion of the 2DEG at zero voltage, without which the enhancement-mode device described in the '294 Patent is unattainable. Exhibit 2016 at 926:16-22, 936:17-937:2 (Lebby) (“If you design a device with p-type material as we’ve heard in this litigation, it’s enhancement-mode.”), 956:13-21 (Schubert). Ex. 2009 at ¶ [111].

Innoscience’s expert from the related ITC proceeding, Dr. Lebby, agreed that a compensated GaN layer results in an enhancement-mode GaN transistor, conceding that there would be no 2DEG beneath the compensated layer 38 (as shown FIG. 2 of the '294 Patent) at zero voltage. Ex. 2016 at 933:19-934:3 (Lebby). It is also undisputed that this depletion of the 2DEG electrons would result in an enhancement-mode device. *Id.* It follows then that claim 1, reciting precisely such a compensated GaN layer, is directed to an enhancement-mode transistor. Indeed, the Chinese National Intellectual Property Administration (CNIPA) found claim 1

to be directed to an enhancement mode transistor in its recent decision finding the identical claims of the Chinese counterpart to the '294 patent valid. Ex. 2019 at 11 (stating “Claim 1 seeks protection for an enhancement mode transistor.”) Ex. 2009 at ¶ [112].

D. Claims 2 and 3 Are Directed to an Enhancement-Mode Transistor

Claims 2 and 3 of the '294 Patent are indisputably directed to enhancement-mode transistors. Claim 2 recites “the acceptor type dopant atoms are passivated by hydrogen,” while claim 3 adds that “the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.” Ex. 1001 at 5:18-23. Claims 2 and 3 thus require the use of acceptor type dopants that can be passivated by hydrogen. The parties do not dispute that only p-type dopants, such as Mg, Zn, Be and Ca, can be passivated by hydrogen. Ex. 2016 at 955:5-21 (Schubert) (“It is only the p-type dopants that are passivated by hydrogen”). Furthermore, testimony from both parties in the related ITC proceeding demonstrates that enhancement-mode operation requires the use of p-type dopants; indeed, the use of a p-type dopant (magnesium) passivated with hydrogen in GaN would result in an enhancement-mode device, as Dr. Lebby (Petitioner’s expert in the ITC proceeding) conceded during the hearing. Ex. 2017 at 997:10-998:1 (Schubert); Ex. 2016 at 936:17-937:2 (Lebby) (“If you design a device with p-type material as we’ve heard in this litigation, it’s enhancement-mode.”), 923:6-17 (Lebby). And as Petitioner admits

in its post-hearing brief for the ITC proceeding, a transistor with p-type doping “passivated with hydrogen **would** function as an enhancement mode device.” Ex. 2010 at 41 (emphasis added). Accordingly, claims 2 and 3 must be directed to an enhancement-mode transistor. Ex. 2016 at 923:6-17 (Lebby) (stating that magnesium passivated with hydrogen produces an enhancement-mode transistor). Ex. 2009 at ¶ [113].

V. REBUTTAL TO STATEMENT OF FACTS

Petitioner’s alleged Statement of Material Facts (Pet. at 12-13) is materially deficient and should be ignored. Petitioner failed to include any citations to the record supporting any of its alleged facts (*see* 37 C.F.R. § 42.22(c)), and therefore, the alleged facts should not be assumed into evidence, nor is it Patent Owner’s responsibility to presuppose and rebut the alleged evidence.

VI. GROUND 1A: CLAIMS 1-3 AND 7-9 ARE NOT UNPATENTABLE OVER SMITH ALONE

In Ground 1A, Petitioner asserts that *Smith* alone “discloses the allegedly inventive elements, including the “compensated GaN” and “semi-insulating” layers recited in independent claims 1 and 7 of the ‘294 patent. Petition, pp. 21-22, 38, 46, 50 and 53. As explained below, Petitioner misinterprets and misrepresents the teachings of *Smith*. Ex. 2009 at ¶ [114].

A. Smith does not disclose an enhancement mode transistor, as required by claims 1-3

Petitioner relies upon FIG. 2A of *Smith* as purportedly disclosing the limitations of claim 1. Claims 1-3 are directed to enhancement mode transistors, as noted above.

By contrast, *Smith* discloses a depletion mode transistor, a fact confirmed by the Chinese National Intellectual Property Administration (CNIPA) in its recent decision finding the identical claims of the Chinese counterpart to the '294 patent valid. Ex. 2009 at ¶ [116]; Ex. 2019 at 10 (stating *Smith* (D1) “discloses a depletion mode transistor...”) Any suggestion that *Smith* can operate as an enhancement mode transistor fails, because FIG. 2A (1) is non-functional as an enhancement mode transistor; and (2) cannot actually be manufactured as depicted in the figure. In his declaration in concurrently pending IPR-2023-01382 and IPR-2023-01384, which relate to U.S. Pat. Nos. 9,748,347 and 10,312,335, respectively, Petitioner’s expert also analyzed U.S. Pat. Pub. No. 2006/0108606 (“*Saxler*”). Ex. 2011 (Shealy Decl. from ‘335 IPR). *Saxler* depicts FIGs. 1B and 2A, which are identical to FIGs. 1B and 2A of *Smith*, respectively, as confirmed by Petitioner’s expert. Ex. 2009 at ¶ [116]; Ex. 2012 at 43:7-49:19. A review of the *Saxler* and *Smith* specifications confirms that both references’ FIGs. 1B and 2A, respectively, describe the same device. Ex. 2009 at ¶ [116].

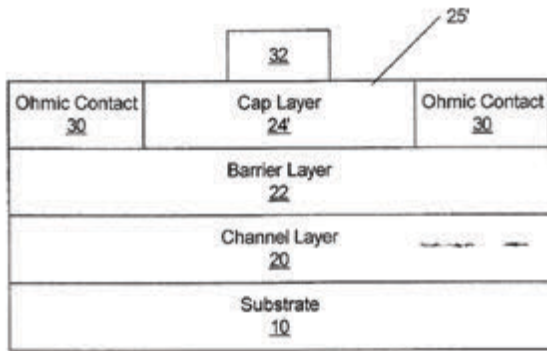


Figure 1B

Smith, FIG. 1B

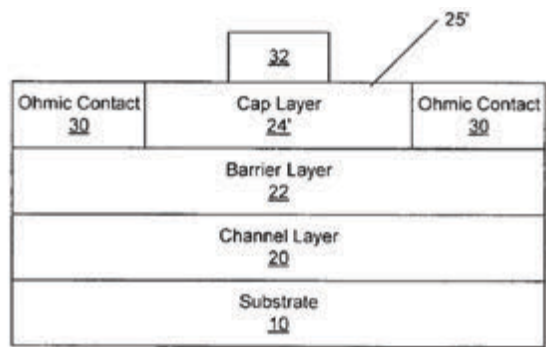


Figure 1B

Saxler, FIG. 1B

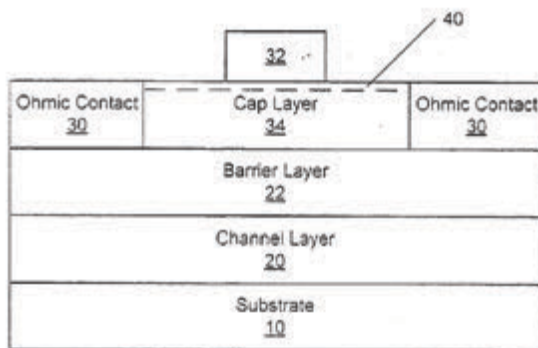


Figure 2A

Smith, FIG. 2A

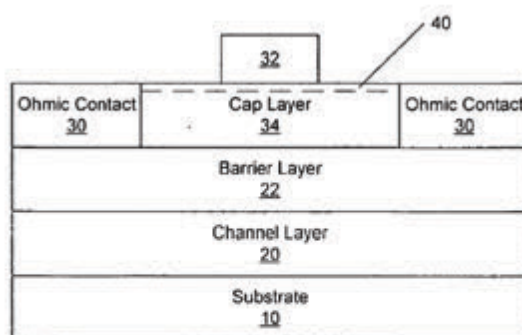


Figure 2A

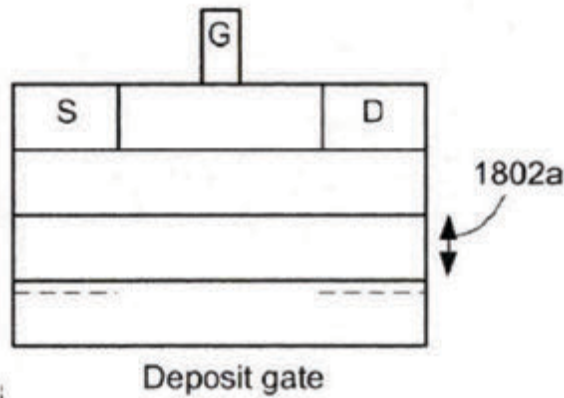
Saxler, FIG. 2A

Furthermore, the only difference between FIG. 1B and FIG. 2A of each reference is that FIG. 2A has a doped region 40 over the cap layer 34, while FIG. 1B does not. Notably, all of the figures from both references show that the cap layer 34 (with or without the doped region 40) extends over the barrier layer 22 and is formed such that it is in direct contact with **both** ohmic contacts 30. Ex.

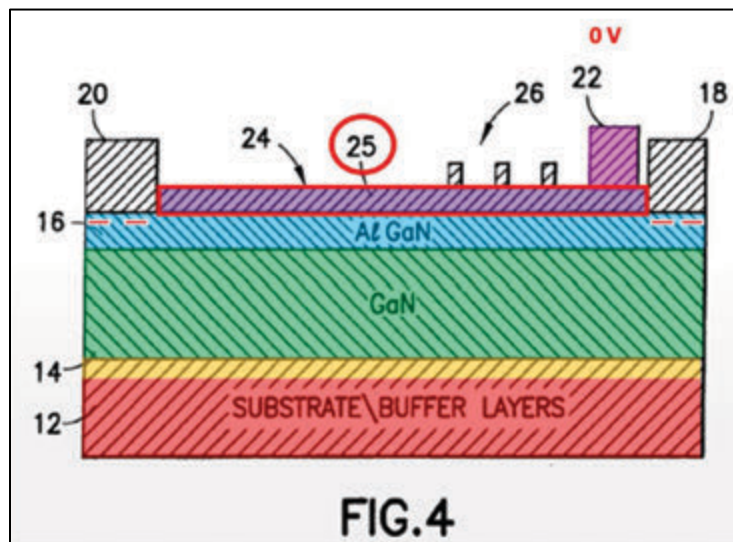
2009 at ¶ [117]; Ex. 2012 at 43:7-49:19. These characteristics render the transistor non-functional in enhancement mode. Ex. 2009 at ¶ [117]; Ex. 2013 at 57:8-12; 62:12-63:12.

If cap layer 34 has p-type doping at zero voltage the p-type doping would deplete the 2DEG the entire length between the ohmic contacts 30. When a positive voltage is applied to the gate contact 32, the 2DEG is only reconstituted generally under the gate, which is insufficient to turn the device ON because the 2DEG is not continuous between the ohmic contacts. Instead, the 2DEG would still be missing in the so-called access regions between the gate contact and the ohmic contacts. Ex. 2009 at ¶ [118].

Several things corroborate this understanding. First, a portion of Fig. 18 of the *Suh* reference, shown below, shows that when p-type GaN extends all the way across from source to drain in a transistor, the entire 2DEG region from source to drain is depleted at zero volts. Petitioner's expert in the ITC proceeding confirms this fact. Ex. 2016 at 937:11-24 (Lebby). That same expert later confirmed that if a positive voltage were to be applied to the gate electrode of *Suh*, only the 2DEG generally below the gate electrode would be reconstituted. *Id.* at 938:1-10 (Lebby). Ex. 2009 at ¶ [119].

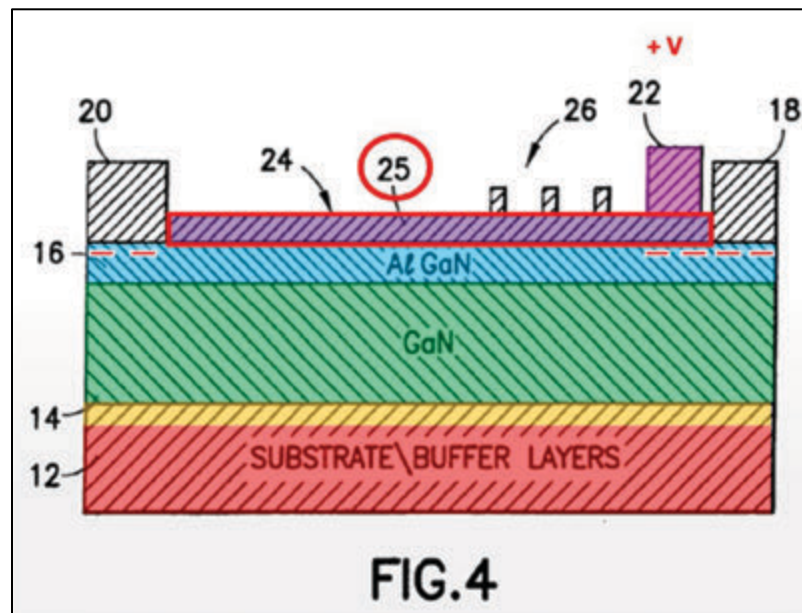


Petitioner and its expert made similar arguments with respect to prior art (*Beach189*) that Petitioner asserted against the '294 patent in the ITC proceeding. At zero voltage, under Innoscience's own interpretation, the 2DEG (represented as red dash "–") is fully depleted from the source to the drain, confirming Dr. Schubert's testimony that the device would be inoperable as an enhancement-mode device. Ex. 2016 at 937:11-24 (Lebby), 954:11-24 (Schubert); Ex. 2010 at 41. Ex. 2009 at ¶ [120].



Ex. 2010 at 41

Innoscience agrees that the 2DEG is not reconstituted between the source and the drain when a positive voltage—necessary for enhancement-mode operation—is applied to the gate. Ex. 2016 at 938:1-10 (Lebby); Ex. 2010 at 41. When such a positive voltage (+v) is applied, as shown below, the 2DEG (represented as red dash “–”) is *only* reconstituted under the gate, which is insufficient to turn the device ON because the 2DEG is not continuous between the source and drain contacts. *Id.* Petitioner’s expert in the ITC proceeding admitted as much during his redirect examination at trial, referring to the image below, noting that “...you can establish a 2DEG with a positive voltage on an enhancement-mode, and the question here is, is that the 2DEG doesn’t – **it’s not continuous all the way from the source to the drain...**” Ex. 2016 at 938:5-10 (emphasis added).



Ex. 2010 at 41

Innoscience theorized that the 2DEG could conceivably exist if you put enough voltage on it. Ex. 2010 at 41-42. But that is scientifically inaccurate. Indeed, Petitioner's expert from the ITC proceeding admitted that he has no quantitative basis for his theory—he conceded that he has neither modeled nor simulated any part of this theory. Ex. 2016 at 938:19-939:8 (Lebby). The expert's vague instructions to a POSA are, thus, to “play with” various aspects, with the understanding that even if such a device were to exist (and it does not), it would have “lots of leakage” due to the massive amount of voltage passing through the gate. *Id.* at 939:5-8.

Returning to the current IPR, Petitioner's expert agreed that the transistor of FIG 1B would be problematic, testifying that if the cap layer were p-doped (as required for enhancement mode operation) and contacted both ohmic contacts, “it would be a disaster,” due to its conductivity because “[i]f you have a conducting layer in 1B, there would always be current flowing from source to – or electron flow or current from source to drain...” Ex. 2013 at 62:12-63:12; *see also id.* at 65:3-5 (noting that p-doping the cap layer “is the primary difference between a depletion and enhancement mode device.”) Petitioner's expert further testified that it was not possible to fabricate a device in which the cap layer abutted both ohmic

contacts, stating: “I just don’t know how you build something like that.” *Id.* at 57:8-12.

Given Petitioner’s expert’s own acknowledgement that FIG. 1B (and FIG. 2A) have common characteristics that render them non-functional and impossible to fabricate as enhancement mode devices, *Smith* cannot form the basis for an anticipatory reference for claims 1-3 of the ’294 patent, as a matter of law.¹ *See Tech. Consumer Prod., Inc. v. Lighting Sci. Grp. Corp.*, 955 F.3d 16, 23 (Fed. Cir. 2020) (“To anticipate, the reference must also enable one of skill in the art to make and use the claimed invention.”) (citations omitted). Moreover, with respect to obviousness, the sworn testimony of Petitioner’s expert in the ITC proceeding, that applying a lot of voltage to a transistor similar to Smith’s Fig. 1B (in relevant regards) would result in a transistor that “may not be an ideal device” with “lots of leakage” evidences that a POSA would not be motivated to modify Smith to be an operational enhancement transistor; *see also* Ex. 2009 at ¶ [120-124].

B. Smith does not disclose the “compensated GaN layer” of claims 1-3.

¹ Petitioner argues that *Smith* alone discloses the claimed “compensated GaN layer,” because “as-grown GaN films are naturally hydrogen passivated” and therefore “a POSITA would have recognized that *Smith*’s cap layer has passivated impurities.” Petition at 39-40. In this regard, Petitioner is applying *Smith* as an anticipatory reference.

Petitioner asserts that the cap layer 34 shown in Figure 2A may be a GaN layer or a GaAlN layer (which is correct) and that **doped region 40** may be doped with p-type dopant, e.g., Mg (also correct). However, Petitioner asserts (incorrectly) that **the cap layer 34**, in the embodiment of Figure 2A, is a compensated layer because “by 2009 it was well-known that hydrogen would be naturally present in such layers,” and “[i]t was known that hydrogen would be present even in as-grown GaN materials, forming acceptor-H neutral complexes that passivate the impurity.” Petition, p. 42. “And because it was well-known that as-grown GaN films are naturally hydrogen passivated, ... *Smith’s* cap layer 34 has passivated impurities.” Petition, p. 39.

1. The mere presence of hydrogen does not result in a compensated GaN layer

Petitioner’s assertion that as-grown GaN is compensated is based on a false premise—that the presence of hydrogen in p-GaN is determinative of compensation. This assertion contravenes both the ’294 patent and the knowledge of a POSA. Ex. 2009 at ¶ [126]. Nowhere does the ’294 patent state that the mere presence of hydrogen is sufficient for the formation of a compensated GaN layer in its transistor. Indeed, for the p-GaN below the gate contact to be considered compensated, according to the ’294 patent, it must be rendered semi-insulating, or non-conductive. Ex. 1001 at 3:47-48; Ex. 2009 at ¶ [126]; Ex. 2012 at 19:19-20:2; Ex. 2010 at 19 (stating: “Compensated GaN Is at Least Nonconductive or Semi-

Insulating.”). Moreover, the hydrogen present in the p-type GaN would need to be established as in fact canceling the electrical effect of the p-type dopants present in the layer (e.g., passivating the p-type dopants), in order for the p-GaN to be considered compensated. The mere presence of hydrogen is not enough, and the mere fact that a layer is something less than conductive is not enough. Ex. 2009 at ¶ [126].

Petitioner also asserts that hydrogen is present at “relatively high concentrations” in as-grown GaN. Petition at 42. To the extent that Petitioner attempts to argue that hydrogen passivation of p-GaN, in general, was known, that argument was already considered during prosecution of the ’294 patent, and the evidence presented by Petitioner is cumulative to *Bowers*, which was examined for precisely that proposition. Ex. 1002 at 114. Ex. 2009 at ¶ [127].

A close reading reveals that Petitioner is playing rhetorical games, trying to equate as-grown GaN with the as-grown **p-GaN** that is necessary for the ’294 claims. In order to be “compensated,” as required by claim 1, the GaN must be first p-doped. Ex. 2009 at ¶ [128]. Indeed, n-doping of GaN (the only other option) is not disclosed in the ’294 patent because its compensation would not result in a functional enhancement mode transistor. *Id.*

2. Conventional manufacture of p-GaN includes a hydrogen anneal

Even if hydrogen was present during epitaxial growth in the particular “conventional growth technique” chosen by a skilled person seeking to produce a device according to *Smith*’s teachings, that skilled person, following conventional wisdom (U.S. Patent No. 6,498,111 (“the ‘111 patent”, Ex. 2005)) would likely have included an anneal/activation step to remove hydrogen (Ex. 2005, lines 13-28) as was conventional (see Ex. 2005, col. 2, lines 13-17); Ex. 2009 at ¶ [129].

The ‘111 patent, which *Smith* incorporates by reference in ¶ [0083], indicates that there are processes which remove hydrogen prior to cool down. Ex. 2005 at 2:1-3. Notably, Petitioner failed to invalidate identical claims in the Chinese counterpart to the ’294 patent using the same argument it tries here. Ex. 2019. In that proceeding, CNIPA rejected Petitioner’s argument that *Smith* inherently has a compensated GaN layer, finding that “[e]ven if the manufacturing process contains hydrogen, the prior art always explicitly teaches to reverse this undesired passivation through annealing/activation or other means.” *Id.* at 7.

Smith provides little detail regarding the formation of the cap layer. *Smith* discloses in ¶ [0077]: “The cap layer 24, 24’ may be blanket formed on the barrier layer 22 and may be epitaxially grown and/or formed by deposition.” Petitioner makes no argument that, if the cap layer is formed by deposition rather than epitaxial growth, hydrogen would be incorporated in the cap layer. With respect to an epitaxial growth process, *Smith* discloses in ¶ [0064]: “The cap layer 24, 24’

may be provided by conventional epitaxial growth techniques where a higher Al concentration is provided during termination of growth of the cap layer 24, 24'. Thus, for example, the cap layer 24, 24' may be provided by MOCVD growth with an increase in the Al source just prior to and during termination of growth." However, importantly, there is no indication in *Smith* that the "conventional epitaxial growth techniques" that *Smith* references are carried out in the presence of hydrogen. Ex. 2009 at ¶ [131].

Importantly, even if hydrogen was present during epitaxial growth in the particular "conventional growth technique" chosen by a skilled person seeking to produce a device according to *Smith*'s teachings, that skilled person, following conventional wisdom (as set forth in the '111 patent (Ex. 2005)) would have included an anneal/activation step to remove hydrogen (Ex. 2005, col. 2, lines 13-28) as was conventional (see Ex. 2005, col. 2, lines 13-17); Ex. 2009 at ¶ [132].

3. Petitioner's reference to "passivation" relates to a separate passivation layer unrelated to the cap layer or doped region

Petitioner's reliance on a reference to "passivation" in ¶ [0083] of *Smith*, is misplaced. That paragraph refers to "[a] conventional passivation layer or a BN passivation layer..." Ex. 1005. This layer is compositionally different from the cap layer and is **not** a part of the cap layer. Ex. 2009 at ¶ [133]; Ex. 1012 at 38:20-41:15. As explained in ¶ [0090], the "BN passivation layer", illustrated with respect to FIGs. 3A and 3B, is a distinct structure that "is provided on exposed

surfaces of the device,” **above** the cap layer. Furthermore, the passivation layers described do not involve hydrogen-passivated p-GaN. ¶ [133].

Rather, the passivation layer is “graphitic and/or amorphous...and may be incorporated with layers of other materials, such as SiN or SiO_x.” Ex. 1005 at ¶ [0090]. Even ¶ [0083], on which Petitioner relies, refers only to BN, SiN, or MgN passivation layers, rather than GaN. *Id.* at ¶ [0083]. A POSA would therefore understand that any reference to annealing in ¶ [0083] does not relate to the cap layer or even GaN in general, but rather to these functionally and structurally different passivation layers that are added to the *Smith* devices. Ex. 2009 at ¶ [134]. In fact, ¶ [0090] of *Smith* explains that a MISHEMT, a HEMT having insulating gate material, cannot be formed without the addition of the passivation layers above the cap layer. Thus, because *Smith* teaches that a separate insulating, passivated layer is necessary for forming a MISHEMT, it follows that the cap layer alone is not enough to form a MISHEMT, meaning the cap layer is not inherently passivated. Ex. 2009 at ¶ [134].

Petitioner’s reliance on a reference to “passivation” in ¶ [0083] of *Smith* also failed to invalidate identical claims in the Chinese counterpart to the ’294 patent. Ex. 2019. In that proceeding, the CNIPA rejected Petitioner’s argument, finding *Smith*’s reference to annealing to be directed to the passivation layers, stating that “it does not disclose passivation of the doped region 40, and the cap layer 34,

which is part of the doped region 40, is not passivated.” *Id.* at 10. Ex. 2009 at ¶ [135].

The Board, in its institution decision, makes a similar mistake as Petitioner in relying on ¶ [0083]. Specifically, the Board noted that the optional annealing step disclosed in ¶ [0083] suggests that Smith’s epitaxial growth techniques would result in the presence of hydrogen in the GaN layer. Paper 11 at 18. But similar to the reasoning used by the CNIPA in rejecting Petitioner’s challenge of the claims based on *Smith*, the hydrogen removal disclosed in ¶ [0083] is not directed to the cap layer 34. Rather, it is directed to the passivation layer (“an anneal of the structure including the passivation layer may be carried out...to remove hydrogen from the layer...”). Ex. 1005 ¶ [0083]. A fair reading of this passage shows that hydrogen may be present in the passivation layer. There is no indication that hydrogen is present in the cap layer. A finding that hydrogen is necessarily present is improper. Ex. 2009 at ¶ [136].

4. There is no motivation to compensate or passivate *Smith*’s cap layer

Petitioner also posits that a POSA would have been motivated to passivate *Smith*’s cap layer to result in the claimed “compensated GaN layer.”

Specifically, at pages 26-27 of the Petition, Petitioner asserts:

A POSITA would have been motivated to adjust *Smith*’s doping by using hydrogen passivation because *Smith* recognizes level of doping as a result-effective variable controlling transistor characteristics, and a POSITA would have known that

hydrogen passivation adjusted the doping level. *Smith* discloses that the level of doping in cap layers is a result-effective variable to control leakage, explaining that “[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths.”

Petitioner confuses the “level of doping” with the level of compensation of dopants. Adjusting the level of doping is different from compensating or passivating. Ex. 2009 at ¶ [139]. In fact, *Smith* discloses that the level of doping is what affects leakage current, identifying n-type, p-type, and deep level dopants as all having an equal impact. Ex. 1005 at ¶¶ [0086], [0087], [0089]. Indeed, if Petitioner were correct that hydrogen passivation affected the level of doping, then compensating the cap layer could not result in a “sufficiently high” enough level of doping to reduce leakage current. Ex. 2009 at ¶ [139]. ¶

Simply adjusting the doping levels does not impart the same effects as passivation. *Id.* at ¶ [140]. Further, passivating a doped GaN layer does not affect the level of doping of that GaN layer. *Id.* Rather, passivation with hydrogen affects to what extent the dopants in a p-GaN layer are compensated, not the level of doping (which is based on the concentration of dopants in the layer). *Id.* Passivation is therefore independent of the level of doping and may cause unexpected, counterintuitive results such as those that precipitated the invention disclosed in the ’294 patent. *Id.* As such, passivation is not a result-effective variable and Petitioner has presented no evidence demonstrating that fact.

Accordingly, absent hindsight, a POSA would not have looked to hydrogen passivation as a way to alter *Smith*'s level of doping.

Smith discloses active, rather than compensated, p-type dopants: "P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and or minimize trapping effects." Ex. 1005 at ¶ [0072]. It further provides concentration ranges for that doping: "With p-type dopants, the doped region 40 may provide a dopant concentration of from about 10^{16} to about 10^{22} cm⁻³." *Id.* at ¶ [0087]. Notably, though hydrogen passivation of GaN, in general, was known at the time of its disclosure – a fact conceded by Petitioner, *Smith* does not describe any such inactivation of the p-type dopants in doped region 40, or elsewhere. A POSA would readily understand that *Smith*'s decision to exclude any mention of compensation/passivation of p-type dopants is thus a deliberate choice. Ex. 2009 at ¶ [141]; Ex. 1020. Indeed, it is consistent with conventional knowledge at the time, which taught away from compensating p-type dopants below the gate contact and **is specifically highlighted by *Smith***. Ex. 2005 at 2:1-3 (U.S. Patent No. 6,498,111 ("the '111 patent")), incorporated by reference in *Smith* ¶ [0083]. Given *Smith*'s teaching requiring active p-type dopants in region 40, a POSA would not contemplate doing the opposite and inactivating the very dopants that *Smith* requires for its devices. Ex. 2009 at ¶ [141].

Indeed, the above quoted passage at ¶ [0087] of *Smith* regarding the “level of doping” states that it “should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths.” The same paragraph indicates that “P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents.” Thus, in ¶ [0087], *Smith* makes it clear that the dopants themselves cause desirable effects, including reducing leakage currents. Compensating those dopants would cancel the electrical characteristics causing those desirable effects. A POSA would not be motivated to do that. Ex. 2009 at ¶ [142]. The Board used similar rationale to question the combination of Smith and Kigami in the institution decision (“[w]e question whether Petitioner adequately explains why one of ordinary skill in the art would have used Kigami’s methods to produce a cap layer with the opposite dopant configuration than desired in Smith.”) Paper 11 at 24.

In summary, the portions of *Smith* relied upon in the Petition relate to methods for achieving a desired level of **doping** in a semiconductor material, not a desired level of passivation/compensation of the dopants. Compensating *Smith*’s doped layer 40 (or 34) would negate the effects of the doping of that layer. Ex. 2009 at ¶ [143]. *Smith* would not dope layer 40 (or 34) only to subsequently compensate the

doping. *Id.* Doing so would be completely counterintuitive and runs completely counter to *Smith*'s stated intentions. *Id.* *Smith*'s disclosure thus goes in **the exact opposite** direction of the compensated gate of the '294 patent.

C. Smith does not disclose the “semi-insulating III-N layer” of independent claim 7

At page 46 of the Petition, Petitioner asserts that “*Smith* discloses that cap layer can be a ‘semi-insulating III-N layer.’” Specifically, on page 47 of the Petition, Petitioner incorrectly refers to Figure 2A of *Smith* as disclosing “*Smith*'s **semi-insulating cap layer 34** above barrier layer 22.” [Emphasis in original.]

In fact, *Smith* never states or even remotely implies that the cap layer 34 is “semi-insulating.” Petitioner effectively concedes that the term “semi-insulating” is actually not associated with *Smith*'s cap layer, but rather comes from *Smith*'s incorporation by reference of *Saxler874* (Ex. 1016). Petition at 46.

Petitioner's argument appears to focus on *Smith*'s disclosure in ¶ [0085] that, “[i]n further embodiments of the present invention, the doped region 40 is doped with a deep level dopant” and that “in some embodiments, doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34.” Invoking *Smith*'s subsequent incorporation by reference of *Saxler874*, Petitioner combines these disclosures in *Smith* with the disclosure in *Saxler874* “that co-doping “provide[s] semi-insulating

Group III nitride layers.” Ex. 1016 at ¶ [0005]. But there is a fundamental flaw in Petitioner’s argument. Ex. 2009 at ¶ [146].

The portion of *Saxler874* on which the Petitioner relies does not state or suggest that *any* type of co-doping results in a semi-insulating Group III nitride layer, as Petitioner implies. Ex. 2009 at ¶ [147]. Rather, in ¶ [0005], *Saxler874* discloses: “Embodiments of the present invention provide semi-insulating Group III nitride semiconductor layers and methods of fabricating semi-insulating Group III nitride layers. In certain embodiments of the present invention, fabrication of a semi-insulating Group III nitride layer includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.” To the extent this disclosure teaches creating a semi-insulating layer using co-doping, a POSA would understand this disclosure to mean that co-doping a shallow level p-type dopant and a deep level dopant is what would result in the semi-insulating layer. Ex. 2009 at ¶ [147].

Conversely, in the context of paragraph [0085], where *Smith* incorporates *Saxler874* by reference, *Smith* at most teaches regions of different dopant concentrations (“In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34”). Ex. 2009 at ¶ [148]. There is no suggestion in *Smith* that region 40, if p-doped, should be co-doped with a deep level dopant.

And Petitioner has provided no motivation as to why a POSA would use that type of co-doping in Smith. *Id.* Accordingly, Petitioner has not established that *Smith* discloses or renders obvious a “**semi-insulating III-N layer above the barrier layer**” as recited in independent claim 7. *Id.*

Therefore, for at least the reasons discussed above, the Board should find claims 1-3 and 7-9 not unpatentable over *Smith*.

VII. GROUND 1B: CLAIMS 1-3 AND 7-9 ARE NOT UNPATENTABLE OVER SMITH IN VIEW OF KIGAMI

In Ground 1B, Petitioner asserts that *Smith* in view of *Kigami* renders obvious the “compensated GaN layer” recited in independent claim 1. Petition, p. 24-31. As explained above, Petitioner misinterprets and misrepresents the teachings of *Smith* with regard to the claimed features recited in independent claim 1. As explained below, *Kigami* does not rectify the deficiencies of *Smith*.

A. Kigami does not rectify the deficiencies of Smith with respect to the “compensated GaN layer” of independent claim 1.

At page 28 of the Petition, Petitioner asserts that a “POSA would have been motivated to apply *Kigami*’s hydrogenation processing step(s) to passivate impurities in *Smith*’s cap layers.” Petitioner also contends that the motivation for modifying *Smith* is provided in *Kigami*: “A POSITA would have been motivated to use *Kigami*’s hydrogen incorporation techniques to form a region with passivated impurities in *Smith*’s cap layer.” *Id.* Patent Owner disagrees.

In *Kigami*, hydrogen is present in the local region 34, within semiconductor layer 32, and purportedly “forms a composite” with the magnesium in the local region 34. Ex. 1008 at [0022]. The semiconductor layer 32 is formed directly on the substrate 22. That semiconductor layer corresponds to a buffer and/or a transition layer with regard to claims 1-3, not a compensated GaN layer. A gate-insulating film 52 is formed *above* the local region 34 of the semiconductor layer 32, and a gate electrode is formed above that gate-insulating film 52. *Id.* at ¶ [0020]. Ex. 2009 at ¶ [152].

Kigami thus discloses a different device from the device recited in claim 1 of the '294 patent and is cumulative to *Bowers*, which was considered for its discussion of passivation by hydrogen in GaN material during prosecution of the '294 patent. Ex. 1002 at 87-88; Ex. 1020. Ex. 2009 at ¶ [153].

Kigami uses an entirely different layer as the “gate insulating film” below the gate contact and incorporates a fully-activated p-type GaN layer and a GaN layer with magnesium and hydrogen to form the channel. Ex. 2009 at ¶ [154]; Ex. 2012 at 21:4-23:20. Nothing in *Kigami* discloses or suggests that its hydrogen-treated p-type GaN layer would be suitable below the gate contact or that a compensated GaN layer including Mg dopants and hydrogen would be acceptable or functional in place of the cap layer 34 of *Smith*. Ex. 2009 at ¶ [154]. A POSA would therefore not seek to combine the teachings of *Smith* with *Kigami*, to “apply

Kigami's hydrogenation techniques to *Smith*'s cap layer 34," absent impermissible hindsight. *Id.*

Furthermore, there is no motivation to combine *Smith* with *Kigami* because a POSA would find the doping of a gate semiconductor followed by the cancellation of the effects of the dopant to be highly counterintuitive. *Id.* at ¶ [155]. *Smith* makes clear the purpose of the dopants it utilizes: "The dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations." *Smith* at ¶ [0064]. As explained above, this doping is intended to reduce leakage current along the dislocations. Ex. 2009 at ¶ [155]. Passivating those dopants would void their purpose in *Smith*, rendering the *Smith* device inoperable for its stated purpose. *Id.* The Board used similar rationale to question the combination of *Smith* and *Kigami* in the institution decision ("[w]e question whether Petitioner adequately explains why one of ordinary skill in the art would have used *Kigami*'s methods to produce a cap layer with the opposite dopant configuration than desired in *Smith*.") Paper 11 at 24.

Smith in view of *Kigami* therefore does not render obvious the claimed "compensated GaN layer," under either party's construction. Ex. 2009 at ¶ [156]

B. Kigami does not rectify the deficiencies of Smith with respect to the "semi-insulating III-N layer" of independent claim 7.

Petitioner does not contend that *Kigami* is relevant or combinable with *Smith* with respect to the “semi-insulating III-N layer” of independent claim 7. Pet. at pp. 46-47, 49-50 and 56. Ex. 2009 at ¶ [157].

Therefore, for at least the reasons discussed above, the Board should find claims 7-9 not unpatentable over *Smith* in view of *Kigami*. Ex. 2009 at ¶ [158].

VIII. GROUND 1C: CLAIMS 1-3 AND 7-9 ARE NOT UNPATENTABLE OVER SMITH IN VIEW OF UEMOTO

In Ground 1C, Petitioner asserts that *Smith* in view of *Uemoto* renders obvious the “compensated GaN layer” recited in independent claim 1. *Uemoto*, however, does not rectify the deficiencies of *Smith* in this regard. Ex. 2009 at ¶ [159].

A. There is no motivation to combine Smith and Uemoto in the manner proposed by Petitioner

At page 31 of the Petition, Petitioner asserts that a “POSITA would have been motivated to apply *Uemoto*’s hydrogen diffusion technique to selectively increase the resistivity of *Smith*’s cap layers.” More specifically, Petitioner asserts that a POSA would have been motivated to use *Uemoto*’s “hydrogen diffusion film 17” in *Smith* to form the “high resistive region 15b,” “to similarly inactivate impurities in *Smith*’s cap layer, generate the highly resistive regions, and reduce leakage.” Ex. 2009 at ¶ [160].

Indeed, a POSA would find no reason, absent hindsight, to deactivate the very p-type dopants that *Smith* teaches are a part of its purported invention. Ex. 2009 at ¶ [161].

Moreover, *Smith* discloses that the level of doping “should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths.” Ex. 1005 at ¶ [87]. The same paragraph indicates that “P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents.” Thus, in paragraph [0087], *Smith* makes it clear that the dopants themselves cause desirable effects, including reducing leakage currents. Compensating those dopants by combining *Smith* with *Uemoto* would cancel the electrical characteristics causing those desirable effects. Ex. 2009 at ¶ [162]. A POSA would not be motivated to do that. *Id.* The Board used similar rationale to question the combination of *Smith* and *Kigami* in the institution decision (“[w]e question whether Petitioner adequately explains why one of ordinary skill in the art would have used *Kigami*’s methods to produce a cap layer with the opposite dopant configuration than desired in *Smith*.”) Paper 11 at 24.

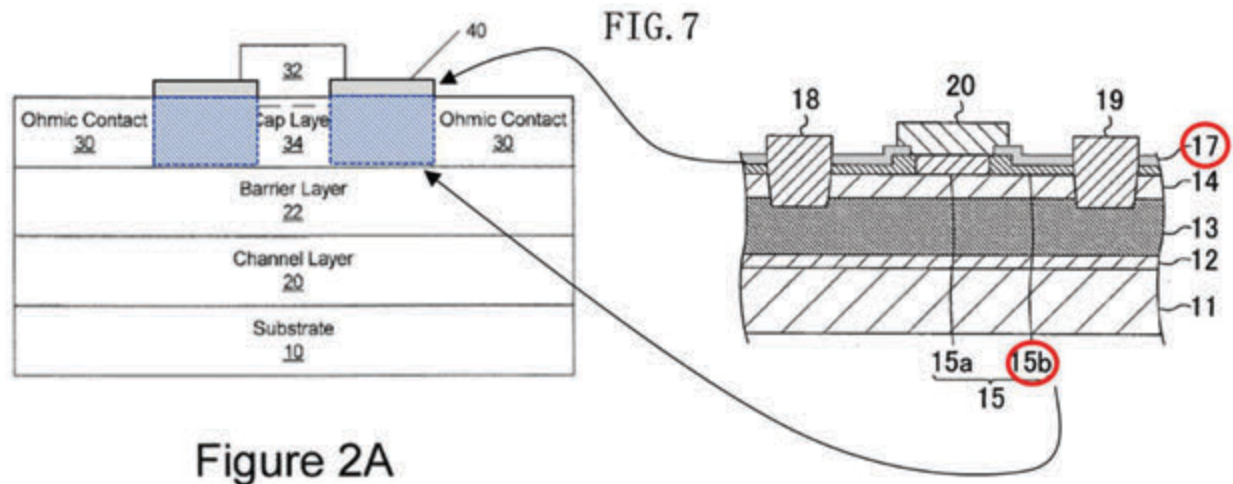
A POSA also cannot rely upon *Uemoto*'s disclosure because it directly contradicts the teaching of the '294 patent, stating that the **2DEG is present under resistive region 15b**: "In the region other than the control region, as shown in FIG. 2B, at the heterointerface the conduction band is located at a lower level than the Fermi level, and thus 2DEG is created." Ex. 1006 at ¶ [0038]; Ex. 2009 at ¶ [163]. That is the exact opposite of what is disclosed in the '294 patent, that the non-conductive (resistive) compensated GaN layer **depletes the 2DEG** at zero voltage. Ex. 1001 at 3:16-17; Ex. 2009 at ¶ [163]. Thus, having reviewed *Uemoto*, a POSA would not be motivated to compensate p-type GaN below the gate metal because, according to *Uemoto*, that would not result in the depletion of the 2DEG below it at zero voltage, preventing the formation of an enhancement mode device, as disclosed by the '294 patent. Ex. 2009 at ¶ [163].

Smith in view of *Uemoto* therefore does not render obvious the claimed "compensated GaN layer," under either party's construction.

B. Petitioner's proposed combination of Smith and Uemoto do not disclose "a gate contact above the compensated GaN layer," as properly construed

Petitioner's arguments for combining *Uemoto* with *Smith* are premised on a misguided understanding of their respective disclosures. As shown below, Petitioner attempts to remedy the deficiencies by artificially inserting *Uemoto*'s

hydrogen diffusion film into FIG. 2A of *Smith* to increase the resistivity of a portion of its cap layer. Petition at 31.



Petition at 31

But Petitioner’s proposed resulting transistor does not disclose “a gate contact above the compensated GaN layer,” as properly construed. That is, Petitioner’s proposed transistor does not have a gate contact and compensated GaN layer that are part of the same gate structure. For example, as can be seen in the figure above, the blue portions of Petitioner’s modified FIG. 2A correspond to the alleged compensated GAN layer. That layer is not part of the gate structure and does not reduce gate capacitance, a critical goal of the ‘294 patent. Ex. 2009 at ¶ [166].

C. Uemoto does not rectify the deficiencies of Smith with respect to the “semi-insulating III-N layer” of independent claim 7.

Petitioner does not contend that *Uemoto* is relevant or combinable with *Smith* with respect to the “semi-insulating III-N layer” of independent claim 7. Pet. at 46-47, 49-50 and 56.

Therefore, for at least the reasons discussed above, the Board should find claim 7 not unpatentable over *Smith* in view of *Uemoto*. Ex. 2009 at ¶ [168].

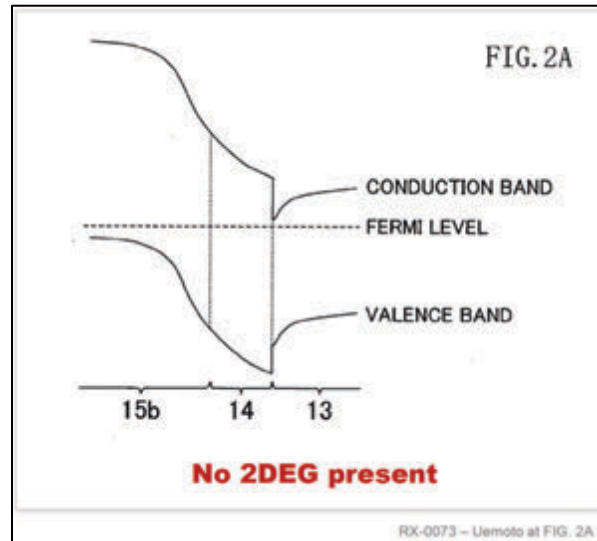
IX. GROUND 2: CLAIMS 1-3 AND 7-9 ARE NOT UNPATENTABLE OVER UEMOTO IN VIEW OF SMITH

In Ground 2, Petitioner reverses the order of the prior art as compared to Ground 1C, and asserts that *Uemoto* in view of *Smith* meets independent claims 1, 4, 7 and 10 of the ‘294 patent. Petition, p. 61-67. As explained below, Petitioner misrepresents the teachings of *Uemoto* with respect to the “compensated GaN layer” of claim 1, and the “semi-insulating III-N layer” of independent claim 7. Ex. 2009 at ¶ [269].

A. The claimed compensated GaN layer has no 2DEG beneath it, but region 15b does

Uemoto is directed to an enhancement-mode transistor that has an activated p-type GaN, region 15a, below the gate electrode. Ex. 1006, ¶¶ [0003], [0033], [0048], [0049]. The 2DEG under this activated p-GaN is depleted at zero voltage. *Id.* On either side of the gate structure, a p-doped high resistive region 15b is present. *Id.* As shown in the energy band diagrams below, *Uemoto* specifically

notes that the 2DEG is depleted under the activated region 15a but is **not** depleted under the high resistive region 15b. Ex. 2009 at ¶ [170].

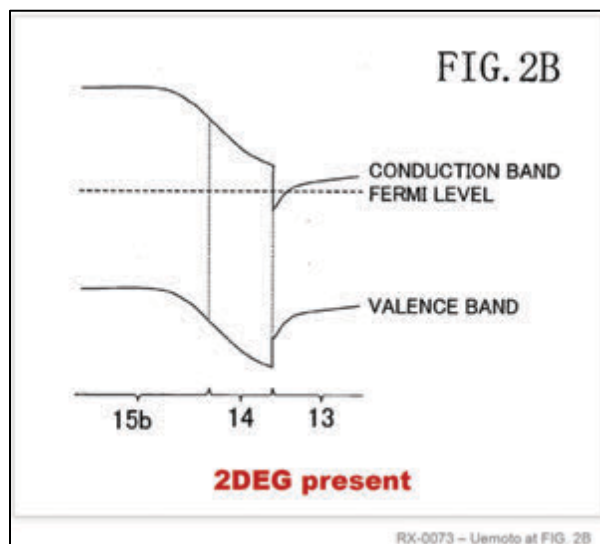


***Uemoto* at FIG. 2A (annotated)**

As shown in the energy band diagram above, the conduction band at activated region 15a (erroneously referred to in *Uemoto* as “15b” in FIG. 2A), which is a part of the gate structure and below the gate electrode, is above the Fermi level. Ex. 2016 at 960:25-961:19 (Schubert). Ex. 2017 at 1031:9-1032:9 (establishing that all parties agree “15b” in FIG. 2A is a typo and should be “15a”). This means that the 2DEG is depleted below activated region 15a. Id. Ex. 2009 at ¶ [171].

By contrast, as shown in Figure 2B of *Uemoto* below, the Fermi level of high resistive region 15b, which Petitioner alleges corresponds to the compensated GaN layer of claim 1, is in the conduction band. Ex. 2016 at 961:22-962:21. This means that the 2DEG is **present and not depleted** under high resistive region 15b,

a point that is not disputed by the parties. *Id.* at 933:10-15 (Lebby). Ex. 2009 at ¶ [172].



***Uemoto* at FIG. 2B (annotated)**

The parties do not dispute that the 2DEG must be depleted under the compensated GaN layer of the '294 Patent's transistor for it to operate as described. Ex. 2015 at 442:17-443:18 (Schubert); *accord* Ex. 2016 at 934:2-3 (Lebby) ("In an enhancement-mode device at 0 volts there will not be a 2DEG underneath the gate"). By contrast, as Patent Owner's expert explained in the ITC proceeding with regard to *Uemoto*: "So if we choose region 15B – 15B as Dr. Lebby proposes, and if we go by the teachings of the prior art, we do not create an enhancement-mode transistor. We do not remove the 2DEG." Ex. 2016 at 962:9-12 (Schubert). Thus, because the 2DEG is present under *Uemoto*'s high resistive region 15b, it cannot correspond to the compensated GaN layer of claim 1. *Id.* at 962:7-21. Ex. 2009 at ¶ [173].

Notably, in a parallel invalidation request to the Chinese Patent Office relating to the Chinese counterpart of the '294 patent proceeding, Petitioner relied upon the p-doped conductive region 15a, not high resistive region 15b, as purportedly disclosing the “compensated GaN layer.” *See* Ex. 2018 at 33-35. That inconsistency demonstrates that Petitioner itself recognizes that it is unreasonable to identify region 15b as meeting the “compensated GaN layer” of independent claim 1, because region 15b is not under the gate electrode 20, as required by claim 1 of the '294 patent. Indeed, CNIPA recognized Petitioner’s untenable position, finding the claim valid because “the control region 15a is conductive and cannot be equivalent to the ‘compensated GaN layer’ in claim 1.” Ex. 2019 at 11. Ex. 2009 at ¶ [174].

Furthermore, *Uemoto* does not disclose the elements of claims 2 or 3. Claim 2 recites “the acceptor type dopant atoms are passivated by hydrogen,” while claim 3, depending from claim 2, recites “the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.” Ex. 1001 at 5:18-23. As explained above, claims 2 and 3 are directed to an enhancement-mode transistor. *See supra* Section III.A.2.ii.a. Petitioner does not dispute that only p-type dopants, such as Mg, Zn, Be and Ca, can be passivated by hydrogen. Ex. 2016 at 955:5-12 (Schubert) (“It is only the p-type dopants that are passivated by hydrogen”). *See supra* Section III.A.2.ii.a. Furthermore, the parties’ testimony in the ITC

proceeding demonstrates that enhancement-mode operation requires the use of p-type dopants. Ex. 2017 at 997:10-998:1 (Schubert); Ex. 2016 at 936:17-937:2 (Lebby). Petitioner's expert in the ITC proceeding, Dr. Lebby, confirms that the use of a p-type dopant (magnesium) passivated with hydrogen in GaN would result in an enhancement-mode device. Ex. 2016 at 923:6-17 (Lebby). Petitioner also admitted in its post-hearing brief that a transistor with p-type doping "passivated with hydrogen *would* function as an enhancement mode device." Ex. 2010 at 41 (emphasis added). Accordingly, Petitioner and its expert agree that p-type doped GaN passivated by hydrogen *causes* a transistor to be an enhancement-mode transistor. Because, as the parties agree, an enhancement-mode transistor is normally OFF due to a depleted 2DEG at zero voltage, it follows that the enhancement-mode transistor recited by claims 2 and 3 has no 2DEG below the hydrogen-passivated p-GaN at zero voltage. Ex. 2015 at 442:17-443:18 (Schubert); *accord* Ex. 2016 at 934:2-3 (Lebby) ("In an enhancement-mode device at 0 volts there will not be a 2DEG underneath the gate"). Ex. 2009 at ¶ [175].

By contrast, *Uemoto's* high resistive region 15b has an intact 2DEG below it. *Uemoto* at Fig. 2B, [0038]. That 2DEG prevents high resistive region 15b from creating an enhancement-mode transistor, as required by claims 2 and 3. *Cf.* Ex. 2016 at 934:2-3 (Lebby) ("In an enhancement-mode device at 0 volts there will not be a 2DEG underneath the gate"). As a result, the high resistive region 15b cannot

correspond to the hydrogen-passivated p-GaN recited in claims 2 and 3, because it is unable to deplete the 2DEG at zero voltage and create an enhancement-mode transistor. *Id.* Ex. 2009 at ¶ [176].

Lastly, even assuming, *arguendo*, that the 2DEG is depleted under high resistive region 15b, the lack of 2DEG under that region would mean that the *entire* 2DEG between the source and the drain of *Uemoto* is removed. And that cannot be the case, as explained with regard to *Smith* above, because depletion of the 2DEG from source to drain results in a non-functional enhancement-mode transistor, as the 2DEG cannot be reconstituted by application of a gate voltage to turn the device ON. *See supra* Section III.A.2.i.c. Ex. 2009 at ¶ [177].

Uemoto in view of *Smith*² therefore does not render obvious the claimed “compensated GaN layer,” under either party’s construction. Ex. 2009 at ¶ [178].

B. Uemoto’s gate electrode is not located above the alleged compensated GaN layer

Uemoto, which Petitioner argues discloses the disputed features of claims 1-3, in fact is akin to the admitted prior art, activated p-GaN transistors discussed in Figure 1 of the ’294 Patent. As described in *Uemoto*, the third nitride semiconductor layer 15 has a region 15a that is activated with conductive, negatively charged Mg acceptors and holes, and element 15b, which is a resistive p-doped AlGaIn/GaN

² Petitioner does not rely on *Smith* to provide an alleged teaching of “compensated GaN layer” in Ground 2.

region. Ex. 2016 at 959:25-960:23 (Schubert); Ex. 1006 at ¶¶ [0033], [0048]-[0049], [0066]. It is this activated region 15a that is below the gate electrode and part of the gate structure. Ex. 2016 at 959:25-960:23 (Schubert); Ex. 1006 at FIG. 7. *Uemoto* reflects the conventional understanding prior to the '294 Patent, that passivation below the gate is unfavorable to the formation of an enhancement-mode transistor. Ex. 2014 at 102:14-105:16 (Lidow); Ex. 1001 at 1:55-2:2. Because it has an activated p-GaN layer below the gate, *Uemoto* “has the known problems of low turn on voltage and high gate leakage current.” Ex. 2016 at 960:16-19 (Schubert). *Uemoto* thus describes a device that is substantially similar to the prior art enhancement-mode device shown in Figure 1 of the '294 Patent (with non-compensated GaN below the gate), and thus does not disclose “a compensated GaN layer above the barrier layer,” as recited in claim 1 of the '294 Patent. *Id.* at 963:5-965:19; 968:1-6. Ex. 2009 at ¶ [179].

High resistive region 15b of *Uemoto* also cannot correspond to the compensated GaN layer, because the design of *Uemoto* precludes its device from providing both the reduced gate leakage current and reduced gate capacitance that the '294 Patent's transistor offers over the prior art. Ex. 2017 at 1011:7-15. Even if high resistive region 15b could reduce gate leakage, it still will not impact gate capacitance, because it is not a part of the gate structure. That failure extends to what Patent Owner's expert referred to as the “sliver” of region 15b that is shown in

Fig. 7 of *Uemoto* to be contacting a very small portion of gate electrode 20 (but not described in *Uemoto*'s specification that way). Ex. 2016 at 964:22-965:19, 968:1-6. Instead, it is activated region 15a that is below the gate contact (and part of the gate structure), and because that region is conductive, the transistor will continue to have the unfavorably high gate capacitance of the prior art devices. Tr. 968:1-6 (Schubert) (contrasting the conductive nature of region 15a under the gate electrode with the non-conductive, compensated GaN layer of the '294 Patent). Ex. 2009 at ¶ [180].

Uemoto further does not disclose "a compensated GaN layer," as recited in claim 1 of the '294 Patent because the p-doped high resistive layer 15b is not a part of the gate structure. Ex. 2017 at 1034:4-11 (Schubert). As Petitioner's expert explained at the ITC hearing, a POSA would not consider high resistive region 15b to be a part of the gate structure because it is not under the gate electrode and is not part of the control region that is used to obtain 2DEG depletion and the normally-OFF characteristics of the *Uemoto* device. *Id.* at 960:20-23, 963:5-964:16; Tr. 931:3-12 (Lebby); Ex. 1006 ¶ [0038]. Ex. 2009 at ¶ [181].

Moreover, a POSA cannot simply move the high resistive region 15b of *Uemoto* below the gate electrode without running counter to *Uemoto*'s stated objective of having a control region below the gate with a lower resistivity. Ex. 2016 at 960:20-23; 963:5-964:16 (Schubert). Indeed, *Uemoto*'s operation requires

that the conductive, activated region 15a be below the gate electrode, such that increasing its resistivity would reflect impermissible hindsight. *Id.* Ex. 2009 at ¶ [182].

There is no narrative disclosure in *Uemoto* of layer 15b being below the gate electrode. In this regard, *Uemoto* does not support Petitioner's contention. In addition, there is no pictorial support of a "layer" 15b being below the gate electrode. The sliver that Petitioner is referring to as being below the gate electrode is not a layer (as required by claim 1 of the '294 patent). Ex. 2009 at ¶ [183].

C. *Uemoto* in view of *Smith* does not disclose the “semi-insulating III-N layer” of independent claim 7.

At page 78 of the Petition, Petitioner concedes that *Uemoto* does not disclose layer 15 as being “semi-insulating.” Petitioner thus relies upon *Smith* for this teaching, referring to the arguments at VIII.G.6 (pp. 46-47) of the Petition.

Petitioner asserts that *Smith*'s cap layer 34 can be formed with “[t]echniques for co-doping Group III-nitride materials,” Ex. 1005 at ¶ [0085], and that *Saxler*⁸⁷⁴ (Ex. 1016), which *Smith* incorporates by reference, explains that co-doping “provide[s] semi-insulating Group III nitride semiconductor layers.” Ex. 1016, ¶ [0005]. Ex. 2009 at ¶ [185].

But, as explained above, there is a fundamental flaw in Petitioner's argument. *Smith* never states or even remotely implies that the cap layer 34 is

“semi-insulating.” Petitioner effectively concedes that the term “semi-insulating” is actually not associated with *Smith*’s cap layer, but rather comes from *Smith*’s incorporation by reference of *Saxler874*. Petition at 46. Ex. 2009 at ¶ [186].

Petitioner’s argument appears to focus on *Smith*’s disclosure in [0085] that, “[i]n further embodiments of the present invention, the doped region 40 is doped with a deep level dopant” and that “in some embodiments, doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34.” Invoking *Smith*’s subsequent incorporation by reference of *Saxler874*, Petitioner combines these disclosures in *Smith* with the disclosure in *Saxler874* “that co-doping “provide[s] semi-insulating Group III nitride layers.” Ex. 1016 at ¶ [0005]. But there is a fundamental flaw in Petitioner’s argument. Ex. 2009 at ¶ [187].

The portion of *Saxler874* on which the Petitioner relies does not state or suggest that *any* type of co-doping results in a semi-insulating Group III nitride layer, as Petitioner implies. Rather, in [0005], *Saxler874* discloses:

Embodiments of the present invention provide semi-insulating Group III nitride semiconductor layers and methods of fabricating semi-insulating Group III nitride layers. In certain embodiments of the present invention, fabrication of a semi-insulating Group III nitride layer includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.

To the extent this disclosure teaches creating a semi-insulating layer using co-doping, a POSA would understand this disclosure to mean that co-doping a

shallow level p-type dopant and a deep level dopant is what would result in the semi-insulating layer. Ex. 2009 at ¶ [189].

Conversely, in the context of ¶ [0085], where *Smith* incorporates *Saxler*⁸⁷⁴ by reference, *Smith* at most teaches regions of different dopant concentrations (“In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34”). There is no suggestion that a p-type dopant be co-doped with a deep level dopant. And Petitioner has provided no motivation as to why a POSA would use that type of co-doping in *Smith*. Ex. 2009 at ¶ [190].

Accordingly, for the reasons set forth above, *Smith* thus does not rectify the admitted deficiency of *Uemoto* with respect to a **“semi-insulating III-N layer above the barrier layer”** as recited in independent claim 7.

X. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

The compensated gate of the '294 patent was a breakthrough invention and resulted in the first commercially viable enhancement-mode GaN transistor. See Ex. 2009 at ¶192-193, and 197 (citing EX2021 (awarding Dr. Alex Lidow with the 2015 SEMI Award “for commercialization of GaN power devices”).

The implementation of a compensated gate material in enhancement mode GaN transistors provided a significant improvement over less efficient prior art enhancement mode devices by substantially reducing gate leakage and gate

capacitance over prior enhancement mode transistors with a conductive gate. *Id.* at ¶196-197. The invention of the '294 patent, particularly the compensated gate, also results in greater switching efficiency. *Id.* at ¶194. As a result, GaN transistors employing the patented compensated gate technology of the '294 patent are used in a wide variety of applications. *See, e.g.*, Ex. 2020 at 1.

Depletion mode GaN transistors were well known at the time of invention of the '294 patent, but they had significant drawbacks, most notably the undesirable “normally ON” mode of operation. Ex. 2009 at ¶195-196. While enhancement mode transistors were also known prior to the invention of the '294 patent, they were not commercially viable because the gate current during device operation, particularly in the ON state, was unacceptably high, leading to high gate leakage, poor performance, and inefficiency. *Id.* at ¶196. The '294 patent solved these drawbacks with its novel and counterintuitive use of a compensated gate material in the gate structure that reduced the capacitance between the gate and the barrier layer and enabled a positive gate voltage application to turn the transistor to its ON state, with low gate leakage. *Id.* at ¶196-197.

The innovative breakthrough of the compensated gate technology of the '294 patent was not an obvious modification of the prior art, but rather a technological leap that laid the foundation for viable enhancement-mode GaN

transistors that compete directly with, and surpass the performance of, silicon-based transistors. *See* EX2020 at 1.

XI. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and no claim should be found unpatentable.

Dated: June 12, 2024

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER's RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 13,549 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

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