UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY AND

INNOSCIENCE AMERICA, INC.,

Petitioner

v.

EFFICIENT POWER

CONVERSION CORPORATION,

Patent Owner

___

Case No. IPR2023-01384

U.S. Patent No.10,312,335

___

DECLARATION OF JAMES RICHARD SHEALY, PH.D.

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1. [1p] An enhancement-mode GaN transistor, comprising:.....55

2. [1a] a GaN layer;.....56

3. [1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 57

4. [1c]: a source contact and a drain contact formed on the barrier layer;.....58

5. [1d]: a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and.....59

6. [1e]: a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,.....66

7. [1f]: wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively. 69

C. [Claim 2]: wherein the pair of horizontal ledges of the p-type gate material are self-aligned. 72

D. [Claim 3]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN). 73

E. [Claim 4]: wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width 73

F. Independent Claim 5 73

1. [5p] An enhancement-mode GaN transistor, comprising: 74

2. [5a] a GaN layer; 74

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 74

4. [5c]: a source contact and a drain contact formed on the barrier layer; 74

5. [5d]: a p-type gate material formed above the barrier layer and between the source and drain contacts; 75

6. [5e]: a gate metal disposed on the p-type gate material, ...75

7. [5f]: wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and 75

8. [5g]: (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer. 76

G. [Claim 6]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN). 76

H. [Claim 7]: wherein the pair of self-aligned ledges are symmetric with respect to the gate metal. 77

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B. [Claim 2] The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned. 86

C. Independent Claim 5 87

1. [5p] An enhancement-mode GaN transistor, comprising: 88

2. [5a] a GaN layer; 88

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 88

4. [5c] a source contact and a drain contact disposed on the barrier layer; 88

5. [5d] a p-type gate material formed above the barrier layer and between the source and drain contacts; 88

6. [5e] and a gate metal disposed on the p-type gate material, ...88

7. [5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and 89

8. [5g] side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer. 89

D. [Claim 6] The enhancement-mode GaN transistor according to claim 5, wherein the barrier layer comprises aluminum gallium nitride (AlGaN). 90

E. [Claim 7] The enhancement-mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal. 90

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C. Independent Claim 1 95

1. [1p] An enhancement-mode GaN transistor, comprising: 95

2. [1a] a GaN layer; 95

3. [1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 96

4. [1c] source contact and a drain contact formed on the barrier layer; 97

5. [1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and

drain contact, respectively, and contacting the barrier layer; and 98

6. [1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material, ... 105

7. [1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively. 107

D. [Claim 2] The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned. 109

E. [Claim 3] The enhancement-mode GaN transistor according to claim 1, wherein the barrier layer comprises aluminum gallium nitride (AlGaN). 109

F. [Claim 4] The enhancement-mode GaN transistor according to claim 1, wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width. 109

G. Independent Claim 5 110

1. [5p] An enhancement-mode GaN transistor, comprising: 110

2. [5a] a GaN layer; 110

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 110

4. [5c] a source contact and a drain contact disposed on the barrier layer; 111

5. [5d] a p-type gate material formed above the barrier layer and between the source and drain contacts; 111

6. [5e] and a gate metal disposed on the p-type gate material, ... 111

7. [5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and 111

8. [5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer. 112

H. [Claim 6] The enhancement-mode GaN transistor according to claim 5, wherein the barrier layer comprises aluminum gallium nitride (AlGaN). 113

I. [Claim 7] The enhancement-mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal. 113

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A. Overview of Ground 6 114

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B. [Claim 2] The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned. 119

C. Independent Claim 5 121

1. [5p] An enhancement-mode GaN transistor, comprising: 121

2. [5a] a GaN layer; 121

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 121

4. [5c] a source contact and a drain contact disposed on the barrier layer; 122

5. [5d] a p-type gate material formed above the barrier layer and between the source and drain contacts; 122

6. [5e] and a gate metal disposed on the p-type gate material, ... 122

7. [5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and 122

8. [5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer. 123

D. [Claim 6] enhancement-mode GaN transistor according to claim 5, wherein the barrier layer comprises aluminum gallium nitride (AlGaN). 124

E. [Claim 7] The enhancement-mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal. 124

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I. INTRODUCTION

[001] I have been retained by Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively "Innoscience"), as an independent expert for the above-identified inter partes review proceeding involving U.S. Patent No. 10,312,335 ("the '335 patent").

[002] I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

[003] Although I am being compensated for my time in connection with this proceeding at my standard hourly consulting rate and reimbursed for reasonable out-of-pocket expenses, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

[004] I have been asked to provide my opinion whether the claims of the '335 patent would have been obvious to a person of ordinary skill in the art at the time of the earliest claimed priority date of the '335 patent. In performing my analysis, I have been asked to assume that the priority date is April 8, 2009. My opinions are set forth below.

[005] Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not

intended to suggest that they are the only support for the propositions for which they are cited.

II. SUMMARY OF OPINIONS

[006] This declaration analyses claims 1-7 of the ’335 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for my opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

[007] Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of April 8, 2009), it is my opinion that claims 1-7 of the ’335 patent would have been obvious based on the asserted grounds discussed below.

III. QUALIFICATIONS AND BACKGROUND

[008] I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A.

[009] I am competent to write this Declaration.

[010] I have been involved in the science and engineering of high-power compound semiconductor transistors for over 40 years. I have been deeply involved in the research and design of III-V compound semiconductor devices over

the course of my career. I have been a Professor at Cornell University, School of Electrical and Computer Engineering, and have been teaching and conducting research at Cornell since 1987. In 2022, I was granted emeritus status.

[011] I received a B.S. degree from North Carolina State University in 1978, a M.S. from Rensselaer Polytechnic Institute in 1980, and a Ph.D. from Cornell University in 1983. I joined the Cornell faculty in 1987. And I am currently a Full Professor at Cornell's School of Electrical and Computer Engineering.

[012] In 1978, I joined the technical staff of General Electric's Corporate Research and Development Center under an Edison Fellowship. While there, among other work, I developed GaAs epitaxial materials for high voltage electronics. I was the inventor of two patents on Vertical Field Effect Transistors.

[013] In 1980, I transferred to General Electric's Advanced Electronics Laboratory where I developed materials and processes for the fabrication of AlGaAs LEDs as well as developing an OMVPE reactor and related processes for the fabrication of AlGaAs quantum well laser diodes. In 1985, I was designated Principal Staff Scientist at General Electric in recognition of my research contributions.

[014] While at General Electric, I was also concurrently working at Cornell. In 1984, my group at Cornell developed the first single quantum well red laser by

Organometallic Vapor-Phase Epitaxy ("OMVPE"), a technique used for growing semiconductor crystals. The fabrication of these devices involved multi-level metallization and dielectric passivation.

[015] I joined the Cornell faculty in 1987 as a Professor of Electrical and Computer Engineering (ECE) and Materials Science and Engineering (MSE). While at Cornell I have continued my research in OMVPE, particularly as it relates to high frequency transistors, LEDs, and laser diodes. I have also researched GaN and related materials for both high-power transistors and LEDs.

[016] In 1997, I was named the Director of Cornell's Optoelectronics Technology Center. In 1998, I was promoted to full professor at Cornell. I have published over 120 articles and am the inventor of over 19 patents, many of which deal with GaN-based materials and devices. Over the years, I have received numerous teaching awards for delivering quality instruction to undergraduates in Materials Science and Electrical Engineering.

[017] In 1998-99, the research group that I led invented and patented a single temperature method for nucleation and growth of GaN materials on sapphire, SiC, and Si substrates. This technique has become the preferred method for growing GaN-based transistors and LED today. This nucleation method was used to grow AlN/GaN layers on silicon. By mid-1999, my research group had

produced a gallium nitride-on-silicon (GaN-Si) RF transistor, a technology currently used by several GaN companies for high efficiency power convertors and RF amplifiers.

[018] By the early 2000s, my research group produced the first RF integrated circuits with gallium nitride-on-silicon carbide (GaN on SiC) transistors including X Band VCOs, TR switches, frequency doublers, and internally matched power amplifiers. By 2008, my group discovered a new passivation technology (LPCVD of AlSiN, patented) for GaN-based FETs which, when applied to GaNSiC HEMTs, produced the largest power density operation (over 18 Watts/mm at 10 GHz) ever observed on submicron gated devices. These devices also delivered record power-added-efficiencies and linear gain during 10 GHz operation (PAE > 65 %, Gain > 36 dB at 60 V bias). These benchmarks remain unchallenged today.

[019] In 2015, I cofounded Akoustis Technology (AKTS on the NASDAQ), a company which manufactures AlN bulk acoustic wave filters which are required for 5G communications. In 2019, I cofounded Odyssey Semiconductor, a company which is developing GaN Vertical field effect transistors for the emerging power convertor market. Odyssey Semiconductor also recently developed the fabrication techniques and built micro-LED Arrays in both AlGaInP and AlGaInN materials.

[020] I have remained current in the field, as evidenced by my publications listed in my curriculum vitae.

[021] I have also served as an expert in certain legal proceedings relating to GaN transistors, including materials growth, device fabrication, and packaging. A list of cases in which I have testified at trial, hearing, or by deposition is provided in my curriculum vitae.

IV. MATERIALS CONSIDERED

[022] In forming my opinions, I read and considered the ’335 patent and its prosecution history, the exhibits listed in the Exhibit List filed with the petition for *inter partes* review of the ’335 patent, as well as any other materials referenced herein. I have reviewed the following at least the following documents:

Exhibit	Description
Ex. 1001	U.S. Patent No. 10,312,335 B2 to Cao et al. (“the ’335 patent”)
Ex. 1002	Prosecution History of the ’335 patent
Ex. 1005	Japanese Patent Publication No. JP H11-261053 to Yoshida
Ex. 1006	Certified Translation of Japanese Patent Publication No. JP H11-261053 to Yoshida (“*Yoshida*”)

Exhibit	Description
Ex. 1007	U.S. Patent Application Publication No. US 2006/0108606 A1 to Saxler et al. ("*Saxler*")
Ex. 1008	U.S. Patent Application Publication No. US 2007/0007547 A1 to Beach ("*Beach*")
Ex. 1009	R.V. Shenoy and M. Datta, *Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*, 143 J. Electrochemical Soc'y, pp. 544-549 (1996) ("*Shenoy*")
Ex. 1010	U.S. Patent No. 5,905,274 to Ahn et al. ("*Ahn*")
Ex. 1011	U.S. Patent Application Publication No. US 2010/0258843 A1 to Lidow et al. ("*Lidow*")
Ex. 1012	U.S. Patent No. 9,748,347 to Cao et al. ("the '347 patent")
Ex. 1013	Prosecution History of the '347 patent
Ex. 1014	Chuan Xu et al., *The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaN/GaN Heterostructure*, 28 IEEE Electron Device Letters, pp. 942-944 (2007) ("*Xu*")
Ex. 1015	U.S. Patent Application Publication No. US 2002/0066908 A1 to Smith ("*Smith*")
Ex. 1016	U.S. Patent Application Publication No. US 2006/0273347 A1 to Hikita et al. ("*Hikita*")
Ex. 1017	U.S. Patent Application Publication No. US 2009/0072272 A1 to Suh et al. ("*Suh*")

Exhibit	Description
Ex. 1018	X. Hu et al., *Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate*, 36 Electronics Letters, pp. 753-754 (2000) ("*Hu*")
Ex. 1019	U.S. Patent Application Publication No. US 2005/0087763 A1 to Kanda et al. ("*Kanda*")
Ex. 1020	Yasushiro Uemoto et al., *A Normally-off AlGaN/GaN Transistor with $R_{on}A=2.6\Omega cm^2$ and $BV_{ds}=640V$ Using Conductivity Modulation*, 2006 International Electron Devices Meeting, IEEE (2006) ("*Uemoto*")
Ex. 1021	U.S. Patent Application Publication No. US 2006/0019435 A1 to Sheppard et al. ("*Sheppard*")
Ex. 1023	Dietrich W. Widmann, *Metallization for Integrated Circuits Using a Lift-Off Technique*, 11 IEEE Journal of Solid-State Circuits, pp. 466-471 (1976) ("*Widmann*")
Ex. 1025	Declaration of Kelley Green Hazel
Ex. 1026	Declaration of Shauna Wiest
Ex. 1027	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 ("*Beach-II*")
Ex. 1028	Petitioner and Complainant's Proposed Claim Construction, ITC 337-TA-1366
Ex. 1029	C. S. Suh et al., "p-GaN/AlGaN/GaN Enhancement-Mode HEMTs, 2006 64th Device Research Conference, June 2006, pp. 163-164 ("Suh 2006")

[023] I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

V. LEGAL STANDARDS

[024] I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

[025] I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can "anticipate" a claim. Second, I have been informed that the prior art can render a claim "obvious" to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

[026] I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

[027] I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-7 of the ’335 patent from the perspective of a person of ordinary skill in the art at the ’335 patent’s earliest claimed priority date in 2009, as described in more detail below.

[028] I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

[029] For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill in the Art

[030] I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

[031] I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Anticipation

[032] I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

C. Obviousness

[033] I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

[034] I have been informed that a proper obviousness analysis includes the following:

a. Determining the scope and content of the prior art;

b. Ascertaining the differences between the prior art and the claims at issue;

c. Resolving the level of ordinary skill in the pertinent art; and

d. Considering evidence of secondary indicia of non-obviousness (if available).

[035] I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the challenged claims is April 8, 2009. My opinions would not change if I assumed a later date of invention.

[036] I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

[037] I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

[038] In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—but not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

[039] I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the

benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

[040] I have been informed that the law permits the application of "common sense" in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

[041] I have been informed that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to

combine references. But I also understand that the "teaching, suggestion, or motivation" test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

[042] I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '335 patent.

[043] I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. OVERVIEW OF THE '335 PATENT

A. The Claims and Specification

[044] The '335 patent relates to enhancement-mode GaN power transistors. Ex. 1001, 1:21-26, 2:34-57, Fig. 5, claims 1-7. Consistent with my own understanding of the state of the art prior to April 2009, the patent describes that conventional prior art GaN HEMT devices suffered from high gate leakage current between the gate and 2DEG region. Ex. 1001, 1:21-2:30. It admits that conventional GaN enhancement-mode devices included **a GaN channel layer**, **an AlGaN barrier layer**, **source** and **drain electrodes**, and a gate structure consisting of a **p-type GaN layer with sloped sidewalls** and an overlying **gate metal**—all features that are in the claims of the '335 patent. Ex. 1001, 1:21-2:30, Figs. 1-2, 3A-3B, claims 1-7. And the figures show numerous prior art systems with these features. Ex. 1001, 1:21-2:30, Figs. 1-2, 3A-3B. Figure 2 shows surface leakage **path 201** along the sloped sidewalls of the **p-type GaN layer 202**. *Id.*

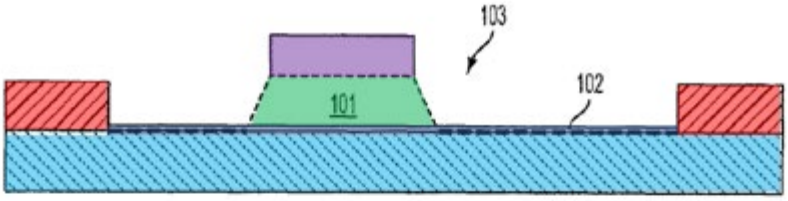


FIG. 1
PRIOR ART

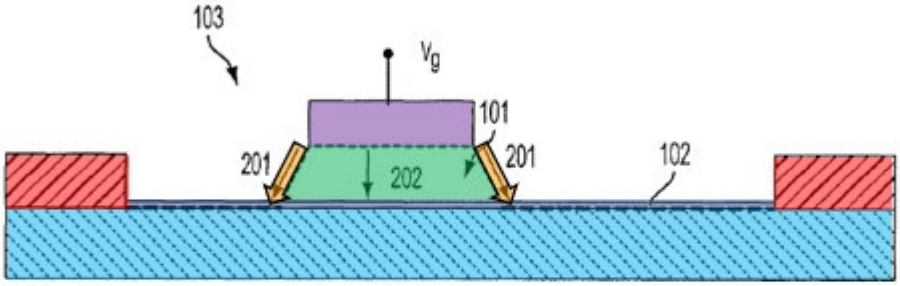


FIG. 2
PRIOR ART

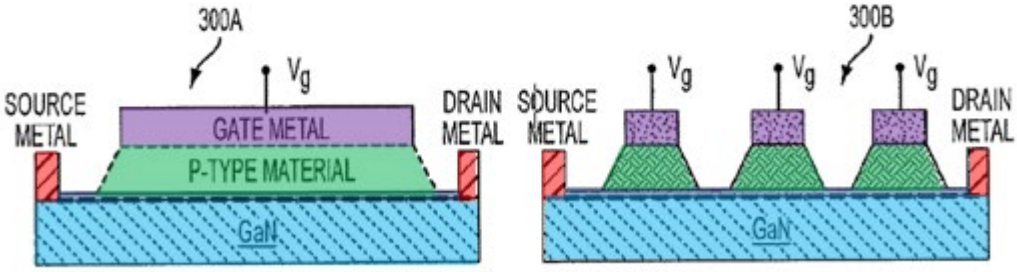
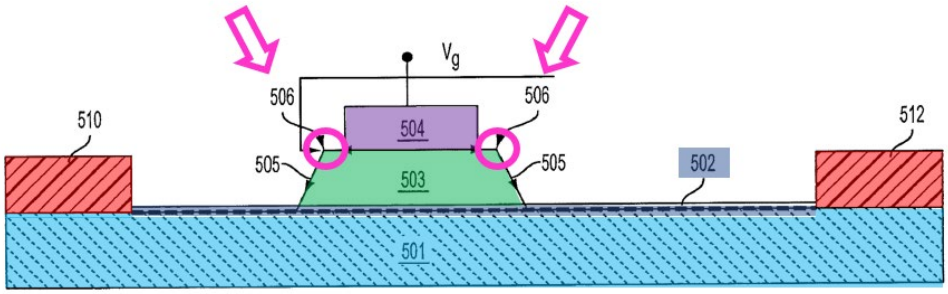


FIG. 3A
PRIOR ART

FIG. 3B
PRIOR ART

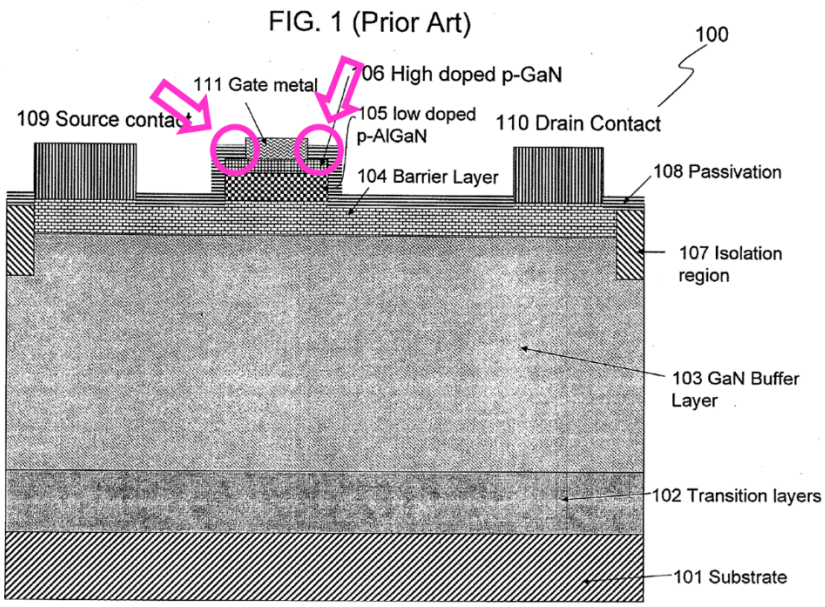
Ex. 1001, Figs. 1-2, 3A-3B.

[045] To solve the leakage problem, the ’335 patent purports to invent ***just one feature***: a pair of **ledges** on the p-type gate material, on either side of the gate metal. Ex. 1001, 2:34-57, 3:65-4:12, 4:40-51, Figs. 1-2, 3A-3B, 4-5, 7A-7B, 8, claims 1-7.



Ex. 1001, Fig. 5.

[046] But, as I will explain in this declaration, the claims were obvious over the prior art. Those ledges were well-known and common going back many years before the ’335 patent. *Infra* §§X-XIII (Grounds 1-6). Indeed, the ’335 patent’s priority application *Lidow* notes such ledges were conventional. *Lidow*, [0006], Fig. 1.



Lidow, Fig. 1.

[047] In some claimed embodiments, the '335 patent makes its **ledges** using a self-alignment process. Ex. 1001, 4:14-39, claims 2, 5. Figures 6A-6C disclose a method of making these "self-aligned ledges." Ex. 1001, 4:14-39. Priority applications also disclose "self-aligned gate" structures having symmetric ledges but do not describe the details of Figures 6A-6C. *E.g.*, *Lidow*, Abstract, [0008], [0022]-[0023], [0029]-[0030], [0036], [0038], [0040], [0044], [0046], claims 1, 6, 9, 10, 23.

[048] In the '335 patent, the self-aligned method includes forming **GaN layer 601**, **AlGaN layer 602**, and **p-type gate material 603**, then depositing the **gate metal 604** as Figure 6A depicts. Ex. 1001, 4:14-39. The self-aligned method then applies **photoresist 605**, etches the gate metal, and etches the p-type gate material so that the outer walls **p-type gate material 603** and **gate metal** align as shown in Figure 6B. Ex. 1001, 4:14-26.

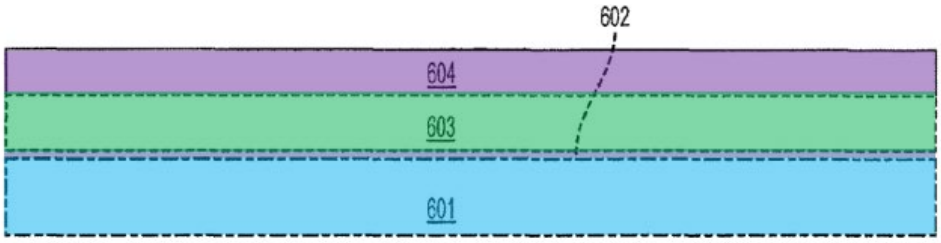


FIG. 6A

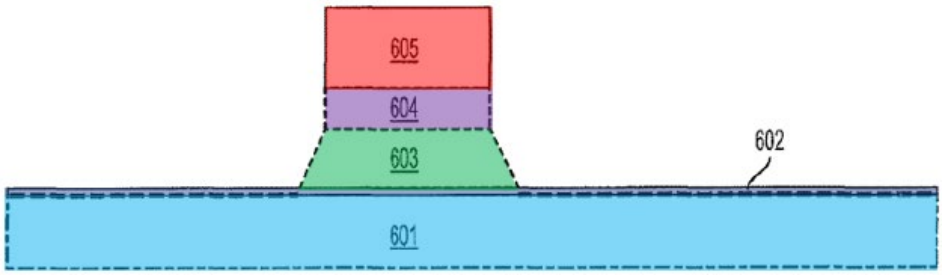


FIG. 6B

Ex. 1001, Figs. 6A-6B.

[049] The ’335 patent discloses that one way to complete the “self-aligned” ledges is to next “isotropically” etch the **gate metal** and undercut the same **photomask**, as shown in Figures 6B-6C. Ex. 1001, 4:23-39.

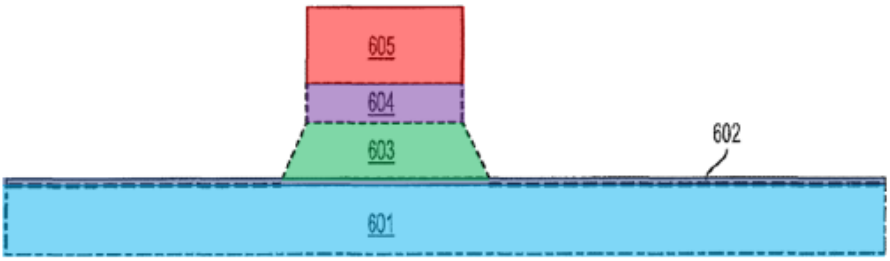


FIG. 6B

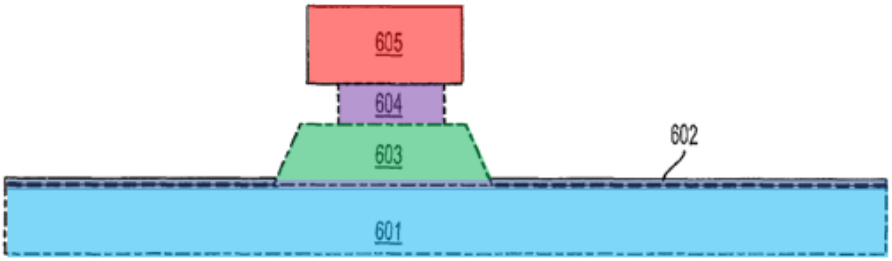


FIG. 6C

Ex. 1001, Figs. 6B-6C.

B. Prosecution History

[050] The ’335 patent was filed on July 20, 2017, as U.S. Application 15/655,438. Ex. 1001, cover. The independent claims included the p-type gate metal material, overlying gate metal, and a pair of horizontal ledges, but did not include the sloped sidewall features. Ex. 1002, 77-79. The application received one non-final Office Action rejecting claims 1-3, 5-8, and 10-11 under 35 U.S.C. § 102, as anticipated by *Hikita* (Ex. 1016). Ex. 1002, 36-43. To overcome the rejection, the applicant amended the independent claims to include sloped sidewalls. Ex. 1002, 34-35, 7-15. The Examiner then allowed the claims, stating

that the combination of the sloped sidewalls and horizontal ledges were allowable. Ex. 1002, 12.

[051] During the examination of the parent application, U.S. Application No. 14/447,069 (U.S. Patent No. 9,748,347 ("the '347 patent")), I understand that the applicant initially received a rejection over prior art reference *Lidow*, then subsequently claimed priority to *Lidow* a continuation-in-part. Ex. 1013, 95-128, 250. The applicant nevertheless next received a rejection over *Lidow* because the claims included the term "isotropically etching," which was not recited in *Lidow*. Ex. 1013, 84-86. The Examiner only found support for the claims of the '347 patent after the applicant broadened the claim to remove the term "isotropically" from the claim. Ex. 1013, 52, 75-76, 85-86. In my opinion, the apparatus claims of the '335 patent covers substantially the same subject matter as the structure which results from the method claims of the '347 patent. Ex. 1001; Ex. 1012. Thus, to the extent the priority claim is valid (which I assume without offering an opinion), *Lidow* also supports the claims of the '335 patent.

VII. LEVEL OF ORDINARY SKILL IN THE ART

[052] In rendering the opinions set forth in this declaration, I have been asked to consider the '335 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the

art," "skilled artisan," "POSITA," "POSA" or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

[053] Taking the factors described in the Legal Standards – Level of Ordinary Skill in the Art section into consideration, it is my opinion that a person of ordinary skill in the art for the '335 patent would have had at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa.

[054] Based on my educational background and experience, I was at least a person of ordinary skill in the art at the earliest priority date of the '335 patent.

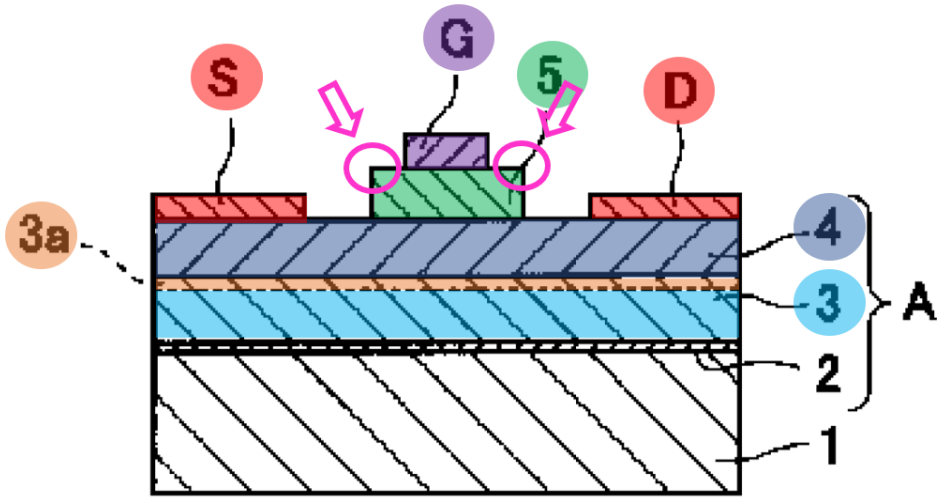
VIII. TECHNOLOGY BACKGROUND AND THE STATE OF THE PRIOR ART

[055] Power transistors fabricated with GaN have a large band gap which increases the maximum electric field strength, resulting in a large breakdown voltage making them attractive for high power applications. Ex. 1001, 1:30-49.

They were well known long before the ’335 patent. *E.g.*, *Smith*, [0004]-[0010] (discussing “well known” features of GaN HEMT devices). Conventional features of such transistors include a **GaN channel** and **AlGaN barrier** layers, at the heterojunction of which a **two-dimensional electron gas (2DEG) region** forms, as well as **source** and **drain electrodes**, and a gate structure including **GaN gate materials** under a **gate metal**. Ex. 1001, 1:28-2:26; *Yoshida*, Abstract; *Suh*, [0002]-[0005], [0015], Figs. 1, 6-7.

[056] Enhancement-mode GaN transistors are normally off, meaning no drain current flows through the 2DEG without applying positive voltage to the gate. Ex. 1001, 1:50-53, 1:64-2:2; *Hu*, 1. These devices achieve the normally-off state in part with a **GaN layer**, often doped p-type, in the gate structure under a **gate metal**, which increases the gate voltage (to a positive value) where the gate has a strong influence on the electron concentration in the 2DEG. Ex. 1001, 1:50-53, 1:64-2:2; *Hu*, 1.

[057] Example GaN HEMT arrangements in publications ranging from 1999 through 2009 (the earliest claimed priority date of the ’335 patent), are shown below. I have marked **horizontal ledges** at the surface of the **p-type GaN gate materials**:



Yoshida, Fig. 1 (1999).

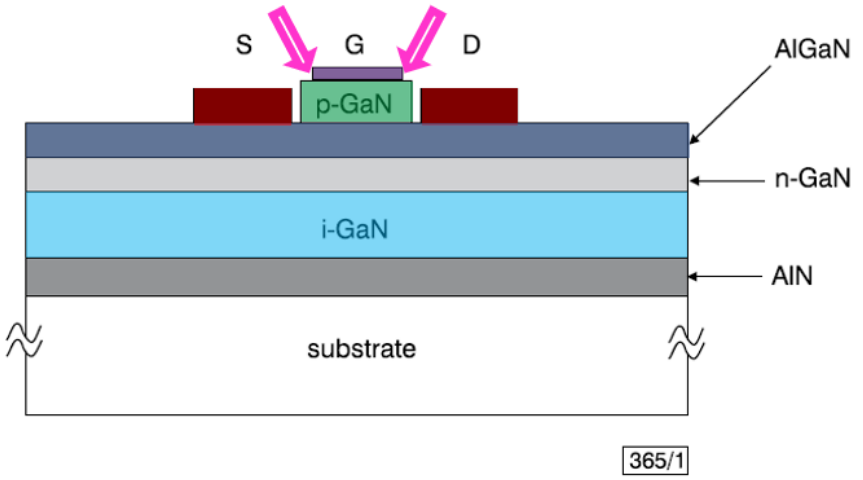


Fig. 1 *Schematic diagram of structure of pn junction regrown gate HFET*

Hu, Fig. 1 (2000).

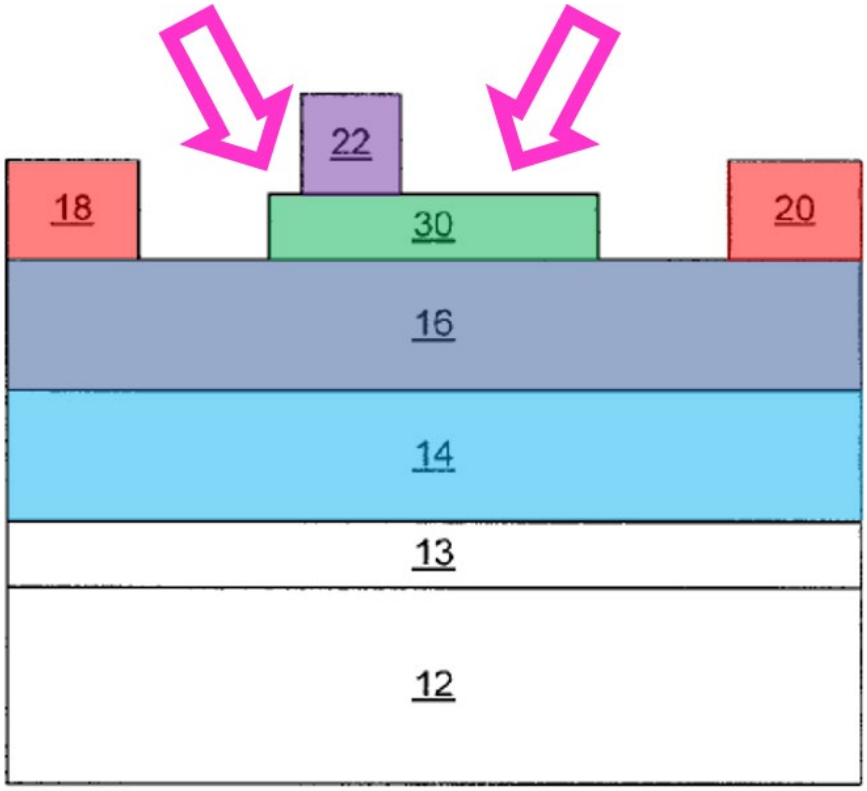
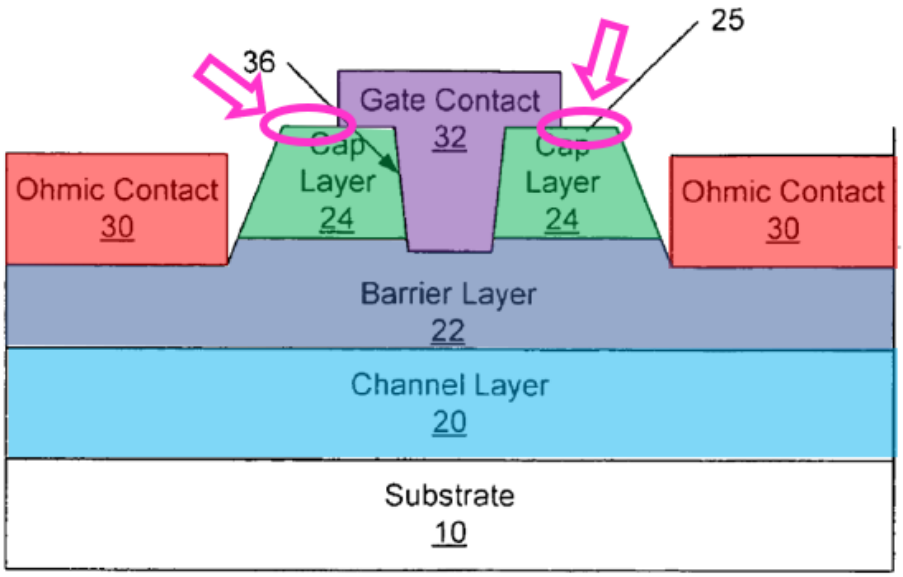
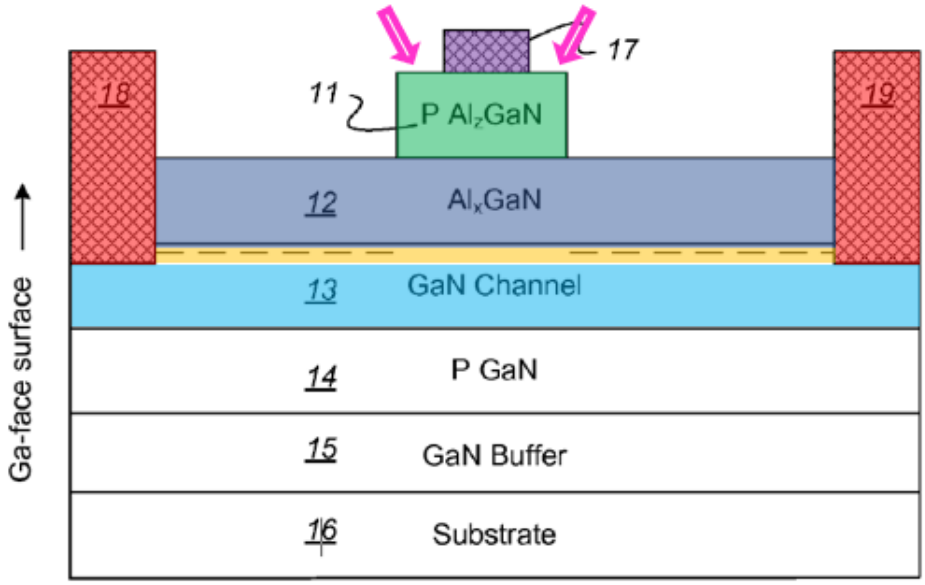


Figure 5B

Smith, Fig. 5B (2002).



Saxler, Fig. 1A (2006).



Suh, Fig. 6 (2009).

[058] As these examples illustrate, the sole point of alleged novelty of the ’335 patent, **horizontal ledges** at the surface of **p-type GaN gate materials**, were common, just as were the other features of the claims.

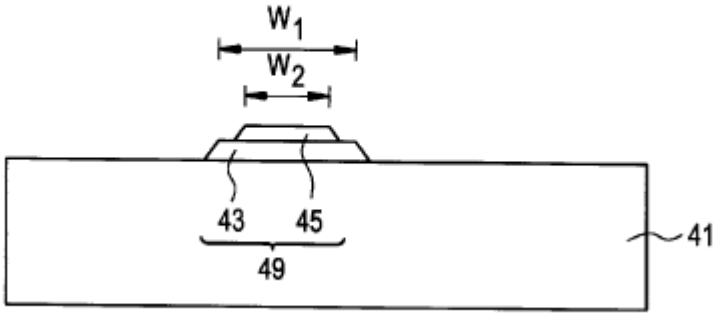
[059] The prior art also included many different methods of manufacturing features of GaN HEMT devices. For example, single-mask techniques to self-align stacked gate structures were long known. *Beach*, [0040]. Conventional etching techniques achieved sloped sidewalls, which were known to increase leakage paths. Ex. 1001, 1:64-2:8, Fig. 2; *Saxler*, [0064], Figs. 1A-1B; *Ahn*; *Xu*; *Sheppard*, [0044]. And it was conventional to create undercuts under photomasks to isotropically etch metals. *Shenoy*.

[060] A POSITA would have been familiar with many methods of making stepped gate structures with **horizontal ledges**, including (i) sequential masking and etching steps, (ii) lift off techniques, and (iii) self-aligned techniques. For example, *Yoshida* discloses masking and etching the p-type GaN **layer 5**, then depositing the **gate electrode**. *Yoshida*, [0022]-[0023]. *Hu* grows gate layers in “selective areas defined by openings in an SiO_2 mask.” *Hu*, 1. *Smith* fabricates its gate structure by patterning the **GaN cap layer**, using conventional etching to remove portions of it, then forming a **gate electrode** on the GaN segment. *Smith*, [0040]-[0041]. *Smith* also uses “conventional photolithographic techniques and

mask alignment tools" to align the edges of a cap layer and gate in some embodiments, i.e., ***self-alignment***. *Smith*, [0041]. *Saxler* discloses sequential masking, etching, and deposition steps to form its stacked gate structure. *Saxler*, [0064]-[0066]. *Suh* likewise etches "to define a gate region where the p-type Al_zGaN cap 11 is located," and depositing the gate on top. *Suh*, [0056].

[061] *Beach* makes a self-aligned two-layer gate structure using a single photomask. *Beach*, [0040], [0045], [0054]. *Ahn*, published in 1999, likewise uses a single mask and further discloses isotropic and anisotropic etching techniques to create stacked gate structures having stepped features and sloped sidewalls, as shown below. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C.

FIG. 4C



Ahn, Fig. 4C.

[062] In addition, long before the '335 patent, *Shenoy* discloses techniques to isotropically etch and undercut metal layers below masks, which a POSITA

would understand would be one method of forming stepped gate structures. *Shenoy*, 2-3. Lift-off had similarly been known for decades for creating stepped metal structures. Ex. 1023.

[063] Typical GaN HEMT devices thus included every feature of the claimed enhancement-mode transistor and they disclosed methods of making such a transistor.

IX. CLAIM CONSTRUCTION

[064] I am not an attorney. However, I have been informed by counsel of certain legal standards that apply with respect to claim construction and indefiniteness, and have used those standards, described below in formulating my opinions.

[065] I have been instructed that the "intrinsic record" includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent's prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office ("Patent Office") concerning the patent (Ex. 1002). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms

or to limit the scope of claim terms in his patent claims, which may differ from the term's plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent's written description, the patent's prosecution history, or both.

[066] I understand that claim interpretation may also be informed by "extrinsic evidence" (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the relevant time period.

[067] I am also informed by counsel that the applicant of the '335 patent can act as their own lexicographer, to set forth a definition of a claim term in the specification. The definition provided by the applicant can differ from the claim term's plain and ordinary meaning. I have also been informed by counsel that when a patent claim uses the term "comprises" as a transitional statement after the preamble, there is a presumption that the claim is open-ended and not limited to the recited elements.

[068] I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a

person of ordinary skill in the art at the earliest claimed priority date of the ’335 patent, other than as identified below.

[069] Based on my review of these materials and my personal knowledge and experience, I have considered the plain and ordinary meaning of each term of the ’335 patent as it would have been understood by one skilled in the art at the earliest claimed priority date of the ’335 patent of April 8, 2009. I apply the plain and ordinary meaning of each claim term throughout this declaration, other than as identified below.

A. “side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer”

[070] I have been informed that the owner of the ’335 patent Efficient Power Conversion Corporation (EPC or Patent Owner) and Petitioner Innoscience have agreed in a related matter that the terms “side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer” in claims 1 and 5 of the ’335 patent should be construed. *ITC Constructions*, pp. 1, 4, 8-9. The parties proposed the following constructions:

Petitioners'	Patent Owner's
"side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer"	"p-type gate material having side surfaces extending horizontally such that the bottom of the material is wider than the top of the material"

[071] As I explain below, the challenged claims are unpatentable under both constructions. But to the extent the Board construes the term, Petitioners' proposed construction should apply.

[072] In my view, the construction agrees with the disclosure of the prior application, *Lidow*, which provides support for the present claims (§VI.B (Prosecution History)). *Lidow* discusses the advantage of using sloped sidewalls in a p-type GaN gate layer to reduce gate leakage. *Lidow*, [0041]-[0042], Fig. 8. The only way *Lidow* distinguishes its sidewalls is by indicating that a "base that is more than 10% wider than the top" advantageously "causes a longer path for electrons to

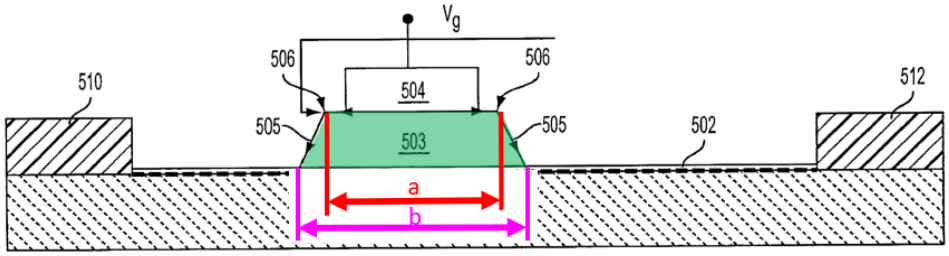
travel between the gate metal 17 and the 2DEG along the pGaN side wall," thereby "result[ing] in lower gate leakage." *Id.*, [0042]. *Lidow*'s depicts and describes the same p-type layer and gate structure that the '335 patent discloses. *Id.*, Fig. 8; Ex. 1001, 3:49-64, Fig. 5.

[073] Petitioner's construction aligns with the purpose of the '335 patent, which is to lower gate leakage, including through the conventional method of sloping the sidewalls to increase the length of sidewall leakage path 201. Ex. 1001, Abstract, 1:21-26, 2:20-48, 3:65-4:12, 4:40-51, Figs. 2, 4, 7A-7B, 8.

[074] Aside from the 10% guidance, *Lidow* provides no other explanation of how much slope would be necessary to achieve the alleged improvement of the '335 patent, reduced gate leakage. Explicit guidance on the amount of slope would be needed to distinguish the claim from the prior art because nearly all layers have at least slightly sloped sidewalls. Few structures, if any, have perfectly vertical sidewalls in practice, even if depicted as vertical in functional diagrams, a point that which *Saxler* notes. *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5; *infra* §XII.C.5 (Ground 4, Limitation [1d]). *Lidow* controls the shape of the p-type GaN material during etching to achieve a base 10% wider than the top and gain the alleged benefits of lower gate leakage due to a longer leakage path as compared to leakage

rates in the prior art. *Lidow*, [0041]-[0042]. Petitioners' construction makes this distinction clear, unlike Patent Owner's construction.

[075] Petitioner's construction likewise agrees with the '335 patent specification. For example, the '335 patent shows a p-type gate material with sloped side surfaces whose bottom surface is more than 10% wider than the top. Ex. 1001, Figs. 5, 6C, 7B.



Ex. 1001, Fig. 5.

Width "b" above is approximately 1.32 times the width of "a" (~30% wider), and the same holds true for Figures 6C and 7B ("b" is 1.36 times wider than "a" in 6C and 1.34 times wider in 7B). If the Patent Owner argues that Fig. 5 and 6C are schematic diagrams not intended to be drawn to scale, Fig. 7B is an actual image of the etched gate structure, and my measurements confirm it has similar dimensions to Fig. 5 and Fig 6C.

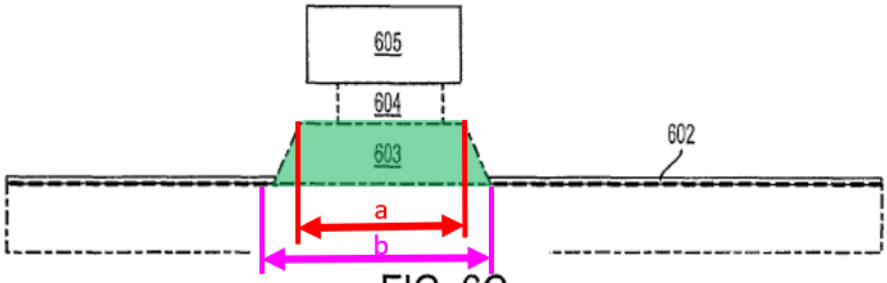


FIG. 6C

Ex. 1001, Fig. 6C.

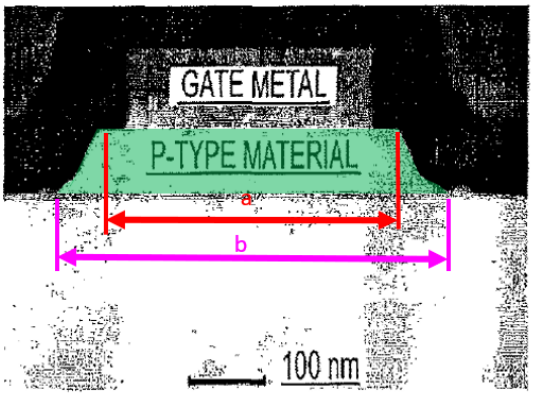


FIG. 7B

Ex. 1001, Fig. 7B.

[076] Of course, any reference that discloses this term under Petitioners' construction will also disclose this term under Patent Owner's broader construction, which is satisfied with any amount of slope whatsoever. All my analysis below showing the references disclose or render obvious the claim elements under Petitioner's construction will thus apply to either construction. Further, if Patent Owner's broader construction is accepted, the patent is

unpatentable under an additional ground, Ground 4, because, as I will explain below, a POSITA would have understood that *Yoshida*'s sidewalls would have included at least a slight slope in practice, although it draws its sidewalls vertically.

B. "self-aligned" ledges

[077] I have been informed that Petitioners proposed that the terms "wherein the pair of horizontal ledges of the p-type gate material are self aligned" / "a pair of self-aligned ledges," which are recited in dependent claim 2 and independent claim 5, are "product-by-process limitations." *ITC Constructions*, pp. 1, 4. I agree with Petitioners that these terms describe ***how*** the ledges are made, not ***what*** the ledges are. As I explain below, "self-aligned" is just one way to make these ledges. There are many other ways to manufacture the ledges described, depicted, and claimed in the '335 patent.

[078] The patent itself admits there are other ways to make the claimed ledges, and a "self-aligned" ledge refers to the process by which the claimed gate structure is made and does not describe the structure itself. Ex. 1001, 4:14-39; *Lidow*, Abstract, [0008], [0022]-[0023], [0029]-[0030], [0036], [0038], [0040], [0044], [0046], Figs. 6A-6C, claims 1, 6, 9, 10, 23. The '335 patent notes that "the gate contact includes a p-type gate material 503 formed on the barrier layer 502 and includes ledges 506 ***that are created by a self-aligned process*** at the top

corners of the p-type gate material 503." Ex. 1001, 3:49-53. The patent repeatedly refers to this "self-aligned manufacturing ***process***." Ex. 1001, 3:13-15, 3:49-53, 3:65-4:39, 4:52-63, Figs. 6A-6B.

[079] Claim 3 of the issued parent application, the '347 patent, illustrates that "self-aligned" ledges refers to how the ledges are made, not what they are. It recites "[t]he *method* according to claim 1, wherein the pair of ledges of the p-type gate material *are self-aligned*."

[080] This is consistent with how "self-aligned" would have been understood by a POSITA—as a product made by a process. For example, *Smith*, a 2002 patent publication, discloses making the ***same*** gate structure two ways—one way uses a process that is not "self-aligned" (Fig. 4C) while the other uses a "self-aligned" process (Fig. 6C).

[081] Referring to Fig. 4C, *Smith* describes a gate structure that is not self-aligned. *Smith*, [0041]. *Smith* states that "[i]n the embodiments shown in FIGS. 4A through 4C, the source-side sidewall of the **gate contact** is aligned with the source-side sidewall of the **GaN cap segment 30** using ***conventional photolithographic techniques and mask alignment tools***," and it shows the gate is indeed aligned on one side to the source-side sidewall. *Smith*, [0041], Fig. 4C.

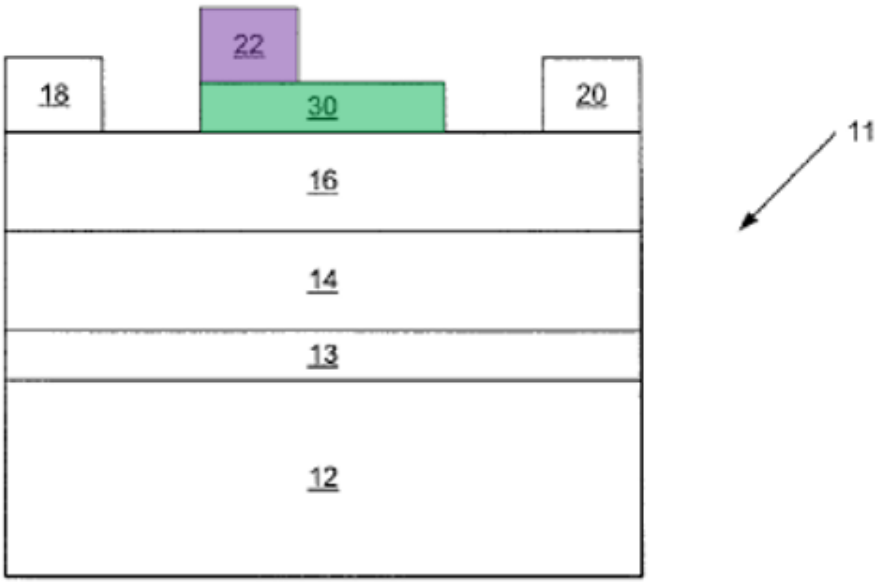


Figure 4C

Smith (Fig. 4C, ***not*** "self-aligned)

[082] *Smith* also discloses making this selfsame gate structure using a "self-aligned method" in [0042]-[0044] and figures 6A-6C. *Smith* explains this approach involves layering the **gate contact** on the **GaN cap segment**, then etching them both with a single mask:

> An etch mask 44 is deposited on the GaN cap layer 30' which partially overlaps the gate metal 22' so as to define the source-side sidewall of the gate electrode 22 and the GaN cap segment 30 and the drain-side sidewall of the GaN cap segment 30.

Smith, [0043].

> As illustrated in FIG. 6B, the exposed portion of the GaN cap layer 30' is etched away, leaving one sidewall of the

> GaN cap segment 30 self-aligned with a sidewall of gate electrode 22.

Smith, [0044].

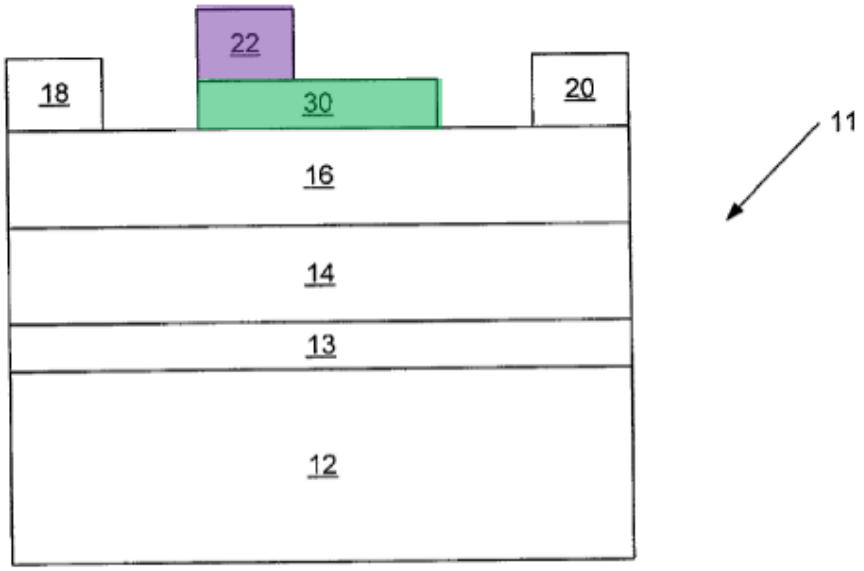


Figure 6C

Smith (Fig. 6C, "self-aligned")

[083] As another example illustrating that illustrates a POSITA would have understood "self-aligned" ledges only describes that the ledges were made by a "self-aligned" process, *Beach* discloses the method of "pattern[ing]" (applying the mask) and etching the two layers of "the stack," the "gate arrangement 24" and "gate barrier 26," which "results in a self-aligned gate arrangement." *Beach*, [0040]. This reference is by the same Robert Beach that is a co-inventor on the priority application *Lidow*, which further supports that the '335 patent's "self-

aligned" ledges (which allegedly have support in *Lidow*) refers to a process by which the ledges are made. *Beach*, cover; *Lidow*, cover; § VI.B.

[084] *Suh 2006* also describes using a "self-aligned" process to make its gate structure. Referring to enhancement-mode HEMT of Fig. 1, it states "The p-GaN in the source/drain regions was etched away prior to ohmic metal deposition using ***a self-aligned dry etch*** while the p-GaN in the access regions was etched away using the ohmic contacts and the gate electrode as masks." *Suh 2006*, 1.

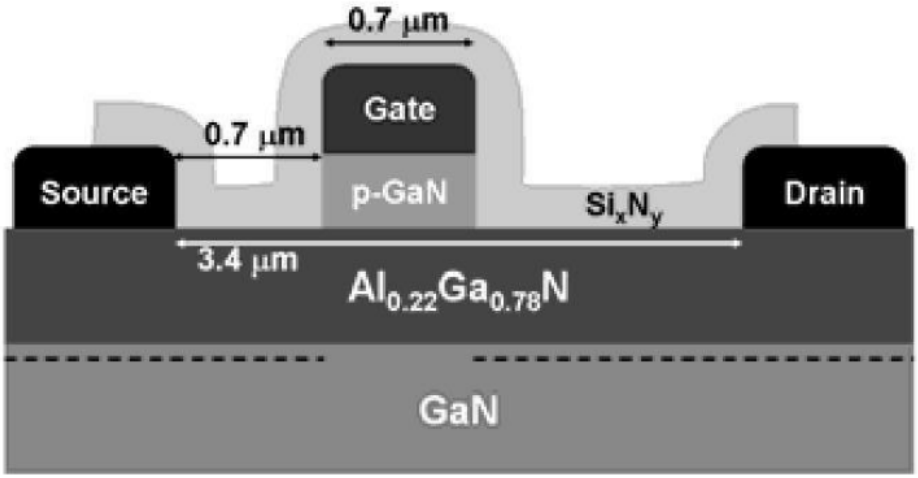


Fig. 1: Schematic cross section of the p-GaN/AlGaN/GaN E-mode HEMT.

Suh 2006 (Fig. 1)

[085] Based on the foregoing, I have been informed by counsel that claims 2 and 5 of the ’335 patent thus recite product-by-process steps in a device claim, which lend no patentable weight. Ex. 1001, claims 2, 5.

X. GROUNDS 1 AND 2: *SAXLER*, ALONE (GROUND 1) OR IN VIEW OF *YOSHIDA* (GROUND 2) RENDERS OBVIOUS CLAIMS 1-7

A. Overview of Grounds 1 and 2

[086] *Saxler* discloses a GaN transistor with the same arrangement of semiconductor layers and structures as those of the ’335 patent’s claims 1-7. It has a stacked gate structure that includes a p-type GaN layer and an overlying gate metal. *E.g.*, *Saxler*, [0061]-[0063], [0066], [0071]-[0073], [0076], [0087], Figs. 1A, 2B. In some embodiments its gate metal is not recessed. *Saxler*, [0052]. *Saxler*’s non-recessed embodiments render obvious claims 1-7. (Ground 1)

[087] The figures of *Saxler* do not depict its non-recessed embodiments. In my opinion, it would be obvious to a POSITA that the non-recessed embodiments include a stepped, stacked gate structure as depicted in Figs. 1A and 2B but with a flush, rather than recessed, gate metal layer. Nevertheless, to the extent Patent Owner argues that *Saxler*’s cap layer does not render the claims obvious because its figures do not show the non-recessed embodiments (despite *Saxler*’s explicit disclosure the recess is optional), *Yoshida* also discloses and depicts a very similar

device with a p-type gate material without a gate recess. The combination of *Saxler* and *Yoshida* renders obvious claims 1-7 (Ground 2).

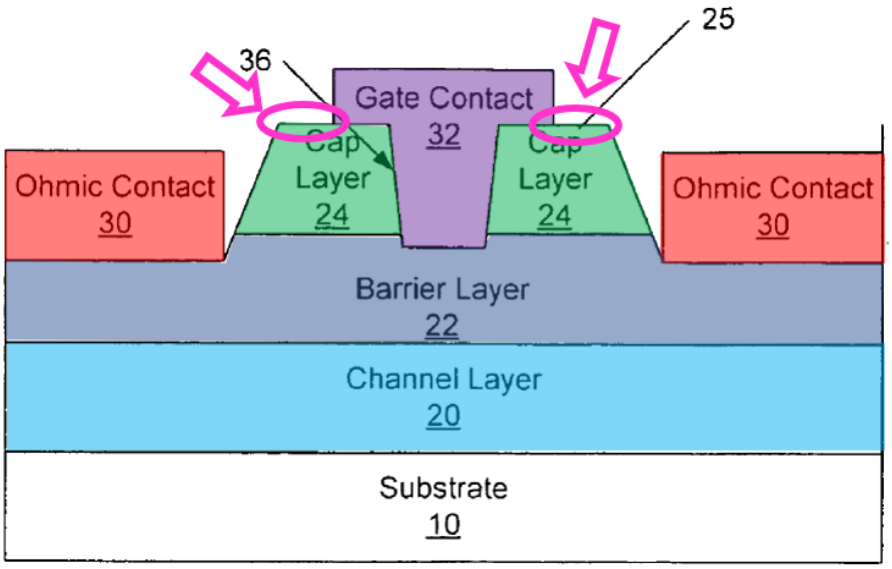
[088] In my analysis below, I will indicate where portions of *Saxler* alone discloses or renders obvious the claim elements (for Ground 1 and Ground 2), and where *Saxler* in view of *Yoshida* discloses or renders them obvious (for Ground 2).

1. Ground 1: *Saxler*

[089] *Saxler* discloses a GaN transistor with high breakdown voltage. *Saxler*, [0006], [0007]-[0030], Figs. 1A, 2B. Below, I will explain how *Saxler*'s device discloses all features of the device claimed by the '335 patent. As I illustrate below with color-coded highlighting, *Saxler*'s **channel layer 20** is a GaN over silicon, and *Saxler*'s **barrier layer 22** is a Group III-nitride that may be AlGaN. *Saxler*, [0057]-[0060], Figs. 1A, 2B. *Saxler* discloses "induc[ing] a **two-dimensional electron gas**" at the interface of these layers, as was typical of such devices. *Saxler*, [0004], [0059] *Saxler* discloses **source** and **drain** contacts. *Saxler*, [0065].

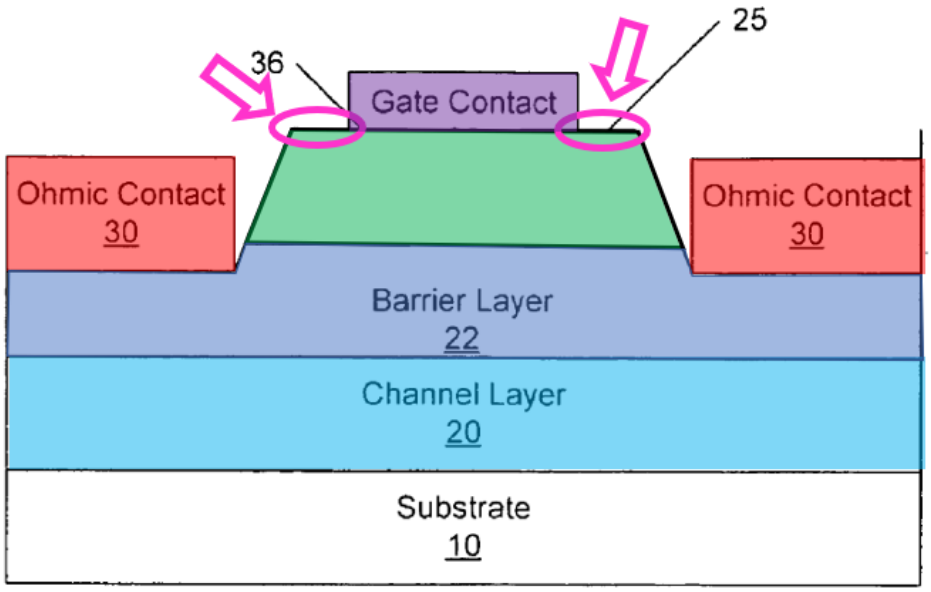
[090] *Saxler*'s device includes a stacked gate structure above the **barrier layer 22** consisting of a **cap layer** and **gate contact** that is metal. *Saxler*, [0061]-[0063], [0066], [0071]-[0073], [0076], [0087], Figs. 1A, 2B. *Saxler* offers several options for its device, including that its **cap layer** may be p-typed doped GaN, and

the **cap layer** is either doped in a subregion or doped throughout. *Saxler*, [0013], [0069], [0071], [0073]. As I explained previously, *Saxler*'s gate contact may be recessed or non-recessed (i.e., flat). *Saxler*, [0052], [0066]. Where utilized, *Saxler*'s recessed **contact** may be T-shaped, and in some embodiments it extends ***through*** the **cap layer** into the **barrier layer**, but in other embodiments the **gate contact** does not contact the **barrier layer**. *Saxler*, [0065].



Saxler, Fig. 1A.

[091] In embodiments where the gate recess is not utilized, a POSITA would have understood that *Saxler* has the following structure—it has the same stepped, stacked gate structure as depicted in Figs. 1A and 2B but with a flush (i.e., flat), rather than recessed, **gate contact** layer:



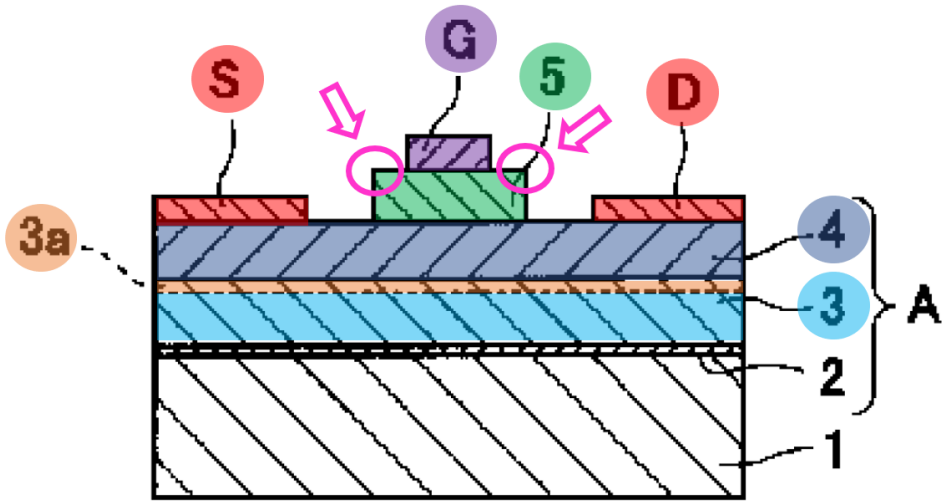
Saxler, Fig. 1A (modified).

2. *Yoshida*

[092] *Yoshida* published ten years before the earliest possible priority of the ’335 patent, and it discloses a structure that has all features of the device claimed by the ’335 patent, just like *Saxler*, as I will explain below. *Yoshida*’s device is a normally-off enhancement-mode GaN transistor having a p-type GaN layer below the gate that “enables voltage control with a small amount of carrier injection,” an arrangement that was entirely conventional by the time of the ’335 patent. *Yoshida*, [0017], [0015], Fig. 1. *Yoshida* purports to improve breakdown voltages over prior art GaN transistors. *Yoshida*, [0008]-[0009].

[093] Just like *Saxler*'s channel and barrier layers, *Yoshida*'s **layer 3** is a GaN layer grown on a GaN buffer layer (layer 1) on a silicon substrate and **layer 4** is an n-type semiconductor, and a **2DEG 3a** forms at their interface. *Yoshida*, Abstract, [0010], [0013], [0019]. The device includes a **source** and **drain** contact, as was conventional. *Yoshida*, Abstract, [0009].

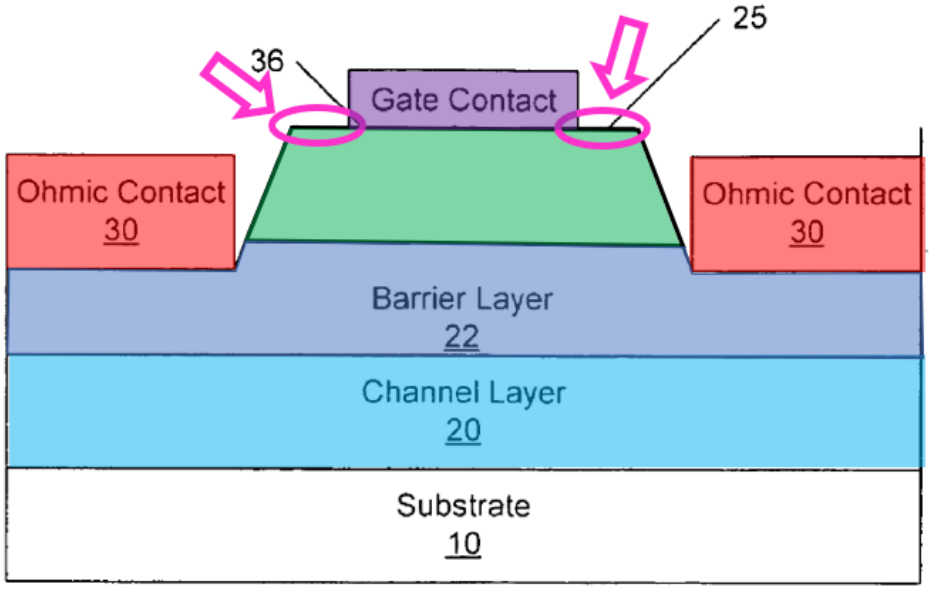
[094] *Yoshida* also discloses a stacked gate structure consisting of a **doped GaN layer** above the **semiconductor layer 4** and an overlying **gate metal**, with a pair of **horizontal ledges** on either side of the gate metal, like the ledges of *Saxler* and the '335 patent. *Yoshida*, Abstract, [0015], Fig. 1.



Yoshida, Fig. 1.

3. Ground 2: The combination of *Saxler* in view of *Yoshida*

[095] Implementing *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure results in the following combined structure. The resulting structure has the same arrangement of components as *Saxler*'s non-recessed embodiment:



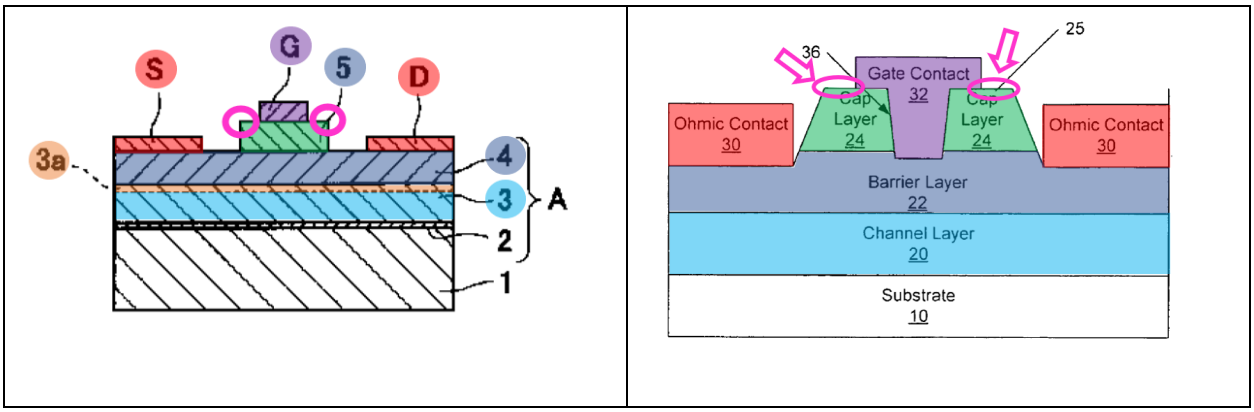
Saxler, Fig. 1A (modified).

4. Ground 2: Motivation to Combine

[096] In my opinion, it would have been obvious to implement *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure.

[097] The devices of these references are compatible. *Saxler* and *Yoshida* disclose compatible enhancement-mode GaN HEMT devices comprising the same layers performing the same functions, including stacked gate structures having a cap layer and gate metal. Both references describe gallium nitride HEMTs that

they claim will improve breakdown voltages over the prior art. *Yoshida*, [0008]-[0009]; *Saxler*, [0006], [0007]-[0030]. Unsurprisingly, *Yoshida* and *Saxler*'s transistors share numerous overlapping features. As I illustrate below, they use the same arrangement of layers.



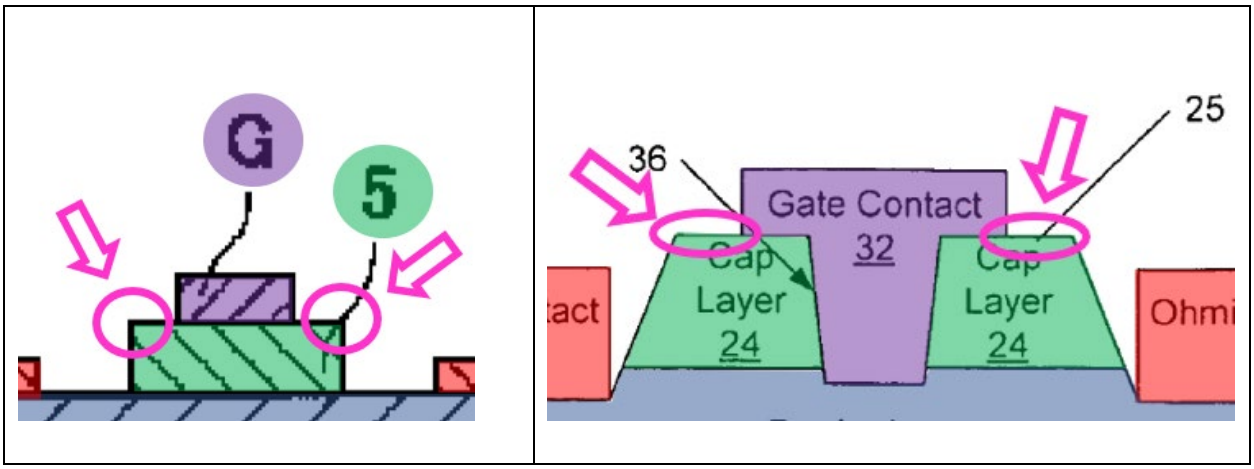
Yoshida, Fig. 1, *Saxler*, Fig. 1A (**2DEG region** present, but not shown).

[098] As I explained above, *Yoshida*'s **layer 3** is GaN over a silicon substrate, as is *Saxler*'s **channel layer 20**. *Yoshida*, [0012], [0019]; *Saxler*, [0057]-[0058]. *Yoshida*'s **layer 4** is an n-type semiconductor, just like embodiments of *Saxler*'s **barrier layer 22**. *Yoshida*, Abstract, [0010], [0013]; *Saxler*, [0059]-[0060]. Both have **2DEG regions** formed at the junction of these two layers, as was typical. *Yoshida*, [0016]; *Saxler*, [0004], [0006], [0008]. Both references have **source**, **drain**, and **gate metal** contacts, which was common. *Yoshida*, Abstract, [0009]; *Saxler*, [0065]-[0066]. And both disclose a **doped layer**

above the **barrier** and in contact with the **gate metal**, which also was common. *Yoshida*, Abstract, [0015]; *Saxler*, [0069], Figs. 1A, 2B.

[099] While *Yoshida* and *Saxler* disclose slightly different topologies for their stacked gate structures, these structures perform identical functions in both references, which is, as *Yoshida* puts it, to control voltage "with a small amount of carrier injection" and "enable[] control of current flowing between channels" at high voltage. *Yoshida*, [0017]; *Saxler*, [0065].

[100] In the embodiments shown in *Saxler*'s figures, the gate metal occupies a recess in the cap layer extending into the barrier layer, and *Saxler* describes that this recess that may reach to touch the barrier layer in some embodiments but may not touch the barrier layer in others. *Saxler*, Abstract, [0007]-[0008], Figs. 1A, 2B. *Yoshida*'s gate metal, in contrast, sits flush on top of layer 5. *Yoshida*, Fig. 1. I have illustrated those structures below.



Yoshida, Fig. 1, *Saxler*, Fig. 1A.

[101] *Saxler* states many times that this gate recess is optional. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88. And while its figures do not explicitly show a stacked gate structure without a gate recess, *Saxler*'s many statements that the recess is optional in view of the rest of *Saxler*'s description and figures disclose or at least render obvious the structure claimed by the '335 patent. To the extent Patent Owner disagrees that *Saxler*'s optional recess renders the claims of the '335 patent obvious (Ground 1), *Yoshida* further renders the claimed device obvious (Ground 2).

[102] In my opinion, a POSITA would have been motivated to combine *Saxler*'s and *Yoshida*'s gate structures and accompanying fabrication techniques and found it obvious to do so. A POSITA would have been familiar with many methods of making such stacked, stepped structures, as I explained above (§ VIII, Technology Background). Given the many interchangeable ways to fabricate such structures, it would have been obvious to combine *Saxler* and *Yoshida* to simplify manufacturing and decrease costs.

[103] For example, *Saxler* references and incorporates *Sheppard* (Ex. 1021) as disclosing "[s]uitable structures and techniques for fabricating GaN-based

HEMTs" of *Saxler*'s embodiments. *Saxler*, [0046] (referencing Ser. No. 10/897,726), [0068] (same). To create the same gate recess as *Saxler* and deposit the gate metal, *Sheppard* discloses complicated and exacting manufacturing processes. *Id.*, [0043], [0046]-[0051], [0053]-[0056], Figs. 1C-1F, 2A-2B, Fig. 3. *Sheppard*'s GaN cap layer may be "about 2 nm to 500 nm thick," for example, and its thin AlGaN underlying barrier layer is between "0.1 nm and about 40 nm." GaN. *Id.*, [0040], [0042]. As a POSITA would have understood, manufacturing tolerances were accordingly extremely small, which raises complexity and costs of manufacturing to avoid costly out-of-tolerance defects. Further, with the recess, *Saxler*'s device is not enhancement mode (always off), and a POSITA would have been motivated to remove the recess to create an enhancement mode device and realize the benefits of a normally off device, which renders it suitable for high power applications. *Suh*, 1.

[104] To avoid these problems, a POSITA would have been motivated to use *Saxler*'s non-recessed gate contact in its stacked gate structure in combination with *Yoshida*'s gate structure and accompanying fabrication techniques. That approach would have eliminated the exacting gate-recess manufacturing steps. In my opinion, a POSITA would have recognized *Yoshida*'s approach as a suitable option for solving such problems. And, as I explained above, a POSITA would

have been familiar with a wide variety of stacked gate structures in GAN HEMT devices, including many without recessed gates, and thus found *Yoshida*'s and *Saxler*'s structures readily combinable and interchangeable.

[105] Indeed, *Saxler* expressly recognizes that various other HEMT structures would be compatible with its purported invention, and explicitly includes *Smith*'s devices among such options. *Saxler*, [0087]. *Smith* discloses non-recessed gate electrodes in stacked structures that are similar to *Saxler*'s recessed stacked gate structure. *Smith*, [0033], [0041], Figs. 3, 5B. *Smith* states that "there is no benefit to recessing the gate down to the barrier layer" in GaN HEMT devices "because the top surface of GaN is generally not conductive." *Id.*, [0010]. And although *Smith* briefly discloses using T-shaped gate electrodes for "microwave and RF" applications (*Smith*, [0017], [0034], claim 20), *Smith* otherwise only discloses stacked gate structures having a **GaN cap layer** with a non-recessed **gate electrode** (*id.*, [0033]-[0037], [0039]-[0043], claim 1, Figs. 3, 4A-4C, 5A-5B). Just like *Saxler*, *Smith*'s GaN HEMT also includes a **GaN channel layer** and **AlGaN barrier layer** (inducing a **2DEG region**), and **source** and **drain electrodes**. *Smith*, [0030]-[0037], [0041]. A POSITA would thus have understood non-recessed electrodes were a suitable option for *Saxler*'s GaN, which bears substantially the same layers and structure.

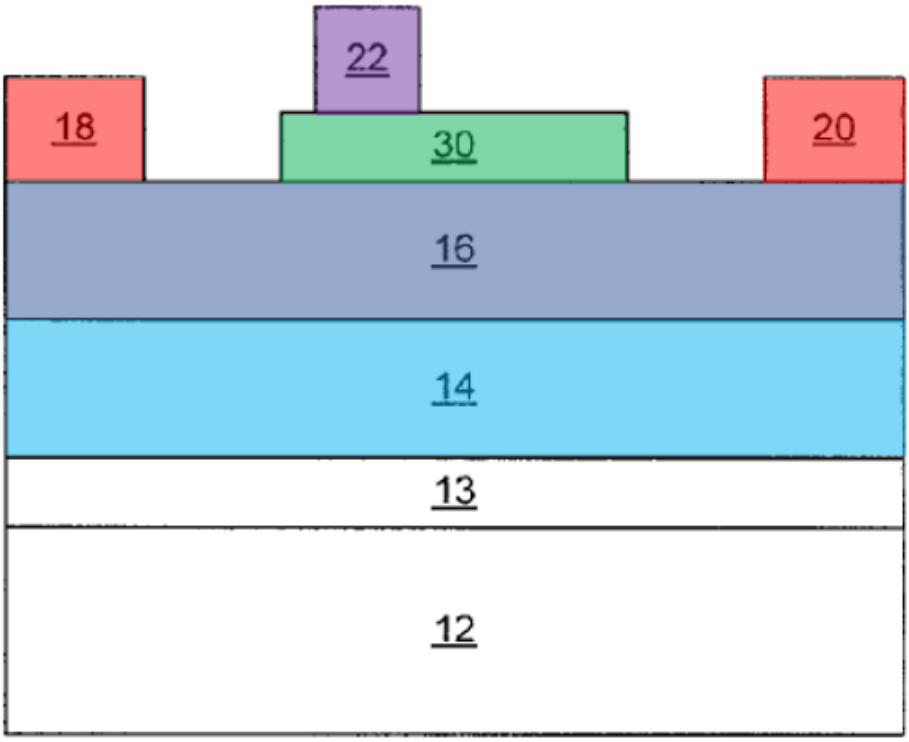


Figure 5B

Smith, Fig. 5B.

[106] In view of the many interchangeable options for stacked gate structures in GaN HEMT, a POSITA would have found the combination of *Yoshida*'s non-recessed gate arrangement in *Saxler*'s gate arrangement a simple substitution of known elements to predictably yield an enhancement mode GaN HEMT device.

B. Independent Claim 1

[107] In my opinion, *Saxler* in view of the knowledge of a POSITA (Ground 1) and in view of *Yoshida* (Ground 2) renders obvious claim 1.

1. [1p] An enhancement-mode GaN transistor, comprising:

[108] *Saxler* discloses or at least renders obvious the preamble. *Saxler* discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer. *Saxler*, [0007]-[0010], [0046], [0059]-[0064], Figs. 1A, 1B. Although Saxler does not use the phrase "enhancement mode," this transistor indeed constitutes a normally-off enhancement-mode GaN transistor when these p-type dopants are placed in the cap layer, as *Saxler* discloses. *Id.*

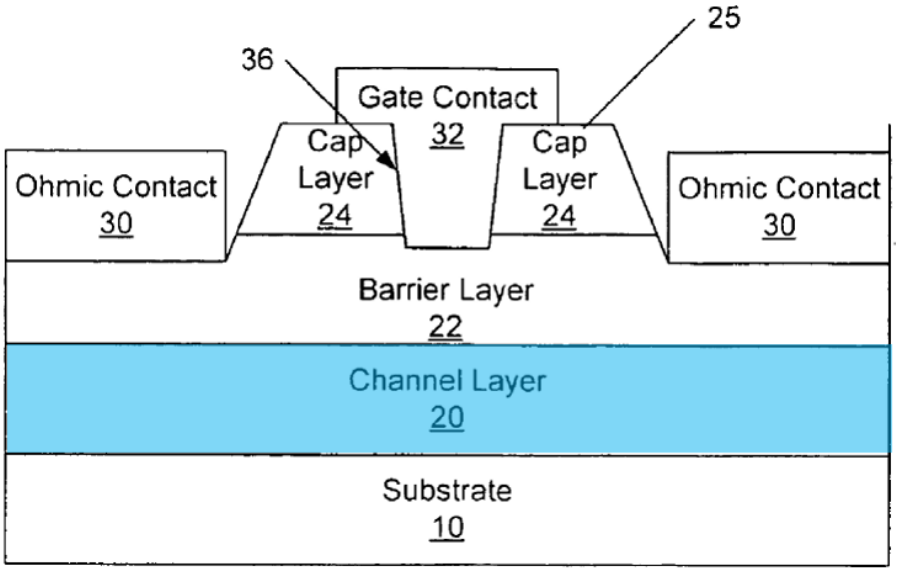
[109] A POSITA would have understood *Saxler*'s transistors were enhancement-mode GaN transistors at least because of their gate structure, which is one of the defining features of enhancement-mode transistors. For example, *Sheppard*, which *Saxler* expressly incorporates (*Saxler*, [0046], [0068], (referencing Ser. No. 10/897,726)), likewise discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer, where the cap layer "moves the top surface of the device physically away from the channel, which may reduce the effects of the surface," and when the

cap layer is doped p-type this will constitute a normally-off enhancement-mode GaN transistor. *Sheppard*, [0014], [0040], [0042], Fig. 1F.

2. [1a] a GaN layer;

[110] As an initial matter, the '335 patent admits Limitation [1a] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B. I agree.

[111] *Saxler* discloses a **GaN channel layer** (Grounds 1-2). *Saxler*, [0007], [0010], [0016], [0058], [0069], Figs. 1A-1F.

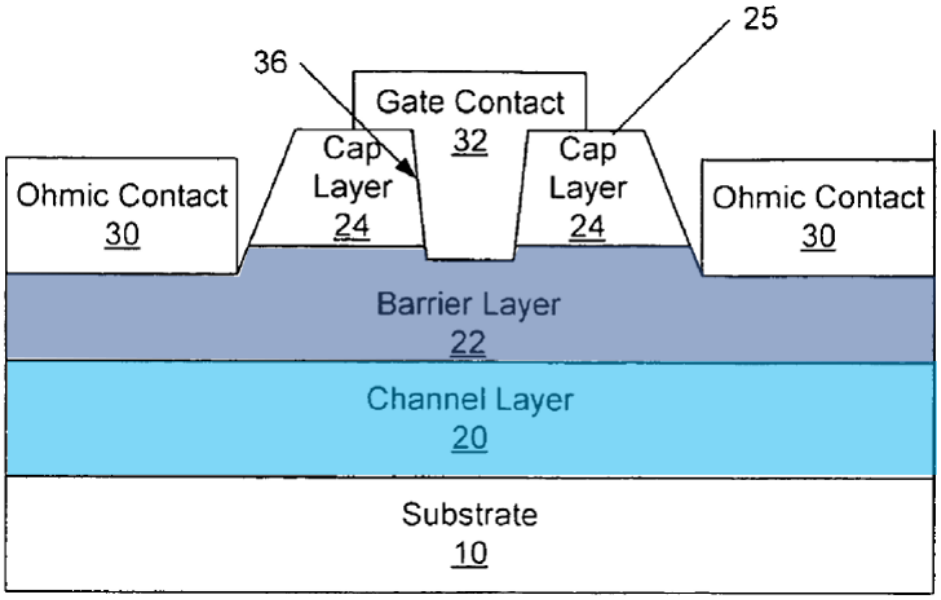


Saxler, Fig. 1A.

3. [1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[112] The '335 patent also admits Limitation [1b] was conventional, and I agree. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B.

[113] *Saxler* discloses Limitation [1b] (Grounds 1-2). *Saxler*'s **barrier layer 22** is disposed on its GaN **channel layer**. *Saxler*, Abstract, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B.



Saxler, Fig. 1A.

[114] *Saxler*'s states that its barrier layer may be an AlGaN layer. *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B. And the '335 patent

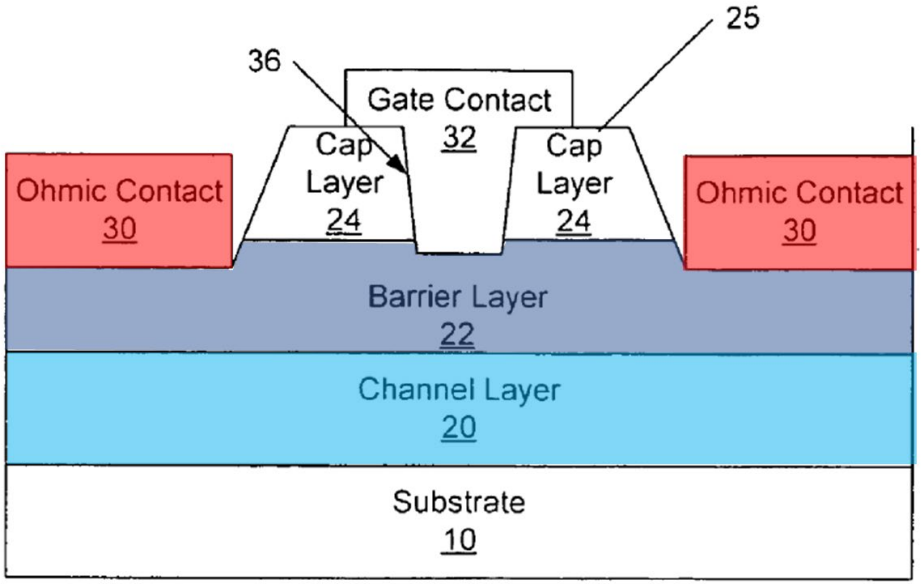
barrier layer of the ’335 patent may also be an AlGaN layer, in embodiments that the dependent claims cover. Ex. 1001, 1:42-63, 3:37-48, 4:16-22, claims 3, 6.

[115] *Saxler* further discloses “induc[ing] a **two-dimensional electron gas**” at the interface of the first GaN layer and second AlGaN layer, which was typical for such devices. *Saxler*, [0004], [0059] (“induce a significant carrier concentration at the interface between the channel layer 20 and the barrier layer 22”).

4. [1c]: a source contact and a drain contact formed on the barrier layer;

[116] Again, the ’335 patent admits Limitation [1c] was conventional, and I agree. Ex. 1001, 1:64-2:19, Figs. 1-2, 3A-3B.

[117] Such source and drain contacts were wholly conventional in GaN transistors, and *Saxler* discloses “ohmic contacts 30” that may “provide **source** and **drain contacts**” formed on barrier layer 22 (Grounds 1-2). *Saxler*, [0065], Figs. 1A, 2B.



Saxler, Fig. 1A.

5. [1d]: a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

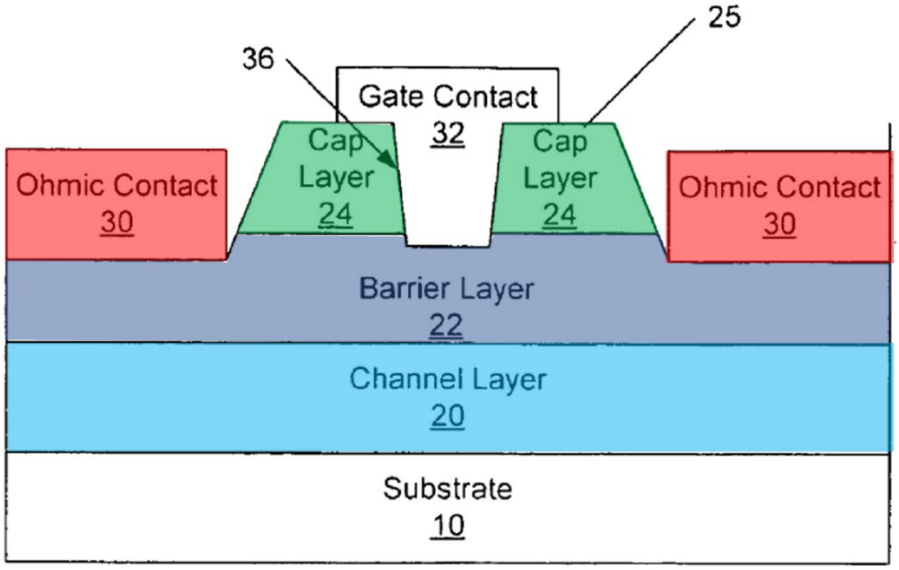
[118] The ’335 patent further admits Limitation [1d] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B. I agree.

[119] *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2) renders obvious Limitation [1d] under either parties’ construction of the side surfaces limitation.

[120] Under Ground 1, *Saxler*’s **cap layer** discloses a p-type gate material. *Saxler*, [0013], [0069], [0071], [0073]. The **cap layer** resides above an AlGaN

barrier layer, as claim 1 of the '335 patent requires. *Saxler*, [0010], [0059]-[0063], Figs. 1A, 2B.

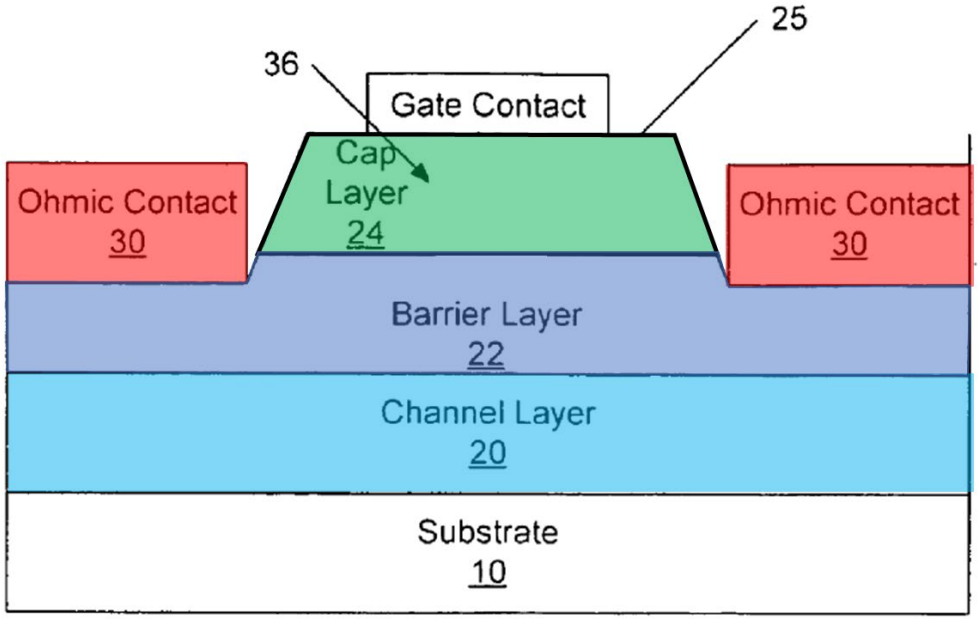
[121] *Saxler*'s **cap layer** also has side surfaces extending horizontally towards the **source** and **drain contact**, and the **cap layer** contacts the **barrier layer**, as I show in the annotated figure below. *Saxler*, [0064], Figs. 1A, 2B.



Saxler, Fig. 1A.

[122] *Saxler* discloses "***a*** p-type gate material … having side surface**s**" as recited in claim 1. Although *Saxler*'s figures show the gate recess separating the **cap layer** into two portions, the recess is optional and even when present does not necessarily extend through the **cap layer** into the **barrier layer**. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88. In my opinion, *Saxler* thus discloses or at least renders obvious a single p-

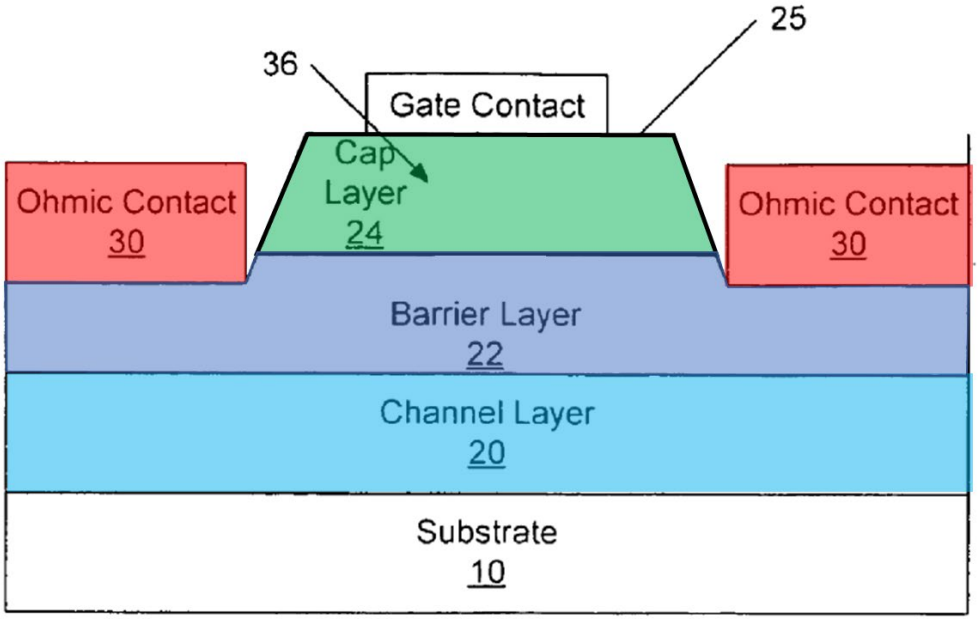
type gate material having two side surfaces that extend horizontally towards the source and drain.



Saxler, Fig. 1A (modified).

[123] Although it is my opinion that *Saxler* discloses or at least renders obvious Limitation [1d] (Ground 1), Patent Owner may incorrectly argue that *Saxler* does not disclose this limitation because its figures only include embodiments wherein the **cap layer** is separated into two portions and does not show a single p-type gate material having side surfaces extending towards the source and drain (as in the non-recessed embodiments or when the recess does not extend into the **barrier layer**). Regardless, the *Saxler-Yoshida* combination of Ground 2 renders this limitation obvious. It would have been obvious to combine

Saxler and *Yoshida*, resulting in the same figure as the *Saxler* non-recessed embodiment. §X.A.4 (Ground 2, Motivation to Combine).

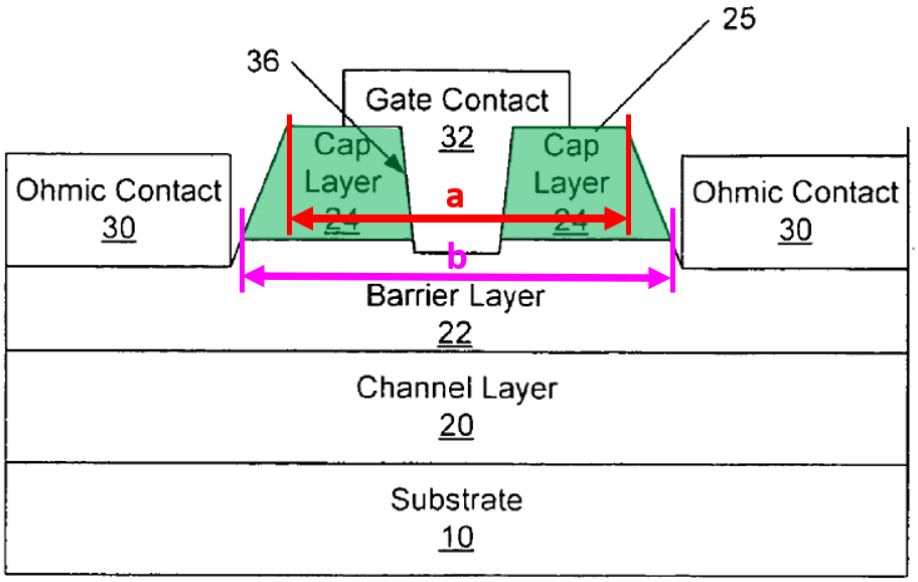


Saxler, Fig. 1A (modified).

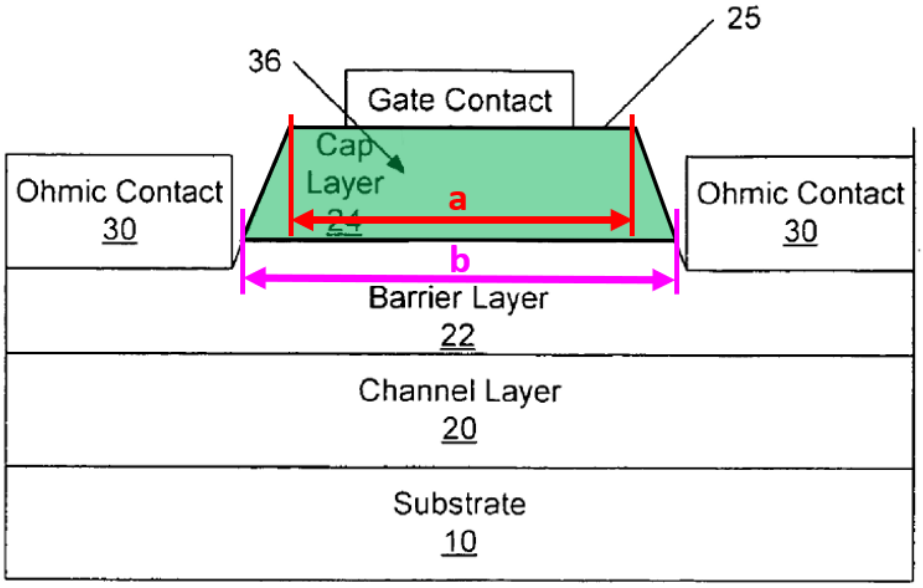
Mapping Under Petitioners' Construction

[124] Both *Saxler* alone (Ground 1) or *Saxler-Yoshida* in combination (Ground 2) discloses and renders obvious side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer, which is Petitioner's construction. §IX.A (Claim Construction). In either the recess or non-recess *Saxler* embodiments, the bottom of the **cap layer** (length "**b**," below)

is about 1.25 times wider than the top (length "**a**"), i.e. more than 10% wider (Ground 1).

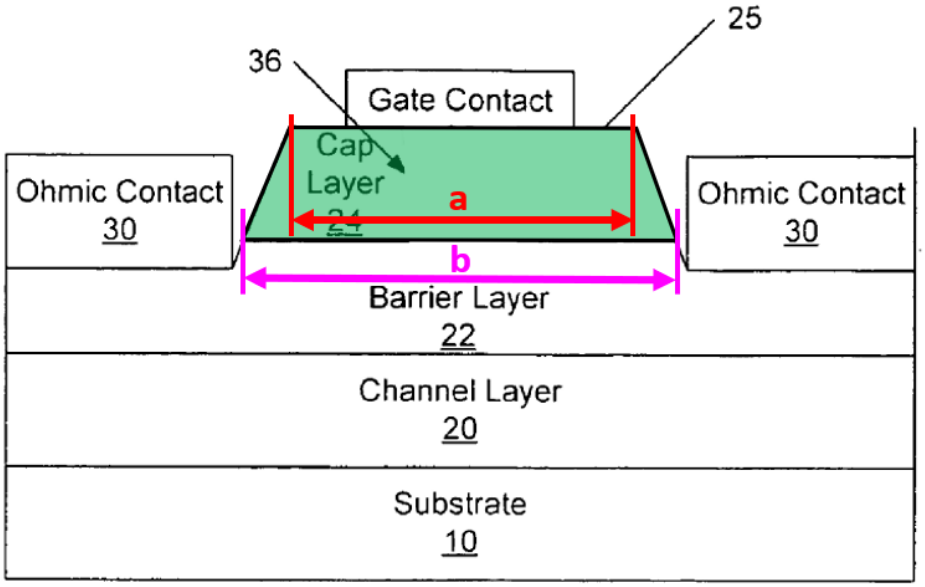


Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

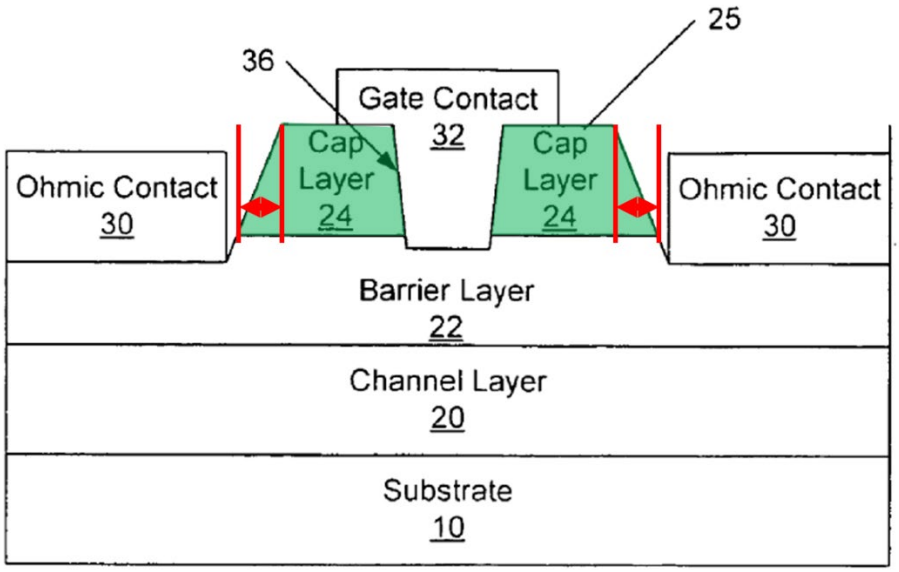
[125] Likewise, in *Saxler-Yoshida*, the bottom of the **cap layer** (length "**b**," below) is more than 10% wider than the top (length "**a**") (Ground 2) (approximately 1.25 times wider).



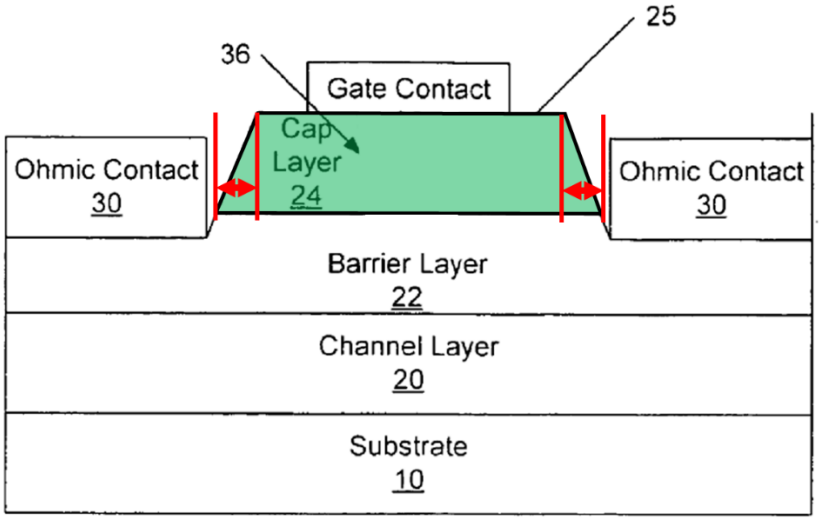
Saxler, Fig. 1A (modified).

Mapping Under Patent Owner's Construction

[126] Both *Saxler* alone (Ground 1) or the *Saxler-Yoshida* in combination (Ground 2) discloses and renders obvious side surfaces of the p-type gate material *such that the bottom of the material is wider than the top of the material* under Patent Owner's construction.



Saxler, Fig. 1A.

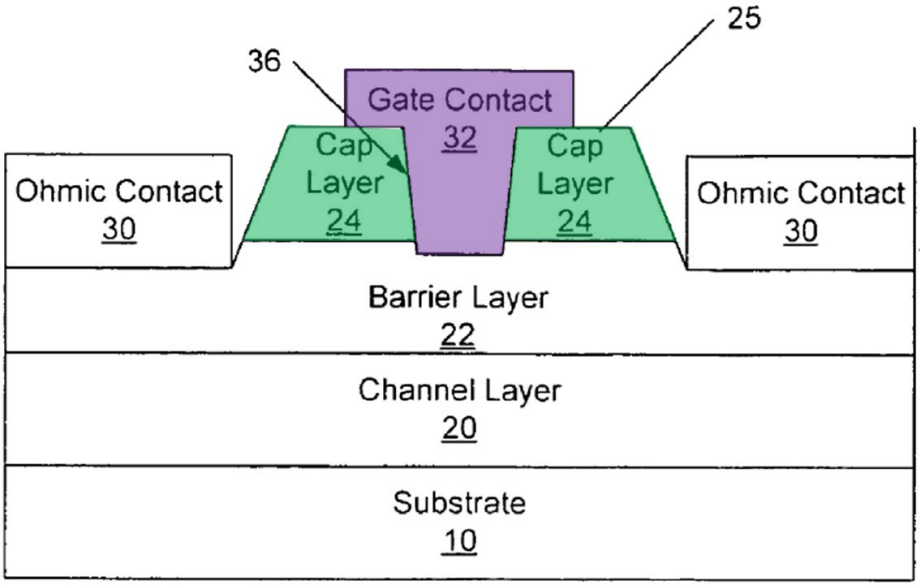


Saxler, Fig. 1A (modified).

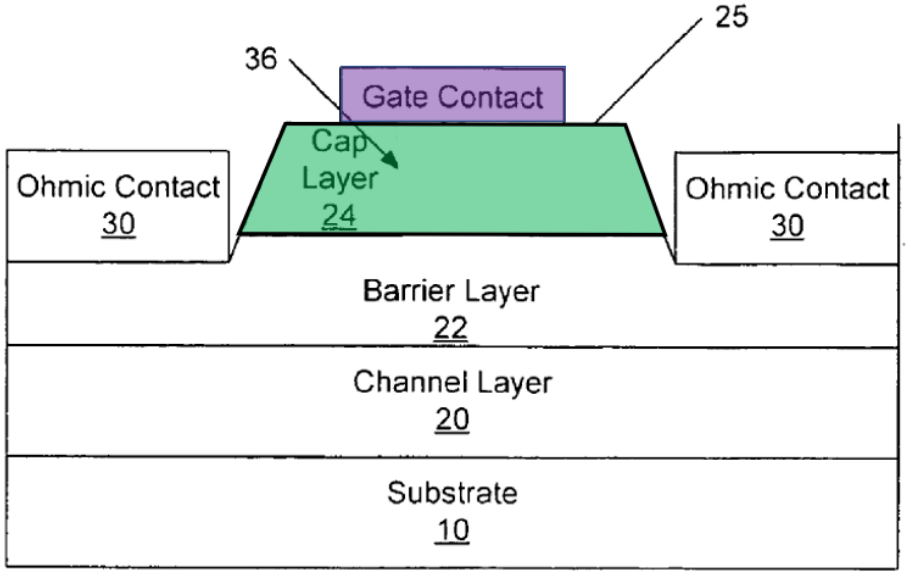
6. [1e]: a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

[127] As with the other limitations, the patent also admits Limitation [1e] was conventional and depicts numerous prior art devices disclosing it. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A. I agree.

[128] In my opinion, *Saxler* alone renders obvious Limitation [1e] (Ground 1). *Saxler*'s **gate contact** is a gate metal (e.g., "Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WSiN") and it is formed on its **cap layer**. *Saxler*, [0066], Figs. 1A, 2B. As I explained above, in some embodiments *Saxler* lacks a gate recess and does not separate the **cap layer** into distinct portions. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; §X.B.5 (Grounds 1-2, Limitation [1d]). In all of *Saxler*'s embodiments, the sidewalls of its **gate contact** extend vertically towards the **cap layer** just as in the recessed embodiments depicted in Figures 1A and 2B.



Saxler, Fig. 1A.

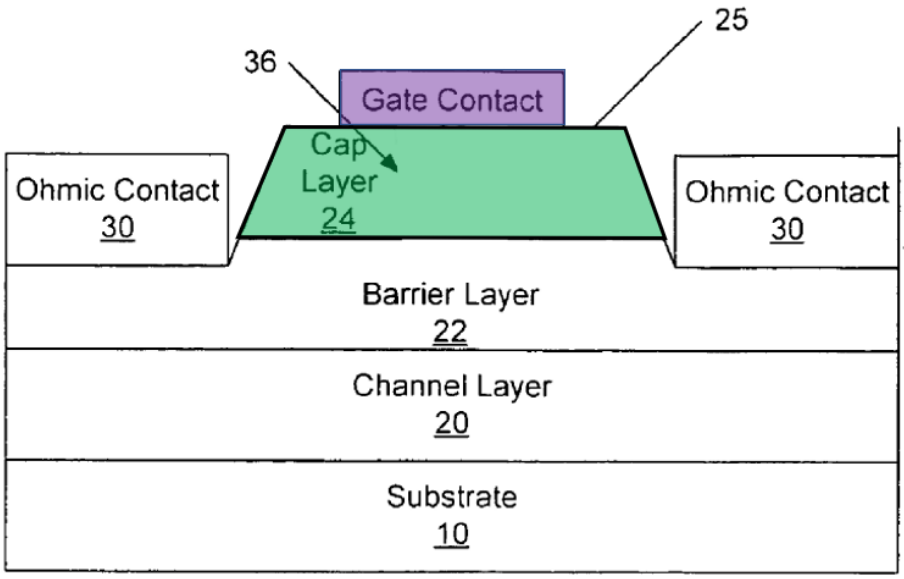


Saxler, Fig. 1A (modified).

[129] In addition, *Saxler* in view of *Yoshida* also renders obvious Limitation [1e] (Ground 2). Both *Saxler*'s gate contact and *Yoshida*'s **gate**

electrode are metals formed on the **cap layer** and p-type GaN **layer 5**, respectively. *Yoshida*, [0016]; §XII.C.6 (Grounds 1-2, Limitation [1e]). It would have been for a POSITA to select a suitable metal for the combined *Saxler-Yoshida* system. Gates were conventional in GaN HEMTS and both references include them. A POSITA would have selected a metal for the gate as a simple design choice, depending on the properties of the system. *Yoshida*, [0002]-[0006], [0016] (disclosing "Au/Pt, Al, and the like" as examples of *Yoshida*'s gate electrode).

[130] Further, the sidewalls of *Saxler-Yoshida*'s **gate contact** extend towards the **cap layer**, as required by Limitation [1e] and shown below. *Yoshida*, Fig. 1; *Saxler*, Fig. 1F.



Saxler, Fig. 1A (modified).

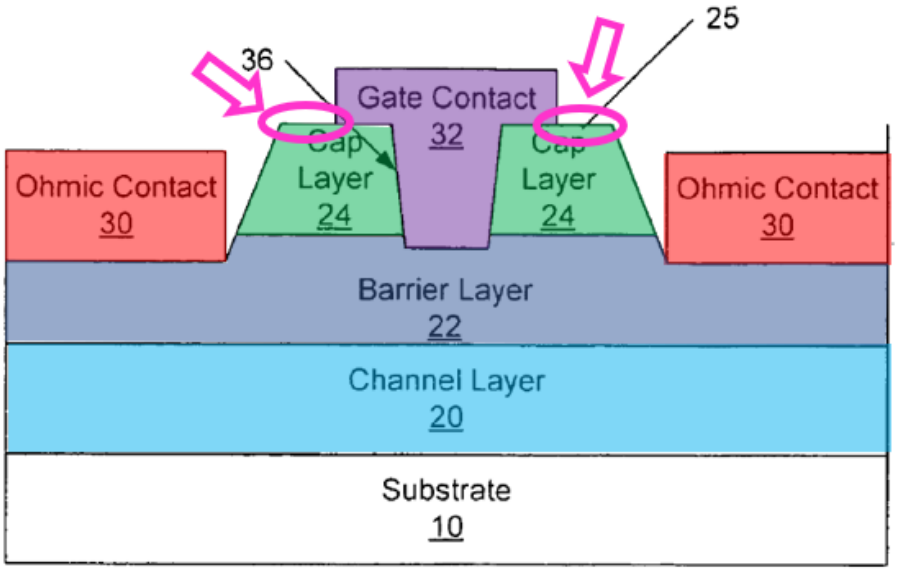
7. [1f]: wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

[131] Limitation [1f] is the only limitation of independent claim 1 that the '335 patent does not admit is found in the prior art. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A. In my opinion, *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2) renders it obvious.

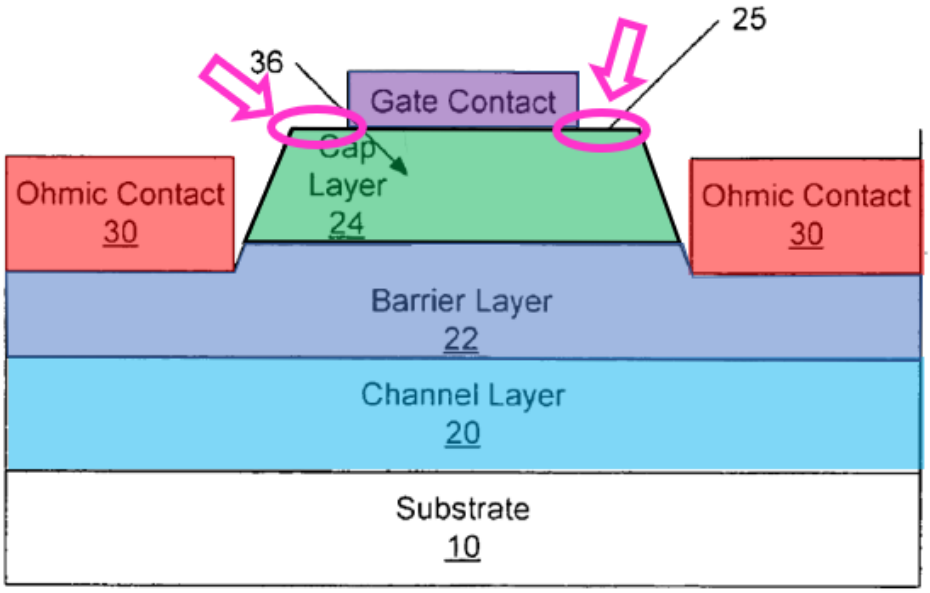
[132] This limitation was conventional. Even the priority application *Lidow* agrees, noting that ledges in a "conventional enhancement mode transistor" are made using separate masks for the p-type gate material and gate metal. *Lidow*, [0006], Fig. 1.

[133] *Saxler* discloses this limitation (Ground 1). Its **gate contact** is narrower than its **cap layer**, which exposes **horizontal ledges** with substantially equal widths that extend past the respective sidewalls of the **gate** and toward the **source** and **drain**, as I have indicated in Figure 1A below. *Saxler*, Fig. 1A. In some embodiments, *Saxler*'s gate recess is not present or does not separate the **cap layer** into distinct portions. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; §X.B.5 (Grounds 1-2,

Limitation [1d]). A POSITA would have understood *Saxler*'s **gate contact** in non-recessed embodiments (or embodiments where the recess did not extend through the **cap layer**) would similarly be narrower than the **cap layer** to expose the **horizontal ledges**. *Saxler* thereby discloses or at least renders Limitation [1f] obvious (Ground 1).

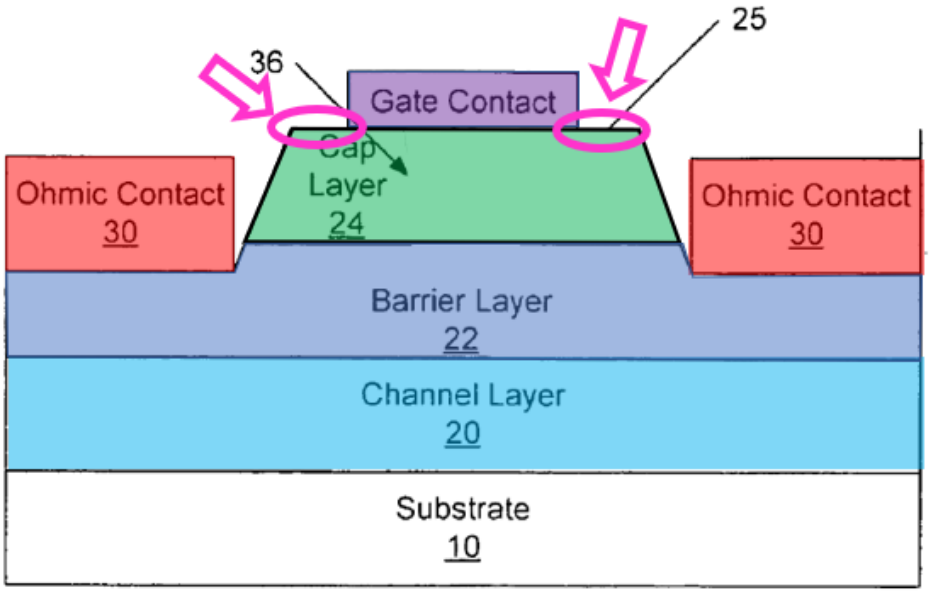


Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

[134] In my opinion, *Saxler* in view of *Yoshida* also renders obvious Limitation [1f] (Ground 2). *Saxler-Yoshida*'s **gate contact** is narrower than its **cap layer**, which creates symmetric **horizontal ledges** that extend past the sidewalls of the **gate** and toward the **source** and **drain**. *Yoshida*, [0022]-[0023], Fig. 1; *Saxler*, [0046], Figs. 1A-1F. These symmetric **ledges** have substantially equal widths, as shown below.



Saxler, Fig. 1A (modified).

C. [Claim 2]: wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

[135] Claim 2 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 2 is thus drawn a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim Construction). So for reasons I explained above for Limitation [1f], claim 2 is obvious over *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2). §X.B.7 (Grounds 1-2, Limitation [1f]).

D. [Claim 3]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

[136] As I explained above for Limitation [1b], *Saxler* discloses that its barrier layer is an AlGaN material. *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B]; §X.B.3 (Grounds 1-2, Limitation [1b]). Claim 3 is accordingly obvious over *Saxler* alone and/or in view of *Yoshida* (Grounds 1-2).

E. [Claim 4]: wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width

[137] Claim 4 only requires that the gate metal is narrower than the p-type gate material, but this feature is already required by Limitation [1f] to form the horizontal ledges under either Party's construction. As I explained for Limitation [1f], *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2) renders obvious this arrangement. *Yoshida*, [0022]-[0023], Fig. 1; *Saxler*, [0014], [0046], claims 1, 18, 20, 29, Fig. 1F; §X.B.7 (Grounds 1-2, Limitation [1f]).

F. Independent Claim 5

[138] *Saxler* in view of the knowledge of a POSITA (Ground 1) and in view of *Yoshida* (Ground 2) renders obvious claim 5.

a. [5p] An enhancement-mode GaN transistor, comprising:

[139] Limitation [5p] is identical to Limitation [1p]. *Saxler* discloses or at least renders it obvious for the reasons I provided for Limitation [1p] (Grounds 1-2). §X.B.1 (Grounds 1-2, Limitation [1p]).

2. [5a] a GaN layer;

[140] Limitation [5a] is identical to Limitation [1a]. *Saxler* discloses it for the reasons I provided for Limitation [1a] (Grounds 1-2). §X.B.2 (Grounds 1-2, Limitation [1a]).

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[141] Limitation [5b] is identical to Limitation [1b]. *Saxler* discloses it for the reasons I provided for Limitation [1b] (Grounds 1-2). §X.B.3 (Grounds 1-2, Limitation [1b]).

4. [5c]: a source contact and a drain contact formed on the barrier layer;

[142] Limitation [5c] is identical to Limitation [1c]. *Saxler* discloses it for the reasons I provided for Limitation [1c] (Grounds 1-2). §X.B.4 (Grounds 1-2, Limitation [1c]).

5. [5d]: a p-type gate material formed above the barrier layer and between the source and drain contacts;

[143] *Saxler* discloses Limitation [5d] for reasons I provided for Limitation [1d] (Grounds 1-2). §X.B.5 (Grounds 1-2, Limitation [1d]). As explained, *Saxler*'s cap layer is a p-type GaN, and the cap layer is disposed between source and drain contacts. *Saxler*, [0013], [0064], [0069], [0071], [0073], Figs. 1A, 2B; §X.B.5 (Grounds 1-2, Limitation [1d]).

6. [5e]: a gate metal disposed on the p-type gate material,

[144] Limitation [5e] is included in Limitation [1e]. *Saxler* discloses Limitation [5e] for the reasons I provided for Limitation [1e] (Grounds 1-2). §X.B.6 (Grounds 1-2, Limitation [1e]).

7. [5f]: wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[145] Claim 5 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 5 thus includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim Construction). Limitation [5f] otherwise is identical to Limitation [1f]. For reasons I provided for Limitation [1f], Limitation [5f] is obvious over *Saxler* alone and/or in view of *Yoshida*. §X.B.7 (Grounds 1-2, Limitation [1f]).

[146] As I previously explained for Limitation [1f], *Saxler*'s gate contact is narrower than the underlying cap layer, which creates horizontal ledges that extend past sidewalls of the gate metal towards the source contact and drain contact. *Saxler*, [0064]-[0066], Figs. 1A-1B, 2B; §X.B.7 (Grounds 1-2, Limitation [1f]). And as I also previously explained, the combination of *Saxler* and *Yoshida* also includes these features. §§X.A (Overview of Grounds 1-2), X.A.4 (Ground 2, Motivation to Combine), X.B.7 (Grounds 1-2, Limitation [1f]).

8. [5g]: (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

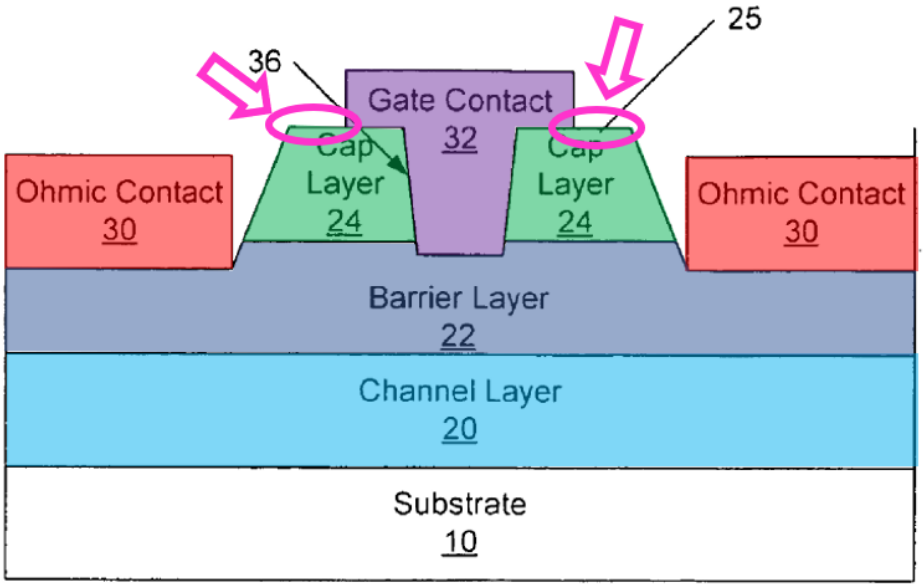
[147] Limitation [5g] is identical to Limitation [1d]. For reasons I provided for Limitation [1d], *Saxler* in view of the knowledge of a POSITA (Ground 1) and in view of *Yoshida* (Ground 2) renders obvious Limitation [5g]. §X.B.5 (Grounds 1-2, Limitation [1d]).

G. [Claim 6]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

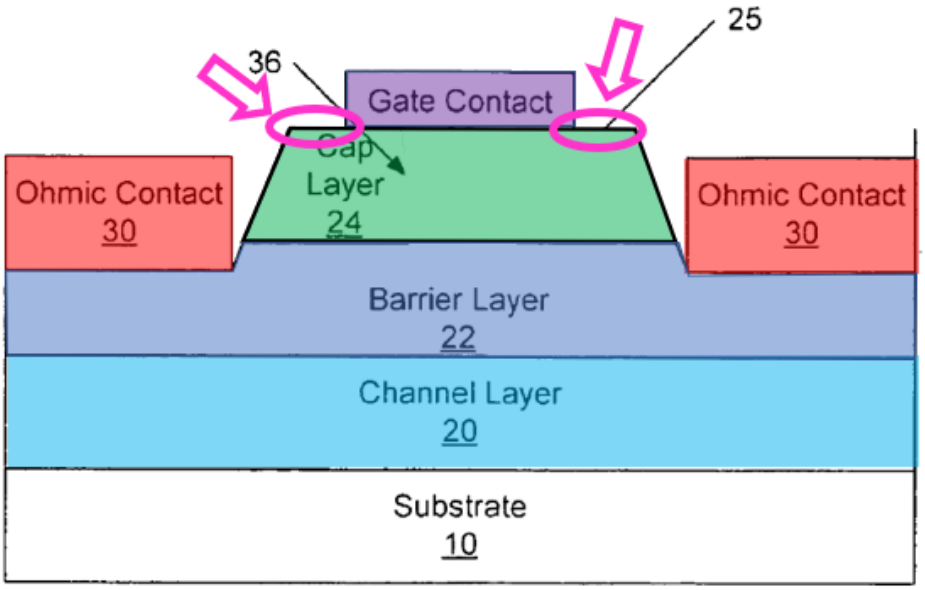
[148] Claim 6 is obvious over *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2). As I explained for Limitation [1b], *Saxler* discloses an AlGaN barrier layer (Grounds 1-2). *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B; §§X.B.3 (Grounds 1-2, Limitation [1b]), X.D (Grounds 1-2, Claim 3).

H. [Claim 7]: wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

[149] As I explained for Limitation [1d] and Limitation [1f], *Saxler* discloses **symmetric ledges** of its **cap layer** on either side the **gate contact**, including in embodiments where the cap layer is not recessed or only partially recessed. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88, Figs. 1A, 2B; §§X.B.5 (Limitation [1d]), X.B.7 (Limitation [1f]). *Saxler* alone thus renders obvious claim 7 (Ground 1).

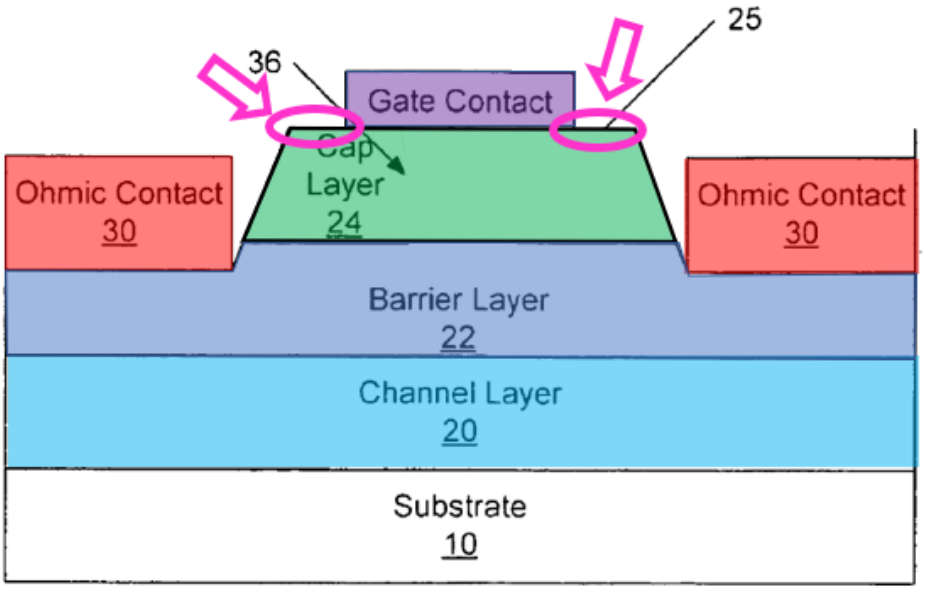


Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

[150] In addition, *Saxler-Yoshida* includes these features (Ground 2) as shown below and as previously explained. §X.B.7 (Grounds 5, Limitation [1f]).



Saxler, Fig. 1A (modified).

XI. GROUND 3: *SAXLER* IN VIEW OF *YOSHIDA*, *BEACH*, AND *SHENOY* RENDERS OBVIOUS CLAIMS 2 AND 5-7

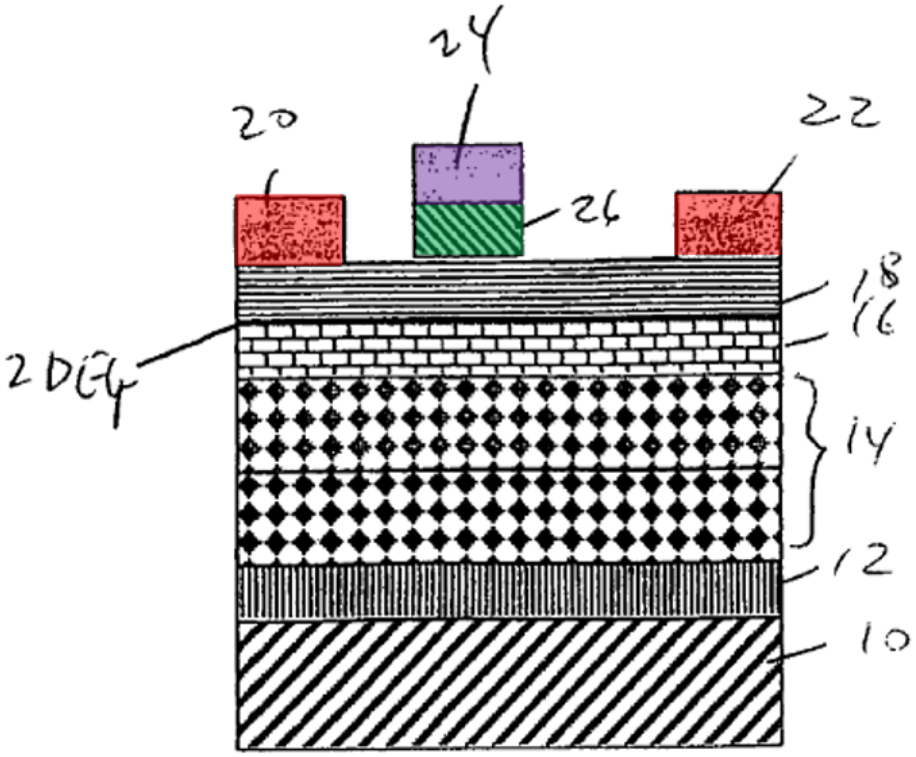
A. Overview of Ground 3

[151] As I explained, the claim term "self-aligned" refers to how the claimed ledges are made, not what they are, and counsel has informed me that this term thus lends no patentable weight. §§IX.B, X.C, X.F.7. But to the extent Patent Owner disagrees that the "self-aligned" recitations of claims 2 and 5 are product-by-process elements that have no patentable weight (§§IX.B, X.C, X.F.7), the combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* uses a self-aligned process to create the non-recessed gate structure of *Saxler* alone or *Saxler-Yoshida* and therefore renders obvious claims 2 and 5-7.

1. *Beach*

[152] *Beach* describes GaN enhancement-mode devices. *Beach*, Abstract, [0003]-[0018]. *Beach* uses a self-aligned method to make stacked gate structures in GaN HEMT devices that relies on using just one mask, a well known approach at the time. *Id.*, [0040], [0045], [0054]. *Beach* provides steps to deposit and pattern these layers with a single mask to make a **gate barrier 26** and **gate arrangement 24** above a p-n junction and between **power electrodes**, as I have illustrated below in color coded shading. *Beach*, [0040]. These self-aligned techniques were

common in the field as of relevant date for the ’335 patent. *Beach*’s “gate arrangement 24” includes a **gate electrode**, which is a metal, and **gate barrier 26**, which is a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F.



Beach, Fig. 1.

2. *Shenoy*

[153] *Shenoy*, which published February 22, 1996, well over a decade before the ’335 patent’s asserted priority date of April 8, 2009, describes well known techniques of using isotropic etching to undercut the metal below photoresist masks. *Shenoy*, 2-3. *Shenoy* provides method to control the “**undercut U**,” illustrated in Figure 1, which evolves symmetrically on both sides of a

symmetric photomask such that the width of the etched metal structure is less than the photomask. *Shenoy*, 2-3. *Shenoy*'s methods were conventional for etching metals in semi-conductors as of the relevant date of the '335 patent.

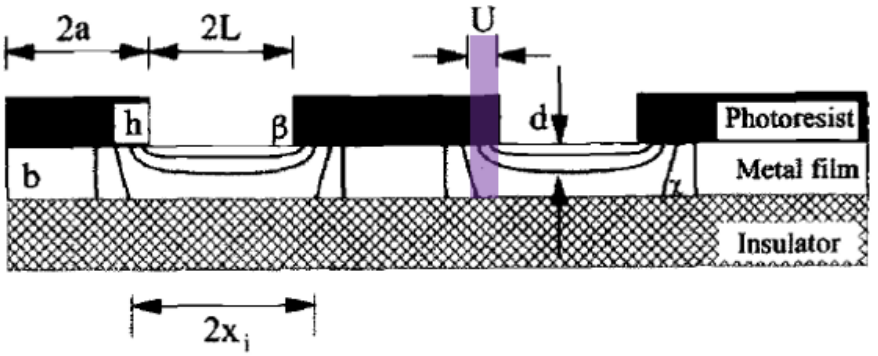


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

Shenoy, Fig. 1.

[154] At least as of April 8, 2009, and as early as its publication date of February 22, 1996, I understand that *Shenoy* was publicly available and disseminated. *See Shenoy*, 1; Ex. 1025 (Declaration of Kelley Hazel). In my opinion, a POSITA designing GaN transistors routinely would have accessed similar scholarly articles and would have looked to *Shenoy* for its techniques of etching metals.

3. Motivation to Combine

[155] In my opinion, a POSITA would have found it obvious to make *Saxler-Yoshida*'s stacked gate structure consisting of a cap layer and gate contact

using the methods of *Beach* and *Shenoy*. §X.A.4 (Ground 2: Motivation to Combine).

[156] The *Saxler-Yoshida* combination describes a sequence of steps to arrive at its stacked gate structure which were typical for GaN HEMT devices. Specifically, *Saxler*'s process includes: (i) forming cap layer 24 on the barrier layer (*Saxler*, [0061], Fig. 1B); (ii) masking and etching the cap layer "to expose the underlying barrier layer 22," for formation of ohmic contacts 30, which creates sloped sidewalls of the cap layer (*id.*, [0064], Figs. 1A-1B); (iii) patterning to deposit the ohmic contacts (*id.*); (iv) removing the mask in non-recessed embodiment or optionally using a second mask to etch and form a gate recess (*id.*, [0065]); (v) removing the mask (*id.*, [0064]-[0066]); and (v) forming a gate contact (*id.*, [0066]).

[157] In addition, *Sheppard*, incorporated by *Saxler* to disclose methods of fabricating *Saxler*'s GaN HEMTs (*Saxler*, [0046], [0068]), describes a similar process. *Sheppard*, [0044]-[0051], Figs. 1A-1F.

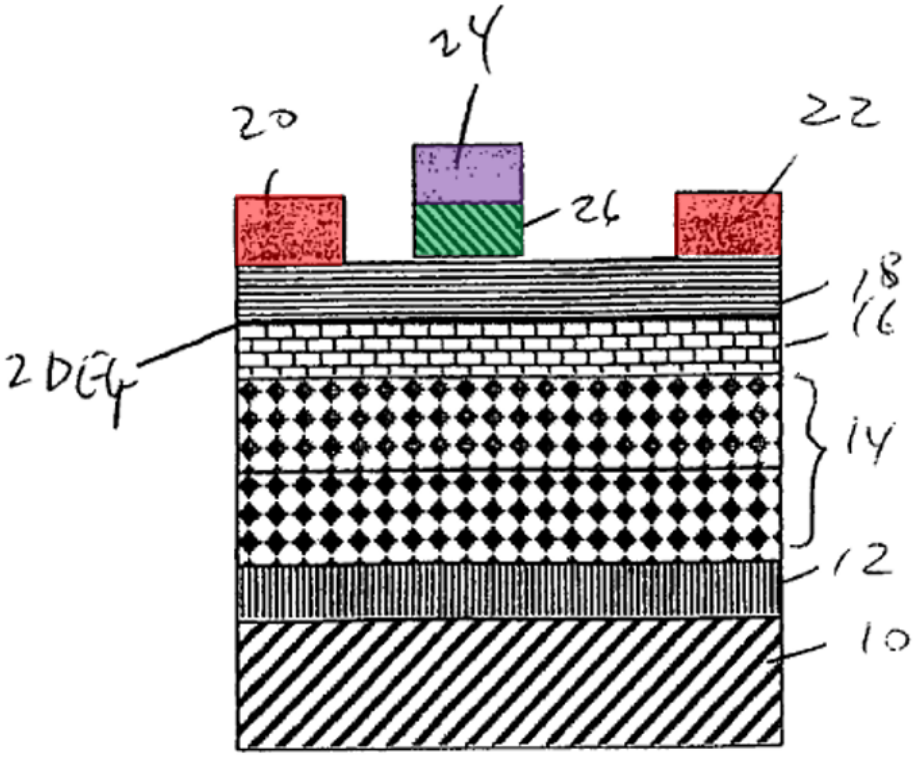
[158] In the *Saxler-Yoshida* combination, step (iv) above would employ the non-recessed option. §X.A.4 (Ground 2: Motivation to Combine). Then, to reliably locate the gate metal, a POSITA would have understood a second patterning step would have been performed, and that second mask would be removed. In my

opinion a POSITA would have been motivated to modify this process by using fewer masking steps which would simplify the process and reduce costs. *Id*.

[159] There were numerous techniques available and known to a POSITA to make *Saxler-Yoshida*'s stepped gate structure, and a POSITA would have used these methods interchangeably. § VIII (Technology Background, discussing common methods to create stepped gate structures). In my opinion, to make *Saxler-Yoshida*'s selfsame gate structure with improved reproducibility and symmetry of the gate contact with respect to the cap layer, a POSITA would have found it obvious to modify *Saxler-Yoshida* by using *Beach*'s self-aligned technique and *Shenoy*'s isotropic etching. This approach was known for making stepped gate structures—*Ahn* uses it in a thin-film transistor. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C. And an additional reason that a POSITA would have been motivated to use this approach would be to reduce masking steps and reduce costs.

[160] As I explained above, *Beach* provides a method of making stacked gate structures in GaN HEMT devices that uses a single mask, which helps ensure alignment of layers. *Beach*, [0040], [0045], [0054]; *Beach-II*, [0047]-[0048]. *Beach*'s gate structure includes the "gate arrangement 24," which includes a gate electrode and an underlying "gate barrier 26," which is a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F. *Beach*'s process (i) deposits "**gate**

barrier 26" and "**gate arrangement 24**" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits **power electrodes**. *Beach*, [0040]. Such self-aligned techniques were common in the field as of relevant date.



Beach, Fig. 1.

[161] In my opinion, a POSITA would have found it obvious to use *Beach*'s approach to create *Saxler-Yoshida*'s gate structure, which would have improved alignment between layers, reduced steps, and reduced costs. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3. It would have been obvious at the time to look to *Beach* for its simple methods of making stacked gate structures. Indeed, *Sheppard*, expressly incorporated by *Saxler* to disclose methods of fabricating GaN HEMTs (*Saxler*,

[0046], [0068]), describes using a flexible approach to masking and etching, which was typical for how POSITAs would have made GaN transistors at the time. *Sheppard* notes that "operations described as multiple steps could be combined into a single step" and vice versa, making the choice of *Beach*'s manufacturing steps no more than simple substitutions. *Sheppard*, [0058].

[162] *Beach*'s gate structure is not stepped, and it does not disclose creating the **horizontal ledges** of *Saxler-Yoshida*'s stepped, stacked gate structure following a self-aligned process. But as I previously explained, *Shenoy* discloses simple, long used, and common isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks. *Shenoy*, 2-3; §XI.A.2 (*Shenoy*).

[163] A POSITA would have found it obvious to integrate these techniques into *Saxler*'s flexible manufacturing approach. *Saxler* describes using several conventional techniques to etch the cap layer and generate the slope sidewalls shown in their figures. *Saxler*, [0064], Figs. 1A-1B. So does *Sheppard*, incorporated into *Saxler* by reference to disclose methods of forming gate structures (*Saxler* [0046] (referencing Ser. No. 10/897,726), [0068] (same)). *Sheppard*, [0044], Figs. 1B-1C.

[164] In my opinion, a POSITA would have found it obvious to use *Beach*'s self-aligned method of making *Saxler-Yoshida*'s stacked gate structure in a GaN

HEMT and to use *Shenoy*'s methods to undercut the **gate electrode** and create *Saxler-Yoshida*'s **horizontal ledges** and **slope cap** layer. This combination of steps was already known in the art for creating stepped, stacked transistor gates. *Ahn*. A POSITA would have found the combination a simple substitution of *Beach*'s and *Shenoy*'s known methods that could be predictably implemented in *Saxler*'s flexible method of manufacturing to improve alignment and symmetry between layers and reduce steps and costs. *Saxler*, [0046], [0068]; *Sheppard*, [0058].

B. [Claim 2] The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

[165] Claim 2 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 2 is thus drawn a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim Construction). But in my opinion, the combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* nevertheless render obvious claim 2, even if it did lend patentable weight.

[166] *Beach* discloses a stacked "***self-aligned*** gate arrangement" using a single photo mask to etch both the "gate arrangement 24" (gate electrode) and the underlying "gate barrier 26" (GaN semiconductor) that is the same process depicted in the '335 patent at Figures 6A-6B. *Beach*, [0032]-[0033], [0040],

Figs. 1, 2E-2F; Ex. 1001, 4:14-26; §§[044] ('335 Patent Overview), XI.A.1 (Ground 3, *Beach*), XIII.A.1 (Ground 3, Motivation to Combine), XIII.B (Ground 3, Claim 2), XI.A.3 (Ground 3, Motivation to Combine).

[167] Then, as I have already explained, *Shenoy* discloses etching a photomask to isotropically undercut the metal layer below the photomask that is the same process depicted in Figures 6B-6C of the '335 patent. *Shenoy*, 2-3; Ex. 1001, 4:23-39; §§[044] ('335 Patent Overview), XI.A.2 (Ground 3, *Shenoy*), XIII.A.1 (Ground 3, Motivation to Combine), XIII.B (Ground 3, Claim 2), XI.A.3 (Ground 3, Motivation to Combine).

[168] In my opinion, it would have been obvious to use *Beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make the gate structure of *Saxler*-*Yoshida*. §XI.A.3 (Ground 3, Motivation to Combine). That approach involved simple substitutions of known manufacturing techniques that could be implemented in *Saxler*'s flexible method of manufacturing. §XI.A.3 (Ground 3, Motivation to Combine).

C. Independent Claim 5

[169] The combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* renders obvious claim 5.

1. [5p] An enhancement-mode GaN transistor, comprising:

[170] As I explained in Grounds 1-2, *Saxler* discloses Limitation [1p]. §X.F.a (Grounds 1-2, Limitation [5p]).

2. [5a] a GaN layer;

[171] As I explained in Grounds 1-2, *Saxler* discloses a GaN layer. §X.F.2 (Grounds 1-2, Limitation [5a]).

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[172] As I explained in Grounds 1-2, *Saxler* discloses Limitation [5b]. §X.F.3 (Grounds 1-2, Limitation [5b]).

4. [5c] a source contact and a drain contact disposed on the barrier layer;

[173] As I explained in Grounds 1-2, *Saxler* discloses Limitation [5c]. §X.F.4 (Grounds 1-2, Limitation [5c]).

5. [5d] a p-type gate material formed above the barrier layer and between the source and drain contacts;

[174] As I explained in Grounds 1-2, *Saxler* alone and/or in combination with *Yoshida* discloses Limitation [5d]. §X.F.5 (Grounds 1-2, Limitation [5d]).

6. [5e] and a gate metal disposed on the p-type gate material,

[175] As I explained in Grounds 1-2, *Saxler* alone and/or in combination with *Yoshida* discloses Limitation [5e]. §X.F.6 (Grounds 1-2, Limitation [5e]).

7. [5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[176] Claim 5 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that Limitation [5f] thus includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim Construction). But in my opinion, the combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* nevertheless render obvious Limitation [5f], even if it did lend patentable weight.

[177] As I explained in Grounds 1-2, *Saxler* alone and/or in combination with *Yoshida* includes the structural features of Limitation [5f]. §X.F.7 (Grounds 1-2, Limitation [5f]). And as I explained in Ground 3, the *Saxler*-*Yoshida* combination in view of *Beach* and *Shenoy* discloses that these ledges are self-aligned, as claimed. §X.F.7 (Grounds 1-2, Limitation [5f]).

8. [5g] side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

[178] *Saxler* alone and/or in view of *Yoshida* discloses Limitation [5g] for reasons I provided for Grounds 1-2. §X.F.8 (Grounds 1-2, Limitation [5g]).

D. [Claim 6] The enhancement-mode GaN transistor according to claim 5, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

[179] *Saxler* discloses claim 6 for reasons I provided for Grounds 1-2. §§X.B.3 (Grounds 1-2, Limitation [1b]), X.C (Grounds 1-2, Claim 2), X.G (Grounds 1-2, Claim 6).

E. [Claim 7] The enhancement-mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

[180] *Saxler* alone and/or in view of *Yoshida* includes the features of claim 7 for reasons I explained for Grounds 1-2. §X.H (Grounds 1-2, claim 7).

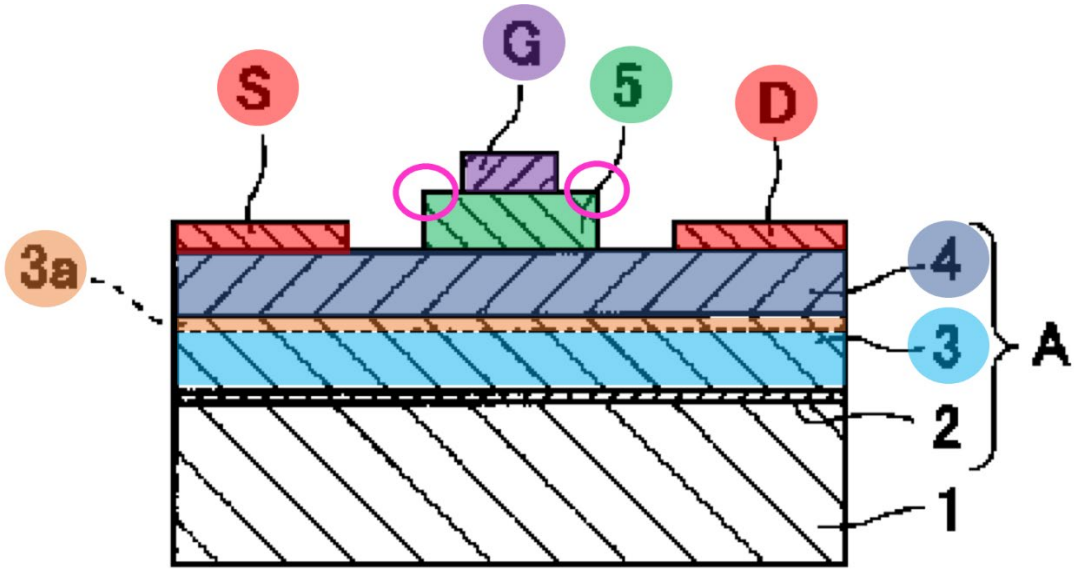
[181] Further, as I explained above, *Beach*'s method of self-aligning the gate structure in combination with *Shenoy*'s methods of symmetrically undercutting the gate metal would have yielded symmetric ledges in the *Saxler-Yoshida* device. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3; §§XI.A.3 (Ground 3, Motivation to Combine), XI.B (Ground 3, Claim 2).

XII. GROUNDS 4 AND 5: *YOSHIDA*, EITHER ALONE OR IN VIEW OF *SAXLER* RENDERS OBVIOUS CLAIMS 1-7

A. Ground 4: *Yoshida* Alone

[182] *Yoshida* discloses the arrangement of semiconductor layers and structures of claims 1-7, including the claimed ledges. Although *Yoshida* depicts that the walls of its p-type GaN material are vertical and not sloped as required by

Limitation [1d] and Limitation [5g], it is my opinion that sloped sidewalls were common and obvious over *Yoshida*, at least because perfectly vertical sidewalls were rare in practice. Under Patent Owner's construction of the slope terms ("p-type gate material having side surfaces extending horizontally such that the bottom of the material is wider than the top of the material"), a POSITA would know any device having a p-type gate material below a gate metal, as claimed, would necessarily extend at least slightly on the bottom due to manufacturing tolerances. In my opinion, *Yoshida* therefore renders obvious claim 1-7 (Ground 4) under at least Patent Owner's construction of the slope terms.



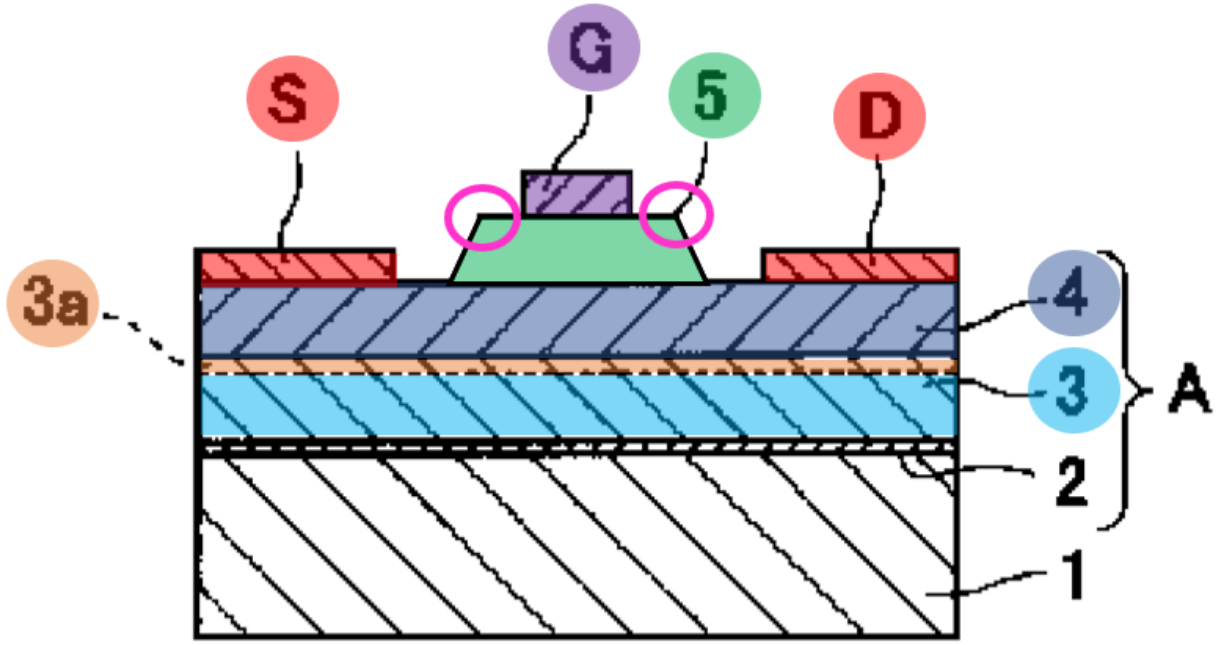
Yoshida, Fig. 1.

B. Ground 5

1. Ground 5: The Combination of *Yoshida* in View of *Saxler*

[183] To the extent Patent Owner disagrees that *Yoshida* renders obvious sidewalls of its **layer 5** that slope outwards towards the source and drain, however, *Saxler* discloses such sloped sidewalls under either Petitioner or Patent Owner's construction, and the combination of *Yoshida* and *Saxler* also renders obvious claims 1-7 (Ground 5).

[184] Implementing *Saxler*'s **sloped sidewalls** in *Yoshida*'s **layer 5** results in the following combined structure.



Yoshida, Fig. 1 (modified).

2. Ground 5: Motivation to Combine

[185] In my opinion, it would have been obvious to modify *Yoshida*'s transistor with the sloped sidewalls of *Saxler*'s capping layer to reduce gate leakage. The combination calls for nothing more than the simple substitution of *Saxler*'s sidewalls to predictably make an enhancement-mode GaN HEMT. And a POSITA would have recognized *Saxler*'s sidewalls would have reliably reduced *Yoshida*'s gate leakage, making the combination obvious.

[186] The references are analogous and compatible for the reasons I explained in Ground 2. §X.A.4 (Motivation to Combine). In view of these many similarities, a POSITA would have found it obvious to incorporate *Saxler*'s known sloped **cap layer** sidewalls into *Yoshida* p-type **layer 5**. Indeed, sloped sidewalls were conventional, as the '335 patent admits (a point with which I agree). Ex. 1001, 1:28-2:26, Figs. 1-4, 7A. For example, the '335 patent provides "conventional schematic[s] [of an] enhancement mode GaN transistor" depicting just such sloped sidewalls. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A. Further, the angle of *Saxler*'s sloped sidewall is typical for known mesa structures. *See, e.g.*, *Xu* (Figs. 1-3); *Kanda* (Fig. 1); *Widman* (Fig. 4). It would have been a simple substitution of *Yoshida*'s vertical sidewalls with *Saxler*'s sloped sidewalls to predictably yield an enhancement-mode GaN HEMT.

[187] In my opinion, a POSITA would have readily understood how to implement the combination of *Yoshida* and *Saxler*. *Saxler* discloses conventional etching techniques to straightforwardly forming its sloped sidewalls that could be used in other devices. *Saxler*, [0064]. And *Yoshida* also forms its p-type **layer 5** through etching. *Yoshida*, [0022]. It would have been a simple substitution to employ *Saxler*'s known etching approach to predictably shape *Yoshida*'s sidewalls.

[188] Accordingly, a POSITA would have recognized that *Saxler* provided a known option for shaping the sidewalls of *Yoshida*'s p-type **layer 5**, and the combination would have been obvious.

[189] It is my further opinion that a POSITA would have additionally recognized that *Saxler*'s sloped sidewalls would have beneficially reduced *Yoshida*'s leakage losses and found the combination obvious. It was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage. *Xu*, 1; *Kanda*, [0013], [0027], [0144], [0157], Fig. 12A. The '335 patent itself recognizes this basic fact, pointing out that capping structures in prior art enhancement-mode GaN transistors with sloped sidewalls had a known "gate leakage current path 201 [that] flows along the sidewall of the p-type gate material 101." Ex. 1001, 1:64-2:8, Fig. 2. A POSITA would have accordingly understood that the geometry of *Saxler*'s sloped

sidewalls provided longer leakage paths than *Yoshida*'s vertical sidewalls, thereby lowering gate leakage. *E.g.*, *Xu*, 1; *Kanda*, [0013], [0027], [0144], [0157], Fig. 12A.

C. Independent Claim 1

[190] In my opinion, *Yoshida* in view of the knowledge of a POSITA (Ground 4) under Patent Owner's construction, and *Yoshida* in view of *Saxler* (Ground 5) renders obvious claim 1, under either construction.

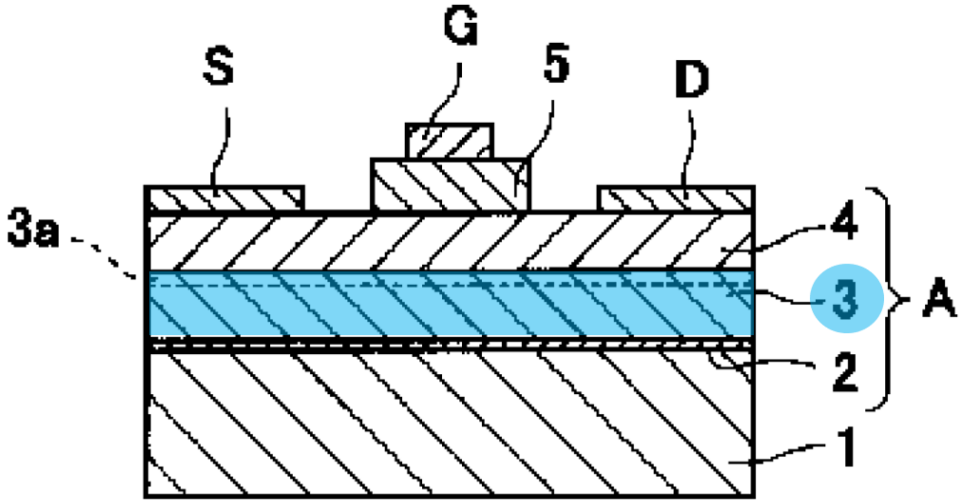
a. [1p] An enhancement-mode GaN transistor, comprising:

[191] To the extent limiting, *Yoshida* discloses the preamble (Grounds 4-5). *Yoshida* discloses a GaN high-mobility transistor that includes a p-type GaN layer below the gate, which "enables voltage control with a small amount of carrier injection." *Yoshida*, [0017], [0015], Fig. 1. Although *Yoshida* does not use the phrase "enhancement mode," such a transistor indeed constitutes a normally-off enhancement-mode GaN transistor.

2. [1a] a GaN layer;

[192] The '335 patent admits enhancement-mode GaN HEMT devices typically included a GaN layer. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B.

[193] *Yoshida* discloses a GaN layer (Grounds 4-5). *Yoshida*'s teaches that "i-type GaN is [a] particularly preferrable" embodiment of "**layer 3**," which is an intrinsic or undoped GaN. *Yoshida*, Abstract, [0012], Fig. 1.

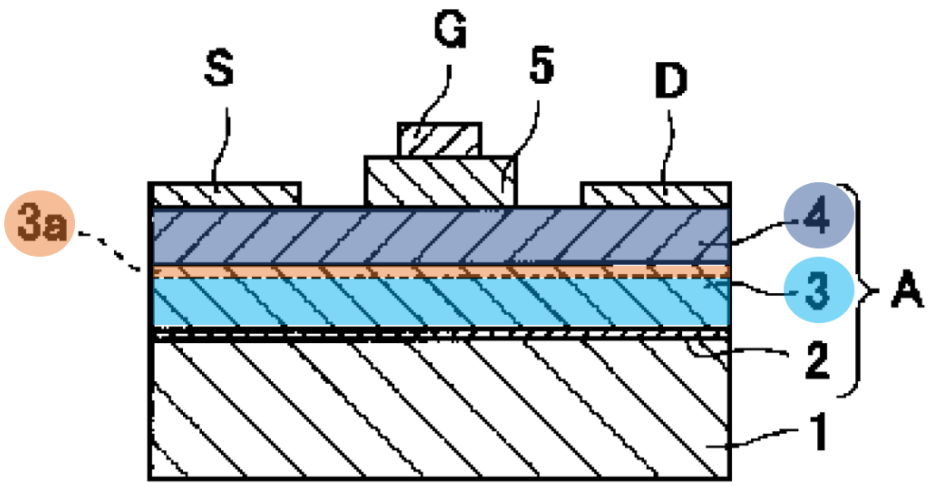


Yoshida, Fig. 1.

3. [1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[194] The '335 patent admits Limitation [1b] was conventional. It notes GaN HEMTs "typically include[d] a barrier layer of AlGaN adjacent to a layer of GaN," inducing a 2DEG at the AlGaN-GaN interface. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B. That arrangement was typical.

[195] *Yoshida* also discloses Limitation [1b] (Grounds 4-5). *Yoshida*'s "**layer 4**" is a barrier layer disposed on GaN **layer 3**. *Yoshida*, Abstract, [0010], [0013], Fig. 1.



Yoshida, Fig. 1.

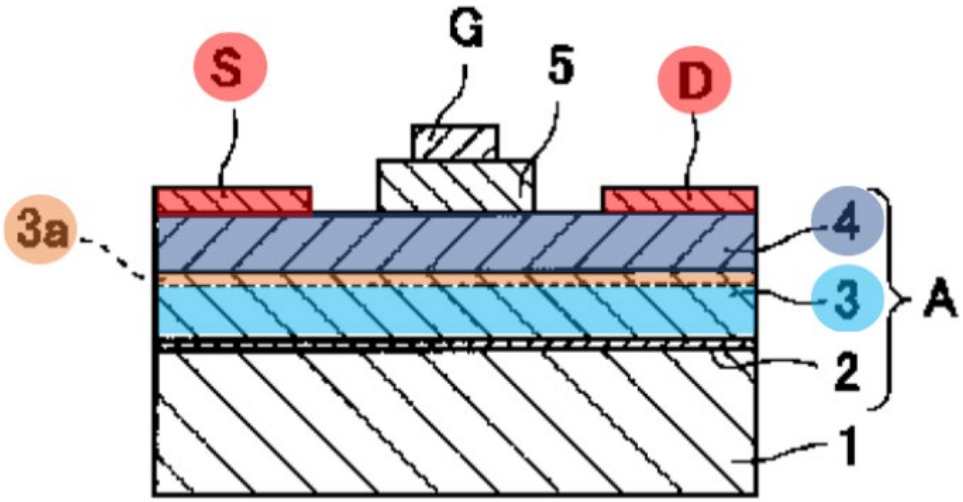
[196] *Yoshida* identifies that "n-type AlGaN is [a] favorable" choice for **layer 4**. *Yoshida*, Abstract, [0010], [0013], Fig. 1. The '335 patent likewise discloses that the claimed barrier layer may be an AlGaN layer, which is covered in dependent claims. Ex. 1001, 1:42-63, 3:37-48, 4:16-22, claims 3, 6.

[197] *Yoshida* further discloses "**two-dimensional electron gas layer 3a** is ***formed at the*** heterojunction ***interface*** between n-type semiconductor **layer 4** and i-type semiconductor **layer 3**, and more specifically at the topmost portion of i-type semiconductor **layer 3**." *Yoshida*, [0016].

4. [1c] source contact and a drain contact formed on the barrier layer;

[198] The contacts of Limitation [1c] were entirely conventional, as the '335 patent admits. Ex. 1001, 1:64-2:19, Figs. 1-2, 3A-3B.

[199] *Yoshida* discloses **source** and **drain electrodes** (contacts) that are "directly loaded" (formed) on barrier **layer 4** (Grounds 4-5). *Yoshida*, Abstract, [0014], [0022], Figs. 1-2, 3A-3B.



Yoshida, Fig. 1.

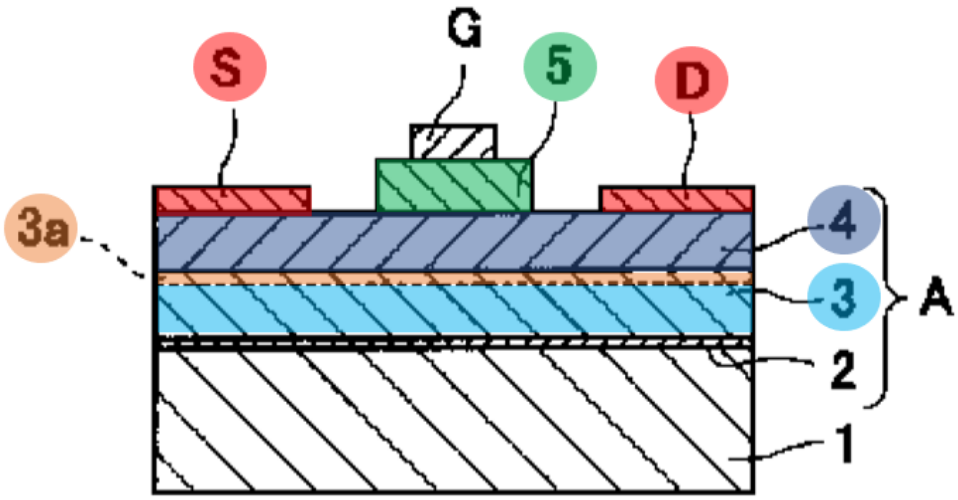
5. [1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[200] The '335 patent admits Limitation [1d] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B.

[201] In my opinion, *Yoshida* in view of the knowledge of a POSITA (Ground 4) and in view of *Saxler* (Ground 5) renders obvious Limitation [1d].

[202] *Yoshida*'s **layer 5** is "a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces … contacting the barrier layer,"

as recited in claim 1. *Yoshida* explains that **layer 5** may be a single- or double-layer comprising a "p-type GaN." *Yoshida*, Abstract, [0009], [0015], [0018], claim 2.

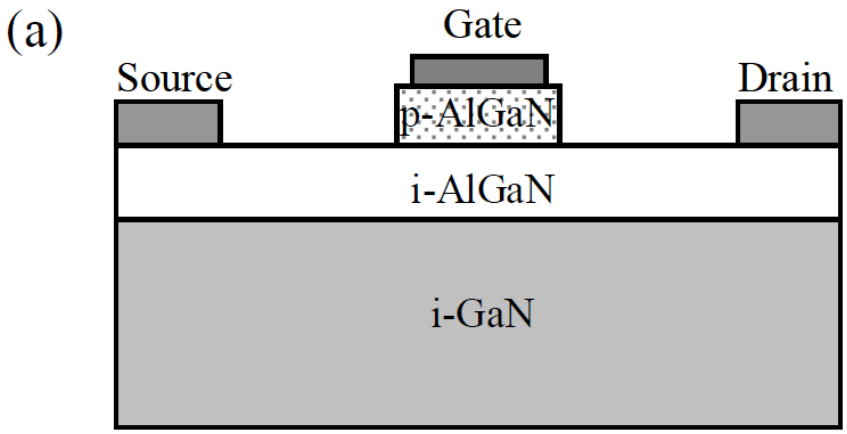


Yoshida, Fig. 1.

<u>Mapping Under Patent Owner's Construction (Ground 4-5)</u>

[203] Ground 4: *Yoshida* renders obvious sloped sidewalls that extend horizontally towards source and drain contacts if the claimed extension of the side surfaces is interpreted to include any amount extension beyond a perfectly vertical sidewall, per Patent Owner's construction. Although *Yoshida* draws substantially vertical sidewalls of p-type **layer 5**, a POSITA would have known a sidewall drawn vertically would in fact have a slight slope when built in a real-world device.

[204] A POSITA would have been familiar with this principle. For example, *Saxler* states that, in practice, "an etched region illustrated as a rectangle will, typically, have ***tapered***, rounded or curved features." *Saxler*, [0042]. As another example, a 2006 IEEE paper on a GaN HEMT with a similar gate structure to *Yoshida* shows its p-AlGaN gate layer with vertical sidewalls in its drawings (Fig. 1) but a microscope image of a device built according to the drawings shows distinctly sloped sidewalls extending horizontally towards source and drain contacts, as shown below. *Uemoto*, Figs. 1-2, Fig. 5.



Uemoto, Fig. 1(a) (drawing).

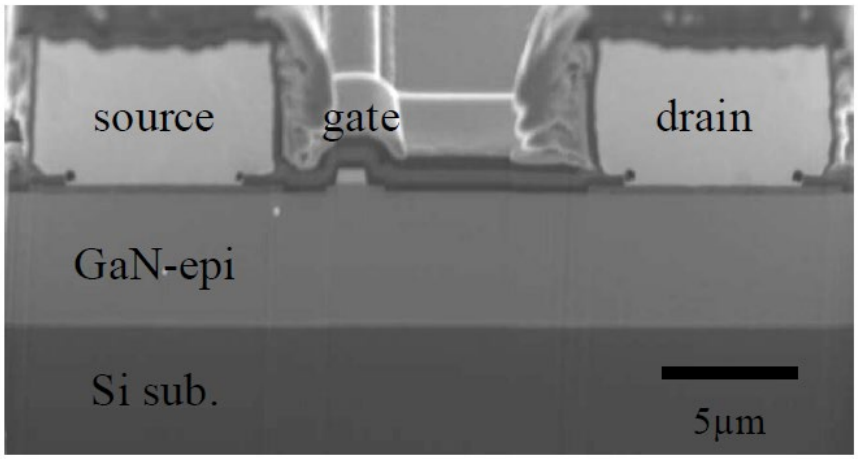
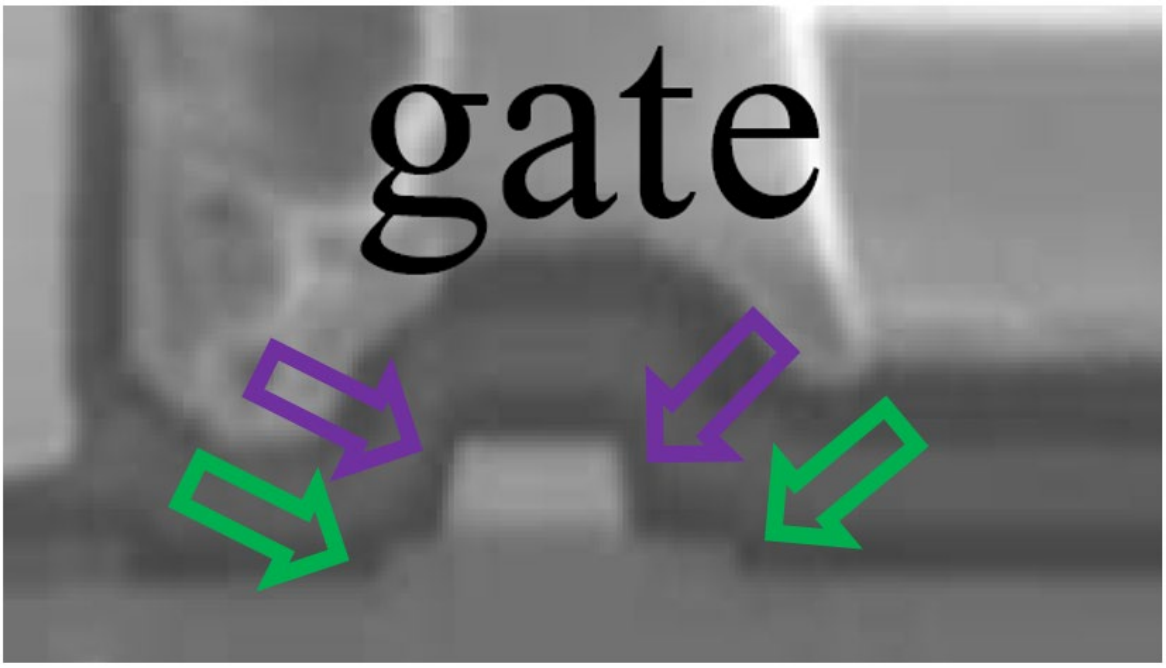


Fig.5 Cross sectional SEM image of GIT on a Si substrate.

Uemoto, Fig. 5 (microscope image).



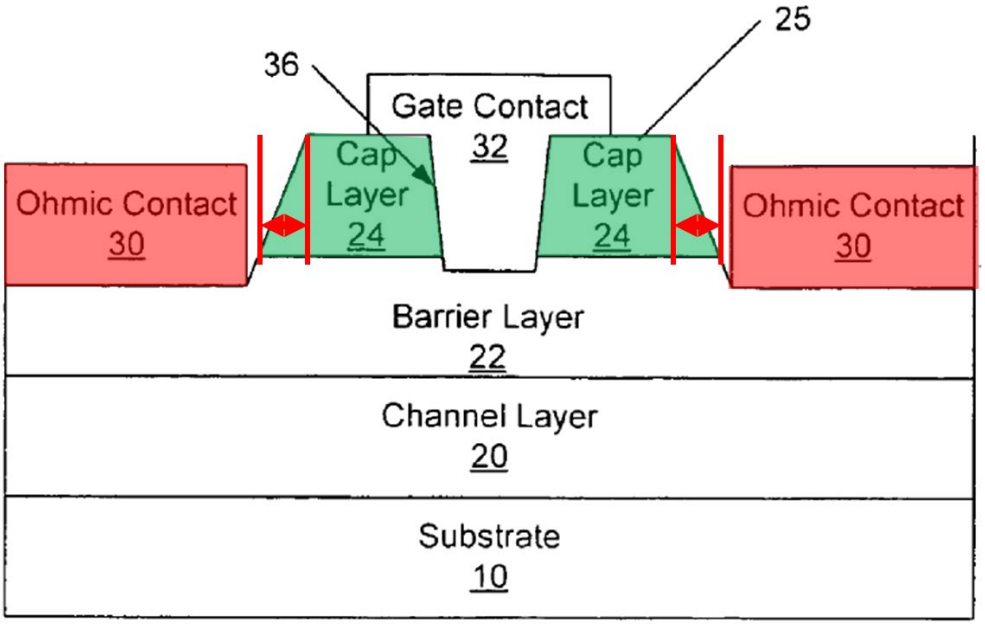
Uemoto, Fig. 5 (showing sloped sidewalls of the **p-AlGaN** layer and **gate metal**).

[205] Thus, if Patent Owner's construction applies and Limitation [1d] covers any amount extension beyond a perfectly vertical sidewall, it is my opinion that a POSITA would have recognized that *Yoshida*'s sidewalls would have had a taper when implemented in practice, and *Yoshida* alone thereby renders obvious Limitation [1d] (Ground 4).

[206] Ground 5: As discussed, *Yoshida*'s drawing shows substantially vertical sidewalls of layer 5 and a POSITA would know that those sidewalls extend towards the **source** and **drain contacts** under Patent Owner's construction in real life, even though the sidewalls are perfectly vertical in the diagram. The drawings in *Saxler*, however, disclose "the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact," as recited in claim 1, and it would have been obvious to incorporate these features into *Yoshida*'s structure. Thus, *Yoshida* in view of *Saxler* renders obvious Limitation [1d] under Patent Owner's construction.

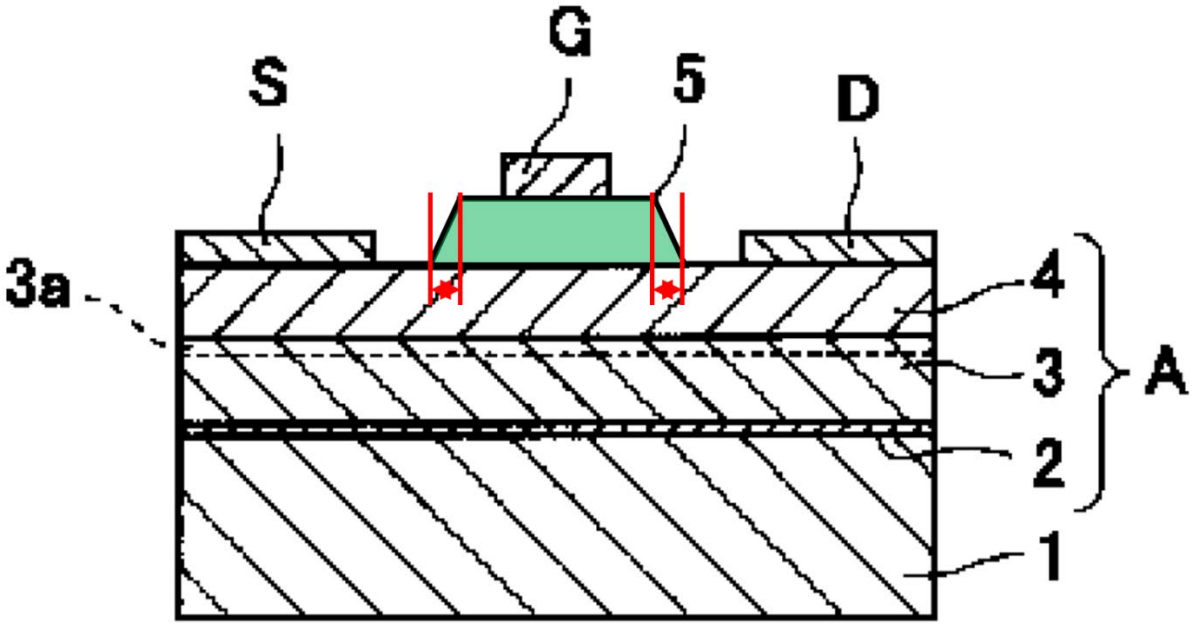
[207] Like *Yoshida*'s layer 5, *Saxler*'s **cap layer** is a p-type gate material that may include a "p-type dopant" in a subregion or doped throughout the layer. *Saxler*, [0013], [0069], [0071], [0073]. The **cap layer** resides above an AlGaN **barrier layer**, just like *Yoshida*'s **layer 5** and as claim 1 of the '335 patent requires. *Saxler*, [0010], [0059]-[0063], Figs. 1A, 2B.

[208] *Saxler* discloses [1d] under Patent Owner's construction. *Saxler*'s **cap layer** has side surfaces that plainly extend horizontally towards the **source** and **drain contact** under Patent Owner's construction, as I have annotated in the below figure. *Saxler*, [0064], Figs. 1A, 2B.



Saxler, Fig. 1A.

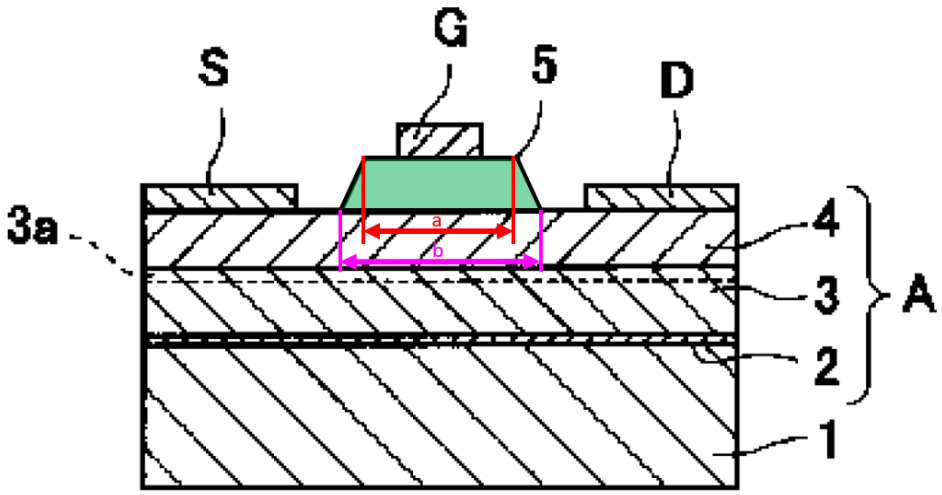
In my opinion, it would have been obvious to combine the sloped sidewalls of *Saxler*'s doped **cap layer** into *Yoshida*'s p-type **layer 5** such that they horizontally extended towards the **source** and **drain contacts** in the *Yoshida-Saxler* device, resulting in a similarly sloped structure. §XII.B.2 (Ground 5, Motivation to Combine).



Yoshida, Fig. 1 (modified).

Mapping Under Petitioners' Construction (Ground 5)

[209] *Yoshida* in view of *Saxler* renders obvious Limitation [1d] under Petitioner's construction (Ground 5). The combined *Yoshida-Saxler* device has side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer, which is the proper construction. §IX.A (Claim Construction). In the combined structure, the bottom of the **p-type gate material** (length "**b**," below) is more than 10% wider than the top (length "**a**"). I measured these distances and found that **b** is approximately 1.24 times the length of **a**.

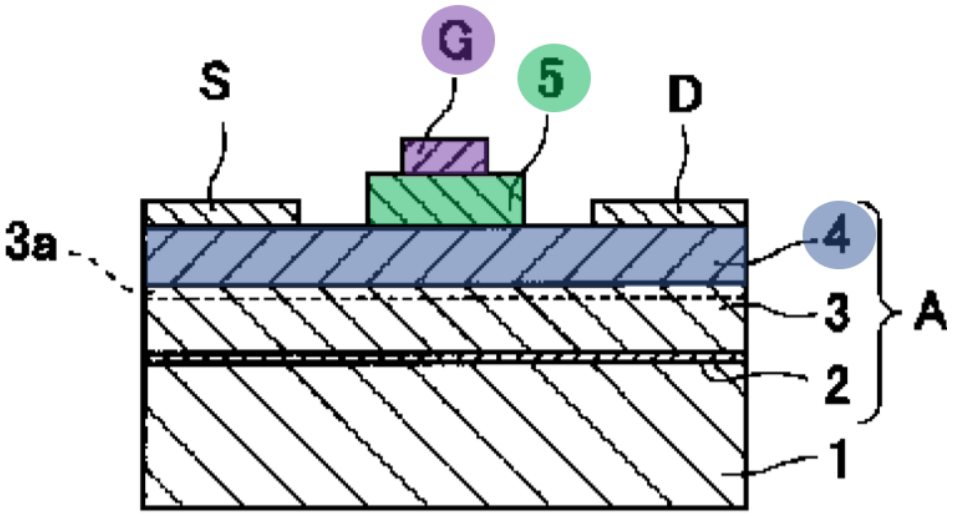


Yoshida, Fig. 1 (modified).

6. [1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

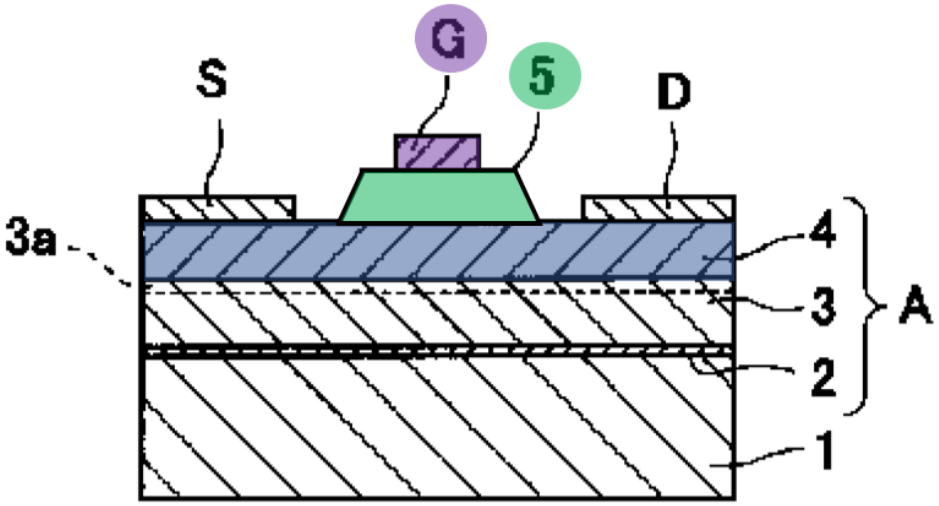
[210] The patent admits the features of Limitation [1e] were conventional and depicts numerous prior art devices disclosing Limitation [1e]. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A.

[211] *Yoshida* discloses Limitation [1e] (Ground 4). *Yoshida*'s "**gate electrode**" is a metal (e.g., "Au/Pt, Al") formed on p-type **layer 5**. *Yoshida*, Abstract, [0006], [0009]-[0010], [0016], [0022]-[0023], claim 1, Fig. 1. Its sidewalls extend downwards towards **layer 5**. *Yoshida*, Fig. 1.



Yoshida, Fig. 1.

[212] In addition, the *Yoshida-Saxler* combination (Ground 5) likewise discloses a gate metal with sidewalls that extend towards the **p-type GaN layer** (Ground 5).

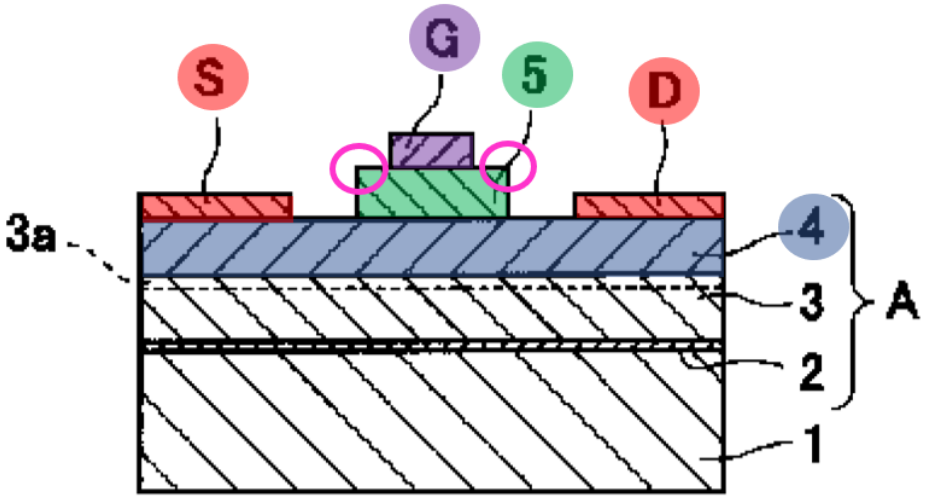


Yoshida, Fig. 1 (modified).

7. [1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

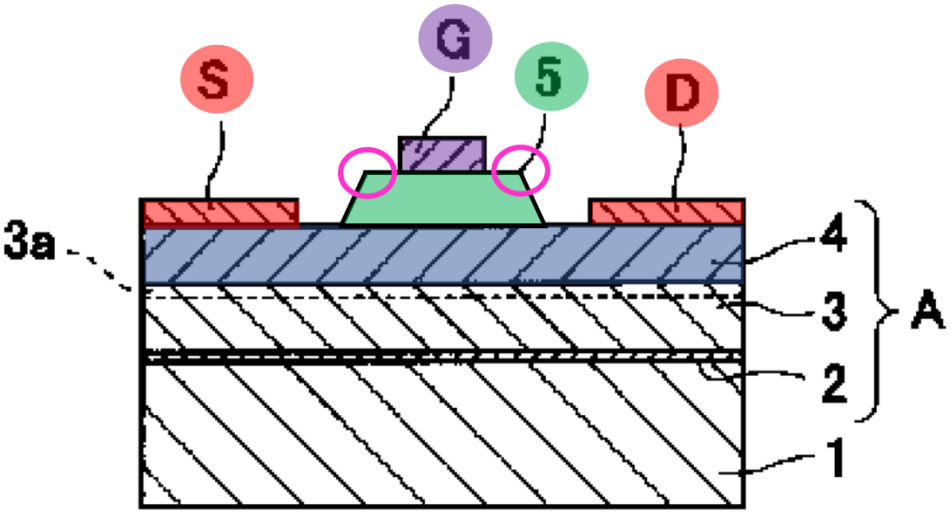
[213] Limitation [1f] is the only feature of independent claim 1 that the ’335 patent does not admit is found in the prior art. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A. *Yoshida* discloses it.

[214] As shown below, *Yoshida*’s **gate electrode** is narrower than **layer 5**, which exposes **horizontal ledges** that extend past the sidewalls of the **gate electrode** and toward the **source** and **drain**, as required in Limitation [1f]. *Yoshida*, [0022]-[0023], Fig. 1. These ledges are symmetric on either side of the gate metal (i.e., having substantially equal widths). *Yoshida*, Fig. 1. *Yoshida* thus discloses this element (Ground 4).



Yoshida, Fig. 1 (modified).

[215] In my opinion, the combination of *Yoshida* and *Saxler* also renders obvious Limitation [1f] (Ground 5). As shown below, *Yoshida-Saxler*'s **gate electrode** is narrower than the modified **layer 5**, which exposes **horizontal ledges** that extend past the sidewalls of the **gate electrode** and toward the **source** and **drain**.



Yoshida, Fig. 1 (modified).

D. [Claim 2] The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

[216] Claim 2 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 2 is thus drawn a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim Construction).

[217] Thus, for reasons I explained for Limitation [1f], claim 2 is obvious over *Yoshida* and *Saxler* (Grounds 4-5). §XII.C.7 (Limitation [1f]).

E. [Claim 3] The enhancement-mode GaN transistor according to claim 1, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

[218] *Yoshida* discloses claim 3. As I explained in Grounds 4-5, Limitation [1b], *Yoshida* discloses that layer 4 comprises AlGaN. *Yoshida*, Abstract, [0010], [0013] ("n-type AlGaN is favorable"), [0021], Fig. 1; §XII.C.3 (Grounds 4-5, Limitation [1b]).

F. [Claim 4] The enhancement-mode GaN transistor according to claim 1, wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width.

[219] Claim 4 only requires that the gate metal is narrower than the p-type gate material, but this feature is already required by Limitation [1f] to form the

horizontal ledges under either Party's construction. As I explained for Limitation [1f], *Yoshida* alone (Ground 4) and/or in view of *Saxler* (Ground 5) discloses a **gate electrode** narrower than **layer 5**. *Yoshida*, [0022]-[0023], Fig. 1; §XII.C.7 (Limitation [1f]).

G. Independent Claim 5

[220] In my opinion, *Yoshida* in view of the knowledge of a POSITA (Ground 4) and in view of *Saxler* (Ground 5) renders obvious claim 5.

1. [5p] An enhancement-mode GaN transistor, comprising:

[221] Limitation [5p] is identical to Limitation [1p]. *Yoshida* discloses it for the reasons I explained for Limitation [1p]. §XII.C.a ((Limitation [1p]).

2. [5a] a GaN layer;

[222] Limitation [5a] is identical to Limitation [1a]. *Yoshida* discloses it for the reasons I explained for Limitation [1a]. §XII.C.2 (Limitation [1a]).

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[223] Limitation [5b] is identical to Limitation [1b]. *Yoshida* discloses it for the reasons I explained for Limitation [1b]. §XII.C.3 (Limitation [1b]).

4. [5c] a source contact and a drain contact disposed on the barrier layer;

[224] Limitation [5c] is identical to Limitation [1c]. *Yoshida* discloses it for the reasons I explained for Limitation [1c]. §XII.C.4 (Limitation [1c]).

5. [5d] a p-type gate material formed above the barrier layer and between the source and drain contacts;

[225] *Yoshida* discloses Limitation [5d]. As I explained for Limitation [1d], *Yoshida*'s **layer 5** may comprise a "p-type GaN" in either a single-layer or double-layer, and it is disposed between source and drain contacts. *Yoshida*, Abstract, [0009], [0015], [0018], claim 2; §XII.C.5 (Limitation [1d]).

6. [5e] and a gate metal disposed on the p-type gate material,

[226] The recitations of Limitation [5e] are included in Limitation [1e]. *Yoshida* discloses Limitation [5e] for the reasons I explained for Limitation [1e]. §XII.C.6 (Limitation [1e]).

7. [5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[227] Claim 5 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 5 thus includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim

Construction). Limitation [5f] otherwise is identical to Limitation [1f]. For reasons I provided for Limitation [1f], Limitation [5f], for reasons I explained for Limitation [1f], Limitation [5f] is obvious over *Yoshida* alone (Ground 4) and in view of *Saxler* (Ground 5)., §XII.C.7 (Limitation [1f]).

[228] As I have explained, *Yoshida*'s gate electrode is narrower than the underlying p-type GaN layer, resulting in the horizontal ledges of the p-type gate material that extend past sidewalls of the gate metal towards the source contact and drain contact as required by Limitation [5f] (Ground 4). *Yoshida*, [0022]-[0023], Fig. 1; §XII.C.7 (Limitation [1f]). The combination of *Yoshida* and *Saxler* also includes these features (Ground 5). §§XII.B.2 (Motivation to Combine), XII.C.7 (Limitation [1f]).

8. [5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

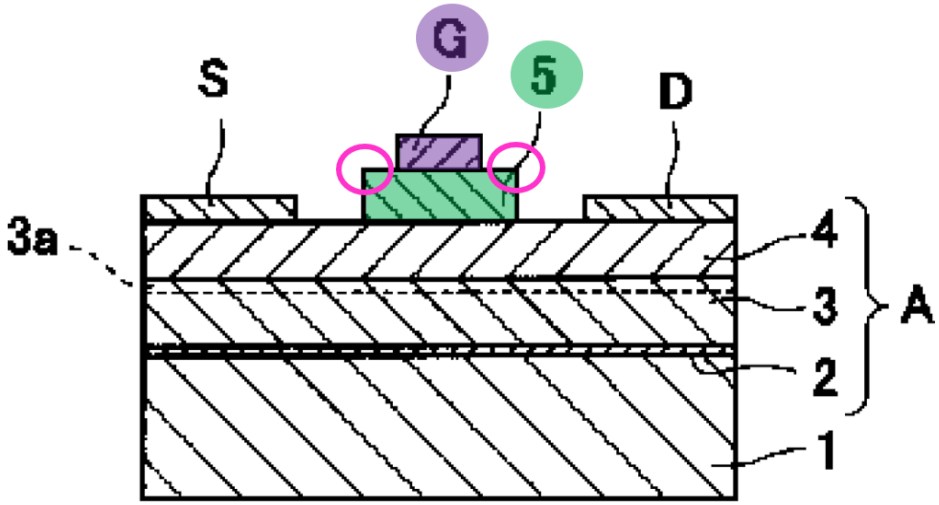
[229] Limitation [5g] has the same requirements as Limitation [1d]. For the reasons I explained for Limitation [1d], *Yoshida* in view of the knowledge of a POSITA (Ground 4) and in view of *Saxler* (Ground 5) renders obvious Limitation [5g]. §XII.C.5 (Limitation [1d]).

H. [Claim 6] The enhancement-mode GaN transistor according to claim 5, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

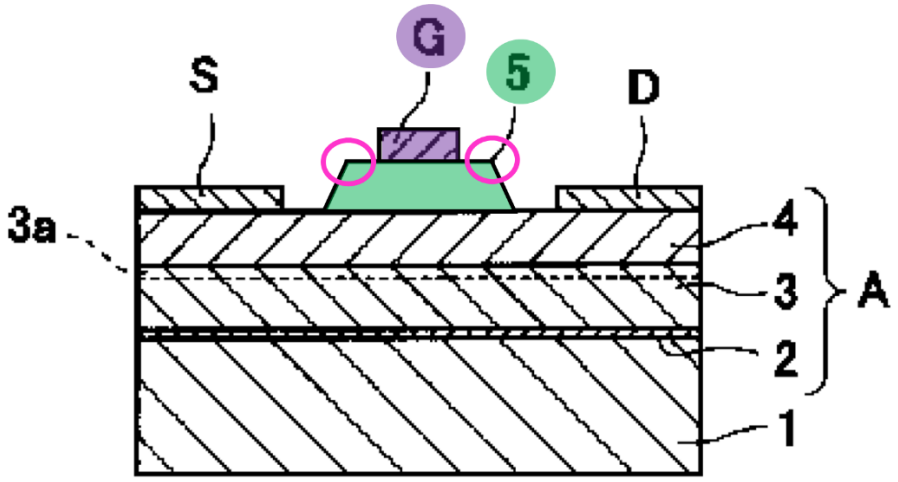
[230] *Yoshida* discloses claim 6 for the reasons I explained for Limitation [1b] (Grounds 4-5). §§XII.C.3 (Limitation [1b], XII.E (Claim 3).

I. [Claim 7] The enhancement-mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

[231] As I explained for Limitation [1f], *Yoshida* discloses that its **p-type gate material** has **symmetric ledges** on either side the **gate metal**, which I have illustrated below (Ground 4). *Yoshida*, Fig. 1; §XII.C.7 (Limitation [1f]). *Yoshida-Saxler* also includes these features, as shown below (Ground 5). §§XII.B.2 (Motivation to Combine), XII.C.7 (Limitation [1f]), XII.D (Claim 2).



Yoshida, Fig. 1.



Yoshida, Fig. 1 (modified).

XIII. GROUND 6: *YOSHIDA* IN VIEW OF *SAXLER*, *BEACH*, AND *SHENOY* RENDERS OBVIOUS CLAIMS 2 AND 5-7

A. Overview of Ground 6

[232] As I explained, the claim term "self-aligned" refers to ***how*** the claimed ledges are made, not ***what*** they are, and counsel has informed me that this term thus lends no patentable weight. §IX.B (Claim Construction). But to the extent Patent Owner disagrees that the "self-aligned" recitations of claims 2 and 5 are product-by-process elements that have no patentable weight, the combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious claims 2 and 5-7.

1. Motivation to Combine

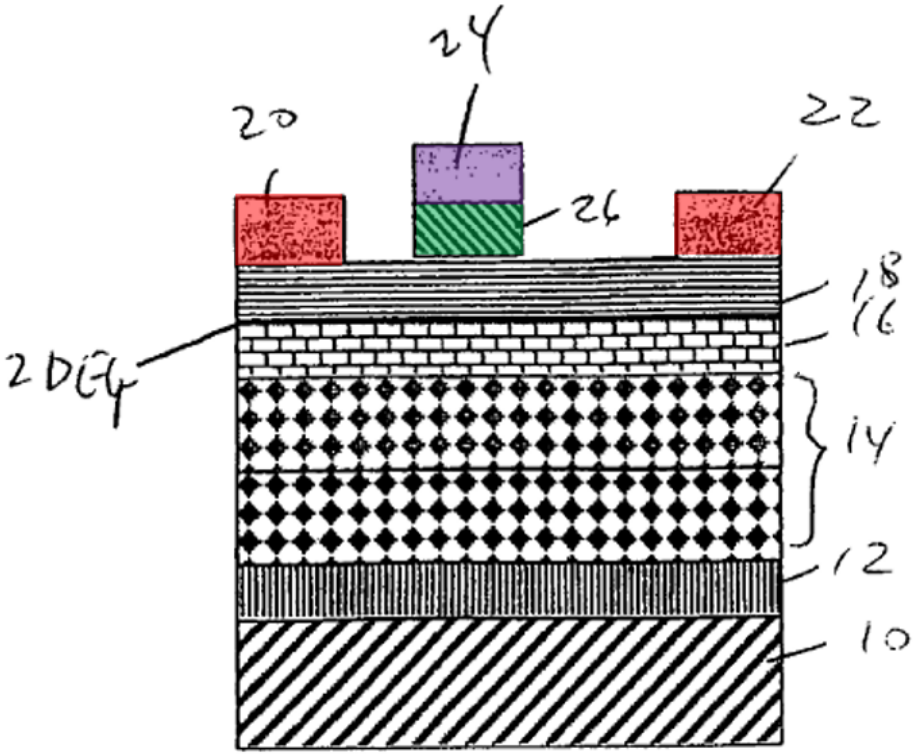
[233] In my opinion, a POSITA would have found it obvious to make the stacked gate structure of the *Yoshida-Saxler* GaN HEMT device using the methods of *Beach* and *Shenoy*. §XII.B.2 (Motivation to Combine).

[234] The *Yoshida-Saxler* combination uses a sequence of steps to create a stepped, stacked gate structure with a p-type GaN layer and a gate electrode. *Yoshida*, [0021]-[0022]. Specifically, *Yoshida* discloses: (i) depositing a p-type GaN layer 5 onto AlGan layer 4 (*Yoshida*, [0021]); (ii) dry etching the "p-type GaN layer except where the gate electrode was to be loaded" (*Yoshida*, [0022]); (iii) depositing an SiO_2 film over the entire surface (*id.*); (iv) patterning with a photoresist, and masking where the gate electrode was to be loaded (*id.*); (v) depositing source and drain electrodes (*id.*); (vi) "etching away the masking and opening the SiO_2 film", (*Yoshida*, [0023]); (vii) masking the source and drain electrodes; and (viii) depositing Au to form the gate electrode (*id.*). That process thus requires two masks. In the *Yoshida-Saxler* combination, etching step (ii) would simply employ *Saxler*'s conventional etching techniques to create sloped sidewalls. *Saxler*, [0064]; §XII.B.2 (Motivation to Combine).

[235] In my opinion, a POSITA would have been familiar with many ways to create *Yoshida-Saxler*'s stepped gate structure and would have used these methods interchangeably. §VIII (Technology Background, discussing common methods to create stepped gate structures). In view of these many interchangeable options, a POSITA would have found it obvious to modify *Yoshida-Saxler* by using *Beach*'s self-aligned technique and *Shenoy*'s isotropic etching to arrive at

that same gate structure, an approach that would have improved efficiency by eliminating masking and etching steps and would have ensured symmetry of the gate metal with respect to the p-gate material. This approach was known—*Ahn* discloses it when making a stepped gate in a thin-film transistor. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C.

[236] A POSITA would have recognized that *Beach* teaches a more efficient method of making stacked gate structures in GaN HEMT devices using fewer steps because it uses a single mask. *Beach*, [0040], [0045], [0054]. *Beach*'s gate structure includes the "gate arrangement 24," which comprises a gate electrode, and an underlying "gate barrier 26," a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F. *Beach*'s process (i) deposits "**gate barrier 26**" and "**gate arrangement 24**" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits **power electrodes**. *Beach*, [0040]. Such self-aligned techniques were common in the field as of relevant date, as I have explained. § VIII (Technology Background).



Beach, Fig. 1.

[237] In my opinion, a POSITA would have found it obvious to use *Beach*'s approach to create *Yoshida-Saxler*'s gate structure, which would have reduced masking steps, thereby driving down manufacturing time and cost. It would have been obvious to look to *Beach* for its simple methods of making stacked gate structures. And a POSITA would have further recognized that *Beach*'s self-aligned gate would have symmetrically aligned *Yoshida-Saxler* gate structure layers for better performance. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3.

[238] A POSITA would have combined *Beach* with *Shenoy* to make the **horizontal ledges** of *Yoshida-Saxler*'s stacked gate structure following its self-aligned process. *Beach* does not disclose making such **ledges**. But as previously explained, *Shenoy* discloses well-known, simple isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks that ordinary artisans used for decades. *Shenoy*, 2-3; §XI.A.2 (*Shenoy*).

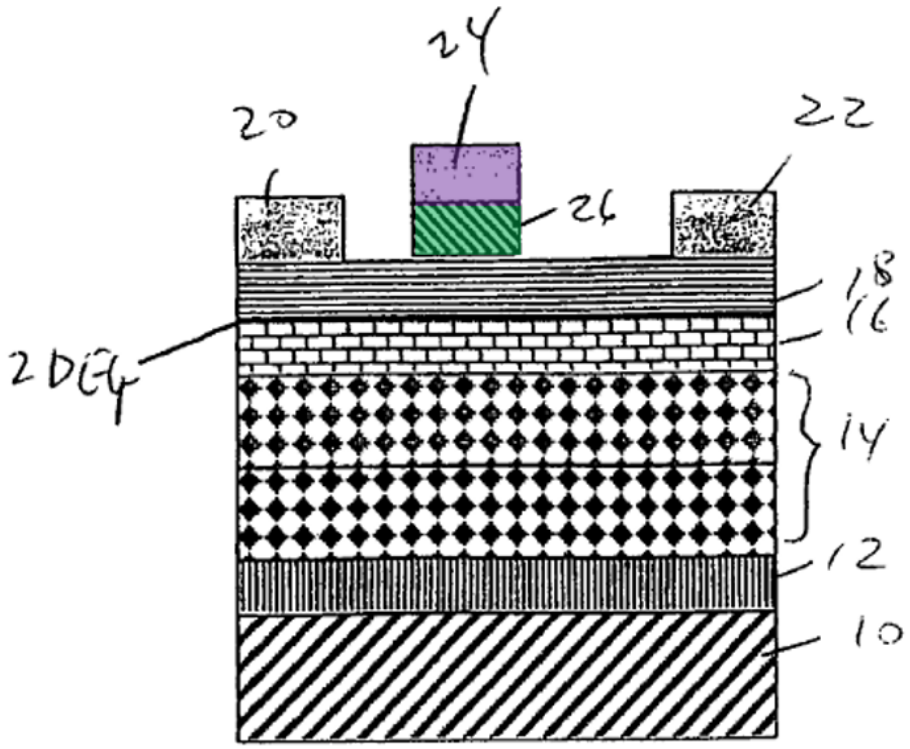
[239] *Saxler* describes using several conventional techniques to etch the cap layer and generate the slope sidewalls shown in their figures. *Saxler*, [0064], Figs. 1A-1B. So does *Sheppard*, incorporated into *Saxler* by reference to disclose methods of forming gate structures (*Saxler* [0046] (referencing Ser. No. 10/897,726), [0068] (same)).*Sheppard*, [0044], Figs. 1B-1C.

[240] Thus, an ordinary artisan would have found it obvious to use *Beach*'s self-aligned method of making *Yoshida-Saxler*'s stacked gate structure in a GaN HEMT and use *Shenoy*'s methods to undercut the **gate electrode** and create *Yoshida-Saxler*'s **horizontal ledges**. A POSITA would have found the combination a simple substitution of *Beach*'s and *Shenoy*'s known methods to predictably create *Yoshida-Saxler*'s stacked gate structure more efficiently and symmetrically.

B. [Claim 2] The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

[241] Claim 2 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 2 is thus drawn a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim Construction). But the combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* nevertheless render obvious claim 2, even if "self-aligned" lends patentable weight.

[242] As I have explained, *Beach* discloses a stacked "***self-aligned*** gate arrangement" using a single photo mask to etch both the "**gate arrangement 24**" (gate electrode) and the underlying "**gate barrier 26**" (GaN semiconductor). *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; §XIII.A.1 (Motivation to Combine). *Beach*'s process is the same self-aligned process for forming stacked gate structures depicted in the '335 patent at Figures 6A-6B. Ex. 1001, 4:14-26; §§[044] ('335 Patent Overview), XIII.A.1 (Motivation to Combine). The resulting structure has self-aligned sidewalls. *Beach*, [0040], Figs. 1, 2E-2F.



Beach, Fig. 1.

[243] And as I have further explained, *Shenoy* discloses etching a photomask to isotropically undercut the metal layer below the photomask. *Shenoy*, 2-3. That undercutting is the selfsame process described in Figures 6B-6C of the ’335 patent, which is just one of many options to form the claimed “self-aligned ledges.” Ex. 1001, 4:23-39; §§[044] (’335 Patent Overview), XIII.A.1 (Motivation to Combine).

[244] In my opinion, it would have been obvious to use *Beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make the gate structure of *Yoshida-Saxler*. §XIII.A.1 (Motivation to Combine). That approach would have reduced manufacturing time and costs and reliably improved symmetry. §XIII.A.1 (Motivation to Combine).

C. Independent Claim 5

[245] The combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious claim 5.

1. [5p] An enhancement-mode GaN transistor, comprising:

[246] As I explained in Grounds 4-5, *Yoshida* discloses Limitation [5p]. §XII.G.1 (Grounds 4-5, Limitation [5p]).

2. [5a] a GaN layer;

[247] As I explained in Grounds 4-5, *Yoshida* discloses a GaN layer. §XII.G.2 (Grounds 4-5, Limitation [5a]).

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[248] As I explained in Grounds 4-5, *Yoshida* discloses Limitation [5b]. §XII.G.3 (Grounds 4-5, Limitation [5b]).

4. [5c] a source contact and a drain contact disposed on the barrier layer;

[249] As I explained in Grounds 4-5, *Yoshida* discloses Limitation [5c]. §XII.G.4 (Grounds 4-5, Limitation [5c]).

5. [5d] a p-type gate material formed above the barrier layer and between the source and drain contacts;

[250] As I explained in Grounds 4-5, *Yoshida* discloses Limitation [5d]. §XII.G.5 (Grounds 4-5, Limitation [5d]).

6. [5e] and a gate metal disposed on the p-type gate material,

[251] As I explained in Grounds 4-5, *Yoshida* discloses Limitation [5e]. §XII.G.6 (Grounds 4-5, Limitation [5e]).

7. [5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[252] Claim 5 is for a transistor, but the term "self-aligned" refers to ***how*** the transistor's ledges are made, not ***what*** the ledges are. Counsel has accordingly informed me that claim 5 thus includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §IX.B (Claim Construction).

[253] Nevertheless, the combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious Limitation [5f], even if "self-aligned" lends patentable weight.

[254] As I explained in Grounds 4-5, *Yoshida* alone and the *Yoshida-Saxler* combination includes the structural features of Limitation [5f]. §§XII.A (Overview of Grounds 4-5), XII.B.2 (Grounds 4-5, Motivation to Combine), XII.G.7 (Grounds 4-5, Limitation [5f]). And as I further explained above in Ground 6, the *Yoshida-Saxler* combination in view of *Beach* and *Shenoy* discloses that these ledges are self-aligned, as claimed. §§XIII.A.1 (Ground 6, Motivation to Combine), XIII.B (Ground 6, Claim 2).

[255] In my opinion, it would have been obvious to use *Beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make the gate structure of *Yoshida-Saxler*. §XIII.A.1 (Motivation to Combine). That approach would have reduced manufacturing time and costs and reliably improved symmetry. §XIII.A.1 (Motivation to Combine).

8. [5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

[256] *Yoshida* in view of *Saxler* discloses Limitation [5g] for reasons I explained for Grounds 4-5. §XII.G.8 (Grounds 4-5, Limitation [5g]).

D. [Claim 6] enhancement-mode GaN transistor according to claim 5, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

[257] *Yoshida* discloses claim 6 for reasons I previously explained for Grounds 4-5, Limitation [1b]. §§XII.C.3 (Grounds 4-5, Limitation [1b]), XII.D (Grounds 4-5, Claim 2), XII.H (Grounds 4-5, Claim 6).

E. [Claim 7] The enhancement-mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

[258] As I previously explained for Grounds 4-5, *Yoshida* alone and the *Yoshida-Saxler* combination includes the features of Limitation [5f]. §§XII.G.7 (Grounds 4-5, Limitation [1f]), XII.I (Grounds 4-5, Claim 7).

[259] As I explained for Ground 6, *Beach*'s method of self-aligning the gate structure in combination with *Shenoy*'s methods of symmetrically undercutting the gate metal would have yielded symmetric ledges in the *Yoshida-Saxler* device, as required by claim 7. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3; §§XIII.A.1 (Ground 6, Motivation to Combine), XIII.B (Ground 6, Claim 2), XIII.C.7 (Ground 6, Limitation [5f]).

XIV. CONCLUSION

[260] For the reasons set forth above, in my opinion, a person of ordinary skill in the art would have found claims 1-7 of the '335 patent obvious.

[261] In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

[262] I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 18, 2023 By: James R. Shealy

James Richard Shealy, Ph.D.