

## **CERTIFICATE OF TRANSLATION ACCURACY**

I am a professional reviewer and editor specializing in translating Chinese, Japanese and Korean to English and vice versa.

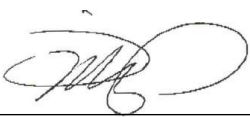
I served as Chief Examiner of the certified court interpreter test for the State of California and as a contract translator and interpreter for various federal agencies through the U.S. Department of State of for more than a decade. I served as an instructor at the University of California at Berkeley and the Middlebury Institute of International Studies at Monterey Graduate Program in Translation.

I have more than 30 years of experience in reviewing thousands of technical, legal, and business documents from Chinese to English submitted to Chinese judicial authorities, U.S. federal courts, the U.S. International Trade Commission (ITC), and the USPTO Patent Trial and Appeal Board (PTAB).

I certify that the following document translated from Chinese into the English language is a true, correct, and complete translation of the corresponding source text to the best of my knowledge and ability.

I certify under penalty of perjury that the foregoing is true and correct.

Executed this 18th day of May 2024 in Contra Costa County of the State of California.

By:   
\_\_\_\_\_  
Alex N. Jo  
Member, ATA



# China National Intellectual Property Administration

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100082

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Haidian District, Beijing  
Beijing Leader Patent & Trademark Firm, Zang Jianming (010-  
62260318)



Issuing date:

October 16, 2023

Application No. or Patent No.: 201080015425.X

Issuing No.: 2023101102645050

Case Number: 4W116886

Title of the Invention-Creation: COMPENSATED GATE MISFET AND METHOD FOR FABRICATING  
THE SAME

Patentee: Efficient Power Conversion Corporation

Petitioner for the Declaration of Invalidation: Innoscience (Suzhou) Technology Co., Ltd

## Notification That Invalidation Request Has Been Filed

To the patentee:

Invalidation request was filed with respect to the Subject Patent on October 11, 2023. Upon formality examination, we find that the request for invalidation of the above-referenced patent is in conformity with relevant provisions of the Chinese Patent Law and its Implementing Regulations and the Guidelines for Patent Examination, and thus duly filed. If the patentee submits their opinion, they must do so within one month upon receipt of this notification. If no response is made within the time limit, it will not affect the examination of China National Intellectual Property Administration. The opinion submitted shall be in two copies with the case number and the patent number indicated thereupon.

As provided in Article 19 of the Chinese Patent Law, where any foreigner, foreign enterprise or other foreign organization having no permanent residence or place of business in China applies for a patent, or has other patent matters to attend to, in China, the person shall appoint a patent agency to act on their behalf. For relevant legal clauses and agent information, please refer to the official website of the China National Intellectual Property Administration: <http://www.cnipa.gov.cn>.

As provided in Rule 69 of the Implementing Regulations of the Chinese Patent Law, in the course of the examination of the request for invalidation, the patentee for the patent for invention or utility model concerned may amend the subject claims, but may not broaden the scope of patent protection. The patentee for the patent for invention or utility model concerned may not amend the subject specification or drawings. The patentee for the patent for design concerned may not amend the subject drawings, photographs or the brief description of the design. The amendments made shall also comply with the relevant requirements for amendments to the patent documents during the invalidation procedure as provided in Article 4.6 of Chapter 3 of Part V of the Guidelines for Patent Examination.

As provided in Article 2.2.1 of Chapter 8 of Part V of the Guidelines for Patent Examination, if the opposing party has objection to the content of the Chinese translation, the opposing party shall submit the Chinese translation for the disputed parts within the above-specified time limit. Failure to submit the Chinese translation shall be deemed as having no objection to the translation.

[Seal affixed] Official Seal of CNIPA  
Patent Reexamination and Invalidation  
Department 1101081361184

Examiner: Xing Dang

CNIPA Reexamination and Invalidation Department

201004 Paper Application: Please send any replies to the Reexamination and Invalidation Department of the China National Intellectual Property Administration, No. 6 Xitucheng Rd., Jimenqiao, Haidian District, Beijing, 100088.

2022.10 Electronic Application: Relevant documents to be submitted in electronic form through the Patent Processing System. Unless otherwise specified, documents submitted in paper or other formats will be deemed as not submitted.



# China National Intellectual Property Administration

Attached herein with are the following documents:

1. Request for invalidation and corresponding annexes submitted by the petitioner on October 11, 2023

*Enclosure: Power of Attorney for Declaration Procedure on Patent Invalidation*



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|         |                                                                                                                                                                                                                                |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 201004  | Paper Application: Please send any replies to the Reexamination and Invalidation Department of the China National Intellectual Property Administration, No. 6 Xitucheng Rd., Jimenqiao, Haidian District, Beijing, 100088.     |
| 2022.10 | Electronic Application: Relevant documents to be submitted in electronic form through the Patent Processing System. Unless otherwise specified, documents submitted in paper or other formats will be deemed as not submitted. |

## Power of Attorney for Declaration Procedure on Patent Invalidation



|                                                   |  |             |
|---------------------------------------------------|--|-------------|
| Patent number                                     |  | Case Number |
| Title of the<br>Invention-Creation                |  |             |
| Petitioner for the<br>Request for<br>Invalidation |  |             |
| Patentee                                          |  |             |

Principal:

Name \_\_\_\_\_ Tel. \_\_\_\_\_  
 Address \_\_\_\_\_ Postal code \_\_\_\_\_

Agent:

Name \_\_\_\_\_ Code \_\_\_\_\_  
 Attorney \_\_\_\_\_ Tel. \_\_\_\_\_  
 Attorney \_\_\_\_\_ Tel. \_\_\_\_\_  
 Address \_\_\_\_\_ Postal code \_\_\_\_\_

The attorney appointed by the principal listed above will represent us in the invalidation proceedings of the Subject Patent, and the authority of the appointment shall be limited to handling matters related to the invalidation proceedings only.

Where:

Attorney \_\_\_\_\_ Agent's authority of power: ☐ General agent ☐ Special agent

Attorney \_\_\_\_\_ Agent's authority of power: ☐ General agent ☐ Special agent

Principal (Signature)

Agent (Signature)

Date

Date

Reminder: Before completing this Power of Attorney form, please make sure to carefully read the cautionary notes below.



## Power of Attorney for Declaration Procedure on Patent Invalidation

1. A patent agency shall not assign a person who is not qualified to act as a patent agent.
2. The Power of Attorney shall be valid only if it meets the following conditions:
  - (1) affixed with the signature or seal of the principal;
  - (2) affixed with the signature or seal of the agent; and
  - (3) description of the entrusted matters and the authority to act.
3. If the authority to act does not involve the disposition of rights, such as submitting requests, statements of opinion, evidence and other related materials, participating in oral hearings, and handling other related matters, the authority to act can be filled in as "general agent".
4. The special agent includes the following four powers:
  - (1) The attorney of the patentee recognizes the invalidation request of the applicant on behalf of the petitioner;
  - (2) The attorney of the patentee amends the claims on behalf of the patentee;
  - (3) The attorney gets reconciliation on behalf of the applicant; and
  - (4) The attorney of the petitioner withdraws the request for invalidation on behalf of the petitioner.
5. If the agent's authority involves the disposition of rights but includes only some of the four powers listed in note 4, or if the agent's authority includes other authorities that are not listed in note 4, the powers shall be itemized in the column of the agent's authority one by one.
6. In case of change or termination of the authority to act, the principal shall inform the China National Intellectual Property Administration in writing.
7. The entrustment procedures shall be handled according to the provisions of Section 3.6, Chapter 3, Part 4 of the Examination Guidelines.

# Request for Declaration of Patent Invalidation



|                                                                                                                                                                                                 |                                                                                                                                                                       |                           |                                                                                              |                                |                           |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|----------------------------------------------------------------------------------------------|--------------------------------|---------------------------|
|                                                                                                                                                                                                 |                                                                                                                                                                       |                           | This box is to be filled in by the<br>China National Intellectual Property<br>Administration |                                |                           |
| ② Patent application                                                                                                                                                                            | Patent No.: 201080015425X    Date of being granted: July 30, 2014                                                                                                     |                           |                                                                                              | ① Case number                  |                           |
|                                                                                                                                                                                                 | Title of the Invention-Creation: COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME                                                                          |                           |                                                                                              |                                |                           |
|                                                                                                                                                                                                 | Patentee: Efficient Power Conversion Corporation                                                                                                                      |                           |                                                                                              |                                |                           |
| ③ Petitioner for the Request for Invalidation                                                                                                                                                   | Name: Innoscience (Suzhou) Technology Co., Ltd                                                                                                                        |                           | User code                                                                                    |                                | Tel: 18500188075          |
|                                                                                                                                                                                                 | Resident identification number or unified social credit code:<br>91320509MA1PY5UE67                                                                                   |                           |                                                                                              |                                | E-mail                    |
|                                                                                                                                                                                                 | Nationality or country (region) of registration: China                                                                                                                |                           |                                                                                              |                                | Postal code 215231        |
|                                                                                                                                                                                                 | Permanent residence or place of business: China                                                                                                                       |                           |                                                                                              |                                |                           |
|                                                                                                                                                                                                 | Province, Autonomous Region, Municipality: Jiangsu Province                                                                                                           |                           |                                                                                              | City/county: Suzhou City       |                           |
|                                                                                                                                                                                                 | City (township), street, suite number: No.98, Xinli Road, Beishe, Lili Town, Wujiang District, China                                                                  |                           |                                                                                              |                                |                           |
| ④ Receiver                                                                                                                                                                                      | Name: Pu Yang                                                                                                                                                         |                           |                                                                                              | Tel.: 010-5769-5665            |                           |
|                                                                                                                                                                                                 | E-mail: pu.yang@fangdalaw.com                                                                                                                                         |                           |                                                                                              | Postal code: 100020            |                           |
|                                                                                                                                                                                                 | Province, Autonomous Region, Municipality: Beijing                                                                                                                    |                           |                                                                                              | City/county: Chaoyang District |                           |
|                                                                                                                                                                                                 | City (township), street, suite number: Shanghai Fangda Partners (Beijing) Law Firm, 27 <sup>th</sup> Floor, North Building, Beijing Kerry Center, No. 1 Guanghua Road |                           |                                                                                              |                                |                           |
| ⑤ Patent Agent                                                                                                                                                                                  | Name: Shanghai Fangda Partners                                                                                                                                        |                           |                                                                                              | Organization Code: 31279       |                           |
|                                                                                                                                                                                                 | Attorney (1)                                                                                                                                                          | Name: Pu Yang             |                                                                                              | Attorney (2)                   | Name: Meng Zuo            |
|                                                                                                                                                                                                 |                                                                                                                                                                       | License No.: 3127910643.6 |                                                                                              |                                | License No.: 3127922191.0 |
|                                                                                                                                                                                                 |                                                                                                                                                                       | Tel: 010-5769-5665        |                                                                                              |                                | Tel: 010-5769-4233        |
| ⑥ A request for invalidation is filed against the Subject Patent in accordance with Article 45 of the Chinese Patent Law and Rule 65 of the Implementing Regulations of the Chinese Patent Law. |                                                                                                                                                                       |                           |                                                                                              |                                |                           |
| ⑦ Grounds for, scope of, and evidence relied upon in the request for invalidation                                                                                                               |                                                                                                                                                                       |                           |                                                                                              |                                |                           |
| Grounds                                                                                                                                                                                         |                                                                                                                                                                       | Scope                     |                                                                                              | Evidence                       |                           |
| According to Article 26(3) of the Chinese Patent Law                                                                                                                                            |                                                                                                                                                                       | Claims 1-3                |                                                                                              | Annexes 1-13                   |                           |



## Request for Declaration of Patent Invalidation

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |            |                                               |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----------------------------------------------|
| According to Article 26(4) of the Chinese Patent Law                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Claims 1-2 | Annexes 3-13                                  |
| According to Article 26(4) of the Chinese Patent Law                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Claim 1    | Common knowledge                              |
| According to Article 22(2) of the Chinese Patent Law                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Claims 1-3 | Comparison Documents 1-3, Annex 9, Annex 14-1 |
| According to Article 22(3) of the Chinese Patent Law                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Claims 1-3 | Comparison Documents 1-3, Annex 9, Annex 14-1 |
| ⑧ Specific Statement of grounds for the request for invalidation in combination with the evidence                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |            |                                               |
| See the <i>Text of Request for Patent Invalidation</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |                                               |
| ⑨ List of Annexes:<br>[Annex Title]: Power of Attorney for Handling Declaration on Patent Invalidation<br>[Annex Title]: Main Text of Opinions<br>[Annex Title]: Proof of subject's qualification<br>[Annex Title]: Exhibit 1<br>[Annex Title]: Exhibit 2<br>[Annex Title]: Exhibit 3<br>[Annex Title]: Exhibit 4<br>[Annex Title]: Exhibit 5<br>[Annex Title]: Exhibit 6<br>[Annex Title]: Exhibit 7<br>[Annex Title]: Exhibit 8<br>[Annex Title]: Exhibit 9<br>[Annex Title]: Exhibit 11<br>[Annex Title]: Exhibit 12<br>[Annex Title]: Exhibit 13<br>[Annex Title]: Exhibit 15<br>[Annex Title]: Exhibit 16<br>[Annex Title]: Exhibit 17<br>[Annex Title]: Exhibit 18<br>[Annex Title]: Exhibit 14-1<br>[Annex Title]: Exhibit 14-2<br>[Annex Title]: Exhibit 14-3 |            |                                               |
| ⑩ Invalidation petitioner or patent agent<br>Shanghai Fangda Partners Law Firm                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                                               |

## Request for Declaration of Patent Invalidation



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## **Attachment**

### **Text of Request for Patent Invalidation**

#### **To the attention of China National Intellectual Property Administration:**

The Petitioner applies for invalidation of all claims 1-3 of Chinese Patent No. 201080015425.X, entitled "Compensated Gate MISFET and Method For Fabricating the Same" (hereinafter referred to as the "Subject Patent"). For the Subject Patent, its application date is April 7, 2010, its priority date is April 8, 2009, and its granted publication number is CN101662694B granted on July 30, 2014.

#### **Chapter I. Legal Basis of the Request for Invalidation**

The application date of the Subject Patent is April 7, 2010, and the priority date is April 8, 2009. Therefore, the Patent Law of the People's Republic of China as amended in 2000 (hereinafter referred to as the "Chinese Patent Law") and the Implementing Regulations of the Chinese Patent Law as amended in 2002 (hereinafter referred to as the "Implementing Regulations of the Chinese Patent Law") are applicable to this case.

As provided in Article 45 of the Chinese Patent Law, where, starting from the date of the announcement of the grant of the patent right by the patent administration department under the State Council, any entity or individual considers that the grant of the said patent right does not comply with the relevant provisions of this Law, it or he may request the Patent Reexamination Board to declare the patent right invalid.

As provided in Rule 64 of the Implementing Regulations of the Chinese Patent Law, anyone requesting entire or partial invalidation of a patent right in accordance with Article 45 of the Patent Law shall submit a written request and necessary supporting documents in duplicate to the Patent Re-examination Board. The said written request shall, in combination of all the submitted supporting documents, specifically state the reasons for the request for invalidation and designate the evidence on which each reason is based.

The reasons for the request for invalidation mentioned in the preceding paragraph refers to when the invention-creation on which the patent right is granted is not in conformity with Article 22, Article 23, Paragraph 3 and Paragraph 4 of Article 26, Article 33 of the Patent Law or Article 2, Paragraph 1 of Article 13, Paragraph 1 of Article 20, Paragraph 2 of Article 21 of these Rules, or falls under Article 5, Article 25 of the Patent Law, or the applicant is not entitled to a patent right in accordance with Article 9 of the Patent Law.

As provided in Article 22(2) of the Chinese Patent Law, novelty means that, the invention or utility model does not form part of the prior art; nor has any entity or individual filed previously before the date of filing with the patent administration department under the State Council an application relating to the identical invention or utility model disclosed in patent application documents published or patent documents announced after the said date of filing.

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As provided in Article 22(3) of the Chinese Patent Law, inventiveness means that, as compared with the prior art, the invention has prominent substantive features and represents a notable progress, and that the utility model has substantive features and represents a progress.

As provided in Article 26(3) of the Chinese Patent Law, the specification shall set forth the invention or utility model in a manner sufficiently clear and complete so as to enable a person having ordinary skill in the art to carry it out; where necessary, drawings are required. The abstract shall briefly state the main technical points of the invention or utility model.

As provided in Article 26(4) of the Chinese Patent Law, the claims shall be supported by the specification and defines the scope claimed by the patent in a clear and concise manner.

As provided in Rule 20(1) of the Implementing Regulations of the Chinese Patent Law, the patent claim shall state the technical features of the invention or utility model, and clearly and concisely define the scope of the requested protection.

## Chapter II. Overview of Grounds and Evidence for the Request for Invalidation

### 1. Overview of grounds for invalidation

| Claims     | Relevant legal provisions                                         | Grounds of Invalidation                     |
|------------|-------------------------------------------------------------------|---------------------------------------------|
| Claims 1-3 | Article 26(3) of the Chinese Patent Law                           | Insufficient disclosure of the description  |
| Claims 1-2 | Article 26(4) of the Chinese Patent Law                           | Failing to get support from the description |
| Claim 1    | Rule 20 (1) of Implementing Regulations of the Chinese Patent Law | Claims being unclear                        |
| Claims 1-3 | Article 22(2) of the Chinese Patent Law                           | Claims failing to possess novelty           |
| Claims 1-3 | Article 22(3) of the Chinese Patent Law                           | Claims failing to possess inventiveness     |

### 2. Evidence used in the request for invalidation and how the evidence was used

**Annex 1:** *Semiconductor Physics and Devices*, edited by Shuyuan Lu et al., Xi'an University of Electronic Science and Technology Press, February 2017;

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**Annex2:** *Physics of Semiconductors and Thin Films*, co-edited by Zhengzhong Yun et al., Chengdu Institute of Telecommunication Engineering, National Defense Industry Press, August 1981;

**Annex 3:** Re-examination Decision No. 104791 issued on January 15, 2016;

**Annex 4:** Characterization of Impurities and Defects in GaN, Jinxing Shi, Semiconductor Intelligence, Volume 35, Issue 1, February 1998

**Annex 5:** *Fundamentals of Solid-State Electronics*, (US) Saji Tang, translated by Gang Ruan et al., Fudan University Press, April 2003

**Annex 6:** *Physics of Semiconductors*, edited by Enke Liu, Bingsheng Zhu, etc., Xi'an Jiaotong University, National Defense Industry Press, December 1979

**Annex 7:** *Working Principle and Manufacturing Process of Power Semiconductor Device*, (U.S.) Ghandhi (S.K. Ghandhi), translated by Guanghua Zhang and Shiqian Zhong, Mechanical Industry Publishing House, September 1982;

**Annex 8:** *Properties and Tests of Insulating Materials with High Voltage Test Equipment*, edited by Shaojun Liu, Dadong Books, July 1954

**Annex 9:** US6498111B1, published on December 24, 2002;

**Annex 10:** p-type doping of GaN materials, ShiyongXie et al., Research and Progress in Solid State Electronics, Volume 21, Issue 2, May 2001;

**Annex 11:** Research progress based on p-type doping of GaN materials, Yibing Liu, Xinmin Huang, Anning Liu, et al., Infrared Technology, Vol. 30, No. 3, March 2008

**Annex 12:** Infringement comparison table and its translation submitted by the patentee in the USITC 337 proceeding;

**Annex 13:** Main contents of evidence of non-triviality grounds of CN102365747B and instructions for use;

**Annex14:** Comparison Document 1: CN101107713, published on January 16, 2008;

**Annex14-1:** US2005145874A1 cited in Comparison Document 1 and its Chinese translation;

**Annex15:** Comparison Document 2: US2006/0015545A1 published on April 17, 2008, and its Chinese translation;

**Annex 16:** Comparison Document 3: TW200414540A, published on August 1, 2004;

**Annex 17:** Text of the granted publication document of the Subject Patent CN102365747B;

**Annex 18:** Business license of the applicant;

**Annex 19:** Power of Attorney

## Attachment



Annexes 1-11 are used to demonstrate the understanding of technical terms by a person having ordinary skill in the art and the background art of the case in question. Annex 12 is used to prove the infringement claims of the patentee in the 337 investigation of the U.S. counterpart of the patent-in-suit (claims 1-3 thereof correspond to claims 1-3 of the Subject Patent). Annex 13 summarizes the purpose of substantiation by Annexes 1-12 and the main paragraphs and contents as used for the purpose.

Annexes 14-16, which are Comparison Document s 1-3 for commenting on novelty and inventiveness, all have a publication date predating the priority date of the Subject Patent. Comparison Document 1 introduces the contents of Annex 14-1 and Annex 9 into the Subject Patent by way of referencing it in their entirety.

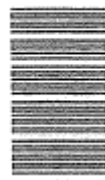
The Comparison Document s are used in the way shown in the table:

| Claims              | Evidence is used for:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Independent claim 1 | <p>Opinion on novelty:</p> <p><u>Comparison Document 1</u></p> <p><u>Comparison Document 2</u></p> <p><u>Comparison Document 3</u></p> <p>Opinion on inventiveness:</p> <p><b><u>Taking Comparison Document 1 as the most relevant prior art</u></b></p> <p>Comparison Document 1 + Common knowledge</p> <p>Comparison Document 1 + Comparison Document 2/3</p> <p>Comparison Document 1 + Comparison Document 2/3 + Common knowledge</p> <p><b><u>Taking Comparison Document 2 as the most relevant prior art</u></b></p> <p>Comparison Document 2 + Common knowledge</p> <p>Comparison Document 2 + Comparison Document 1/3</p> <p>Comparison Document 2 + Comparison Document 1/3 + Common knowledge</p> <p><b><u>Taking Comparison Document 3 as the most relevant prior art</u></b></p> <p>Comparison Document 3 + Common knowledge</p> <p>Comparison Document 3 + Comparison Document 1/2</p> <p>Comparison Document 3 + Comparison Document 1/2 + Common knowledge</p> |

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| Claims     | Evidence is used for:                                                                                                                                                                                                                                            |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claims 2-3 | <p>Additional technical features:</p> <p>Comparison Document 1 or Comparison Document 1 + Common knowledge</p> <p>Comparison Document 2 or Comparison Document 2 + Common knowledge</p> <p>Comparison Document 3 or Comparison Document 3 + Common knowledge</p> |

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### Chapter III. Specific Statement of Grounds for Invalidation

Claim 1 seeks to protect a column III Nitride transistor. For ease of analysis, the technical features of claim 1 are numbered as follows:

"1-1 A column III Nitride transistor, comprising:

1-2 a substrate,

1-3 a set of III-N (column III Nitride) Transition layers above the substrate,

1-4 a III-N buffer layer above the set of transition layers,

1-5 a III-N barrier layer above the buffer layer,

1-6 a compensated GaN layer above the barrier layer, and

1-7 a gate contact above the compensated GaN layer."

Claim 2 further defines the compensated GaN layer of claim 1 as "the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen".

Claim 3 further defines the acceptor type atoms of claim 2 as "the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca."

#### **1. Claims 1-3 are not sufficiently disclosed in the specification and do not comply with Article 26(3) of the Chinese Patent Law.**

As recorded in Section 2.1.3 of Chapter 2 of Part II of the Examination Guidelines, "the specification shall clearly set forth the technical solution of the invention or utility model, describe in detail the specific modes for carrying out the invention or utility model, and entirely disclose the technical specifics necessary for understanding and carrying out the invention or utility model, to such an extent that a person having ordinary skill in the art can carry out the invention or utility model. If the examiner can reasonably doubt that the invention or utility model does not meet the requirement of sufficient disclosure, he shall invite the applicant to make a clarification. The following circumstances are regarded as not possible to be carried out due to lack of technical means to solve the technical problem:



## Attachment

- (1) The specification sets forth only a task and/or an assumption, or simply expresses a wish and/or a result, providing no technical means that a person having ordinary skill in the art can implement;
  - (2) The specification sets forth a technical means, but the means is so ambiguous and vague that a person having ordinary skill in the art cannot concretely implement it according to the contents of the specification;
  - (3) The specification sets forth a technical means, but a person having ordinary skill in the art cannot solve the technical problem of the invention or utility model by adopting said means;
- ....."

The technical solutions of claims 1-3 correspond to the first embodiment of the specification (paragraphs 0025-0029 of the specification), and there is an apparent contradiction or an apparent lack of clarity in the specification with respect to the description of the composition, the implementation means, and the Technical Effect of the "compensated GaN layer" in claim 1 (Article 1). In addition, the first embodiment intends to disclose a MISFET in the form of a GaN transistor, and there are apparent ambiguities in the functions realized by the transistor and the functions realized by the layers comprising the transistor (e.g., the buffer layer) (Section 2).

**(1) The "compensated GaN layer" of claim 1 corresponds to the "compensated semiconductor layer 38", and there is an apparent contradiction or an apparent lack of clarity in the specification with respect to the description of the composition, the implementation means, and the Technical Effect of the compensated GaN layer.**

**Main grounds are as follows:**

Firstly, conventional growth processes (e.g., MOCVD, MOVPE, etc.) of p-GaN (where the acceptor is magnesium, zinc, carbon, etc.) with or without additional hydrogen passivation can result in p-GaN that is a deeply hydrogen-passivated, highly compensated semi-insulator. That is, the preferred/only embodiment of the compensated semiconductor 38 (compensated GaN layer) of the Subject Patent is obviously the prior art. Thus, the technical solutions of claims 1-3 clearly cover the prior art, and a person having ordinary skill in the art would not be able to clearly distinguish between the patent technology and the prior art (see Article 1.1).

Secondly, based on the disclosure of the specification, a person having ordinary skill in the art cannot make clear why the "additional hydrogen passivation" is provided and what kind of resistivity of the GaN layer is the goal of the "additional hydrogen passivation" (see Article 1.2).

Thirdly, the patentee does not describe clearly how the compensated GaN layer of the Subject Patent can simultaneously achieve two technical effects with opposite requirements for conductive electron density/resistivity (see Article 1.3).

## Attachment

In order to facilitate the panel's understanding of the petitioner's relevant points, the petitioner gave a description of the relevant terms of the patent-in-suit based on the evidence (see Article 1.0).

### (1.0.) Description of terms

Terms employed: compensated semiconductors, highly compensated semiconductors, enhancement mode devices (enhancement mode HEMT)

**(1.0.1)** Conventional definitions of "compensated semiconductor" and "highly compensated semiconductor" in the art and the meaning of "compensated GaN layer" in the Subject Patent

Firstly, according to Annexes 1-3, the compensated semiconductor in the art is defined as a semiconductor that contains both donor and acceptor impurities, and according to Annex 3, the highly compensated semiconductor in the art is defined as a semiconductor in which neither electrons nor holes provide conductivity when the donor density is comparable to the acceptor density ( $N_A \approx N_D$ ).

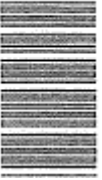
According to Annex 1 (*Semiconductor Physics and Devices*, see p. 60), "a compensated semiconductor is a semiconductor that contains both donor impurities and acceptor impurities in the semiconductor. The compensated semiconductor can be formed by doping an N-type semiconductor that has been previously doped with donor impurities with acceptor impurities, or by doping a P-type semiconductor that has been previously doped with acceptor impurities with donor impurities. The compensated semiconductor can be categorized according to the size relationship between the two impurities doped in the compensated semiconductor, and is called a P-type compensated semiconductor if  $N_A > N_D$ ; if  $N_D > N_A$ , it is called an N-type compensated semiconductor; and if  $N_A = N_D$ , it is called a fully compensated semiconductor, and the conduction electron density of a fully compensated semiconductor is the same as that of an intrinsic semiconductor".

According to Annex 2 (*Physics of Semiconductors and Thin Films*, see p. 9), "the situation in which the above mentioned donor and acceptor impurities are present in a semiconductor to offset the conductive interactions is called the compensating effect of the impurities. A semiconductor with impurity compensation is called a compensated semiconductor. For highly compensated semiconductors ( $N_A \approx N_D$ ), since neither electrons nor holes provide conductivity, although the measured resistivity of the material is high, it does not mean that the material is a pure material. In this case, it must be supplemented with measurements of other parameters, such as mobility, to identify its purity."

Annex 3 (Re-examination Decision No. 104791) is consistent with Annexes 1-2 with respect to the definition of compensated semiconductors. That is, "the compensated semiconductor is defined as a semiconductor containing both donor and acceptor impurity atoms in the same region. Since the acceptor energy level is much lower than the donor energy level, the electrons in the donor energy level first have to fill the acceptor energy level, so that the ability of the donor to supply electrons to the conduction band and the ability of the acceptor to supply holes to the valence band are weakened by the offsetting of each other. Generally,  $N_d$  indicates the density of the donor,  $N_a$  indicates the density of the acceptor, when  $N_d > N_a$ , the semiconductor is the n-type compensated semiconductor, the electron density in the conduction band is  $n = N_d - N_a$ , known as the equivalent donor density. Conversely, when  $N_d < N_a$ , the semiconductor is the p-type compensated semiconductor. When  $N_d = N_a$ , all the electrons on the donor exactly make the acceptor ionized, and the conduction electrons in the energy band can only be generated by intrinsic excitation; and the semiconductor is known as a fully compensated semiconductor, and exhibits the properties of an intrinsic semiconductor. The compensation doping is usually utilized in semiconductor fabrication techniques to obtain the desired Fermi energy level."

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Second, the compensated GaN layer/compensated semiconductor 38 layer of the Subject Patent refers to the passivation or compensation of hydrogen (acting as a donor) to magnesium and the like (p-type acceptor impurities with easy hydrogen binding qualities) in the GaN layer.

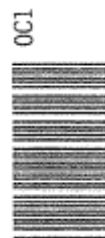
One of the major problems that GaN, as a specific semiconductor, faced during its development was the difficulty in obtaining p-type conductivity. The reason for this is that when Mg is used as the acceptor dopant, Mg is passivated by hydrogen in the semiconductor growth process to produce MgH, and therefore must be "usually doped and then subjected to low-energy electron-beam irradiation or thermal annealing in order to obtain P-type conductivity" (see Annex 4, Section 2, "Doping of GaN and Characterization of Various Impurities" of *Characterization of Impurities and Defects in GaN*).

Annex 4, Section 2.1, "Role of Hydrogen in Doping" states that "H can be inferred to be the donor H + in p M QaN,... For Mg-doped GaN, if it is grown at high temperature above 1200 K, it is always highly compensated, and the center of compensation can be N vacancy or H (if H<sub>2</sub> is present). The conclusion is consistent with experimental facts. In molecular beam epitaxy (MBE) growth, the only P-type GaN that can be obtained without post-growth treatments is low-temperature growth below 1000 K and the absence of H. If H is present, the H concentration is essentially equal to the Mg concentration, and the H donor and Mg acceptor actually form an electrically neutral complex with a binding energy of 0.7 eV. The binding energy is sufficiently low for the complex to dissolve at the growth temperature; however, when the sample is cooled to room temperature, the Mg and H will form an Mg-H pair."

Furthermore, according to the specification, "the compensated semiconductor layer 38 preferably comprises AlGa<sub>1-x</sub>N<sub>x</sub> or GaN having deeply passivated p-type impurities such as Mg, Zn, Be, Cd, or Ca". As well, the patentee asserted in the United States litigation (claims 1-3 correspond exactly to claims 1-3 of the present patent) that the detection of a certain level of hydrogen and Mg in the accused infringing product is considered to be that the GaN layer is a compensated GaN layer based on SIMS data.

According to the characteristics of the GaN semiconductor itself, combined with the specification and the patentee's relevant claims, it can be determined that the compensated GaN layer in the patent-in-suit refers to the passivation or compensation of hydrogen (acting as a donor) in the GaN layer to magnesium and the like (p-type acceptor impurities with easy hydrogen binding qualities).

**(1.0.2)** A "semi-insulator" in the art corresponds to a relatively high resistivity (or a relatively low conductive electron density), but there is no standardized range of resistivity (or conductive electron density) in the art.



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According to Annex 5 (*Fundamentals of Solid-State Electronics*), conductors, semi-insulators and insulators are distinguished on the basis of resistivity/conductive electron density, with the resistivity of conductors, semi-insulators, and insulators increasing and the conduction electron density decreasing in that order.

| Type of material | Resistivity ( $\Omega\cdot\text{cm}$ ) | Conductive electron density ( $\text{cm}^{-3}$ ) |
|------------------|----------------------------------------|--------------------------------------------------|
| Conductor        | $10^{-2} - 10^9$                       | $10^6 - 10^{17}$                                 |
| Semi-insulator   | $10^{10} - 10^{14}$                    | $10 - 10^5$                                      |
| Insulator        | $10^{14} - 10^{22}$                    | 1-10                                             |

According to Annex 5, the resistivity of the semiconductor is from  $10^{-2}$  to  $10^{-9} \Omega\cdot\text{cm}$ , the resistivity of the semi-insulator is from the  $10^{10}$  to  $10^{14} \Omega\cdot\text{cm}$ , and the resistivity of the insulator is from  $10^{14}$  to  $10^{22} \Omega\cdot\text{cm}$ .

However, according to Annex 6 (*Physics of Semiconductors*), a material with a resistivity greater than  $10^6$  to  $10^7 \Omega\cdot\text{cm}$  is classified as semi-insulator.

According to Annex 7 (*Principles of Operation and Manufacturing Processes of Power Semiconductor Devices*), materials with resistivity exceeding  $100 \Omega\cdot\text{cm}$  are often classified as semi-insulators.

According to Annex 8 (*Properties and Tests of Insulating Materials with High Voltage Test Equipment*), the resistivity of semi-insulators is between  $10^6$  to  $10^{12} \Omega\cdot\text{cm}$ , and the resistivity of insulators is more than  $10^{12} \Omega\cdot\text{cm}$ .

Thus, the semi-insulators are generally distinguished according to the resistivity/conductive electron density. However, the range of resistivity/conductive electron density of semi-insulators defined by the prior art varies greatly. When the semi-insulator is a key attribute for the person skilled in the art to distinguish between the patented technology and the prior art, the range of resistivity/conductive electron density corresponding to the semi-insulator should be limited in the patent.

### (1.0.3.) p-GaN Enhancement mode device (Enhancement mode HEMT)

Enhancement mode HEMTs can be realized in a variety of ways, one of which is a p-GaN enhancement mode device. That is, the P-GaN layer is placed between the barrier layer and the gate metal (i.e., where the compensated GaN layer is located in the Subject Patent), and a certain density of P-type conductive electrons is required to keep the device in a normally closed state.

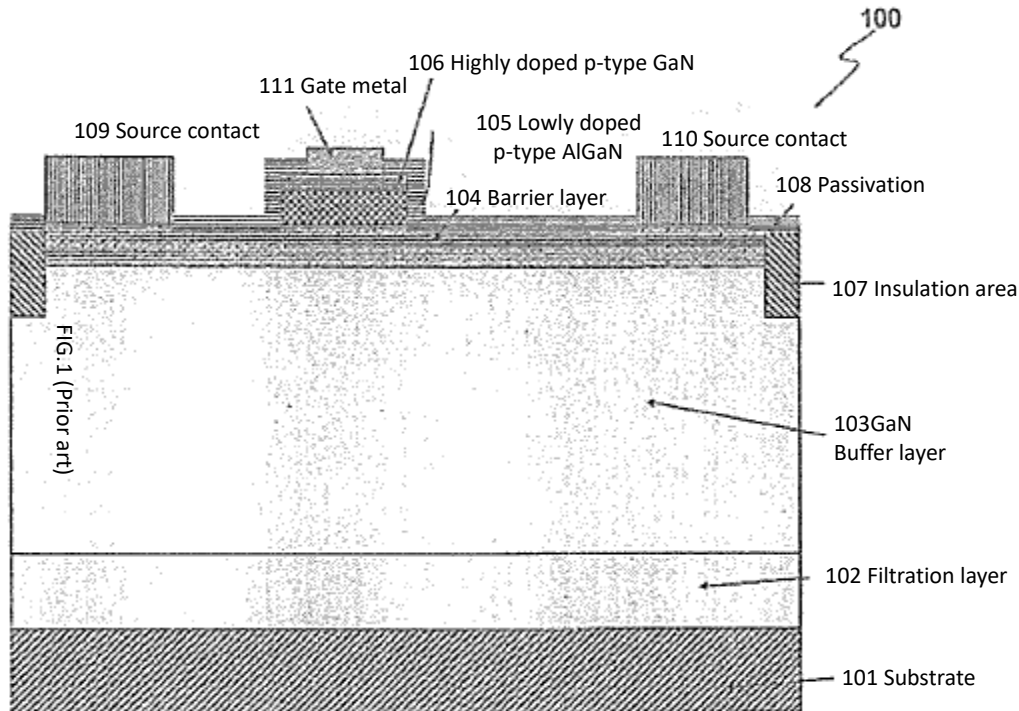
Typical high electron mobility transistors (HEMTs) are normally-on or depletion-type, which utilize an AlGaN layer (i.e., the barrier layer 104 in FIG. 1) provided on the GaN layer (i.e., the buffer layer 103 in FIG. 1) to generate two-dimensional electron gas (2DEG) for realizing the high electron mobility (see paragraphs 0003-0004 of the specification of the Subject Patent).

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Unlike the normally-on or depletion-type devices, the enhancement mode devices (see paragraph 0005 of the specification of the Subject Patent) have a p-GaN layer (105, 106) between the barrier layer 104 and the gate metal 111. Only a certain concentration of P-type carriers in the p-GaN layer allows the device to be normally closed into off-state.



### (1.0.4.) MISFET

MISFETs are field effect tubes (FETs) with a metal-insulator-semiconductor (MIS) structure.

1.1. The p-GaN obtained by conventional growth processes (e.g., MOCVD, MOVPE, etc.) of p-GaN (where the acceptor is magnesium, zinc, carbon, etc.) with or without additional hydrogen passivation can be a deeply hydrogen-passivated highly compensated semi-insulator. That is, the preferred/only embodiment of the compensated semiconductor 38 (compensated GaN layer) of the Subject Patent is obviously the prior art. Thus, the technical solutions of claims 1-3 clearly cover the prior art, and a person having ordinary skill in the art would not be able to clearly distinguish between the patent technology and the prior art.

First, in the conventional growth process of p-GaN (e.g., MOCVD, MOVPE), it is difficult to avoid hydrogen passivation of p-type acceptors such as magnesium, and in this case, a highly compensated semi-insulator with deep hydrogen passivation can be obtained. Thus, the preferred (and only) embodiment described in the specification is a deep hydrogen-passivated highly compensated semi-insulator, which is naturally obtained by the conventional growth process of P-GaN.

Annex 9 (US6498111B1) submitted by the petitioner describes that: during the growth of p-GaN by MOCVD, the acceptor passivation of the reactor-cooled device is unavoidable when the acceptor is magnesium, zinc, carbon, etc.: "Hydrogen is common in a MOCVD reactor during growth of the GaN material and subsequent reactor cooling, generally coming from two sources. Hydrogen is commonly used during growth as a carrier gas

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for the growth source gasses. In addition, ammonia (NH<sub>3</sub>) is used as a source gas for nitrogen (N) during growth of the GaN material and is also used to stabilize the GaN material during reactor cooling. Hydrogen is produced as a by-product of the ammonia decomposition during growth and cooling. In the conventional GaN growth process, there is sufficient hydrogen in the reactor to cause passivation of the p-type region during cooling." (see paragraph 1 of column 2 of the translation of Annex 9). The p-type receptors that are susceptible to passivation by hydrogen include magnesium, zinc, and carbon (see paragraph 3 of column 1 of the translation of Annex 9). Removal of all hydrogen sources is impractical and passivation during reactor cooling is unavoidable (see paragraph 2 of column 2 of the translation of Annex 9).

In addition, hydrogen passivation of magnesium and other receptors (forming Mg-H complexes) inactivates magnesium and other receptors, resulting in materials that become insulating or weakly p-type in the as-grown state. Generally speaking, the purpose of doping is to obtain certain conductive electrons, the difficulty of obtaining low resistivity P-GaN due to the hydrogen passivation is the main factor hindering the development of p-GaN (See Annex 9 and Annex 10: *p-type doping of GaN materials*, and Annex 11 *Research progress based on p-type doping of GaN materials*).

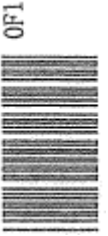
For example,

As described in Annex 9 (see paragraph 3 of column 1 of the translation of Annex 9), "a common problem is electrical passivation of acceptors like Mg, zinc (Zn), carbon (C) and others by hydrogen atoms. The smaller hydrogen atoms diffuse into the GaN material, where they neutralize the Mg acceptors and the holes produced by the Mg. The passivation process leaves the Mg acceptors inactive, resulting in the material becoming insulating or weakly p-type in its as-grown state."

As described in Annex 10 (see paragraph 3 of column 1 of p. 206), "however, at first the progress was not smooth. When GaN was grown by MOGVD, even when doped with Mg up to  $10^{19}$  to  $10^{20}$  cm<sup>-3</sup>, the GaN remained semi-insulating with a resistivity as high as  $10^8 \Omega \cdot \text{cm}$ , which is a phenomenon known as passivation of Mg. The Mg must be reprocessed after growth in order to activate the Mg and obtain P-type GaN".

Second, in order to obtain lower resistivity ones, the level of hydrogen passivation in p-GaN needs to be reduced by additional activation of P-type carrier processes (e.g., annealing) or by designing special structures (e.g., passivation layers). However, it is difficult to eliminate hydrogen passivation in p-GaN in its entirety. Therefore, even if the patentee asserts that claim 1 protects a greater scope than the preferred embodiment and there is no limitation on the extent of hydrogen passivation of receptors such as magnesium, it clearly covers the hydrogen passivation that remains in the prior art after the p-GaN undergoes an additional activation process or is designed to reduce the hydrogen passivation with a special structure.

According to Annexes 9-11 provided by the petitioner, with the aid of additional activation processes (e.g., annealing), it is possible to reduce the degree of hydrogen passivation, thereby obtaining p-GaN with a relatively low electrical resistivity. However, it is possible to remove only a portion of the hydrogen passivation, with a certain degree of hydrogen passivation still remaining.



For example, as described in Annex 10 (see last paragraph on p. 208 to paragraph 1 on p. 209, that is, the last paragraph of section 4), "but even after the LEEBI or RTA treatment, the hole concentration of Mg-doped GaN is usually still not more than  $10^{18}\text{cm}^{-3}$ , and the doping efficiency is only 0.1% to 1%, which cannot well meet the device needs. On one hand, a large amount of H remains in the treated Mg-doped GaN [13], which compensates for the partially affected Mg".

**(1.2.) Based on the disclosure of the specification, a person having ordinary skill in the art cannot make clear why the "additional hydrogen passivation" is provided and what resistivity of the GaN layer is the goal of the "additional hydrogen passivation".**

As described in paragraph 0028 of the specification of the patent-in-suit, "additional hydrogen passivation" is performed after the growth of the compensated semiconductor 38:

"Referring to FIG. 7, the next step is to grow the compensated semiconductor layer 38 on the barrier layer 34. Referring to FIG. 8, the next step is to deposit a gate contact layer 37 on the compensated semiconductor layer 38. ... The gate shading mask is subsequently removed. Additional hydrogen passivation can be performed by exposing the device to an ammonia or hydrogen plasma at elevated temperatures."

First, the specification does not clearly explain the reasonableness and necessity of "additional hydrogen passivation".

According to the evidence provided by the Petitioner, in the art, during the growth of P-GaN layer (with magnesium as the acceptor, etc.), a highly compensated semi-insulating GaN layer can be obtained without the need for an additional annealing process (see Annex 4 and Annexes 11-13). That is, the compensated semiconductor 38 formed by natural growth prior to performing additional hydrogen passivation can satisfy the requirements of the preferred embodiment of the present patent with respect to the P-GaN properties.

It is clear that the purpose of the "additional hydrogen passivation" is to improve the degree of hydrogen passivation, and it is difficult for a person having ordinary skill in the art to understand the reasonableness and necessity of performing the "additional hydrogen passivation" based on the preparation method provided in the specification corresponding to the transistor of claim 1.

Second, the semi-insulation does not correspond to a defined range of resistivity, and a person having ordinary skill in the art does not know when the "additional hydrogen passivation" is required, and thereby is unable to determine the extent of "additional hydrogen passivation".

For the preferred embodiment of the patent disclosure, "semi-insulating" corresponds to a very vague resistivity range (Point (2) of Article 1.0 of this text). A person having ordinary skill in the art would not know when the "additional hydrogen passivation" is required, or what resistivity GaN layer is intended to be formed by the "additional hydrogen passivation".

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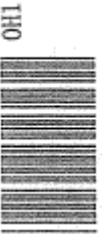


It is assumed that the patentee asserts that claim 1 protects a greater scope than the preferred embodiment, and there is no limitation on the extent of hydrogen passivation of a receptor such as magnesium. A person having ordinary skill in the art can generate P-GaN with different resistivities by varying annealing parameters such as annealing temperature, and a certain amount of residual hydrogen passivation remains even after the annealing process. Thus, a person having ordinary skill in the art at this point would be less able to determine when the "additional hydrogen passivation" is required and to what extent the "additional hydrogen passivation" is required.

**(1.3.) The patentee does not describe clearly how the compensated GaN layer of the Subject Patent can simultaneously achieve two technical effects with opposite requirements for conductive electron density/resistivity.**

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Requiring low resistivity<br>Enhancement mode devices require a certain density of p-type carriers in p-GaN.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Requiring High resistivity<br>Conduction electrons in p-GaN are highly compensated to become semi-insulating materials.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Record of the patent-in-suit<br>[0026] "The compensated layer 38 ..... forming an enhancement mode device".                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Record of the patent-in-suit<br>[0026] "using a compensated semiconductor layer 38 leads to low gate leakage during device operation" and "the insulating nature of compensated layer 38 reduces the gate capacitance of the device".<br>[0029] "the passivation of a p-type impurity using hydrogen. The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, ..... Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art. |
| Technical Effect 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Technical Effect 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <p>First, when the resistivity is so high that the compensated semiconductor layer 38 is a "highly compensated semi-insulating material", the p-type conduction electrons are comparable in density to the hydrogen ions (<math>N_A \approx N_D</math>), and almost all of the p-type conduction electrons are passivated by the hydrogen ions, making the device unusable as an enhancement mode device.</p> <p>Second, it is assumed that the patent right emphasizes that the compensated GaN of the Subject Patent does not necessarily require a "highly compensated semi-insulating material" in terms of resistivity, but only a higher resistivity than that of general p-GaN. However, due to different processes and applications, there is generally no clear range of resistivity for p-GaN. It is also difficult for a person having ordinary skill in the art to determine what kind of resistivity a higher resistivity is, and therefore it is not possible to determine the specific type of a compensated GaN layer that belongs to the technical contribution of the present invention.</p> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

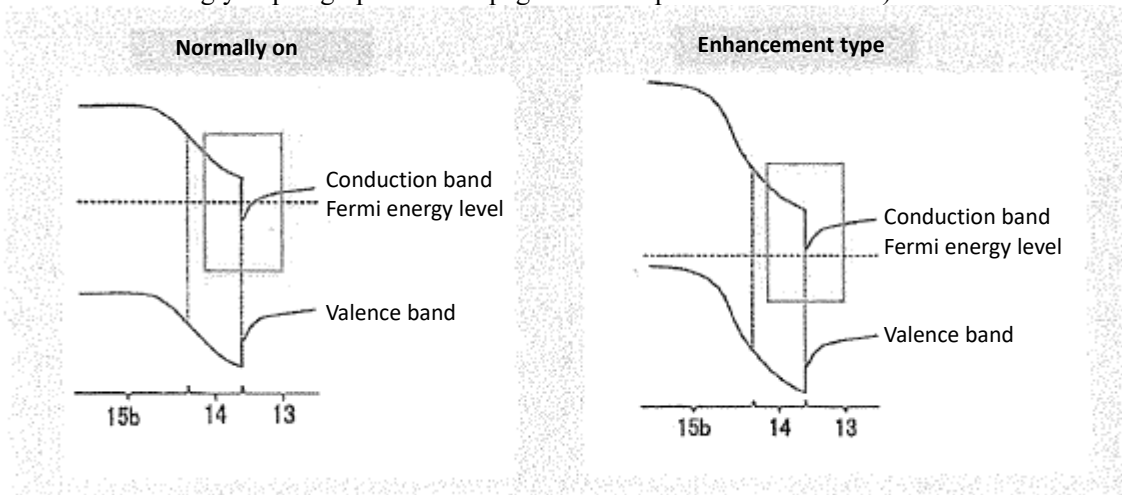
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**The operation principle of enhancement mode devices dictates that the p-type carriers in p-GaN must have a certain density:**

The conduction band of a normally on device (shown below on the left) has a discontinuity at the heterogeneous interface between the first nitride semiconductor layer 13 (GaN) and the second nitride semiconductor layer 14 (AlGaN). At the heterogeneous interface, the conduction band is located at an energy level lower than that of the Fermi energy level (there is a triangular region in the red box where the conduction band is lower than that of the Fermi energy level), thus giving rise to a 2DEG.

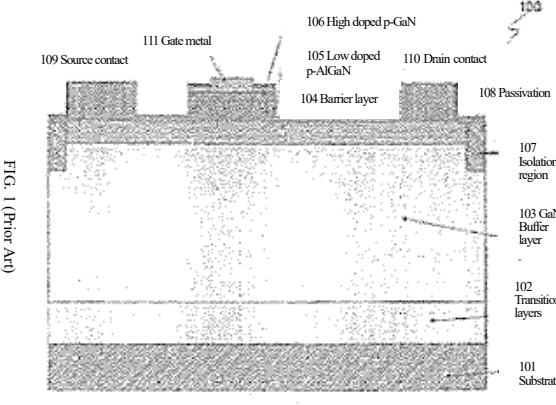
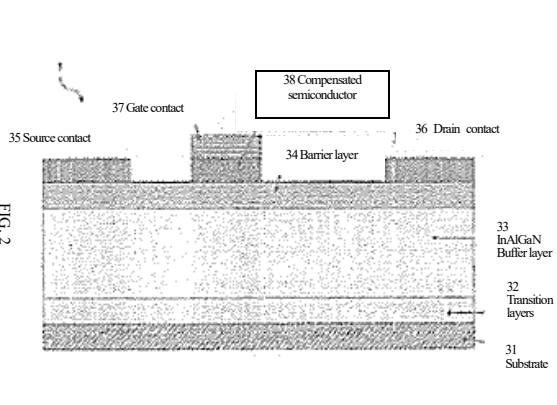
For the enhancement mode devices (shown below on the right), a third nitride semiconductor layer 15 is provided on top of the second nitride semiconductor layer 14, and only the activation (i.e., with a certain concentration) of the p-type impurities in this layer can lead to an increase in the energy levels of the second nitride semiconductor layer 14 and the first nitride semiconductor layer 13 until the conduction band at the heterogeneous interface between the first nitride semiconductor layer 13 and the second nitride semiconductor layer 14 is located at an energy level higher than the Fermi energy level (the conduction bands in the red box are all above the Fermi energy level). At this point, no 2DEG is generated at the heterogeneous interface, thus leading to obtaining the normally broken feature of the nitride semiconductor transistor. Thus, when the p-type impurities in the semiconductor layer 16 are not activated or are deeply passivated, the normally broken function cannot be achieved, which means that the transistor is no longer an enhancement mode device (the above principle is described accordingly in paragraph 0083 on page 3 of Comparison Document 2).



(2) According to the specification, the first embodiment realizes a transistor that is both an MBFET and a hybrid enhancement mode device (HEMT). However, according to the common sense of a person skilled in the art, it is difficult to form a transistor that is both a MISFIT and a hybrid enhancement mode device (HEMT) with the structure of the first embodiment. Since the function realized by the device determines the function realized by each layer, a person having ordinary skill in the art cannot clearly understand what is meant by "the buffer layer 33 separates the transition layers 32 from a barrier layer 34" emphasized in the specification.



# Attachment

| BACKGROUND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | First embodiment                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  <p>FIG. 1 (Prior Art)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |  <p>FIG. 2</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <p>Paragraph [0005] of the specification: "Device 100 includes substrate 11.. . , transition layers 102 typically composed of AlN and AlGaN that is about 0.1 to about 1.0 <math>\mu\text{m}</math> in thickness, buffer material 103 typically composed of <u>GaN</u> that is about 0.5 to about 10 <math>\mu\text{m}</math> in thickness, barrier material 104 typically composed of <u>AlGaN</u> where the Al to Ga ratio is about 0.1 to about 0.5 with thickness from about 0.005 to about 0.03 <math>\mu\text{m}</math>, p-type AlGaN 105, heavily doped p-type GaN 106, isolation region 107, passivation region 108, ohmic contact metals 109 and 110, and gate metal 111 typically composed of a nickel (Ni) and gold (Au) metal contact over a p-type GaN gate."</p> <p>[Description] The structure of the background art is a typical structure of the <u>enhancement mode device (HEMT)</u>, where the GaN layer (buffer layer) and the AlGaN layer (barrier layer) form a heterojunction to generate a two-dimensional electron gas. In addition, the provision of p-type GaN enable the device to be normally off.</p> | <p>Paragraph [00025] of the specification: "FIG. 2 shows a <u>MISFET</u> in the form of GaN transistor 1 according to an embodiment of the present invention. substrate 31 that for example... Over and in contact with the substrate 31 are transition layers 32. Transition layers 32 may comprise, for example, AlN or AlGaN, with a thickness of between 0.1 to 1.0 <math>\mu\text{m}</math>. <u>A buffer layer 33 separates the transition layers 32 from a barrier layer 34.</u> The buffer layer 33 is preferably formed of InAlGaN with any concentration of In and Al (including 0% In and/or Al) and has a thickness between 0.5 and 3 <math>\mu\text{m}</math>. The barrier layer 34 is formed of AlGaN and has a thickness between 0.005 and 0.03 <math>\mu\text{m}</math> and an Al percentage of about 10% to 50%. A gate contact 37, formed of for example, Ta, Ti, TiN, W, or WSi<sub>2</sub>, ... In accordance with the present invention, a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the gate contact 37..."</p> <p>[Description] The first embodiment is a <u>MISFET</u>, and the specification only emphasizes the role of the buffer layer as "the buffer layer 33 separates the transition layer 32 from the barrier layer 34".</p> |

The devices which have different functions may have different requirements for the layers. A person having ordinary skill in the art, due to failing to understand the role of the buffer layer that is emphasized therein, may have different understandings of the device functions that can be achieved by the first embodiment.

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As described in paragraph 0026 of the specification, "the high doping level of compensated layer 38 leads to enhancement mode devices". Embodiment 1 is a transistor that is both a MISFET and an enhancement type device, but according to common sense of the art, it is difficult to form a transistor that is both a MISFET and an enhancement type (HEMT) simply by raising the resistivity of the p-type GaN in the enhancement type device. That is, it is difficult to form a transistor that is both a MISFET and an enhancement type (HEMT) with the structure of this embodiment.

Since there are different understandings of the functions realized by the device, there are also different understandings of the functions that can be realized by each layer. For example, it is the enhancement mode (HEMT) in the background art. Generally, a person having ordinary skill in the art believes that the transition layer is provided for nucleation or lattice matching, and the heterojunction formed by the buffer layer (GaN layer) and the barrier layer (AlGaIn layer) is provided to generate a two-dimensional electron gas. However, the first embodiment emphasizes that the transistor is a MISFET, and according to the comparison of the descriptions of the layers in the above table between the background art and the first embodiment, there are many differences between the descriptions of the layers in the first embodiment and the descriptions of the layers in the background art. In particular, the first embodiment additionally emphasizes that "the buffer layer 33 separates the transition layer 32 from the barrier layer 34". A person having ordinary skill in the art cannot clearly understand the above differences and the meaning of "the buffer layer 33 separates the transition layer 32 from the barrier layer 34" (emphasized).

### **2. Claims 1-2 cannot be supported by the specification, and thereby are not in conformity with Article 26.4 of the Chinese Patent Law.**

**(1) The "compensated GaN layer" in claim 1 generalizes a wide range, and the specification only gives a specific "preferred" embodiment. It is not clear to a person having ordinary skill in the art whether other embodiments, except the preferred embodiment, can also solve the same technical problem and achieve the same technical effect.**

The specification gives only a "preferred" embodiment of the general concept "compensated GaN layer" (see paragraphs 0025 and 0029 of the specification) as that "FIG. 2 shows a MISFET in the form of GaN transistor 1 according to an embodiment of the present invention... the compensated semiconductor layer 38 preferably comprises AlGaIn or GaN having deeply passivated p-type impurities such as Mg, Zn, Be, Cd, or Ca". In addition, "the passivation of a p-type impurity using hydrogen". The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material."

In this preferred embodiment, the acceptor is "Mg, Zn, Be, Cd, or Ca", and hydrogen acts as an applicator to passivate or compensate for the acceptor, such as Mg, with a concentration of hydrogen equal to the concentration of Mg ( $N_A \approx N_D$ ), resulting in a highly compensated p-GaN. That is, neither electrons nor holes provide electrical conductivity (see Annex 3 for the definition of a highly compensated semiconductor), and the p-GaN is a high resistivity insulator or semi-insulator at this point.

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A person having ordinary skill in the art does not know whether there are other ways of realizing the "compensated GaN layer" other than the preferred embodiment that can also solve the technical problems of the present invention and achieve the same technical effect.

**(2) Claim 2 further defines the "compensation GaN layer" but is still a generalization of the preferred embodiment. It is not clear to a person having ordinary skill in the art whether other embodiments, except the preferred embodiment, can also solve the same technical problem and achieve the same technical effect.**

Claim 2 further defines the compensated GaN layer of claim 1 as "the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen".

**(2.1.) Claim 2 does not define the types of "acceptor type atoms" that include the type of "acceptor type dopant atoms" failing to solve the technical problems of the invention and achieving the same technical effect, such as "the group consisting of C, Fe, Mn, Cr and V", and so on.**

**(2.2.) Claim 2 does not define the degree of "hydrogen passivation", and therefore includes technical solutions (e.g., the solution in FIG. 1 of the Background Art) failing to solve the technical problems of the invention and achieving the same technical effect.**

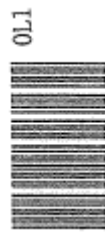
The specification discloses only one implementation manner to passivate the hydrogen passivation to an insulator or semi-insulator: the corresponding embodiment is a "transistor being a MISFET" with a "metal-insulator-semiconductor" structure. Underneath the gate contacts (metal) is a compensated semiconductor layer 38 of "AlGaIn or GaN deeply passivated p-type impurities" (see paragraph 0025), and the compensated semiconductor layer 38 is a "highly compensated semi-insulating material" (see paragraph 0029).

Claim 2 does not define the degree or result of "hydrogen passivation". Since hydrogen passivation is unavoidable when the receptor is a heterogeneous substance such as magnesium, this claim is clearly included in the technical solution of the prior art, which cannot solve the technical problem of the invention or achieve the same technical effect.

### **3. The protection scope of claim 1 is unclear, so it does not comply with Rule 22(2) of the Implementing Regulations of the Chinese Patent Law.**

The protection scope of the "compensated GaN layer" in claim 1 is not clear. In the art, hydrogen passivation cannot be avoided during the growth process of p-GaN (the acceptor is magnesium, etc.). That is, the p-GaN (acceptor is magnesium, etc.) obtained by the conventional process is a "compensated GaN layer", and magnesium is one of the earliest acceptors used to realize p-GaN. Thus, according to the "compensated GaN layer" of claim 1, a person having ordinary skill in the art cannot even distinguish the technical solution of claim 1 from the technical solution of the background art. Therefore, claim 1 clearly defines the protection scope in an unclear manner.

## Attachment



**4. Claims 1-3 lack novelty provided in Article 22(2) of the Chinese Patent Law.**

**(1) Independent claim 1 lacks novelty provided in Article 22(2) of the Chinese Patent Law over Comparison Document 1, Comparison Document 2, or Comparison Document 3.**

**(1.1.) Claim 1 lacks novelty over Comparison Document 1.**

The correspondence between the features of claim 1 of the Subject Patent and the disclosure of Comparison Document 1 (CN101107713A) is shown in the following table. It should be noted that the following table is only an exemplary enumeration, and the technical specifics disclosed in Comparison Document 1 are not limited to the words and pictures listed in the following table.

|                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>1-1 A column III Nitride transistor, comprising:</p> | <p><b>[Description]</b></p> <p><b><u>The feature 1-1 is disclosed by Comparison Document 1:</u></b></p> <p>Comparison Document 1 discloses a column III Nitride transistor.</p> <p><b><u>[Contents specifically disclosed by the Comparison Document]</u></b></p> <p><b><u>[see the second paragraph from the bottom on superscript page 2 of the specification of Comparison Document 1]</u></b></p> <p>"Some embodiments of the present invention provide Group III-nitride high electron mobility transistors and methods of fabricating Group III-nitride high electron mobility transistors..."</p> <p><b><u>[see the last paragraph on superscript page 9 of the specification of Comparison Document 1]</u></b></p> <p><b><u>Document 1]</u></b></p> <p>"Embodiments of the present invention may be particularly well suited for use in nitride-based devices such as Group III-nitride based HEMTs. As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In)."</p> |
| <p>1-2 a substrate,</p>                                 | <p><b>[Description]</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

## Attachment

TWO



**The features 1-2 is disclosed by Comparison Document 1:**

The substrate disclosed by Comparison Document 1 is equivalent to the substrate of claim 1.

**[Contents specifically disclosed by the Comparison Document]**

**[see the last paragraph on superscript page 12 of the specification, and FIG. 2A of Comparison Document 1]**

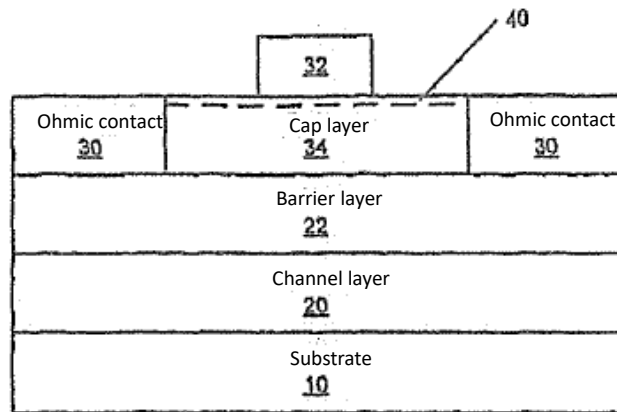


**FIG. 2A**

"Turning to Figs. 1A and 1B, a substrate 10 is provided on which nitride based devices may be formed. In particular embodiments of the present invention, the substrate 10 may be a semi-insulating silicon carbide (SiC) substrate that may be, for example, 4H polytype of silicon carbide.

Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes."

**[see the second paragraph from the bottom on superscript page 13 of the specification of Comparison Document 1]**

"Although silicon carbide may be used as a substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like."

1-3 a set of III-N  
(column III  
Nitride) Transition  
layers above the  
substrate,

**[Description]**

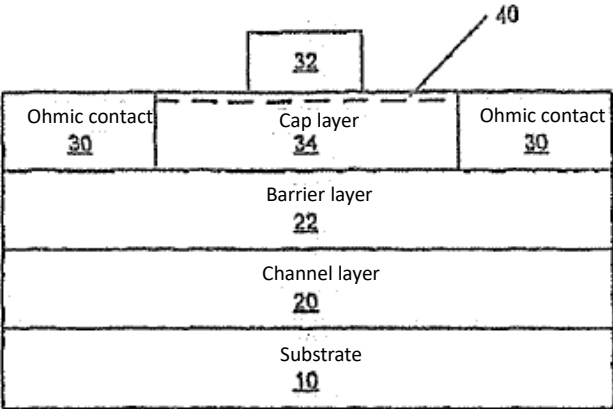
**The feature 1-3 is disclosed by Comparison Document 1:**

Comparison Document 1 discloses an AlN buffer layer (not shown in the figures), which is equivalent to the transition layer of claim 1. According to the specification (see paragraph 0025 of the Subject Patent), the transition layer of the Subject Patent may include AlN.

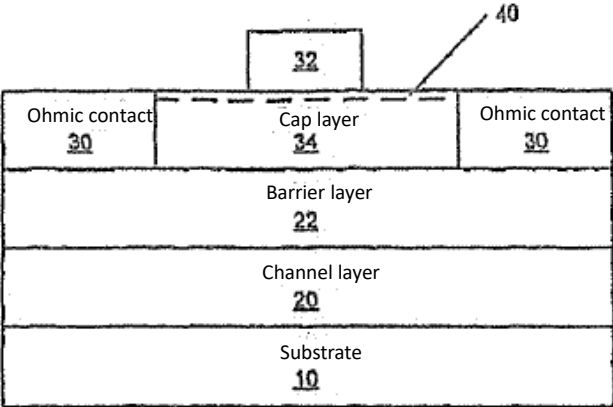
**[Contents specifically disclosed by the Comparison Document]**

## Attachment

101

|                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                              | <p><b><u>[see paragraph 2 on superscript page 13 of the specification of Comparison Document 1]</u></b></p> <p>"Optional buffer, nucleation and/or transition layers (<u>not shown</u>) may be provided on the substrate 10. For example, <u>an AlN buffer layer may be provided</u> to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device."</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1-4 a III-N buffer layer above the set of transition layers, | <p><b>[Description]</b></p> <p><b><u>The feature 1-4 is disclosed by Comparison Document 1:</u></b></p> <p>Comparison Document 1 discloses a channel layer 20 (channel layer 20 is a Group III nitride), which is equivalent to the III-N buffer layer of claim 1.</p> <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b><u>[see the last paragraph on superscript page 13 to paragraph 2 on superscript page 14 of the specification, and FIG. 2A of Comparison Document 1]</u></b></p> <div style="text-align: center;">  </div> <p><b>FIG. 2A</b></p> <p>"Returning to Figs. 1A and 1B, a channel layer 20 is provided on the substrate 10. The channel layer 20 may be deposited on the substrate 10 using buffer layers, transition layers, and/or nucleation layers as described above...</p> <p>In some embodiments of the present invention, <u>the channel layer 20 is a Group III-nitride</u>, such as <math>\text{Al}_x\text{Ga}_{1-x}\text{N}</math> where <math>0 \leq x &lt; 1</math>, provided that the energy of the conduction band edge of the channel layer 20 is less than the energy of the conduction band edge of the barrier layer 22 at the interface between the channel and barrier layers. In certain embodiments of the present invention, <math>x=0</math>, indicating that the channel layer 20 is GaN. The channel layer 20 may also be other Group III-nitrides such as InGa<sub>3</sub>N, AlInGa<sub>3</sub>N or the like. The channel layer 20 may be undoped (unintentionally doped) and may be grown to a thickness of greater than about 20 Å."</p> |

## Attachment

|                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>1-5 a III-N barrier layer above the buffer layer,</p>    | <p><b>[Description]</b></p> <p><b><u>The feature 1-5 is disclosed by Comparison Document 1:</u></b></p> <p>Comparison Document 1 discloses that the barrier layer 22 (the barrier layer 22 may be a Group III nitride), which corresponds to the III-N barrier layer of claim 1.</p> <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b><u>[see the last two paragraphs on superscript page 14 of the specification, and FIG. 2A of Comparison Document 1]</u></b></p> <div style="text-align: center;">  </div> <p><b>FIG. 2A</b></p> <p>"A barrier layer 22 is provided on the channel layer 20. The channel layer 20 may have a bandgap that is less than the bandgap of the barrier layer 22 and the channel layer 20 may also have a larger electron affinity than the barrier layer 22. The barrier layer 22 may be deposited on the channel layer 20. In certain embodiments of the present invention, the barrier layer 22 is AlN, AlInN, AlGa<sub>N</sub> or AlInGa<sub>N</sub> with a thickness of between about 0.1 nm and about 40 nm.</p> <p><u>The barrier layer 22 may be a Group III-nitride and has a bandgap larger than that of the channel layer 20 and a smaller electron affinity than the channel layer 20."</u></p> |
| <p>1-6 a compensated GaN layer above the barrier layer,</p> | <p><b>[Description]</b></p> <p><b><u>The feature 1-6 is disclosed by Comparison Document 1:</u></b></p> <p>The cap layer 34 disclosed by Comparison Document 1 is based on such as the GaN layer or GaAlN layer,</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

## Attachment

and

Wherein the doped region 40 is doped with a p-type dopant (e.g., Mg, etc.), and the cap layer 34 in the embodiment in which the passivation layer is not provided has a highly compensated semi-insulating property, which corresponds to the compensated GaN layer of claim 1.

**Specific reasons are as follows:**

Comparison Document 1 cites Annex 14-1 (US2005145874A1)

and Annex 9 (US6498111) in their entirety, and hydrogen passivation is unavoidable or is an intrinsic defect and impurity when p-type dopants (e.g., Mg, etc.) are used in doped region 40.

According to Annex 9, the purpose of providing the passivation layer is to reduce the degree of hydrogen passivation in the p-GaN instead of the annealing process. For the embodiment in which the passivation layer is not provided, i.e., corresponding to the embodiment in which no passivation layer is provided for the cap layer p-GaN, no other technical means of reducing the degree of hydrogen passivation is provided in the embodiment either according to Comparison Document 1. Thus, the cap layer p-GaN of the embodiment is apparently highly compensated for the semi-insulating nature of the p-GaN.

**[Contents specifically disclosed by the Comparison Document]**

**[see paragraph 2 on superscript page 18 of the specification, and FIG. 2A of Comparison Document 1]**

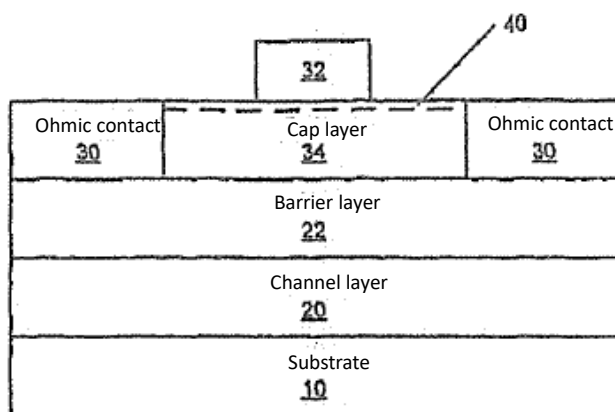
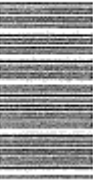


**FIG. 2A**

"Figs. 2A and 2B illustrate high electron mobility transistors having a cap layer 34, 34' according to further embodiments of the present invention. The substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30 and gate contact 32 may be provided as discussed above with reference to Figs. 1A and 1B. As seen in Figs. 2A and 2B, the cap layer 34, 34' includes a doped region 40 at or near the outer surface of the cap layer 34, 34'. The cap layer 34, 34' may be a GaN based cap layer, such as a GaN layer and/or an AlGaN layer as described, for example, in the patents and patent application incorporated by reference herein.

## Attachment

001



In some embodiments of the present invention, the doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C... Techniques for co-doping Group III-nitride materials are described, for example, in U.S. patent application Ser. No. 10/752,970, filed Jan. 7, 2004 entitled "CO-DOPING FOR FERMI LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES," the disclosure of which is incorporated herein as if set forth in its entirety."

**[see the last paragraph on superscript page 19 to paragraph 1 on superscript page 20 of the specification Comparison Document 1]**

"In other embodiments, the doped region 40 is a region doped with p-type dopants. In particular embodiments of the present invention without a gate recess, the doped region 40 extends into the cap layer 34 from about 2.5 Å to about 100 Å...with p-type dopants, the doped region 40 may provide a dopant concentration of from about  $10^{16}$  to about  $10^{22}$  cm<sup>-3</sup>. The p-type dopants may be Mg, Be, Zn, Ca and/or C... The level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant "surface" state but not so high as to provide introduce traps or leakage paths by becoming a conductive layer."

**[see paragraph 3 on superscript page 17 of the specification of Comparison Document 1]**

"A conventional passivation layer or a BN passivation layer as described below may also be provided on the structures of Figs. 1A and 1B. For example, a SiN layer and, in some embodiments, an extremely thin SiN layer, may be formed in situ. A MgN passivation layer, such as that described in U.S. Pat. No. 6,498,111 entitled "FABRICATION OF SEMICONDUCTOR MATERIALS AND DEVICES WITH CONTROLLED ELECTRICAL CONDUCTIVITY," the disclosure of which is incorporated herein by reference as if set forth in its entirety, could also be utilized."

**[see paragraph [0032] of Annex 14-1 as incorporated in Comparison Document 1 by reference]**

## Attachment

OR1



|                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                      | <p>"The Group III nitride layer may also be annealed, for example, to remove <u>native defects and impurities, such as hydrogen</u>, that may result from the co-doping of the semi-insulating Group III nitride layer. For example, a post growth nitrogen anneal could be performed on the Group III nitride layer."</p> <p><b><u>[see paragraphs 1 and 3 of column 1 and paragraph 2 of column 2 of Annex 9 as incorporated in Comparison Document 1 by reference]</u></b></p> <p>"The present invention provides a method of achieving the desired electrical conductivity in doped semiconductor materials that experience passivation. The invention specifically teaches methods of fabricating barrier layers to prevent or reduce the diffusion and incorporation of hydrogen into the semiconductor material, thus preventing or reducing dopant passivation."</p> <p>"During growth of GaN p-n junction diodes using Metal-Organic Chemical Vapor Deposition (MOCVD), it is difficult to grow a p-type material with good structural, optical, and electrical integrity. The p-type region of a GaN junction diode is commonly grown in a MOCVD reactor by adding magnesium (Mg) to achieve the desired conductivity. However, <u>a common problem is electrical passivation of acceptors like Mg, zinc (Zn), carbon (C) and others by hydrogen atoms</u>. The smaller hydrogen atoms diffuse into the GaN material, where they neutralize the Mg acceptors and the holes produced by the Mg. <u>The passivation process leaves the Mg acceptors inactive, resulting in the material becoming insulating or weakly p-type in its as grown state.</u>"</p> <p>"The presence of NH<sub>3</sub> during reactor cooling produces hydrogen and leads to passivation. As such, it was thought that the removal of all hydrogen sources was not practical and that passivation during reactor cooling could not be avoided."</p> |
| 1-7 a gate contact above the compensated GaN layer." | <p><b>[Description]</b></p> <p><b><u>The feature 1-7 is disclosed by Comparison Document 1:</u></b></p> <p>The gate contact 32 disclosed by Comparison Document 1 is equivalent to the gate contact of claim 1.</p> <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b><u>[see paragraph 2 on superscript page 18 of the specification, and FIG. 2A of Comparison Document 1]</u></b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

## Attachment

150

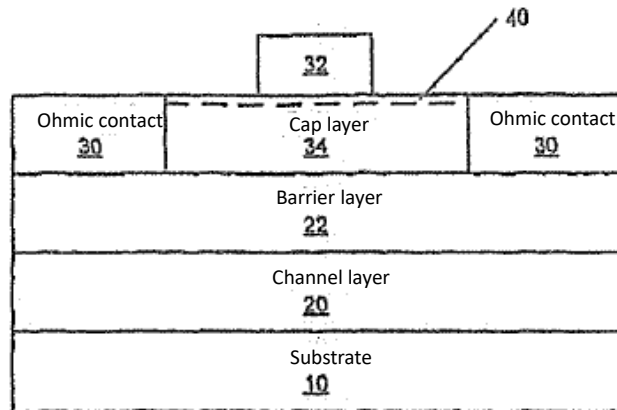


**FIG. 2A**

"Figs. 2A and 2B illustrate high electron mobility transistors having a cap layer 34, 34' according to further embodiments of the present invention. The substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30 and gate contact 32 may be provided as discussed above with reference to Figs. 1A and 1B. As seen in Figs. 2A and 2B, the cap layer 34, 34' includes a doped region 40 at or near the outer surface of the cap layer 34, 34'. The cap layer 34, 34' may be a GaN based cap layer, such as a GaN layer and/or an AlGaN layer as described, for example, in the patents and patent application incorporated by reference herein. In some embodiments of the present invention, the doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C...

Thus, Comparison Document 1 discloses all the technical features of claim 1. Both claim 1 and Comparison Document 1 belong to the same technical field, solve the same technical problem and bring about the same technical effect. Therefore, the technical solution claimed in claim 1 lacks novelty provided in Article 22(2) of the Chinese Patent Law.

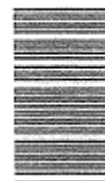
### **(1.2.) Claim 1 lacks novelty over Comparison Document 2.**

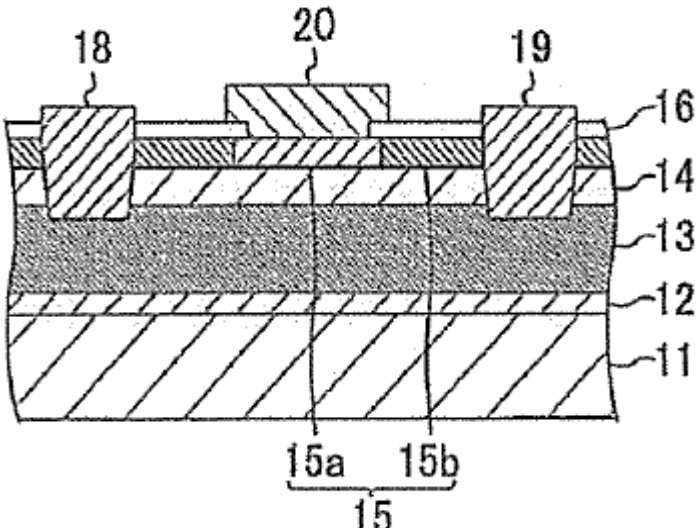
The correspondence between the features of claim 1 of the Subject Patent and the disclosure of Comparison Document 2 (US2008087915A1) is shown in the following table. It should be noted that the following table is only an exemplary enumeration, and the technical specifics disclosed in Comparison Document 2 are not limited to the words and pictures listed in the following table.

|                                                  |                                                                                                                                                                                 |
|--------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-1 A column III Nitride transistor, comprising: | <p><b>[Description]</b></p> <p><b><u>The feature 1-1 is disclosed by Comparison Document 2:</u></b></p> <p>Comparison Document 2 discloses a column III Nitride transistor.</p> |
|--------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Attachment

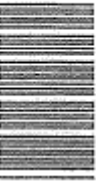
011

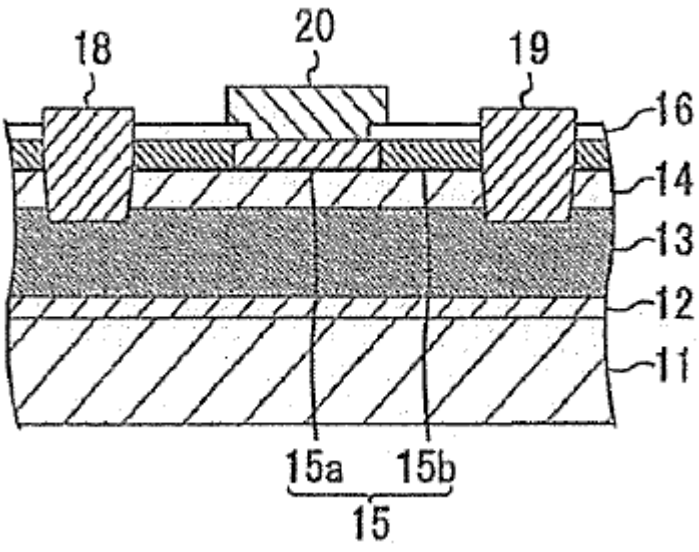


|                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                         | <p><b>[Contents specifically disclosed by the Comparison Document]</b><br/> <b><u>[see paragraph 0003 of the translation of Comparison Document 2]</u></b><br/>         "The present invention relates to nitride semiconductor transistors and their fabrication methods.<br/>         In particular, the present invention relates to normally-off type nitride semiconductor transistors applicable to power switching devices, and their fabrication methods."</p> <p><b><u>[see paragraph 0005 of the translation of Comparison Document 2]</u></b><br/>         "In recent years, field effect transistors (FET) made of gallium nitride (GaN)-based materials have been widely investigated for high frequency devices and high power devices."</p> |
| 1-2 a substrate,                        | <p><b>[Description]</b><br/> <b><u>The feature 1-2 is disclosed by Comparison Document 2:</u></b><br/>         The substrate 11 disclosed by Comparison Document 2 is equivalent to the substrate of claim 1.</p> <p><b>[Contents specifically disclosed by the Comparison Document]</b><br/> <b><u>[see FIG. 1 and paragraph 0031 of the translation of Comparison Document 2]</u></b><br/>         FIG.1</p>  <p>"Referring to FIG. 1, a <u>substrate 11</u> is made of silicon and its principal plane is the (111) plane. A buffer layer 12 of AlN having a thickness of 100 nm is formed on the principal plane of the substrate 11."</p>                         |
| 1-3 a set of III-N (column III Nitride) | <p><b>[Description]</b><br/> <b><u>The feature 1-3 is disclosed by Comparison Document 2:</u></b><br/>         Comparison Document 2 discloses an AlN buffer layer 12, which is equivalent to the transition layer of claim 1. According to the specification (see paragraph 0025 of the Subject Patent), the transition layer of the Subject Patent may include AlN.</p>                                                                                                                                                                                                                                                                                                                                                                                  |

## Attachment

001



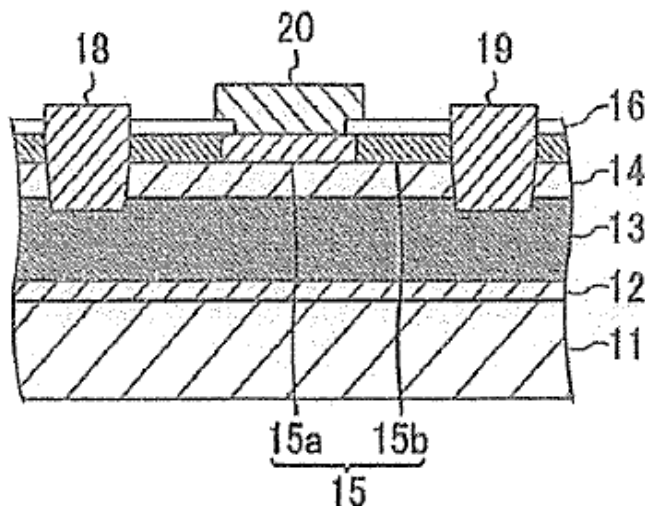
|                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>Transition layers<br/>above the<br/>substrate,</p>                           | <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b>[see FIG. 1 and paragraph 0031 of the translation of Comparison Document 2]</b></p> <p>FIG.1</p>  <p>"Referring to FIG. 1, a <u>substrate 11</u> is made of silicon and its principal plane is the (111) plane. A <u>buffer layer 12</u> of AlN having a thickness of 100 nm is formed on the principal plane of the substrate 11."</p> |
| <p>1-4 a III-N buffer<br/>layer above the<br/>set of transition<br/>layers,</p> | <p><b>[Description]</b></p> <p><b><u>The feature 1-4 is disclosed by Comparison Document 2:</u></b></p> <p>Comparison Document 2 discloses a first nitride semiconductor layer 13 of undoped GaN on a buffer layer 12, which is equivalent to the III-N buffer layer of claim 1.</p> <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b><u>[see FIG. 1 and paragraph 0032 of the translation of Comparison Document 2]</u></b></p>                                           |

# Attachment

0V1



FIG.1



"A first nitride semiconductor layer 13 of undoped GaN having a thickness of 2  $\mu\text{m}$  and a second nitride semiconductor layer 14 of undoped  $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$  having a thickness of 25 nm are formed on the buffer layer 12. A channel region of the transistor which will be described later is formed in the interface region between the first nitride semiconductor layer 13 and the second nitride semiconductor layer 14."

1-5 a III-N barrier layer above the buffer layer,

## [Description]

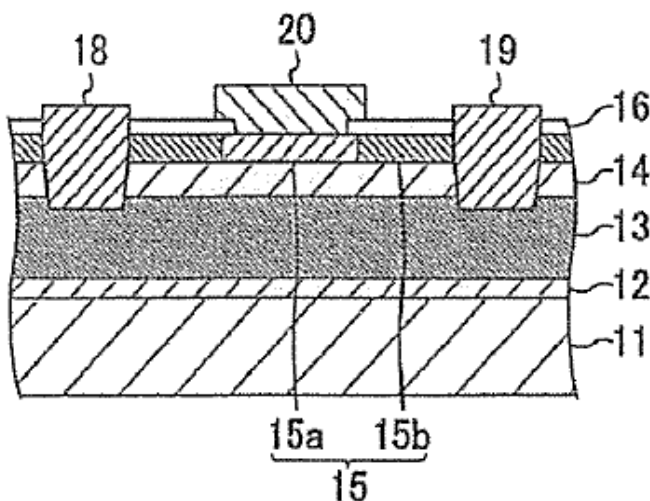
### The feature 1-5 is disclosed by Comparison Document 2:

Comparison Document 2 discloses a second nitride semiconductor layer 14 of undoped  $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$  as formed on the first nitride semiconductor layer 13, which corresponds to the III-N barrier layer of claim 1.

## [Contents specifically disclosed by the Comparison Document]

### [see FIG. 1 and paragraph 0032 of the translation of Comparison Document 2]

FIG.1



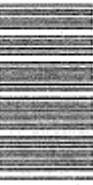
## Attachment



|                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                          | <p>"A first nitride semiconductor layer 13 of undoped GaN having a thickness of 2 <math>\mu\text{m}</math> and a <u>second nitride semiconductor layer 14</u> of undoped <math>\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}</math> having a thickness of 25 nm are formed on the buffer layer 12. A channel region of the transistor which will be described later is formed in the interface region between the first nitride semiconductor layer 13 and the second nitride semiconductor layer 14."</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1-6 a compensated GaN layer above the barrier layer, and | <p><b>[Description]</b></p> <p><b><u>The feature 1-6 is disclosed by Comparison Document 2:</u></b></p> <p>Comparison Document 2 discloses a third nitride semiconductor layer 15 formed on the second nitride semiconductor layer 14, which is equivalent to the compensated GaN layer of claim 1.</p> <p>The third nitride semiconductor layer 15 includes a high resistive region 15b in which Mg is not activated (in hydrogen passivation). Therefore, its resistance is higher than in the region 15a where Mg is activated. Although partial hydrogen passivation is eliminated in 15a by activation, hydrogen passivation cannot be completely eliminated (second point 2 of Article 1.1 of Chapter 1 of this Request). Alternatively, according to paragraph 0039, the Mg concentration after activation of 15a is set to about <math>1 \times 10^{19} \text{ cm}^{-3}</math>, while the carrier concentration is set to about <math>1 \times 10^{18} \text{ cm}^{-3}</math>, with a doping efficiency of 10%, and it is clear that a significant amount of hydrogen passivation is still present. Therefore, assuming that there is no specific limitation on the extent of hydrogen passivation in compensated GaN as asserted by the patentee in the U.S. Litigation, 15a is also a compensated GaN layer.</p> <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b><u>[see FIG. 1 and paragraph 0033 of the translation of Comparison Document 2]</u></b></p> <p>FIG.1</p> <p>"On the second nitride semiconductor layer 14, a <u>third nitride semiconductor layer 15</u> is formed which is made of <math>\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}</math> doped with magnesium (Mg) and has a thickness of 200 nm.</p> |

## Attachment

011



|                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                      | <p>The third nitride semiconductor layer doped with Mg is composed of: a control region 15a in which Mg is activated to exhibit a p-type conductivity; and a high resistive region 15b in which Mg is not activated to offer a higher resistance than the control region 15a. The control region 15a is formed in the shape of, for example, stripes each having a width of 1 <math>\mu\text{m}</math>."</p> <p><b><u>[see paragraph 0039 of the translation of Comparison Document 2]</u></b></p> <p>"The Mg concentration doped into the third nitride semiconductor layer 15 is set at about <math>1 \times 10^{19} \text{ cm}^{-3}</math>, and the carrier concentration in the control region 15a is set at about <math>1 \times 10^{18} \text{ cm}^{-3}</math>."</p> <p><b><u>[see paragraph 0046 of the translation of Comparison Document 2]</u></b></p> <p>"Hereinafter, a method for fabricating a transistor according to the first embodiment will be described. First, by a metal organic chemical vapor deposition (MOCVD) method, the buffer layer 12 of AlN, the first nitride semiconductor layer 13 of undoped GaN, and the second nitride semiconductor layer 14 of undoped Al<sub>0.15</sub>Ga<sub>0.85</sub>N are sequentially grown on the substrate 11. Thereafter, the third nitride semiconductor layer 15 of Al<sub>0.15</sub>Ga<sub>0.85</sub>N is grown with Mg doped as a p-type impurity. Then, the hydrogen diffusion barrier film 16 of AlN is formed."</p> <p><b><u>[see paragraph 0049 of the translation of Comparison Document 2]</u></b></p> <p>"When, for example, Mg is doped as a p-type impurity during crystal growth for the nitride semiconductor layer by a MOCVD method, Mg is introduced into the nitride semiconductor. However, <u>Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom.</u> When a thermal treatment is performed in an inert gas atmosphere at 800°C for about 20 to 60 minutes, the hydrogen atom is desorbed from Mg. Then, the Mg is activated, and thus the nitride semiconductor layer shows p-type conductivity.</p> |
| 1-7 a gate contact above the compensated GaN layer." | <p><b>[Description]</b></p> <p><b><u>The feature 1-7 is disclosed by Comparison Document 2:</u></b></p> <p>The gate electrode 20 disclosed by Comparison Document 2 is equivalent to the gate contact of claim 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

## 021



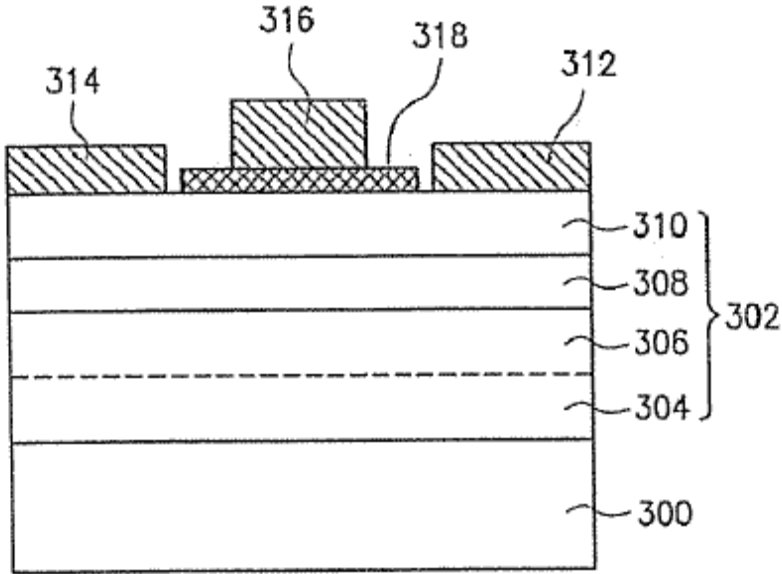
[see FIG. 1 and paragraph 0034 of the translation of Comparison Document 2]

"On the hydrogen diffusion barrier film 16, a gate electrode 20 is formed to cover the opening. The gate electrode 20 is made of palladium (Pd), and comes into ohmic contact with the control region 15a."

**(1.3.) Claim 1 lacks novelty over Comparison Document 3.**

|                                                         |                                                                                                                                                                                                                                                                                                                                                                    |
|---------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>1-1 A column III Nitride transistor, comprising:</p> | <p><b>[Description]</b></p> <p><b><u>The feature 1-1 is disclosed by Comparison Document 3:</u></b></p> <p>Comparison Document 3 discloses a column III Nitride transistor.</p>                                                                                                                                                                                    |
|                                                         | <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b>[see paragraph 1 on subscript page 5 of the specification of Comparison Document 3]</b></p> <p>The present invention relates to a field effect transistor (FET) structure, and in particular to a field effect transistor structure having a GaN-based gate insulating layer.</p> |



|                                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>1-2 a substrate,</p>                                                               | <p><b>[Description]</b></p> <p><b>The feature 1-2 is disclosed by Comparison Document 3:</b></p> <p>The substrate 300 disclosed by Comparison Document 3 is equivalent to the substrate of claim 1.</p> <p><b>[Contents specifically disclosed by the Comparison Document]</b></p> <p><b><u>[see the second paragraph from bottom of subscript page 12 of the specification, and FIG. 5 of Comparison Document 3]</u></b></p>  <p><b>FIG. 5</b></p> <p>"FIG. 5 shows a schematic structure of a field-effect transistor according to a second preferred embodiment of the present invention. Referring to FIG. 5, a modulated doped field-effect transistor (MODFET) is composed of a gallium nitride substrate 300, a gallium nitride-based semiconductor layer 302, a gallium nitride-based open insulating layer 318, a source electrode 312, a drain electrode 314, and a gate electrode 316."</p> |
| <p>1-3 a set of III-N (column III Nitride) Transition layers above the substrate,</p> | <p><b>[Description]</b></p> <p><b><u>The feature 1-3 is disclosed by Comparison Document 3:</u></b></p> <p>Comparison Document 3 discloses a buffer layer 304, and when the layer 1=0, the buffer layer 304 is AlGaH, which is equivalent to the transition layer of claim 1. According to the specification (see paragraph 0025 of the Subject Patent), the transition layer of the Subject Patent may include AlGaH.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

## Attachment

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[Contents specifically disclosed by the Comparison Document]

[see the last paragraph on subscript page 12 to paragraph 1 on subscript page 13 of the specification, and FIG. 5 of Comparison Document 3]

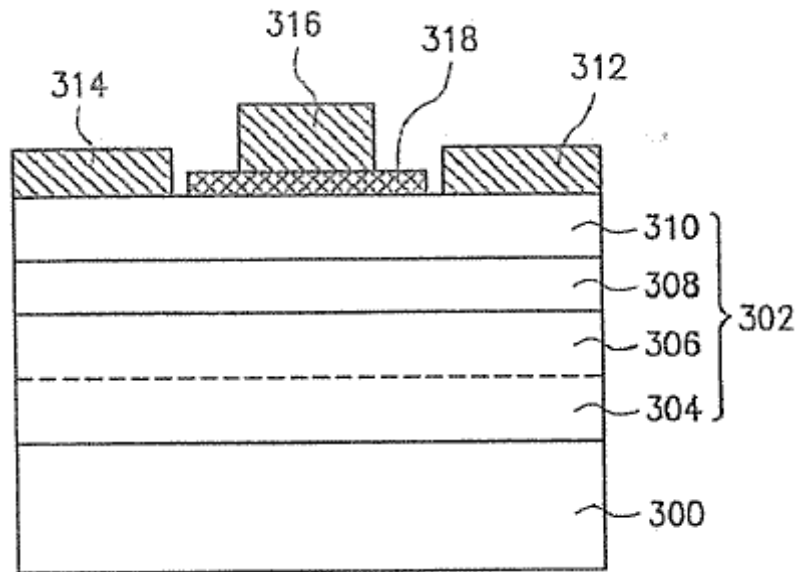


**FIG. 5**

Referring to FIG. 5, in the structure of the modulated doped field-effect transistor, the gallium nitride-based semiconductor layer 302, for example, is hastened by a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310, wherein the buffer layer 304 and the channel layer 306 are, for example, a doped  $A_{1-a}In_bGa_{1-a-b}N$  layer, and  $a \geq 0, b \geq 0, 1 \geq a + b, x > a$ ;

1-4 a III-N buffer layer above the set of transition layers,

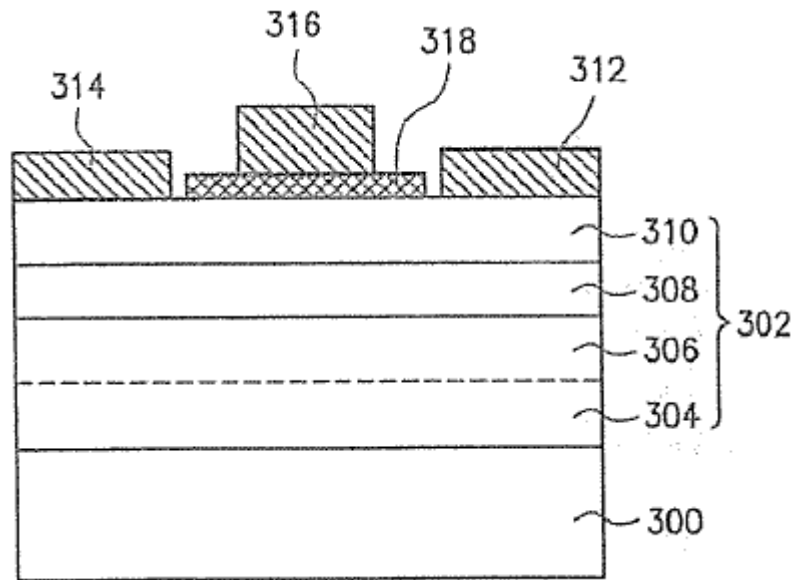
**[Description]**

**The feature 1-4 is disclosed by Comparison Document 3:**

Comparison Document 3 discloses a channel layer 306, which is equivalent to the III-N buffer layer of claim 1.

[Contents specifically disclosed by the Comparison Document]

[see the last paragraph on page 12 to paragraph 1 on page 13 of the specification, and FIG. 5 of Comparison Document 3]

**FIG. 5**

Referring to FIG. 5, in the structure of the modulated doped field-effect transistor, the gallium nitride-based semiconductor layer 302, for example, is hastened by a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310, wherein the buffer layer 304 and the channel layer 306 are, for example, a doped  $A_1aIn_bGal_{1-a-b}N_x$  layer, and  $a \geq 0$ ,  $b \geq 0$ ,  $1 \geq a + b$ ,  $x > a$ ;

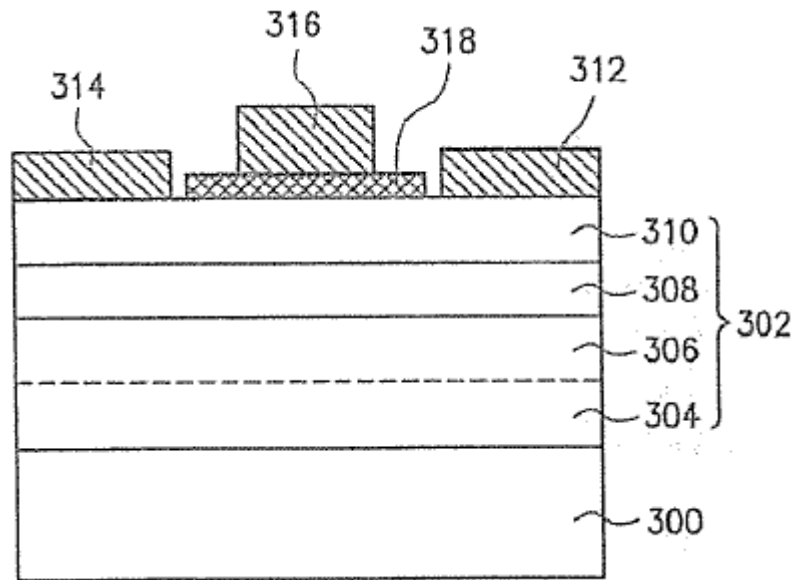
1-5 a III-N barrier layer above the buffer layer,

**[Description]****The feature 1-5 is disclosed by Comparison Document 3:**

Comparison Document 3 discloses a gap layer 308 and barrier layer 310, which corresponds to the III-N barrier layer of claim 1.

**[Contents specifically disclosed by the Comparison Document]**

**[see the last paragraph on subscript page 12 to paragraph 1 on subscript page 13 of the specification, and FIG. 5 of Comparison Document 3]**

**FIG. 5**

"Referring to FIG. 5, in the structure of the modulated doped field-effect transistor, the gallium nitride-based semiconductor layer 302, for example, is hastened by a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310, wherein the buffer layer 304 and the channel layer 306 are, for example, a doped  $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$  layer, and  $a \geq 0, b \geq 0, 1 \geq a + b, x > a$ ; the gap layer 308 is, for example, an undoped  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  layer with  $x \geq 0, y \geq 0, 1 \geq x + y$ ; and the barrier layer 310 is, for example, a silicon-doped  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  layer with  $x \geq 0, y \geq 0, 1 \geq x + y$ ."

1-6 a compensated GaN layer above the barrier layer, and

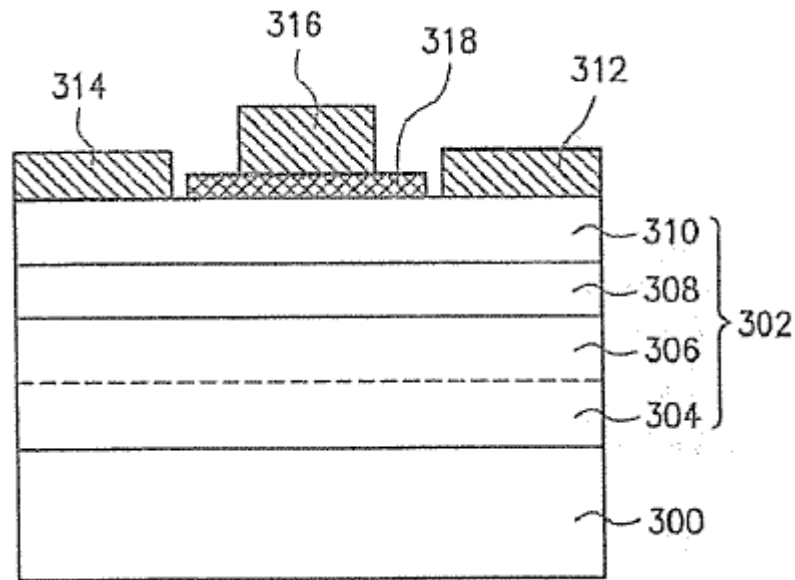
**[Description]****The feature 1-6 is disclosed by Comparison Document 3:**

Comparison Document 3 discloses a magnesium-doped gallium nitride-based gate insulating layer 318 provided on the barrier layer 310, which is equivalent to the compensated GaN layer of claim 1:

The magnesium-doped p-GaN layer having a high resistivity apparently utilizes the compensation or passivation effect of hydrogen on magnesium. That is, the p-GaN with insulating or semi-insulating properties due to hydrogen paving is implicitly disclosed in Comparison Document 3, i.e., the compensated GaN layer in the preferred embodiment of the Subject Patent.

**[Contents specifically disclosed by the Comparison Document]**

**[see the last paragraph on subscript page 12 to paragraph 2 on subscript page 13 of the specification, and FIG. 5 of Comparison Document 3]**

**FIG. 5**

"Referring to FIG. 5, in the structure of the modulated doped field-effect transistor, the gallium nitride-based semiconductor layer 302, for example, is hastened by a buffer layer 304, a channel layer 306, a gap layer 308, and a barrier layer 310, wherein the buffer layer 304 and the channel layer 306 are, for example, a doped  $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$  layer, and  $a \geq 0$ ,  $b \geq 0$ ,  $1 \geq a + b$ ,  $x > a$ ; the gap layer 3 is, for example, an undoped  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  layer with  $x \geq 0$ ,  $y \geq 1 \geq x + y$ ; and the barrier layer 310 is, for example, a silicon-doped  $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$  layer with  $x \geq 0$ ,  $y \geq 0$ ,  $1 \geq x + y$ .

Similar to the previous example, the gallium nitride-based open insulating layer 318 of this embodiment may also have a dopant to increase the resistance value of the gallium nitride-based dielectric layer 318 (between about 109 and 1012 ohms/ $\square$ ). This dopant may for example be a metal such as carbon, magnesium, iron, etc. or a combination thereof, and such dopant (carbon, iron and magnesium, etc.) is for example doped during the epitaxial process."

1-7 a gate contact above the compensated GaN layer."

**[Description]**

**The feature 1-7 is disclosed by Comparison Document 3:**

The gate electrode 316 disclosed by Comparison Document 3 is equivalent to the gate contact of claim 1.



[Contents specifically disclosed by the Comparison Document]

[see the second paragraph from bottom of subscript page 12 of the specification, and FIG. 5 of Comparison Document 3]

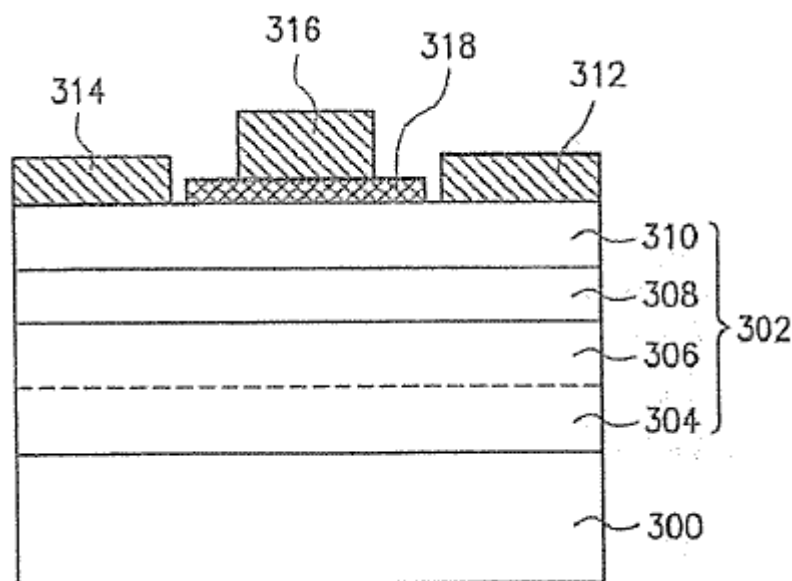


**FIG. 5**

"FIG. 5 shows a schematic structure of a field-effect transistor according to a second preferred embodiment of the present invention. Referring to FIG. 5, a modulated doped field-effect transistor (MODFET) is composed of a gallium nitride substrate 300, a gallium nitride-based semiconductor layer 302, a gallium nitride-based open insulating layer 318, a source electrode 312, a drain electrode 314, and a gate electrode 316."

Thus, Comparison Document 3 discloses all the technical features of claim 1. Both claim 1 and Comparison Document 3 belong to the same technical field, solve the same technical problem and bring about the same technical effect. Therefore, the technical solution claimed in claim 1 lacks novelty provided in Article 22(3) of the Chinese Patent Law.

**(2) Claims 2-3 lack novelty provided in Article 22(2) of the Chinese Patent Law.**

Claim 2 refers claim 1, and its additional technical feature is "wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen".

Claim 3 further defines claim 2, and its additional technical feature is "the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca."

**(2.1.) The additional technical features of claims 2-3 have been disclosed by Comparison Document 1.**

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Comparison Document 1 discloses following technical features (see paragraph 2 on superscript page 18 of the specification of Comparison Document 1): "in some embodiments of the present invention, the doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C."

The Annex 9 as incorporated in Comparison Document 1 by Comparison Document discloses following contents (see paragraph 3 of column 1): "during growth of GaN p-n junction diodes using Metal-Organic Chemical Vapor Deposition (MOCVD), it is difficult to grow a p-type material with good structural, optical, and electrical integrity. The p-type region of a GaN junction diode is commonly grown in a MOCVD reactor by adding magnesium (Mg) to achieve the desired conductivity. However, a common problem is electrical passivation of acceptors like Mg, zinc (Zn), carbon (C) and others by hydrogen atoms. The smaller hydrogen atoms diffuse into the GaN material, where they neutralize the Mg acceptors and the holes produced by the Mg. The passivation process leaves the Mg acceptors inactive, resulting in the material becoming insulating or weakly p-type in its as grown state."

Thus, there is bound to be hydrogen passivation of the above receptors by hydrogen for GaN layers doped with Mg, Be, Zn, Ca and other receptors.

Comparison Document 1 gives different embodiments, such as a technical solution with a passivation layer and an implementation without a passivation layer, wherein the passivation layer (e.g. a hydrogen absorbing layer) is provided as an alternative to the annealing process with the purpose of mitigating the hydrogen passivation of P-GaN when Mg is used as an acceptor. Obviously, the content of providing no passivation layer or annealing of the p-GaN cap layer actually discloses the solution of "magnesium and other acceptor type dopant atoms passivated with hydrogen".

Furthermore, assuming that the degree of hydrogen passivation in the compensated GaN is not specifically limited as claimed by the patentee in the U.S. litigation, the extent of hydrogen passivation in the compensated GaN is not limited even if a passivation layer is provided. Even if a passivation layer is installed or an annealing operation is performed on the p-GaN cover layer, hydrogen passivation remains, which is equivalent to disclosing "magnesium and other acceptor type dopant atoms passivated with hydrogen".

### **(2.2.) The additional technical features of claims 2-3 have been disclosed by Comparison Document 2.**

Comparison Document 2 discloses that (see paragraph 0049 of the translation of Comparison Document 2): Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom (that is, acceptor type dopant atoms passivated with hydrogen); "when, for example, Mg is doped as a p-type impurity during crystal growth for the nitride semiconductor layer by a MOCVD method, Mg is introduced into the nitride semiconductor. However, Mg introduced into the nitride semiconductor is inactivated in which it is combined with a hydrogen atom.

## Attachment



### **(2.3.) The additional technical features of claims 2-3 have been disclosed by Comparison Document 3.**

Comparison Document 3 discloses that (see paragraph 2 on page 13 of the specification of Comparison Document 3 ): when Mg is introduced into a nitride semiconductor, the nitride semiconductor into which Mg is introduced exhibits insulating or semi-insulating high resistivity characteristics. For a person having ordinary skill in the art, the high resistivity is derived from the hydrogen passivation. "Similar to the previous example, the gallium nitride-based open dielectric layer 318 of this embodiment may also have a dopant to increase the resistance value of the gallium nitride-based dielectric layer 318 (between about 10<sup>9</sup> and 10<sup>12</sup> ohms/□). This dopant may for example be a metal such as carbon, magnesium, iron, etc. or a combination thereof, and such dopant (carbon, iron and magnesium, etc.) is for example doped during the epitaxial process."

Thus, the additional technical features of claims 2-3 have been disclosed by Comparison Document s 1-3. Therefore, since the cited claim 1 lacks novelty over Comparison Document s 1-3, dependent claims 2-3 lack novelty provided in Article 22(2) of the Chinese Patent Law over Comparison Document 1.

### **5. Claims 1-3 lack inventiveness provided in Article 22(3) of the Chinese Patent Law.**

#### **(1) Independent claim 1 lacks inventiveness provided in Article 22(3) of the Chinese Patent Law.**

##### **(1.1.) Taking Comparison Document 1 as the most relevant prior art**

##### **(1.1.1.) Claim 1 lacks inventiveness over Comparison Document 1 and the combination of Comparison Document 1 and common knowledge.**

As described in Article 1.1 of Chapter 4 herein, Comparison Document 1 has disclosed all of the technical features of claim 1, and claim 1 lacks novelty over Comparison Document 1. Claims 1 lacks inventiveness over Comparison Document 1 under a case where claim 1 lacks novelty over Comparison Document 1. Assuming that patentee contends that there is a minor difference between claim 1 and Comparison Document 1, the difference is also common knowledge in the art.

##### **(1.1.2.) Claim 1 lacks inventiveness over Comparison Document 1 and Comparison Document 2/3 or further the combination with common knowledge.**

It is assumed that the patentee asserts that Comparison Document 1 does not disclose the provision of a compensated GaN layer between the barrier layer and the gate level contact, i.e., assuming that the features 1.6-1.7 are distinguishing technical features. The above distinguishing technical features are disclosed by Comparison Document 2/3, or can be obtained by combining common knowledge under the teaching of Comparison Document 2/3.

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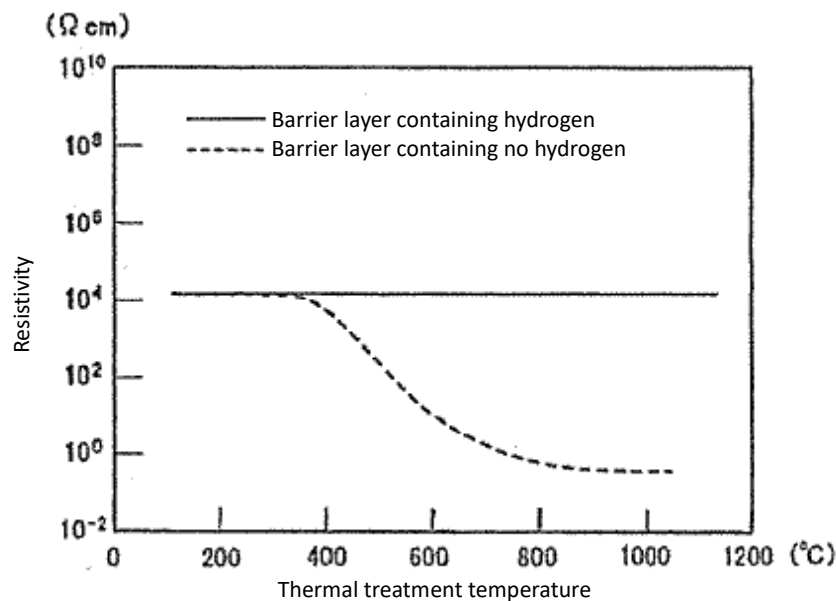


(1.1.2.1.) Comparison Document 2 discloses the distinguishing technical features, or Comparison Document 2 discloses the distinguishing technical feature in combination with common knowledge.

The distinguishing technical feature is disclosed by Comparison Document 2 (see opinions in Article 1.2 of Chapter 4).

Further, Comparison Document 2 further discloses that different temperature settings for the thermal treatment (also known as activation and annealing) may lead to different electrical resistivity (see paragraph 0050 of the translation of Comparison Document 2): "FIG. 4 shows the correlation between the temperature of the thermal treatment and the resistivity in the case where an  $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$  layer doped with Mg to have a concentration of about  $1 \times 10^{19} \text{ cm}^{-3}$  is subjected to a thermal treatment. The thermal treatment was performed in a nitrogen atmosphere for 20 minutes. As shown in FIG. 4, in the case of forming no hydrogen diffusion barrier film of AlN, the resistivity of the Mg doped  $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$  layer decreases with an increasing temperature of the thermal treatment, and becomes almost constant at around 800 °C."

FIG. 4



When Mg is doped as a p-type impurity during crystal growth of a nitride semiconductor layer by a conventional process (e.g., MOCVD), the Mg introduced into the nitride semiconductor is deactivated due to bonding with hydrogen atoms and thus first assumes a high resistivity state (insulator or semi-insulator). In addition, a person having ordinary skill in the art can adjust the parameters of subsequent annealing/activation/heating, or perform no annealing/activation/heating, so as to obtain a nitride semiconductor of desired resistivity. Thus, it belongs to a technique well known by a person having ordinary skill in the art prior to the priority date that the Mg introduced into a nitride semiconductor is passivated by hydrogen, and the ability to reduce or retain hydrogen purification can enable a nitride semiconductor to exhibit a different resistivity, which does not belong to the contribution to the prior art by the Subject Patent.

(1.1.2.2.) Comparison Document 3 discloses the distinguishing technical feature, or Comparison Document 3 discloses the distinguishing technical feature in combination with common knowledge.

The distinguishing technical feature is disclosed by Comparison Document 3 (see opinions in Article 1.3 of Chapter 4).

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Further, Comparison Document 3 discloses that when Mg is doped as a p-type impurity during the crystal growth (crystal epitaxial fabrication process) of a nitride semiconductor layer, the doping makes the nitride semiconductor layer exhibit a high resistivity state (insulator or semi-insulator). Therefore, when a person having ordinary skill in the art wishes to provide an insulator or semi-insulator (i.e., to form a MISFET) between a gate electrode and a barrier layer (semiconductor), it is possible to obtain a nitride semiconductor with a high resistivity by doping Mg as a p-type impurity during the crystal growth (epitaxial fabrication) of a nitride semiconductor layer, as described in the Comparison Document 3. It is known to a person having ordinary skill in the art that the reason for the high resistivity at this time is the passivation of Mg by hydrogen.

### **(1.2.) Taking Comparison Document 2 as the most relevant prior art**

#### **(1.2.1.) Claim 1 lacks inventiveness over Comparison Document 2 and the combination of Comparison Document 2 and common knowledge.**

As described in Article 1.2 of Chapter 4 herein, Comparison Document 2 has disclosed all of the technical features of claim 1, and claim 1 lacks novelty over Comparison Document 2. Claim 1 lacks inventiveness over Comparison Document 2 under a case where claim 1 lacks novelty over Comparison Document 2. Assuming that patentee contends that there is a minor difference between claim 1 and Comparison Document 2, the difference is also common knowledge in the art.

#### **(1.2.2.) Claim 1 lacks inventiveness over Comparison Document 2 and Comparison Document 1/3 or further the combination with common knowledge.**

It is assumed that the patentee asserts that Comparison Document 2 does not disclose the provision of a compensated GaN layer between the barrier layer and the gate level contact, i.e., assuming that the features 1.6-1.7 are distinguishing technical features. The above distinguishing technical features are disclosed by Comparison Document 1/3, or can be obtained by combining common knowledge under the teaching of Comparison Document 1/3.

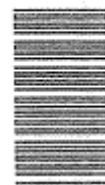
**(1.2.2.1.)** Comparison Document 1 discloses the distinguishing technical feature, or Comparison Document 1 discloses the distinguishing technical feature in combination with common knowledge.

The distinguishing technical feature is disclosed by Comparison Document 1 (see opinions in Article 1.1 of Chapter 4).

Comparison Document 1 discloses that hydrogen passivation cannot be avoided when Mg is doped as a p-type impurity during crystal growth of a nitride semiconductor layer by a conventional process (e.g., MOCVD). Comparison Document 1 discloses that a person having ordinary skill in the art can reduce the degree of hydrogen passivation of magnesium by providing a passivation layer or by an annealing process. In fact, it also discloses a solution without annealing and without providing a passivation layer. According to the solution disclosed in Comparison Document 1, a person having ordinary skill in the art can clearly know the reason for the formation of high resistivity when Mg is doped as a p-type impurity during crystal growth of a nitride semiconductor layer, and the different methods for obtaining the desired resistivity.

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**(1.2.2.2.)** Comparison Document 3 discloses the distinguishing technical features, or Comparison Document 3 discloses the distinguishing technical feature in combination with common knowledge (see the contents of Section 1.1.2.2 of this chapter).

### **(1.3.) Taking Comparison Document 3 as the most relevant prior art**

#### **(1.3.1.) Claim 1 lacks inventiveness over Comparison Document 3 and the combination of Comparison Document 3 and common knowledge.**

As described in Article 1.3 of Chapter 4 herein, Comparison Document 3 has disclosed all of the technical features of claim 1, and claim 1 lacks novelty over Comparison Document 3. Claims 3 lacks inventiveness over Comparison Document 1 under a case where claim 1 lacks novelty over Comparison Document 3. Assuming that patentee contends that there is a minor difference between claim 1 and Comparison Document 3, the difference is also common knowledge in the art.

#### **(1.3.2.) Claim 1 lacks inventiveness over Comparison Document 2 and Comparison Document 1/3 or further the combination with common knowledge.**

It is assumed that the patentee asserts that Comparison Document 3 does not disclose the provision of a compensated GaN layer between the barrier layer and the gate level contact, i.e., assuming that the features 1.6-1.7 are distinguishing technical features. The above distinguishing technical features are disclosed by Comparison Document 1/2, or can be obtained by combining common knowledge under the teaching of Comparison Document 1/2.

**(1.3.2.1.)** Comparison Document 1 discloses the distinguishing technical features, or Comparison Document 1 discloses the distinguishing technical feature in combination with common knowledge (see Article 1.2. 2.1 of this chapter).

**(1.3.2.2.)** Comparison Document 2 discloses the distinguishing technical features, or Comparison Document 2 discloses the distinguishing technical feature in combination with common knowledge (see the contents of Section 1. 1. 2. 1 of this chapter).

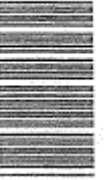
### **(2) Claims 2-3 lack inventiveness as provided in Article 22(3) of the Chinese Patent Law.**

The additional technical features of claims 2-3 have been disclosed by Comparison Document 1/Comparison Document 2/Comparison Document 3 (see Section 2 of Chapter 4). Therefore, since the cited claim lacks inventiveness, claims 2-3 lack inventiveness provided in Article 22(3) of the Chinese Patent Law, either.

# Attachment

## Chapter IV Conclusion

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In summary, the technical solutions corresponding to claims 1-3 are not sufficiently disclosed in the specification, so it does not comply with Article 26(3) of the Chinese Patent Law; the claims are not supported by the specification and thereby not in conformity with Article 26(4) of the Chinese Patent Law; claims 1-3 are not clear, so it does not comply with Rule 20(1) of Implementing Regulations of the Chinese Patent Law; claims 1-3 lack novelty provided in Article 22(2) of the Chinese Patent Law; and claims 1-3 lack inventiveness as provided in Article 22(3) of the Chinese Patent Law. Thus, the petitioner earnestly requests your office to declare all the patent rights invalid.

Respectfully submitted.