

CERTIFICATE OF TRANSLATION ACCURACY

I am a professional reviewer and editor specializing in translating Chinese, Japanese and Korean to English and vice versa.

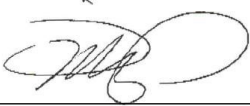
I served as Chief Examiner of the certified court interpreter test for the State of California and as a contract translator and interpreter for various federal agencies through the U.S. Department of State of for more than a decade. I served as an instructor at the University of California at Berkeley and the Middlebury Institute of International Studies at Monterey Graduate Program in Translation.

I have more than 30 years of experience translating thousands of technical, legal, and business documents from Korean to English submitted to, among others, Chinese judicial authorities, U.S. federal courts, the U.S. International Trade Commission (ITC), and the USPTO Patent Trial and Appeal Board (PTAB).

I certify that the following document translated from Chinese into the English language is a true, correct, and complete translation of the corresponding source text to the best of my knowledge and ability.

I certify under penalty of perjury that the foregoing is true and correct.

Executed this 9th day of May 2024 in Contra Costa County of the State of California.

By: 

Alex N. Jo
Member, ATA



China National Intellectual Property Administration

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Date of issuance:

April 30, 2024



Application or Patent Number: 201080015425.X

Issuance SN: 2024042601308110

Case Number: 4W116886

Title of Invention/Creation: Compensated gate MISFET and method for fabricating the same

Patentee: Efficient Power Conversion Corporation

Invalidation Petitioner: Innoscience (Suzhou) Technology Co., Ltd.

Decision on Invalidation Request

(No. 567338)

Pursuant to the provisions of Article 46.1 of the Chinese Patent Law, the China National Intellectual Property Administration has examined the invalidation request filed by the invalidation petitioner for the aforementioned patent right and hereby makes the following decision:

- ☐ The patent right is declared invalid in full.
☐ The patent right is declared partially invalid.
☒ The patent right is maintained valid.

Pursuant to the provisions of Article 46.2 of the Chinese Patent Law, any party dissatisfied with this decision may file a lawsuit with the Beijing Intellectual Property Court within three months from the date of receipt of this notification, and the opposing party shall participate in the lawsuit as a third party.

Attached: The main text of the decision consists of 12 pages (starting from Page 2).

Panel Chair: Lifang Liu

Primary Examiner: Jie Xiong

Participating Examiner: Xiaodong Fan

seal affixed *Seal for Patent Reexamination
and Invalidation Services of the China
National Intellectual Property
Administration
1101081361184*

Reexamination and Invalidation Department of the Patent Office

- 201019 Paper Application: Please send any replies to the Reexamination and Invalidation Department of the China National Intellectual Property Administration, No. 6 Xitucheng Road, Jimenqiao, Haidian District, Beijing 10088
- 2022.10 Electronic Application: Related documents should be submitted in electronic form through the patent business processing system. Unless otherwise specified, documents submitted in paper or other formats will be considered as not submitted.

Decision on Invalidation Request of the China National Intellectual Property Administration (No. 567338)



Case Number	No. 4W116886
Decision Date	April 23, 2024
Title of Invention/Creation	Compensated gate MISFET and method for fabricating the same
International Classification Number	H01L29/778
Invalidation Petitioner	Innoscience (Suzhou) Technology Co., Ltd.
Patentee	Efficient Power Conversion Corporation
Patent Number	201080015425.X
Filing Date	April 7, 2010
Priority Date	April 8, 2009
Date of Authorized Publication	July 30, 2014
Invalidation Request Date	October 11, 2023
Legal Basis	Articles 26.3, 26.4, 22.2 and 22.3 of the Chinese Patent Law Rule 20.1 of the Implementing Rules of the Chinese Patent Law

Key Points of the Decision:

If a person skilled in the art can realize the technical solution claimed in the claim based on the statements in the description, it should be considered that the description involved in the claim meets the requirements of sufficient disclosure.

If the technical solution of the claim can be generalized from the content disclosed in the description, the claim can be supported by the description.

If the protection scope of the technical solution of the claim can be clearly defined for a person skilled in the art, the protection scope of the claim is clear.

The claim has distinctive features relative to the closest prior art, and if such distinctive features are not disclosed by other prior art, and there is no evidence that they are common knowledge in the art, and such distinctive features provide beneficial technical effects to the technical solution of the claim, then the claim possesses inventiveness.



I. Cause of action

The patent number of the present patent is 201080015425.x, the application date is April 7, 2010, the priority date is April 8, 2009, and the authorized publication date is July 30, 2014. The claims at the time of authorized publication of the present patent are as follows:

1. A column III Nitride transistor comprising:

a substrate,

a set of III-N (column III Nitride) transition layers above the substrate,

a III-N buffer layer above the set of transition layers,

a III-N barrier layer above the buffer layer,

a compensated GaN layer above the barrier layer, and

a gate contact above the compensated GaN layer.

2. The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.

3. The transistor of claim 2, wherein the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.

Innoscence (Suzhou) Technology Co., Ltd. (hereinafter referred to as the petitioner) filed an invalidation request to the China National Intellectual Property Administration on October 11, 2023 on the ground that: the description does not clearly record the technical solutions sought to be protected in claims 1-3 of the present patent, which is inconsistent with the provisions of Article 26.3 of the Chinese Patent Law; claims 1-2 are not supported by the description, which is inconsistent with the provisions of Article 26.4 of the Chinese Patent Law; the scope of protection of claim 1 is unclear, which is inconsistent with the provisions of Article 20.1 of the Implementing Regulations of the Chinese Patent Law; and claims 1-3 do not meet the provisions of Articles 22.2 and 22.3 of the Chinese Patent Law. The petitioner requested that claims 1-3 of the present patent be declared invalid in their entirety, and submitted the following attachments as evidences:

Attachment 1: "Physics and Devices of Semiconductors" edited by Shuyuan Lv, et. al., published by Xidian University Publishing House, pages 59-65 of the main text, publication date: February 2017;

Attachment 2: "Physics of Semiconductors and Films" compiled by Zhengzhong Yun, et. al., Chengdu Telecommunication Engineering Institute, National Defense Industry Press, pages 8-10 of the main text, publication date: August 1981;

Attachment 3: The Reexamination Decision No. 104791 of the China National Intellectual Property Administration, date of decision: January 15, 2016;

Attachment 4: "Characteristics of Impurities and Defects in GaN", Jinxing Shi, "Semiconductor Information", Volume 35, Issue 1, publication date: February 1998;

Attachment 5: "Fundamentals of Solid-State Electronics" written by Sze (US), translated by Gang Ruan, et al., published by Fudan University Press, pages 1-10 of the main text, publication date: April 2003;

Attachment 6: "Physics of Semiconductors" edited by Enke Liu, Bingsheng Zhu et al., Xi'an Jiaotong University, National Defense Industry Press, pages 54-57 of the main text, publication date: December 1979;

Attachment 7: "Operating Principles and Manufacturing Technology of Power Semiconductor Devices" written by S.K. Ghandhi (US), translated by Guanghua Zhang and Shuqian Zhong, published by China Machine Press, pages 8-12 of the main text, publication date: September 1982;

Attachment 8: "Properties and Testing of Insulating Materials with High-Voltage Test Equipment" edited by Shaojun Liu, published by Dadong Bookstore, pages 112-115 of the main text, publication date: July 1954;



Attachment 9: US6498111B1 and its Chinese translation, publication date: December 24, 2002;

Attachment 10: "p-Type Doping of GaN Materials", Shiyong Xie, et al., "Research and Progress in Solid-State Electronics", Volume 21, Issue 2, publication date: May 2001;

Attachment 11: "Research Progress on p-Type Doping Based on GaN Materials", Yibing Liu, Xinmin Huang, Anning Liu, et al., "Infrared Technology", Volume 30, Issue 3, March 2008;

Attachment 12: Infringement comparison table and its translation submitted by the patentee in the USITC 337 proceeding;

Attachment 13: Main content and instructions for use of the evidence for non-novelty, non-inventiveness, and non-usefulness in CN102365747B;

Attachment 14 (Attachment 14 and 14-1 are collectively referred to as D1): CN101107713A, publication date: January 16, 2008;

Attachment 14-1: US2005145874A1 referenced in Attachment 14 and its Chinese translation, publication date: July 7, 2005;

Attachment 15 (hereinafter referred to as D2): US2008/0087915A1 and its Chinese translation, publication date: April 17, 2008;

Attachment 16 (hereinafter referred to as D3): TW200414540A, publication date: August 1, 2004;

Attachment 17: The authorized announcement text of this patent, CN102365747B.

Having passed the formal examination, the China National Intellectual Property Administration accepted the above invalidation request on October 16, 2023, and established a panel to examine the case. The invalidation request and copies of the evidence were forwarded to the patentee.

In response to the above invalidation request, the patentee submitted an Observation on November 30, 2023, arguing that the invalidation grounds raised by the petitioner were unfounded and submitting the following counter-evidence:

Counter-Evidence 1: An Inter Partes Reexamination Request of the U.S. Patent No. US8350294 to the U.S. Patent and Trademark Office (IPR2023-01381), along with a partial Chinese translation.

The panel forwarded the Observation and counter-evidence to the petitioner on December 14, 2023.

On January 10, 2024, the panel issued oral hearing notification to both parties, scheduled for March 6, 2024.

The oral hearing was held as scheduled, with both parties entrusting agents to attend. During the oral hearing:

1. Both parties had no objections to the identity and qualifications of the opposing party's participants and did not request the withdrawal of any panel member or clerk.
2. It was clarified that the basis for the oral hearing was the authorized announcement text of the patent.
3. The petitioner indicated that Attachments 12-13 were for the panel's reference only and would not be used as evidence.
4. The patentee submitted the following counter-evidence during the oral hearing:

Counter-Evidence 2: "Principles of Electronic Circuits" (Volume 1), published by Machinery Industry Press, authored by Sanley G. Bums (U.S.), including the cover, copyright page, preface, introduction, directory, and pages 34-36 of the main text. Publication date: April 2001.

Counter-Evidence 3: "Terminology for Semiconductor Materials", Chinese National Standard GB/T14264-93, publication date: March 12, 1993.

The petitioner received the above counter-evidence on the spot.



5. The patentee had no objection to the authenticity and publication dates of Attachments 1-11, 14, 14-1, 15, and 16, as well as the accuracy of the Chinese translations of these attachments. The petitioner had no objection to the authenticity and publication dates of Counter-Evidence 1-3 submitted by the patentee, acknowledged that Counter-Evidence 2 can be used as common knowledge evidence, but believed that Counter-Evidence 3 cannot be used as common knowledge evidence.

6. The petitioner specified the arguments for invalidation as follows:

(1) The disclosure in the patent description is insufficient, involving claims 1-3, and does not comply with Article 26.3 of the Chinese Patent Law;

(2) Claims 1-2 are not supported by the description, and do not comply with Article 26.4 of the Chinese Patent Law;

(3) The scope of protection of claim 1 is unclear, and does not comply with Rule 20.1 of the Implementing Rules of the Chinese Patent Law;

(4) Claims 1-3 do not possess novelty as defined in Article 22.2 of the Chinese Patent Law relative to D1, D2, or D3;

(5) Claims 1-3 do not possess inventiveness. The specific evidence combinations are as follows ("+" indicates "combination"):

Independent claim 1: D1 + common knowledge; D1 + D2; D1 + D3; D1 + D2 + common knowledge; D1 + D3 + common knowledge. D2 + common knowledge; D2 + D1; D2 + D3; D2 + D1 + common knowledge; D2 + D3 + common knowledge. D3 + common knowledge; D3 + D1; D3 + D2; D3 + D1 + common knowledge; D3 + D2 + common knowledge.

Dependent claim 2: D1; D1 + common knowledge; D2; D2 + common knowledge; D3; D3 + common knowledge.

Dependent claim 3: D1; D1 + common knowledge; D2; D2 + common knowledge; D3; D3 + common knowledge.

At this point, the panel believes that the facts of the case are clear and a decision can be made.

II. Reasons for the Decision

1. Basis of Examination

The basis of this decision is the authorized announcement text of the patent.

2. Evidence Determination

The patentee has no objection to the authenticity and publication dates of Attachments 1-11, 14, 14-1, 15, and 16, as well as the accuracy of the Chinese translations of these attachments.

After review, the panel has not found any obvious flaws in Attachments 1-11, 14, 14-1, 15, and 16, so the authenticity and publication dates of these attachments are recognized.

Among them, D1-D3 (Attachments 14, 14-1, 15, 16) are patent documents, and their publication dates are prior to the priority date of the present patent, which can be used as prior art to evaluate the novelty and inventiveness of the present patent. The disclosed content of D1-D2 shall be based on the Chinese translation submitted by the petitioner.



Regarding Counter-Evidence 1-3 submitted by the patentee, the petitioner has no objection to the authenticity and publication dates of Counter-Evidence 1-3. After review, the panel has not found any obvious flaws in Counter-Evidence 1-3 and recognizes the authenticity and publication dates of Counter-Evidence 1-3. The petitioner acknowledges that Counter-Evidence 2 can be used as common knowledge evidence, but believes that Counter-Evidence 3 cannot be used as common knowledge evidence. Counter-Evidence 1 is a request for Inter Partes Review (IPR) of US Patent US8350294 from the United States Patent and Trademark Office, case number IPR2023-01381, along with its partial Chinese translation, which does not meet the definition of common knowledge evidence in the Patent Examination Guidelines and therefore cannot be used as such. Counter-Evidence 3 is a national standard of the People's Republic of China, which can be used as common knowledge evidence. Counter-Evidence 2 is a textbook, which can also be used as common knowledge evidence.

3. Regarding Article 26.3 of the Chinese Patent Law

Article 26.3 of the Chinese Patent Law stipulates that the description shall clearly and completely describe the invention or utility model to enable a person skilled in the art to carry it out.

If a person skilled in the art can realize the technical solution claimed for protection in the present patent based on the description, it shall be deemed to have met the requirement of sufficient disclosure.

The petitioner argues that: The "compensated GaN layer" in claim 1 corresponds to the "compensated semiconductor layer 38" in the patent description. There are obvious contradictions or unclear descriptions in the description regarding the composition, implementation methods, and technical effects of the compensated GaN layer. Specifically:

(1) The conventional growth processes (such as MOCVD, MOVPE, etc.) of p-GaN (acceptor is Mg, Zn, C, etc.) can produce highly compensated semi-insulating p-GaN with deep hydrogen passivation, whether with or without additional hydrogen passivation. This implementation method of the present patent's compensated semiconductor 38 (compensated GaN layer) is prior art. Therefore, the technical solutions of claims 1-3 obviously cover prior art, and a person skilled in the art cannot clearly distinguish between the technology of the present patent and prior art.

(2) Based on the disclosed content of the description, it is unclear to a person skilled in the art what resistivity of GaN layer is intended to be achieved by setting "additional hydrogen passivation" and its purpose.

(3) The description does not clearly explain how the compensated GaN layer can achieve two technical effects that have opposite requirements for conductive electron density/resistivity simultaneously.

(4) According to the description, the first embodiment realizes both a MISFET and an enhancement mode device (HEMT) transistor. However, based on the technical knowledge of a person skilled in the art, the structure of the first embodiment is difficult to form as both a MISFET and an enhancement mode device (HEMT) transistor. Since the function of the device determines the function of each layer, a person skilled in the art cannot clearly understand the specific meaning of "*a buffer layer 33 separates the transition layers 32 from a barrier layer 34*" emphasized in the description.

The petitioner uses Attachments 1-3 to prove the definition of "compensated semiconductor", Attachment 4 to prove that H can be used as a donor H⁺ in p-type GaN, Attachments 5-8 to prove that different books and documents have different descriptions for the resistivity of semi-insulating materials, thus semi-insulating materials do not correspond to a fixed resistivity, and Attachments 9-11 to prove that p-type GaN (acceptor is Mg, Zn, C, etc.) obtained from conventional growth processes (such as MOCVD, MOVPE) is itself a compensated GaN layer.

In response, the panel believes that, first, it is necessary to clarify the meaning of "compensated GaN layer" in claim 1 of the present patent. The counter-evidence 2 provided by the patentee states (referring to GB/T14264-93 "Terminology of Semiconductor Materials"): Compensated semiconductors have both donor impurities and acceptor impurities present simultaneously.



The electrons released by the donor impurities are received by the acceptor impurities, and their effects offset each other.

Attachment 1 submitted by the petitioner discloses (referring to page 60 of "Physics and Devices of Semiconductors"): A compensated semiconductor refers to a semiconductor that contains both donor impurities and acceptor impurities. ... If $N_A = N_D$, it is called a fully compensated semiconductor, and the density of conduction electrons in a fully compensated semiconductor is the same as that in an intrinsic semiconductor. Attachment 2 submitted by the petitioner discloses (referring to page 9 of "Physics of Semiconductors and Thin Films"): The situation where the above-mentioned donor and acceptor impurities coexist in a semiconductor, causing their conductive effects to cancel each other out, is called the compensation effect of impurities. For a highly compensated semiconductor ($N_A \approx N_D$), because neither electrons nor holes contribute to conductivity, although the resistivity of such a material is measured to be very high, it does not represent a very pure material. The description of this patent describes that: *Compensated semiconductor layer 38 preferably comprises AlGaIn or GaN with a deep level passivated p-type impurity (refer to paragraph 0025). Advantageously, the high doping level of compensated layer 38 leads to enhancement mode devices. In addition, using a compensated semiconductor layer 38 leads to low gate leakage during device operation. Finally, the insulating nature of compensated layer 38 reduces the gate capacitance of the device (refer to paragraph 0026). The critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen. The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material. Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art.*

Based on the above descriptions in the description, as well as counter-evidence 2 submitted by the patentee and attachments 1-2 submitted by the petitioner, a person skilled in the art can understand that the meaning of the "compensated GaN layer" in claim 1 of this patent is: a GaN layer with the insulating nature in which one type of impurity (such as donor) offsets the electrical effect of another type of impurity (such as acceptor). On this basis, the response to the invalidity reason of insufficient disclosure claimed by the petitioner is as follows:

(1) First, whether the content of Claims 1-3 is prior art is unrelated to whether the disclosure of the description involved is sufficient. Second, the petitioner did not provide sufficient evidence to prove that the content of Claims 1-3 is prior art. The specific reasons are as follows: The passivation of p-type GaN layers does not necessarily occur in all cases (referring to columns 1-2 on page 61 of Attachment 9 and Attachment 10 submitted by the petitioner). Even if the manufacturing process contains hydrogen, the prior art always explicitly teaches to reverse this undesired passivation through annealing/activation or other means. It is commonly pursued by those skilled in the art to improve conductivity by activating or high-temperature annealing to prevent hydrogen passivation, as can be seen in Attachments 3, 4, 10, and 11 submitted by the petitioner. Especially in the final product, hydrogen passivation of p-type GaN is not inevitable, as it can be avoided by methods such as low-energy electron beam irradiation (LEEBI), molecular beam epitaxy (MBE), rapid thermal annealing (RTA), etc. Therefore, the attachments cited by the petitioner do not disclose "a compensated GaN layer above the barrier layer" in claim 1. Therefore, the petitioner's invalidity reason that "the technical solutions of claims 1-3 cover prior art, and those skilled in the art cannot clearly distinguish the technology of this patent from prior art" is unfounded.

(2) According to the description in paragraph 0028 of the patent description: *an additional hydrogen passivation can be performed by exposing the device to ammonia or hydrogen plasma at a high temperature.* Based on the above description, the present patent does not require that "additional hydrogen passivation" must be performed, but it can be performed optionally. According to the description in the patent description, those skilled in the art can fully understand that if the Mg acceptor is not sufficiently passivated during the preparation process (e.g., molecular beam epitaxy MBE method), additional hydrogen passivation can be implemented. Therefore, based on the statements in the description, those skilled in the art can understand that the purpose of setting "additional hydrogen passivation" is to make the compensated GaN layer more fully passivated.

(3) As recorded in paragraph 0026 of the description of this patent, *the high doping level of compensated layer 38 leads to enhancement mode devices.*



In addition, using a compensated semiconductor layer 38 leads to low gate leakage during device operation. Finally, the insulating nature of compensated layer 38 reduces the gate capacitance of the device. According to the description, the high doping level compensated semiconductor layer 38 not only forms enhancement mode devices but also achieves low gate leakage due to its insulating nature and high resistivity. Therefore, the invalidation reason put forward by the petitioner that "the patentee has not explained how the compensated GaN layer of the present patent can simultaneously achieve two technical effects with opposite requirements on conductivity electron density/resistivity" is unfounded.

(4) According to Figure 2 of the present patent, due to the insulating nature of the compensated semiconductor layer 38, which is located between the gate contact 37 and the AlGa_N barrier layer 34, combined with the description in paragraph 0026 of the present patent, the high doping level of the compensated layer 38 leads to enhancement mode devices. Furthermore, the use of the compensated semiconductor layer 38 results in low gate leakage during device operation, ultimately reducing the gate capacitance of the device. Therefore, the device in embodiment 1 of the present patent (referring to Figure 2) forms both a MISFET and an enhancement-type transistor. The statement "*a buffer layer 33 separates the transition layers 32 from a barrier layer 34*" clearly means that the buffer layer is located between the transition layers and the barrier layer, and its meaning is unambiguous.

In summary, the description of the present patent provides a clear and complete description of the composition, implementation methods, technical effects of the compensated GaN layer, and the purpose of additional hydrogen passivation. There are no contradictions or ambiguities. the skilled in the art can implement the technical solution of the invention, solve its technical problems, and achieve the expected technical effects according to the content described in the description. Therefore, the descriptions related to claims 1-3 are sufficiently disclosed and comply with the provisions of Article 26.3 of the Chinese Patent Law.

4. Regarding Article 26.4 of the Chinese Patent Law

Article 26.4 of the Chinese Patent Law stipulates that the claims shall clearly and concisely state the requested patent protection scope in accordance with the description.

If the technical solution of a claim can be generalized from the content disclosed in the description, then the claim can be supported by the description.

The petitioner argues that (1) the compensated GaN layer in claim 1 generalizes a relatively wide scope, while the description only provides a "preferred" embodiment, and the skilled in the art do not know if there are other compensated GaN layers that can achieve the same technical effects.

(2) Claim 2 does not specify the type of dopant atoms or the degree of hydrogen passivation; therefore it obviously includes technical solutions that cannot solve the technical problems of the invention. Therefore, claims 1-2 are not supported by the description and do not comply with the provisions of Article 26.4 of the Chinese Patent Law.

In response, the panel believes that: (1) Paragraph 0025 of the patent description states that *a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the gate contact 37. Compensated semiconductor layer 38 preferably comprises AlGa_N or Ga_N with a deep level passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca.* Paragraph 0026 of the description states that *the high doping level of compensated layer 38 leads to enhancement mode devices. In addition, using a compensated semiconductor layer 38 leads to low gate leakage during device operation. Finally, the insulating nature of compensated layer 38 reduces the gate capacitance of the device.* Paragraph 0029 of the description states that *first, in Ga_N transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in Ga_N transistor 100 of the prior art, layer 105 is a conductive p-type material.* Based on the above statements, the description of the present patent has provided detailed exemplary explanations for the structure and function of the "compensated GaN layer." On this basis, the skilled in the art, based on their knowledge and abilities, can reasonably predict that besides the specific embodiments described in the description of the present patent, there are also "compensated GaN layers" with other material parameters. Therefore, the skilled in the art can generalize the "compensated GaN layer" in claim 1 based on the statements in the description. Therefore, claim 1 can be supported by the description and complies with the provisions of Article 26.4 of the Chinese Patent Law.

(2) According to paragraph 0025 of the description, *compensated semiconductor layer 38 preferably comprises AlGa_N or Ga_N with a deep level passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca.* "Mg, Zn, Be, Cd or Ca" are all acceptor type dopant atoms.



On this basis, the patent description has made detailed exemplary descriptions of "acceptor type dopant atoms". Based on their knowledge level and ability, those skilled in the art can reasonably predict that there are other acceptor type dopant atoms in addition to the specific embodiments described in the patent description. Therefore, those skilled in the art can generalize the "acceptor type dopant atoms" in claim 2 based on the statements in the description.

According to paragraph 0029 of the description: *The critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen. The passivation leads to two differences. First, in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material. Second, the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art.* According to the above statements, the patent description has made detailed exemplary descriptions of "hydrogen passivation". On this basis, those skilled in the art can generalize the "hydrogen passivation" in claim 2 based on the statements in the description.

In summary, the invalid reason provided by the petitioner that claims 1-2 are not supported by the description is unfounded, and claims 1-2 can be supported by the description, which complies with the provisions of Article 26(4) of the Chinese Patent Law.

5. Regarding Rule 20.1 of the Implementing Regulations of the Chinese Patent Law

Rule 20.1 of the Implementing Regulations of the Chinese Patent Law stipulates that the claims shall specify the technical features of the invention or utility model, and clearly and concisely express the scope of protection.

If the technical solution of the claim can be clearly defined for those skilled in the art, the scope of protection of the claim is clear.

The petitioner believes that the scope of protection for the "compensated GaN layer" in claim 1 is unclear, and therefore claim 1 does not comply with the provisions of Rule 20.1 of the Implementing Regulations of the Chinese Patent Law.

In this regard, the collegial panel believes that: referring to the comments on Article 26.3 of the Chinese Patent Law in Section 3 above, the meaning of "compensated GaN layer" in claim 1 is a GaN layer with the insulating nature in which one type of impurity (such as donor) offsets the electrical effect of another type of impurity (such as acceptor). Therefore, the scope of protection of the "compensated GaN layer" in claim 1 is clear, and claim 1 complies with the provisions of Rule 20.1 of the Implementing Regulations of the Chinese Patent Law.

6. Regarding Article 22.2 of the Chinese Patent Law

Article 22.2 of the Chinese Patent Law stipulates that Novelty means that the invention or utility model is not an existing technology, and prior to the date of application, no entity or individual has filed an application heretofore with the patent administrative department of the State Council for the identical invention or utility model and recorded it in the patent application documents or patent documents released after the said date of application.

If the technical solution of the claim has distinctive features from the technical solution of the reference document, resulting in the technical solutions of the two being substantively different, then the claim is novel relative to the reference document.

6.1. Claim 1

6.1.1. Relative to D1



Claim 1 seeks protection for a column III Nitride transistor. As mentioned earlier, the meaning of "compensated GaN layer" in claim 1 of this patent is a GaN layer with the insulating nature in which one type of impurity (such as donor) offsets the electrical effect of another type of impurity (such as acceptor).

D1 discloses a column III nitride high electron mobility transistor and a method for manufacturing a column III nitride high electron mobility transistor, and discloses: *Turning to FIGS. 1A and 1B, a substrate 10 is provided on which nitride based devices may be formed. Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate 10. For example, an AlN buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. A channel layer 20 is provided on the substrate 10, and the channel layer 20 is a column III nitride. A barrier layer 22 is provided on the channel layer 20. The barrier layer 22 can be a column III nitride. FIGS. 2A and 2B illustrate high electron mobility transistors having a cap layer 34, 34' according to further embodiments of the present invention. The substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30 and gate contact 32 may be provided as discussed above with reference to FIGS. 1A and 1B (see the last paragraph on page 12 to paragraph 3 on page 14 of the description). As seen in FIGS. 2A and 2B, the cap layer 34, 34' includes a doped region 40 at or near the outer surface of the cap layer 34, 34'. The cap layer 34, 34' may be a GaN based cap layer, such as a GaN layer and/or an AlGaN layer. In some embodiments of the present invention, the doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C. In other embodiments of the present invention, the doped region 40 is doped with an n-type dopant, such as Si, Ge and/or O. In further embodiments of the present invention, the doped region 40 is doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co. The dopant may be incorporated into the cap layer 34 during deposition or growth of the cap layer 34, 34' or may be subsequently implanted, for example, using ion implantation (see paragraph 2 on page 18 of the description of D1). In further embodiments of the present invention, the outer surface of the cap layer of a nitride-based HEMT is doped with p-type, n-type or deep-level dopants such that the cap layer has a higher concentration of dopants at a surface of the cap layer that is remote from the barrier layer than at other regions of the cap layer. The cap layer may be a GaN based cap layer. The dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations. The dopant may have different characteristics when at a dislocation than when in the bulk crystal (see the last paragraph on page 11 of the description of D1). N-type dopants may be used to screen the channel region from surface states and pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects (see paragraph 2 on page 19 of the description of D1). P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents (see paragraph 1 on page 20 of the description of D1).*

The petitioner believes that the cap layer 34 in D1 is equivalent to the compensated GaN layer in claim 1. D1 discloses all the technical features of claim 1, and both belong to the same technical field, solving the same technical problem and achieving the same technical effect. Therefore, the technical solution claimed in claim 1 does not possess novelty as defined in Article 22.2 of the Chinese Patent Law relative to D1.

In this regard, the collegial panel believes that D1 discloses that *an anneal of the structure including the passivation layer may be carried out in an oxygen environment to remove hydrogen from the layer and alter surface states and/or add oxygen to the surface (see paragraph 3 on page 17 of the description); the annealing may be performed at a temperature and for a time insufficient to oxidize a structure underlying the passivation layer but sufficient to remove at least some hydrogen from the passivation layer or exchange some hydrogen with deuterium (see paragraph 2 on page 6 of the description).* According to the statements of D1, it does not disclose passivation of the doped region 40, and the cap layer 34, which is part of the doped region 40, is not passivated. D1 discloses a depletion mode transistor, and the doped region 40 cannot deplete two-dimensional electron gas. The role of the doped region 40 and the cap layer 34 is to screen the channel region from surface states and pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects.



Claim 1 seeks protection for an enhancement mode transistor, in which the compensated GaN layer plays a role in depleting the two-dimensional electron gas in the corresponding region of the gate, while the p-type dopant is further passivated by donors to reduce gate leakage and capacitance. D1 does not disclose that the cap layer 34 is a compensated semiconductor layer, and the role of the cap layer 34 is also completely different from the compensated GaN layer in claim 1. Therefore, the cap layer 34 in D1 cannot be equivalent to the compensated GaN layer in claim 1.

Therefore, claim 1 has at least one distinctive technical feature from D1: a compensated GaN layer above the barrier layer.

Since claim 1 has at least the above distinctive feature relative to D1, the technical solution of claim 1 is not substantively the same as that of D1. Claim 1 possesses novelty as defined in Article 22.2 of the Chinese Patent Law relative to D1.

6.1.2. Relative to D2

D2 discloses nitride semiconductor transistors and their fabrication methods, and discloses: *Referring to FIG. 1, a substrate 11 is made of silicon and its principal plane is the (111) plane. A buffer layer 12 of AlN having a thickness of 100 nm is formed on the principal plane of the substrate 11. A first nitride semiconductor layer 13 of undoped GaN having a thickness of 2 [μm] and a second nitride semiconductor layer 14 of undoped Al_{0.15}Ga_{0.85}N having a thickness of 25 nm are formed on the buffer layer 12. On the second nitride semiconductor layer 14, a third nitride semiconductor layer 15 is formed which is made of Al_{0.15}Ga_{0.85}N doped with magnesium (Mg) and has a thickness of 200 nm. The third nitride semiconductor layer doped with Mg is composed of: a control region 15a in which Mg is activated to exhibit a p-type conductivity; and a high resistive region 15b in which Mg is not activated to offer a higher resistance than the control region 15a. The control region 15a is formed in the shape of, for example, stripes each having a width of 1 [μm]. On the hydrogen diffusion barrier film 16, a gate electrode 20 is formed to cover the opening. The gate electrode 20 is made of palladium (Pd), and comes into ohmic contact with the control region 15a* (see paragraphs 0031-0034 of the translation and Figure 1).

The petitioner believes that the control region 15a in D2 is equivalent to the compensated GaN layer in claim 1. D2 discloses all the technical features of claim 1, and both belong to the same technical field, solving the same technical problem and achieving the same technical effect. Therefore, the technical solution claimed in claim 1 does not possess novelty as defined in Article 22.2 of the Chinese Patent Law relative to D2.

In this regard, the collegial panel believes that D2 has disclosed that *the third nitride semiconductor layer doped with Mg is composed of: a control region 15a in which Mg is activated to exhibit a p-type conductivity*. Therefore, the control region 15a is conductive and cannot be equivalent to the "compensated GaN layer" in claim 1. Therefore, claim 1 has at least one distinctive technical feature relative to D2: a compensated GaN layer above the barrier layer.

Since claim 1 has at least the above distinctive features relative to D2, the technical solution of claim 1 is not substantively the same as that of D2. Claim 1 possesses novelty as defined in Article 22.2 of the Chinese Patent Law relative to D2.

6.1.3. Relative to D3

D3 discloses a modulated doped field effect transistor (see the last two paragraphs on page 12 to paragraph 2 on page 13 of the description, Figure 5): the transistor comprises a gallium nitride substrate 300, a gallium nitride-based semiconductor layer 302, a gallium nitride-based gate insulating layer 318, a source electrode 312, a drain electrode 314, and a gate electrode 316. The gallium nitride-based semiconductor layer 302 comprises a buffer layer 304, a channel layer 306, an interlayer 308, and a barrier layer 310. The gallium nitride-based insulating layer 318 can be doped, and the dopant can be magnesium.

The petitioner believes that the gallium nitride-based gate insulating layer 318 in D3 is equivalent to the compensated GaN layer in claim 1. D3 discloses all the technical features of claim 1, and both belong to the same technical field, solving the same technical problem, and achieving the same technical effect.



Therefore, the technical solution claimed in claim 1 does not possess novelty as defined in Article 22.2 of the Chinese Patent Law relative to D3.

In this regard, the collegial panel believes that the barrier layer 310 in D3 is Si-doped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$, and its conductivity type is N-type. Therefore, D3 is a depletion mode transistor. The role of the gallium nitride-based gate insulating layer 318 in D3 is to improve the lattice matching between the gate insulating layer and the gallium nitride-based semiconductor layer, and the role of Mg doping in the gallium nitride-based gate insulating layer is to increase the resistance of the gate insulating layer 318. However, the role of the compensated GaN layer in claim 1 is: depleting the two-dimensional electron gas in the corresponding region of the gate, while the p-type dopant is further passivated by donors to reduce gate leakage and capacitance. D3 does not record that the gallium nitride-based gate insulating layer 318 is a compensated GaN layer, and it is impossible to determine that the gallium nitride-based gate insulating layer 318 is equivalent to the compensated GaN layer in claim 1 only by Mg doped in the "gallium oxide-based gate insulating layer".

Therefore, claim 1 has at least one different technical feature relative to D3: a compensated GaN layer above the barrier layer.

Since claim 1 has at least the above distinctive features relative to D3, the technical solution of claim 1 is not substantively the same as that of D3. Claim 1 possesses novelty as defined in Article 22.2 of the Chinese Patent Law relative to D3.

6.2. Dependent claims 2-3

Claims 2-3 are dependent claims of claim 1. When the claim 1 referred to in claim 2-3 is novel in relation to D1 or D2 or D3, claims 2-3 also possess novelty as defined in Article 22.2 of the Chinese Patent Law.

7. Article 22.3 of the Chinese Patent Law

Article 22.3 of the Chinese Patent Law stipulates that inventiveness means that, as compared with the technology existing before the date of application the invention has prominent substantive features and represents a notable progress and that the utility model has substantive features and represents progress.

The claim has distinctive features relative to the closest prior art. If the distinctive features are not disclosed by other prior art and there is no evidence that they are common knowledge in the art, and the distinctive features provide beneficial technical effects to the technical solution of the claim, then the claim possesses inventiveness.

7.1 Claim 1

Claim 1 seeks protection for a column III Nitride transistor. As mentioned in Section 6 above, claim 1 has at least one distinctive technical feature relative to D1: a compensated GaN layer above the barrier layer.

Based on the distinctive feature above, it is determined that the technical problem to be actually solved in claim 1 is to form enhancement mode devices by the high doping level of the compensated GaN layer, while utilizing the insulating nature of the GaN layer to reduce the gate leakage and gate capacitance of the device.

As described in Section 6.1 above, neither D2 nor D3 discloses the above distinctive feature, nor is there any evidence that the above distinctive feature is common knowledge in the art. Moreover, the distinctive feature also has the following beneficial technical effects: using the high doping level of the compensated GaN layer to form enhancement mode devices, and using the insulating nature of the compensated GaN layer to reduce gate leakage and device gate capacitance.

Similarly, as mentioned in Section 6.1 above, claim 1 differs from D2 at least in the technical feature of a compensated GaN layer above the barrier layer. However, neither D1 nor D3 discloses the above distinctive feature, and there is no evidence that the above distinctive feature is common knowledge in the art. Moreover, the above distinctive feature also has the above beneficial technical effect.



Similarly, as mentioned in Section 6.1 above, claim 1 differs from D3 at least in the distinctive technical feature of a compensated GaN layer above the barrier layer. Neither D1 nor 2 discloses this distinctive feature, and there is no evidence that this distinctive feature is common knowledge in the art. Furthermore, this distinctive feature possesses the aforementioned beneficial technical effects.

Therefore, claim 1 possesses the inventiveness stipulated in Article 22.3 of the Chinese Patent Law relative to the combination of evidence presented by the petitioner.

7.2 Claims 2-3

Both claims 2 and 3 refer to claim 1. Based on the fact that claim 1 possesses inventiveness relative to the combination of evidence presented by the petitioner, claims 2 and 3 also possess the inventiveness stipulated in Article 22.3 of the Chinese Patent Law relative to the same combination of evidence.

In summary, all the invalidation arguments put forward by the petitioner are unfounded. Therefore, the collegial panel makes the following decision.

III. Decision

Maintain the validity of the invention patent No. 201080015425.X.

If any party is dissatisfied with this decision, they may file a lawsuit at the Beijing Intellectual Property Court within three months from the date of receiving this decision in accordance with Article 46.2 of the Chinese Patent Law. According to this provision, if one party files a lawsuit, the other party shall participate in the lawsuit as a third party.

Panel Chair: Lifang Liu
Primary Examiner: Jie Xiong
Participating Examiner: Xiaodong Fan

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