

Exhibit 28

INFRINGEMENT OF CLAIMS 1-3 OF U.S. PATENT NO. 8,350,294 (“’294 patent”) COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME BY INN650DA140A (“’294 Accused Products”)

CHART FOR ’294 ACCUSED PRODUCTS—HIGHER VOLTAGE GAN TRANSISTORS	
U.S. Patent No. 8,350,294 Claim Language	’294 Accused Products
Claim 1	
[1a] A column III Nitride transistor comprising:	To the extent the preamble is considered a limitation, INN650DA140A (“INN650”), representative of Innoscience’s higher voltage GaN transistors, is [1a] a column III Nitride (gallium nitride) transistor. <i>See, e.g.</i>, Exhibit 55 at 1 (annotated and reproduced below); <i>see also</i> the ’294 patent at 3:13-15 (“A III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ where $x+y \leq 1$.”). INN650DA140A 650V GaN Enhancement-mode Power Transistor  INN650DA140A 1. General description 650V GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 5 mm × 6 mm size

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[1b] a substrate,

INN650 includes **[1b] a substrate**. A portion of a Si substrate can be seen in a TEM (transmission electron microscopy) image of an INN650 sample.



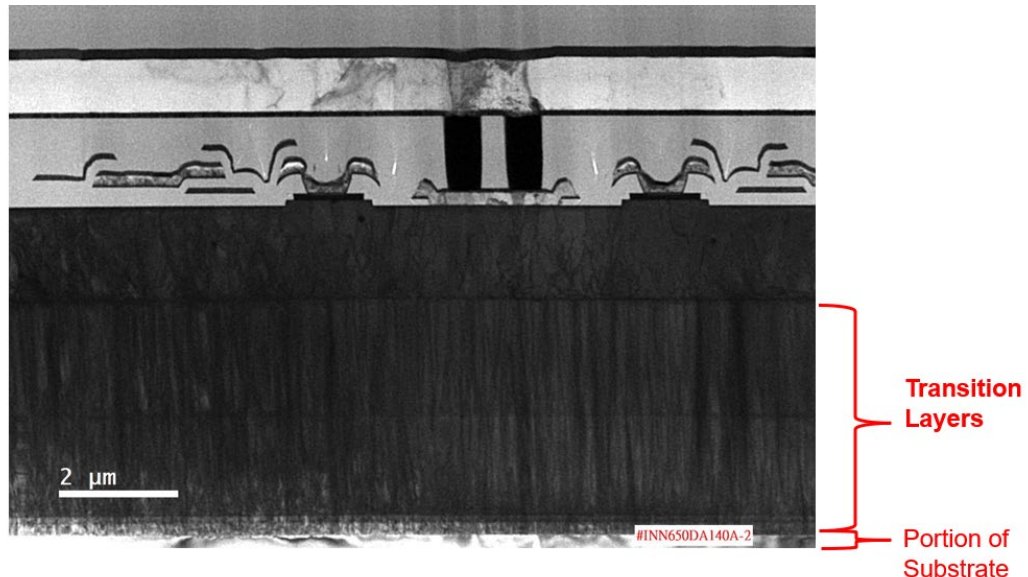
**Portion of
Substrate**

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[1c] a set of III-N transition layers above the substrate,

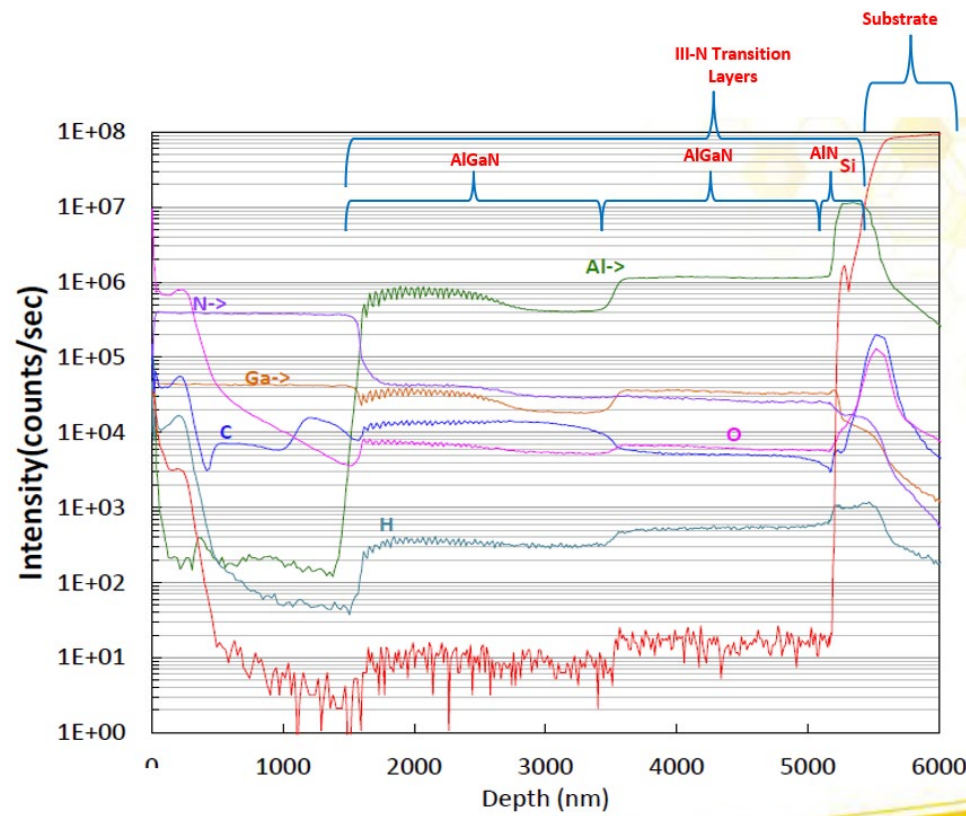
INN650 includes [1c] a set of III-N transition layers above the substrate.

A set of III-N transition layers above the substrate can be seen in a TEM image of the INN650 sample.



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Secondary Ion Mass Spectrometry (SIMS) data confirms the transition layers are formed of a III-N material (e.g., AlN and AlGaN).¹ See, e.g., the ’294 patent at 3:13-15 (“A III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ where $x+y \leq 1$.”).



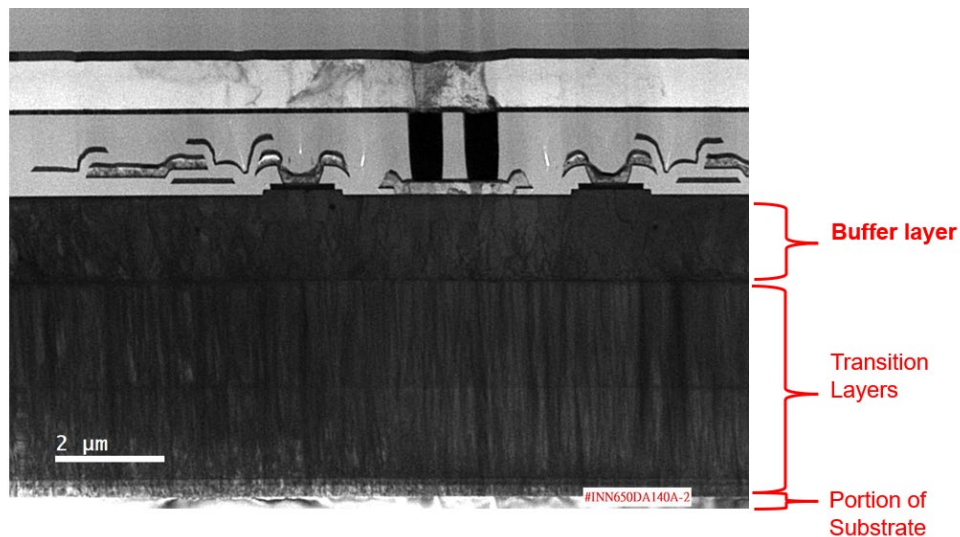
¹ Depth is measured from a topmost surface of the gate stack’s GaN layer. The annotated brackets are approximations of where one layer starts, and another begins.

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[1d] a III-N buffer layer above the set of transition layers,

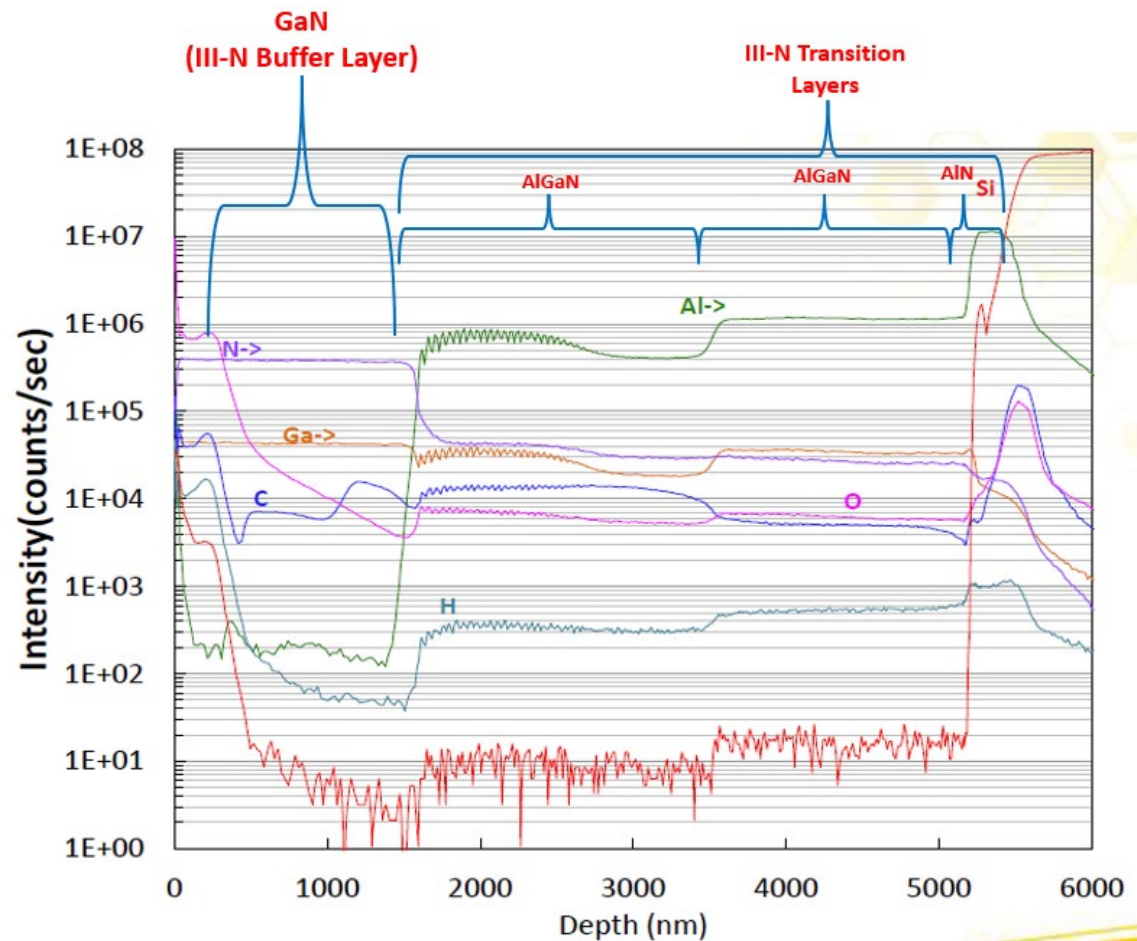
INN650 includes [1d] a III-N buffer layer above the transition layers.

A III-N buffer layer above the transition layers can be seen in a TEM image of the INN650 sample.



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SIMS data confirms the buffer layer is formed of a III-N material (e.g., GaN).² See, e.g., the ’294 patent at 3:13-15 (“A III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ where $x+y \leq 1$.”).



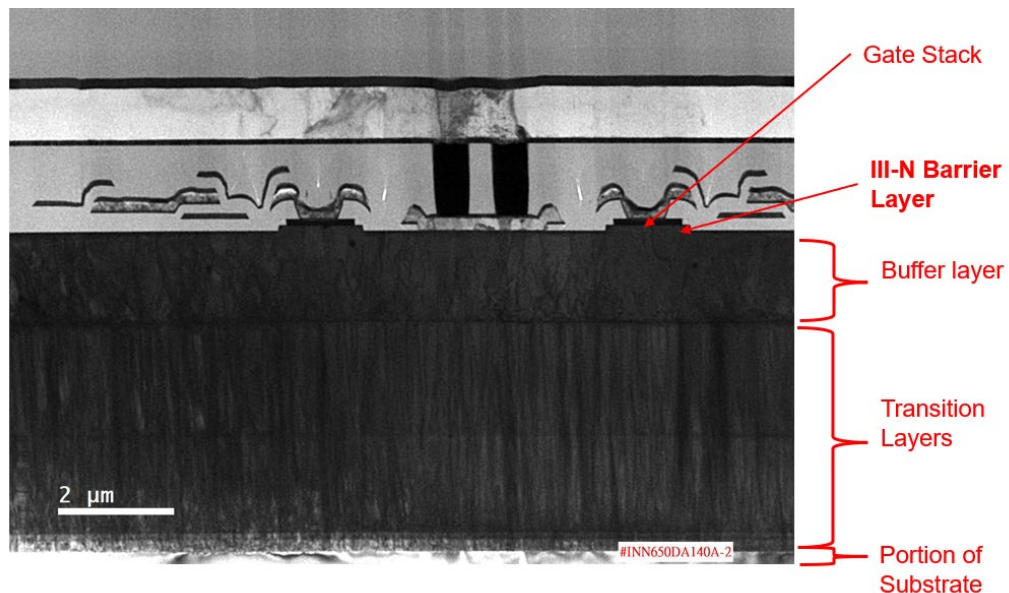
² Depth is measured from a topmost surface of the gate stack’s GaN layer. The annotated brackets are approximations of where one layer starts, and another begins.

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[1e] a III-N barrier layer above the buffer layer,

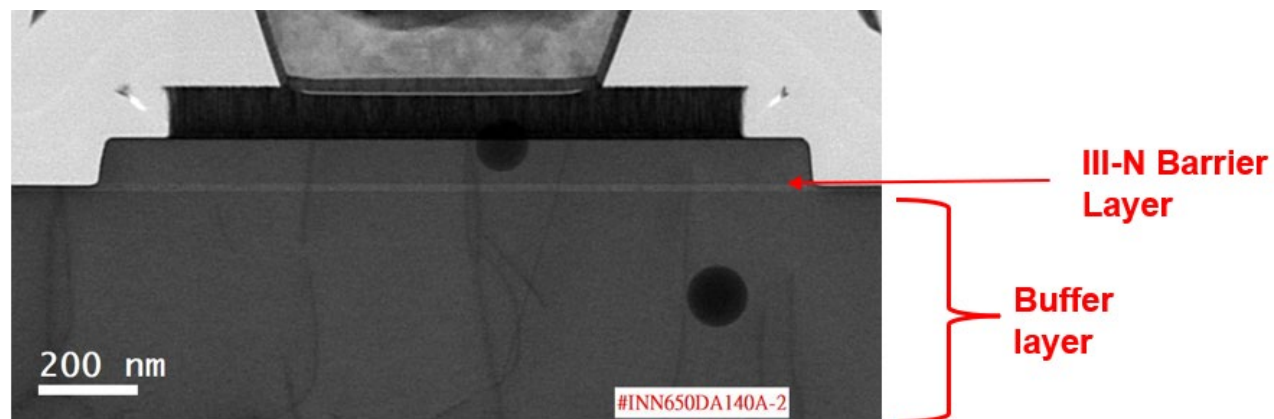
INN650 includes [1e] a III-N barrier layer above the buffer layer.

A III-N barrier layer above the buffer layer can be seen in the TEM images of the INN650 sample.



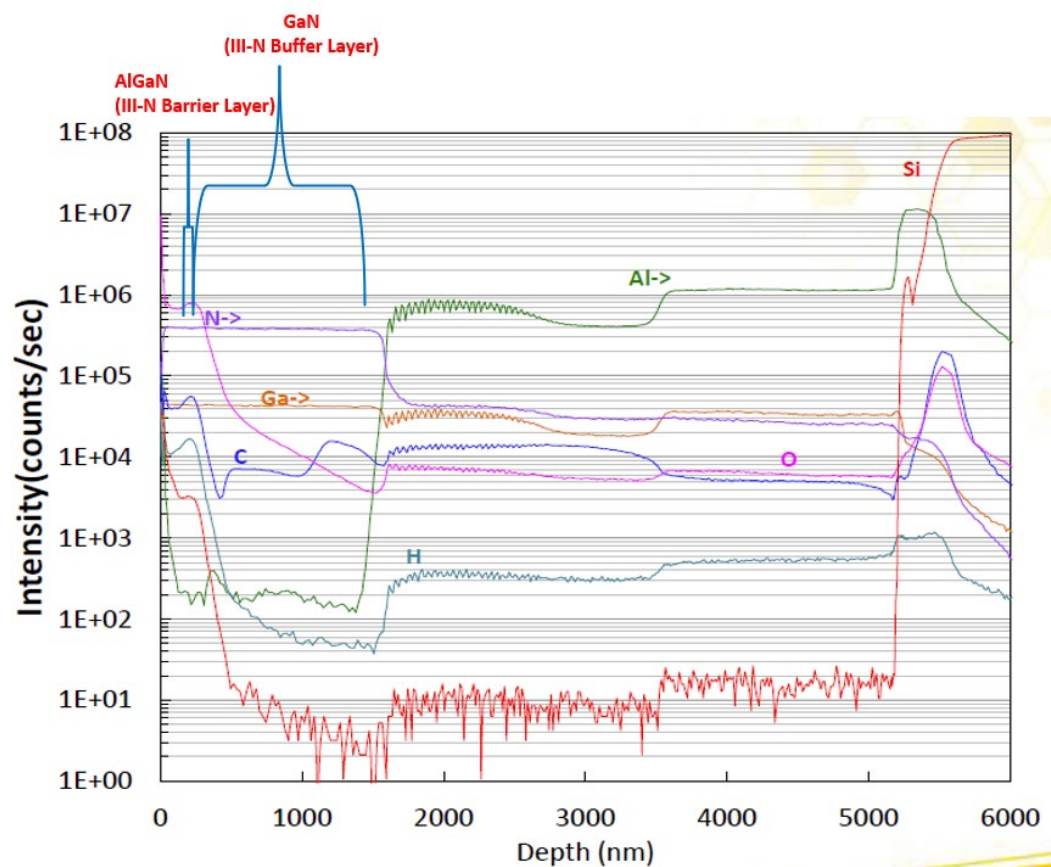
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A magnified image shows the barrier layer more clearly.



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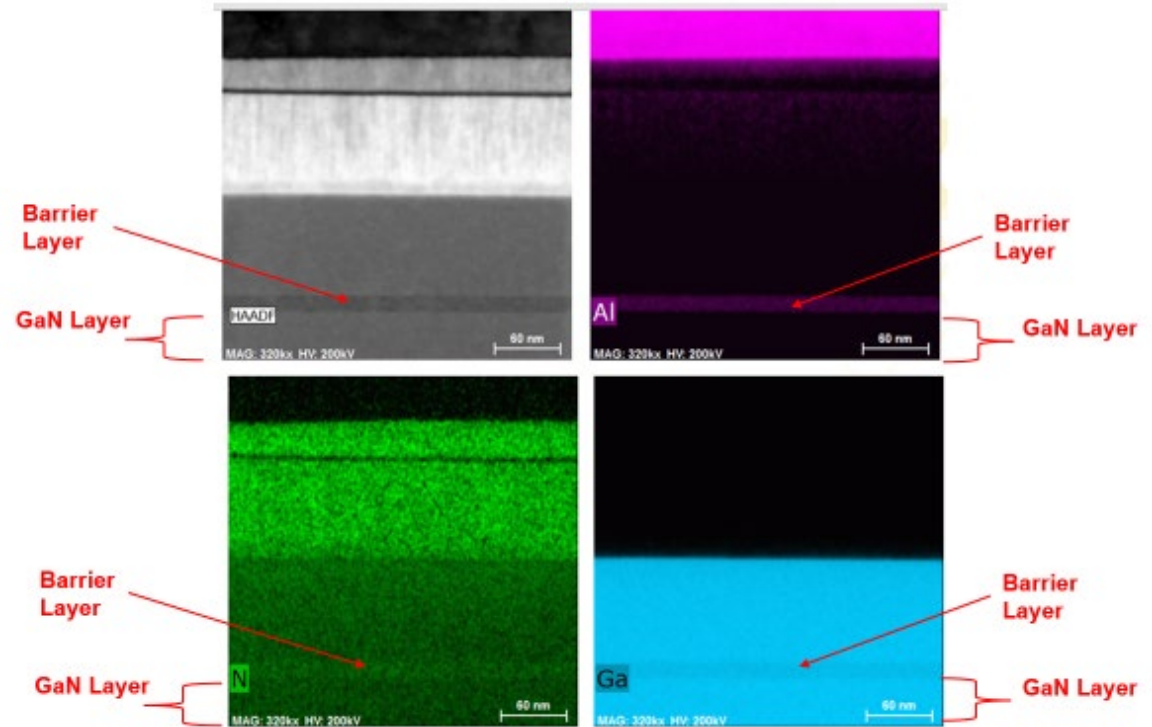
SIMS data confirms the barrier layer is formed of a III-N material ((e.g., AlGaN).³ See, e.g., the ’294 patent at 3:13-15 (“A III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$ where $x+y \leq 1$.”).



³ Depth is measured from a topmost surface of the gate stack’s GaN layer. The annotated brackets are approximations of where one layer starts, and another begins.

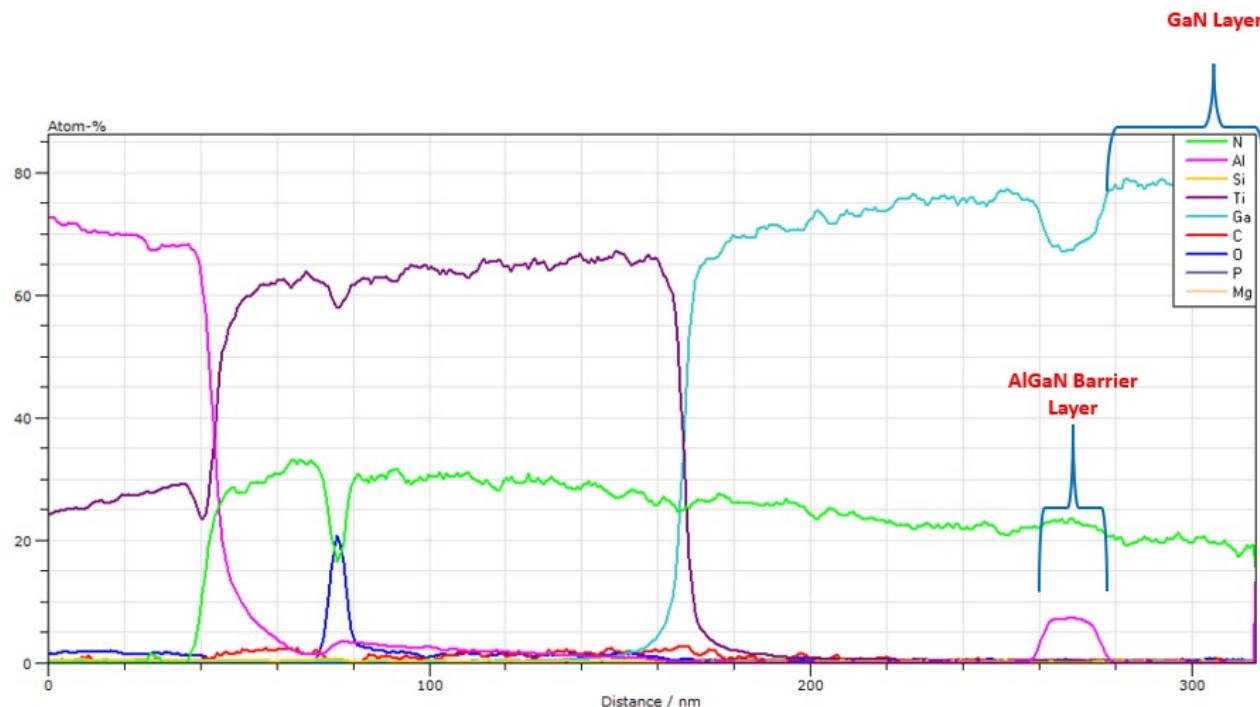
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Energy-dispersive X-ray spectroscopy (EDS) further confirms [1e] a III-N barrier layer above the buffer layer as evidenced by the detection of aluminum (pink color in top right image) above a layer (the GaN layer) in which aluminum is below the level of detection (dark layer underneath).



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The plot below shows the detection of Ga, Al, and N at depths consistent with the expected location of the AlGa_N barrier layer and the detection of Ga and N at depths consistent with the expected location of the GaN layer.⁴



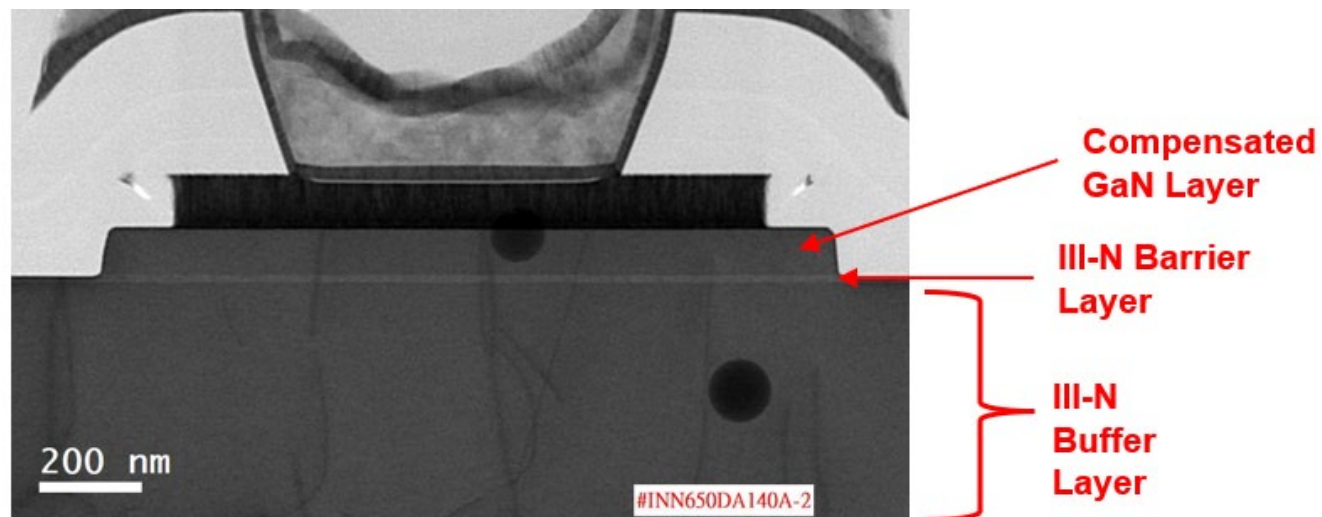
⁴ The 0 nm reference for EDS is above the top surface of the gate stack's gate.

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[1f] a compensated GaN layer above the barrier layer, and

INN650 includes [f] compensated GaN layer above the barrier layer.

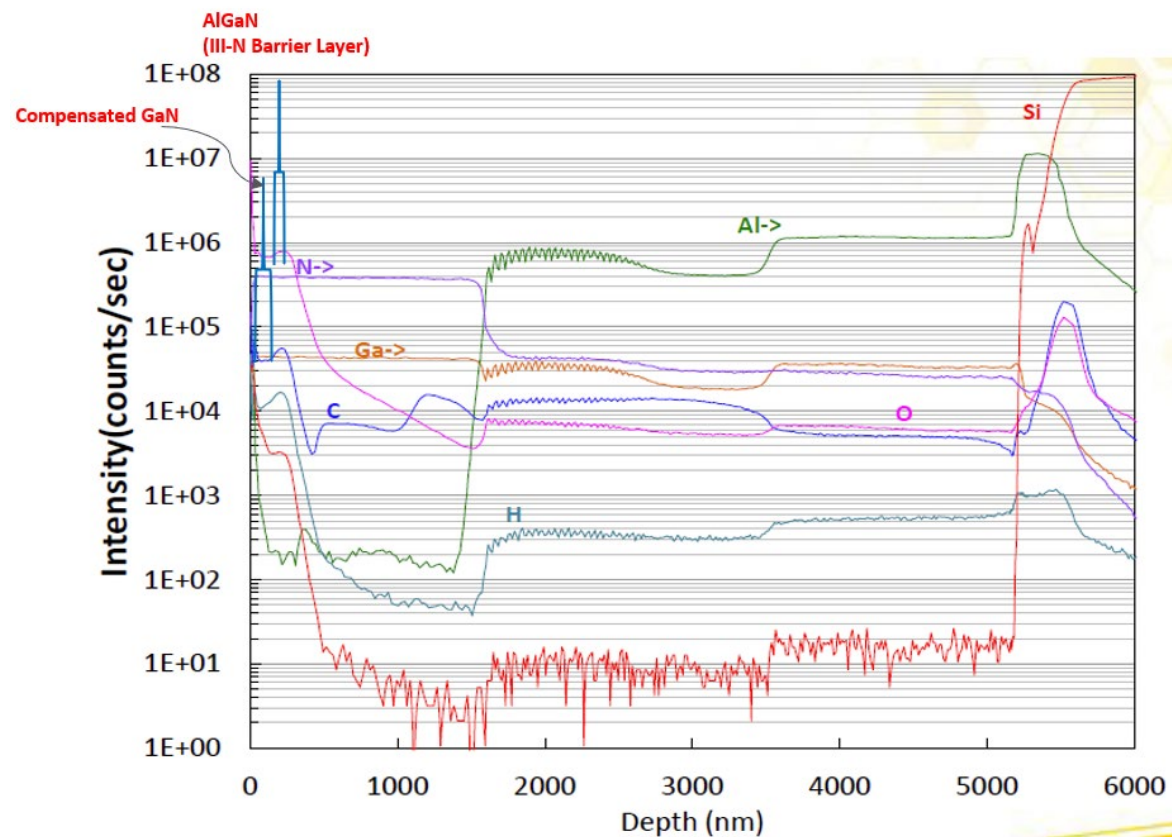
A GaN layer can be seen in a TEM image of the INN650 sample.⁵ The GaN layer is compensated as discussed further below.



⁵ Depth is measured from a topmost surface of the gate stack's GaN layer. The annotated brackets are approximations of where one layer starts, and another begins.

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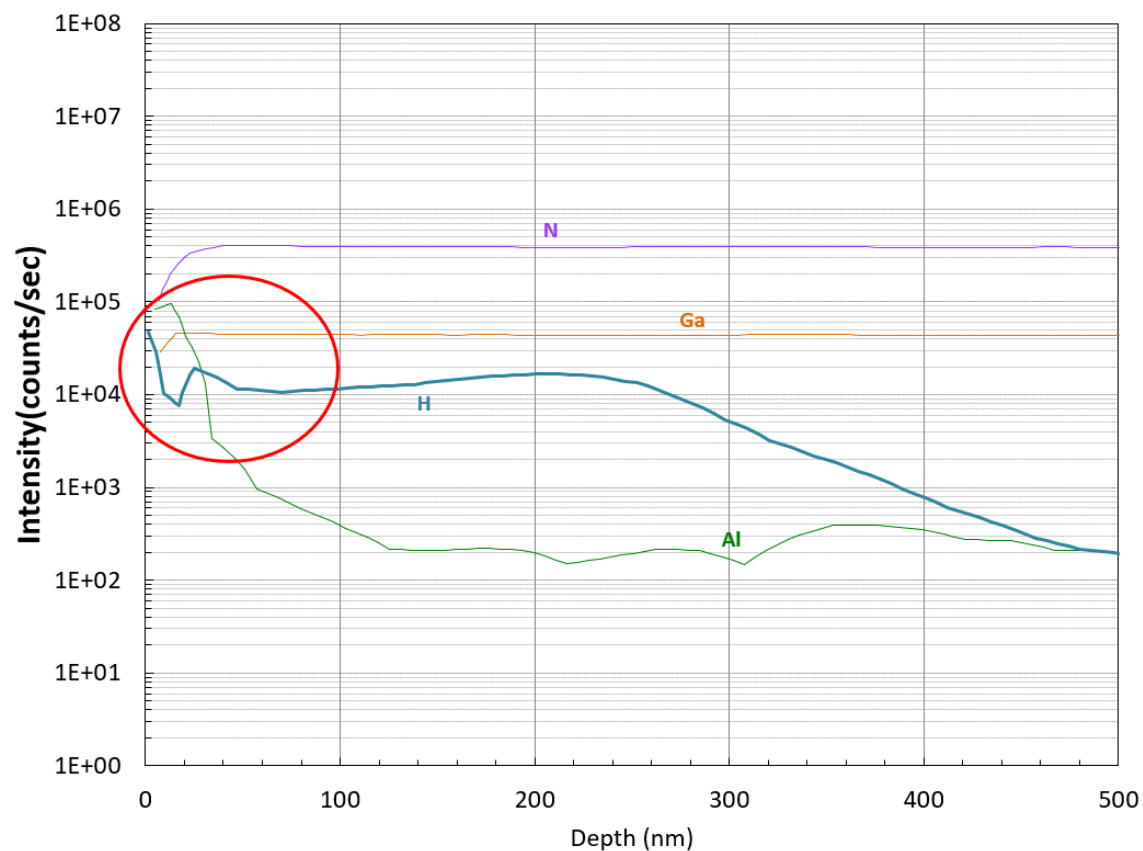
The SIMS data confirms the GaN layer is formed with gallium (Ga) and nitrogen (N).



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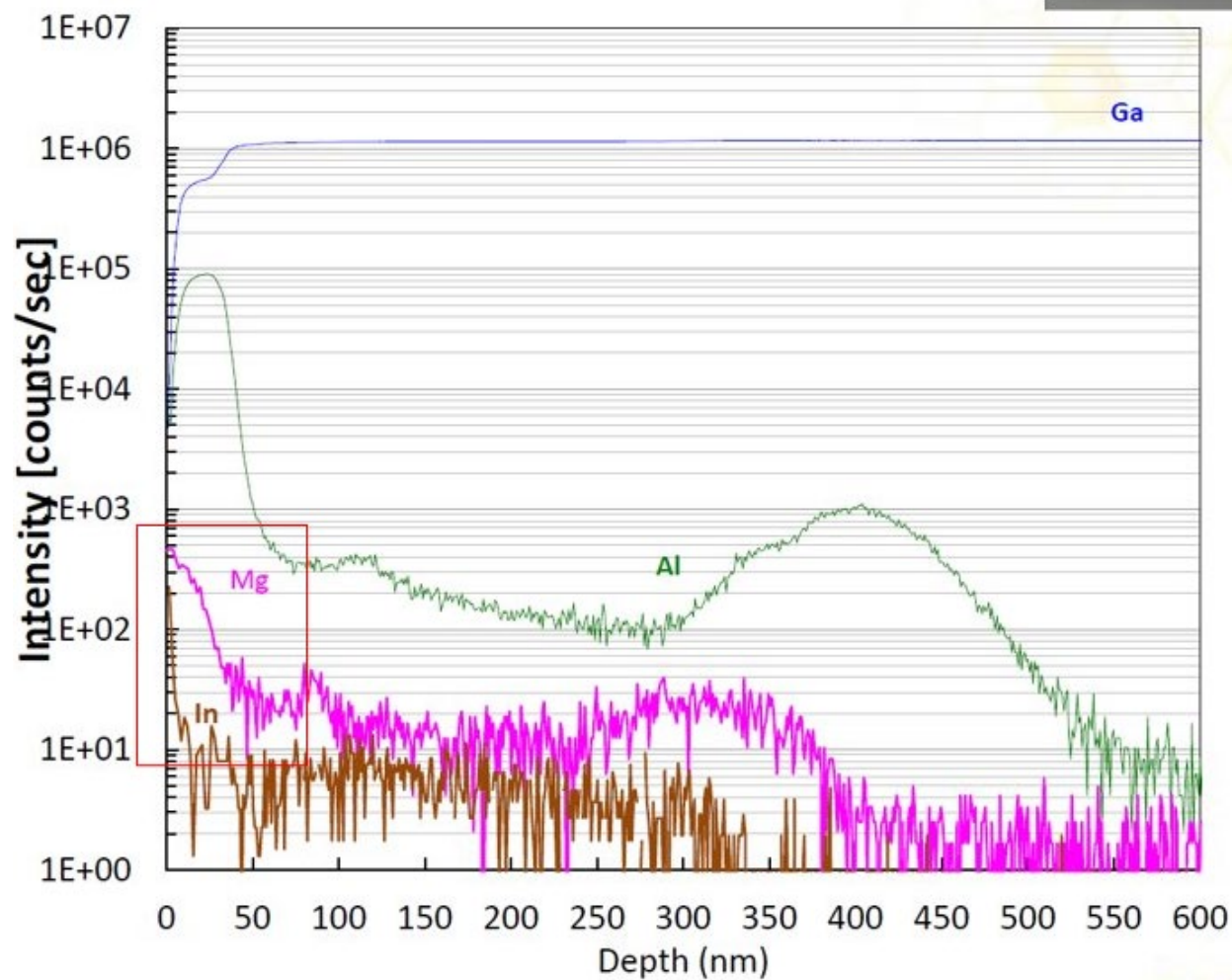
In addition, SIMS data shows that the GaN layer is **compensated**; that is, the GaN layer has elevated levels of hydrogen (H) and magnesium (Mg) as compared to the layers below the GaN layer (annotated above).

Hydrogen:



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Magnesium:



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This is further confirmed by an Innoscience authored paper that characterizes its GaN layer above the barrier layer as a “Mg doped p-type GaN (p-GaN) layer.” *See* Exhibit 49 at 172 (reproduced and highlighted below); *see also* Fig. 1 (reproduced below).

In the development phase, transistor processing is done in imec’s 200 mm CMOS pilot line using a Au-free process flow. The growth of III-N layers is carried out by metalorganic chemical vapor deposition (MOCVD) on 200 mm Si (111) wafers. The Mg doped p-type GaN (p-GaN) layer is grown in sequence with a AlN nucleation layer, the (Al)GaN buffer, GaN channel and AlGaN barrier layers. The TiN gate metal layer is deposited directly on the p-GaN surface. First, the TiN layer is etched, followed by a selective p-GaN to AlGaN dry etch step using a BCl_3/SF_6 chemistry. The access area is passivated by a dielectric stack containing Al_2O_3 and SiO_2 layers. Ohmic contact formation of the source and drain contacts is done in sequence with the gate processing using a metal stack consisting of Ti, Al and TiN. The process flow is completed by back-end metallization modules including field plates, where SiO_2 is used for the inter-metal dielectric layers. The 650 V power devices have a gate-drain distance of 16 μm and a gate width of 36 mm. Also various field plates are processed to reduce device dispersion.

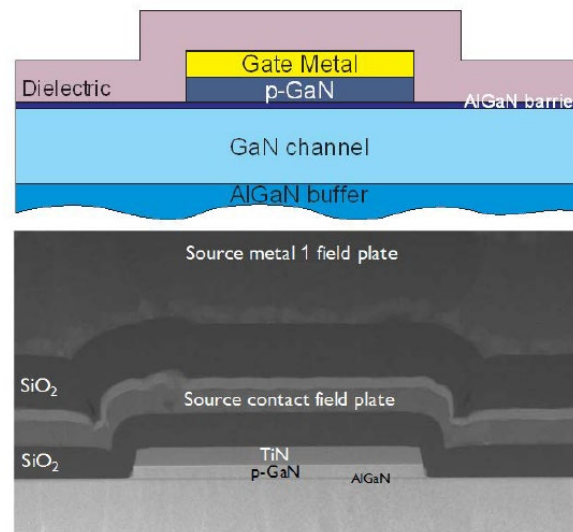


Fig. 1. Schematic illustration (top) and cross-section TEM micrograph (bottom) of the gate area of the p-GaN gate transistors.

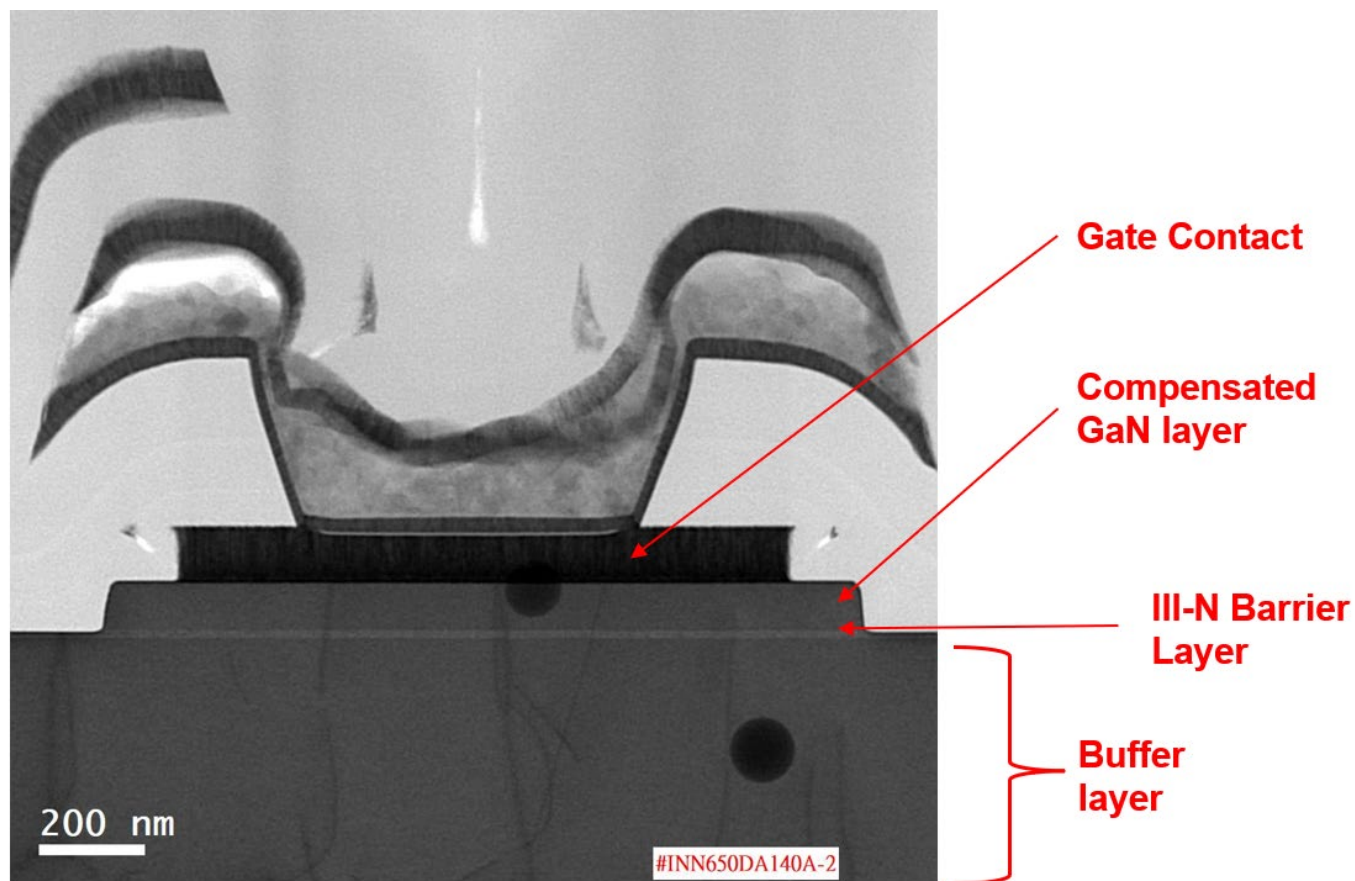
The Mg doped p-type GaN layer with the presence of hydrogen, as evidenced by Innoscience’s admissions and the above SIMS data, demonstrates that the gate material GaN layer is doped with Mg (p-GaN) and passivated by hydrogen evidencing a compensated GaN layer.

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[1g] a gate contact above the compensated GaN layer.

INN650 includes [g] a gate contact above the compensated GaN layer.

A gate contact above the compensated GaN layer can be seen in a TEM image of the INN650 sample.



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This is further confirmed by the Innoscience authored paper that states a gate metal layer is deposited directly on the p-GaN (i.e., compensated GaN layer) surface. *See* Ex 49 at 172 (reproduced and highlighted below); *see also id.*, Fig. 1 (reproduced below).

In the development phase, transistor processing is done in imec’s 200 mm CMOS pilot line using a Au-free process flow. The growth of III-N layers is carried out by metalorganic chemical vapor deposition (MOCVD) on 200 mm Si (111) wafers. The Mg doped p-type GaN (p-GaN) layer is grown in sequence with a AlN nucleation layer, the (Al)GaN buffer, GaN channel and AlGaN barrier layers. The TiN gate metal layer is deposited directly on the p-GaN surface. First, the TiN layer is etched, followed by a selective p-GaN to AlGaN dry etch step using a BCl_3/SF_6 chemistry. The access area is passivated by a dielectric stack containing Al_2O_3 and SiO_2 layers. Ohmic contact formation of the source and drain contacts is done in sequence with the gate processing using a metal stack consisting of Ti, Al and TiN. The process flow is completed by back-end metallization modules including field plates, where SiO_2 is used for the inter-metal dielectric layers. The 650 V power devices have a gate-drain distance of 16 μm and a gate width of 36 μm . Also various field plates are processed to reduce device dispersion.

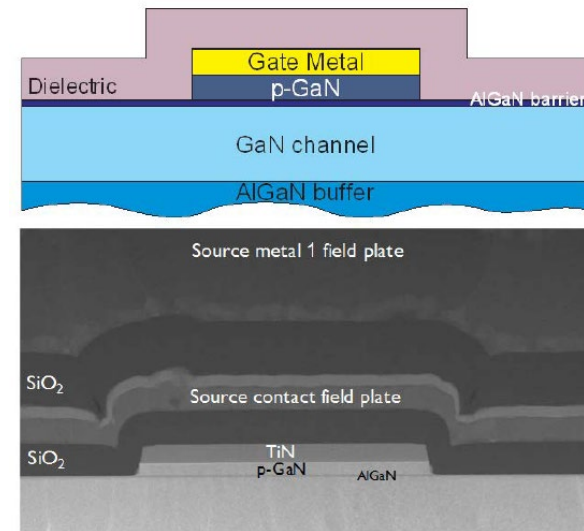
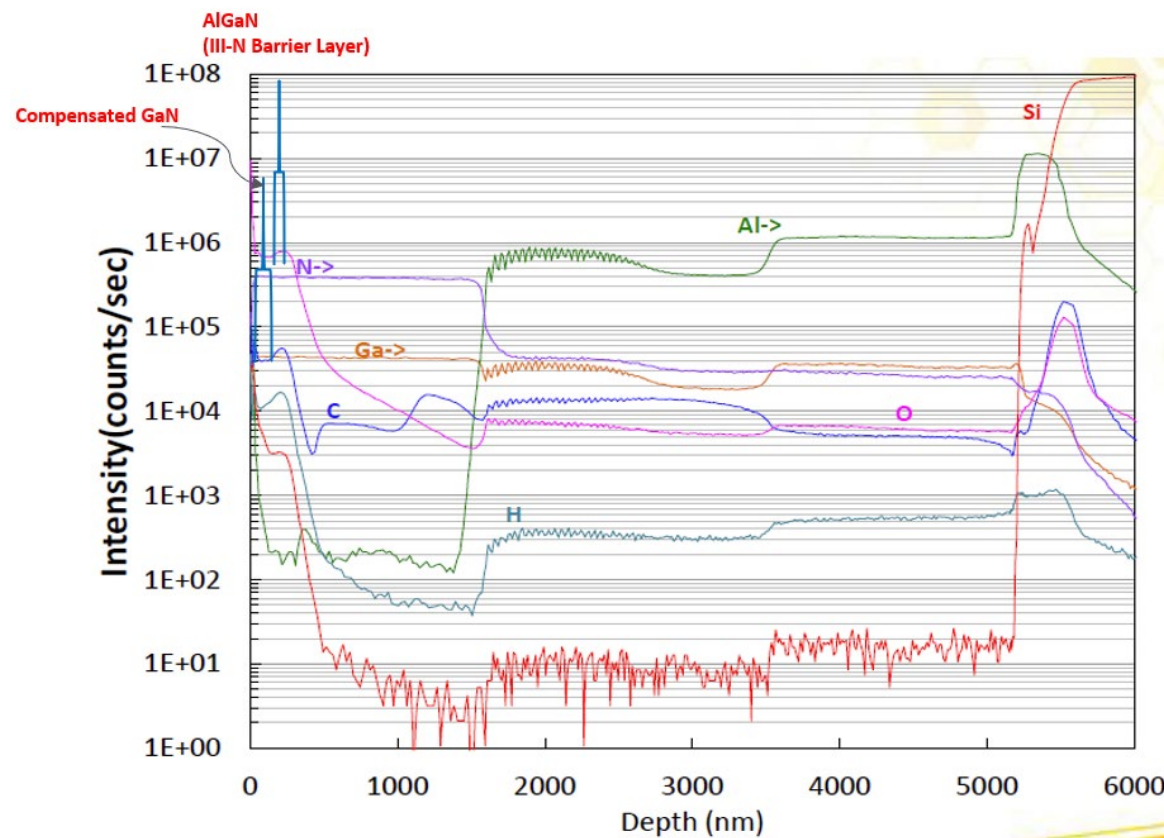


Fig. 1. Schematic illustration (top) and cross-section TEM micrograph (bottom) of the gate area of the p-GaN gate transistors.

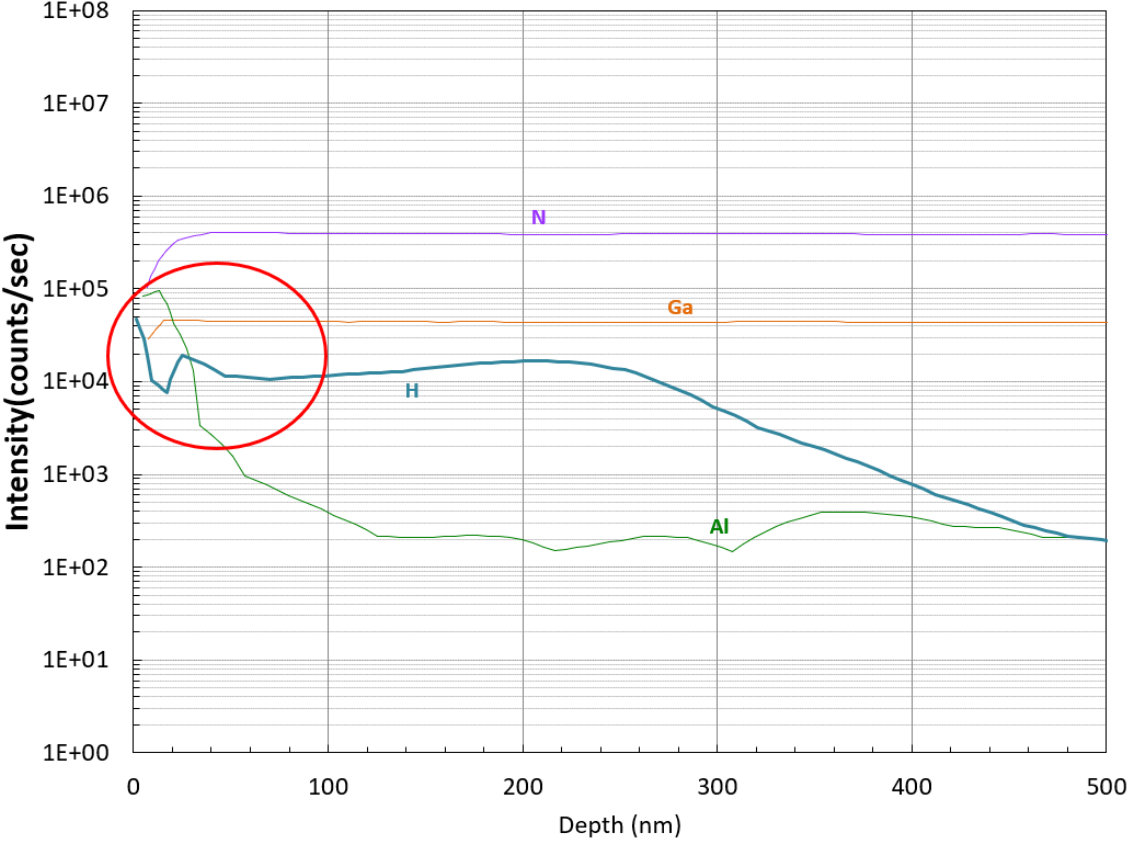
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Claim 2	
[2a] The transistor of claim 1,	See Claim 1.
[2b] wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.	See Claim element [1 f]. In addition, as described above, the INN650 compensated GaN layer is doped with Magnesium (Mg) atoms, which are [2b] acceptor type dopant atoms passivated with hydrogen. The Mg doped p-type GaN layer and hydrogen demonstrates that the gate material GaN layer is doped with Mg (p-GaN) and passivated by hydrogen in the compensated GaN layer.

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Claim 3	
[3a] The transistor of claim 2,	<i>See Claims 1; 2.</i>

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[3b] where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.

INN650 includes a compensated GaN layer doped with **[3b] Mg**. *See* Claim element [1f]; Claim element [2b].

