

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before the Honorable Clark S. Cheney
Chief Administrative Law Judge**

In the Matter of

**CERTAIN SEMICONDUCTOR DEVICES,
AND METHODS OF MANUFACTURING
SAME AND PRODUCTS CONTAINING
THE SAME**

Inv. No. 337-TA-1366

COMPLAINANT'S RESPONSIVE POST-HEARING BRIEF

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Pursuant to Ground Rule 14.2, Efficient Power Conversion Corporation (“EPC” or “Complainant”) submits the following Responsive Post-Hearing Brief in response to Respondents’ Innoscience (Zhuhai) Technology Company, Ltd. (“Innoscience Zhuhai”) and Innoscience America, Inc. (“Innoscience America”) (collectively, “Innoscience” or “Respondents”) Post-Hearing Initial Brief (hereinafter, “RPHIB”).

I. INTRODUCTION

The patents at issue in this case are innovative, novel, and fundamental. They are the product of laborious research and experimentation by brilliant scientists who set out to create a new type of semiconductor. The inventors, including Drs. Alex Lidow and Robert Beach, engaged in years of diligent research and endured numerous failures before achieving their “a-ha” moment.¹ The inventors went outside conventional wisdom to arrive at a gallium nitride (GaN) transistor with extremely low gate leakage, increased performance, reduced cost of manufacturing, and higher efficiency. As Dr. Lidow put it, their trial-and-error yielded something “that was completely different than what we expected.”² Their discoveries resulted in U.S. Patent Nos. 8,350,294 (“the ’294 Patent”) and 8,404,508 (“the ’508 Patent”).

The ’294 Patent describes a novel transistor including a semi-insulating compensated GaN layer located in the gate stack between the gate contact and the 2DEG layer that not only allows the 2DEG to be depleted, but also reduces gate leakage and gate capacitance—significant deficiencies of the prior art.

¹ See Tr. 91:25-93:22 (Lidow) (explaining research done), 96:18-101:5 (detailing first attempts to design a novel GaN device), 106:10-111:13 (detailing experiments), 111:14-140:7 (detailing failures and progress towards “a-ha” discovery), 151:23-153:15 (detailing “body of knowledge” developed), 155:20-157:12 (explaining perfecting device with low leakage current “100,000 times better” than conventional devices and other benefits); CX-0103C at 200 *et seq.* (EPC inventor notebook).

² Tr. 134:6-7 (Lidow).

Innoscence's invalidity challenge to the '294 Patent is based on two arguments, both of which rely on prior art that is fundamentally different from the invention of the '294 Patent and the claims at issue. In one argument, Innoscence relies on U.S. Patent Application No. 2006/0145189 A1 ("*Beach189*"), which discloses a conductive "field plate," and incorrectly contends that the field plate of *Beach189* is equivalent to the claimed semi-insulating compensated GaN layer. Innoscence also argues that *Beach189*, if combined with other prior art, teaches the asserted claims. But the proposed combination is nothing more than a hindsight reconstruction of the invention, completely lacking in motivation. Moreover, the proposed combination would not result in the claimed invention, but rather a non-functional device.

In yet another argument regarding the '294 Patent, Innoscence relies on U.S. Patent Application Publication No. US 2008/0087915 A1 ("*Uemoto*"), which, similar to the admitted prior art in the '294 Patent, discloses an activated acceptor type doped GaN (pGaN) between the gate contact and the 2DEG that results in high gate leakage and gate capacitance.

Innoscence's invalidity challenge to the '508 Patent also comes up short. The '508 Patent describes a method of manufacturing an enhancement-mode GaN transistor that results in a self-aligned gate structure. Again, Innoscence fails to establish any plausible motivation to combine steps from various prior art processes to achieve the claimed invention. With all the benefits of hindsight, Innoscence borrows selected steps from various prior art processes, but never explains how such a hypothetical combined process would work. Indeed, as EPC's expert explained at trial, Innoscence's hypothetical prior art process would not work.

Accordingly, Innoscence's invalidity challenges do not rise to the level of clear and convincing evidence.

II. LEGAL STANDARDS

A. Validity

Innoscience has the burden to prove invalidity, and the burden of proof never shifts to the patentee to prove validity. *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. NV.*, 528 F.3d 1365, 1380 (Fed. Cir. 2008). “Under the patent statutes, a patent enjoys a presumption of validity, *see* 35 U.S.C. § 282, which [Innoscience] must overcome through facts supported by clear and convincing evidence.” *SRAM Corp. v. AD -II Eng’g, Inc.*, 465 F.3d 1351, 1357 (Fed. Cir. 2006); *see also* *Microsoft Corp. v. i4i Ltd. P’ship*, 564 U.S. 91, 100-114 (2011) (upholding the “clear and convincing” standard for invalidity). The clear and convincing evidence standard has been described as evidence that “produces in the mind of the trier of fact an abiding conviction that the truth of a factual contention is ‘highly probable.’” *Price v. Symsek*, 988 F.2d 1187, 1191 (Fed. Cir. 1993) (quoting *Buildex, Inc. v. Kason Indus., Inc.*, 849 F.2d 1461, 1463 (Fed. Cir. 1988)).

1. Anticipation

To establish that a patent is invalid as being anticipated under 35 U.S.C. § 102, Innoscience must prove by clear and convincing evidence that each and every limitation is found either expressly or inherently in a single prior art reference. *Celeritas Techs. Inc. v. Rockwell Int’l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998). Anticipation is a question of fact, including whether a limitation, or element, is inherent in the prior art. *In re Gleave*, 560 F.3d 1331, 1334-35 (Fed. Cir. 2009). Although an identity of terminology is not required, the limitations must be arranged or combined the same way as in the claimed invention. *Id.* at 1334 (“the reference need not satisfy an *ipsissimis verbis* test”). In addition, the prior art reference’s disclosure must enable one of ordinary skill in the art to practice the claimed invention “without undue experimentation.” *Gleave*, 560 F.3d at 1334-35.

While a prior art reference that allegedly anticipates the claims of a patent is presumed enabled, Complainant may present evidence of non-enablement to overcome this presumption. *See e.g., Raytheon Techs. Corp. v. Gen. Elec. Co.*, 993 F.3d 1374, 1381-82 (Fed. Cir. 2021). “[W]hether a prior art reference is enabling is a question of law based upon underlying factual findings.” *Gleave*, 560 F.3d at 1335.

2. Obviousness

To establish that a patent is invalid as being obvious under 35 U.S.C. § 103, Innoscience must establish by clear and convincing evidence that “the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103; *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007) (“[T]he burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so.”). The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is an apparent reason to combine the known elements in the fashion claimed by the patent at issue. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417-18 (2007). Because obviousness is determined at the time of invention, rather than the date of litigation, “[t]he great challenge of the obviousness judgment is proceeding without any hint of hindsight.” *Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1375 (Fed. Cir. 2011).

Obviousness is a determination of law based on underlying determinations of fact. *Star Scientific*, 655 F.3d at 1374. The factual determinations, otherwise known as *Graham* factors,

behind a finding of obviousness include: (1) the scope and content of the prior art, (2) the level of ordinary skill in the prior art, (3) the differences between the claimed invention and the prior art, and (4) secondary considerations of non-obviousness. *KSR*, 550 U.S. at 399 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)).

Complainant may also establish objective indicia of non-obviousness (also known as “secondary considerations of non-obviousness”), which include factors such as commercial success, long felt but unresolved need, and the failure of others. *Id.* When present, objective indicia “give light to the circumstances surrounding the origin of the subject matter sought to be patented,” but they are not dispositive on the issue of obviousness. *Geo. M. Martin Co. v. Alliance Mach. Sys. Int’l*, 618 F.3d 1294, 1304-06 (Fed. Cir. 2010). Objective indicia of non-obviousness carry more substantial weight where there is a nexus between the evidence and the merits of the claimed invention. *See W. Union Co. v. MoneyGram Payment Sys. Inc.*, 626 F.3d 1361, 1372–73 (Fed. Cir. 2010) (citing *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995)).’

III. Validity

A. Validity of the ’294 Patent

The ’294 Patent is entitled “Compensated Gate MISFET and Method for Fabricating the Same” and is directed towards a column III Nitride transistor having, in certain embodiments, a compensated semiconductor gate layer 38 formed over the barrier layer 34 and under the gate contact 37.³ The ’294 Patent names Alexander Lidow and Robert Beach, among others, as inventors.⁴ The ’294 Patent issued from U.S. Patent Application Serial No. 12/756,906, filed on

³ See JX-0014 at 3:8-9.

⁴ *Id.* at [75].

April 8, 2010, and claims priority to U.S. Provisional Patent Application Serial No. 61/167,792, filed on April 8, 2009.⁵

The '294 Patent identifies several advantages over preexisting transistors, including that “(1) the capacitance from gate to channel layer when the device is on is lower than in the prior art; (2) the gate bias can be driven much more positive without significant current through the gate . . .; and (3) hole injection from the gate into the channel layer is dramatically reduced relative to the prior art.”⁶ The '294 Patent explains that the compensated semiconductor gate, in particular, a compensated GaN gate material, “leads to low gate leakage during device operation” and “reduced the gate capacitance of the device.”⁷ It further teaches that “the high doping level of the compensated layer 38 leads to enhancement mode devices.”⁸

The '294 Patent describes improvements to conventional enhancement-mode (E-mode) GaN transistors.⁹ At the time of the '294 Patent, high gate current leakage occurred in conventional enhancement-mode GaN transistors from the gate contact through and around the gate semiconductor material.¹⁰ Therefore, the inventors of the '294 Patent designed and achieved a GaN transistor with low gate leakage current through, in part, the inclusion of a compensated GaN layer above the barrier layer and below the gate contact layer.¹¹ In particular, compensated GaN layer 38 is located in the gate structure and prevents a bulk leakage current between gate contact 37 and barrier layer 34.¹²

⁵ *Id.* at [21]-[22], [60].

⁶ *Id.* at 4:21-29.

⁷ *Id.* at 3:18-21.

⁸ *Id.* at 3:16-17.

⁹ *See id.* at 1:13-18, 4:55-57.

¹⁰ *Id.* at 2:3-6.

¹¹ *Id.* at 2:13-19.

¹² *Id.* at 3:7-9.

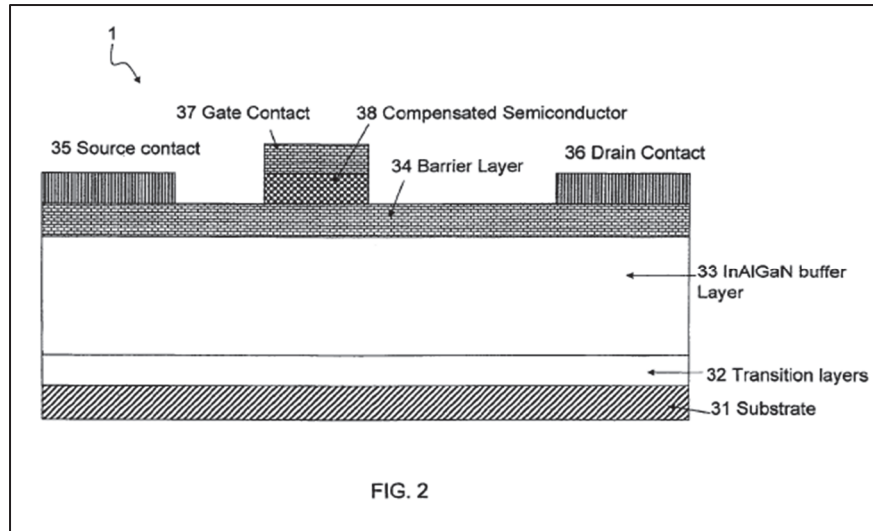


Figure III.A-01: '294 Patent FIG. 2.¹³

Figure 2 of the '294 Patent (reproduced above), provides an exemplary embodiment of its enhancement-mode III-N (GaN) transistor. As would be understood by a person of ordinary skill in the art (POSA),¹⁴ additional materials and layers would be deposited and formed above the source, drain, and gate contacts to produce a functional transistor. The III-N (GaN) transistor of the '294 Patent includes substrate 31, which can be made of, for example, silicon, silicon carbide, or sapphire.¹⁵ As high-quality GaN cannot be deposited directly on the substrate, the '294 Patent includes a set of III-N transition layers 32 to transition from the substrate to a III-N (GaN) buffer layer.¹⁶ According to the '294 Patent, the set of transition layers can include AlN or AlGaIn.¹⁷ A buffer layer 33 separates the transition layers from a barrier layer 34.¹⁸ The buffer layer can include some combination of In, Al, and GaN with any concentration of In and Al (including a

¹³ *Id.* at FIG. 2.

¹⁴ Declaration of Dr. Eric Fred Schubert in Support of Complainant's Opening Claim Construction Brief ¶ 24. The result in this investigation is the same whether EPC's or Innoscience's definition of a POSA is applied.

¹⁵ JX-0014 at 2:57-59.

¹⁶ *Id.* at 2:59-62.

¹⁷ *Id.*

¹⁸ *Id.* at 2:62-65.

concentration of 0% for In and/or Al).¹⁹ The barrier layer is formed from AlGaN.²⁰ The aforementioned compensated semiconductor layer 38 sits above barrier layer 34 and under the gate contact 37.²¹ Compensated semiconductor layer 38 includes AlGaN or GaN with a passivated p-type impurity such as, Mg, Zn, Be, Cd, or Ca.²²

At the hearing, Innoscience’s expert, Dr. Lebby, identified three prior art patent documents that he alleges invalidate claims 1-3 of the ’294 Patent, namely U.S. Patent Application Publication No. 2006/0145189 A1 (“*Beach189*”), U.S. Patent Application Publication No. US 2008/0087915 A1 (“*Uemoto*”), and JP 2006253224A (“*Kigami*”).

1. Overview of the Prior Art

i. Beach189

Beach189 discloses a depletion-mode transistor with a “field plate,”²³ not a compensated layer between the gate contact and the barrier layer of the transistor that prevents gate leakage during operation of the transistor.²⁴

Both EPC’s and Innoscience’s experts agree that depletion-mode (normally-ON) devices require the application of a *negative* voltage to turn off the device, unlike enhancement-mode (normally-OFF) devices, which require a positive voltage to turn on the device.²⁵ *Beach189* is a depletion-mode transistor.²⁶ Its specification is unequivocal that it is intended for transistors that operate using a negative voltage:

To control the current in a high power application, a ***large negative voltage*** is applied to the gate electrode in order to change the voltage at the gate electrode

¹⁹ *Id.*

²⁰ *Id.* at 2:66-67.

²¹ *Id.* at 3:8-9.

²² *Id.* at 3:10-12.

²³ Tr. 948:20-949:5 (Schubert); RX-0011.

²⁴ *Cf.* JX-0014 3:16-21.

²⁵ Tr. 924:22-925:7 (Lebby); 953:16-954:8 (Schubert); JX-0014 at 1:53-54.

²⁶ Tr. 953:18-954:8 (Schubert).

rapidly. When a large voltage is applied to the gate electrode rapidly, a high voltage develops between the gate electrode and the drain electrode.²⁷

Figure 4 of *Beach189*, reproduced below, shows the elements of the *Beach189* device:

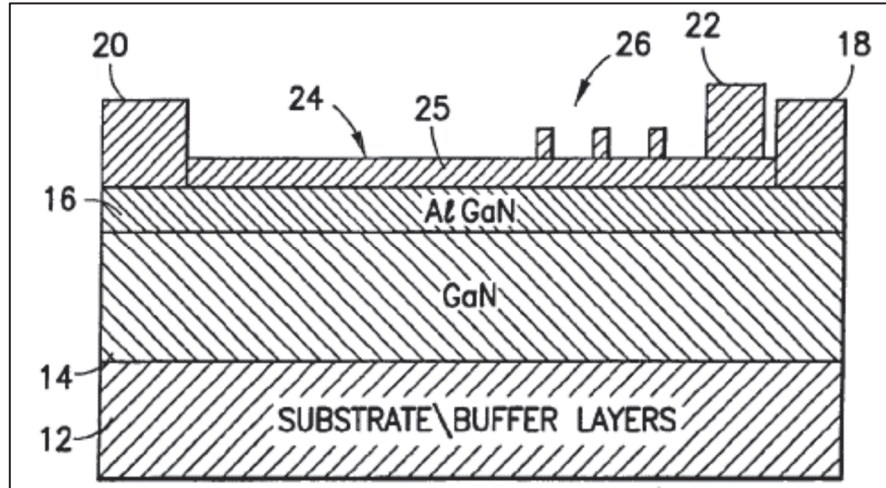


Figure III.1.i-01: *Beach189* at FIG. 4.²⁸

The field plate described in *Beach189* is a highly resistive field plate 25, an element that is separate and distinct from the gate structure.²⁹ The *Beach189* field plate is described as a “field relaxation feature,” and is intended to spread out the electrical field so that it does not damage the gate.³⁰ The gate material, referred to as gate structure 22, is protected from large electrical fields by field plate 25, which “reduce[s] the intensity of the electric fields around the gate in order to increase the breakdown voltage of the device.”³¹ *Beach189* clearly identifies a distinct element as “gate structure 22,” separate from “field plate 25.”³² Further, the *Beach189* field plate is not part of the gate, but rather protects the gate structure 22 from high electric fields.³³

²⁷ RX-0011 ¶ [0003] (emphasis added).

²⁸ *Id.* at FIG. 4.

²⁹ *Id.* ¶¶ [0004], [0006], [0028].

³⁰ *Id.* ¶¶ [0004], [0006].

³¹ *Id.* ¶ [0004].

³² *Id.* ¶¶ [0026]-[0028].

³³ Tr. 950:14-953:15 (Schubert).

ii. Uemoto

Uemoto is directed to “normally-off type nitride semiconductor transistors.”³⁴ *Uemoto* describes a third nitride semiconductor layer 15 with region 15a that is activated with conductive, negatively charged Mg acceptors and holes, and element 15b, element 15b, which is a resistive p-doped AlGaN/GaN region.³⁵ Region 15a is below the gate electrode and part of the control region.³⁶

Figure 7 of *Uemoto* shows the elements of the *Uemoto* device:

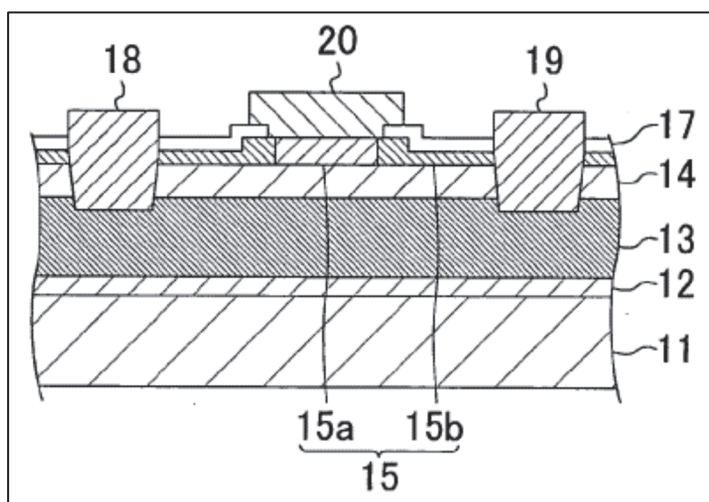


Figure III.1.ii-01: *Uemoto* at FIG. 7.³⁷

Uemoto discloses a barrier layer 14 under a third nitride semiconductor layer 15, which is partitioned into regions 15a and 15b.³⁸ Region 15a is activated with negatively charged Mg acceptors and holes.³⁹ Upon application of a positive gate voltage, the activated p-type material of region 15a operates like the “highly doped p-GaN 106” shown in prior art Figure 1 of the ’294 Patent, such that the *Uemoto* device conducts with high gate current relative to the device of the

³⁴ RX-0073 ¶ [0003].

³⁵ *Id.* ¶¶ [0033], [0048]-[0049], [0066].

³⁶ Tr. 960:25-961:4 (Schubert); Tr. 931:9-12 (Lebby); RX-0073, at FIG. 7.

³⁷ RX-0073, at FIG. 7.

³⁸ Tr. 959:24-960:10 (Schubert); RX-0073 ¶ [0033]; CDX-0003.20-21.

³⁹ *Id.*

'294 Patent.⁴⁰ According to *Uemoto*, at zero voltage, the 2DEG is depleted under control region 15a, but remains present under high resistive region 15b.⁴¹

The conductive control region 15a of *Uemoto* contains activated (conductive) p-type material.⁴² *Uemoto* intentionally activates the Mg dopants in the control region: “When a thermal treatment is performed in an inert gas atmosphere at 800°C. for about 20 to 60 minutes, the hydrogen atom is desorbed from Mg. Then, the Mg is activated, and thus the nitride semiconductor layer shows p-type conductivity.”⁴³ *Uemoto* specifically notes that this activation process is performed in a nitrogen atmosphere.⁴⁴ That is in contrast to the high resistive region 15b, “in which the p-type impurity is not activated to offer a high resistive layer,” and is not part of the control region.⁴⁵ As *Uemoto* explains: “The third nitride semiconductor layer doped with Mg is composed of: a control region 15a in which Mg is activated to exhibit a p-type conductivity; and a high resistive region 15b in which Mg is not activated to offer a higher resistance than the control region 15a.”⁴⁶

iii. Kigami

Kigami is directed to a normally-OFF transistor in which hydrogen is present in the electron channel, not in the gate semiconductor above the channel.⁴⁷ Specifically, hydrogen is located in local region 34, above the semiconductor layer 32, and purportedly “forms a composite” with the magnesium in the local region 34.⁴⁸ The semiconductor layer 32 is formed directly on the substrate

⁴⁰ RX-0073 ¶ [0049]; JX-0014, at FIG. 1.

⁴¹ Tr. 959:24-960:10, 964:22-965:4 (Schubert); RX-0073 ¶ [0038].

⁴² Tr. 959:24-960:10 (Schubert); RX-0073 ¶ [0033]; CDX-0003.20-21.

⁴³ RX-0073 ¶ [0051].

⁴⁴ *Id.* ¶ [0048].

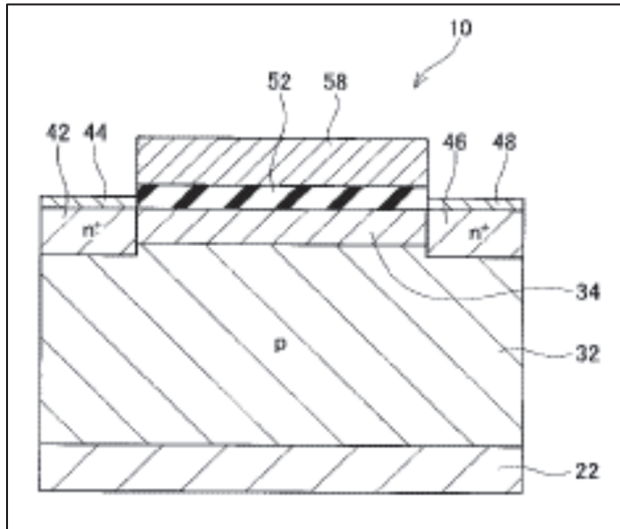
⁴⁵ *Id.* ¶¶ [0033], [0051]; Tr. 964:19-968:6 (Schubert).

⁴⁶ RX-0073 ¶ [0033].

⁴⁷ RX-0079 ¶¶ [0020]-[0022]; Tr. 949-21:950:8 (Schubert).

⁴⁸ *Id.* ¶ [0022]; Tr. 949-21:950:8 (Schubert); CDX-0003.6 (citing RX-0079, at FIG. 1).

film 52.⁵¹

Figure III.1.iii-01: *Kigami* at FIG. 1.⁵²insulator.⁵⁵

⁴⁹ *Id.* ¶ [0024].

50 *Id.*

⁵¹ *Id.* ¶ [0020].

⁵² *Id.* at FIG. 1.

⁵³ *Id.* at FIG. 1 & ¶ [0020]; Tr. 949-21:950:8 (Schubert); CDX-0003.6 (citing RX-0079, at FIG. 1).

⁵⁴ RX-0079 ¶ [0023]; Tr. 958:24-959:11 (Schubert); CDX-0003.18.

⁵⁵ Tr. 957:17-958:17 (Schubert).

2. Beach189

i. Beach189 does not anticipate Claim 1

a. Claim 1 is directed to an enhancement-mode transistor

Claim 1 of the '294 Patent is directed to an enhancement-mode transistor. The “Field of the Invention” section of the '294 Patent confirms that the invention “relates to the field of enhancement mode gallium nitride (GaN) transistors.”⁵⁶ In describing embodiments of its invention, the '294 Patent discloses two types of enhancement-mode GaN transistors: “**an enhancement mode GaN transistor with a compensated GaN layer or a semi-insulating GaN layer** below the gate contact and above the barrier layer.”⁵⁷ Claim 1 of the '294 Patent recites one of these types of enhancement-mode transistors: “[a] column III Nitride transistor comprising....a compensated GaN layer above the barrier layer...”⁵⁸

The specification of the '294 Patent also explains that the compensated semiconductor GaN layer 38, which is recited in claim 1, is formed over the barrier layer 34 and under the gate contact 37,⁵⁹ and further discloses that “the high doping level of the compensated layer 38 leads to enhancement mode devices.”⁶⁰ The '294 Patent describes the compensated semiconductor gate, in particular, a compensated GaN gate material, as the element that “leads to low gate leakage during device operation” and “reduces the gate capacitance of the device,”⁶¹ which remedies deficiencies (very high gate leakage) in the prior art enhancement-mode GaN transistor described in FIG. 1.⁶²

⁵⁶ JX-0014 at 1:13-14.

⁵⁷ *Id.* at 1:14-17 (emphasis added).

⁵⁸ *Id.* at 5:11-17.

⁵⁹ *See id.* at 3:8-9.

⁶⁰ *Id.* at 3:16-17.

⁶¹ *Id.* at 3:18-21.

⁶² *Id.* at 2:3-6 (referring to FIG. 1).

At the evidentiary hearing, EPC's expert, Dr. Schubert, further confirmed that the compensated GaN layer of claim 1 results in an enhancement-mode transistor, stating: "The high doping of the semi-insulating [compensated] layer 38 leads to enhancement-mode devices. The 2DEG region is depleted, that is, removed."⁶³ Moreover, in his comparison of the prior art enhancement-mode device to the compensated GaN transistor disclosed by the '294 Patent, Dr. Schubert explained that both devices were enhancement-mode, but the difference between the two was the non-conductive nature of the compensated pGaN layer of the inventive device.⁶⁴ Thus, as Innoscience agrees, the p-doping of the pGaN that is required for forming the compensated GaN layer recited in claim 1 necessarily results in an enhancement-mode transistor.⁶⁵

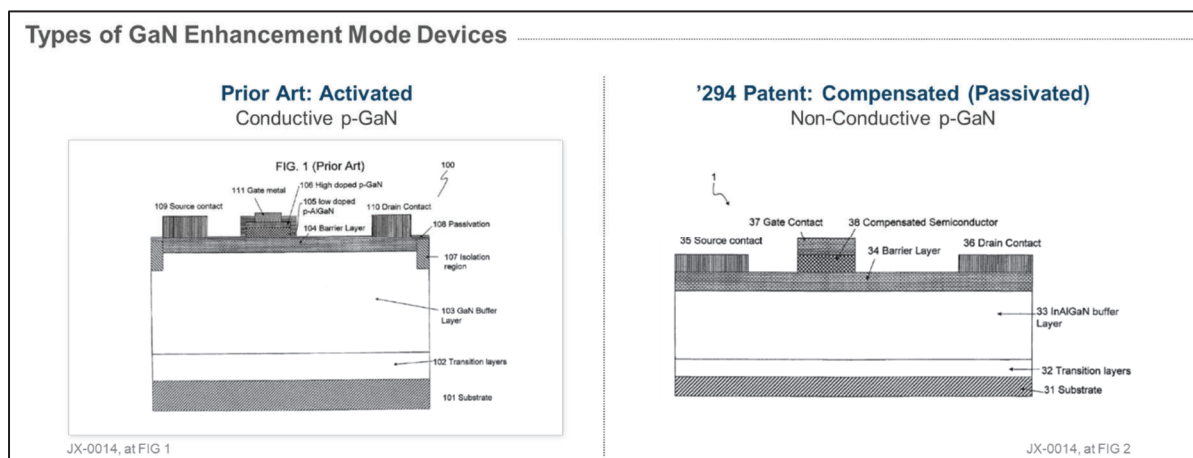


Figure III.A.2.i.a-01: '294 Patent at FIGS. 1 & 2.⁶⁶

The '294 Patent discloses (and must use) p-type dopants in its compensated GaN gate material, in order to deplete the 2DEG, as explained above, and thereby forms an enhancement-mode device.⁶⁷ Indeed, the '294 Patent states that its "[c]ompensated semiconductor layer 38

⁶³ Tr. 436:5-17, 442:20-443:18 (Schubert).

⁶⁴ *Id.* at 433:5-22.

⁶⁵ Tr. at 936:17-937:2 (Lebby) ("If you design a device with p-type material as we've heard in this litigation, it's enhancement-mode.").

⁶⁶ CDX0002.3 (citing JX-0014, at FIG. 1 and FIG. 2).

⁶⁷ *See* Tr. 926:1-22 (Lebby) (admitting that p-type doping is necessary for a device to be enhancement-mode).

preferably comprises AlGa_N or Ga_N with a deep level passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca.”⁶⁸ Both parties’ experts agree that p-type dopants are necessary for depletion of the 2DEG at zero voltage, without which the enhancement-mode device described in the ’294 Patent is unattainable.⁶⁹

Innoscence’s expert, Dr. Lebby, agreed that a compensated Ga_N layer results in an enhancement-mode Ga_N transistor, conceding that there would be no 2DEG beneath the compensated layer 38 (as shown FIG. 2 of the ’294 Patent) at zero voltage.⁷⁰ It is also undisputed that this depletion of the 2DEG electrons would result in an enhancement-mode device.⁷¹ It follows then that claim 1, reciting precisely such a compensated Ga_N layer, is directed to an enhancement-mode transistor.

b. Beach189 is not directed to an enhancement-mode transistor, as required by Claim 1

Beach189, in contrast to claim 1 of the ’294 Patent, is directed to a depletion-mode transistor.⁷² Indeed, *Beach189* is concerned with improving the operation of depletion-mode transistors:

To control the current in a high power application, a large negative voltage is applied to the gate electrode in order to change the voltage at the gate electrode rapidly. When a large voltage is applied to the gate electrode rapidly, a high voltage develops between the gate electrode and the drain electrode.⁷³

Beach189 attempts to address the damage that such a high negative voltage would cause to the device’s gate.⁷⁴ That is consistent with the entirety of *Beach189*, which does not mention

⁶⁸ JX-0014 at 3:10-12.

⁶⁹ Tr. 926:16-22, 936:17-937:2 (Lebby) (“If you design a device with p-type material as we’ve heard in this litigation, it’s enhancement-mode.”); Tr. 956:13-21 (Schubert).

⁷⁰ *Id.* at 933:19-934:3 (Lebby).

⁷¹ *Id.*

⁷² Tr. 953:16-954:8 (Schubert); CDX-0003.12 (citing RX-0011 ¶ [0003], FIG. 4).

⁷³ RX-0011 ¶ [0003]; Tr. 377:23-378:13 (Beach).

⁷⁴ RX-0011 ¶¶ [0003]-[0004].

positive voltage *anywhere* in its disclosure. As Dr. Schubert explained, and Dr. Lebbby agreed, only depletion-mode transistors operate using a negative voltage.⁷⁵

More specifically, Dr. Schubert explained that a negative voltage is used to deplete the 2DEG in a normally-ON depletion-mode device: “putting a negative voltage on the gate or putting a negative charge on the gate will deplete the pre-existing 2DEG, thereby reducing the current.”⁷⁶ Innoscience’s expert, Dr. Lebbby, agreed, conceding that *Beach189*’s disclosure of negative voltage meant that it was directed to a depletion-mode device: “Paragraph three is in the background of the invention. I will agree with you that a negative voltage is typically one would expect from a deletion [*sic*, depletion] mode device...”⁷⁷

Dr. Schubert explained that depletion-mode transistors are vastly different from and inferior to enhancement-mode devices.⁷⁸ Depletion-mode transistors, unlike enhancement-mode transistors, require a fully extant 2DEG at zero voltage, and operate using a negative voltage, rather than the positive voltage that enhancement-mode devices need to reconstitute the 2DEG for operation.⁷⁹ Due to those differences, a POSA would not consider the depletion-mode *Beach189* device equivalent to the enhancement-mode transistor claimed in the ’294 Patent.⁸⁰

⁷⁵ Tr. 953:16-954:8 (Schubert); Tr. 924:22-925:7 (Lebbby).

⁷⁶ Tr. 954:3-6 (Schubert).

⁷⁷ Tr. 925:4-7 (Lebbby).

⁷⁸ Tr. 432:4-435:5 (Schubert)

⁷⁹ Tr. 914:15-915:11 (Lebbby).

⁸⁰ Tr. 953:18-954:8 (Schubert) (“*Beach189* is a depletion-mode transistor.”); Tr. 377:23-378:21 (*Beach*); 432:8-433:4 (Schubert) (explaining the technical differences between depletion- and enhancement-mode devices); Tr. 914:22-915:7 (Lebbby) (same).

c. Operating Beach189 as an enhancement-mode transistor would result in a non-functioning device

Beach189's design as a depletion-mode (normally-ON) transistor requires that its components do *not* deplete the 2DEG at zero voltage.⁸¹ As such, under the interpretation proposed by Innoscience, the *Beach189* field plate—which extends from the source to the drain—would prevent the transistor from operating as an enhancement-mode device.⁸²

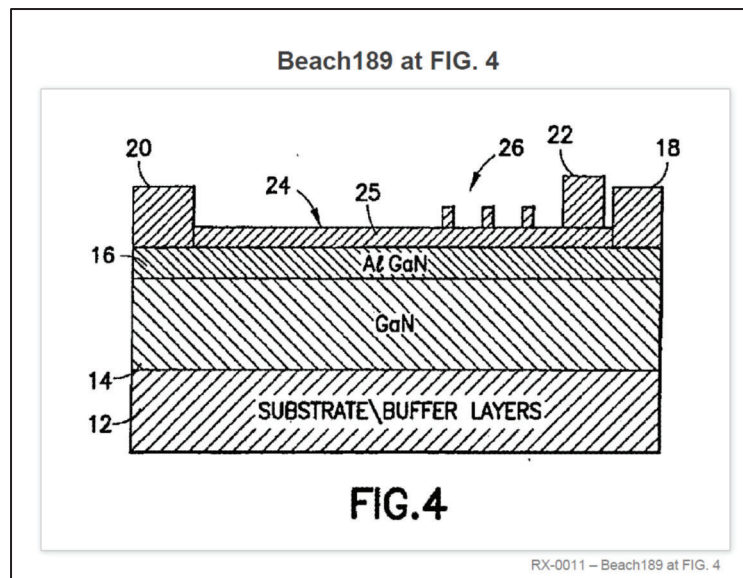


Figure III.A.2.i.c-01: *Beach189* at FIG 4.⁸³

As shown in FIG. 4 of *Beach189* above, the field plate that Innoscience equates to the claimed compensated GaN layer extends from the source to the drain of the depletion-mode transistor and is in contact with both.⁸⁴ Although EPC maintains that the *Beach189* field plate as disclosed is not doped by a p-type dopant, there are only two possible ways the field plate could be doped: (1) with a p-type dopant; or (2) with an n-type dopant.⁸⁵ If the field plate were p-doped

⁸¹ Cf. Tr. 953:16-954:8 (Schubert) (establishing that a depletion-mode device requires that a negative gate voltage be applied to deplete the 2DEG); Tr. 914:15-917:8 (Lebby) (same).

⁸² Tr. 954:11-955:3 (Schubert); Tr. 925:20-927:12 (Lebby).

⁸³ CDX-0003.4.

⁸⁴ *Id.*

⁸⁵ Tr. 954:11-955:12 (Schubert); *see also* Tr. 926:11-15 (Lebby).

and then compensated by hydrogen, the “compensated” field plate would act as “an electron sponge,”⁸⁶ depleting the 2DEG from the source to the drain.⁸⁷ Once the 2DEG was depleted across the entire length between the source and drain, the application of a positive voltage to the gate would not reconstitute the 2DEG across that length.⁸⁸ Accordingly, the transistor would be unable to turn on, and would be non-functional as an enhancement-mode device.⁸⁹ Conversely, if the *Beach189* field plate was n-doped, it would contain donor-type dopants that could not be passivated by hydrogen because both are electron donors.⁹⁰ As a result, the n-doped field plate would have an excess of electrons and would not be able to accept any 2DEG electrons. Because it cannot deplete the 2DEG, the parties agree that an n-doped field plate would necessarily result in a depletion-mode transistor.⁹¹

At the evidentiary hearing, Innoscience’s expert, Dr. Lebby, attempted to introduce a new opinion that was inconsistent with his prior testimony regarding the non-functional nature of *Beach189* in enhancement-mode.⁹² At the hearing, Dr. Lebby improperly testified, with regard to *Beach189*’s operability, that “if you put enough voltage on it... You may have lots of leakage, but certainly you can make it work and make it an operating device.”⁹³ EPC objected to the testimony as new and outside the scope of Dr. Lebby’s report and deposition testimony, and the CALJ held

⁸⁶ Tr. 378:5-21 (Beach).

⁸⁷ Tr. 954:11-955:3 (Schubert).

⁸⁸ Tr. 926:24-927:12 (Lebby).

⁸⁹ Tr. 953:21-955:3 (Schubert).

⁹⁰ See *id.* at 955:5-21 (Schubert); 926:11-22 (Lebby).

⁹¹ Cf. *id.* at 955:5-21 (Schubert) (nothing that a field plate with an n-type dopant could not operate as an enhancement-mode device); 936:19-937:2 (Lebby) (stating that “if you design a device with n-type material then it is a depletion-mode. If you design a device with p-type material as we’ve heard in this litigation, it’s enhancement-mode.”)

⁹² Tr. 938:11-943:9 (Lebby).

⁹³ *Id.* at 938:11-939:8.

that objection in abeyance.⁹⁴ As apparent from the hearing,⁹⁵ Dr. Lebby's new opinion is absent from his report and is directly contradicted by his deposition testimony below, in which he admitted that he did not perform any analysis on the operability of *Beach189*, in enhancement-mode or in general.

1	Is it your opinion that Figure 4 shows an
2	operational transistor?
3	A So the question is, is Exhibit 6,
4	Beach189 -- is what is taught in this patent
5	application publication of a gallium nitride FET
6	that uses -- that uses an ultra resistive field
7	plate formed with highly electrically resistive
8	material that includes compensated gallium nitride
9	in paragraph 26 of Beach189 is such a device, even
10	though I haven't seen any results of whether this
11	device is operational in Beach189.
12	And I certainly haven't seen any analysis
13	by Dr. Schubert to say whether this device is
14	operational or not. And I certainly haven't done a
15	model or a simulation to say whether Figure 4 in
16	Beach189 is operational or not.

Lebby Dep. Tr. at 90:1-16

⁹⁴ *Id.* at 943:6-9.

⁹⁵ Tr. 939:11-942:24 (highlighting that Dr. Lebby was asked about the state of *Beach189*'s 2DEG if the field plate were compensated and did not have any specific theory on how to make *Beach189* operational at that time or countering Dr. Schubert's explanation of *Beach189*'s source-to-drain depletion of the 2DEG if enhancement-mode operation was attempted).

8 Q How would you respond to Dr. Schubert's
9 statement in that paragraph that if field plate were
10 compensated (passivated) p-type gallium nitride, it
11 would deplete 2DEG electrons below it, and that
12 since the field plate extends across the entire
13 length between the source and drain, the entire 2DEG
14 (from source to drain) is depleted?

15 A So the comment here by Dr. Schubert
16 really is about the Beach189 gallium nitride FET
17 structure at Figure 4.

18 What we don't know about Figure 4 is,
19 there's no scaling on the figure. So we don't
20 really know how far the distance is between the
21 source and the drain. We don't really know what the
22 size of the gate is. We don't really know how close

94

1 the gate is to the source or the drain. And we
2 don't really know where those field conductors 26
3 are actually positioned.

4 There is a top view, but even in top
5 view, there really isn't a scale.

6 And so while Dr. Schubert has certainly
7 made some assumptions assuming this is perfectly to
8 scale, I would argue that I don't see this as being
9 exactly to scale. And I certainly don't see it
10 being exactly how Dr. Schubert expects it to be.

11 I've already indicated on record,
12 depending on a lot of different parameters in this
13 device, this certainly could operate as a
14 depletion-mode FET, but it could also operate as an
15 enhancement-mode FET.

Lebby Dep. Tr. at 93:8-94:15

12 Q Your first sentence in paragraph 154
13 states, Nor do I agree with EPC that Beach189
14 describes a depletion-mode device. Nothing in
15 Beach189 describes it as a depletion-mode device.
16 Does anything in Beach189 describe it as
17 an enhancement-mode device?
18 A As I skim through Beach189, I don't
19 believe Beach expressly calls out a depletion-mode
20 device, and I don't believe Beach expressly calls
21 out an enhancement-mode device.
22 So I don't think Beach expressly calls
1 out a MISFET. But it does teach the fact that you
2 can use a gallium nitride compensation layer on
3 layer 25, which is another term for that, that
4 Beach189 uses is a field layer and does indicate to
5 me, even though I haven't done any analysis or
6 modeling a simulation, that it could operate either
7 as a depletion-mode device or an enhancement-mode
8 device.
9 But I agree with you, I don't see any
10 evidence of it expressly calling out an E-mode or
11 enhancement device.

Lebby Dep. Tr. at 98:12-99:11

Under Ground Rule 9 and due to the prejudice to EPC, Dr. Lebby's new opinion on the alleged operability of *Beach189* in enhancement-mode should be stricken.⁹⁶

Moreover, Dr. Lebby's new theory regarding the alleged functionality of *Beach189* in enhancement-mode has no scientific basis. As Dr. Schubert testified, to turn an enhancement-mode transistor ON, the previously depleted 2DEG must be fully reconstituted between the source and the drain.⁹⁷ If *Beach189*'s field plate was p-doped and passivated with hydrogen, as alleged by Innoscience, it would be incapable of being turned on.⁹⁸

⁹⁶ Order No. 2, Ground Rule 9; 19 C.F.R. § 210.27(f).

⁹⁷ Cf. Tr. 954:11-24 (Schubert) (testifying that the device in *Beach189* could not be an enhancement-mode device because "the 2DEG on its entire length from the source to the drain would be depleted and the current path between the source and drain could not be re-established . . .).

⁹⁸ *Id.* at 954:11-955:3.

Indeed, Innoscience’s own demonstrative (reproduced below) illustrates that *Beach189* is non-functional as an enhancement-mode device. At zero voltage, under Innoscience’s own interpretation of *Beach189*, the 2DEG (represented as red dash “—”) is fully depleted from the source to the drain, confirming Dr. Schubert’s testimony that the device would be inoperable as an enhancement-mode device.⁹⁹

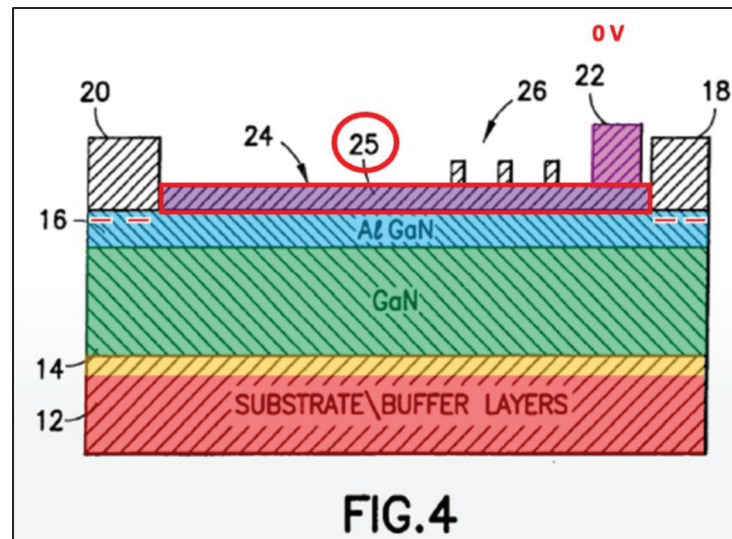


Figure III.A.2.i.c-02.¹⁰⁰

Innoscience agrees that the 2DEG is not reconstituted between the source and the drain when a positive voltage—necessary for enhancement-mode operation—is applied to the gate.¹⁰¹ When such a positive voltage (+v) is applied, as shown in Dr. Lebby’s demonstrative below, the 2DEG (represented as red dash “—”) is *only* reconstituted under the gate, which is insufficient to turn the device ON because the 2DEG is not continuous between the source and drain contacts.¹⁰² Dr. Lebby admitted as much during his redirect examination, referring to the image below, noting that “...you can establish a 2DEG with a positive voltage on an enhancement-mode, and the

⁹⁹ Tr. 937:11-24 (Lebby); Tr. 954:11-24 (Schubert).

¹⁰⁰ RDX-0100.4.

¹⁰¹ Tr. 938:1-10 (Lebby).

¹⁰² *Id.*

question here is, is that the 2DEG doesn't – **it's not continuous all the way from the source to the drain...**"¹⁰³

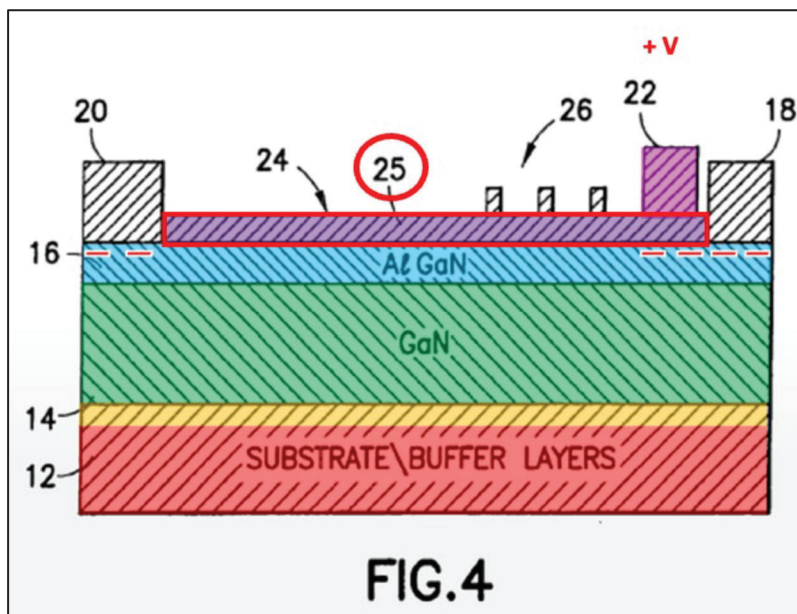


Figure III.A.2.i.c-03.¹⁰⁴

Dr. Lebby's new theory, that the 2DEG could conceivably exist "if you put enough voltage on it," is scientifically inaccurate. Indeed, Dr. Lebby admits that he has no quantitative basis for his theory—he conceded that he has neither modeled nor simulated any part of this new theory.¹⁰⁵ Dr. Lebby's vague instructions to a POSA are, thus, to "play with" various aspects of *Beach189*, with the understanding that even if such a device were to exist (and it does not), it would have "lots of leakage" due to the massive amount of voltage passing through the gate.¹⁰⁶

Moreover, Dr. Lebby's attempt to create an operational enhancement-mode device from the above Figure 4 contradicts *Beach189*'s disclosure. To arrive at this purported enhancement-mode device, Dr. Lebby would have a POSA contravene *Beach189*'s explicit teaching to use a

¹⁰³ *Id.* at 938:5-10 (emphasis added).

¹⁰⁴ RDX-0100.5.

¹⁰⁵ Tr. 938:19-939:8 (Lebby).

¹⁰⁶ *Id.* at 939:5-8.

negative voltage, substitute instead a positive voltage, and then experiment in some unexplained way with various parts of the device to make it functional.¹⁰⁷ Patent law does not permit a party to convert a prior art document into an invalidating document by opining, in handwaving fashion, that a POSA could “play with” the structure until, with the benefit of hindsight reconstruction, they arrive at the claimed invention.¹⁰⁸ Accordingly, *Beach189* does not provide an enabling disclosure for an enhancement-mode transistor, and thus, is not germane to claim 1.

d. Beach189’s field plate does not correspond to the claimed compensated GaN Layer

The field plate of *Beach189*, referred to as a field relaxation feature, is substantially different from the “compensated GaN layer” recited in claim 1 of the ’294 Patent. Those two structures perform disparate functions in a transistor, such that one cannot correspond to the other.

Dr. Schubert explained at the evidentiary hearing that the purpose of the field plate is to reduce the electric field between the source and the drain in order to prevent damage to the transistor.¹⁰⁹ To serve as a field plate, region 25 of *Beach189* must have some degree of conductivity, such that it cannot be the claimed compensated GaN layer, which must be non-conductive.¹¹⁰ Dr. Schubert explained, with reference to the diagram below, that the field plate “has free charges, is conductive, and these free charges reorient themselves based on the primary field.”¹¹¹

¹⁰⁷ *Id.* at 937:4-939:8.

¹⁰⁸ *See Apple Inc. v. Int’l Trade Comm’n*, 725 F.3d 1356, 1363-64 (Fed. Cir. 2013) (affirming a finding of no anticipation because prior art patent did not have an enabling disclosure of a fully transparent surface as claimed but only suggested that such a surface should be considered for “future work,” and further stating that “[t]here is no disclosure that the authors had achieved a transparent touch screen and the record does not indicate that it would have been routine to do so.”); *see also Raytheon Techs.*, 993 F.3d at 1381; *In re Antor Media Corp.*, 689 F.3d 1282, 1290-91 (Fed. Cir. 2012).

¹⁰⁹ Tr. 951:12-952:13 (Schubert).

¹¹⁰ *Id.* at 950:14-951:8.

¹¹¹ *Id.* at 952:4-13.

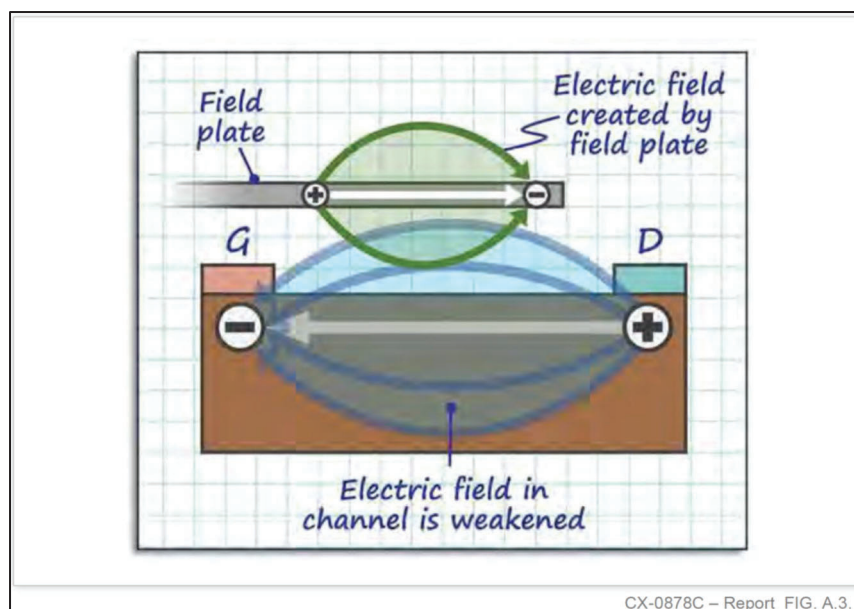


Figure III.A.2.i.d-01.¹¹²

By redistributing its free charges, the field plate creates its own electric field, which opposes and reduces the primary electric field created during transistor operation.¹¹³ In this manner, the field plate prevents damage to the transistor. The field plate's ability to create an opposing electric field, however, is dependent on its conductivity.¹¹⁴ A non-conductive field plate would lack the free charges that are necessary to generate an opposing electric field to the primary field between the source and the drain.¹¹⁵ Accordingly, interpreting the *Beach189* field plate as non-conductive, as proposed by Innoscience, would render it ineffective for its stated purpose.¹¹⁶

Indeed, Innoscience lacks any substantive support for its assertion that the *Beach189* field plate is conductive.¹¹⁷ Innoscience initially attempted to introduce extrinsic evidence, a book by Dr. Stephen Pearton, to support new opinions regarding the Pearton book in demonstratives to be

¹¹² CDX-0003.10.

¹¹³ Tr. 952:18-25 (Schubert).

¹¹⁴ *Id.*

¹¹⁵ *Id.* at 952:4-25.

¹¹⁶ *Id.* at 952:18-953:8.

¹¹⁷ *Id.* at 862:25-863:24 (Lebby).

used during Dr. Lebby's direct examination.¹¹⁸ EPC, however, objected, and Innoscience withdrew that material from its demonstratives prior to Dr. Lebby's testimony, even admitting at the hearing that "[w]e are not seeking to introduce that book into evidence anymore...."¹¹⁹ Innoscience nevertheless attempted to bring in that same withdrawn material through Dr. Lebby's testimony without the use of the objected-to demonstratives.¹²⁰ Following EPC's trial objection, the CALJ precluded Dr. Lebby from testifying on the Pearton book.¹²¹ Undeterred, Innoscience attempts to introduce the same subject matter in its post-hearing brief that was excluded from its demonstratives and was not permitted to enter through Dr. Lebby's testimony.¹²² In fact, Innoscience's post-hearing brief relies on a comparison of Figure 2 from *Beach189* to the very same parts of the Pearton book that it was prevented from entering into evidence.¹²³ This comparison, in prose, is identical to what Innoscience removed from its demonstrative and precisely what the CALJ barred Dr. Lebby from testifying to at the hearing. Indeed, Dr. Lebby has never opined on Figure 2 of *Beach189* or provided any analysis of the Pearton book. Innoscience's arguments related to the conductivity of field plates as it pertains to the Pearton book are therefore untimely, prejudicial to EPC, and should be stricken, in accordance with the CALJ's previous ruling.¹²⁴ Moreover, Innoscience's new arguments lack any supporting expert opinion and should therefore be given no weight.

¹¹⁸ *Id.* at 862:18-23.

¹¹⁹ *Id.* at 862:25-11.

¹²⁰ *Id.* at 862:5-16 (Lebby).

¹²¹ *Id.* at 862:25-863:24.

¹²² *See* RPHIB at 40 ("Even textbooks such as Dr. Pearton's (RX-0075), describe non-conductive field plates . . .").

¹²³ *Id.* at 39 (comparing the Pearton book (RX-0075) with Fig. 2 of *Beach189* (RX-0011)).

¹²⁴ Tr. 862:25-863:24 (Lebby); Order No. 2, Ground Rule 9; 19 C.F.R. § 210.27(f).

In contrast to the *Beach189* field plate, the “compensated GaN layer” of the ’294 Patent is indisputably non-conductive - and must be - in order to achieve the reduction in gate leakage current that is a stated advantage of the invention.¹²⁵ If it were conductive, the “compensated GaN layer” could not function as described in the ’294 Patent – a point Innoscience does not dispute.¹²⁶ Thus, when the required functionality of the compensated GaN layer in the ’294 Patent is considered, the *Beach189* field plate cannot correspond to the compensated GaN layer.

The *Beach189* field plate also does not correspond to the compensated GaN layer of claim 1 because it is not a part of the gate material.¹²⁷ It is undisputed that claim 1 of the ’294 Patent is directed to a column III nitride transistor.¹²⁸ In order to form such a transistor, the “compensated GaN layer” which is situated between the gate contact and the barrier layer, must be a part of the gate.¹²⁹ Indeed, the ’294 Patent is entitled “**Compensated Gate** MISFET and Method for Fabricating the Same.”¹³⁰ Further, as explained above in Section III.A.2.c, a p-doped compensated GaN layer that is not part of the gate material and extends from source to drain would deplete the 2DEG and prevent the device from turning on.¹³¹ As the CALJ astutely observed during the claim construction hearing with regard to such a structure: “Yeah, but then it wouldn’t be a transistor.”¹³² *Beach189*’s field plate therefore cannot correspond to the compensated GaN layer of the ’294 Patent.

¹²⁵ Tr. at 953:1-8 (Schubert).

¹²⁶ *Id.*

¹²⁷ *Id.* at 953:10-15.

¹²⁸ JX-0014-0018 at 5:12.

¹²⁹ Tr. 433:7-435:13; 953:10-15 (Schubert).

¹³⁰ JX-0014-0016 (emphasis added).

¹³¹ *See supra* Section III.A.2.c.

¹³² Claim Construction Hr’g Tr. at 91:7-12 (Oct. 13, 2023).

ii. Beach189 in combination with Kigami does not render Claims 2 and 3 obvious

a. Claims 2 and 3 are directed to an enhancement-mode transistor

Claims 2 and 3 of the '294 Patent are indisputably directed to enhancement-mode transistors. Claim 2 recites “the acceptor type dopant atoms are passivated by hydrogen,” while claim 3 adds that “the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.”¹³³ Claims 2 and 3 thus require the use of acceptor type dopants that can be passivated by hydrogen. The parties do not dispute that only p-type dopants, such as Mg, Zn, Be and Ca, can be passivated by hydrogen.¹³⁴ Furthermore, testimony from both parties demonstrates that enhancement-mode operation requires the use of p-type dopants;¹³⁵ indeed, the use of a p-type dopant (magnesium) passivated with hydrogen in GaN would necessarily result in an enhancement-mode device, as Dr. Lebby conceded during the hearing.¹³⁶ And as Innoscience admits in its post-hearing brief, a transistor with p-type doping “passivated with hydrogen **would** function as an enhancement mode device.”¹³⁷ Accordingly, claims 2 and 3 must be directed to an enhancement-mode transistor.¹³⁸

¹³³ JX-0014-0018 at 5:18-23.

¹³⁴ Tr. 955:5-21 (Schubert) (“It is only the p-type dopants that are passivated by hydrogen”).

¹³⁵ Tr. 997:10-998:1 (Schubert); CDX-0003.39 (citing RX-0041 ¶ [0011]); Tr. 936:17-937:2 (Lebby) (“If you design a device with p-type material as we’ve heard in this litigation, it’s enhancement-mode.”)

¹³⁶ Tr. 923:6-17 (Lebby).

¹³⁷ RPHIB at 41 (emphasis added).

¹³⁸ Tr. 923:6-17 (Lebby) (stating that magnesium passivated with hydrogen produces an enhancement-mode transistor).

b. There is no Motivation to combine Beach189 and Kigami, because operating Beach189 as an enhancement-mode transistor would result in a non-functioning device

As explained in Sections III.A.2.i.b and III.A.2.i.c above, *Beach189* is directed to a depletion-mode device and is rendered non-functional when operated in enhancement-mode.¹³⁹ Because *Beach189* cannot operate as an enhancement-mode device, a POSA would not be motivated to combine *Kigami*'s use of hydrogen to passivate magnesium with *Beach189* to arrive at the enhancement-mode transistor recited in claims 2 and 3.¹⁴⁰ *Kigami* discloses the use of hydrogen to passivate magnesium in a different layer of a fundamentally different type of device, for a different purpose.¹⁴¹ The combination of *Beach189* and *Kigami* therefore does not disclose the elements of claims 2 and 3.¹⁴² Innoscience's contrived combination of the two references would illogically require a POSA to combine a depletion-mode transistor (*Beach189*) with an enhancement-mode transistor (*Kigami*), and then retrospectively change the location of the hydrogen passivation in *Kigami* to match claims 2 and 3.

Innoscience's position is also self-contradictory on its face, asserting that *Beach189* could work in enhancement-mode, but then also requiring it to be combined with *Kigami* to arrive at the enhancement-mode transistor of claims 2 and 3. Indeed, if it is necessary with *Beach189* to "play with the level of resistance or the level of the semi-insulating level of layer 25....[to] actually get

¹³⁹ See *supra* Sections III.A.2.i.a-c.

¹⁴⁰ Tr. 957:17-958:17 (Schubert); see *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1359 (Fed. Cir. 2020) (finding no motivation to combine references where there are "fundamental differences between the references"); see also *Tec Air, Inc. v. Denso Mfg. Michigan Inc.*, 192 F.3d 1353, 1360 (Fed. Cir. 1999) ("If when combined, the references would produce a seemingly inoperative device, then they teach away from their combination.") (internal quotations omitted).

¹⁴¹ Tr. 957:17-958:17 (Schubert).

¹⁴² *Id.*; CDX-0003.17-19 (highlighting the different location and purpose of the hydrogen passivation in *Kigami*).

the 2DEG to go from the source to drain if you put enough voltage on it”,¹⁴³ then there is no reason or motivation to combine *Beach189* with *Kigami* or any other reference.¹⁴⁴ Moreover, as Innoscience’s expert, Dr. Lebby, observed at the hearing, that theoretical application of a large, undefined quantity of positive voltage to *Beach189* would not even yield a properly functional enhancement-mode transistor: “Now I will say that may not be an ideal device. You may have lots of leakage. . . . [m]ay not be the best device, but you can make it work.”¹⁴⁵ This stark admission by Dr. Lebby underscores the lack of motivation to combine *Beach189* with *Kigami*.

Furthermore, the language in the ’294 Patent conveys to a POSA that the 2DEG is depleted because the passivated p-type doping at the gate semiconductor creates enhancement-mode devices.¹⁴⁶ As Dr. Schubert explained, and as Dr. Lebby agreed, an enhancement-mode device has no 2DEG under the gate at zero gate bias; thus, the 2DEG is depleted.¹⁴⁷ *Kigami* instead discloses hydrogen passivation in a different transistor layer, the 2DEG region, and for a different purpose, reducing threshold voltage.¹⁴⁸ As a result, there is no teaching or suggestion in *Beach189* or *Kigami* that would motivate a POSA to dope a semiconductor below the gate and then seek to *cancel* the effects of the very dopant that was added, such that the POSA could arrive at a functional enhancement-mode transistor.¹⁴⁹ Indeed, there is no disclosure, teaching, or suggestion in

¹⁴³ Tr. 938 25-939:8 (Lebby).

¹⁴⁴ See *Raytheon Techs.*, 993 F.3d at 1381 (finding that a § 103 “reference must necessarily enable the relied-upon portion of its own disclosure . . .”).

¹⁴⁵ Tr. at 939:5-8 (Lebby).

¹⁴⁶ JX-0014 at 3:16-21.

¹⁴⁷ Tr. 442:17-443:18 (Schubert); *accord* Tr. 934:2-3 (Lebby) (“In an enhancement-mode device at 0 volts there will not be a 2DEG underneath the gate”).

¹⁴⁸ Tr. 957:17-958:17 (Schubert); CDX-0003.18 (noting that in *Kigami*, “[h]ydrogen is introduced to lower threshold voltage and form a channel under the gate insulating film (52), not reduce gate leakage”); RX-0079 ¶ [0004] (describing lowering p-type impurity concentration “in order to lower the threshold voltage,” rather than reduce the gate leakage current).

¹⁴⁹ See Tr. 955:24-957:9 (Schubert) (discussing generally how a POSA would not have known to cancel the effect of dopant added to a semiconductor).

Beach189 or *Kigami* that would lead a POSA to such a transistor, absent hindsight.¹⁵⁰ It would be therefore counter-intuitive and non-obvious to a POSA to combine *Beach189* with *Kigami* to arrive at the invention of claims 2 and 3.¹⁵¹

c. There are additional reasons why no motivation exists to combine Beach189 and Kigami

There is also no motivation to combine *Beach189* with *Kigami* because a POSA would find the doping of a gate semiconductor followed by the cancellation of the effects of the dopant to be highly counterintuitive.¹⁵² As Dr. Schubert explained at the hearing, the primary motivation for doping is to control the electrical conductivity of a semiconductor.¹⁵³ Donors increase the electrical conductivity by creating free electrons that are available for conduction, while acceptors increase the electrical conductivity by creating free holes that are available for conduction.¹⁵⁴ A POSA would not be motivated to create conductivity in the GaN gate semiconductor and then purposely remove that conductivity, particularly because the state of the art at the time of the '294 Patent required a conductive p-type GaN.¹⁵⁵ At the time of the '294 Patent, a POSA would have sought to remove hydrogen, rather than reintroduce it to cancel the conductivity of p-type GaN.¹⁵⁶

In *Kigami*, hydrogen is present in the electron channel, not in the gate semiconductor above the channel.¹⁵⁷ Specifically, hydrogen is located in local region 34, above the semiconductor layer 32, and purportedly “forms a composite” with the magnesium in the local region 34.¹⁵⁸ A gate-insulating film 52 is formed *above* the local region 34 of the semiconductor layer 32, and a gate

¹⁵⁰ *Id.*

¹⁵¹ *Id.* at 955:24-957:9, 959:14-21.

¹⁵² *Id.* at 955:24-957:9.

¹⁵³ *Id.* at 445:2-12.

¹⁵⁴ *Id.*

¹⁵⁵ Tr. 956:4-21 (Schubert).

¹⁵⁶ *Id.*; Tr. 104:11-105:16 (Lidow).

¹⁵⁷ RX-0079 ¶¶ [0020]-[0022].

¹⁵⁸ *Id.* ¶ [0022].

electrode is formed above that gate-insulating film 52.¹⁵⁹ *Kigami* thus has a gate insulator 52 that is *above* the insulating barrier (local region 34), and hydrogen is introduced to lower the threshold voltage and form a channel *under* the gate insulator 52.¹⁶⁰ As *Kigami* makes clear, hydrogen-passivated local region 34 is *not* the same as the compensated GaN layer recited in the '294 Patent, and there is no disclosure in *Kigami* that would motivate a POSA to passivate the gate semiconductor with hydrogen.¹⁶¹

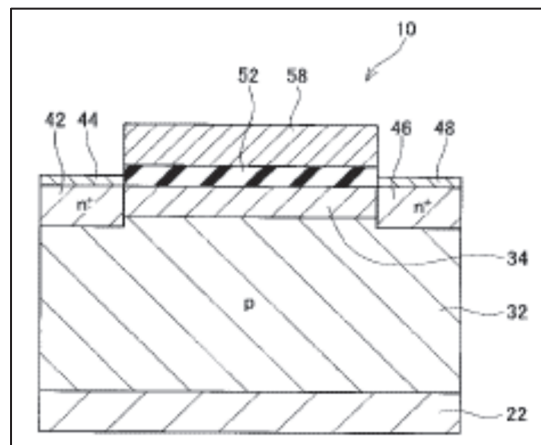


Figure III.A.2.ii.c-01: *Kigami* at FIG. 1.¹⁶²

3. Uemoto

i. Uemoto's alleged compensated GaN layer does not correspond to the claimed compensated GaN layer of Claims 1-3

a. Uemoto's claimed compensated GaN layer has no 2DEG beneath it, but region 15b does

Uemoto, as explained in Section III.A.1.ii above, is directed to an enhancement-mode transistor that has an activated p-type GaN, region 15a, below the gate electrode.¹⁶³ The 2DEG under this activated pGaN is depleted at zero voltage.¹⁶⁴ On either side of the gate structure, a p-

¹⁵⁹ *Id.* ¶ [0020].

¹⁶⁰ Tr. 957:17-958:17 (Schubert).

¹⁶¹ *Id.* at 957:17-958:17, 959:14-21.

¹⁶² RX-0079, at FIG. 1.

¹⁶³ *See supra* Section III.A.1.ii.

¹⁶⁴ *Id.*

doped high resistive region 15b is present.¹⁶⁵ As shown in the energy band diagrams below, *Uemoto* specifically notes that the 2DEG is depleted under the activated region 15a but is **not** depleted under the high resistive region 15b.

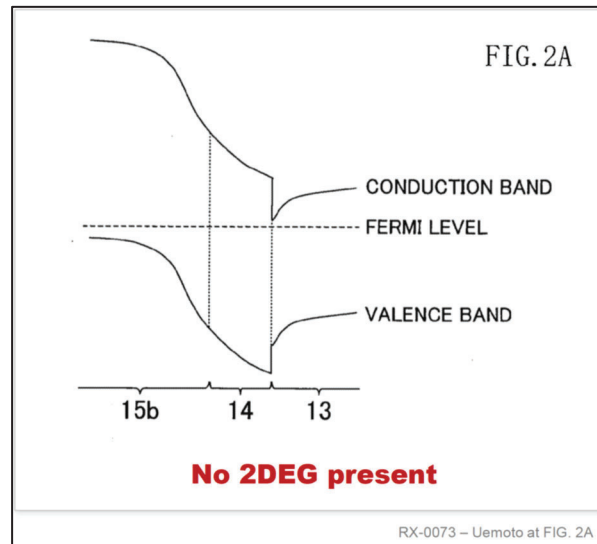


Figure III.A.3.i.a-01: *Uemoto* at FIG. 2A.¹⁶⁶

As shown in the band diagram above, the conduction band at activated region 15a (erroneously referred to in *Uemoto* as “15b” in FIG. 2A),¹⁶⁷ which is a part of the gate structure and below the gate electrode, is above the Fermi level.¹⁶⁸ This means that the 2DEG is depleted below activated region 15a.¹⁶⁹

By contrast, as shown in Figure 2B of *Uemoto* below, the Fermi level of high resistive region 15b, which Innoscience alleges corresponds to the compensated GaN layer of claim 1, is in

¹⁶⁵ *Id.*

¹⁶⁶ CDX-0003.21 (citing RX-0073 at FIG. 2A).

¹⁶⁷ Tr. 1031:9-1032:9 (establishing that all parties agree “15b” in FIG. 2A is a typo and should be “15a”).

¹⁶⁸ Tr. 960:25-961:19 (Schubert).

¹⁶⁹ *Id.*

the conduction band.¹⁷⁰ This means that the 2DEG is **present and not depleted** under high resistive region 15b,¹⁷¹ a point that is not disputed by the parties.¹⁷²

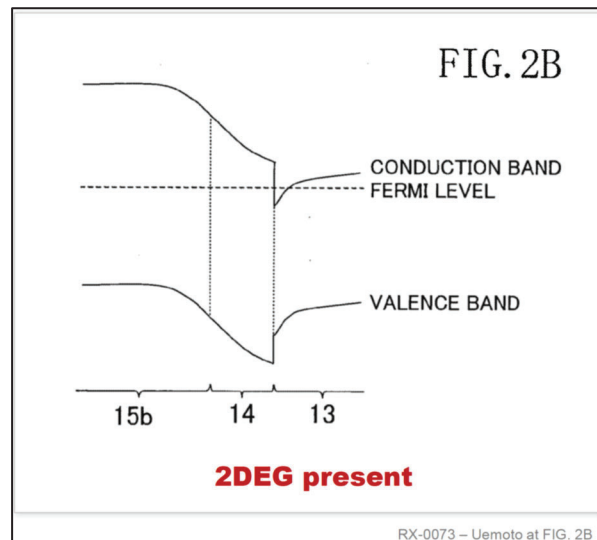


Figure III.A.3.i.a-02: *Uemoto* at FIG. 2B.¹⁷³

The parties do not dispute that the 2DEG must be depleted under the compensated GaN layer of the '294 Patent's transistor for it to operate as described.¹⁷⁴ By contrast, as Dr. Schubert explains with regard to *Uemoto*: "So if we choose region 15B – 15B as Dr. Lebbby proposes, and if we go by the teachings of the prior art, we do not create an enhancement-mode transistor. We do not remove the 2DEG."¹⁷⁵ Thus, because the 2DEG is present under *Uemoto*'s high resistive region 15b, it cannot correspond to the compensated GaN layer of claim 1.¹⁷⁶

Furthermore, *Uemoto* does not disclose the elements of claims 2 or 3. Claim 2 recites "the acceptor type dopant atoms are passivated by hydrogen," while claim 3, depending from claim 2,

¹⁷⁰ *Id.* at 961:22-962:21.

¹⁷¹ *Id.*

¹⁷² Tr. at 933:10-15 (Lebbby).

¹⁷³ CDX-0003.22 (citing RX-0073 at FIG. 2B).

¹⁷⁴ Tr. 442:17-443:18 (Schubert); *accord* Tr. 934:2-3 (Lebbby) ("In an enhancement-mode device at 0 volts there will not be a 2DEG underneath the gate").

¹⁷⁵ Tr. 962:9-12 (Schubert).

¹⁷⁶ *Id.* at 962:7-21.

recites “the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.”¹⁷⁷ As explained above, claims 2 and 3 are directed to an enhancement-mode transistor.¹⁷⁸ Innoscience does not dispute that only p-type dopants, such as Mg, Zn, Be and Ca, can be passivated by hydrogen.¹⁷⁹ Furthermore, the parties’ testimony demonstrates that enhancement-mode operation requires the use of p-type dopants.¹⁸⁰ Innoscience’s expert, Dr. Lebby, confirms that the use of a p-type dopant (magnesium) passivated with hydrogen in GaN would necessarily result in an enhancement-mode device.¹⁸¹ Innoscience also admits in its post-hearing brief that a transistor with p-type doping “passivated with hydrogen *would* function as an enhancement mode device.”¹⁸² Accordingly, Innoscience and its expert agree that p-type doped GaN passivated by hydrogen *causes* a transistor to be an enhancement-mode transistor. Because, as the parties agree, an enhancement-mode transistor is normally OFF due to a depleted 2DEG at zero voltage, it follows that the enhancement-mode transistor recited by claims 2 and 3 has no 2DEG below the hydrogen-passivated pGaN at zero voltage.¹⁸³

By contrast, *Uemoto*’s high resistive region 15b has an intact 2DEG below it.¹⁸⁴ That 2DEG prevents high resistive region 15b from creating an enhancement-mode transistor, as required by claims 2 and 3.¹⁸⁵ As a result, the high resistive region 15b cannot correspond to the

¹⁷⁷ JX-0014-0018 at 5:18-23.

¹⁷⁸ See *supra* Section III.A.2.ii.a.

¹⁷⁹ Tr. 955:5-12 (Schubert) (“It is only the p-type dopants that are passivated by hydrogen”).

¹⁸⁰ Tr. 997:10-998:1 (Schubert); CDX-0003.39 (citing RX-0041 ¶ [0011]); Tr. 936:17-937:2 (Lebby).

¹⁸¹ Tr. 923:6-17 (Lebby).

¹⁸² RPHIB at 41 (emphasis added).

¹⁸³ Tr. 442:17-443:18 (Schubert); *accord* Tr. 934:2-3 (Lebby) (“In an enhancement-mode device at 0 volts there will not be a 2DEG underneath the gate”).

¹⁸⁴ Tr. 962:7-21 (Schubert).

¹⁸⁵ Cf. Tr. 934:2-3 (Lebby) (“In an enhancement-mode device at 0 volts there will not be a 2DEG underneath the gate”).

hydrogen-passivated pGaN recited in claims 2 and 3, because it is unable to deplete the 2DEG at zero voltage and create an enhancement-mode transistor.¹⁸⁶

Furthermore, even assuming, *arguendo*, that the 2DEG is depleted under high resistive region 15b, the lack of 2DEG under that region would mean that the *entire* 2DEG between the source and the drain of *Uemoto* is removed. And that cannot be the case, as explained with regard to *Beach189* above, because depletion of the 2DEG from source to drain results in a non-functional enhancement-mode transistor, as the 2DEG cannot be reconstituted by application of a gate voltage to turn the device ON.¹⁸⁷

ii. Uemoto's gate electrode is not located above the alleged compensated GaN layer

Uemoto, which Innoscience argues discloses the disputed features of claims 1-3, in fact is akin to the admitted prior art, activated pGaN transistors discussed in Figure 1 of the '294 Patent. As described in *Uemoto*, the third nitride semiconductor layer 15 has a region 15a that is activated with conductive, negatively charged Mg acceptors and holes, and element 15b, which is a resistive p-doped AlGaIn/GaN region.¹⁸⁸ It is this activated region 15a that is below the gate electrode.¹⁸⁹ *Uemoto* reflects the conventional understanding prior to the '294 Patent, that passivation below the gate is unfavorable to the formation of an enhancement-mode transistor.¹⁹⁰ Because it has an activated pGaN layer below the gate, *Uemoto* "has the known problems of low turn on voltage and high gate leakage current."¹⁹¹ *Uemoto* thus describes a device that is substantially similar to the prior art enhancement-mode device shown in Figure 1 of the '294 Patent (with non-compensated

¹⁸⁶ *Id.*

¹⁸⁷ *See supra* Section III.A.2.i.c.

¹⁸⁸ Tr. 959:25-960:23 (Schubert); RX-0073 at ¶¶ [0033], [0048]-[0049], [0066].

¹⁸⁹ Tr. 959:25-960:23 (Schubert); RX-0073 at FIG. 7.

¹⁹⁰ Tr. 102:14-105:16 (Lidow); JX-0014 at 1:55-2:2.

¹⁹¹ Tr. 960:16-19 (Schubert).

GaN below the gate), and thus does not disclose “a compensated GaN layer above the barrier layer,” as recited in claim 1 of the ’294 Patent.¹⁹²

High resistive region 15b of *Uemoto* also cannot correspond to the compensated GaN layer, because the design of *Uemoto* precludes its device from providing both the reduced gate leakage current and reduced gate capacitance that the ’294 Patent’s transistor offers over the prior art.¹⁹³ Even if high resistive region 15b could reduce gate leakage, it still will not impact gate capacitance, because it is not a part of the gate structure. That failure extends to what Dr. Schubert referred to as the “sliver” of region 15b that is shown in Fig. 7 of *Uemoto* to be contacting a very small portion of gate electrode 20 (but not described in *Uemoto*’s specification that way).¹⁹⁴ Instead, it is activated region 15a that is below the gate, and because that region is conductive, the transistor will continue to have the unfavorably high gate capacitance of the prior art devices.¹⁹⁵

Uemoto further does not disclose “a compensated GaN layer,” as recited in claim 1 of the ’294 Patent because the p-doped high resistive layer 15b is not a part of the gate material.¹⁹⁶ As Dr. Schubert explained at the hearing, a POSA would not consider high resistive region 15b to be a part of the gate material because it is not under the gate electrode and is not part of the control region that is used to obtain 2DEG depletion and the normally-OFF characteristics of the *Uemoto* device.¹⁹⁷ Moreover, a POSA cannot simply move the high resistive region 15b of *Uemoto* below the gate electrode without running counter to *Uemoto*’s stated objective of having a control region

¹⁹² *Id.* at 963:5-965:19; 968:1-6.

¹⁹³ *Id.* at 1011:7-15.

¹⁹⁴ *Id.* at 964:22-965:19, 968:1-6.

¹⁹⁵ *See* Tr. 1212:17-1213:21 (Doolittle) (explaining the difference between the capacitance curves for conductive and semi-insulating pGaN); Tr. 968:1-6 (Schubert) (contrasting the conductive nature of region 15a under the gate electrode with the non-conductive, compensated GaN layer of the ’294 Patent).

¹⁹⁶ Tr. 1034:4-11 (Schubert).

¹⁹⁷ *Id.* at 960:20-23, 963:5-964:16; Tr. 931:3-12 (Lebby); RX-0073 ¶ [0038].

below the gate with a lower resistivity.¹⁹⁸ Indeed, *Uemoto*'s operation requires that the conductive, activated region 15a be below the gate electrode, such that increasing its resistivity would reflect impermissible hindsight.¹⁹⁹

Innoscence's position on the teaching of *Uemoto* is also self-contradictory. While it argued at the hearing that *Uemoto* discloses each of the contested features of claim 1, Innoscence, perhaps retrospectively recognizing the weakness of its position, introduces an untimely new argument in its post-hearing brief that the compensated GaN layer is "at least suggested and rendered obvious" by *Uemoto*.²⁰⁰ Innoscence has never before raised an obviousness argument relying on *Uemoto* with respect to the claimed compensated GaN layer and lacks any expert testimony in support of this new, untimely position. This new position should therefore be stricken under Ground Rule 11.2 and due to the prejudice to EPC.²⁰¹

Furthermore, Innoscence's unsubstantiated position is incorrect for at least two reasons. First, it is inconsistent with Innoscence's insistence that *Uemoto* alone discloses all of the elements of claim 1.²⁰² Second, high resistive region 15b does not render the compensated GaN layer obvious because as explained above: (1) it is in a different location; (2) it does not perform the same function of depleting the 2DEG below the gate to create an enhancement-mode device; and (3) moving it below the gate electrode would contravene the *Uemoto* disclosure.

4. Objective indicia of non-obviousness

In asserting that EPC has not met its burden to bring forth objective evidence of non-obviousness for the '294 Patent, Innoscence wholly ignores Dr. Lidow's testimony. Both Dr.

¹⁹⁸ Tr. 960:20-23; 963:5-964:16 (Schubert).

¹⁹⁹ *Id.*

²⁰⁰ RPHIB at 30.

²⁰¹ Order No. 2, Ground Rule 11.2.

²⁰² RPHIB at 50.

Lidow and EPC's expert, Dr. Schubert, tied the claimed transistor to EPC's devices, and Dr. Lidow clearly explained that the '294 Patent contributed to improved characteristics that resulted in smaller, faster, safer devices with better performance and reduced manufacturing costs.²⁰³ The objective indicia detailed by Dr. Lidow included failure by others, industrial praise, and copying by others.²⁰⁴ Taken together, EPC demonstrated significant—and unrebutted—objective indicia of non-obviousness.

B. Validity of the '508 Patent

The '508 Patent, entitled *Enhancement Mode GaN HEMT Device and Method for Fabricating the Same*, names Drs. Lidow and Beach, among others, as inventors. It issued from U.S. Patent Application 12/756,960, filed on April 8, 2010, which further claims priority to U.S. Provisional Patent Application 61/167,777, filed on April 8, 2009.

The '508 Patent is directed to forming an enhancement-mode GaN transistor.²⁰⁵ The process results in a self-aligned gate structure achieved by etching the doped GaN or AlGaN and the doped contact metal material using a single photo mask to pattern the etching during photolithography.²⁰⁶

In a described embodiment, the process to manufacture an enhancement-mode GaN transistor includes serially depositing and/or growing the epitaxial layers. After the formation of the epitaxial structure,²⁰⁷ a layer of gate metal is deposited over the epitaxial structure.²⁰⁸ After the gate metal is formed, the self-aligning processing steps begin including the etching of the gate metal layer and the etching of the p-type GaN gate material. The '508 Patent describes using a

²⁰³ Complainant's Initial Post-Hearing Br. at 117-22.

²⁰⁴ *Id.*

²⁰⁵ JX-0015; Tr. 968:11-16 (Schubert); CDX-0003.27 (citing JX-0015 at Claim 1, FIGS. 3A-3E).

²⁰⁶ JX-0015 at 3:1-6; Tr. 970:3-971:18 (Schubert); CDX-0003.30.

²⁰⁷ JX-0015 at 3:39-40.

²⁰⁸ *Id.*

single photo mask to pattern the structure and etch both the gate metal and the p-type GaN gate layer.²⁰⁹ These etchings occur when both the gate metal and gate contact layers are deposited across the wafer. Embodiments of a self-aligned process are shown below.²¹⁰

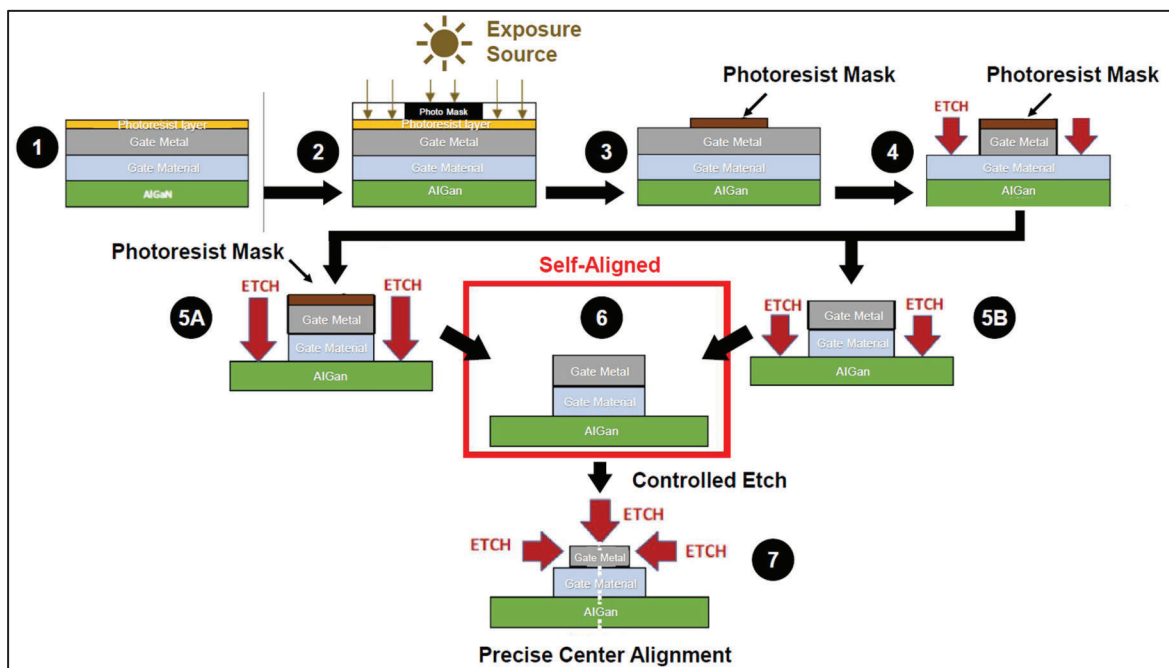


Figure III.B-01²¹¹

After the self-aligned gate metal and gate semiconductor layer have been etched to form the gate structure, a protective dielectric material, for example, silicon nitride, can be deposited.²¹² A two-mask etching process is used to form the ohmic contacts.²¹³ A contact opening photo mask is used to pattern a contact photo resist pattern.²¹⁴ The dielectric material is etched away in the source and drain contact areas for the deposition of the source and drain metal on the barrier layer.²¹⁵ The

²⁰⁹ *Id.* at 3:45-49.

²¹⁰ Tr. 970:3-971:18 (Schubert); CDX-0003.30.

²¹¹ CDX-0003.30 (Annotated)

²¹² JX-0015 at 3:57-61; Tr. 108:12-109:25 (Lidow) (“we tried low pressure silicon nitride to coat the entire device with it and that was good...”).

²¹³ Tr. 968:11-969:4 (Schubert); CDX-0003.27 (citing JX-0015 at Claim 1, FIGS. 3A-3E).

²¹⁴ JX-0015 at 3:57-61.

²¹⁵ *Id.* at 3:58-61.

ohmic contact metal is deposited, including in the openings where the dielectric material was removed.²¹⁶ After the contact metal is deposited, an additional photo mask is used to etch the ohmic contact metal outside the source and drain contact regions.²¹⁷ The final step of the described process is to use rapid thermal annealing (RTA) to form the ohmic contacts to the AlGa_N barrier layer 14.²¹⁸

1. Overview of the Prior Art

Innoscience alleges a sole argument of invalidity for the '508 Patent: U.S. Patent Application Publication 2006/0273347 A1 ("*Hikita*") in combination with U.S. Patent 7,238,560 B2 ("*Sheppard*") and International Patent Application Publication 2005/057624 A2 ("*Beach624*"). Innoscience cites *Sheppard* for teaching a set a transition layers (i.e., step [1a]), *Beach624* for both groups of steps relating to forming the self-aligned gate structure and for forming the Ohmic contacts (i.e., steps [1f]-[1i] and [1n]-[1q]), and *Hikita* for the remaining steps (i.e., steps [1pre], [1b]-[1d], [1j]-[1m], and [1r]). But these three references, even in combination, fail to disclose or suggest by clear and convincing evidence that each limitation of claim 1 of the '508 Patent was obvious to a POSA.

i. Hikita

Hikita describes an enhancement-mode Ga_N transistor, as demonstrated by the presence of a Mg-doped Ga_N portion of a layer between its AlGa_N barrier layer and gate contact.²¹⁹ *Hikita*'s enhancement-mode transistor includes substrate 401, Al_N buffer layer 402, undoped Ga_N layer 403, undoped AlGa_N layer 404, p-type AlGa_N layer 405, and heavily doped p-type Ga_N layer

²¹⁶ *Id.* at 3:62-64.

²¹⁷ *Id.* at 3:64-67.

²¹⁸ *Id.* at 3:67-4:2.

²¹⁹ Tr. 997:10-998:1 (Schubert); CDX-0003.39 (citing RX-0041 ¶ [0011]); Tr. 936:25-937:2 (Lebby) ("If you design a device with p-type material as we've heard in this litigation, it's enhancement-mode.").

406.²²⁰ *Hikita* further describes gate electrode 411, source electrode 409, and drain electrode 410, and a process for forming the same as illustrated in FIGS 8A-8F shown below.²²¹

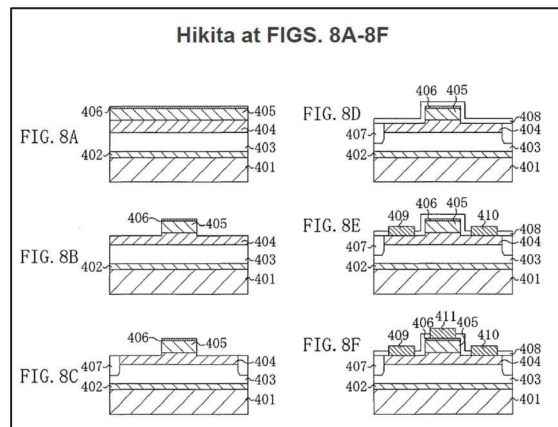


Figure III.B.1.i-01: *Hikita* at FIGS. 8A-8F.²²²

Hikita describes a gate-last process in which, as shown in FIG. 8A, buffer layer 402 is grown, undoped GaN layer 403 follows, undoped AlGaIn layer 404 is subsequently formed, and p-type AlGaIn layer and heavily doped p-type GaN layer 406 are formed.²²³ The gate material 405 is then patterned and etched as shown in FIG. 8B. Then, a silicon nitride layer 408 is deposited as shown in FIG 8D.²²⁴ Source 409 and drain 410 contacts are then formed in the silicon nitride layer.²²⁵ And only after source and drain contacts are formed is the gate contact 411 formed in the silicon nitride layer above the gate material, as shown in FIG. 8F.²²⁶ *Hikita* further describes a single photo mask ohmic contact formation process, a lift up process, but does not disclose or suggest a two photo mask process to make its ohmic contacts.²²⁷ Thus, although *Hikita* does state

²²⁰ RX-0041 ¶ [0048].

²²¹ *Id.* ¶¶ [0048], [0055-61]; Tr. 973:2-13 (Schubert); CDX-0003.34 (citing RX-0041 at FIGS. 8A-8F); RX-0041 ¶¶ [0044], [0056].

²²² CDX-0003.34 (citing RX-0041 at FIGS. 8A-8F).

²²³ Tr. 972:25-973:13 (Schubert); CDX-0003.34 (citing RX-0041 at FIGS. 8A-8F); RX-0041 ¶¶ [0044], [0056].

²²⁴ RX-0041 ¶ [0059].

²²⁵ *Id.* ¶ [0061].

²²⁶ *Id.*

²²⁷ Tr. 973:7-13 (Schubert); CDX-0003.34 (citing RX-0041 at FIGS. 8A-8F).

that the source, drain, and gate contact can be formed before the silicon nitride layer, its source and drain contacts are always formed after the gate material has been *patterned* and *etched* and before the gate metal is deposited on the gate contact and patterned.²²⁸

ii. Beach624

Beach624 describes a unique process of manufacturing a depletion-mode device. The process of *Beach624* begins by depositing a dielectric layer over the epitaxial layers.²²⁹ Openings are then formed in the dielectric and gate source and drain contacts are deposited and formed at the same time.²³⁰ This is done in a coupled fabrication process using a single step of forming resist material 13 over the ohmic material and using this single resist material to simultaneously pattern and form the gate, source, and drain contacts.²³¹ Indeed, the focus of *Beach624* is to simultaneously form the gate, source, and drain contacts.

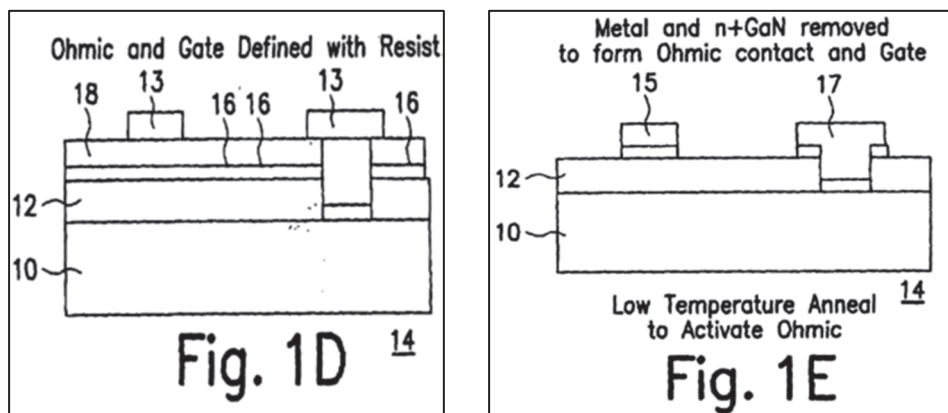


Figure III.B.1.ii-01: *Beach624* at FIGS. 1A-1E.²³²

²²⁸ Tr. 973:2-13 (Schubert); CDX-0003.34 (citing RX-0041 at FIGS. 8A-8F).

²²⁹ Tr. 995:24-996:7 (Schubert); CDX-0003.37.

²³⁰ Tr. 996:8-12 (Schubert); CDX-0003.37.

²³¹ Tr. 973:14-23, 996:8-12 (Schubert); CDX-1003.35 (citing RX-0286 FIGS. 1A-1E); RX-0286 ¶ [0047].

²³² CDX-1003.35 (citing RX-0286 FIGS. 1A-1E).

iii. Sheppard

Sheppard is solely relied upon for allegedly teaching a set of transition layers. Innoscience has not asserted that *Sheppard* cures the deficiencies of *Hikita* regarding any other claim element.

2. **Beach624 does not teach separate steps of applying a gate photo resistant pattern and applying a metal photo resistant pattern**

Innoscience relies on a single process step described in *Beach624* as teaching two independent process steps recited in the '508 Patent. Specifically, Innoscience cites *Beach624*'s deposition of resist material 13 as disclosing both “applying a gate photo resistant pattern” (step [1f]) and “applying a metal photo resistant pattern” (step [1o]).²³³ “Where a claim lists elements separately, the clear implication of the claim language is that those elements are distinct components of the patented invention.” *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1250 (Fed. Cir. 2010). In *Id.*, the Federal Circuit reasoned that where limitations of a hinged arm and spring means connected to the hinged arm were listed as separate elements, prior art in which these structures were not separate would not invalidate the claims. *Id.* at 1254-55. Although the claim at issue in the '508 Patent is a method claim, the logic holds: a single process step of the prior art should not invalidate two individual steps (“applying a gate photo resistant pattern” (step [1f]) and “applying a metal photo resistant pattern” (step [1o])).

As can clearly be seen from the below figure and corresponding text, *Beach624* teaches forming both gate contact 15 and ohmic contact 17 in a single step with a single photo resist pattern 13.²³⁴

²³³ RPHIB at 65-66 (citing RX-0286 ¶¶ [0045], [0047] – [0049]; Tr. 907:23-25 (Lebby)); RPHIB at 70 (citing RX-0286 ¶¶ [0045], [0047] – [0049]).

²³⁴ Tr. 973:14-23, 1007:2-1008:12 (Schubert); CDX-1003C.49-50; RX-0286 ¶ [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17”).

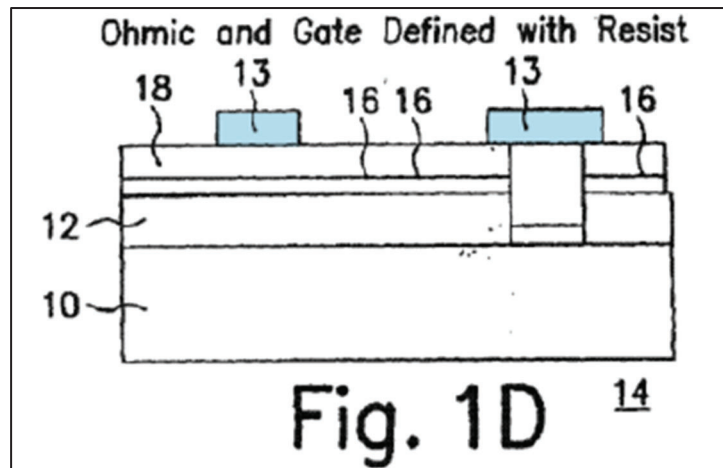


Figure III.B.2-01: *Beach624* at FIG. 1D (Annotated).²³⁵

[0047] Referring now to Figure ID, resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17. After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13.”²³⁶

Contrary to Innoscience’s arguments, element 13 of FIG. 1D of *Beach624* is deposited in a single process step and does not correspond to two discrete structural elements or result from two discrete process steps. The language in paragraph 47 is particularly telling. *Beach624*’s use of the singular word, “pattern,” in conjunction with the described single deposition step, informs a POSA that one, and only one, pattern is deposited in a single step to permit the simultaneous formation of the gate contact 15 and ohmic contact 17. As such, Innoscience cannot claim this single prior art step corresponds to two discrete claim process elements.

Recognizing how strained that position is, Innoscience now attempts to provide expert opinion or explanation that it would be obvious to apply *Beach624*’s two purportedly different photo resist patterns sequentially.²³⁷ This is a new opinion that was never disclosed in contentions, expert reports, or at trial. Even the testimony cited by Innoscience from its own expert does not

²³⁵ CDX-0003.50 (RX-0286 at FIG. 1D).

²³⁶ RX-0286 ¶ [0047] (emphasis added).

²³⁷ RPHIB at 85-86.

support this position.²³⁸ Instead, at that juncture, Innoscience's expert is explaining gate formation can occur after or simultaneous in the claim of the '508 Patent—not the prior art.²³⁹ Innoscience provided no evidence that it would have been obvious to a POSA to apply resist material 13 (which must be applied across the entire wafer) sequentially, rather than in one step. Any reliance on expert testimony to support this argument should therefore be stricken under Ground Rule 9 and due to the prejudice to EPC.²⁴⁰ Moreover, as noted above, this argument lacks supporting expert opinion and should be afforded no weight.

But even if this new argument is considered, it fails. Innoscience itself explained that a POSA would be motivated to eliminate a multi-photoresist pattern sequence in order to simplify the manufacturing process and reduce costs.²⁴¹ Modifying a single photoresist deposition, like the deposition of photo resist pattern 13, to instead require multiple steps in sequence would result in a more complicated and expensive process.²⁴² Innoscience provides no expert testimony in support of its naked allegation that it would be obvious to apply *Beach624*'s two purportedly different photo resist patterns sequentially instead of simultaneously. Therefore, a POSA would not have been motivated to modify *Beach624*'s single resist application to a sequential more complicated process, nor has Innoscience explained how the process would operate.

Finally, a POSA would not have been motivated to combine *Beach624* and *Hikita* to include a sequential application of resist material 13. *Beach624* intended to form the gate, source, and drain at the same time in an efficient single photoresist application step.²⁴³ Modifying

²³⁸ See *id.* (citing Tr. 891:16-24 (Lebby)).

²³⁹ Tr. 891:16-24 (Lebby).

²⁴⁰ Order No. 2, Ground Rule 9; 19 C.F.R. § 210.27(f).

²⁴¹ RPHIB at 69.

²⁴² Tr. 1002:23-1003:14 (Schubert); CDX-0003.44 (*comparing* RX-0041 at Figs. 8A-8F *with* RX-0286 at Figs. 1A-1E).

²⁴³ Tr. 973:14-23 (Schubert); RX-0286 ¶ [0047].

Beach624 to form the gate, source and drain in multiple steps is contrary to the express teachings of *Beach624*. A POSA would not have been motivated to make that modification and render the resultant device inoperable for its intended use.²⁴⁴ *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984) (finding a lack of motivation to modify the prior art because the prior art would have been rendered inoperable for its intended purpose); *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1354 (Fed. Cir. 2001) (explaining that references teach away from the combination if the combination would produce a “seemingly inoperative device” and therefore cannot serve as predicates for a *prima facie* case of obviousness).

As such, Innoscience’s proposed combination of *Hikita* and *Beach624* cannot teach both method steps of “applying a gate photo resistant pattern” and “applying a metal photo resistant pattern” and, consequently, cannot invalidate claim 1 of the ’508 Patent.

3. Innoscience’s expert never provided a step-by-step description of the proposed combination of *Hikita* and *Beach624*

Even through its initial post-hearing brief, Innoscience has still not fully detailed its proposed combination of the *Hikita/Beach624* fabrication process. Innoscience criticizes EPC’s expert Dr. Schubert for improperly understanding the prior art, rather than meeting its burden to clearly explain its hypothetical combination.²⁴⁵ “A party seeking to invalidate a patent on obviousness grounds must demonstrate by clear and convincing evidence that a skilled artisan would have been motivated to combine the teachings of the prior art reference to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *InTouch Techs., Inc. v. VGo Commc’ns., Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014). In *InTouch Techs.*, the Federal Circuit vacated a finding of infringement because the defendant’s

²⁴⁴ Tr. 995:22-997:8 (Schubert); CDX-0003.37-38; Tr. 973:14-23, 1007:2-1008:12 (Schubert); CDX-1003C.49-50.

²⁴⁵ RPHIB at 89-91.

expert opined that the elements of the claim existed in the prior art but failed to explain how to combine the elements:

Dr. Yanco's testimony was nothing more than impermissible hindsight; she opined that all the elements of the claims disparately existed in the prior art, but failed to provide the glue to combine these references. While she opined that the references were like separate pieces of a simple jigsaw puzzle, she did not explain what reason or motivation one of ordinary skill in the art at the time of the invention would have had to place those pieces together.

Id. at 1348-49. Innoscience made general statements concerning motivation to combine types of features, but it failed to tie that motivation to the particular references or explain how the "pieces of the jigsaw" actually even fit together and solely relied upon hindsight of two disparate prior art references.²⁴⁶ This is insufficient for Innoscience to meet its clear and convincing burden.

Dr. Schubert explained his understanding of Dr. Lebby's proposed combination *Beach624* and *Hikita*.²⁴⁷ Although Dr. Schubert's analysis was correct, Innoscience now attempts to obfuscate the issue by transferring the burden to EPC. But it remains Innoscience's burden to explain how the substantially different processes described in *Hikita* and *Beach624* could be combined into a single process to render claim 1 obvious.

Innoscience simply identified different "modules," the equivalent of different claim element groups in the prior art, but did not expressly describe how they could be combined to form steps of a process meeting claim 1.²⁴⁸ In other words, Innoscience identified claim elements in different prior art references, but did not explain a coherent combination of the process steps. Moreover, contrary to Innoscience's claim, it clearly articulates a process that includes performing

²⁴⁶ RPHIB at 65-72, 87-88.

²⁴⁷ Tr. 974:10-975:12, 995:22-997:9 (Schubert); CDX-0003.36-38.

²⁴⁸ Tr. 974:10-975:12 (Schubert); CDX-0003.36; Tr. 910:15-24 (Lebby) ("I take Beach624, the gate formation process, which is shown in figure 1E and put that starting at figure 8A of Hikita. In figure 8A I can put the gate down on top of 406 and I can start the process from there, the gate will be done before the ohmic metals.").

Beach624's simultaneous gate and ohmic material formation in the beginning of *Hikita*'s fabrication process and then subsequently proceeding with *Hikita*'s silicon nitride deposition.²⁴⁹ EPC showed that any reasonable proposed combination would not result in a functioning transistor.²⁵⁰

Although Innoscience claims it clearly explained the process steps and that *Hikita* describes an embodiment where the doped GaN layer is etched to form the gate structure before depositing a silicon nitride layer, Innoscience actually only selectively quoted the full sentence of *Hikita*.²⁵¹ *Hikita* states the gate, source, and drain contacts can be deposited before the silicon nitride layer, and never splits those steps—which Innoscience failed to address.²⁵² In particular, Innoscience provides no explanation of how *Beach624*'s simultaneous gate and ohmic contact process would integrate into such a post silicon nitride deposition process.²⁵³ Claim 1 requires, in part, “etching the dielectric layer to open the drain and source contact areas,” but Innoscience failed to address how any such post-silicon nitride deposition process would still meet this claimed process step.

Innoscience's hindsight cobbling together of elements from multiple prior art sources without fully explaining the hypothetical process itself, or why a POSA would be motivated to perform the hypothetical process, is insufficient to meet its burden. Nor has Innoscience explained how such a process would be operable. In contrast, EPC clearly explained why Innoscience's combination would not have resulted in an operable device.²⁵⁴ As the hypothetical method would

²⁴⁹ Tr. 910:15-24 (Lebby).

²⁵⁰ Tr. 995:22-997:8 (Schubert); CDX-0003.37-38.

²⁵¹ Tr. 910:3-24 (Lebby).

²⁵² RX-0041 ¶ [0061] (“The source electrode 409, the drain electrode 410 and the gate electrode 411 may be formed before formation of the SiN film 408”).

²⁵³ Tr. 999:4-21 (Schubert); CDX-0003.41.

²⁵⁴ Tr. 974:10-975:12, 995:22-997:8 (Schubert); CDX-0003.36-38.

result in an inoperable device, a POSA would not have been motivated to make the combination as proposed by Innoscience with any expectation of success.

4. Innoscience failed to establish a motivation to replace Hikita's gate last process with Beach624's simultaneous process

Innoscience's failure to clearly define the hypothetical combination is further demonstrated by its failure to identify a motivation to replace *Hikita*'s gate-last process with *Beach624*'s simultaneous gate and ohmic contact formation. *Hikita* only describes a gate-last process, including a series of steps starting with Figure 8A and ending at Figure 8F. Innoscience contends that a POSA can form *Hikita*'s epitaxial process as shown in Figure 8A, and then perform *Beach624*'s process illustrated in its Figure 1E to form the gate.²⁵⁵

Innoscience, however, failed to provide a motivation to combine with an expectation of success in abandoning *Hikita*'s distinctly different gate formation process and substituting *Beach624*'s gate formation process. As shown below, a substitution of the process step in FIG. 1E of *Beach624* following FIG. 8A of *Hikita* would result in simultaneous etching of gate and ohmic contact without any process to open a dielectric layer as none has been laid down, as required by claim step [11] "etching the dielectric layer to open the drain and source contact area."²⁵⁶

²⁵⁵ Tr. 910:15-24 (Lebby).

²⁵⁶ *Id.* ("I take Beach624, the gate formation process, which is shown in figure 1E and put that starting at figure 8A of Hikita. In figure 8A I can put the gate down on top of 406 and I can start the process from there, the gate will be done before the ohmic metals.").

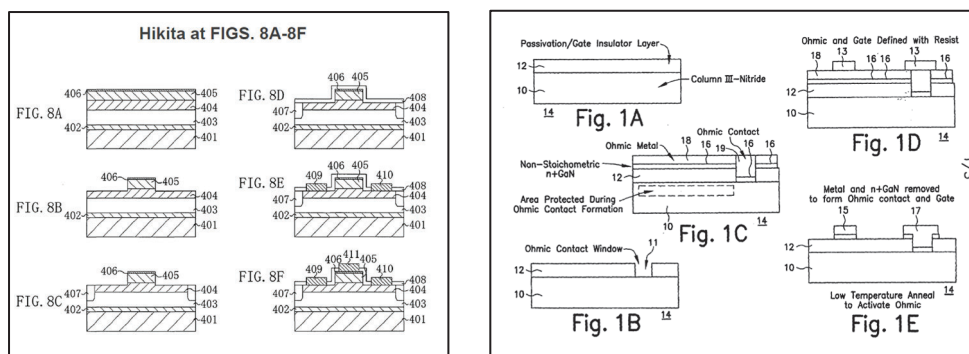


Figure III.B.4-01: *Hikita* at FIGS. 8A-8F; *Beach624* at FIGS. 1A-1E.²⁵⁷

Moreover, simultaneous formation of source, gate, and drain contacts is not common in the field and results in additional restrictions on the process.²⁵⁸ If the gate metal is deposited on the pGaN layer of *Hikita*, followed by the process of *Beach624* simultaneously forming the gate and ohmic contacts, it would result in the ohmic contacts being formed on the pGaN material rather than on the AlGa_N barrier layer.²⁵⁹ This would result in an inoperable device.²⁶⁰ Furthermore, the evidence shows that, although *Beach624* describes simultaneous gate and ohmic contact formation, in commercial fabrication this simultaneous process is not done.²⁶¹ The source and drain contacts have different functions than the gate and also have different structures and materials in their respective local vicinity, making fabrication difficult.²⁶² This makes it less desirable to modify *Hikita*'s single gate process with a simultaneous gate and ohmic contact process.²⁶³

Innoscience argues that a POSA would combine *Hikita* with *Beach624* because self-aligned gate etching processes were known in the art and conventional.²⁶⁴ But Innoscience never articulates why or how a POSA would be motivated to: (1) change the gate last process of *Hikita*

²⁵⁷ RX-0041 (*Hikita*); RX-0286 (*Beach624*).

²⁵⁸ Tr. 1005:11-1006:24 (Schubert); CDX-0003.47-48.

²⁵⁹ *Id.*

²⁶⁰ Tr. 974:10-975:12, 995:22-997:8 (Schubert); CDX-0003.36-38.

²⁶¹ *Id.*

²⁶² *Id.*

²⁶³ *Id.*

²⁶⁴ Tr. 908:2-19, 909:10-23 (Lebby).

to a simultaneous process, (2) deposit a gate contact metal on the pGaN material, then (3) apply resist material 13 to pattern and etch the pGaN and gate metal, and (4) subsequently deposit a silicon nitride layer. There is simply no motivation to combine or expectation of success to drastically modify the process of *Hikita* in view of *Beach624*.

As discussed above, *Hikita* describes an embodiment where the gate, source and drain contacts are deposited before the formation of the dielectric layer.²⁶⁵ Innoscience never explained how, based upon that disclosure, a POSA would modify *Hikita* in view of *Beach624* as proposed.²⁶⁶ Indeed, Innoscience selectively quotes *Hikita*, which actually states in full that “[t]he source electrode 409, the drain electrode 410 *and* the gate electrode 411 may be formed before formation of the SiN film 408.”²⁶⁷ (emphasis added). Innoscience never explains how, in the proposed modification, the step of “etching the dielectric layer to open the drain and source contact area” would be performed, as Innoscience’s identified dielectric, the SiN film, would not be deposited prior to deposition of source and gate. Thus, not only does Innoscience fail to explain how the selected quote supports its hypothetical modified process, the full quote in *Hikita* in fact cuts against Innoscience’s proposed modification. This is yet another reason a POSA would not have combined *Hikita* and *Beach624* as proposed by Innoscience—or if done, would not achieve the claimed process.

²⁶⁵ RPHIB at 70 (citing RX-0041 ¶ 0061).

²⁶⁶ *Id.*

²⁶⁷ RX-0041 ¶ [0061].

5. **Innocience never established a motivation to replace Hikita’s single mask source and drain formation with Beach624’s two photo mask process**

Hikita describes a simpler single mask source and drain formation process applying a liftoff process.²⁶⁸ Neither *Hikita* nor *Beach624* teach away from such a process.²⁶⁹ Indeed, it is a faster and more efficient process than using a two photo mask source and drain formation process.²⁷⁰ Dr. Schubert explained an exemplary single photo mask process to form source and drain formation, as illustrated below.²⁷¹

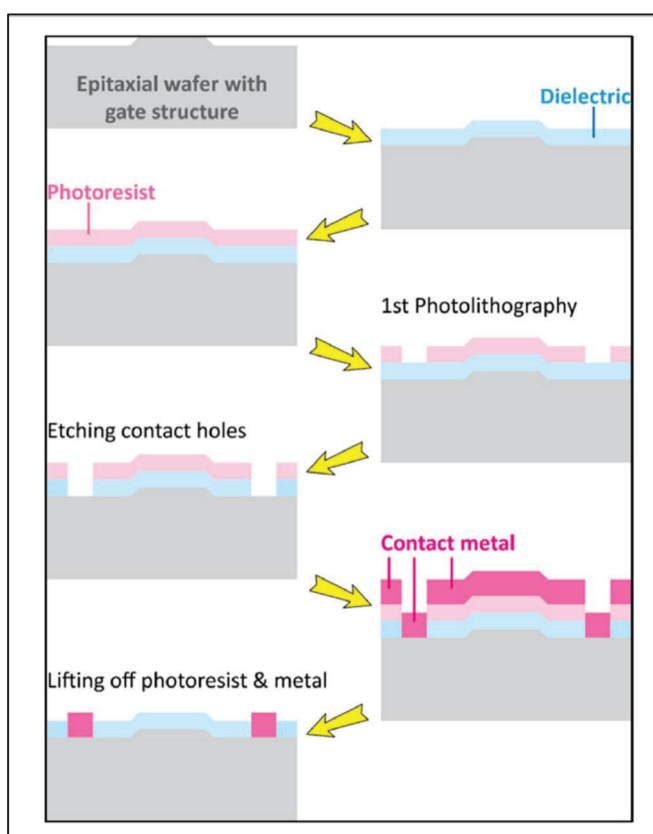


Figure III.B.5-01: CDX-0003.31.

²⁶⁸ Tr. 1000:15-1003:17 (Schubert); CDX-0003.42-43 (citing RX-0041 ¶¶ [0059]-[0060]; RX-0286 ¶¶ [0042], [0047]).

²⁶⁹ *Id.*

²⁷⁰ Tr. 1002:11-1003:14 (Schubert); CDX-0003.43-44 (citing RX-0286 ¶¶ [0042], [0047]).

²⁷¹ Tr. 971:21-972:10 (Schubert); CDX-0003.31.

In contrast, *Beach624* describes a two-mask process, which simultaneously creates source and drain contacts using photoresist material 13.²⁷² As can be seen in FIGS. 1A through 1E of *Beach624*, in a first step, an ohmic contact window is opened in the passivation/gate insulator layer. Subsequently, the simultaneous formation of the gates using resist material 13 occurs.²⁷³

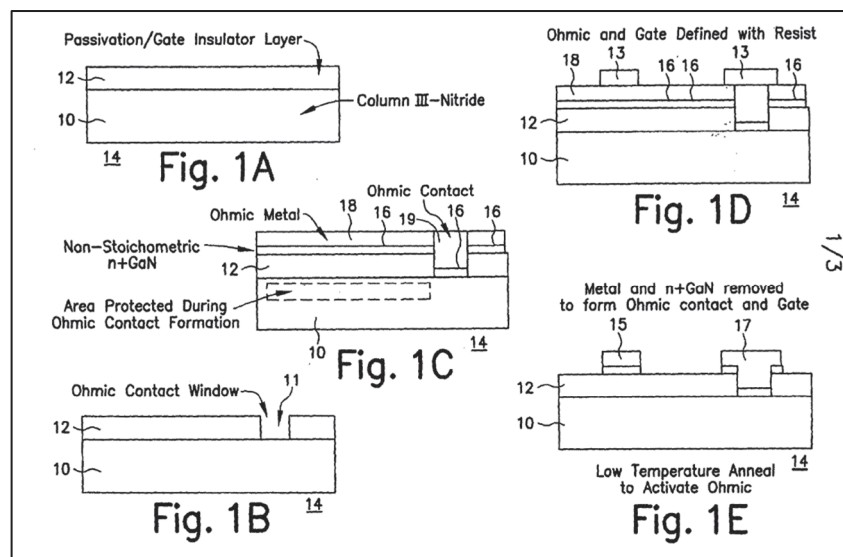


Figure III.B.5-02: *Beach624* at FIGS. 1A-1E.²⁷⁴

Dr. Schubert also detailed an exemplary two photo mask process to form source and drain formation, as illustrated below.²⁷⁵

²⁷² Tr. 1001:19-1002:22 (Schubert); CDX-1003.43.

²⁷³ *Id.*

²⁷⁴ RX-0286.

²⁷⁵ Tr. 971:21-972:10 (Schubert); CDX-0003.32.

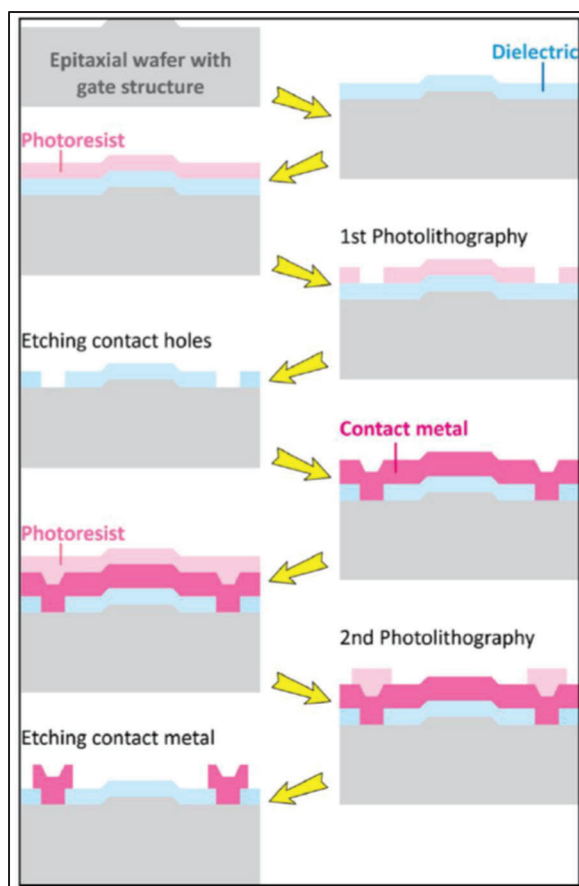


Figure III.B.5-03: CDX-0003.32.

A single mask process is materially different than a two-mask process. Although its burden, Innoscience failed to provide any specific motivation for a POSA to substitute the faster and more efficient process of *Hikita* with *Beach624*'s two photo mask process. Indeed, it is contrary to Innoscience's own position that a POSA would modify a process to simplify manufacturing process and save cost.²⁷⁶

Moreover, in contrast to its statement just pages before contending that motivation supported including the self-aligned gate process of *Beach624* into *Hikita* (steps [1e]-[1i]), Innoscience here generically contends that a more difficult and expensive process would be an

²⁷⁶ RPHIB at 69.

obvious substitution when favoring performance over simplicity.²⁷⁷ However, there is no motivation to give up a well-known type of process using a single photo mask for manufacturing the source and drain for a more complicated, less advantageous process.²⁷⁸ In addition, Innoscience fails to explain how this specific combination would result in improved performance, especially given it never details the actual proposed combination.

6. No motivation to combine teachings from Hikita’s enhancement-mode device process with Beach624’s depletion-mode device process

There is no dispute that *Hikita* is an enhancement-mode transistor as it includes pGaN under that gate contact that would deplete the 2DEG.²⁷⁹ Innoscience provides no evidence from its experts that *Beach624* is not limited to depletion-mode devices,²⁸⁰ even though depletion-mode devices are so unsimilar to enhancement-mode devices in structure, formation processes, and function that a POSA would not seek to combine the teachings.²⁸¹

Instead, Innoscience attempts to rely on out of context testimony to infer *Beach624* can operate either as an enhancement-mode or depletion-mode device.²⁸² However, the only discussion of enhancement-mode devices in *Beach624* is the general background section of the patent, which is inapplicable to Innoscience’s proposed combination or any particular embodiments or teachings of the described invention.²⁸³ Even Innoscience’s cross-examination of Dr. Schubert on this topic related solely to the background of the state of the art and not to the

²⁷⁷ Compare RPHIB at 69 with *id.* at 71.

²⁷⁸ Tr. 1002:23-1003:17 (Schubert); CDX-1003C.44 (citing RX-0041, RX-0286).

²⁷⁹ Tr. 997:10-998:1 (Schubert); CDX-0003.39 (citing RX-0041 ¶ [0011]); Tr. 936:17-937:2 (Lebby).

²⁸⁰ Tr. 934:5-19 (Lebby) (discussing RX-0286 ¶ [0039]); Tr. 998:3-10, 1024:20-23 (Schubert); CDX-0003.40 (citing RX-0286 ¶ [0039] (“nominally on”)).

²⁸¹ Tr. 999:3-1000:10 (Schubert); CDX-0003.41 (*comparing* RX-0041, at FIG. 4 with RX-0286, at FIG. 1E).

²⁸² RPHIB at 89.

²⁸³ RX-0286 ¶¶ [0004], [0008], [0012].

embodiments relied upon by Innoscience for its hypothetical prior art process.²⁸⁴ Innoscience simply mischaracterized *Beach624* as framing the intent of the invention, rather than discussing the state of the art.²⁸⁵ Innoscience never identified any part of *Beach624*'s intended transistor or process of manufacture that includes pGaN (or other enhancement-mode generating material) between the gate contact and barrier layer that would actually result in an enhancement-mode device.

Enhancement-mode devices such as *Hikita* have significant incompatibilities with depletion-mode devices such as *Beach624*; most notably, different structures and, thereby, different formation processes.²⁸⁶ Hence, a POSA would not have been motivated to combine the teachings of *Hikita* and *Beach624* to obtain an operable enhancement-mode device, as required by *Hikita*.²⁸⁷

7. Objective indicia of non-obviousness

In asserting that EPC has not met its burden to bring forth objective evidence of non-obviousness for the '508 Patent, Innoscience wholly ignores Dr. Lidow's testimony. Dr. Lidow, Dr. Beach, and EPC's expert, Dr. Schubert, tied the claimed process to EPC's process, and Dr. Lidow clearly explained that the '508 Patent contributed to improved characteristics including smaller, faster, safer devices with better performance and reduced manufacturing costs.²⁸⁸ The objective indicia detailed by Dr. Lidow included failure by others, industrial praise, and copying

²⁸⁴ Tr. 1025:25-1026:24 (Schubert); RX-0286 ¶¶ [0004], [0008], [0012].

²⁸⁵ *Id.*

²⁸⁶ Tr. 999:3-1000:10 (Schubert); CDX-0003.41 (*comparing* RX-0041, at FIG. 4 *with* RX-0286, at FIG. 1E).

²⁸⁷ *Id.*

²⁸⁸ EPC Post-Hearing Initial Br. 117-22.

by others.²⁸⁹ Taken together, EPC’s actual evidence of non-obviousness rebuts Innoscience’s theories of obviousness.

C. The PTAB’s recent institution decisions should have no persuasive value in this investigation

On March 20, 2024, the Patent Trial and Appeal Board (“PTAB”) granted institution on two petitions for *inter partes* review (“IPR”) filed by Innoscience challenging each of the claims in the ’294 and ’508 Patents (IPR2023-01381 and IPR2023-01383, respectively). Those institution decisions should not be assigned any persuasive value to the issues that must be resolved in this investigation for several reasons. First, the decisions are not final and “non-final IPR proceedings have no bearing on Commission investigations.” *Certain Magnetic Data Storage Tapes & Cartridges Containing the Same*, Inv. No. 337-TA-1012, Comm’n Op., at n. 26 (Apr. 2, 2018).

Second, the institution decisions are based on different burdens of proof than present in this investigation. *See Certain Audio Processing Hardware, Software, & Prod. Containing the Same*, Inv. No. 337-TA-1026, Init. Det. at 64-66 (Oct. 26, 2017) (“*Audio Processing Hardware*”) (noting different burdens of proof). There is a significant difference between a petitioner’s burden to establish a “reasonable likelihood of success” at institution, and actually proving invalidity by a “preponderance of the evidence” at a PTAB trial. *See id.* (citing *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016)); 37 C.F.R. § 42.108(c); 35 U.S.C. § 316(e). The difference between the “reasonable likelihood of success” standard at the PTAB’s institution stage and the “clear and convincing” standard used in ITC investigations is even greater.

Third, the institution decisions are based on a considerably less complete and different record than is present in this investigation. *See Audio Processing Hardware* at 65-66 (“The PTAB’s finding that Apple has a reasonable likelihood of success is a preliminary decision that

²⁸⁹ *Id.*

was made without the benefit of a full record.”) (internal quotations omitted). As is common for patentees, prior to institution, EPC did not submit any expert declarations or provide any arguments regarding the dependent claims of the ’294 and ’508 Patents in its preliminary responses, respectively attached hereto as Exhibit A and Exhibit B.²⁹⁰

Even as to the independent claims of the ’294 and ’508 Patents, EPC did not present the full array of arguments that it has presented in this investigation. Indeed, the PTAB acknowledged the need for a full record before a final decision on the merits can be made.²⁹¹ Accordingly, the institution decisions are based on only a subset of the record available during this investigation and should have no persuasive value.

IV. CONCLUSION

For the foregoing reasons, Innoscience has failed to demonstrate by clear and convincing evidence that any of claims 1-3 of the ’294 Patent and claim 1 of the ’508 Patent are invalid.

* * *

GROUND RULE 1.6 CERTIFICATION

I hereby certify that this brief contains 14,337 words, counted according to the method described in G.R. 1.6.

²⁹⁰ *Innoscience (Zhuhai) Technology Co., Ltd. v. Efficient Power Conversion Corp.*, IPR 2023-01381, Paper 7 (P.T.A.B. Dec. 21, 2023); *Innoscience (Zhuhai) Technology Co., Ltd. v. Efficient Power Conversion Corp.*, IPR 2023-01383, Paper 7 (P.T.A.B. Dec. 21, 2023).

²⁹¹ *Innoscience (Zhuhai) Technology Co., Ltd. v. Efficient Power Conversion Corp.*, IPR 2023-01381, Paper 11, pp. 28-29 (P.T.A.B. Mar. 20, 2024) (“we determine that Patent Owner’s arguments...raise, at most, a material issue of fact that is best resolved on a complete trial record.”); *Innoscience (Zhuhai) Technology Co., Ltd. v. Efficient Power Conversion Corp.*, IPR 2023-01383, Paper 11, p. 35 (P.T.A.B. Mar. 20, 2024) (“Patent Owner’s arguments, which are similar to those set forth with respect to ground 1, raise issues best resolved on a full record.”).

Respectfully submitted,

Dated: March 29, 2024

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Exhibit A

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01381
U.S. Patent No. 8,350,294

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	Jorg Neugebauer et al., “Role of Hydrogen Complexes in Doping of GaN,” Material Research Society Symposium Proceedings, Vol. 423 (1996), pp. 619-24 (“Neugebauer-MRS1”)
2002	Jorg Neugebauer et al., “Theory of Point Defects and Complexes in GaN,” Material Research Society Symposium Proceedings, Vol. 395 (1996), pp. 645-56 (“Neugebauer-MRS2”)
2003	EPC’s Responsive Claim Construction Brief: Inv. No. 337-TA-1366, dated October 6, 2023
2004	IEEE Dictionary definition for “compensated”
2005	U.S. Patent No. 6,498,111 (“the ‘111 patent”)
2006	Translation of Innoscience’s Invalidation Request to the Chinese Patent Office for the Chinese Counterpart to the ‘294 Patent

I. INTRODUCTION

In accordance with 37 C.F.R. § 42.107, Patent Owner Efficient Power Conversion Corporation (“EPC” or “Patent Owner”) submits this preliminary response to the Petition (the “Petition” or “Pet.”) filed by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (“Petitioner”) for *Inter Partes* Review of claims 1-12 of U.S. Patent No. 8,350,294 (the “’294 patent”). Patent Owner respectfully requests that the Board deny the Petition for at least the reasons set forth below.

The ‘294 patent relates to a compensated gate MISFET (title). Claim 1 specifically recites “a compensated GaN layer” beneath the gate contact. As explained below, the compensated GaN layer in the gate allows the claimed transistor of the ‘294 patent to operate in a normally OFF (enhancement) mode, while also rendering the gate semi-insulating, thereby reducing undesirable gate leakage.

Compellingly, none of the prior art relied upon in the Petition even mentions the word “compensated” or remotely suggests a transistor with a compensated gate. This is because the compensated gate invention of the ‘294 patent, which achieves two technical effects having opposite requirements for electrical conductivity, was entirely unexpected and went in a direction completely contrary to conventional wisdom at the time of the invention.

Accordingly, for the reasons explained below, Petitioner has not established that there is a reasonable likelihood that at least one of the challenged claims of the ‘294 patent is unpatentable, and the Petition should be denied.

II. BACKGROUND

A. The ‘294 Patent

The ‘294 patent describes and claims a GaN (Gallium Nitride) MISFET (Metal Insulator Semiconductor Field Effect Transistor). GaN FETs are known for their ability to carry greater current and withstand higher voltages than their silicon counterparts. ‘294 patent at 1:21-24.

GaN transistor devices may be categorized into two different categories: (1) depletion-mode FETs and (2) enhancement-mode FETs. *See* ‘294 patent at 1:42-54. *See id.* Depletion-mode FETs maintain an “ON” state at zero gate-source voltage (normally ON), while enhancement mode FETs maintain an “OFF” state at zero gate source voltage (normally OFF). *See id.* Depletion-mode FETs deplete the 2DEG located near the junction of two layers having different band gaps. *See id.* In the depletion-mode FETs, an electron channel that exists at zero gate voltage is depleted by applying a negative gate voltage, thereby turning the FET OFF. *See id.* Conversely, enhancement-mode FETs have no electron channel at zero gate voltage, but an electron channel can be induced by applying a positive gate voltage, thereby turning the FET ON. *See id.*

The structure of a conventional GaN FET generally includes a substrate, a transition layer or layers (including a nucleation layer) that transitions the crystal growth from the substrate to the III-N epitaxial layers (e.g., AlGaN), a III-N buffer layer (e.g., GaN), a III-N barrier layer (e.g., AlGaN), and an optional p-type gate semiconductor material (e.g., GaN). *See* '294 patent at 1:55-2:2. A FET further includes three metal contacts: source, gate, and drain. *See id.*

As shown in Fig.1 of the '294 patent, an enhancement-mode transistor in the prior art has a conductive p-type GaN gate semiconductor. '294 patent at 1:55-2:2. When the p-type doping concentration in the GaN gate semiconductor (e.g., doping with Mg) is sufficiently high and the layer is sufficiently thick, the acceptors in the gate layer accept electrons, specifically electrons of the 2DEG, thereby depleting the 2DEG and interrupting the electron channel formed between source and drain. *Id.* at 1:42-2:2.

In the enhancement mode embodiment of Figs. 2-9, the '294 patent discloses a GaN transistor in which “a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the gate contact 37.” *Id.* at 3:8-9. The '294 patent explains that the compensated GaN gate material “leads to low gate leakage during device operation,” (*id.* at 3:18-19) and “reduces the gate capacitance of the device.” *Id.* at 3:20-21. The '294 patent further notes that “the high doping level of the compensated layer 38 leads to enhancement mode devices.” *Id.* at 3:16-17.

The '294 patent identifies several improvements achieved by its invention over preexisting transistors, including that “(1) the capacitance from gate to channel layer when the device is on is lower than in the prior art; (2) the gate bias can be driven much more positive without significant current through the gate...; and (3) hole injection from the gate into the channel layer is dramatically reduced relative to the prior art.” *Id.* at 3:22-29.

The compensated GaN layer of the '294 patent achieves two opposing effects related to electrical conductivity requirements. First, as the p-type GaN layer is grown, the Mg acceptors accept electrons from the 2DEG, thereby depleting the 2DEG and creating a normally-OFF (enhancement-mode) transistor. *See id.* at 3:10-17. Second, during the growth process, the remaining Mg acceptors are passivated by hydrogen, so that the p-type conductivity in the p-doped GaN is substantially reduced, and the p-doped GaN is in fact semi-insulating. *See id.* at 3:15-21, 43-52. As a result, the undesirable gate bulk leakage current through the bulk (not surface) of the p-doped GaN becomes small. *See id.* This is in accordance with the teaching of the '294 patent: “the compensated semiconductor layer 38 is a highly compensated semi-insulating material” '294 patent at 3:47-48.

These two opposite effects were entirely unexpected according to the conventional wisdom. Based on the teachings of the prior art technical literature, a

POSA (person of skill in the art) would have concluded that passivated p-doped GaN cannot be used to deplete the 2DEG and cannot create enhancement transistors. Ex. 1018; Ex. 2001; Ex. 2002. The prior art at the time of the '294 patent disclosed that passivated Mg-H complexes are neutral. Being neutral means that there is no electrical effect and a POSA would thus not have found passivation of p-doped GaN to be useful in the design of enhancement-mode transistors. The invention of the '294 patent fundamentally altered this thinking.

B. Grounds of Challenge

The petitioner challenges the patentability of claims 1-12 of the '294 patent on three grounds:

Ground 1: Claims 1-12 are challenged as being obvious over Smith, either alone (Ground 1A), in view of Kigami (Ground 1B), or in view of Uemoto (Ground 1C).

Ground 2: Claims 1-12 are challenged as being obvious over Uemoto in view of Smith.

III. CLAIM CONSTRUCTION

Petitioner correctly sets forth Petitioner's proposed claim construction from a related matter but misstates Patent Owner's construction, which was modified during responsive briefing of the related matter. Ex. 2003 at 6. Patent Owner proposes that the term "a compensated GaN layer" in claim 1 should be construed

as “a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).”

Patent Owner’s construction applies the plain meaning to a POSA of “GaN layer” and “compensated” consistent with the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005). Petitioner’s incorrect construction - “a doped GaN layer formed with a step to passivate its impurities” - fails to recognize that a POSA would understand the claimed “GaN layer” to be a GaN *gate* material. Moreover, Petitioner improperly seeks to have the limitation construed as a product-by-process limitation, contending that “compensated” refers to a process. As discussed below, however, a POSA would understand the term “compensated” in the context of the claim to be referring to and connoting a specific structure and electrical characteristics in the claimed “GaN layer,” not a process to create a GaN layer.

But regardless of whether Petitioner’s or Patent Owner’s claim construction is applied, the result is the same. The prior art relied upon by Petitioner simply does not disclose or suggest a transistor with a “compensated GaN layer”.

A. “GaN Layer” Refers to GaN Gate Material

A POSA would understand the plain meaning of the term “compensated GaN layer” in view of both the claim and the specification to be referring to a

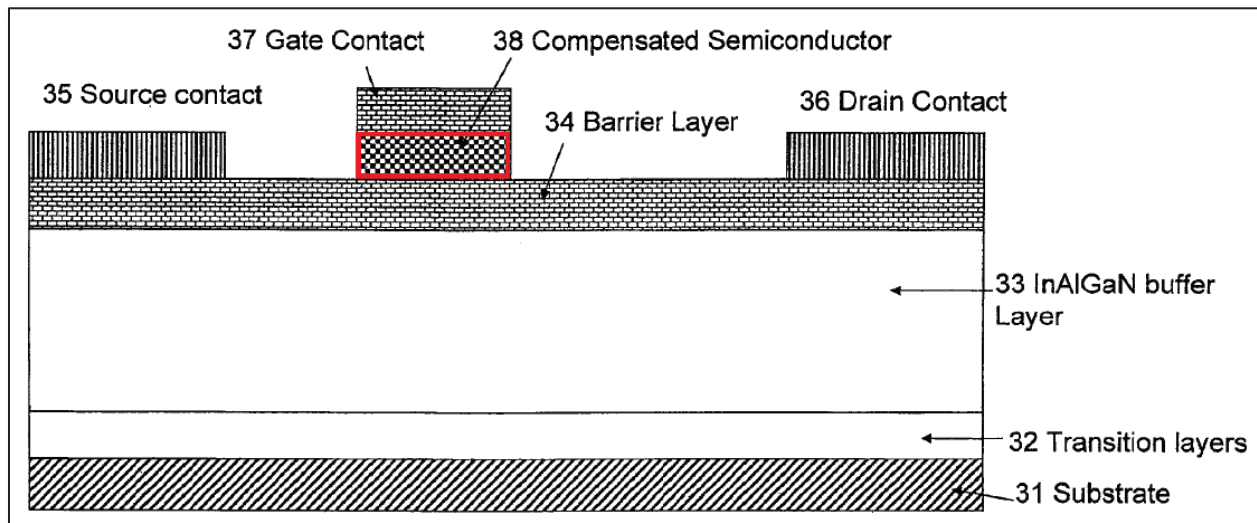
“compensated GaN gate material.” No claim term should be construed in a vacuum, out of context with the other words in a claim. *Phillips*, 415 F.3d at 1314

Claim 1 of the '294 patent describes a transistor where the “compensated GaN layer” is formed “above the barrier layer” and that “a gate contact” is formed “above the compensated GaN layer.” A POSA would understand from the placement of the “compensated GaN layer” between the barrier and the gate contact that the “GaN layer” is a GaN gate material.

The POSA’s interpretation and understanding of this fundamental claim term based on the claim language itself is confirmed by the specification. “[T]he specification is always highly relevant to the claim construction analysis . . . [and] it is the single best guide to the meaning of a disputed term.” *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Here, the entirety of the specification refers solely to a compensated GaN gate material. The '294 patent is titled “Compensated **Gate** MISFET and Method for Fabricating Same.” The specification details the problems with prior art GaN transistors having unfavorable **gate** leakage (*see* '294 patent at 1:55-2:6) and identifies a solution to that problem by creating a compensated **gate** “with low **gate** leakage.” *Id.* at 2:13-14 (emphasis added).

The figures and Summary of Invention further confirm the POSA’s understanding of the meaning of “compensated GaN layer” based on the claim

itself. Indeed, in describing Figure 2, the specification explains that “a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the **gate** contact 37.” *Id.* at 3:7-9 (emphasis added). Figure 2 (excerpted below with the compensated GaN layer annotated in red) has the same structure as recited in claim 1.



A POSA would understand that the layer between the gate contact and the barrier layer - in Figure 2 just as in claim 1 - refers to a GaN gate material. Indeed, the Summary of Invention explains that the claimed inventions are directed to using a material “below the gate contact and above the barrier layer” to “reduce[]” “gate leakage.” *Id.* at 2:14-16; *see also id.* at 3:18-21 (“using a compensated semiconductor layer **38** leads to low **gate** leakage during device operation”) (emphasis added). A POSA would understand that it is the gate material between these layers that contributes to reducing gate leakage, not some other type of GaN

layer. Moreover, the specification provides a method of making the device depicted in Figure 2 (a transistor) and recites the step of “etch[ing] away the compensated semiconductor layer 38, except the portion beneath the gate contact layer 37.” *See id.* at 3:35-38. A POSA reading the claim in light of the specification would have understood the ’294 patent to be describing the manufacturing of a gate stack, where the gate material is beneath the gate contact, and serves the purpose of turning the transistor on or off.

In short, the intrinsic evidence confirms that a POSA would have understood the term “compensated GaN layer” as used in claim 1 to be referring to a compensated GaN gate material, which is the only structure described in the intrinsic evidence as providing the advantages to the claimed transistor over the prior art and which the applicant identified as being at the heart of the claimed inventions.

B. Compensated Describes a Semiconductor with Modified Electrical Characteristics

A POSA would have understood the term “compensated” to have its plain and ordinary meaning in the art. The IEEE dictionary defines “compensated semiconductor” as “[a] semiconductor in which one type of impurity or imperfection (for example, donor) partially cancels the electric effects of the other type of impurity or imperfection (for example, acceptor).” Ex. 2004. Patent Owner’s construction is consistent with that definition.

The description of “compensated” in the specification of the ’294 patent is consistent with the plain and ordinary meaning of “compensated.” For example, the specification explains that the compensated GaN gate material includes a p-type impurity (e.g., Mg, Zn, Be, Cd, or Ca) that imparts an electric effect (i.e., conductivity), and a second impurity, e.g., hydrogen, that partially cancels the electric effect of the p-type impurity by rendering it semi-insulating. ’294 patent at 3:10-13, 3:43-45. The specification explains further that by having the electrical effect of the p-type impurity cancelled out by another impurity, the p-type gate material is differentiated from the prior art by having modified electrical characteristics—specifically, by being more resistive than the conductive structures found in the prior art. *See id.* at 3:46-49 (“the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material.”). A more resistive p-type GaN gate material has improved functional characteristics compared to the prior art, including “low gate leakage during device operation,” *id.* at 3:16-19, reduced gate capacitance, and the ability to act as an enhancement mode device (where the transistor is activated only when a positive voltage is applied to the gate contact). Indeed, nowhere does the ’294 patent refer to a compensated GaN material anywhere other than in connection with the compensated GaN gate. In fact, a POSA reading the ’294 patent – beginning with its title – would have

understood the compensated GaN as part of the gate structure to be the novel feature that distinguished the claimed transistor from the prior art by reducing gate leakage.

Because the term “compensated” has a plain meaning in the art and because the intrinsic evidence describes a “compensated GaN layer” consistent with the plain meaning of the term, Patent Owner’s plain-meaning construction should be adopted.

C. Petitioner’s Construction Should be Rejected

Petitioner’s construction of “compensated GaN layer” as “a doped GaN layer formed with a step to passivate its impurities” is incorrect for several reasons.

First, Petitioner’s construction does not apply the plain and ordinary meaning of “compensated GaN layer” to a POSA as “compensated **GaN gate material**.” As discussed above, the claimed structure is not referring to any GaN layer, but rather a gate material. Thus, Petitioner’s non-construction renders the term impermissibly broader than its plain meaning in view of the intrinsic evidence.

Second, Petitioner’s failure to construe GaN layer consistent with the intrinsic evidence by limiting the GaN layer to the gate material would encompass transistor designs in which the compensated GaN layer does not serve as gate semiconductor material and does not reduce the gate leakage current, as taught in

the '294 patent. For example, a transistor with a compensated GaN layer that is separate from the gate structure and in contact with the source and the drain would fall under Petitioner's expansive construction. In such a transistor, the gate structure would consist only of the metal, and as a result, the compensated GaN layer would not prevent gate leakage, as taught by the '294 patent. Petitioner's reading of the claim term in isolation is therefore incorrect.

But even if there was an equal choice between Petitioner's broad construction and Patent Owner's narrower construction - which there is not for the reasons discussed above - the proper choice would be the narrower construction proposed by EPC. *See Takeda Pharm. Co. v. Zydus Pharms. USA, Inc.*, 743 F.3d 1359, 1365 (Fed. Cir. 2014) ("We long ago established that '[w]here there is an equal choice between a broader and a narrower meaning of a claim, and there is an enabling disclosure that indicates that the applicant is at least entitled to a claim having the narrower meaning, we consider the notice function of the claim to be best served by adopting the narrower meaning.'") (quoting *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996)).

Third, Petitioner's proposed construction improperly limits the scope of the claim to a single type of compensation – i.e., passivation. Petitioner's proposed construction is incorrect, because it improperly limits the term "compensated"

based on the specification's reference to passivation as the "critical step" in achieving the claim "compensated GaN layer."

Fourth, "compensated GaN layer" is not a product-by-process limitation. Indeed, nothing in the claim defines the "compensated GaN layer" in terms of the processes used to compensate. The purpose of the product-by-process "doctrine is to prevent foreclosing inventors 'from the benefits of the patent system simply because a product is difficult to describe in words, or its structure is insufficiently understood.'" *In re Biogen* 335 F. Supp. 3d 688, 712 (D.N.J. 2018) (quoting *SmithKline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312 (Fed. Cir. 2006)), *rev'd and remanded sub nom. Biogen MA Inc. v. EMD Serono, Inc.*, 976 F.3d 1326 (Fed. Cir. 2020). In this case, claim 1 of the '294 patent is not directed to a product that the inventors were unable to describe in words or where the product's structure was not sufficiently understood. *Id.* As discussed above, the IEEE dictionary itself underscores that the term is well understood in the field and a POSA would have readily understood that the term "compensated GaN" layer refers to a GaN layer having certain structural and electric characteristics, not a GaN layer made according to a particular process.

Petitioner argues that "while the claim uses 'compensated as an adjective, that adjective derives from a past-tense verb" and that "[t]he past-tense form of 'compensated' suggests that the step of compensating had occurred." Petition at

14. Even if Respondents were correct that the term “compensated” derives from a past-tense verb, that does not transform the term “compensated” into a process term. Indeed, in *In re Garnero*, the predecessor court to the Federal Circuit recognized that past-tense verbs such as “‘intermixed,’ ‘ground in place,’ ‘press fitted,’ ‘etched,’ and ‘welded’ all . . . at one time or another have been separately held capable of construction as structural, rather than process, limitations.” 412 F.2d 276, 279 (C.C.P.A. 1969); *see also 3M Innovative Prop. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (“‘[S]uperimposed’ . . . neither transforms claim 1 into a product-by-process claim nor even limits the scope of the claim to a serial method of manufacture; it describes only the structural relationship between the embossing patterns.”); *Hazani v. U.S. Int’l Trade Comm’n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997) (“‘chemically engraved’ not a process term). As discussed above, “compensated GaN layer” is not merely “capable of construction as [a] structural, rather than a process, limitation,” *In re Garnero*, 412 F.2d at 279, a POSA would understand the term to be a structural term.

But even if the Court believes that “compensated” can be interpreted as both a structural limitation (as Patent Owner proposes) and as a process limitation (as Petitioner proposes), the term still would not be a product-by-process limitation. “[W]ords of limitation that can connote with equal force a structural characteristic

of the product or a process of manufacture are commonly and *by default* interpreted in their structural sense, unless the patentee has demonstrated otherwise.” *In re Nordt Dev. Co.*, 881 F.3d 1371, 1375 (Fed. Cir. 2018) (emphasis added). Here, Patent Owner has clearly demonstrated that “compensated” is to be interpreted in its structural sense as allowing for modified electric characteristics in a GaN gate material that were otherwise possible in a material that was not compensated. *See Hazani*, 126 F.3d at 1479 (“chemically engraved” limitation not a product-by-process limitation because the limitation, “read in context, describes the product more by its structure than by the process used to obtain it”).

IV. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1A (SMITH ALONE)

In Ground 1A, Petitioner asserts that *Smith* alone “discloses the allegedly inventive elements, including the “compensated GaN” and “semi-insulating” layers recited in independent claims 1, 4, 7 and 10 of the ‘294 patent. Petition, pp. 21-22, 38, 46, 50 and 53. As explained below, Petitioner misinterprets and misrepresents the teachings of *Smith*.

Smith discloses a HEMT device with a cap layer 34 that extends completely between the ohmic contacts 30. As described in para [0070], a doped region 40 is provided over the cap layer.

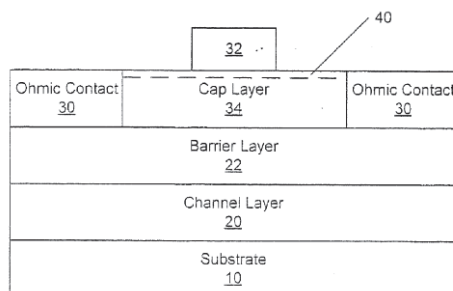


Figure 2A

Per *Smith*, paragraph [0085]:

In some embodiments of the present invention, the **doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C.** In other embodiments of the present invention, the doped region 40 is doped with an n-type dopant, such as Si, Ge and/or O. In further embodiments of the present invention, the doped region 40 is doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co. The dopant may be incorporated into the cap layer 34 during deposition or growth of the cap layer 34, 34' or may be subsequently implanted, for example, using ion implantation. In some embodiments of the present invention, the cap layer 34 has a dopant incorporated throughout the cap layer 34, 34'. In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34'. [Emphasis added.]

In other embodiments, e.g., Figs. 3B/4B, without a doped region 40, a passivation layer (BN Layer 100' or SiC layer 110') is provided above the cap layer:

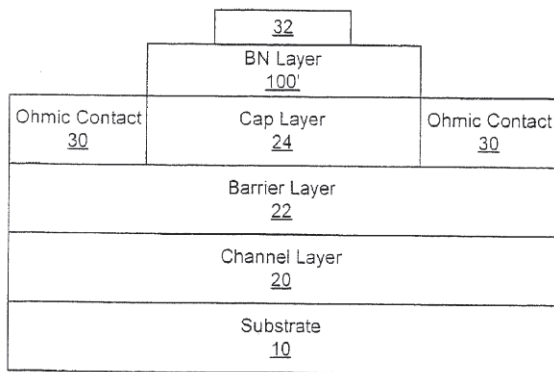


Figure 3B

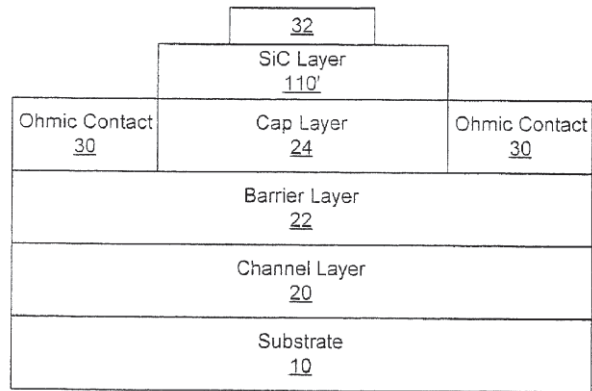


Figure 4B

A. Smith does not disclose the “compensated GaN layer” of independent claim 1.

Petitioner asserts that the cap layer 34 shown in Figure 2A may be a GaN layer or a GaAlN layer (which is correct) and that **doped region 40** may be doped with p-type dopant, e.g., Mg (also correct). However, Petitioner asserts (incorrectly) that **the cap layer 34**, in the embodiment of Figure 2A, is **necessarily** a compensated layer because “by 2009 it was well-known that hydrogen would be naturally present in such layers,” and “[i]t was known that hydrogen would be present even in as-grown GaN materials, forming acceptor-H neutral complexes that passivate the impurity.” Petition, p. 42. “And because it was well-known that as-grown GaN films are naturally hydrogen passivated, ... *Smith*’s cap layer 34 has passivated impurities.” Petition, p. 39.

Petitioner’s assertion is based on a false premise and is incorrect for at least three important interrelated reasons:

1. *Smith* provides little detail regarding the formation of the cap layer.

Smith discloses in [0077]: “The cap layer 24, 24’ may be blanket formed on the barrier layer 22 and may be epitaxially grown and/or formed by deposition.” Petitioner makes no argument that, if the cap layer is formed by deposition rather than epitaxial growth, hydrogen would be incorporated in the cap layer. With respect to an epitaxial growth process, *Smith* discloses in [0064]: “The cap layer 24, 24’ may be provided by conventional epitaxial growth techniques where a higher Al concentration is provided during termination of growth of the cap layer 24, 24’. Thus, for example, the cap layer 24, 24’ may be provided by MOCVD growth with an increase in the Al source just prior to and during termination of growth.” **However, importantly, there is no indication in *Smith* that the “conventional epitaxial growth techniques” that *Smith* references are carried out in the presence of hydrogen.**

2. U.S. Patent No. 6,498,111 (“the ‘111 patent”), which *Smith* incorporates by reference in [0083], indicates that there are processes which remove hydrogen prior to cool down. Ex. 2005 at 2:1-3.
3. Importantly, even if hydrogen was present during epitaxial growth in the particular “conventional growth technique” chosen by a skilled person

seeking to produce a device according to *Smith*'s teachings, that skilled person, following conventional wisdom (as set forth in the '111 patent) would have included an anneal/activation step to remove hydrogen ('111 patent, lines 13-28) as was conventional (see the '111 patent, col. 2, lines 13-17). Indeed, in [0083], *Smith* explicitly suggests that "an anneal of the structure including the passivation layer may be carried out in an oxygen environment to remove hydrogen from the layer."¹

Petitioner also posits that a POSA would have been motivated to passivate *Smith*'s cap layer to result in the claimed "compensated GaN layer."

Specifically, at pages 26-27 of the Petition, Petitioner asserts:

A POSITA would have been motivated to adjust *Smith*'s doping by using hydrogen passivation because *Smith* recognizes level of doping as a result-effective variable controlling transistor characteristics, and a POSITA would have known that hydrogen passivation adjusted the doping level. *Smith* discloses that the level of doping in cap layers is a result-effective variable to control leakage, explaining that "[t]he level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant 'surface' state but not so high as to provide introduce traps or leakage paths." By 2009, a POSITA was intimately familiar with acceptor doping and hydrogen passivation. A POSITA would have known that incorporating hydrogen in GaN layers would passivate acceptor dopants affecting the level of doping.

¹ The '111 patent **teaches away** from passivation with hydrogen. A skilled person reading the '111 patent would have been led in the opposite direction of the invention of the '294 patent, and would have sought to **avoid compensation** of p-GaN by passivation of hydrogen.

Petitioner confuses the “level of doping” with the level of compensation of dopants. Passivating a doped GaN layer does not affect the level of doping of that GaN layer. Rather, passivation with hydrogen affects to what extent the dopants in a p-GaN layer are compensated, not the level of doping (which is based on the concentration of dopants in the layer). Accordingly, absent hindsight, a POSA would not have looked to hydrogen passivation as a way to alter *Smith*’s level of doping.

Moreover, *Smith* requires active, rather than compensated, p-type dopants: “P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and or minimize trapping effects.” Ex. 1005 at ¶ [0072]. *Smith* even discloses a preferred p-type dopant level: “With p-type dopants, the doped region 40 may provide a dopant concentration of from about 10^{16} to about 10^{22} cm^{-3} .” Ex. 1005 at ¶ [0087]. Given *Smith*’s teaching requiring active p-type dopants in region 40, a POSA would not contemplate doing the opposite and compensating the very dopants that are necessary for the *Smith* device to function effectively.

Even the above quoted passage at ¶ [0087] of *Smith* regarding the “level of doping” states only that it “should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths.” Thus, in paragraph

[0087], *Smith* simply reiterates that a specific **concentration of dopants** is necessary, **not that those dopants should be compensated**. *Smith* therefore provides no motivation for a POSA to compensate.

In summary, the portions of *Smith* relied upon in the Petition relate to methods for achieving a desired level of **doping** in a semiconductor material, not a desired level of passivation/compensation of the dopants. Compensating *Smith*'s doped layer 40 would negate the effects of the doping of that layer. *Smith* would not dope layer 40 only to subsequently compensate the doping. Doing so would be completely counterintuitive and runs completely counter to *Smith*'s stated intentions. *Smith*'s disclosure thus goes in **the exact opposite** direction of the compensated gate of the '294 patent.

***Smith* therefore does not disclose compensation**, under either party's construction, and it cannot be implied or rendered obvious from the disclosure of *Smith* for the reasons stated above. If compensation occurred naturally in *Smith* during the "conventional growth techniques", as assumed by Petitioner, *Smith* would have taken steps to remove the hydrogen, so that region 40, if p-doped, would work as intended. ***Smith* thus does not disclose or suggest the "compensated layer" of independent claim 1, and a POSA would not be motivated to compensate *Smith*'s cap layer.**

B. Smith does not disclose the "semi-insulating III-N layer" of independent claims 4, 7 and 10.

At page 46 of the Petition, Petitioner asserts that “*Smith* discloses that cap layer can be a ‘semi-insulating III-N layer.’” Specifically, on page 47 of the Petition, Petitioner incorrectly refers to Figure 2A of *Smith* as disclosing “*Smith*’s **semi-insulating cap layer 34** above barrier layer 22.” [Emphasis in original.]

In fact, *Smith* never states or even remotely implies that the cap layer 34 is “semi-insulating.” Petitioner effectively concedes that the term “semi-insulating” is actually not associated with *Smith*’s cap layer, but rather comes from *Smith*’s incorporation by reference of *Saxler874* (Ex. 1016). Petition at 46.

Petitioner’s argument appears to focus on *Smith*’s disclosure in [0085] that, “[i]n further embodiments of the present invention, the doped region 40 is doped with a deep level dopant” and that “in some embodiments, doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34.” Invoking *Smith*’s subsequent incorporation by reference of *Saxler874*, Petitioner combines these disclosures in *Smith* with the disclosure in *Saxler874* “that co-doping “provide[s] semi-insulating Group III nitride layers.” Ex. 1016 at [0005]. But there is a fundamental flaw in Petitioner’s argument.

The portion of *Saxler874* on which the Petitioner relies does not state or suggest that *any* type of co-doping results in a semi-insulating Group III nitride layer, as Petitioner implies. Rather, in [0005], *Saxler874* discloses:

“Embodiments of the present invention provide semi-insulating Group III nitride semiconductor layers and methods of fabricating semi-insulating Group III nitride layers. In certain embodiments of the present invention, fabrication of a semi-insulating Group III nitride layer includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.” To the extent this disclosure teaches creating a semi-insulating layer using co-doping, a POSA would understand this disclosure to mean that co-doping a shallow level p-type dopant and a deep level dopant is what would result in the semi-insulating layer.

Conversely, in the context of paragraph [0085], where *Smith* incorporates *Saxler*⁸⁷⁴ by reference, *Smith* at most teaches co-doping regions of different dopant concentrations (“In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34’”). There is no suggestion in *Smith* that region 40, if p-doped, should be co-doped with a deep level dopant. And Petitioner has provided no motivation as to why a POSA would use that type of co-doping in *Smith*. Accordingly, Petitioner has not established that *Smith* discloses or renders obvious a **“semi-insulating III-N layer above the barrier layer”** as recited in independent claims 4, 7 and 9.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 1A.

V. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1B

In Ground 1B, Petitioner asserts that *Smith* in view of *Kigami* renders obvious the “compensated GaN layer” recited in independent claim 1. Petition, p. 24-31. As explained above, Petitioner misinterprets and misrepresents the teachings of *Smith* with regard to the claimed features recited in independent claim 1. As explained below, *Kigami* does not rectify the deficiencies of *Smith*.

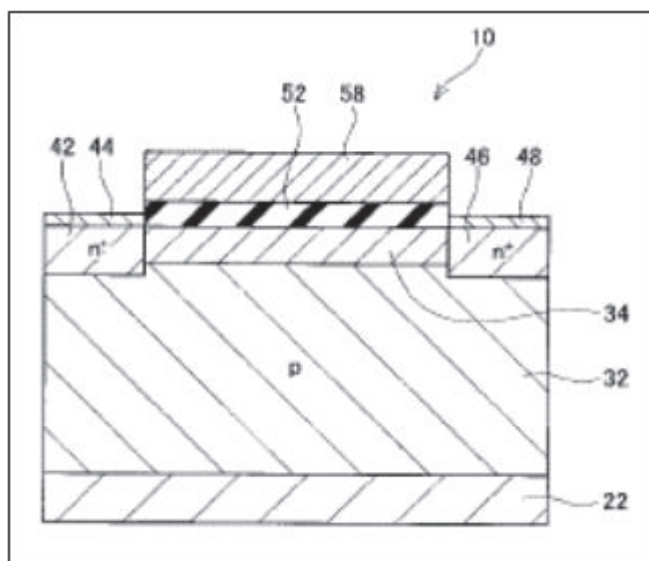
A. Kigami does not rectify the deficiencies of Smith with respect to the “compensated GaN layer” of independent claim 1.

At page 28 of the Petition, Petitioner asserts that a “POSITA would have been motivated to apply *Kigami*’s hydrogenation processing step(s) to passivate impurities in *Smith*’s cap layers.” Petitioner also contends that the motivation for modifying *Smith* is provided in *Kigami*: “A POSITA would have been motivated to use *Kigami*’s hydrogen incorporation techniques to form a region with passivated impurities in Smith’s cap layer.” *Id.* Patent Owner disagrees.

In *Kigami*, hydrogen is present in the local region 34, above the semiconductor layer 32, and purportedly “forms a composite” with the magnesium in the local region 34. Ex. 1008 at [0022]. The semiconductor layer 32 is formed directly on the substrate 22. That semiconductor layer corresponds to a buffer

and/or a transition layer with regard to claim 1. A gate-insulating film 52 is formed *above* the local region 34 of the semiconductor layer 32, and a gate electrode is formed above that gate-insulating film 52. *Id.* at ¶[0020].

The *Kigami* device, as shown in Figure 1 below, thus has a gate insulator 52 that is *above* the insulating barrier (local region 34). Hydrogen is introduced to lower the threshold voltage and form a channel *under* the gate insulator 52. A fully activated (not compensated) p-GaN layer (semiconductor layer 32) *below* the local region 34 depletes the 2DEG from the channel.



***Kigami* at FIG. 1**

Kigami discloses a different device from the device recited in claim 1 of the '294 patent and is cumulative to *Bowers*, which was considered for its discussion of passivation by hydrogen in GaN material during prosecution of the '294 patent. Ex. 1002 at 87-88; Ex. 1020.

Kigami uses an entirely different layer as the “gate insulating film” below the gate contact and incorporates a fully-activated p-type GaN layer and a GaN layer with magnesium and hydrogen to form the channel. Nothing in *Kigami* discloses or suggests that its hydrogen-treated p-type GaN layer would be suitable below the gate contact or that a compensated GaN layer including Mg dopants and hydrogen would be acceptable or functional in place of the cap layer 34 of *Smith*. In fact, as explained above, hydrogen is introduced to the GaN layer in *Kigami* in order to form a channel, not to reduce gate leakage. A POSA would therefore not seek to combine the teachings of *Smith* with *Kigami*, to “apply *Kigami*’s hydrogenation techniques to *Smith*’s cap layer 34,” absent impermissible hindsight.

Furthermore, there is no motivation to combine *Smith* with *Kigami* because a POSA would find the doping of a gate semiconductor followed by the cancellation of the effects of the dopant to be highly counterintuitive. *Smith* makes clear the purpose of the dopants it utilizes: “The dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations.” *Smith* at [0064]. Passivating those dopants would void their purpose in *Smith*, rendering the *Smith* device inoperable for its stated purpose.

Smith in view of *Kigami* therefore do not render obvious the claimed “compensated GaN layer,” under either party’s construction.

B. Kigami does not rectify the deficiencies of Smith with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10.

Petitioner does not contend that *Kigami* is relevant or combinable with *Smith* with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10. Pet. at pp. 46-47, 49-50 and 56.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 1B.

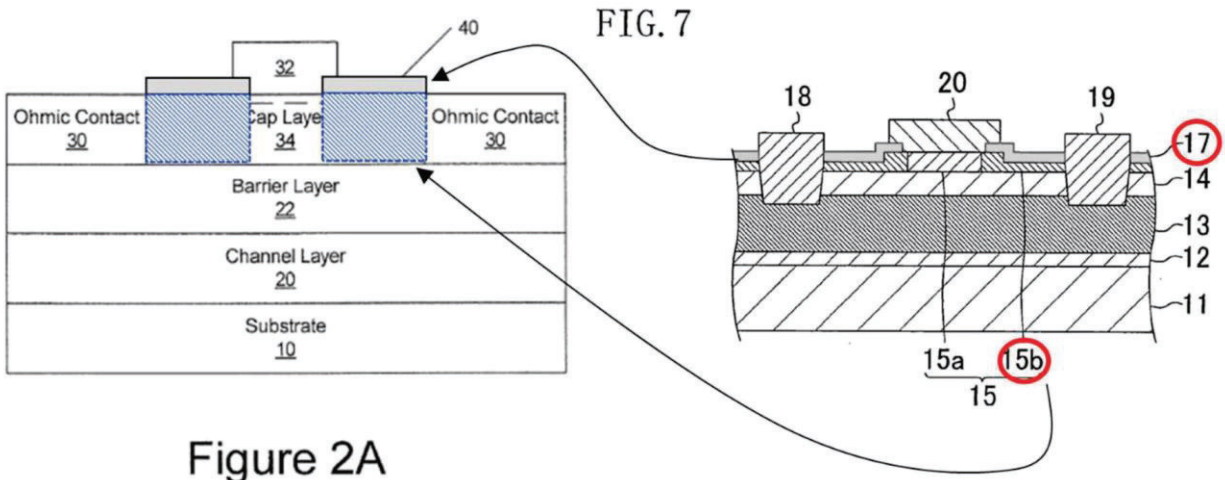
VI. THE BOARD SHOULD DENY INSTITUTION OF GROUND 1C

In Ground 1C, Petitioner asserts that *Smith* in view of *Uemoto* renders obvious the “compensated GaN layer” recited in independent claim 1. Petition at 25-26. As explained above, Petitioner misinterprets and misrepresents the teachings of *Smith* with regard to this claimed feature. As explained below, *Uemoto* does not rectify the deficiencies of Smith in this regard.

A. Uemoto does not rectify the deficiencies of Smith with respect to the “compensated GaN layer” of independent claim 1.

At page 31 of the Petition, Petitioner asserts that a “POSITA would have been motivated to apply *Uemoto*’s hydrogen diffusion technique to selectively increase the resistivity of Smith’s cap layers.” More specifically, Petitioner asserts that a POSA would have been motivated to use *Uemoto*’s “hydrogen diffusion film 17” in *Smith* to form the “high resistive region 15b,” “to similarly inactivate

impurities in *Smith*'s cap layer, generate the highly resistive regions, and reduce leakage."



Petitioner is incorrect. Absent hindsight, there would have been no motivation for a POSA to modify *Smith* to incorporate the teachings of *Uemoto*, and even if the two were combined as Petitioner proposes, the resultant device would still not have a compensated layer under the gate contact as claimed.

Petitioner argues that *Uemoto* suggests and motivates the combination of *Smith* and *Uemoto*. Petition at 32. Specifically, Petitioner posits that inactivating impurities increases resistivity and reduces leakage, which would assist *Smith* with its concern with fabrication methods that reduce transistor leakage. But *Smith*'s focus is on adjusting the level of doping, not inactivating impurities. Petitioner has provided no motivation as to why, given *Smith*'s concern with doping level adjustments, a POSA would seek to inactivate impurities in *Smith*.

Moreover, Petitioner does not argue or provide any proof that the alleged compensated GaN layer of the *Smith-Uemoto* combination is under the gate contact. *See* Petition at 31-33, 43. Even if Petitioner did so, the resultant combined *Smith-Uemoto* device would not have “a gate contact above the compensated GaN layer,” as recited in claim 1 of the ’294 patent. For example, on page 43 of the Petition, Petitioner asserts that “applying *Uemoto*’s technique to diffuse hydrogen would result in cap layer 34 being “compensated,” as the term is used in the ’294 patent. But as is evident from Petitioner’s above illustration of the proposed combination of *Smith* and Fig. 7 of *Uemoto*, the alleged “compensated” region of *Smith* is NOT under the gate contact 32 of *Smith*, as required by claim 1. Thus, the proposed combination, even if attempted, would not result in a GaN transistor as claimed, with a compensated layer under the gate contact.

Smith in view of *Uemoto* therefore do not render obvious the claimed “compensated GaN layer,” under either party’s construction.

B. Uemoto does not rectify the deficiencies of Smith with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10.

Petitioner does not contend that *Uemoto* is relevant or combinable with *Smith* with respect to the “semi-insulating III-N layer” of independent claims 4, 7, and 10. Pet. at 46-47, 49-50 and 56.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 1C.

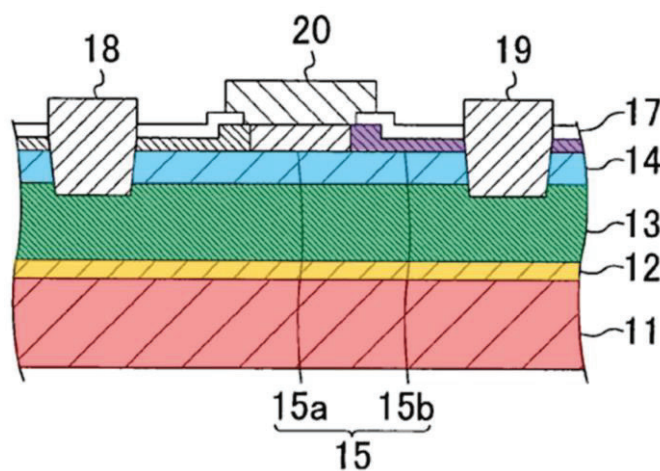
VII. THE BOARD SHOULD DENY INSTITUTION OF GROUND 2

In Ground 2, Petitioner reverses the order of the prior art as compared to Ground 1C, and asserts that *Uemoto* in view of *Smith* meets independent claims 1, 4, 7 and 10 of the ‘294 patent. Petition, p. 61-67. As explained below, Petitioner misrepresents the teachings of *Uemoto* with respect to the “compensated GaN layer” of claim 1, and the “semi-insulating III-N layer” of independent claims 4, 7, and 10.

A. Uemoto does not disclose the “compensated GaN layer” of independent claim 1.

At page 61 of the Petition, Petitioner asserts that *Uemoto* discloses the compensated GaN layer of independent claim 1, because *Uemoto* discloses that “a third nitride semiconductor layer 15” is formed with GaN doped with magnesium.” Petitioner asserts that “layer 15 is compensated,” “because *Uemoto* discloses that the impurities in region 15b of the layer 15 are inactivated when ‘hydrogen from the hydrogen diffusion film 17 is supplied during a thermal treatment.’” *Id.*

FIG. 7



Uemoto at FIG. 7.

Importantly, Petitioner conflates two separate elements of *Uemoto* in its analysis: element 15a, which is a p-doped *conductive*, activated AlGaIn/GaN region, and element 15b, which is a resistive p-doped AlGaIn/GaN region. *Uemoto* at ¶ [0033], [0063]. Petitioner conflates those two distinct elements of *Uemoto* to obscure the fact that it is the *conductive*, activated p-doped AlGaIn region 15a, not the resistive region 15b, which is situated above the barrier layer 14 and below the gate electrode 20, as recited in independent claim 1 of the '294 patent.

As shown in Figure 2B of *Uemoto*, there is always a 2DEG under p-doped high resistive region 15b. *See* Ex. 1006 at Fig. 2B, [0038]. Upon application of a positive gate voltage, the activated p-type material of region 15a operates like the “highly doped p-GaN 106” shown in prior art Figure 1 of the '294 patent, such that the *Uemoto* device depletes the 2DEG under the gate and conducts with a high gate

leakage current relative to the device of the '294 patent. *See* Ex. 1006 at Fig. 2A, 2B, [0038]; '294 patent at Fig. 1, 2:3-6.

Thus, a fundamental issue with Petitioner's argument is that region **15b** is not under the gate, nor is the overlying hydrogen passivation film 17 that supplies hydrogen to inactivate the acceptors (e.g., magnesium) in region 15b under the gate. Region 15b serves absolutely no function in depleting the underlying 2DEG and turning the device on or off. Rather, that function is carried out by gate contact 20 and underlying region 15a, which is conductive, not inactivated.

It is clear that the conductive control region 15a of *Uemoto* contains activated (conductive) rather than passivated (semi-insulating) p-type material because *Uemoto* intentionally activates the Mg dopants in the control region:

“When a thermal treatment is performed in an inert gas atmosphere at 800° C. for about 20 to 60 minutes, the hydrogen atom is desorbed from Mg. Then, the Mg is activated, and **thus the nitride semiconductor layer shows p-type conductivity.**”

Id. at ¶ [0049] (emphasis added). *Uemoto* specifically notes that this activation process is performed in a nitrogen atmosphere. *Id.* at ¶ [0048]. That is in contrast to *Uemoto*'s discussion of the high resistive region 15b, “in which the p-type impurity is not activated to offer a high resistive layer.” *Id.* at ¶ [0051]. *Uemoto* discloses: “The third nitride semiconductor layer doped with Mg is composed of: a control region **15 a** in which Mg is activated to exhibit a p-type conductivity; and

a high resistive region **15 b** in which Mg is not activated to offer a higher resistance than the control region **15 a**.” *Id.* at ¶ [0033]. *Uemoto* thus reflects the conventional understanding prior to the ’294 patent, that passivation below the gate is unfavorable to the formation of an enhancement mode transistor.

Notably, in a parallel invalidation request to the Chinese Patent Office relating to the Chinese counterpart of the ’294 patent proceeding, Petitioner relied upon the p-doped conductive region 15a, not high resistive region 15b, as purportedly disclosing the “compensated GaN layer.” *See* Ex. 2006 at 23-25. That inconsistency demonstrates that Petitioner itself recognizes that it is unreasonable to identify region 15b as meeting the “compensated GaN layer” of independent claim 1, because region 15b is not under the gate electrode 20, as required by claim 1 of the ’294 patent.

Furthermore, it would not have been obvious to adjust *Uemoto*’s gate electrode 20 and region 15b such that region 15b was under the gate because such a modification would run counter to *Uemoto*’s stated goal of having a control region under the gate with much lower resistivity than the high resistive region 15b. *See* Ex. 1006 at [0033]. *Uemoto* highlights the importance of activation in the control region below the gate, stating “in the control region, as shown in Figure 2A, the p-type impurity contained in the third nitride semiconductor layer **15** is

activated” and that this activation “results in obtaining the normally-off characteristics of nitride semiconductor transistors.” *Id.* at [0038].

Moreover, *Uemoto* does not disclose “a compensated GaN layer,” as recited in claim 1 of the ’294 patent because the p-doped high resistive region 15b is not a part of the gate material (that is, region 15b is not under the metal gate). As shown in Figure 7 above, it is the conductive control region 15a that “comes into ohmic contact with” and is part of the gate structure along with gate electrode 20. *Id.* at [0034]. But *Uemoto* discloses no such contact between the gate electrode and the p-doped high resistive region 15b, and Figure 7 shows that it is: (1) separated from the gate electrode by the hydrogen diffusion film 17, and (2) extends well beyond the structure of the gate.

Because *Uemoto* does not disclose a “compensated GaN layer,” for at least the reasons outlined above, *Uemoto* cannot disclose “a gate contact above the compensated GaN layer,” as recited in claim 1 of the ’294 patent. The gate contact and compensated GaN layer, as recited in claim 1 of the patent, together form the gate structure of the transistor of claim 1. *Uemoto* does not disclose, teach, or suggest that element, and therefore the element, “a gate contact above the compensated GaN layer,” of claim 1 is not disclosed by *Uemoto*.

Uemoto in view of *Smith*² therefore do not render obvious the claimed “compensated GaN layer,” under either party’s construction.

B. Uemoto in view of Smith does not disclose the “semi-insulating III-N layer” of independent claims 4, 7 and 10.

At page 78 of the Petition, Petitioner concedes that *Uemoto* does not disclose layer 15 as being “semi-insulating.” Petitioner thus relies upon *Smith* for this teaching, referring to the arguments at VIII.G.6 (pp. 46-47) of the Petition.

Petitioner asserts that *Smith*’s cap layer 34 can be formed with “[t]echniques for co-doping Group III-nitride materials,” Ex. 1005 at [0085], and that *Saxler*⁸⁷⁴ (Ex. 1016), which *Smith* incorporates by reference, explains that co-doping “provide[s] semi-insulating Group III nitride semiconductor layers.” Ex. 1016, [0005].

But, as explained above, there is a fundamental flaw in Petitioner’s argument. *Smith* never states or even remotely implies that the cap layer 34 is “semi-insulating.” Petitioner effectively concedes that the term “semi-insulating” is actually not associated with *Smith*’s cap layer, but rather comes from *Smith*’s incorporation by reference of *Saxler*⁸⁷⁴. Petition at 46.

² Petitioner does not rely on *Smith* to provide an alleged teaching of “compensated GaN layer” in Ground 2.

Petitioner's argument appears to focus on *Smith*'s disclosure in [0085] that, "[i]n further embodiments of the present invention, the doped region 40 is doped with a deep level dopant" and that "in some embodiments, doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34." Invoking *Smith*'s subsequent incorporation by reference of *Saxler874*, Petitioner combines these disclosures in *Smith* with the disclosure in *Saxler874* "that co-doping "provide[s] semi-insulating Group III nitride layers." Ex. 1016 at [0005]. But there is a fundamental flaw in Petitioner's argument.

The portion of *Saxler874* on which the Petitioner relies does not state or suggest that *any* type of co-doping results in a semi-insulating Group III nitride layer, as Petitioner implies. Rather, in [0005], *Saxler874* discloses:

Embodiments of the present invention provide semi-insulating Group III nitride semiconductor layers and methods of fabricating semi-insulating Group III nitride layers. In certain embodiments of the present invention, fabrication of a semi-insulating Group III nitride layer includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.

To the extent this disclosure teaches creating a semi-insulating layer using co-doping, a POSA would understand this disclosure to mean that co-doping a shallow level p-type dopant and a deep level dopant is what would result in the semi-insulating layer.

Conversely, in the context of paragraph [0085], where *Smith* incorporates *Saxler*⁸⁷⁴ by reference, *Smith* at most teaches co-doping regions of different dopant concentrations (“In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34”). There is no suggestion that a p-type dopant be co-doped with a deep level dopant. And Petitioner has provided no motivation as to why a POSA would use that type of co-doping in *Smith*.

Accordingly, for the reasons set forth above, *Smith* thus does not rectify the admitted deficiency of *Uemoto* with respect to a **“semi-insulating III-N layer above the barrier layer”** as recited in independent claims 4, 7 and 10.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 2.

VIII. RESERVATION OF RIGHTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if IPR is instituted. Similarly, Patent Owner does not concede any underlying contentions in the Petition and reserves the right to rebut any such contention later. Further, Patent Owner is not limited to the arguments presented in this Preliminary Response, but

expressly reserves the right to raise further arguments, including claim construction arguments, not presented herein.

IX. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

Dated: December 21, 2023

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER's PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 8,034 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

Dated: December 21, 2023

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

Innoscience-EPC-IPRs@finnegan.com

Dated: December 21, 2023

Respectfully submitted,

/s/ Walter D. Davis, Jr.

Walter D. Davis, Jr. (Reg. No. 45,137)

Counsel for Patent Owner

Exhibit B

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01383
U.S. Patent No. 8,404,508

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

In accordance with 37 C.F.R. § 42.107, Patent Owner Efficient Power Conversion Corporation (“EPC” or “Patent Owner”) submits this preliminary response to the Petition (the “Petition” or “Pet.”) filed by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (“Petitioner”) for *Inter Partes* Review of claims 1-5 of U.S. Patent No. 8,404,508 (the “‘508 patent”). Patent Owner respectfully requests that the Board deny the Petition for at least the reasons set forth below.

First, Petitioner fails to establish that the asserted prior art teaches both a “gate photo resistant pattern” and a “metal photo resistant pattern” (or “fourth photo resistant pattern”). The ‘508 patent describes and claims a separate and distinct “gate photo resistant pattern” and “metal photo resistant pattern.” Petitioner admits that each of the asserted primary references (*Yoshida*, *Hikita-347*, *Hikita-023*) fails to disclose these two photo resistant patterns, instead relying on *Beach*. But Petitioner points to a single photo resist pattern in *Beach* as allegedly teaching both the claimed “gate photo resistant pattern” and a “metal photo resistant pattern.” Because the claims require separate patterns that are used at different times in the claimed processes, Petitioner’s challenges are deficient.

Second, Petitioner has not established that a person of ordinary skill in the art (“POSA”) would have been motivated to combine the asserted primary

references (*Yoshida*, *Hikita-347*, *Hikita-023*) with *Beach* to result in the claimed methods of forming an enhancement mode GaN transistor. The ‘508 patent describes and claims processes for forming transistors in which a gate structure is formed before source and drain contacts are formed. These “gate first” processes are substantially different than the asserted primary references, which all form a gate structure after source and drain contacts are formed. These “gate first” processes are also substantially different than the crucial *Beach* reference, which simultaneously forms a gate structure and ohmic contacts (which Petitioner equates to the source and drain contacts). Petitioner has provided no motivation as to why a POSA would combine a “gate last” process with a simultaneous gate/ohmic formation process to result in a “gate first” process, as disclosed and claimed by the ‘508 patent.

Accordingly, Petitioner has not established that there is a reasonable likelihood that at least one of the challenged claims of the ‘508 patent is unpatentable, and the Petition should be denied.

II. BACKGROUND

A. The ‘508 Patent

The ‘508 patent describes and claims a method for making an enhancement-mode GaN HEMT (high electron mobility transistor) device using a single photo mask to form a gate structure, applying a photoresist pattern to pattern and etch

areas in a dielectric layer within which the source and drain contacts will be deposited, and applying a photoresist pattern to pattern and etch metal to form the source and drain contacts. The process results in an enhancement-mode GaN HEMT with a self-aligned gate structure. *See* '508 patent at 4:55-59.

The single mask self-alignment of the gate described in the '508 patent prevents misalignment between the gate metal and the GaN gate material. The '508 patent discloses a method for forming a GaN HEMT device in which the “gate metal 17 and the p-type GaN material 15 are patterned and etched using a single photo mask and are thus self-aligned.” *Id.* at 4:55-59. The resulting HEMT performs better than those previously known in the art (particularly with respect to undesirable gate leakage) and can be manufactured less expensively due to the single photo mask process. *See id.* at 4:7-19.

As illustrated in the below Figures 3A-3C from the '508 patent, after epitaxial growth, shown in Fig. 3A, a gate metal 17 (for example, TiN) is deposited atop the p-type GaN layer 15. '508 patent at 3:26-44. Then, using photolithography, a gate photo-resist pattern is formed on the epitaxial wafer surface. *Id.* at 3:45-56. Then the gate metal 17 is then etched. *Id.* Subsequently, the p-type GaN gate layer 15 is etched using the same photo-resist pattern used to form the gate metal contact 17, resulting in the device of Fig. 3C. *Id.* Because the

two etching processes are formed with a single photo mask, the resulting gate structure is self-aligned.

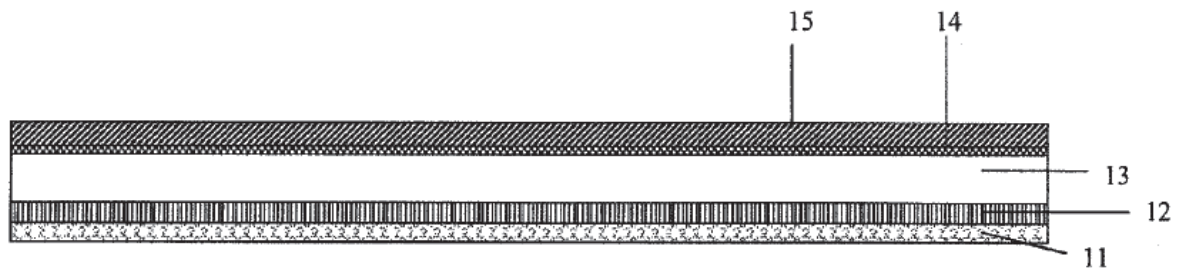


FIG. 3A

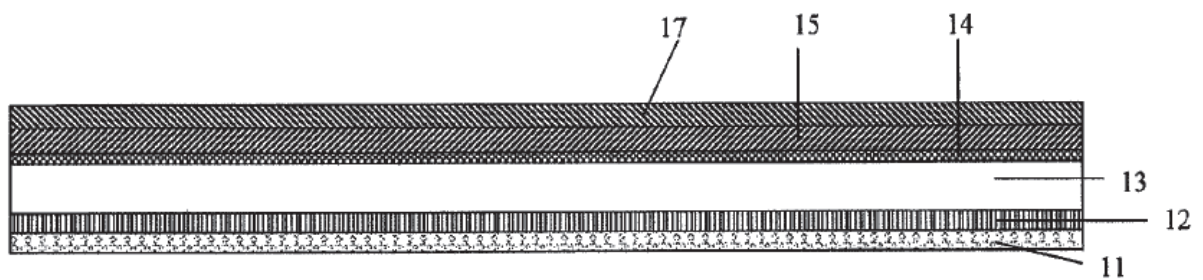


FIG. 3B

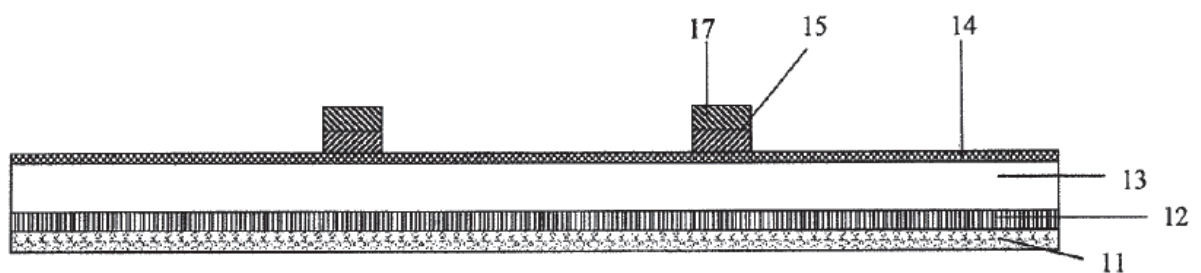


FIG. 3C

'508 Patent Figs. 3A-3C.

The gate structure of the '508 patent is formed before the source and drain contacts. That is, the '508 patent is directed to a “gate first” process. For example, as depicted in Fig. 3C, before source and drain contacts are formed, a single photo mask is used to pattern and etch the gate metal 17 and the p-type GaN gate layer 15. '508 patent at Fig. 3C, 3:45-47.

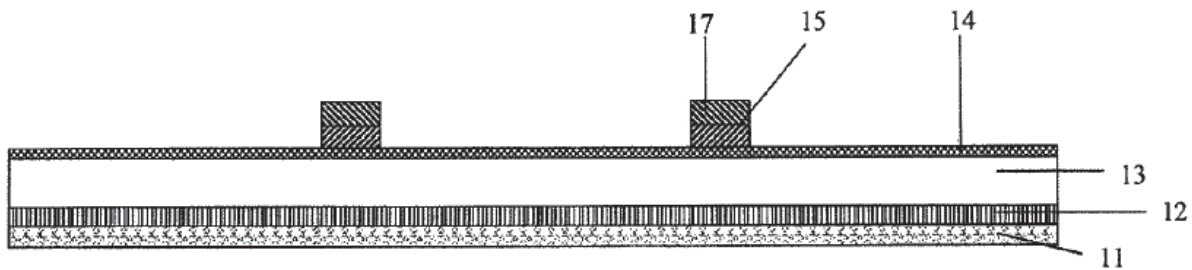


FIG. 3C

Subsequently, dielectric material 18 is deposited. After deposition of the dielectric material 18, a contact photo mask is used to pattern and etch the dielectric material 18, followed by a photoresist strip. The source and drain (20 and 19, respectively) are ultimately formed in the openings left by etching the dielectric material. '508 patent at Figs. 3D, 3E, 3:57-67.

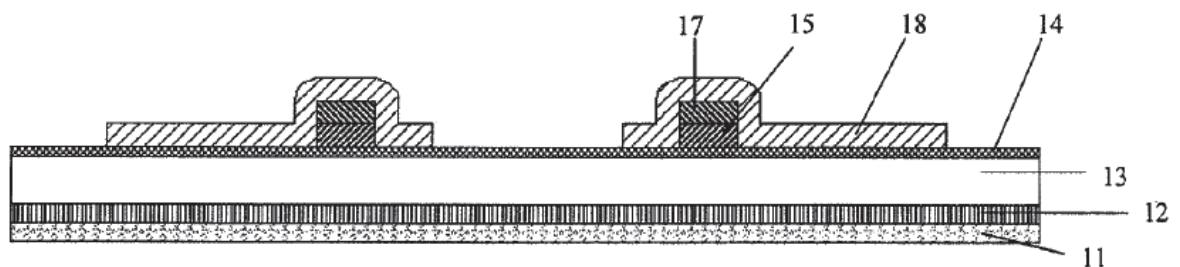


FIG. 3D

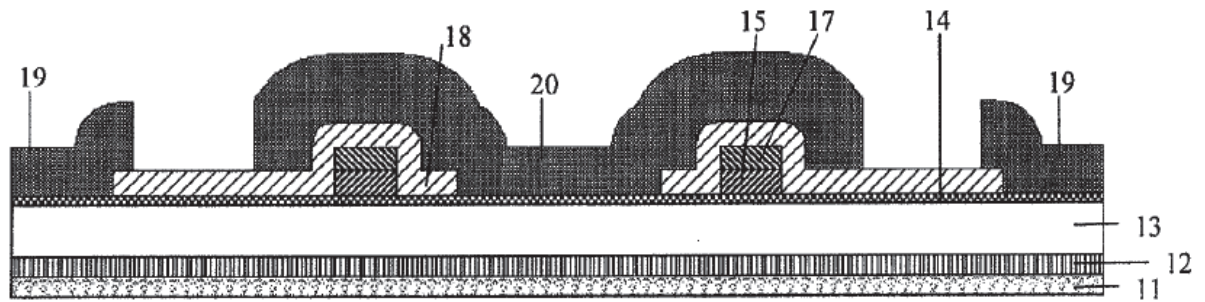


FIG. 3E

The claims are consistent with this description of a “gate first” process. For example, claim 1 requires “applying a gate photo resistant pattern,” “etching away the gate contact layer outside the gate region,” “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact,” and “removing the gate photo resistant pattern.” These claimed steps result in a gate structure.

Claim 1 also requires “depositing a dielectric layer,” “applying a contact photo resistant pattern,” and “etching the dielectric to open the drain and source contact area.” Because the claimed dielectric layer is etched to open the drain and source contact area, a POSA would understand that the dielectric layer must be deposited before forming the source and drain contacts. A POSA would also understand these claimed requirements to mean that the claimed gate structure was formed before the claimed source and drain contacts, because the claims do not specify that the dielectric layer is etched to form an opening for the gate structure. And if the dielectric layer was deposited before forming the gate structure, such an

opening in the dielectric layer would be necessary in order to result in an operating transistor.

Other embodiments, including the embodiments to which independent claims 4 and 5 are directed, have similar recitations that a POSA would understand describe a “gate first” process. *See* ‘508 patent at Figs. 5C, 5D, 5E, 7C, 7D, 7E, 7F, 4:41-54, 5:4-15.

B. Grounds of challenge

Petitioner challenges the patentability of the claims of the ‘508 patent on three grounds:

Ground 1: Claims 1-3 are challenged as being obvious over *Yoshida*, *Beach* and *Sheppard*.

Ground 2: Claims 1-4 are challenged as being obvious over *Hikita* 347, *Beach* and *Sheppard*.

Ground 3: Claim 5 is challenged as being obvious over *Hikita* 023, *Beach* and *Sheppard*.

III. CLAIM CONSTRUCTION

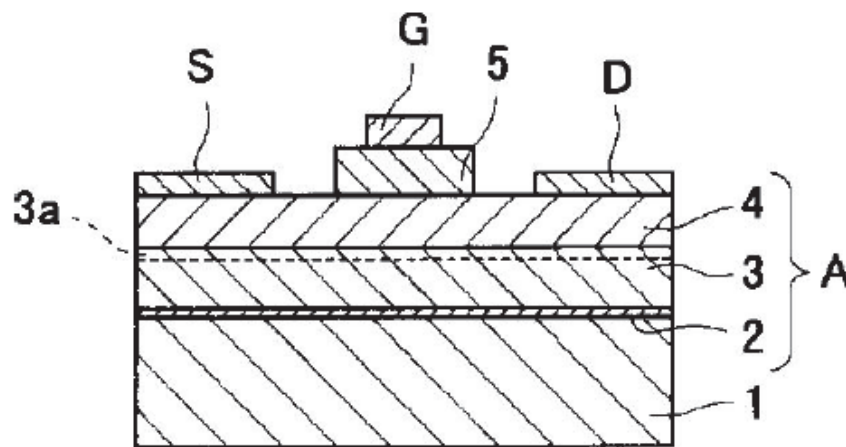
Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Without waiving its right to submit proposed claim

constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction.

IV. Overview of Selected References Relied Upon by Petitioner

A. Yoshida

Yoshida discloses an enhancement mode GaN HEMT, with a p-GaN layer under the gate contact:



Ex. 1004, Fig. 1.

The enhancement mode GaN HEMT of *Yoshida* is made by a process in which the gate structure is formed *after* forming the source and drain contacts (e.g., a “gate-last” process), as opposed to the “gate-first” process of the ‘508 patent. Specifically, as described in the Petition and in the ‘508 patent, Yoshida discloses the following process:

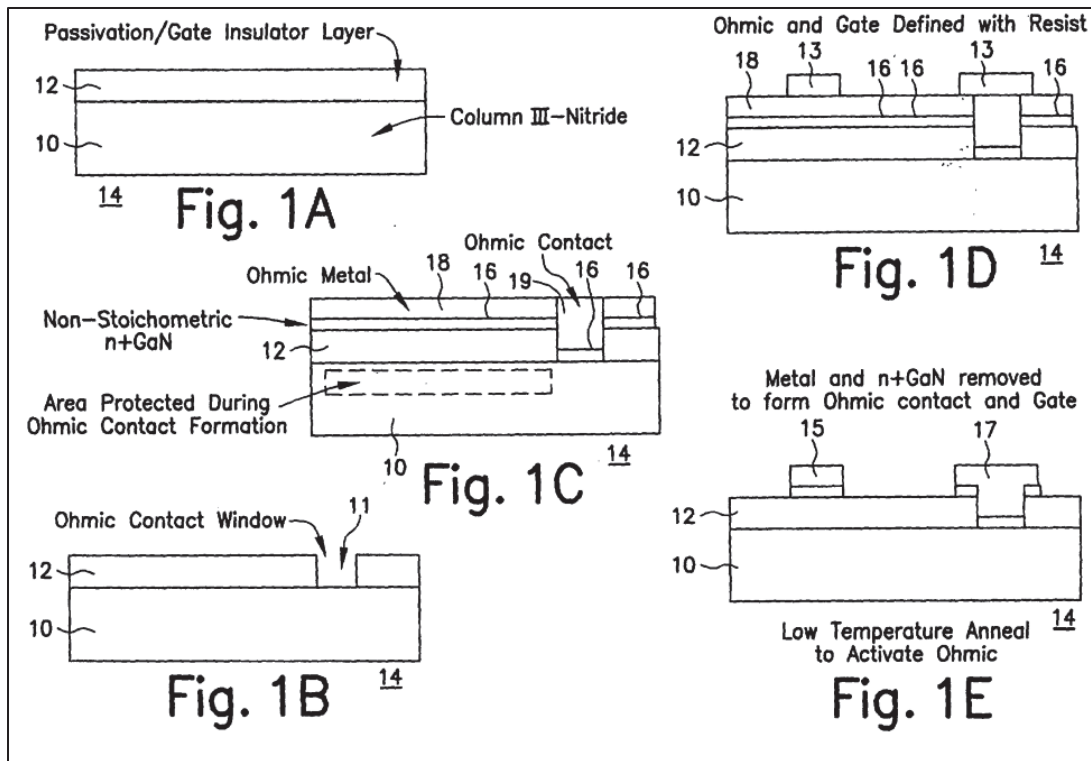
1. grow layers 2-5 over the substrate 1;

2. etch away the p-GaN layer 5 except where the gate electrode is to be loaded;
3. deposit a dielectric layer (SiO_2) to cover the entire surface, including the p-GaN layer 5;
4. apply photo resist/mask, open areas in the dielectric layer for the source S and drain D electrodes;
5. deposit Al in the openings to form the source S and drain D electrodes on the AlGaN barrier layer;
6. remove the mask and open the SiO_2 film over the gate p-GaN material 5, leaving the source S and drain D electrodes masked.
7. deposit Au in the opening to form the gate electrode G and form the gate contact above the p-GaN layer to produce an enhancement mode GaN transistor.

Petition at 14-15, citing *Yoshida* at [0013], [0021]-[0023].

B. Beach

The Beach process differs significantly from the “gate-first” process of the ‘508 patent and the “gate-last” process of *Yoshida*, described above. This process is shown in Figures 1A-1E below.



Ex. 1005 at Figs. 1A-1E.

First, as shown in Figure 1A, a III-nitride layer 10 and a gate insulator layer 12 are formed on a substrate. Ex. 1005 at [0039] and [0040].

Second, as shown in Figure 1B, “an ohmic contact window 11 is opened in layer 12 to provide access to layer 10 for the deposition of an ohmic contact.” *See id.* at [0042]. The gate insulator layer 12 serves as the insulator layer in the depletion mode MISFET of Beach.

Third, as shown in Figure 1C, non-diffusive protective layer 16, is formed over the device 14 of Figure 1B. *See id.* at [0043]. After the deposition of the material layer 16 atop the III-nitride layer 10 and the gate insulator layer 12 and

within the ohmic contact window 11, an ohmic metal material layer 18 is deposited. *See id* at [0045].

Fourth, as shown in Figure 1D, “resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17.” *See id.* at [0047]. After the photoresist layer 13 has been deposited, an etching takes place, removing the portions of the ohmic metal layer 18 and material layer 16 except within the areas protected by the photoresist layer 13. *See id.* Notably, as is evident from this description, *Beach* teaches a single etching step to finalize the formation of the gate 15 and ohmic contact 17, such as source and drain contacts, all at the same time.

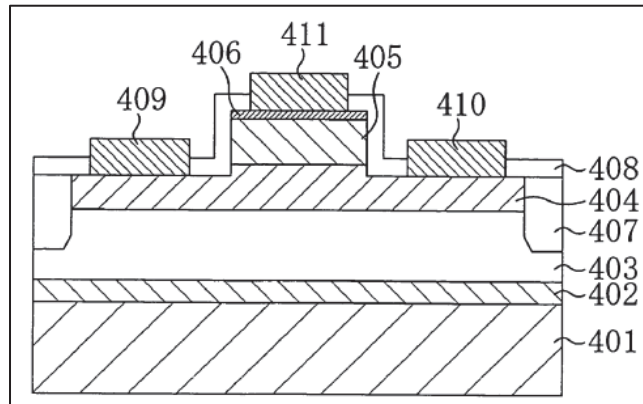
Last, “the photoresist layer 13 is stripped off and the resultant structure is subjected to a low temperature anneal step,” *Id.* at [0049].

Figure 1E shows the results of this final etching step. There now exists a defined gate contact 15 and an ohmic contact 17, **both formed in a single step.**

C. Hikita-347

Hikita-347 discloses an enhancement-mode GaN transistor for use in consumer-electronic products. Ex. 1007 at [0001] and [0011]. *Hikita-347*’s enhancement-mode GaN transistor includes a substrate 401, an AlN buffer layer 402, an undoped GaN layer 403, an undoped AlGaIn layer 404, and a p-type AlGaIn layer 405, a heavily doped p-type GaN layer 406, a gate electrode 411,

source electrode 409, and drain electrode 410. Id. at [0048]. An exemplary embodiment of *Hikita-347* is presented in the following figure:

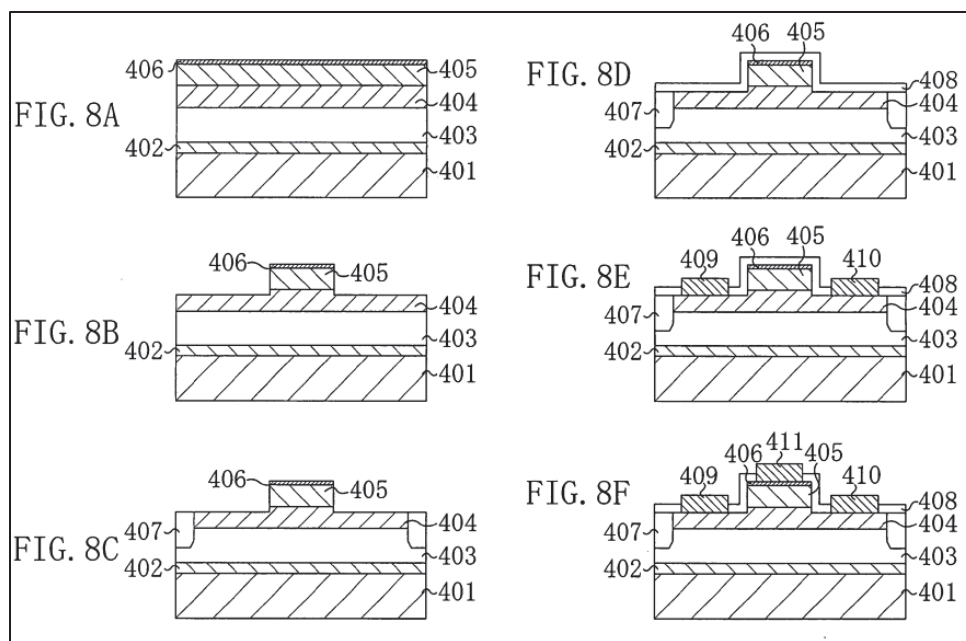


Ex. 1007 at Fig. 4.

Notably, *Hikita-347* corresponds to the enhancement mode device identified in Fig. 1 of the ‘508 patent as “Prior Art”. Compare Fig. 4 of *Hikita-347* with Fig. 1 of the ‘508 patent.

Hikita-347 also discloses an additional transistor structure that only has a single p-type layer 105, the equivalent to 405 above, rather than two doped p-type GaN layers 405 and 406 as shown in Figure 4 above. *See* Ex. 1007 at [0040] (explaining that “it is not necessary that the heavily doped p-type GaN layer 106 is provided”).

Hikita-347 also describes the process to form the GaN transistors of Figure 4. *See* Ex. 1007 at [0055]-[0061]. This process is shown in Figures 8A-8F below.



Ex. 1007 at Figs. 8A-8F.

First, as shown in Figure 8A, an AlN buffer layer 402, an undoped GaN layer 403, an undoped AlGaIn layer 404, a p-type AlGaIn layer 405, and an optional heavily doped p-type GaN layer 406 are formed on a sapphire substrate. *See* Ex. 1007 at [0040] and [0056].

Second, as shown in Figure 8B, the heavily doped p-type GaN layer 406, the p-type AlGaIn layer 405 and an upper portion of the undoped AlGaIn layer 404 are etched. *See* Ex. 1007 at [0035], [0057].

Third, as shown in Figure 8C, an isolation region 407 is formed by implanting boron into parts of the undoped AlGaIn layer 404 and undoped GaN layer 403, blocking the remaining regions of the device with photoresist, as in Figure 8C. *See* Ex. 1007 at [0058].

Fourth, as shown in Figure 8D a SiN film 408 is formed to cover the upper surface of the wafer. *See* Ex. 1007 at [0059].

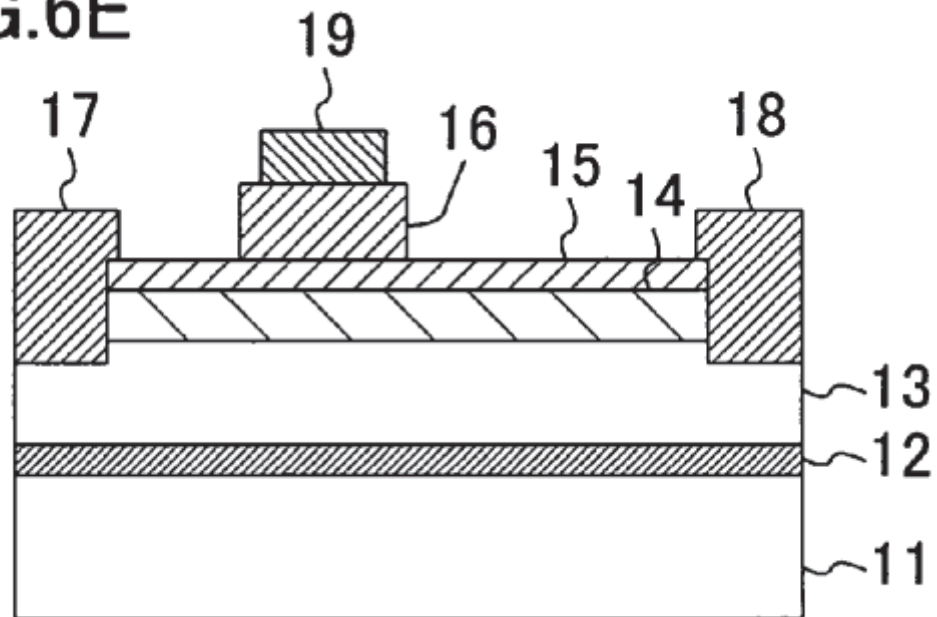
Fifth, as shown in Figure 8E, openings are formed in the SiN film 408. Then, a source electrode 409 and a drain electrode 410 are formed within these openings, followed by a heat treatment in an N₂ atmosphere at 650° C. *See* Ex. 1007 at [0060].

Last, after the source and drain contacts have been fully formed as shown in Figure 8F, an opening is created in the upper surface of SiN film 408 above the p-type semiconductor layers 405 and 406. A gate electrode 411 is formed in the opening. *See* Ex. 1007 at [0061]. Thus, *Hikita-347* is another example of a “gate last” process.

D. Hikita-023

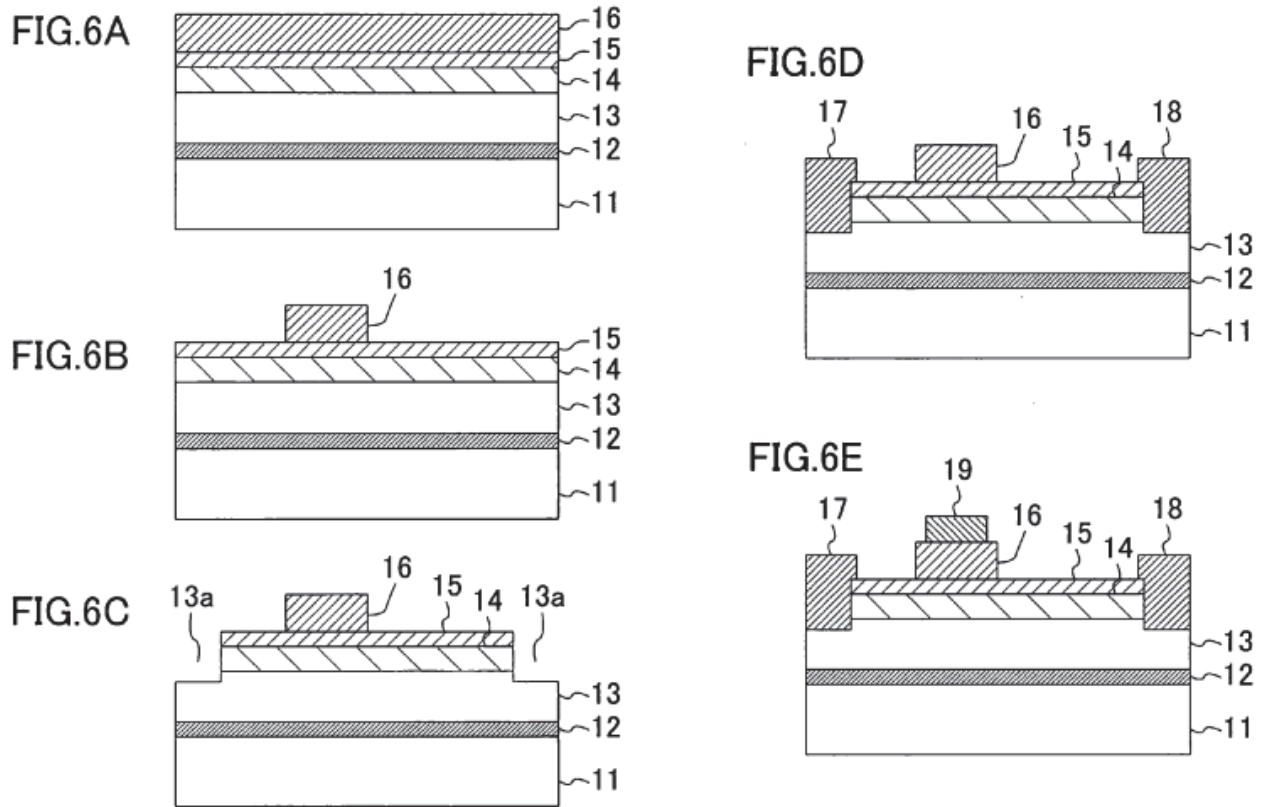
Hikita-023 discloses an enhancement-mode GaN transistor for use in consumer-electronic products. Ex. 1008 at [0014] and [0037]. *Hikita-023*’s enhancement-mode GaN transistor includes a substrate 11, a buffer layer 12, a channel layer 13, an undoped GaN barrier layer 14, a p-type AlGaIn layer 15, and a p-type GaN layer 16, source electrode 17, and drain electrode 18, and a gate electrode 19. *Id.* at [0076]-[0080]. An exemplary embodiment of *Hikita-023* is presented in the following figure:

FIG.6E



Ex. 1008 at Fig. 6E.

Hikita-023 also describes the process to form the GaN transistors of Figure 4. *See Hikita-023* at [0055]-[0061]. This process is shown in Figures 8A-8F below.



Ex. 1008 at Figs. 6A-8E.

First, as shown in Figure 6A, a buffer layer 12, a channel layer 13, an undoped GaN barrier layer 14, a p-type AlGaIn layer 15, and a p-type GaN layer 16, are formed on a substrate 11. *See* Ex. 1008 at [0076].

Second, as shown in Figure 6B, the p-type GaN layer 16 is etched. *See id.* at [0077].

Third, as shown in Fig. 6C, the “p-type AlGaIn layer 15, the barrier layer 14, and the upper portion of the channel layer 13 are selectively removed to form recesses 13a serving as source and drain electrode formation regions in the epitaxial layer.” *Id.* at [0078].

Fourth, as shown in Figure 6D, the source electrode 17 and drain electrode 18 are formed by a liftoff method. *See Id.* at [0079].

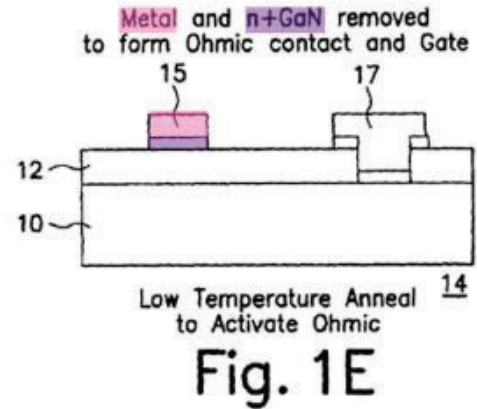
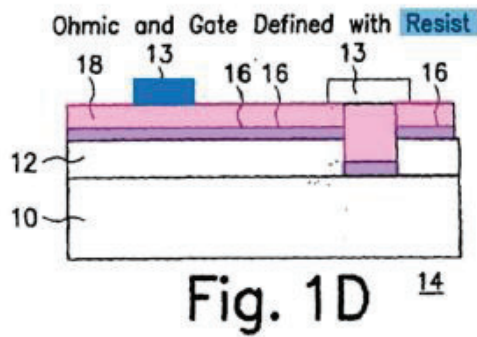
Lastly, **after** the source and drain contacts have been fully formed as shown in Figure 6D, as shown in Figure 6E, the gate electrode 19 is formed on the p-type GaN layer 16 by a liftoff method. *See Ex. 1008* at [0080]. Thus, *Hikita-023* is another example of a “gate last” process.

V. The Board Should Deny Institution of Ground 1

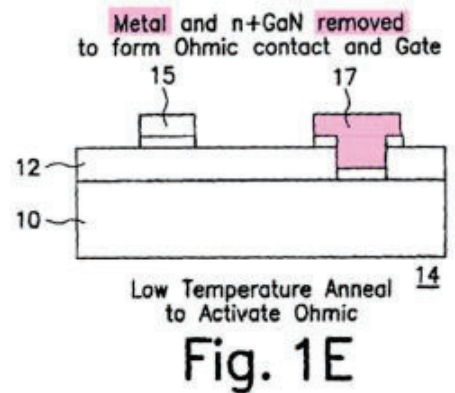
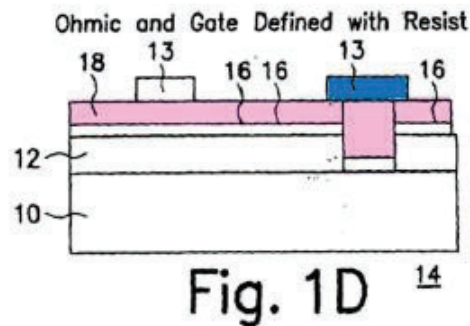
A. Petitioner has not established that *Yoshida*, alone or in combination with *Beach* and *Sheppard*, does teaches both a “gate photo resistant pattern” and a “metal photo resistant pattern” as required by claim 1

Petitioner concedes that *Yoshida* does not disclose the claimed “applying a gate photo resistant pattern” and the claimed “applying a metal photo resistant pattern.” *See* Petition at 30-33 and 35-39, respectively. Instead, Petitioner alleges that *Beach* discloses these steps, and that it renders obvious the claimed elements missing from *Yoshida*. *See id.* Petitioner is incorrect.

In *Beach*, the Petitioner points to the same photoresist 13 as the evidence for both the “gate photo resistant pattern” and “metal photo resistant pattern.” Petition at 32-33 and 36-37. Specifically, Petitioner has provided the following annotated figures which make clear that it is referring to a single element of Beach (photoresist 13), as both the alleged “gate photo resistant pattern” and “metal photo resistant pattern”:



Petition at 33.



Petition at 37.

Furthermore, Petitioner alleges the following:

Second, *Beach* discloses step [1e2], i.e., applying a gate photo resistant pattern 13 (mask) to the structure, as shown below. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17”).

Third, *Beach* discloses step [1e3], i.e., etching away the gate contact layer outside the gate region, and step [1e4], i.e., etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact, as shown below. *Beach*, [0047] (“After the deposition of photoresist layer 13, material 18 is removed, as by etching, except

where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.”).

Petition at 32-33.

First, *Beach* discloses that an ohmic contact metal 18 is deposited in ohmic contact window 11. *Beach*, [0045] (“Material 18 deposited over layer 16 and in ohmic contact window 11 ... may be an ohmic metal”).

Second, *Beach* discloses that a metal photo resistant pattern 13 (mask) is applied over the ohmic contact metal 18. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17.”).

Third, *Beach* discloses that the ohmic contact metal 18 is etched except the portion protected by the mask. *Beach*, [0047] (“After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13.”).

Petition at 36-37.

Thus, Petitioner improperly conflates the use of a single photoresist (13) in *Beach* with the use of a “gate photo resistant pattern” and “metal photo resistant pattern,” which are distinctly claimed in the ’508 patent and correspond to separate photo resistant patterns that are used at different times in the claimed process. For example, the claimed “gate photo resistant pattern” is used to form a gate structure using a single mask. *See* ’508 patent at 3:45-50, claim 1. Separately, the claimed “metal photo resistant pattern,” a different pattern than the “gate photo resistant pattern,” is used as part of the process to form the claimed source and drain contacts, which occurs at a different time than using the “gate photo resistant pattern” to form a gate structure. *See* ’508 patent at 3:64-67, claim 1. A single

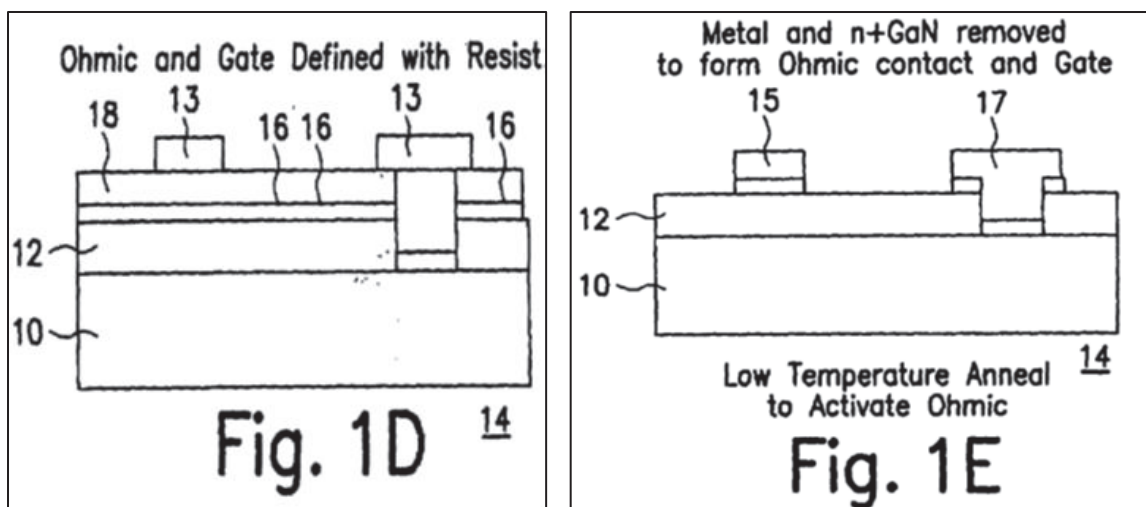
photoresist pattern that is used to simultaneously form a gate and ohmic contacts (which Petitioner equates to the source and drain contacts), such as Beach's photoresist 13, cannot correspond to the separately claimed "gate photo resistant pattern" and "metal photo resistant pattern."

Therefore, for at least the reasons above, Petitioner has not established that *Yoshida*, alone or in combination with *Beach* or *Sheppard* render obvious the claimed "applying a gate photo resistant pattern" and "applying a metal photo resistant pattern" as recited in claim 1 of the '508 patent.

Accordingly, the Board should deny institution of Ground 1.

B. A POSA would not be motivated to combine *Yoshida* and *Beach*

A POSA would not have found it obvious to combine the teachings of *Yoshida* with *Beach* to result in the claimed method, absent hindsight. *Beach*'s teaching of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teachings of *Yoshida*. *Beach*'s simultaneous contact formation process of *Beach* is shown in the figures below.



Ex. 1005, Figs. 1D and 1E.

As seen in these figures, *Beach* discloses a transistor that has a III-N (typically GaN) channel layer (10), and a gate insulator (12). *Beach* forms openings in the gate insulator (12) and deposits a protective layer 16. *See* Ex. 1005 at [0042]-[0043], [0048]. Then, *Beach* deposits a metal layer (18) and forms a photoresist pattern (13) on the metal layer. *See id.* at [0046]-[0047]. These steps result in the device as depicted above in *Beach* Figure 1D.

Subsequently, *Beach* forms the gate and ohmic contacts by etching the metal layer at the same time. *See id.* at [0048]. Notably, *Beach* forms both the gate and ohmic contacts from the same metal material layer 18. *See id.*

Conversely, *Yoshida* forms the drain and source contacts *before* the formation of a gate electrode. *See* Ex. 1004 at [0021]-[0023]. As such, *Yoshida* discloses a “gate-last” process, in which the gate is fabricated after the source and drain contacts have been fabricated. Both the simultaneous gate/ohmic contact

formation of *Beach* and the “gate last” process of *Yoshida* are dramatically different from the “gate first” process of the ‘508 patent. Petitioner has provided no motivation as to why a POSA would combine a “gate last” process, like *Yoshida*, with the simultaneous gate/ohmic formation process of *Beach* to result in a “gate first” process, as disclosed and claimed by the ‘508 patent. *Personal Web Technologies v. Apple*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) ([Petitioner] conten[ds] that a person of ordinary skill in the art reading [two references] would have understood that the combination of [them] would have allowed for the selective access features of [one reference] to be used with [the other reference’s] content-dependent identifies feature. But that reasoning seems to say no more than that a skilled artisan, once presented with two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.) (quotations omitted).

Therefore, for at least the reasons discussed above, the Board should deny institution of Ground 1.

VI. The Board Should Deny Institution of Ground 2

- A. *Hikita-347*, alone or in combination with *Beach* and *Sheppard*, does not teach both a “gate photo resistant pattern” and a “metal photo resistant pattern” as required by claims 1 and 4**

Petitioner concedes that *Hikita-347* does not disclose the claimed “applying a gate photo resistant pattern” and the claimed “applying a metal photo resistant pattern.” *See* Petition at 56-58 and 60-61, respectively. Instead, Petitioner alleges that *Beach* discloses these steps, and that it renders obvious the claimed elements missing from *Hikita-347*. *See id.* Petitioner is incorrect.

Just as it has done in Ground 1, Petitioner points to the same photo resist pattern (13) as the evidence for both the “gate photo resistant pattern” and “metal photo resistant pattern.” Petition at 61.

Thus, similar to Ground 1, Petitioner improperly conflates the use of a single photoresist (13) in *Beach* with the use of a “gate photo resistant pattern” and “metal photo resistant pattern,” which are distinctly claimed in the ‘508 patent and correspond to separate photo resistant patterns that are used at different times in the claimed process. For example, the claimed “gate photo resistant pattern” is used to form a gate structure using a single mask. *See* ‘508 patent at 3:45-50, 4:41-44, claims 1 and 4. Separately, the claimed “metal photo resistant pattern,” a different pattern than the “gate photo resistant pattern,” is used as part of the process to form the claimed source and drain contacts, which occurs at a different time than using the “gate photo resistant pattern” to form a gate structure. *See* ‘508 patent at 3:64-67, 4:49-52, claims 1 and 4. A single photoresist pattern that is used to simultaneously form a gate and ohmic contacts (which Petitioner equates to the

source and drain contacts), such as Beach’s photoresist 13, cannot correspond to the separately claimed “gate photo resistant pattern” and “metal photo resistant pattern.”

Therefore, for at least the reasons above and for those provided above in conjunction with Ground 1, Petitioner has not established that *Hikita-347*, alone or in combination with *Beach* or *Sheppard* render obvious the claimed “applying a gate photo resistant pattern” and “applying a metal photo resistant pattern” as recited in claims 1 and 4 of the ’508 patent.

Accordingly, the Board should deny institution of ground 2.

B. A POSA would not be motivated to combine *Hikita-347* and *Beach*

A POSA would not have found it obvious to combine the teachings of *Hikita-347* with *Beach* to result in the claimed method, absent hindsight. *Beach*’s teaching of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teachings of *Hikita-347*.

Conversely, *Hikita-347* forms the drain and source contacts *before* the formation of a gate electrode. *See* Ex. 1007 at [0059]-[0061] and Figures 8D-8F. As such, *Hikita-347* discloses a “gate-last” process, in which the gate is fabricated after the source and drain contacts have been fabricated. Both the simultaneous gate/ohmic contact formation of *Beach* and the “gate last” process of *Hikita-347* are dramatically different from the “gate first” process of the ’508 patent.

Petitioner has provided no motivation as to why a POSA would combine a “gate last” process, like *Hikita-347*, with the simultaneous gate/ohmic formation process of *Beach* to result in a “gate first” process, as disclosed and claimed by the ‘508 patent. *Personal Web Technologies v. Apple*, 848 F.3d at 993-94.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 2.

VII. The Board Should Deny Institution of Ground 3

A. *Hikita-023*, alone or in combination with *Beach* and *Sheppard*, does not teach both a “gate photo resistant pattern” and a “fourth photo resistant pattern” as required by claim 5

Petitioner concedes that *Hikita-023* does not disclose the claimed “applying a gate photo resistant pattern” and the claimed “applying a fourth photo resistant pattern.” See Petition at 84-86 and 89-90, respectively. Instead, Petitioner alleges that *Beach* discloses these steps, and that it renders obvious the claimed elements missing from *Hikita-023*. See *id.* Petitioner is incorrect.

Just as it has done in Grounds 1 and 2, Petitioner points to the same photo resist pattern (13) in *Beach* as the evidence for both the “gate photo resistant pattern” and “fourth photo resistant pattern.” Petition at 84-86 and 89-90.

Thus, similar to Grounds 1 and 2, Petitioner improperly conflates the use of a single photoresist (13) in *Beach* with the use of a “gate photo resistant pattern” and “fourth photo resistant pattern,” which are distinctly claimed in the ‘508 patent

and correspond to separate photo resistant patterns that are used at different times in the claimed process. For example, the claimed “gate photo resistant pattern” is used to form a gate structure using a single mask. *See* ‘508 patent at 5:4-8, claim 5. Separately, the claimed “fourth photo resistant pattern,” a different pattern than the “gate photo resistant pattern,” is used as part of the process to form the claimed source and drain contacts, which occurs at a different time than using the “gate photo resistant pattern” to form a gate structure. *See* ‘508 patent at 3:64-67, 4:49-52, 5:13-15, claim 5. A single photoresist pattern that is used to simultaneously form a gate and ohmic contacts (which Petitioner equates to the source and drain contacts), such as Beach’s photoresist 13, cannot correspond to the separately claimed “gate photo resistant pattern” and “fourth photo resistant pattern.”

Therefore, for at least the reasons above and for those provided above in conjunction with Grounds 1 and 2, Petitioner has not established that *Hikita-023*, alone or in combination with *Beach* or *Sheppard* render obvious the claimed “applying a gate photo resistant pattern” and “applying a fourth photo resistant pattern” as recited in claim 5 of the ‘508 patent.

Accordingly, the Board should deny institution of Ground 3.

B. A POSA would not be motivated to combine *Hikita-023* and *Beach*

A POSA would not have found it obvious to combine the teachings of *Hikita-023* with *Beach* to result in the claimed method, absent hindsight.

Beach’s teaching of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teachings of *Hikita-023*.

Conversely, *Hikita-023* forms the drain and source contacts *before* the formation of a gate electrode. *See* Ex. 1008 at [0075]-[0080], Figs. 6A-6E. As such, *Hikita-023* discloses a “gate-last” process, in which the gate is fabricated after the source and drain contacts have been fabricated. Both the simultaneous gate/ohmic contact formation of *Beach* and the “gate last” process of *Hikita-023* are dramatically different from the “gate first” process of the ‘508 patent. Petitioner has provided no motivation as to why a POSA would combine a “gate last” process, like *Hikita-023*, with the simultaneous gate/ohmic formation process of *Beach* to result in a “gate first” process, as disclosed and claimed by the ‘508 patent. *Personal Web Technologies v. Apple*, 848 F.3d at 993-94.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 3.

VIII. RESERVATION OF RIGHTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if IPR is instituted. Similarly, Patent Owner does not concede any underlying contentions in the Petition and reserves the right to rebut any such contention later. Further, Patent

Owner is not limited to the arguments presented in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented herein.

IX. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

Dated: December 21, 2023

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER's PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 4843 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

Dated: December 21, 2023

Respectfully submitted,

/s/ Walter D. Davis, Jr.

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

Innoscience-EPC-IPRs@finnegan.com

Dated: December 21, 2023

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing ***Complainant's Responsive Post-Hearing Brief*** was served upon the following as indicated below on March 29, 2024:

The Honorable Lisa R. Barton Secretary to the Commission U.S. INTERNATIONAL TRADE COMMISSION 500 E Street, S.W. Washington, DC 20436	VIA ELECTRONIC FILING EDIS
The Honorable Clark S. Cheney Administrative Law Judge U.S. INTERNATIONAL TRADE COMMISSION 500 E Street, S.W. Washington, DC 20436	VIA BOX, NOTIFICATION VIA EMAIL Cheney1366@usitc.gov
Commission Investigative Attorney: R. Whitney Winston, Esq. Office of Unfair Import Investigations U.S. INTERNATIONAL TRADE COMMISSION 500 E Street, S.W. Washington, DC 20436	VIA ELECTRONIC MAIL Whitney.Winston@usitc.gov
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