

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY AND

INNOSCIENCE AMERICA, INC.,

Petitioner

v.

EFFICIENT POWER

CONVERSION CORPORATION,

Patent Owner

Case No. IPR2023-01381

U.S. Patent No. 8,350,294

**SUPPLEMENTAL DECLARATION OF JAMES RICHARD SHEALY,
PH.D. IN SUPPORT OF PETITIONER'S OPPOSITION TO PATENT
OWNER'S MOTION TO AMEND**

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I. INTRODUCTION

[01] I have been retained by Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively "Innoscience"), as an independent expert for the above-identified inter partes review proceeding involving U.S. Patent No. 8,350,294 ("the '294 patent").

[02] I submitted a first declaration in this matter in connection with Innoscience's Petition (Paper No. 1). My first declaration is marked as Ex. 1003. Since submitting my first declaration, Patent Owner ("EPC") filed its Preliminary Response (Paper No. 8) and the Board instituted an *inter partes* review for the '294 patent (Paper No. 11).

[03] Following institution, I was deposed on May 31, 2024. A transcript of my deposition is marked as Ex. 2012. And EPC submitted a response to the Board's Institution Decision, which included a declaration by Dr. E. Fred Schubert. EPC's Response is marked as Paper No. 18 and Dr. Schubert's declaration is marked as Ex. 2009. EPC also submitted a "Motion to Amend under 35 U.S.C. §316(d) and 37 C.F.R. §42.121," which is marked as Paper No. 17. In the Motion to Amend, EPC asks for "claims 4-6 and 10-12 be cancelled and that proposed new claims 13-14 be entered." Paper No. 17, 1.

[04] I also prepared a supplemental declaration in support to Innoscience's Reply to EPC's response. That supplemental declaration is marked as Ex. 1033.

[05] In this supplemental declaration in support of Innoscience's opposition to EPC's motion to amend I provide below my opinions regarding EPC's proposed new claims 13 and 14. I incorporate by reference the analysis I provided in my declaration accompanying the Petition (Ex. 1003) in its entirety, including my understanding of legal standards (Section V), which I also apply herein.

II. LEGAL STANDARDS

[06] As noted in my first declaration, I am not a lawyer. Ex. 1003 §V. My understanding of the legal standards to apply for my opinions are based on discussions based with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in these proceeding. In my first declaration, I described the legal standards for level of ordinary skill, obviousness, and anticipation. Ex. 1003 §V. In preparing this declaration, I was also informed of other legal standards for the "written description" and "enablement" requirements under 35 USC §112.

A. Written Description Requirement

[07] I have been informed that to be valid claims must comply with a "written description requirement" from 35 USC §112. Under this requirement a

patent specification must describe the claimed invention in sufficient detail that a person of ordinary skill in the art would have reasonably concluded that the inventor possessed the claimed invention as of the effective filing date or date of invention.

[08] I understand that the level of detail required varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology. Complex, unpredictable, or counterintuitive technology require higher disclosure than technology involving predictable factors.

[09] I further understand that a patent specification does not have to describe every conceivable and possible future embodiment of the claimed invention. However, I understand that the patent specification must have sufficient description to demonstrate that the inventor possessed, and actually invented, the claimed subject matter.

B. Enablement Requirement

[010] I understand that a claimed invention must be enabled. A claimed invention is not enabled and, therefore, unpatentable, if the specification does not teach those of ordinary skill in the art how to make and use the full scope of the claim without undue experimentation as of either the effective filing date of the invention or the date of invention.

[011] I understand that I may consider one or more of the following factors in determining whether a person of ordinary skill would have required undue experimentation to make and use the full scope of the claimed invention: (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims.

[012] I understand that the purpose of the enablement requirement is, in part, to ensure that the invention is communicated to the interested public in a meaningful way.

C. The Enablement Requirement Standard is Different From the Obviousness Standard

[013] I understand that the standard to show a claim is not enabled is different from the standard to show a claim is obvious in view of the prior art. A claimed invention can be not enabled and also obvious in view of the prior art because the two invalidity inquiries focus on different standards.

[014] Enablement asks whether a POSITA can make and use the full scope of the invention as claimed. Because the enablement inquiry looks to the full scope of the claim it is possible that the prior art could render an embodiment that falls

within the scope of the claim obvious, but that prior art viewed with the teachings of the patent may still not enable the full scope of the claim. For example, an embodiment disclosed in the prior art and falling within the scope of the claim render the claim invalid as obvious. But, simultaneously, if the teachings of the patent when viewed with the invalidating prior art do not teach a POSITA how to practice the full scope of the claim, the claim can also be invalid for lack of enablement.

[015] Therefore, I have been informed, that a finding of non-enablement is not inconsistent with a finding of obviousness since the two invalidity inquiries focus on different standards, i.e., the specification must enable the full scope of the claim compared to only needing to show that the prior art renders obvious at least one embodiment falling anywhere within the scope of the claim. Therefore, it is possible for a claim to be obvious because of various prior art references while still non-enabled given deficiencies in the specification.

[016] Also, I have been informed that a claim can be not enabled and also obvious in view of prior art when the prior art has comparable (or exceeding) disclosure as the patent specification. I understand that while the specification must enable the full scope of the claim (e.g., each and every possible combination as claimed), the claim is obvious in view of prior art when the prior art renders

obvious even one alternative. And I understand that prior art should be presumed to be operable and enabling and the prior art need not show proof of its efficacy.

III. PROPOSED AMENDED CLAIMS

[017] In its Motion to Amend (Paper No. 17), Patent Owner proposes the following amendments. Claim 13 is a substitute for claim 4.

[13p] An enhancement mode [A] column III nitride transistor comprising:

- [13a] a substrate,
- [13b] a set of III-N transition layers above the substrate,
- [13c] a III-N buffer layer above the set of transition layers,
- [13d] a III-N barrier layer above the buffer layer, [and]
- [13e.1] a semi-insulating III-N layer above the barrier layer, [13e.2] wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
- [13f] a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

[018] Claim 14 is a substitute for claim 10.

[14p] A compensated gate enhancement mode MISFET transistor comprising:

- [14a] a III-N barrier layer beneath a gate contact,
- [14b] a drain contact, a source contact, and
- [14c.1] a semi-insulating III-N layer between the barrier layer and the gate contact, [14c.2] wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
- [14d] a gate comprising the gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

[019] In my opinion, these claims are invalid over the prior art because, as I further discuss below, to a POSITA claims 13 and 14 would have been obvious in view of the prior art and the POSITA's knowledge and the level of skill.

[020] I also find that the claims fail to meet the written description requirement and the enablement requirement. As I further discuss below, the new claims would not meet the written description requirement because the '294 patent does not provide sufficient description to inform a POSITA that the inventors had possession of the devices in new claims 13-14 when the application was filed. Further, as I also discuss below, the new claims would not meet the enablement requirement because the '294 patent does not include sufficient information regarding the subject matter of the claims to enable a POSITA to make and use the full scope of the inventions in the new claims. For example, the '294 patent fails to

inform a POSITA that the inventors had possession of an “enhancement mode” transistor, with a “semi-insulating III-N layer comprises a compensated GaN layer,” and “wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.” The specification in the '294 patent also fails to teach a POSITA how to make and/or use such device without undue experimentation because the '294 patent is silent regarding critical parameters that a POSITA would have need to know to implement claims 13-14.

IV. LEVEL OF ORDINARY SKILL IN THE ART

[021] Like for my first declaration, marked as Ex. 1003, I was asked to render opinions about new claims 13 and 14 through the eyes of a person of ordinary skill in the art (“POSITA”). The opinions I render here are through the eyes of the POSITA I defined in my first declaration. Ex. 1003 ¶53.

[022] I understand Dr. Schubert proposed a level of ordinary skill for the '294 patent that differs from the one I proposed in my first declaration. Ex. 2009 ¶¶81-83. He defined a person of ordinary skill in the art as:

a graduate having a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN. Moreover, relevant graduate

education could substitute for the professional work experience.

Ex. 2009 ¶82.

[023] As I noted in my supplemental reply declaration marked Ex. 1033, however, the two definitions are very similar. Ex. 1033 ¶¶6-8. While I continue to find my definition more appropriate given the scope and description of the '294 patent, my analysis and opinions regarding the new claims 13 and 14 would not depend on the differences between the two definitions. As Dr. Schubert seems to agree, the differences in the level of ordinary skill in the art between the two definitions would not change the outcome of the invalidity analysis in any material manner. Ex. 2009 ¶83.

V. THE PROPOSED AMENDED CLAIMS ARE NOT SUPPORTED BY THE WRITTEN DESCRIPTION, BROADEN THE MEANING OF “SEMI-INSULATING LAYER,” AND WOULD HAVE REQUIRED UNDUE EXPERIMENTATION

A. The Patent Lacks Written Description Support for “Wherein the Semi-insulating III-N Layer Comprises a Compensated GaN Layer Containing Acceptor Type Dopant Atoms Passivated With Hydrogen”

[024] In my opinion, proposed new claims 13 and 14 lack written description support for a “semi-insulating III-N layer [that] comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen.” Paper 17, 4-7. Nowhere does the '294 patent describe a “semi-

insulating III-N layer” that comprises a “compensated GaN layer.” Instead, the ’294 patent describes two different and separate layers—a semi-insulating layer (described in the patent as “semi-insulating layer 39”) and a compensated layer (described in the patent as a different layer, “compensated layer 38”). The patent provides no support for a “semi-insulating layer” that comprises, or includes within it, a “compensated layer.”

[025] The patent describes the two layers differently and not interchangeably. The field of invention plainly distinguishes the terms, stating “the invention relates to an enhancement mode GaN transistor with a compensated GaN layer *or* a semi-insulating GaN layer below the gate contact and above the barrier layer.” Ex. 1001, 1:14-17 (emphasis added). The summary of the invention makes the same distinction, describing two embodiments, one “with a compensated GaN layer” and “another . . . employing a semi-insulated layer.” Ex. 1001, 2:11-19.

[026] Throughout, the ’294 patent maintains these layers as separate and different. For Figures 2 to 9 and accompanying text, the patent only depicts and describes “compensated semiconductor layer 38” without mentioning a “semi-insulating III-N layer.” Ex. 1001, 2:56-3:52. In contrast, Figures 10 to 13 and associated text disclose a “second embodiment” whose defining feature is “a semi-insulating layer 39 *in place of* the compensated semiconductor layer 38.” Ex. 1001,

3:53-4:29 (emphasis added). The patent again distinguishes compensated and semi-insulating in the “third embodiment” of Figures 14 to 15, which contains a “semi-insulating layer 39” without mentioning compensated layer. Ex. 1001, 4:30-63. The final embodiment in Figure 16 likewise includes a “semi-insulating layer” without a compensated layer. Ex. 1001, 4:64-5:2, Fig. 16.

[027] The patent never describes an embodiment in which a semi-insulating layer *comprises* a compensated GaN layer as recited in the proposed claims. Paper 17, 4-7. While the '294 patent notes “a GaN transistor may have *both* a semi-insulating layer *and* a compensated semiconductor layer,” Ex. 1001, 3:60-61, the '294 patent clearly describes the two layers as different, not one comprised in another. The '294 patent's description of an embodiment with both semi-insulating and compensated layers does not disclose “the semi-insulating III-N layer *comprises* a compensated GaN layer” as recited in proposed claims 13-14, Paper 17, 4-7 (emphasis added). It describes the opposite, because this passage describes two separate and different layers, consistent with the rest of the specification and claims. Ex. 1001, 3:60-61.

[028] The patent employs different methods to make these layers—with hydrogen passivation for the “compensated layer” but never with passivation for “semi-insulating layer.” *Compare* Ex. 1001, 3:43-52, 5:18-20 (compensated layer)

with Ex. 1001, 3:53-5:2, 5:24-6:5 (semi-insulating layer). Hydrogen passivation distinguishes the compensated layer embodiment of Figures 2-9 from the prior art. Ex. 1001, 3:43-52; *see id.* 5:18-20 (claim 2). “The critical step in the above process that differentiates the device of the present invention from the prior art device (FIG. 1) is the passivation of a p-type impurity using hydrogen” which results in “compensated semiconductor layer 38 [being] a highly compensated semi-insulating material.” Ex. 1001, 3:43-52. In contrast, the '294 patent never describes using hydrogen passivation for the “semi-insulating layer.” Ex. 1001, 3:53-5:2, 3:53-6:2, 6:1-5 (claims 5-6), 6:13-15 (claim 8).

[029] The patent does not explain how to mix and match impurities or overlap “compensated layer” and “semi-insulating layer” such that a “semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen,” as recited in proposed claims 13-14. Instead, the patent consistently describes using different impurities for the two layers.

[030] On one hand, a “[c]ompensated semiconductor layer 38 preferably comprises AlGaN or GaN with a deep level *passivated p-type* impurity such as, for example, *Mg, Zn, Be, Cd, or Ca.*” Ex. 1001, 3:10-12, 5:12-23 (claims 1-3). Thus, when describing a “compensated GaN layer” as having a “passivated p-type

impurity” the patent provides examples from groups IIA and IIB of the periodic table as shown in the table below in **pink**. Those examples are all shallow acceptors and are amenable to passivation, i.e. they introduce holes that can be inactivated.

[031] On the other hand, the patent states “[s]emi-insulating layer 39 may comprise, for example, AlGaN or GaN, with deep level impurity atoms, for example, *C, Fe, Mn, Cr, V, or Ni*.” Ex. 1001, 3:57-59, 5:24-6:5 (claims 4-6). These examples are from groups VB, VIB, VIIB, and IVA of the periodic table as shown below in **blue**. They have deep level traps that prevent mobile charge from traveling in the semi-insulating layer. Passivation has no effect on their ability to prevent mobile charge. Notably, the '294 patent specifies no overlap between the impurity atoms of the “compensated layer” and the impurity atoms of the “semi-insulating layer.”

[032] As highlighted in the below periodic table, the example “semi-insulating layer” impurities and “compensated GaN layer” impurities are from different groups of the periodic table. They have different properties when introduced to a III-N layer—they create holes and can be passivated to prevent mobile charge from flowing (**passivated p-type impurities**), or they have deep level **traps** that prevent charge from flowing.

Passivated p-type impurities

Deep level impurity atoms

Periodic Table of the Elements

1 1A 1A																	18 VIIIA 8A		
2 He																	2		
1 H Hydrogen 1.008	2 He																	17 VIIA	7A
3 Li Lithium 6.941	4 Be Beryllium 9.012																	10 Ne	
11 Na Sodium 22.990	12 Mg Magnesium 24.305																	18 Ar	
19 K Potassium 39.098	20 Ca Calcium 40.078	21 Sc Scandium 44.956	22 Ti Titanium 47.88	23 V Vanadium 50.942	24 Cr Chromium 51.996	25 Mn Manganese 54.938	26 Fe Iron 55.933	27 Co Cobalt 58.933	28 Ni Nickel 58.693	29 Cu Copper 63.546	30 Zn Zinc 65.39	31 Ga Gallium 69.723	32 Ge Germanium 72.61	33 As Arsenic 74.922	34 Se Selenium 78.09	35 Br Bromine 79.904	36 Kr Krypton 84.80		
37 Rb Rubidium 84.468	38 Sr Strontium 87.62	39 Y Yttrium 88.906	40 Zr Zirconium 91.224	41 Nb Niobium 92.906	42 Mo Molybdenum 95.94	43 Tc Technetium 98.907	44 Ru Ruthenium 101.07	45 Rh Rhodium 102.906	46 Pd Palladium 106.42	47 Ag Silver 107.868	48 Cd Cadmium 112.411	49 In Indium 114.818	50 Sn Tin 118.71	51 Sb Antimony 121.760	52 Te Tellurium 127.6	53 I Iodine 126.904	54 Xe Xenon 131.29		
55 Cs Cesium 132.905	56 Ba Barium 137.327	57-71																86 Rn	
87 Fr Francium 223.020	88 Ra Radium 226.025	89-103																118 Uuo	
57 La Lanthanum 138.906	58 Ce Cerium 140.115	59 Pr Praseodymium 140.908	60 Nd Neodymium 144.24	61 Pm Promethium 144.913	62 Sm Samarium 150.36	63 Eu Europium 151.966	64 Gd Gadolinium 157.25	65 Tb Terbium 158.925	66 Dy Dysprosium 162.50	67 Ho Holmium 164.930	68 Er Erbium 167.26	69 Tm Thulium 168.934	70 Yb Ytterbium 173.04	71 Lu Lutetium 174.967					
89 Ac Actinium 227.028	90 Th Thorium 232.038	91 Pa Protactinium 231.036	92 U Uranium 238.029	93 Np Neptunium 237.048	94 Pu Plutonium 244.064	95 Am Americium 243.061	96 Cm Curium 247.070	97 Bk Berkelium 247.070	98 Cf Californium 251.080	99 Es Einsteinium [254]	100 Fm Fermium 257.095	101 Md Mendelevium 258.1	102 No Nobelium 259.101	103 Lr Lawrencium [262]					

[033] Co-inventor Dr. Robert Beach testified in the related ITC investigation on the differences between compensated and semi-insulating layers. That testimony aligns with the description in the '294 patent. When questioned by Chief Administrative Law Judge Cheney during open session, Dr. Beach distinguished “compensated layers” from “semi-insulating layers” described in the '294 patent testifying that while “compensated” layers have hydrogen passivation, “semi-insulating” layers have a “trap approach.” Ex. 1034, 394:12-395:7. On redirect, Dr. Beach testified “semi-insulating focuses more on the resistance” and “something in it is a trap that prevents the charge from moving in the insulator.” *Id.*, 402:7-19.

[034] Dr. Beach's description of “compensated GaN layers” is consistent with the patent's description of using “passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca” to make the compensated GaN layer in the first embodiment. Ex. 1001, 3:10-15, 5:12-23 (claims 1-3). Passivation removes holes from these dopants. For example, hydrogen would react with magnesium to remove a hole.

[035] Dr. Beach's testimony that a “semi-insulating layer” has a “trap approach” is similarly consistent with the patent's description of using “deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni” to make the “semi-

insulating layer” of embodiments 2 through 4. Ex. 1001, 3:57-60, 6:6-15 (claims 7-8). These dopants have traps, which can capture a holes from the valence band. As a result, holes cannot travel in the semi-insulated layer and it has a high resistivity, just like Dr. Beach testified when he said “something in it is a trap that prevents the charge from moving in the insulator.” Ex. 1034, 402:7-19. A semi-insulating layer of the patent is not passivated.

[036] Further, the '294 patent acknowledges that the second embodiment with a semi-insulating layer “is not as sensitive to future processing steps involving hydrogen and/or high temperatures” as compared to the first embodiment with a compensated GaN layer. Ex. 1001, 3:63-4:3. This too aligns with Dr. Beach's and the patent's description that the semi-insulating layer contains dopants that have traps while the compensated GaN contains dopants that are passivated. While both approaches increase resistivity and decrease conductivity, they have clearly distinct approaches and characteristics. As the patent admits, only the resistivity of a compensated GaN is sensitive to “steps involving hydrogen and/or high temperatures” because those steps influence passivation. Hydrogen passivates dopants like Mg to remove holes. High temperature processing steps cause hydrogen to diffuse out, thereby decreasing passivation. In contrast, the ability of “deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni” to remove

mobile charge from the layer using traps is unaffected by hydrogen or high temperature during post-epitaxy processing steps.

[037] The following table summarizes the above differences between a “semi-insulating layer” and “compensated GaN layer.”

Compensated GaN Layer	Semi-Insulating Layer
Embodiment 1: Figures 2-9, Ex. 1001, 2:56-3:52, claims 1-3.	Embodiments 2-4: Figures 10-14, Ex. 1001, 3:53-5:2, claims 4-12.
Passivated	No Passivation
Contains “passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca.” Ex. 1001, 3:10-15, claims 1-3.	Contains “deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni.” Ex. 1001, 3:57-60, claims 7-8.
“sensitive to future processing steps involving hydrogen and/or high temperatures.” Ex. 1001, 3:63-4:3.	“not as sensitive to future processing steps involving hydrogen and/or high temperatures.” Ex. 1001, 3:63-4:3.
Inventor testimony hydrogen passivation prevents mobile charge in layer. Ex. 1033, 394:12-395:7, 402:7-19.	Inventor testimony “trap approach” prevents mobile charge in layer. Ex. 1033, 394:12-395:7, 402:7-19.

[038] In my opinion, the proposed claims accordingly lack written description support for a “semi-insulating III-N layer [that] comprises a compensated GaN containing acceptor type dopant atoms passivated with hydrogen” because the amendments mix layers that the '294 patent solely describes as separate and different.

B. The Amendments Broaden the Claims by Expanding the Scope of “Semi-insulating III-N Layer” to Include “Compensated Layer”

[039] In my opinion, the proposed amendments broaden the meaning of “semi-insulating III-N layer” expanding the term to include a “compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen” for the same reasons discussed for lack of written description support (see above §V.A).

[040] I see that EPC noted in its Motion to amend that the patent states “compensated semiconductor layer 38 is a highly compensated semi-insulating material” to allege the amendments do not broaden the claim. Paper 17, 3; Ex. 1001, 3:43-52. I disagree.

[041] Viewed in full, the cited passage only describes the compensated GaN layer is not a conductive *material* like prior art devices: “in GaN transistor 1, the compensated semiconductor layer 38 is a highly compensated *semi-insulating material*, while in GaN transistor 100 of the prior art, layer 105 is a *conductive* p-

type material.” Ex. 1001, 3:43-52 (emphasis added). That the “compensated layer 38” has the electrical property of being a “semi-insulating *material*” does not mean it is, or is a part of, the “semi-insulating *layer* 39,” which the patent describes separately and distinctly from “compensated semiconductor *layer* 38.” See above §V.A. A POSITA would have understood from “compensated semiconductor layer 38 is a highly compensated semi-insulating material” that the compensated layer has characteristics of a semi-insulating *material*: i.e., it is a material with a high resistivity. A POSITA would not understand that this passage equates the “compensated layer” and “semi-insulating layer” because the patent distinguishes “layer” from “material,” and describes the compensated layer and semi-insulating layer as being different *layers* with different characteristics and different chemical species, as I discuss above. See above §V.A. When the patent discloses a “semi-insulating III-N layer,” it never describes that this layer would “comprise[] a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen.” See above §V.A. The amendment broadens the scope of the term “semi-insulating III-N layer” to include a layer that includes a “compensated GaN layer.” In my opinion, the '294 patent does not support such broadening of “semi-insulating III-N layer” to include a different compensated layer. Indeed, as I discussed above, there is no reason to passivate the “deep level impurity atoms, for

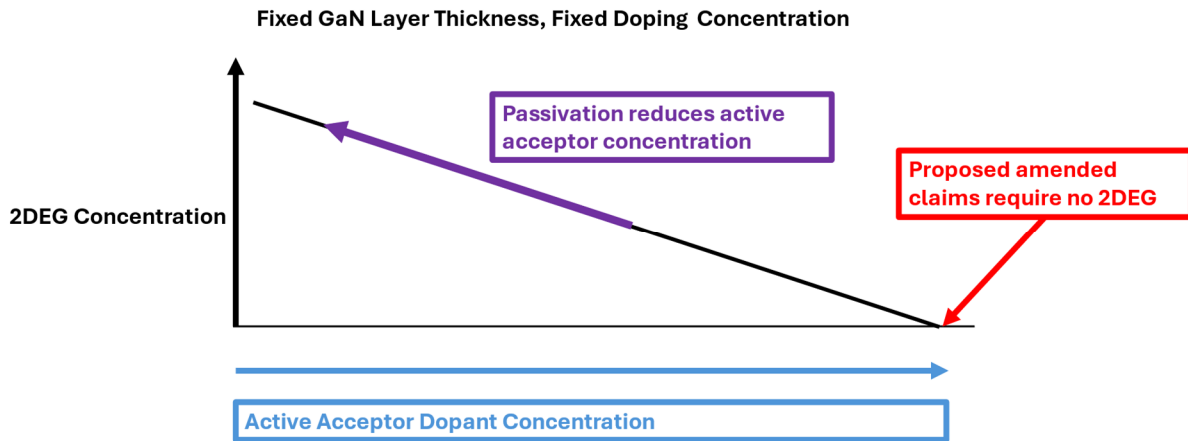
example, C, Fe, Mn, Cr, V, or Ni” of the semi-insulating layer because those atoms already prevent mobile charge from moving in the layer with its trap approach.

C. The Patent Specification Fails to Adequately Disclose to a POSITA How to Make Claims 13 and 14 and Implementing Them Would Require Undue Experimentation

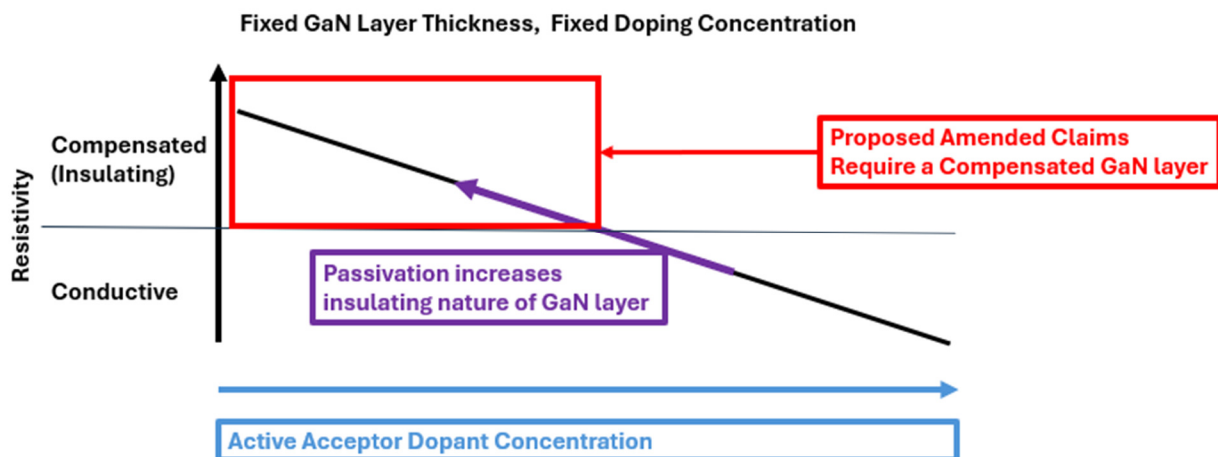
[042] Proposed amended claims 13 and 14 are drawn to an “enhancement mode” transistor that includes a “semi-insulating III-N layer [that] comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen” and has “no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.” Claim 14 additionally requires its device is a “MISFET.” In my opinion, the patent specification fails to adequately disclose how to achieve the claimed combinations without undue experimentation.

[043] First, the '294 patent provides no guidance on key parameter values of the “compensated GaN layer” that control depletion of the 2DEG and control whether the layer is compensated: GaN layer thickness, doping concentration, and the amount of passivation.

[044] Regarding 2DEG depletion, for a given thickness, doping and passivation have competing effects. Higher levels of relative passivation *decrease* the ability of the p-GaN to deplete the 2DEG and thus make it more difficult to achieve an enhancement mode device. This is shown below.



[045] Regarding a “compensated GaN layer,” the ’294 patent explains a “compensated GaN” has an insulating nature, unlike the prior art. Ex. 1001, 3:43-52. Doping and passivation have competing effects on whether the layer is “compensated.” For a given thickness, higher levels of relative passivation *increases* the insulating nature of the GaN layer. This is shown below.



[046] Layer thickness also plays a role in determining the insulating nature of the GaN layer when performing the post-growth passivation step disclosed in the patent. Ex. 1001, 3:37-39 (“An additional hydrogen passivation can be performed by exposing the device to ammonia or hydrogen plasma at a high temperature.”). A thicker layer is more difficult to passivate with hydrogen (as claimed in claims 13-14) and thus more difficult to arrive at a compensated state. This is difficult for an additional reason: in a p-GaN, holes are removed by surface depletion, and as layer thickness increases, at some thickness the surface will not deplete the entire layer and mobile charge (holes) will be introduced.

[047] Claim 14 further requires a MISFET—a Metal Insulator Semiconductor Field Effect Transistor—which requires an insulator in the gate, and the patent discloses a MISFET when the gate structure consists of a gate contact with either a compensated or semi-insulating layer. Ex. 1001, Abstract, 2:13-19, 2:56-3:21, claim 10, Fig. 2. To be an insulator with a compensated layer acceptor type dopants would need to be sufficiently passivated. But to achieve a depleted 2DEG for an enhancement mode device with a p-GaN layer, as required by claim 14, would require active (unpassivated) acceptors.

[048] The patent is silent regarding these multiple parameters and achieving the combinations of features recited in new claims 13-14 would thus have required

undue experimentation. The patent provides no guidance on GaN layer thickness, doping, and passivation to meet the combined goals of depleting the 2DEG to make an enhancement mode device while also being “compensated.” In view of the tradeoffs between doping, passivation, and GaN layer thickness, the '294 patent does not enable how to achieve “no two-dimensional electron gas (2DEG) region [] below the gate at zero volts applied gate bias” when the gate structure also includes a “semi-insulating III-N layer compris[ing] a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen” as recited in claims 13 and 14. The patent likewise does not provide any guidance on how to be a MISFET and enhancement mode.

1. An enhancement mode device would require sufficiently high levels of active acceptor type dopants in the “compensated GaN” to deplete the 2DEG

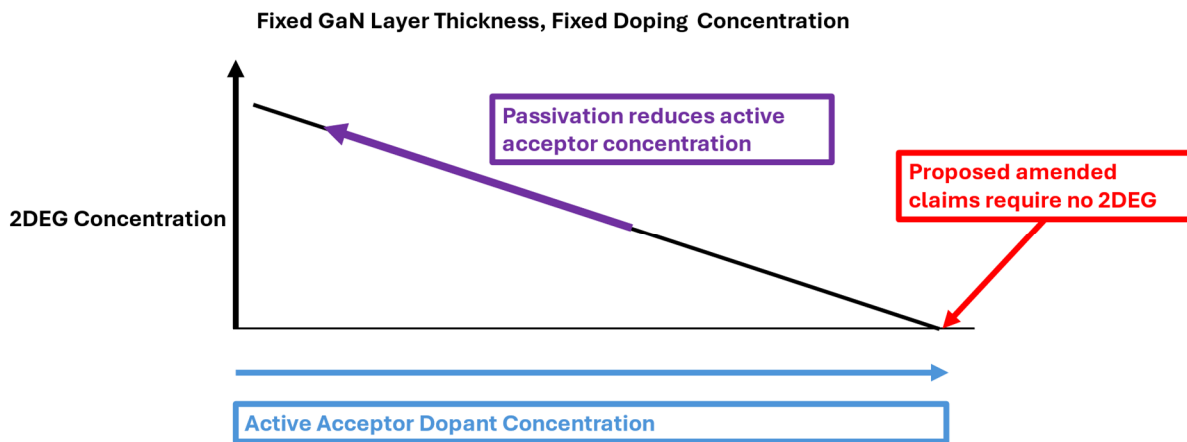
[049] In enhancement mode devices a 2DEG is depleted below the gate at zero volts applied bias. The '294 patent agrees, noting “enhancement mode devices are normally off” and “require[] a positive bias applied at the gate in order to conduct current.” Ex. 1001, 1:50-54. Enhancement mode is achieved when “the 2DEG region is depleted, i.e. removed, below the gate at zero applied gate bias.” Ex. 1001, 1:47-50. Proposed claims 13 and 14 similarly require an “enhancement

mode” transistor with “no two-dimensional electron gas (2DEG) region [] below the gate at zero volts applied gate bias.” Paper 17, 4-7.

[050] At least three parameters of the claimed “compensated GaN layer” govern whether the 2DEG is depleted: its thickness, doping concentration, and concentration of active (unpassivated) acceptor type dopants. This is because the 2DEG can be removed below the gate when the “compensated GaN layer” contains sufficient sheet charge in the form of “acceptor type dopant atoms” that are *not* “passivated with hydrogen.” Dr. Schubert agrees. Ex. 2009 ¶61. When “acceptor type dopant atoms” are “passivated with hydrogen,” they become inactive and do not contribute to the depletion of the 2DEG. The sheet charge of a GaN layer that contains only passivated dopants drops to zero, and it cannot deplete the 2DEG. Without any guidance in the patent, determining the concentration of active acceptor type dopants necessary to achieve the 2DEG depletion would require undue experimentation for a POSITA.

[051] As shown below, doping and passivation have competing effects on the ability of the p-GaN layer to deplete the 2DEG. For a given thickness and total doping concentration, increased passivation reduces the amount of active acceptor type atoms and thus reduces the ability of the p-GaN layer to deplete electrons from the 2DEG. The following figure illustrates the relationship between

passivation and 2DEG concentration for a given magnesium-doped GaN layer with a given thickness and a fixed dopant concentration.



[052] Accordingly, to achieve the claimed “enhancement mode” transistor with no 2DEG below the gate as required in claims 13 and 14, active acceptor concentration must be sufficiently *high* to deplete the 2DEG. The difficulty in achieving this feature is complicated by the fact that there are limits to how heavily the layer can be doped, and to increase the total amount of active acceptor at some point the layer may need to become thicker to account for the high number of dopants atoms. But as the layer becomes thicker, the acceptors are further from the 2DEG and become less effective at depleting it. And a thicker layer is more difficult to passivate with hydrogen. The relationship between active acceptor concentration, total dopant concentration, layer thickness, passivation, and 2DEG

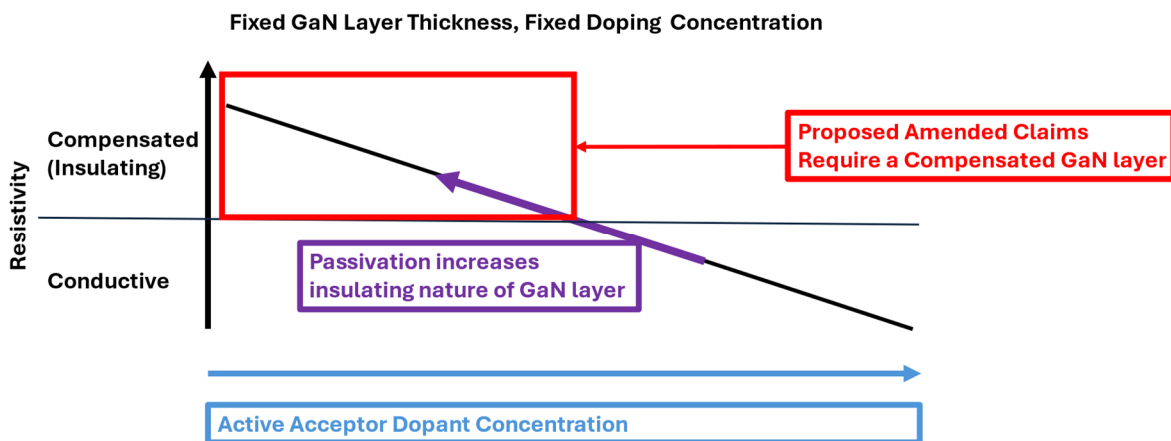
depletion are complex but the patent does not describe any of these principles or how to achieve its goal of depleting the 2DEG. A POSITA would have required much experimentation.

2. A “semi-insulating III-N layer [that] comprises a compensated GaN layer” would require sufficiently high levels of passivated acceptor atoms

[053] In the '294 patent, “compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material.” Ex. 1001, 3:47-49. The '294 patent also states that “the capacitance of the gate electrode to channel layer is reduced in the present invention as compared to the prior art.” Ex. 1001, 3:50-51. EPC has alleged that these disclosures support the limitation of “the semi-insulating III-N layer comprises a compensated GaN layer.” Paper No. 17, 3. As noted above, I disagree that the patent supports this limitation because the patent distinguishes “semi-insulating layer 39,” from “compensated layer 38” and the “semi-insulating material” characteristic. See above §V.A. But, even if these sections of the patent described “the semi-insulating III-N layer comprises a compensated GaN layer” (which I disagree with), they would describe that the “compensated” layer requires a sufficiently high passivation and a low concentration of active acceptor dopants to be “semi-insulating.” However, active acceptors would need to be sufficiently

high to deplete the 2DEG in the claims. The patent does not enable these competing requirements without undue experimentation.

[054] A POSITA knew that GaN layer thickness, doping, and passivation dictate the resistivity (insulating nature) of the GaN layer. Doping and passivation have competing effects on the GaN layer conductivity and whether it has an insulating nature. A high level of activated acceptor dopant concentration leads to increased conductivity (i.e., a conductive layer), while a low activated acceptor dopant concentration results in low conductivity (i.e., an insulating nature/high resistivity). The following figure illustrate the relationship between passivation and resistivity of the GaN layer when holding GaN layer thickness and doping concentration fixed.



[055] Accordingly, to achieve the claimed “enhancement mode” transistor with no 2DEG below the gate of claims 13 and 14, activated acceptor dopant concentration must be sufficiently *low* to be a “semi-insulating III-N layer [that] comprises a compensated GaN layer,” while at the same time achieving “no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias,” as recited in new claims 13 and 14. The patent does not describe how to achieve this combination of features as recited in new claims 13 and 14. Without any guidance in the patent, in my opinion achieving such characteristics would require undue experimentation.

3. The '294 patent does not explain how to achieve the combination of features in claims 13 and 14 without undue experimentation in light of tradeoffs on layer thickness and compensated GaN layer doping considerations in an enhancement mode device

[056] The patent does not provide any guidance on how to achieve the combination of features recited in the new claims 13 and 14 in light of tradeoffs on layer thickness and compensated GaN layer doping considerations in an enhancement mode device. If a POSITA tried to achieve them, it would face technical obstacles that would require undue experimentation.

[057] For example, enhancement mode devices turn on after a positive gate threshold voltage is exceeded. Ex. 1001, 1:53-54. A POSITA knew that in

enhancement mode devices using a p-GaN layer—like the one disclosed in Ex. 1010, in the admitted prior art, and in the '294 patent—it was desirable for the p-GaN layer to be thin, because a thin layer is more effective than a thick layer at modulating the charge in the channel when applying the gate voltage. This is due to the layer electrostatics: negative charge in the layer repels negative charge in the channel. Similarly, to be a “semi-insulating III-N layer [that] comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen” a POSITA would have known that a thin layer is desirable because a thin layer is easier to passivate with hydrogen.

[058] But when a POSITA attempted to make the enhancement-mode device recited in the new claims, it would face a difficult technical obstacle. The desirable thin p-GaN layer would require incredibly high concentrations of dopant to have sufficient charge after passivation to deplete the 2DEG and create an enhancement mode device (e.g., to have sufficient active Mg). That doping would be a very difficult process to achieve (if even possible) and would require much experimentation because the '294 patent does not provide any guidance on how to achieve it. For example, while a POSITA may have attempted to make a thicker p-GaN layer to facilitate doping, the thick layer then becomes less insulating and harder to passivate. And there is an upper limit to layer thickness because thickness

drives the turn on voltage in the wrong direction—a thicker layer can result in a negative turn on voltage. Yet, the patent is completely silent regarding any of these parameters and a POSITA would have faced the competing effect of enhancement mode devices requiring a positive turn on voltage.

[059] The '294 patent is completely silent on any of these interactions between different variables in the device of the new claims 13 and 14. The patent never describes how to balance these tradeoffs and achieve the device of claims 13 and 14. A POSITA seeking to practice the invention as claimed in the new claims 13 and 14 would face undue experimentation.

4. The '294 patent provides no guidance on how to achieve the competing requirements of a transistor that has “semi-insulating III-N layer [that] comprises a compensated GaN layer” and is “enhancement mode” requiring undue experimentation to practice the invention

[060] The patent does not explain to a person of skill how to make a GaN layer that is a “semi-insulating III-N layer [that] comprises a compensated GaN layer” in an “enhancement mode” transistor with no 2DEG under the gate at zero volts. To make such a device, a POSITA would have needed undue experimentation to probe the multi-dimensional parameter space that governs whether a transistor has a “semi-insulating III-N layer [that] comprises a compensated GaN layer” and whether the device is “enhancement mode.” Without

any guidance in the patent, a POSITA would have been required to engage in undue experimentation, varying variables like thickness, conductivity, doping, and passivation in an unguided brute force trial-and-error of multiple variables in an inherently expensive and complex process.

[061] As I explained above, the activated acceptor concentration must be sufficiently *high* to deplete the 2DEG, but it must at the same time be sufficiently *low* to be “compensated.” See above §§V.C.1-V.C.2. More dopant requires a thicker layer, which is more difficult to passivate, but active acceptors in a thick layer are further from the 2DEG and less effective at depleting it. See above §V.C.3. The patent does not explain how to find the appropriate doping, conductivity, passivation, and GaN layer thickness to make the devices of claims 13 and 14.

[062] Regarding the claimed passivation, the '294 patent only suggests to “expos[e] the device to ammonia or hydrogen plasma at a high temperature.” Ex. 1001, 3:30-42. This lack of guidance is especially problematic because hydrogen passivation levels are influenced by many factors, including doping concentration, GaN layer thickness, gas flows, hydrogen exposure time, and temperature. The patent provides none of that information.

[063] In addition, downstream processing steps also influence passivation levels, but the patent is silent as to how such steps affect passivation or how to control the processing steps. The patent does not explain how to account for the effects of, for example, an anneal at high temperature. The patent discusses implementing an anneal, stating “future processing steps involving hydrogen and/or high temperature,” suggesting that the second embodiment with a semi-insulating layer is “less sensitive” to such steps than the “compensated layer” embodiment. Ex. 1001, 3:67-4:5. But hydrogen tends to diffuse out during anneal, thereby reducing the level of passivation. The patent does not describe how to perform such steps, or even how they affect the process, when making an enhancement mode device with a “semi-insulating III-N layer [that] comprises a compensated GaN layer.”

[064] I have been informed that enablement is determined based on the level of ordinary skill as of the application's priority date. And under any of the proposed definitions for a POSITA (see above §IV), it would not have been able to identify the narrow range of GaN layer thickness, doping concentration, conductivity, and passivation level that meet the combination of features in the proposed claims without undue experimentation (if such a range indeed exists). Without guidance from the patent, a POSITA would have needed to engage in

undue experimentation, with hundreds—even thousands—of trial-and-error experiments, testing, and device architectures to attempt to arrive at the claimed device (if ever).

5. The '294 patent does not describe how to make the “compensated gate enhancement mode MISFET” that is passivated with hydrogen as required in claim 14

[065] The new claim 14 requires features of (1) a “MISFET,” (2) “enhancement mode,” (3) contains a “semi-insulating III-N layer [that] comprises compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen.” The patent has not explained how to make such a device. As I will explain below, the patent fails to provide sufficient guidance on how to achieve this combination of features, which presents trade-offs and competing effects, which would have forced a POSITA to engage in undue experimentation to attempt to achieve the claimed combination.

[066] First, MISFET stands for Metal Insulator Field Effect Transistor. A MISFET has an insulating layer below the gate contact, , and the patent discloses a MISFET when the gate structure consists of a gate contact with either a compensated or semi-insulating layer. Ex. 1001, Abstract, 2:13-19, 2:56-3:21, claim 10, Fig. 2.

[067] Second, for an enhancement mode, the 2DEG must be depleted when the gate voltage is 0V. For a p-GaN in an enhancement mode device, the p-GaN must have fixed negative charge in the layer in the form of activated p-type dopants (e.g., Mg). A POSITA knew that 2DEG depletion would require fixed negative charge in the layer below the gate contact (in claim 14 the “semi-insulating III-N layer” that comprises a “compensated GaN layer”). The patent does not describe how to achieve a “MISFET” that has fixed negative charge in the layer below the gate which is an insulator and at the same time make an “enhancement mode” device.

[068] Third, claim 14 requires a “semi-insulating III-N layer [that] comprises compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen.” As I have already explained, the patent does not describe or enable this limitation. See above §§V.A, V.C.1-V.C.4. It never describes using deep level traps when also using p-type dopants, for example. But additionally, this condition works against the requirement to be enhancement mode, because passivating p-type acceptors reduces the ability to deplete the 2DEG for the enhancement-mode operation.

[069] In sum, claim 14 requires a MISFET, operating in enhancement mode, with a semi-insulating layer comprising a compensated GaN layer that contains p-

type dopants passivated with hydrogen. But such conditions present trade-offs and competing effects, and the patent does not provide any guidance and how to achieve the claimed device given those tradeoffs.

[070] To a POSITA, these three points together lead to competing (even contradictory) requirements, as shown in the table below.

Claim Term	Condition in Claimed Device
MISFET	p-GaN layer below the gate is insulating.
Enhancement mode	p-GaN layer below the gate has active p-type acceptor atoms (e.g., Mg) to deplete the 2DEG.
compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen	p-GaN layer below the gate is passivated and is insulating. Passivation will reduce the ability to deplete the 2DEG.

[071] These three requirements in claim 14 present trade-offs and competing effects. The patent does not explain how to reconcile these competing requirements. Without guidance from the patent, a POSITA would have required undue experimentation to achieve the device of claim 14 (if it is even possible).

VI. THE PROPOSED CLAIMS ARE OBVIOUS

[072] The plain language of “wherein the semi-insulating III-N layer *comprises* a compensated GaN layer” as recited in of [13e.2] and [14c.2] can be

interpreted as either (i) the “compensated GaN layer” *is* the “semi-insulating III-N layer” or (ii) the “compensated GaN layer” is included in a larger “semi-insulating III-N layer.” Although it is my opinion that the specification does not support these limitations under any interpretation (see above §V), I present two alternative views of invalidity over the prior art below based on these two interpretations. The claims are obvious over the prior art under both interpretations.

[073] The prior art mappings of limitations [13e.1], [13e.2], [13f], [14c.1], [14c.2] and [14d] are affected by these interpretations. For each such limitation, I present an analysis under both interpretations.

[074] In my analysis I identify prior art GaN layers that disclose limitations [13e.1]/[14c.1] and [13e.2]/[14c.2] under these two different interpretations. Under the first interpretation, a “compensated GaN layer” is the “semi-insulating III-N layer,” and a prior art GaN layer with a “passivated p-type impurity such as, for example, **Mg**, **Zn**, **Be**, **Cd**, or **Ca**” that is above a barrier and below a gate contact discloses [13e.1]/[14c.1]. This is because the patent provides these impurities as examples for a compensated GaN. Ex. 1001, 3:10-12, claims 1-3. When passivated with hydrogen, the same prior art GaN layer also discloses [13e.2] “wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen.”

[075] Under the second interpretation, a “compensated GaN layer” is included in a larger “semi-insulating III-N layer,” and a prior art GaN layer with “deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni” that is above a barrier layer and below a gate contact discloses [13e.1]/[14c.1]. This is because the patent provides these impurities as examples for a semi-insulating III-N layer. Ex. 1001, 3:57-59, 5:24-6:5 (claims 4-6), 5:24-6:5 (claims 4-6). If that GaN layer also includes a subregion with a “passivated p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca,” then it discloses [13e.2] “wherein the semi-insulating III-N layer *comprises* a compensated GaN layer” because the patent provides these impurities as examples for a compensated GaN. Ex. 1001, 3:10-12, claims 1-3.

[076] The following chart illustrates the above discussion of prior art GaN layers that disclose [13e.1]/[14c.1] and [13e.2]/[14c.2] under these two interpretations.

Limitations	<u>Interpretation i:</u> “compensated GaN layer” is a “semi- insulating III-N layer”	<u>Interpretation ii:</u> “compensated GaN layer” is included in a larger “semi-insulating III-N layer”
[13e.1] a semi-insulating III-N layer above the barrier layer	A prior art GaN layer with a “passivated p-type impurity such as, for example, Mg, Zn, Be,	A prior art GaN layer with “deep level impurity atoms, for example, C,
[14c.2] a semi-insulating III-N layer between the barrier layer and the gate contact	Cd, or Ca” above a barrier layer and below a gate contact discloses [13e.1]/[14c.1].	Fe, Mn, Cr, V, or Ni” above a barrier layer and below a gate contact discloses [13e.1]/[14c.1].

Limitations	<u>Interpretation i:</u> “compensated GaN layer” is a “semi-insulating III-N layer”	<u>Interpretation ii:</u> “compensated GaN layer” is included in a larger “semi-insulating III-N layer”
[13e.2] wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen	If the p-doped GaN layer of [13e.1]/[14c.1] is passivated with hydrogen, then it discloses [13e.2]/[14c.2].	If the GaN layer of [13e.1]/[14e.1] contains a region with a “p-type impurity such as, for example, Mg, Zn, Be, Cd, or Ca ” passivated with hydrogen, then it discloses [13e.2]/[14c.2].
[14c.2] wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen		

[077] The following table lists the prior art that, in my opinion, show the new claims 13 and 14 would still be invalid as obvious

Exhibit	Prior Art
1005	<i>Smith</i> , U.S. Patent Publication No. 2007/0164315, published July 19, 2007
1006	<i>Uemoto</i> , U.S. Patent Publication No. 2008/0087915, filed July 24, 2007, and published April 17, 2008.
1007 (Translation 1008)	<i>Kigami</i> , Japanese Patent Publication No. JP2006-253224, published September 21, 2006
1035 (Translation 1036)	<i>Sheu</i> , Taiwanese Patent Office Publication No. TW200414540A published August 1, 2004.

[078] The below chart summarizes the grounds presented here.

“compensated GaN layer” is a “semi-insulating III-N layer”	“compensated GaN layer” is included in a larger “semi-insulating III-N layer”
Ground 1.A.i: <i>Smith</i> renders obvious Claims 13 and 14	Ground 1.A.ii: <i>Smith</i> renders obvious Claims 13 and 14
Ground 1.B.i: <i>Smith</i> in view of <i>Kigami</i> renders obvious Claims 13 and 14	Ground 1.B.ii: <i>Smith</i> in view of <i>Kigami</i> renders obvious Claims 13 and 14

“compensated GaN layer” is a “semi-insulating III-N layer”	“compensated GaN layer” is included in a larger “semi-insulating III-N layer”
Ground 1.C.i: <i>Smith</i> in view of <i>Uemoto</i> renders obvious Claims 13 and 14	Ground 1.C.ii: <i>Smith</i> in view of <i>Uemoto</i> renders obvious Claims 13 and 14
Ground 2.A: <i>Sheu</i> in view of <i>Kigami</i> renders obvious Claims 13 and 14	Ground 2.A.ii: <i>Sheu</i> in view of <i>Kigami</i> renders obvious Claims 13 and 14

**A. The New Claims Remain Unpatentable in View of *Smith*,
Smith/Kigami, and *Smith/Uemoto***

1. Motivation to combine *Smith/Kigami* and *Smith/Uemoto*

a. Interpretation i: “compensated GaN layer” is a “semi-insulating III-N layer”

[079] For reasons provided in my declaration that accompanied the Petition, under the first interpretation, a POSITA would have been motivated to combine *Smith* with *Kigami* or *Uemoto*. Ex. 1003 ¶¶104-140.

**b. Interpretation ii: “compensated GaN layer” is
included in a larger “semi-insulating III-N layer”**

[080] *Smith* includes an embodiment in which a GaN **cap layer 34** is co-doped with deep level dopants and p-type acceptors (e.g., Mg) throughout but with a heavily doped p-type region 40. *Smith*, [0085]. Modified Figure 2A, below,

depicts the GaN **cap layer 34** above a **barrier layer 22** (which may be GaN or AlGaN), below a **gate contact 32**, and between **ohmic contacts 30**.

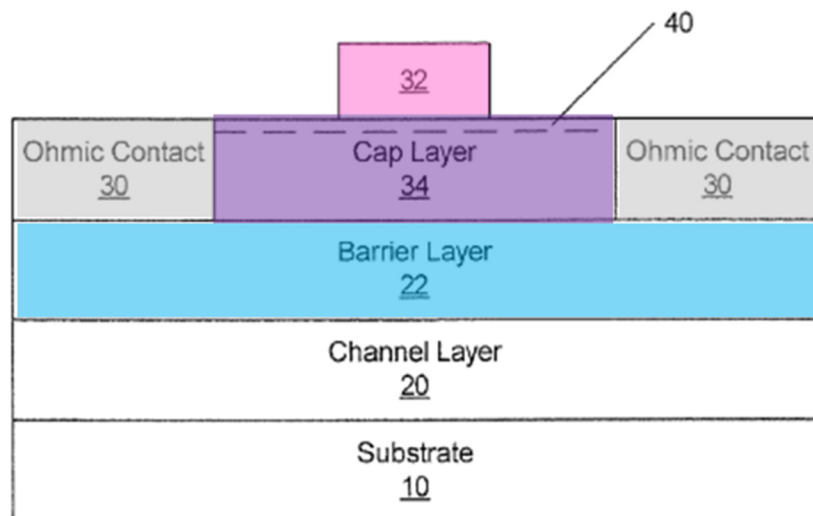


Figure 2A

Smith, Figure 2A (modified)

[081] As I will explain, in embodiments where **cap layer 34** is co-doped with deep level dopants and p-type acceptors (e.g., Mg) throughout but with a heavily doped p-type region 40, a POSITA would have found it obvious over *Smith* alone, or in view of *Kigami* and *Uemoto*, to passivate *Smith*'s **cap layer 34** with hydrogen to control acceptor concentration, prevent the layer from becoming conductive, and reduce gate leakage. Ex. 1003 ¶¶123-140; *Smith*, [0087].

[082] *Smith* discloses doping **cap layer 34** “throughout the cap layer” and using “[t]echniques for co-doping” incorporating *Saxler874* by reference to teach the co-doping aspects. *Smith*, [0085]. In turn, *Saxler874* describes doping such that Mg concentration is lower than the concentration of the deep level dopants. *Saxler874*, [0005]-[0006].

[083] *Smith* further discloses a subregion 40 of the cap layer 34 that is doped heavily p-type in some embodiments to control gate leakage. *Smith*, [0085], [0087]. *Smith* specifically notes “doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C,” and “cap layer 34, 34’ has a dopant incorporated throughout. In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34’.” *Smith*, [0085]. *Smith* teaches that the level of doping should be controlled to be high enough to reduce leakage current, but low enough to not act as a conductive layer. *Smith*, [0087]. Thus, *Smith* discloses low levels of p-type dopant below region 40 and high levels in region 40.

[084] Then, A POSITA would have found it obvious over *Smith* alone, or in view of *Kigami* and *Uemoto*, to passivate *Smith*'s cap layer with hydrogen to control acceptor concentration while reducing gate leakage. There are many reasons why a POSITA would have been motivated to passivate with hydrogen.

[085] First, a POSITA would be motivated to do so for the reasons I discussed in my declaration accompanying the Petition. Ex. 1003 ¶¶123-140.

[086] Second, a POSITA would have been additionally motivated to use hydrogen to passivate **cap layer 34** in the co-doping embodiments to make the portion below region 40 a semi-insulating layer. Because *Smith's* incorporation of *Saxler874* leads to lower levels of p-type acceptor dopants in the portion of **cap layer 34** below region 40 than in region 40, this portion would be fully passivated while maintaining active acceptor concentration in region 40. *Smith*, [0085]; *Saxler874*, [0005]-[0006]. The portion below region 40 would thus be insulating because it contains only passivated dopants that prevent charge from traveling.

[087] Modified Figure 2A, below, depicts the insulated region and **cap layer 34**.

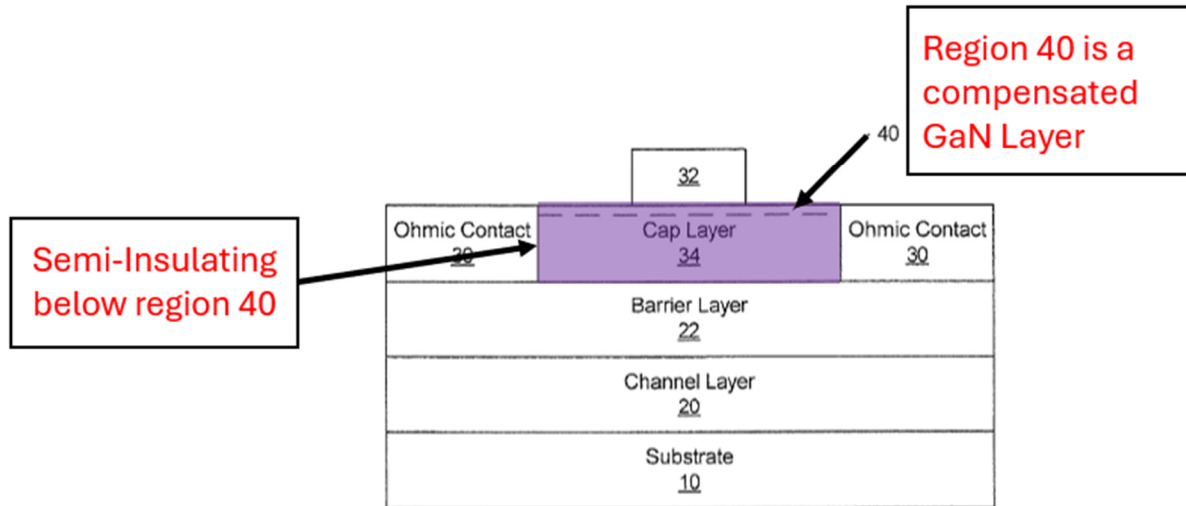


Figure 2A

2. Independent Claim 13

a. [13p] An enhancement mode column III nitride transistor comprising:

[088] *Smith* discloses [13p]. As I previously explained for [1p], *Smith* discloses a “column III nitride transistor.” Ex. 1003 ¶142. Further, as discussed in my supplemental declaration, *Smith* discloses embodiments that operate as “enhancement mode” transistor. Ex. 1033 ¶¶46-67. For example, *Smith* discloses embodiments in which a doped GaN cap layer (e.g., cap layer 34) is below the gate (e.g., gate electrode 32) and above an AlGaN barrier layer (e.g., barrier layer 32). *Smith*, [0014], [0017], [0085]. And *Smith* discloses the cap layer being p-type,

doped with acceptors and with a combination of acceptors and deep level dopants.

Smith, [0085]-[0087].

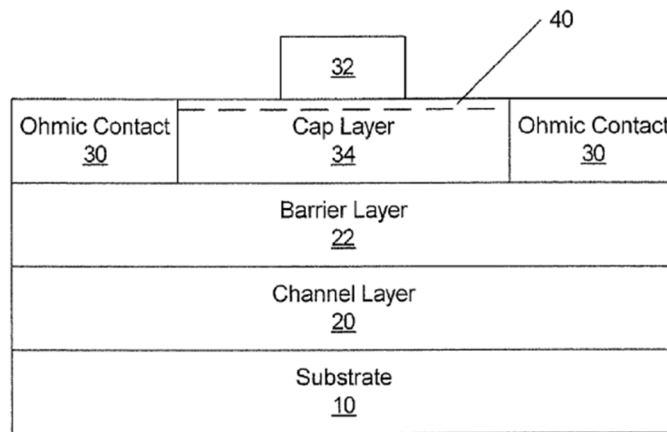


Figure 2A

Smith, Fig. 2A

[089] Accordingly, as I further note in my supplemental declaration, a POSITA would have recognized that such *Smith* devices disclose an “enhancement mode column III nitride transistor.” Ex. 1033 ¶¶44-67.

b. [13a] a substrate,

[090] *Smith* discloses [13a]. As previously explained for [1a], *Smith*'s **substrate 10** discloses “a substrate.” Ex. 1003 ¶143.

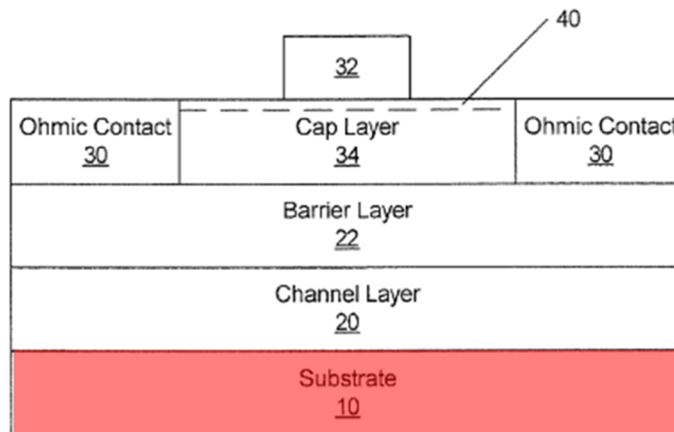


Figure 2A

Smith, Fig. 2A (annotated).

c. [13b] a set of III-N transition layers above the substrate

[091] *Smith* discloses [13b]. As I explained for [1b], *Smith*'s **transition layers** disclose "a set of III-N transition layers above the substrate." Ex. 1003 ¶144.

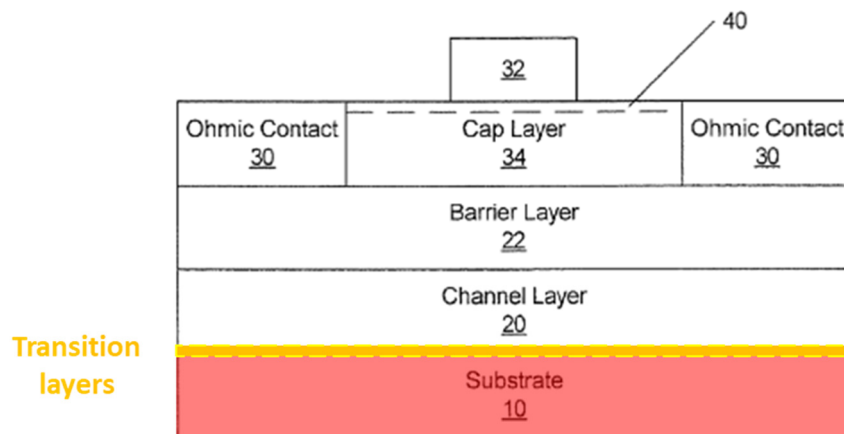


Figure 2A

Smith, Fig. 2A (modified)

d. [13c] a III-N buffer layer above the set of transition layers,

[092] *Smith* discloses [13c]. As previously explained for [1c], *Smith*'s

channel layer 20 discloses “a III-N buffer layer above the set of transition layers.”

Ex. 1003 ¶¶146-149.

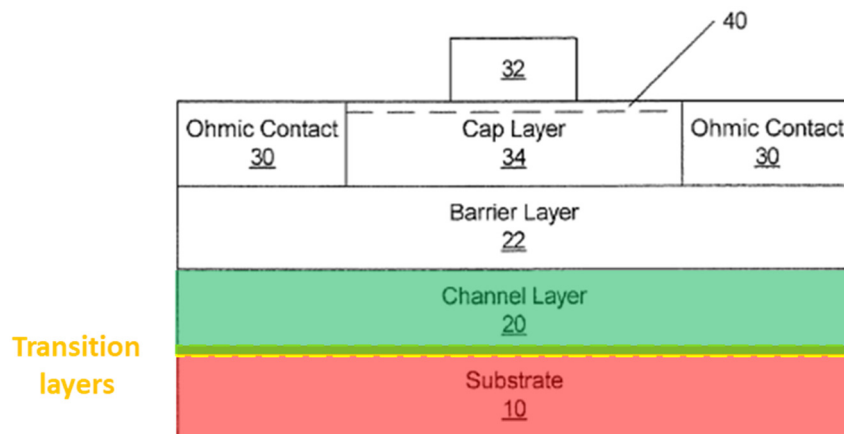


Figure 2A

Smith, Fig. 2A (modified)

e. [13d] a III-N barrier layer above the buffer layer,

[093] *Smith* discloses [13d]. As previously explained for [1d], *Smith*'s

barrier layer 22 discloses “a III-N barrier layer above the buffer layer.” Ex. 1003

¶150.

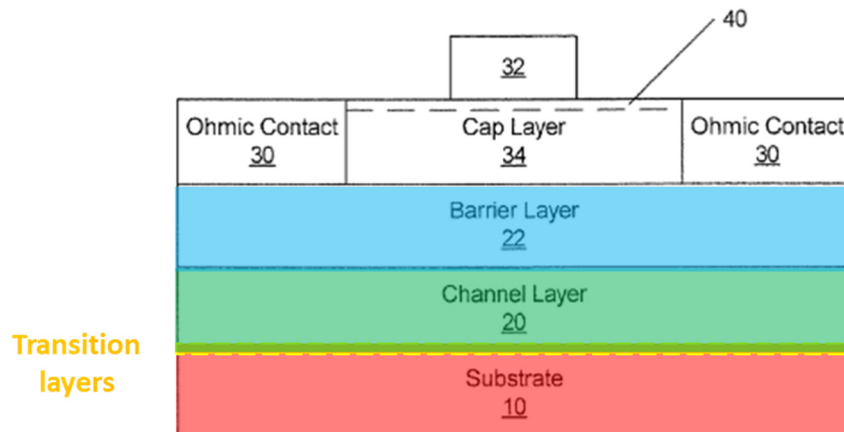


Figure 2A

Smith, Fig. 2A (modified).

- f. [13e.1] a semi-insulating III-N layer above the barrier layer,
 - i. Interpretation i: “compensated GaN layer” is a “semi-insulating III-N layer”

[094] *Smith*, alone or in view of *Kigami* or *Uemoto* renders obvious [13e.1] under the first interpretation of [13e.2].

[095] As previously explained for [1e], *Smith* alone or in view of *Kigami* or *Uemoto* renders obvious “a compensated GaN layer above the barrier layer” under Petitioner’s proposed construction or EPC’s original proposed construction.

Ex. 1003 ¶¶105-122, 151-163. And as discussed in my declaration in support of Petitioner’s Reply, *Smith* alone or in view of *Kigami* or *Uemoto* also renders

obvious a “compensated GaN layer above the barrier layer” under EPC’s revised construction. Ex. 1033 §III.C.

Innoscience construction	EPC initial construction	EPC revised construction
“Doped GaN layer formed with a step to passivate its impurities” which is a “product-by-process” limitation	“A semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor).”	“a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).”

[096] In each of Grounds 1A (*Smith*), 1B (*Smith/Kigami*), and 1C (*Smith/Uemoto*) it would have been obvious that *Smith*’s **cap layer 34** (as taught by *Smith* or as modified by *Kigami* or *Uemoto*) is a “compensated GaN layer,” above **barrier layer 22**, a III-N layer (specifically GaN), under both EPC’s and Innoscience’s construction of the term. Ex. 1003 ¶¶105-122, 151-168.; Ex. 1033 §III.C.

[097] Thus, under an interpretation of [13e.2] that the “compensated GaN layer” *is* the claimed “semi-insulating III-N layer,” *Smith* alone and/or in view of *Kigami* or *Uemoto* render obvious [13e.1].

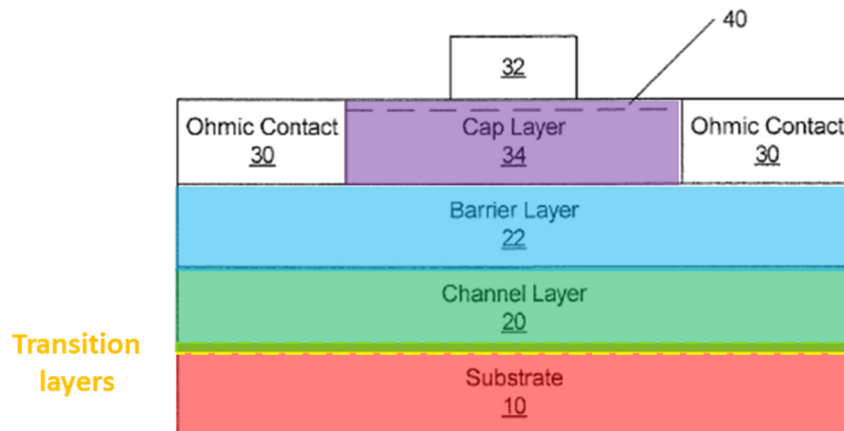


Figure 2A

Smith, Fig. 2A (modified).

ii. Interpretation ii: “compensated GaN layer” is included in a larger “semi-insulating III-N layer”

[098] *Smith* discloses [13e.1] under the second interpretation of [13e.2]. As previously explained for [4e], *Smith*'s **cap layer 34**, which is above **barrier layer 22**, discloses “a semi-insulating III-N layer above the barrier layer” in embodiments of **cap layer 34** using co-doping and deep level dopants. Ex. 1003 ¶¶175-176. *Smith* provides example deep a level dopant such as “Fe, C, V, Cr, Mn, Ni and/or Co” that overlap with the examples provided in the '294 patent of “C,

Fe, Mn, Cr, V, or Ni.” Ex. 1001, 3:57-59, 5:24-6:5 (claims 4-6), 5:24-6:5

(claims 4-6). Further, like the '294 patent, *Smith* discloses the semi-insulating layer being formed with AlGa_N or Ga_N, doped with deep level impurity atoms.

Compare Smith, [0089] (“cap layer 34, 34' may be a Ga_N based cap layer, such as a Ga_N layer and/or an AlGa_N . . . deep level dopants may be Fe, C, V, Cr, Mn, Ni, Co) with Ex. 1001, 2:66-67 (“Semi-insulating layer 39 may comprise, for example, AlGa_N or Ga_N, with deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni”).

[099] *Smith* further discloses co-doping Ga_N **cap layer 34** with both deep a level dopant such as “Fe, C, V, Cr, Mn, Ni and/or Co” *and* a “p-type dopant, such as Mg, Be, Zn, Ca and/or C.” *Smith*, [0085] (incorporating *Saxler874* to disclose co-doping techniques); *Saxler874*, Abstract, [0005]-[0006]. When co-doping Ga_N **cap layer 34** in this way, *Smith* discloses the “semi-insulating layer” of limitation [13e.1].

- g. [13e.2] wherein the semi-insulating III-N layer comprises a compensated Ga_N layer containing acceptor type dopant atoms passivated with hydrogen, and
 - i. Interpretation i: “compensated Ga_N layer” is a “semi-insulating III-N layer”

[0100] *Smith*, alone or in view of *Kigami* or *Uemoto*, renders obvious [13e.2] under the first interpretation of [13e.2] that the “compensated GaN layer” is a “semi-insulating III-N layer.” As I explained for limitation [13e.1], *Smith*’s **cap layer 34** renders obvious a “compensated GaN layer” under any proposed construction. See above §VI.A.2.f.i. Further, as previously explained for claim 2, *Smith*, alone or in view of *Kigami* or *Uemoto*, also renders obvious that the **cap layer 34** “contain[s] acceptor type dopant atoms passivated with hydrogen” as required in limitation [13e.2]. Ex. 1003 ¶¶105-122, 123-140, 165-168.

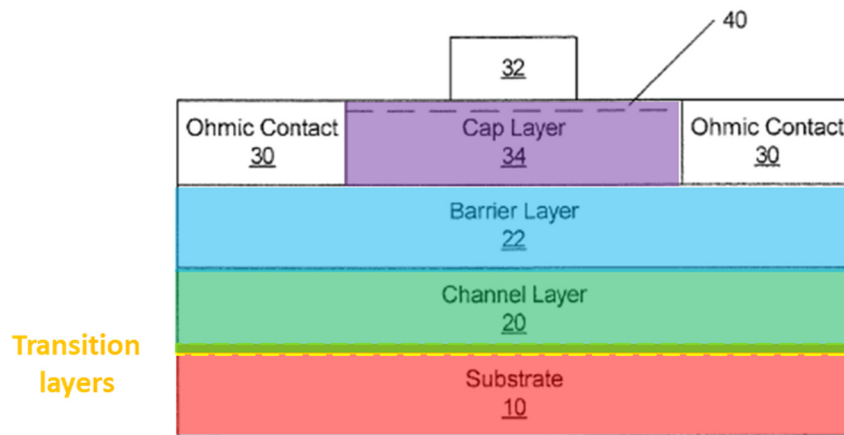


Figure 2A

Smith, Fig. 2A (modified).

- ii. **Interpretation ii: “compensated GaN layer” is included in a larger “semi-insulating III-N layer”**

[0101] *Smith*, alone or in view of *Kigami* or *Uemoto*, renders obvious [13e.2] under its second interpretation. As I explained for limitation [13e.1], embodiments of **cap layer 34** that are co-doped with deep level and p-type impurities render obvious the claimed “semi-insulating III-N layer.” See above §VI.A.2.f.ii.

[0102] Within the larger **cap layer 34**, *Smith* discloses region 40 as a subregion. In Grounds 1A-1C the subregion “compensated GaN layer containing acceptor type dopant atoms,” as recited in [13e.2]. *Smith* discloses region 40 is doped heavily p-type in some embodiments. *Smith*, [0085], [0087]. For example, in some embodiments *Smith* notes “doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C,” and “cap layer 34, 34’ has a dopant incorporated throughout.” *Smith*, [0085]. *Smith* further states that in such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer. *Smith*, [0085]. In the same passage, *Smith* explicitly incorporates the co-doping techniques of *Saxler*⁸⁷⁴. *Smith*, [0085] (“Techniques for co-doping Group III-nitride materials are described, for example, in U.S. patent application Ser. No. 10/752,970, filed Jan. 7, 2004 entitled “CO-DOPING FOR FERMI LEVEL

CONTROL IN SEMI-INSULATING GROUP III NITRIDES,” the disclosure of which is incorporated herein as if set forth in its entirety”).

[0103] *Smith* discloses embodiments where the concentration of p-type dopants (e.g., Mg) in region 40 is higher than the deep level dopant concentrations. *Smith*, [0085], [0087]. Thus, a POSITA would have understood that in the combinations of Grounds 1A-1C the doped region 40 is a “compensated GaN layer containing acceptor type dopants” within the larger cap layer 34, which is a “semi-insulating III-N layer” because it contains deep acceptor atoms in *Smith*'s co-doped embodiments.

[0104] *Smith*'s **cap layer 34** is highlighted below in annotated Figure 2A, showing **cap layer 34** above the **barrier layer 22** and region 40 within the cap layer.

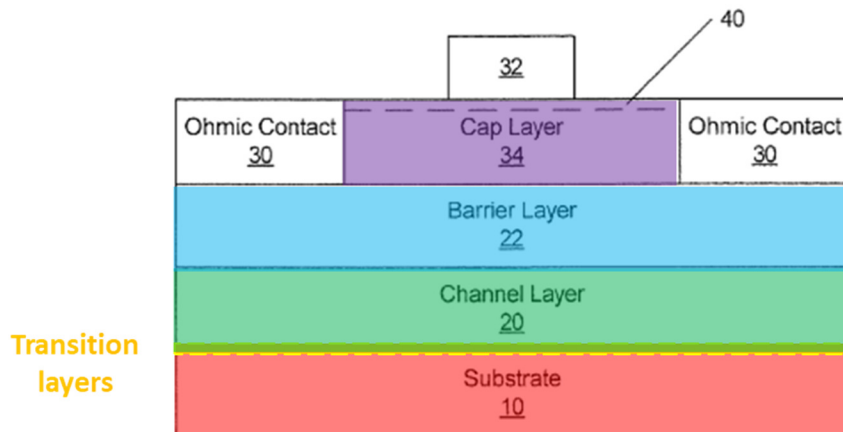


Figure 2A

Smith, Fig. 2A (modified).

[0105] In such embodiments, *Smith* alone and/or in view of *Kigami* or *Uemoto* render obvious “wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms *passivated with hydrogen*” as recited in claim [13e.2]. For the same reasons I provided with respect to limitation [1e] and claim 2, *Smith*’s p-type dopants like magnesium would be passivated with hydrogen in each of Grounds 1A-1C. Ex. 1003 ¶¶105-122, 151-163-168.

[0106] Briefly, a POSITA would have understood that, when doping with Mg as *Smith* discloses, hydrogen would have been naturally incorporated into the cap layer and passivated dopants, including in region 40. Ex. 1003 ¶¶113-114. In

addition, *Smith* itself would have further motivated a POSITA to control active acceptor concentration using well-known methods of hydrogen passivation to control the level of doping in the layer, prevent the layer from becoming conductive, and reduce gate leakage. Ex. 1003 ¶¶123-127. And a POSITA would also have been motivated to implement *Kigami*'s and *Uemoto*'s methods of using hydrogen to passivate and control active dopant concentrations in *Smith*'s device and reduce gate leakage. Ex. 1003 ¶¶128-140.

[0107] For these reasons, under the second interpretation of [13e.2] where the “compensated GaN layer” is included within a larger “semi-insulating III-N layer,” *Smith*'s region 40 alone and/or in view of *Kigami* and *Uemoto* renders obvious a “compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen.”

- h. [13f] a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.**

[0108] *Smith*, alone or in view of *Kigami* or *Uemoto*, renders obvious [13f] under both interpretations of [13e.2].

[0109] First, *Smith*, alone or in view of *Kigami* or *Uemoto*, renders obvious “a gate comprising a gate contact and the compensated GaN layer.” As previously

explained for [1f], *Smith*'s **gate contact 32** is a "gate contact" above **cap layer 34**.
Ex. 1003 ¶0164. And *Smith*'s **cap layer 34** alone and/or as modified in
Smith/Kigami and *Smith/Uemoto* render obvious the "compensated GaN layer"
under both interpretations. See above §§VI.A.2.g.i, VI.A.2.g.ii. In the Grounds 1A-
1C, therefore, *Smith*'s **gate contact 32** and **cap layer 34** form a "gate comprising a
gate contact and the compensated GaN layer."

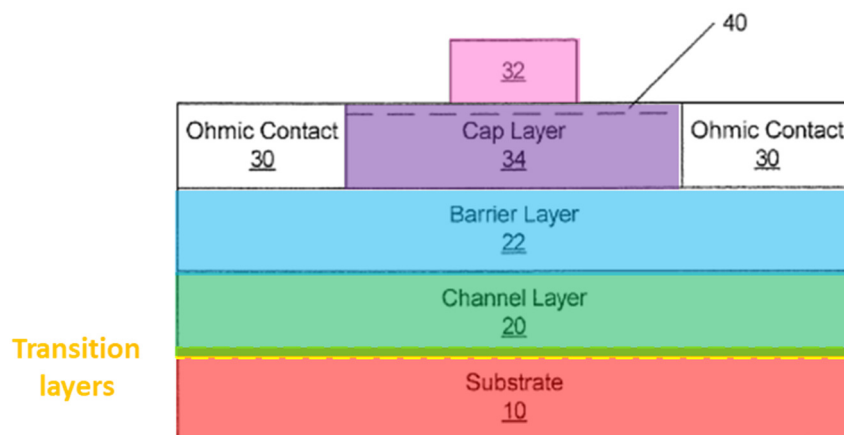


Figure 2A

Smith, Fig. 2A (modified).

[0110] Further, the grounds 1A-1C combinations meet the "wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias" limitation under any of the interpretations of [13e.2].

- i. **Interpretation i: "compensated GaN layer" is a "semi-insulating III-N layer"**

[0111] Under the first interpretation, *Smith* alone and/or in view *Kigami* or *Uemoto* also render obvious “wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.”

[0112] As I explained, *Smith* alone renders obvious an “enhancement mode” device due to the presence of cap layer 34, which is doped p-type, below the gate and above an AlGa_N barrier layer. See above §VI.A.2.a; Ex. 1033 ¶¶50-53. And while the passivation of dopants in cap layer would reduce active acceptor concentration and increase 2DEG concentration, to a POSITA it would have been obvious to determine a passivation that results in an enhancement mode device given the knowledge of the POSITA and the information *Smith*, *Uemoto*, or *Kigami* provide.

[0113] For example, a POSITA knew that hydrogen would have been naturally incorporated into the cap layer and passivated dopants, including in region 40. Ex. 1003 ¶¶113-114. But *Smith* specifies different ranges of doping concentrations and layer thicknesses that a POSITA would have identified as resulting in enhancement mode devices even with natural passivation. For example, *Smith* describes the cap layer “may have a thickness of from about 2 nm to about 500 nm” with doping regions between “30 Å to about 5000 Å.” *Smith*, [0077], [0087]. *Smith* also discloses different doping concentrations and profiles,

describing concentrations in different areas of the cap layer ranging from “from about 10^{18} to about 10^{21} cm^{-3} ” with surface dopant concentration “from about 10^{11} to about 10^{15} cm^{-2} .” *Smith*, [0087]. *Smith*, thus, describes multiple embodiments and ranges that a POSITA would have identified as resulting in enhancement mode devices with active acceptor concentration sufficiently high to deplete the 2DEG below the gate at zero volts applied gate bias.

[0114] Further, references like *Kigami* and *Uemoto* describe techniques for localized hydrogenation of GaN layers. *Kigami* describes for example localized hydrogenation where “the concentration distribution of the hydrogen atoms to be introduced, and the like can be adjusted by forming in advance on the front-surface side of the semiconductor device 100 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these.” *Kigami*, [0036]. *Uemoto* also teaches methods for localized selective hydrogenation. *Uemoto*, [0062]. The description of *Kigami* and *Uemoto* for localized and controlled passivation in combination with *Smith*'s disclosure, made obvious the grounds 1A-1C combinations describe devices with enhancement mode operation where “no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.”

[0115] Further, when passivating the cap layer with hydrogen to reduce gate leakage with well-known hydrogen passivation methods, which would have been obvious over *Smith* alone and/or in view of *Kigami* and *Uemoto*, a POSITA would have sought to use the thickness, doping, and arrangement *Smith* discloses while maintaining an active dopant concentration that resulted in “no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias” in [13f]—and function as an enhancement mode device. A POSITA would have been motivated to do so to realize the benefits of enhancement mode devices, including reduced power consumption and suitability for high power applications (e.g., use of a p-GaN below gate contact provides higher threshold voltage and added safety in power switching, high power applications). *Suh2006*, 1.

ii. Interpretation ii: “compensated GaN layer” is a “semi-insulating III-N layer”

[0116] Under the second interpretation, *Smith* alone, or in view *Kigami* or *Uemoto*, also render obvious “wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.”

[0117] In the *Smith* grounds, a POSITA would have understood hydrogen impurities (from the *Smith*'s MOCVD, *Kigami*'s hydrogenation, or *Uemoto*'s hydrogen diffusion) would passivate the heavily p-type doped region 40. See

above §VI.A.2.g.ii. But, noted above, based on knowledge, and the disclosures in *Smith*, *Kigami*, and *Uemoto*, a POSITA would have found it obvious to have *Smith*'s device with parameters so the active acceptor concentration resulted in an enhancement-mode device.

[0118] For example, to a POSITA it would have been obvious that the parameters *Smith* describes for its embodiment with co-doping and heavily doped p-type region 40 along with the doping techniques *Kigami* and *Uemoto* describe would result in a device where “no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.”

[0119] *Smith* describes embodiments in which the concentration of p-type dopant is higher in region 40 than the other dopants in the cap layer. *Smith*, [0085]. To a POSITA, it would have been obvious that in some embodiments of *Smith*, cap layer 34 would contain sufficient acceptors to fully deplete the 2DEG as required by limitation [13f] and *Smith*'s transistor would function as an enhancement mode device as required by limitation [13p].

[0120] As discussed above, in view of *Smith* alone and/or in view of *Kigami* and *Uemoto*, a POSITA would have found it obvious to passivate the cap layer with hydrogen to reduce gate leakage. See above §VI.A.2.g.i. When passivating with hydrogen in these combinations, a POSITA would have maintained an active

dopant concentration that still allowed heavily p-type doped region 40 to deplete the 2DEG as required by [13f] and function as an enhancement mode device. A POSITA would have been motivated to do so to realize the benefits of enhancement mode devices, including reduced power consumption and suitability for high power applications (e.g., use of a p-GaN below gate contact provides higher threshold voltage and added safety in power switching, high power applications). *Suh2006*, 1.

3. Independent Claim 14

a. [14p] A compensated gate enhancement mode MISFET transistor comprising:

[0121] *Smith*, alone or in combination with *Uemoto* and *Smith*, discloses [14p].

[0122] As noted above regarding [13p], *Smith*, alone or in combination with *Uemoto* or *Smith*, discloses a “compensated gate enhancement mode ... transistor” by disclosing a transistor where **cap layer 34** is compensated, p-type doped (e.g., with magnesium), and forming an enhancement mode transistor. See above §VI.A.2.a.

[0123] Additionally, *Smith*, alone or in combination with *Uemoto* or *Kigami*, discloses the transistors being MISFETs. As I discussed in my first

declaration, *Smith*, alone or in combination with *Kigami* or *Uemoto*, discloses a compensated gate MISFET transistor. Ex. 1003 ¶¶195-198. For example, the annotated Figure 3B illustrates *Smith*'s disclosure of the "compensated gate MISFET transistor" of [10p]. Ex. 1003 ¶196. *Smith* discloses "in the embodiments illustrated in FIG. 3B, a MISHEMT may be provided." *Smith*, [0095].

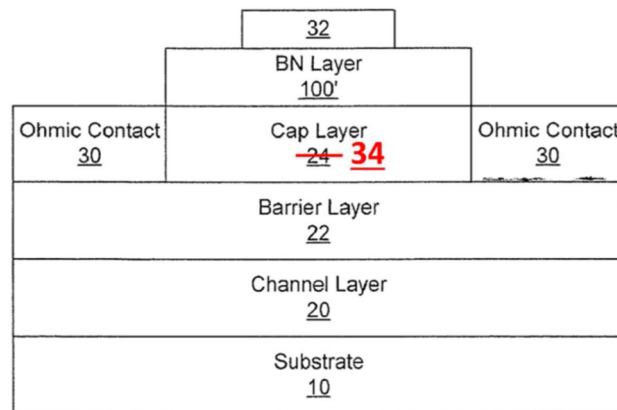


Figure 3B

***Smith*, Fig. 3B (modified to substitute "cap layer 24"
for "cap layer 34")**

[0124] Further, because *Smith* discloses cap layer 34 being p-type doped, to a POSITA it would have been obvious that *Smith*'s MISFET would operate in enhancement mode. *Smith*, [0087]. As I explained above and in my declaration marked Ex. 1033, when cap layer 34 is p-type doped it would deplete the 2DEG at 0V applied gate voltage. See above §VI.A.2.a; Ex. 1033 §IV.A. As I pointed out in

my supplemental declaration, Dr. Schubert noted that “if a p-type gate material is present over the barrier layer, it can deplete the 2DEG under the gate to create an enhancement mode, i.e., normally ‘OFF’, transistor.” Ex. 2009 ¶31. That is the configuration above in Fig. 3B, where cap layer 34 is p-type gate material present over the barrier layer 22.

[0125] Therefore, *Smith* discloses a “compensated gate enhancement mode MISFET transistor,” as recited in [14p].

b. [14a] a III-N barrier layer beneath a gate contact,

[0126] *Smith* discloses [14a]. As previously explained for [10a] for the Petition, *Smith*'s **barrier layer 22** is a III-N barrier layer beneath **gate contact 32**, as highlighted below in annotated Figure 3B. Ex. 1003 ¶199-200.

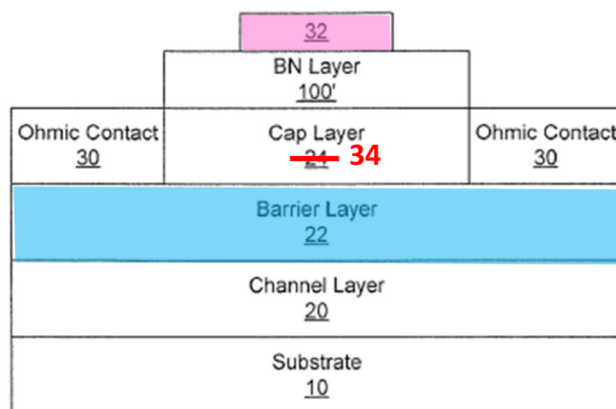


Figure 3B

Smith, Fig. 3B (modified).

c. [14b] a drain contact, a source contact,

[0127] *Smith* discloses [14b]. As previously explained for [10a] for the Petition, *Smith*'s **ohmic contacts 30** of Figure 3B disclose “a drain contact, a source contact,” shown below. Ex. 1003 ¶201. *Smith*, [0090].

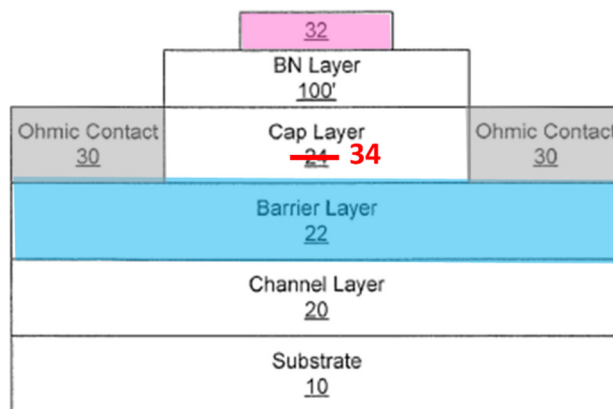


Figure 3B

Smith, Fig. 3B (modified).

d. [14c.1] a semi-insulating III-N layer between the barrier layer and the gate contact,

[0128] Element [14c.1] and [13e.1] both require “a semi-insulating III-N layer.” And as I explained in reference to [13e.1], *Smith*'s **cap layer 34**, alone or in view of *Kigami* or *Uemoto*, renders obvious the claimed “semi-insulating III-N layer” under either interpretation of “wherein the semi-insulating III-N layer *comprises* a compensated GaN layer.” See above §§VI.A.2.f.i, VI.A.2.f.ii.

[0129] Element [14c.1] requires that the “semi-insulating III-N layer is *between the barrier layer and the gate contact.*” Modified Figure 3B, below, shows that **cap layer 34** is between **gate contact 32** and **barrier layer 22**. *Smith*, [0090].

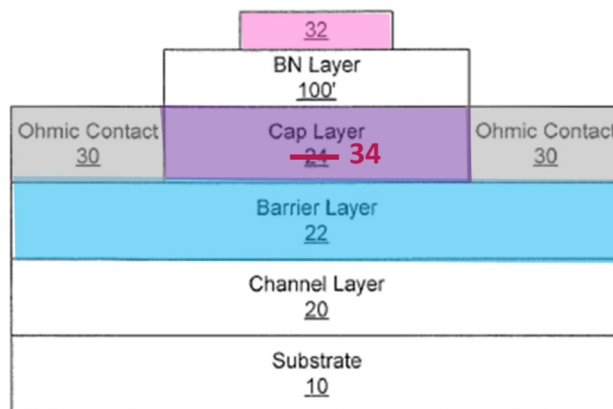


Figure 3B

Smith, Figure 3B (modified)

- e. [14c.2] wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and,

[0130] Limitations [14c.2] and [13e.2] are the same. As I explained in reference to [13e.2], *Smith*, alone or in view of *Kigami* or *Uemoto*, renders obvious this limitation under either interpretation of “wherein the semi-insulating III-N layer *comprises* a compensated GaN layer.” *See above* §§VI.A.2.g.i, VI.A.2.g.ii.

- f. **[14d] a gate comprising the gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.**

[0131] Limitations [14d] and [13f] are the same. As I explained in reference to [13f], *Smith*, alone or in view of *Kigami* or *Uemoto*, renders obvious this limitation under either interpretation of “wherein the semi-insulating III-N layer *comprises* a compensated GaN layer.” See above §§VI.A.2.h.i, VI.A.2.h.ii;

B. The New Claims Are Unpatentable in view of *Sheu* and *Kigami*

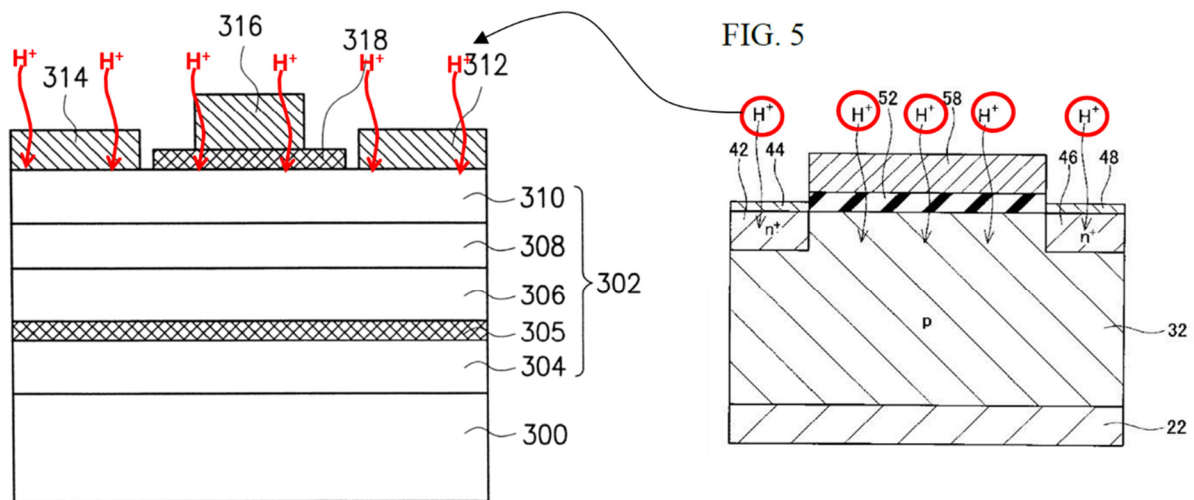
1. Motivation to combine *Sheu* and *Kigami*

[0132] A POSITA would have found it obvious to apply *Kigami*'s teachings to the transistors disclosed in *Sheu*. For example, a POSITA would have found it obvious to apply the *Kigami*'s hydrogenation techniques to passivate dopants in *Sheu*'s magnesium-doped GaN “gate insulating layer 318.” A POSITA would have been motivated to use *Kigami*'s hydrogenation process to passivate the magnesium dopants in *Sheu*'s GaN gate insulating layer to adjust the layer's resistivity and achieve the advantages of localized hydrogenation discussed in *Kigami*. *Kigami*, [0007]-[0012].

[0133] *Sheu* states that gate insulating layer 318 is doped “to enhance the resistance value.” *Sheu*, p. 10. As I discussed in my first declaration, by the priority

date of the '294 patent it was well-known how hydrogen-passivated dopants (specifically magnesium) in GaN layers enhanced the layer's resistivity. Ex. 1003 ¶¶60-64. Therefore, a POSITA would have found it obvious to apply *Kigami's* hydrogenation process (*Kigami*, [0026]) to passivate the magnesium in *Sheu's* gate insulating layer 318 (*Sheu*, p. 10) seeking to control the resistivity of the layer.

[0134] *Sheu's* Figure 6, is modified below based on *Kigami's* Figure 5, shows the application of *Kigami's* hydrogenation process to *Sheu's* device structure.



***Sheu*, Fig. 6 (left, modified); *Kigami*, Fig. 5 (right, modified)**

[0135] Multiple rationales support the application of *Kigami's* hydrogenation in *Sheu's* device.

[0136] First, a POSITA would have found that *Sheu* and *Kigami* are relevant to one other and combinable because both are directed to III-nitride transistors and techniques to fabricate them. *Sheu*, p. 5; *Kigami*, Abstract. Both specifically describe techniques for fabricating HEMTs and transistors with metal-insulator-semiconductor (MIS) structures. *Sheu*, p. 9; *Kigami*, [0009]-[0010]. And both are directed to structures and techniques to improve III-nitride transistor robustness and operation. *Sheu*, p. 6; *Kigami*, [0010]. For example, *Sheu* explains that with its disclosed structures “it is expected that the breakdown voltage of the [transistor] will be significantly increased, thereby reducing the gate leakage current of the [transistor].” *Sheu*, p. 4. Similarly, *Kigami* states that its structures and fabrication methods seek to improve transistor operation by enabling “a low threshold voltage and a high withstand voltage.” *Kigami*, [0006]-[0007]. *Sheu* and *Kigami* are, thus, from the same field of endeavor, seeking to resolve the same problems in the same devices, and a POSITA would have considered their teachings both relevant and combinable.

[0137] Further, a POSITA would have been motivated to modify *Sheu*'s device in view of *Kigami*'s teachings because *Kigami* suggests and motivates such combination. *Kigami* teaches that its hydrogenation techniques are particularly suitable when using magnesium-doped GaN layers. *Kigami*, [0012] (explaining that

“[t]he present invention is particularly useful in situations in which magnesium is used as a p-type impurity”). And *Sheu* specifically discloses situations in which magnesium is used as p-type impurity; explicitly stating that “gate insulating layer 318 in this embodiment may also have a dopant ... such as carbon, **magnesium**, iron or a combination of these materials.” *Sheu*, p. 10 (emphasis added).

[0138] *Kigami* teaches that introducing hydrogen into Mg-doped GaN transistor layers, like *Sheu*'s insulating layer 318, improves transistor performance. *Kigami*, [0007]. *Kigami* states that “utilizing the phenomenon in which the p-type impurity is inactivated by hydrogen atoms” to locally lower active impurity concentrations permits “having a low threshold voltage and a high withstand voltage.” *Kigami*, [0007]. *Kigami* similarly suggests that applying its hydrogenation process to such layers has “effects of stabilized threshold voltage, increased switching speed, and the like.” *Kigami*, [0029].

[0139] A POSITA would have been motivated to apply *Kigami*'s teachings to *Sheu*'s device because of *Kigami*'s explicit suggestion to apply it when magnesium is used as a p-type impurity in GaN and because of *Kigami*'s claimed benefits in improving threshold voltage, breakdown voltage, and switching speed. A POSITA would have recognized that *Sheu* was also concerned with improving the transistor's operation and those specific characteristics *Kigami* improves. *Sheu*, p. 10

(explaining its transistors are suited to “high-frequency operation”), p. 4 (stating goals of improving “breakdown voltage” and reducing “gate leakage current”). A POSITA would have recognized that applying *Kigami*'s techniques would further *Sheu*'s stated goals of transistor performance and making layer 318 insulating.

[0140] Moreover, a POSITA would have found it obvious to apply *Kigami*'s hydrogenation process to *Sheu*'s device because a POSITA would have recognized that the combination would simply require the use of a known technique (*Kigami*'s hydrogenation process) to known device (*Sheu*'s) ready for improvement. *Kigami* discloses a known technique—the use of ionized hydrogen to locally passivate magnesium in p-type GaN layers. *Kigami*, [0012]. *Sheu* discloses a known device with a gate insulating layer 318 doped with magnesium. *Sheu*, p. 10. *Kigami* explains that its hydrogenation technique improves III-nitride transistors by adjusting the transistor's threshold voltage, enhancing the breakdown voltage, and permitting high-frequency applications. *Kigami*, [0007]-[0008], [0029]. *Kigami* also explains that its hydrogenation process results in high-resistivity semiconductor materials. *Kigami*, [0007] (stating that “the resistance of the III-V group compound semiconductor is made high”). A POSITA would have been motivated to use *Kigami*'s technique to improve *Sheu*'s transistor in the same way because *Sheu* shared the goals of enhancing the resistance of the gate insulating layer, improving

transistor operation, having high breakdown voltage, and operating at high frequencies. *Sheu*, pp. 5, 10. A POSITA would have recognized *Sheu*'s device as a base device that could be improved with *Kigami*'s hydrogenation techniques for magnesium passivation. Because *Sheu*'s and *Kigami*'s devices are comparable, both being III-nitride transistors with a Mg-doped GaN cap layer, a POSITA would have applied *Kigami*'s technique to *Sheu*'s device.

[0141] Furthermore, in my opinion a POSITA would have reasonably expected to succeed in applying *Kigami*'s hydrogenation process to *Sheu*'s transistor. By the priority date of the '294 patent, it was well-known how hydrogen-passivated magnesium in GaN layers affects the layer's conductivity. The passivation of magnesium with hydrogen had been known since the early 1990s. Ex. 1018. *Kigami* also provides experimental data showing the effect of hydrogen passivation on transistor performance. *Kigami*, [0028], Fig. 6. And *Kigami* also explains the mechanisms for hydrogen diffusion and impurity passivation, detailing how the hydrogen diffusion would be performed and how it would affect the magnesium dopants. *Kigami*, [0022]-[0026], Fig. 5. Given the general knowledge about doping and hydrogen passivation in p-type GaN, and *Kigami*'s disclosures, a POSITA would have reasonably expected to succeed in applying *Kigami*'s

hydrogenation techniques to *Sheu*'s device structure, and specifically layer 318, when seeking to control the layer's resistivity.

2. Independent Claim 13

a. [13p] An enhancement mode column III nitride transistor comprising:

[0142] The *Sheu/Kigami* combination discloses “[a]n enhancement mode column III nitride transistor” as recited in [13p].

[0143] *Sheu* discloses “a field effect transistor with a GaN-based gate insulating layer.” *Sheu*, p. 3. *Sheu* also specifies that “the present invention provides a field effect transistor, mainly composed of a gallium nitride substrate, a GaN-based semiconductor layer, a GaN-based gate insulating layer, a source/drain and a gate.” *Sheu*, p. 5. Specifically, *Sheu* discloses “a high electron mobility transistor (HEMT).” *Sheu*, p. 9. And *Sheu* claims a column III Nitride transistor: “A field effect transistor, comprising: a gallium nitride substrate.” *Sheu*, claim 1. Because a POSITA would have recognized that GaN is a III Nitride material, a POSITA would have recognized that *Sheu* discloses a “column III Nitride transistor” as recited in [13p].

[0144] In the figure below, *Sheu* illustrates “a structural schematic diagram of a field effect transistor according to a second exemplary embodiment of the present invention.” *Sheu*, p. 9.

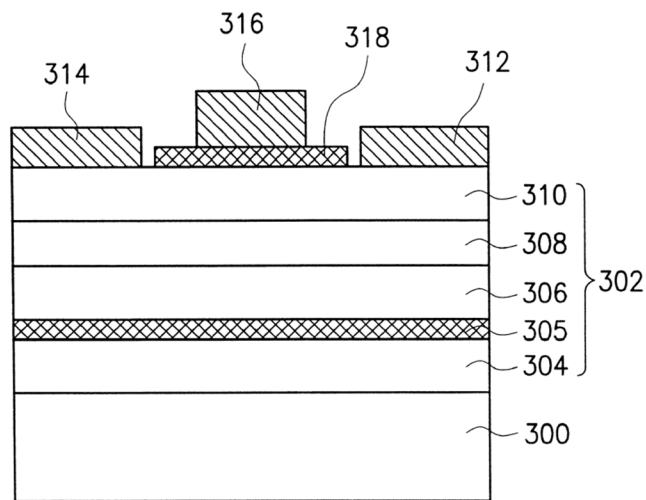


FIG. 6

Sheu, Fig. 6

[0145] Further, a POSITA would have recognized that the transistor *Sheu* discloses in Fig. 6 would operate in “enhancement mode” when layer 318 is p-doped. As shown in Fig. 6 above, *Sheu* discloses a transistor in which a “gate 316” is on top of a “gate insulating layer 318” that is on top of a “barrier layer 310.” *Sheu*, pp. 9-10. *Sheu* additionally discloses the “gate insulating layer 318” being p-type doped with magnesium or a combination of magnesium and iron. *Sheu*, p. 10.

A POSITA would have recognized that when “gate insulating layer 318” is p-type doped *Sheu*'s transistor operates as an enhancement-mode device.

[0146] The formation of an enhancement mode device with a p-type capping layer, like “gate insulating layer 318,” had been known for almost a decade before the '294 patent. As Dr. Suh noted in his thesis “[e]nhancement-mode operation in AlGa_N/Ga_N HEMTs with a p-type gate was first demonstrated by Hu et al. in 2000.” Ex. 1015, 34 (citing Ex. 1014).

[0147] Even Dr. Schubert notes in his declaration that “if a p-type gate material is present over the barrier layer, it can deplete the 2DEG under the gate to create an enhancement mode.” Ex. 2009 ¶31. And that is the same configuration in the *Sheu/Kigami* combination because in *Sheu/Kigami* has a “p-type gate material over the barrier layer,” namely *Sheu*'s p-type doped layer 318 is over barrier layer 310. *Sheu*, p. 10. *Sheu/Kigami* also provides resistivity ranges, specific doping procedures, post-epitaxy conditions, and techniques of how to perform a localized and controlled passivation of the magnesium. *Sheu*, pp. 7-10; *Kigami* ¶[0026]. Therefore, to a POSITA it would have been obvious that in *Sheu/Kigami* the p-type doped layer 318 depletes the 2DEG under the gate at 0 V making disclosing an “enhancement mode ... transistor,” as recited in [13p].

b. [13a] a substrate,

[0148] The *Sheu/Kigami* combination discloses “a substrate” as recited in [13a].

[0149] *Sheu* discloses “a gallium nitride substrate 300.” *Sheu*, p. 9. *Sheu* also states that the “GaN-based semiconductor layer 302 is located on the gallium nitride **substrate 300.**” *Sheu*, p. 9 (emphasis added). *Sheu* additionally discloses alternative substrates: “a silicon substrate is generally used, but for high-speed computing or high operating power integrated circuits, a semiconductor compound substrate with gallium nitride (GaN), gallium arsenide (GaAs) or indium phosphate (InP) as a main material is used.” *Sheu*, p. 3. Annotated Figure 6 below highlights *Sheu*'s **substrate 300**, which discloses [13a].

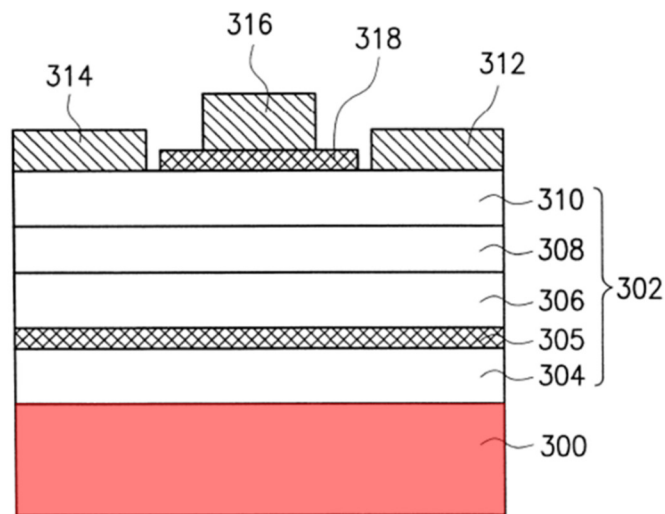


FIG. 6

Sheu, Fig. 6 (annotated)

c. [13b] a set of III-N transition layers above the substrate

[0150] The *Sheu/Kigami* combination discloses “a set of III-N transition layers above the substrate” as recited in [13b].

[0151] *Sheu* discloses a transistor with a “buffer layer 304” and an “isolation layer 305.” *Sheu* explains that the “buffer layer 304” is made of “ $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, and $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $x > a$ ” and the “isolation layer 305” is formed with “ $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ like that of the gate insulating layer 318, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.” *Sheu*, p. 10. *Sheu*'s buffer and isolation layers comprise materials such as AlN and AlGa_N—for example when $a=1$ and $b=0$ in $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ or $x>0$ and $y=0$ in $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$. AlN and AlGa_N are the same materials the '294 patent discloses as the claimed “set of III-N transition layers.” Ex. 1001, 1:59-60 (“transition layers 102 typically composed of AlN and AlGa_N”). Accordingly, *Sheu*'s buffer layer 304 and isolation layer constitute “a set of III-N transition layers,” as recited in [13b].

[0152] Moreover, as annotated Figure 6 below shows, *Sheu* teaches a **buffer layer 304 and isolation layer 305** located above **substrate 300**. *Sheu* thus discloses [13b].

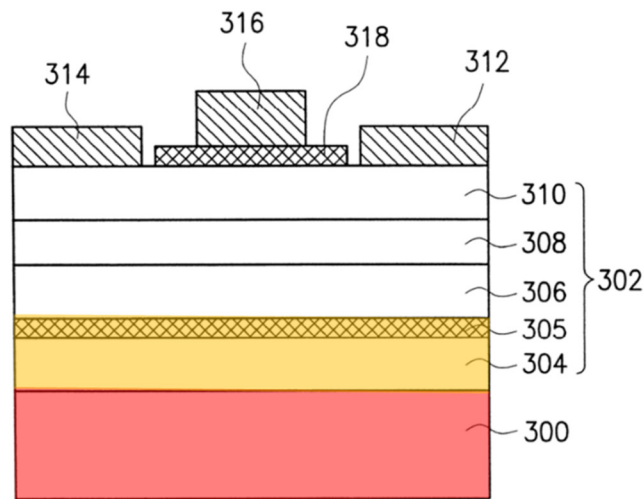


FIG. 6

Sheu, Fig. 6 (annotated)

d. [13c] a III-N buffer layer above the set of transition layers,

[0153] The *Sheu/Kigami* combination discloses “a III-N buffer layer above the set of transition layers” as recited in [13c].

[0154] *Sheu* discloses the transistor includes a “channel layer 306” and a “gap layer 308.” *Sheu*, p. 10. *Sheu* explains that the “channel layer 306” is made of an “Al_aIn_bGa_{1-a-b}N layer, and $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $x > a$ ” and that the “gap layer 308” is made of an “Al_xIn_yGa_{1-x-y}N layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.” *Sheu*, p. 10. The materials for both the “channel layer 306” and a “gap layer 308” encompass GaN—e.g., when $a=0$ and $b=0$ in Al_aIn_bGa_{1-a-b}N and when $x=0$ and $y=0$ in Al_xIn_yGa_{1-x-y}N. GaN is also the same material the '294 patent discloses for the claimed “III-

N buffer layer.” Ex. 1001, 1:60 (“buffer material 103 typically composed of GaN”). Each of *Sheu*'s “channel layer 306” and “gap layer 308” constitutes “a III-N buffer layer” as recited in element [13c].

[0155] Annotated Figure 6, shown below, illustrates *Sheu*'s **channel layer 306 and gap layer 308**, which are located above **buffer layer 304** and **isolation layer 305**.

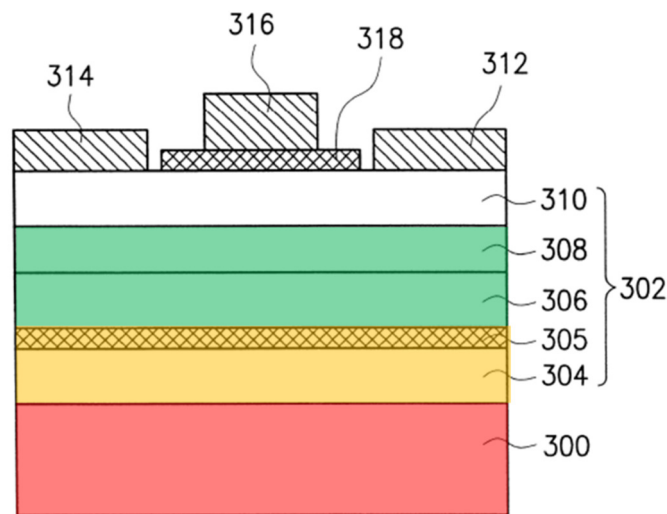


FIG. 6

Sheu, Fig. 6 (annotated)

e. [13d] a III-N barrier layer above the buffer layer,

[0156] The *Sheu/Kigami* combination discloses “a III-N barrier layer above the buffer layer” as recited in [13c].

[0157] *Sheu* discloses the transistor includes a “barrier layer 310.” *Sheu*, p. 10. *Sheu* explains that the “barrier layer 310” is made of “Al_xIn_yGa_{1-x-y}N layer,

and $x \geq 0$, $y \geq 0$, $1 \geq x+y$." *Sheu*, p. 10. *Sheu*'s "barrier layer 310" encompasses AlGa_xN—e.g., when $x > 0$ and $y = 0$ in Al_xIn_yGa_{1-x-y}N. AlGa_xN is the same material the '294 patent discloses as the claimed "III-N barrier layer." Ex. 1001, 1:61-62 ("barrier material 104 typically composed of AlGa_xN where the Al to Ga ratio is about 0.1 to about 0.5"). Accordingly, *Sheu*'s "barrier layer 310" constitutes "a III-N barrier layer," as recited in element [13d].

[0158] As Fig. 6 illustrates below, *Sheu* discloses a **barrier layer 310** located above **channel layer 306** and **gap layer 308**.

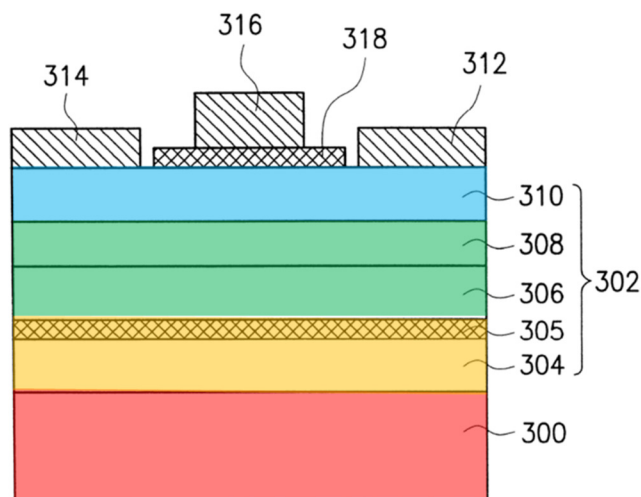


FIG. 6

Sheu, Fig. 6 (annotated)

- f. [13e.1] a semi-insulating III-N layer above the barrier layer,
 - i. Interpretation i: "compensated GaN layer" is a "semi-insulating III-N layer"

[0159] The *Sheu/Kigami* combination renders obvious “a semi-insulating III-N layer above the barrier layer” in [13e.1] under the first interpretation by disclosing a “gate insulating layer 318” that is p-type doped with magnesium and subject to *Kigami*'s hydrogenation.

[0160] *Sheu* teaches that “gate insulating layer 318” is “ $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$,” which includes GaN (e.g., when x and y are 0). *Sheu*, p. 9. As Fig. 6 below illustrates, *Sheu*'s **gate insulating layer 318** is located above **barrier layer 310**. Therefore, *Sheu*'s **gate insulating layer 318** constitutes “a . . . III-Nitride layer above the barrier layer.”

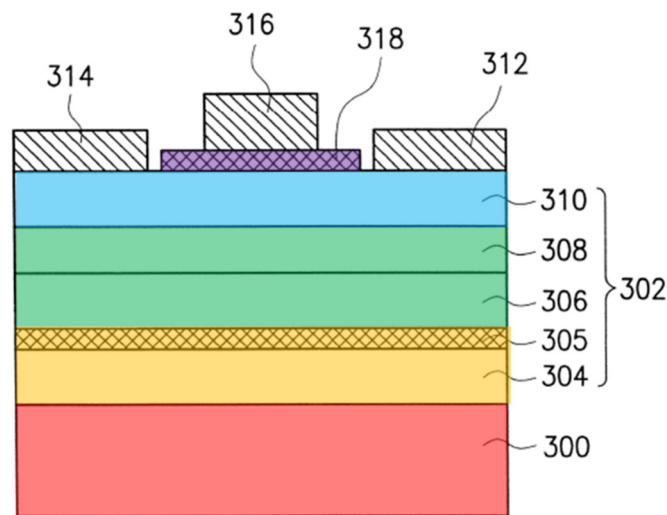


FIG. 6

Sheu, Fig. 6 (annotated)

[0161] Further, in the *Sheu/Kigami* combination, **gate insulating layer 318** is “compensated” under any of the competing claim constructions.

[0162] *Sheu* states that “the GaN-based gate insulating layer 318 . . . may also have a dopant to enhance the resistance value of the GaN-based gate insulating layer 318.” *Sheu*, p. 9. *Sheu* also teaches the resistance value of gate insulating layer 318 is about 10^9 ohms/sq to 10^{12} ohms/sq, and specifies the **gate insulating layer 318** being doped with magnesium. *Sheu*, p. 10.

[0163] Additionally, *Kigami* teaches the intentional passivation of magnesium acceptors in p-type GaN layers, like *Sheu*'s **gate insulating layer 318**, through *Kigami*'s hydrogenation. *Kigami*, [0026]. As I discussed above, a POSITA would have found it obvious to apply *Kigami*'s techniques to **gate insulating layer 318**, and the combination would have resulted in **gate insulating layer 318** being compensated under any of the parties' constructions.

[0164] When *Kigami*'s hydrogenation technique is applied to *Sheu*'s device structure (e.g., to control the resistivity of **gate insulating layer 318**), the **gate insulating layer 318** would be a “doped GaN layer [being] formed with a step to passivate its impurities,” as proposed in Innoscience's construction. Similarly, when *Kigami*'s hydrogenation technique is applied to *Sheu*'s device, the **gate insulating layer 318** is “[a] semiconductor GaN gate material in which one type of

impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor),” as in EPC’s proposed construction.

[0165] Therefore, the *Sheu/Kigami* combination discloses [13e.1] under the first interpretation of “wherein the semi-insulating III-N layer *comprises* a compensated GaN layer” as the “compensated GaN layer” being the “semi-insulating III-N layer.”

ii. Interpretation ii: “compensated GaN layer” is included in a larger “semi-insulating III-N layer”

[0166] The *Sheu/Kigami* combination renders obvious [13e.1] under the second interpretation by disclosing “**gate insulating layer 318**” is doped with combined magnesium and iron and subject to *Kigami*’s hydrogenation.

[0167] *Sheu*’s **gate insulating layer 318** is above **barrier layer 310**. *Sheu*, Fig. 6. Further, a POSITA would have recognized that when *Sheu*’s **gate insulating layer 318** is doped with both magnesium and iron, the layer is a semi-insulating because a POSITA knew that such combined doping (which *Smith* and *Saxler874* describe as “co-doping”) yields a semi-insulating layer. *Sheu*, p. 10; *Smith*, [0085]; *Saxler874*, [0005].

[0168] For example, a POSITA knew that, as explained in *Saxler874* (which I discussed in greater detail in my first declaration), the combination of magnesium

and iron dopants creates a semi-insulating layer. Ex. 1003 ¶¶175-176, 223.

Saxler874 described the “fabrication of a semi-insulating Group III nitride layer [that] includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.” *Saxler874*, [0005]. And *Saxler874* specifies that “[t]he shallow level p-type dopant may be Mg” and “[t]he deep level transition metal dopant may be Fe.” *Saxler874*, [0006]. Therefore, a POSITA would have recognized that, as *Saxler874* explains, the magnesium-iron co-doping *Sheu* describes makes **gate insulating layer 318** semi-insulating.

[0169] Further, *Sheu* describes the **gate insulating layer 318** having a sheet resistance of about 10^9 ohms/sq to 10^{12} ohms/sq (*Sheu*, p. 10), which a POSITA would have identified as a “semi-insulating” resistivity.

[0170] Moreover, *Sheu*'s disclosure of a semi-insulating layer is confirmed by the specific dopant and material *Sheu* discloses for **gate insulating layer 318**. Like the '294 patent, *Sheu* discloses the semi-insulating layer being formed with AlGa_N or Ga_N and doped with iron, a deep level impurity. *Compare Sheu*, pp. 9-10 (describing layer 318 formed with “Al_xIn_yGa_{1-x-y}N, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$ ” and using iron, Fe, as a dopant) with Ex. 1001, 2:66-67 (describing “[s]emi-

insulating layer 39 may comprise, for example, AlGaN or GaN, with deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni”).

[0171] Therefore, the *Sheu/Kigami* combination discloses [13e.1] under the second interpretation of “wherein the semi-insulating III-N layer *comprises* a compensated GaN layer” because, as further discussed below for [13e.2], the **gate insulating layer 318** is “semi-insulating III-N layer” and includes a “compensated GaN layer.”

- g. [13e.2] wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
 - i. Interpretation i: “compensated GaN layer” is a “semi-insulating III-N layer”

[0172] The combination *Sheu/Kigami* renders obvious “wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen” of [13e.2] under the first interpretation that the “compensated GaN layer” is a “semi-insulating III-N layer.” As I explained for limitation [13e.1], when *Sheu's* **gate insulating layer 318** is doped with magnesium and subject to *Kigami's* hydrogenation, **gate insulating layer 318** renders obvious a “compensated GaN layer” under any proposed construction. See above §VI.A.2.f.

[0173] Further, the *Sheu/Kigami* combination also meet the limitation of the “compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen” because *Sheu* specifies **gate insulating layer 318** is doped with magnesium (i.e., the layer contains acceptor type dopants), that get passivated with the hydrogen introduced via *Kigami*'s hydrogenation.

ii. Interpretation ii: “compensated GaN layer” is included in a larger “semi-insulating III-N layer”

[0174] The *Sheu/Kigami* combination renders obvious [13e.2] “wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopants passivated with hydrogen” under the second interpretation. As discussed above, embodiments of **gate insulating layer 318** that use the combination of magnesium and iron doping (i.e., co-doping) meet the “semi-insulating III-N layer.” See above §VI.B.2.f.ii .

[0175] Further, when *Kigami*'s hydrogenation is applied to locally passivate magnesium in a region of **gate insulating layer 318, gate insulating layer 318** would comprise a “compensated GaN layer” under any of the proposed constructions.

[0176] *Kigami* explains that its technique allows the formation of a layer in which “hydrogen atoms are unevenly distributed in a local region of the III-V

group compound semiconductor.” *Kigami*, [0008] (emphasis added). *Kigami* also explains that with its hydrogenation technique “the region into which the hydrogen atoms are to be introduced, the concentration distribution of the hydrogen atoms to be introduced, and the like can be adjusted by forming in advance on the front-surface side of the semiconductor device 10 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these.” *Kigami*, [0026].

[0177] To a POSITA it would have been obvious to apply *Kigami*'s technique to form a **gate insulating layer 318** having an uneven hydrogen distribution. And with such implementation, with uneven hydrogen distribution, **gate insulating layer 318** would have some of the regions having hydrogen concentration that passivates the magnesium dopants (making the layer compensated GaN) but others not (remaining co-doped and semi-insulating).

[0178] An example a **gate insulating layer 318** with uneven hydrogen distribution is exemplified below.

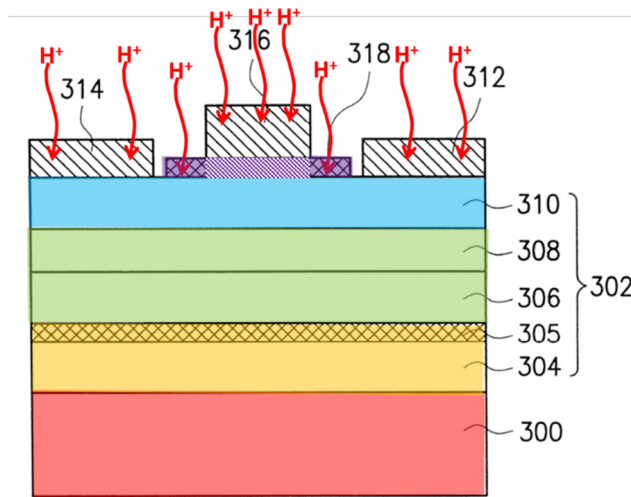


FIG. 6

Sheu, Fig. 6 (modified)

[0179] As shown in the example above, to a POSITA it would have been obvious to implement *Kigami*'s technique with uneven hydrogen distribution so that the areas immediately below gate 316 (marked with a purple-hashed pattern) have a lower hydrogen concentration than the regions not immediately below gate 316 (and thus more exposed to *Kigami*'s hydrogenation, shown as purple without hashed pattern). In this implementation, for example, gate 316 would be formed with one of the "material[s] through which it is difficult for hydrogen ions to pass" *Kigami* discloses. *Kigami*, [0026].

[0180] To a POSITA it would have been obvious to implement *Kigami*'s hydrogenation as exemplified in the drawing above based on *Kigami*'s teachings

and to, for example, adjust effect of the insulating layer 318 to the 2DEG and/or reduce leakage current. A POSITA would have been motivated to experiment with different uneven distributions because, as I discussed above, a POSITA knew about the relationship between active acceptors and 2DEG depletion. See above §V.C. Additionally, a POSITA knew that localized passivation (e.g., in edges as shown in the figure above) would reduce gate leakage current. As one example, prior art *Uemoto* discloses the passivation of regions of the capping layer, similar as the example above, to reduce leakage current. *Uemoto*, [0061], Fig. 7.

[0181] With the uneven hydrogen distribution *Kigami* teaches, and as exemplified above, **gate insulating layer 318** would be a “semi-insulating layer” that comprises “a compensated GaN layer.” In the example, the left and right sides of **gate insulating layer 318**, the semi-insulating layer, would be “compensated GaN layer[s],” under both of the parties’ proposed construction for the term.

[0182] The example, above, however, should not be considered limiting. I can envision other implementations with different hydrogen distributions based on *Kigami*’s teachings. For example, to a POSITA it would have been obvious to form **gate insulating layer 318** with uneven hydrogen distributions where the hydrogen concentration is higher at the top than on the bottom, or where the hydrogen

distributions in which the hydrogen concentrations is higher immediately below gate 316.

[0183] Further, the compensated GaN layer(s) of **gate insulating layer 318** would contain “acceptor type dopant atoms passivated with hydrogen,” as recited in [13e.2]. In the example above the compensated GaN layers (in the left and right of **gate insulating layer 318**) would have acceptor type dopants atoms (the magnesium from *Sheu*) that gets passivated with hydrogen (the hydrogen introduced with *Kigami*'s localized hydrogenation).

[0184] Therefore, under the second interpretation of [13e.2] where the “compensated GaN layer” is included within a larger “semi-insulating III-N layer,” the *Sheu/Kigami* combination renders obvious a “compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen.”

- h. [13f] a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.**

[0185] *Sheu/Kigami* render obvious [13f] under both interpretations of [13e.2].

- i. Interpretation i: “compensated GaN layer” is a “semi-insulating III-N layer”**

[0186] The *Sheu/Kigami* combination renders obvious [13f] under the first interpretation by disclosing a “gate 316,” which is a gate contact and is on top of the **gate insulating layer 318** and thus forming “a gate comprising a gate contact and the compensated GaN layer.”

[0187] *Sheu* discloses a transistor with a “gate 316.” *Sheu*, p. 9. According to *Sheu*, “the gate 316 is . . . provided on the GaN-based gate insulating layer 318.” *Sheu*, p. 9. *Sheu*'s Fig. 6 shows **gate 316**, which is a gate contact, and **gate insulating layer 318**, the “compensated GaN layer,” forming “gate comprising a gate contact and the compensated GaN layer.”

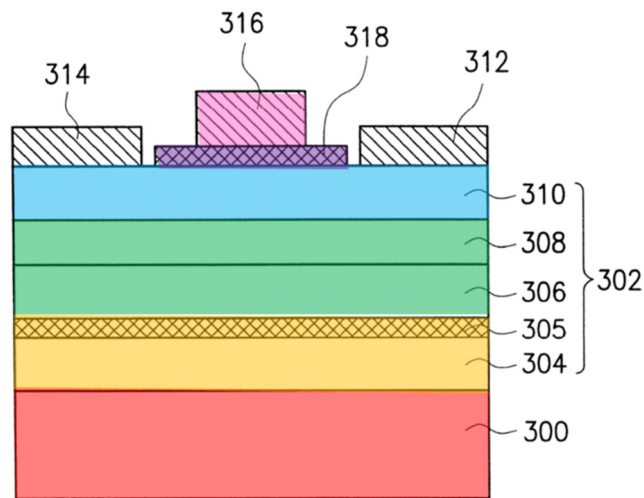


FIG. 6

Sheu, Fig. 6 (annotated)

[0188] Further, while the *Sheu/Kigami* combination does not explicitly disclose “wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias,” such feature would have been obvious because, as I explained above, the *Sheu/Kigami* combination results in an enhancement mode device.

[0189] As I explained above, the *Sheu/Kigami* combination renders obvious an “enhancement mode” limitation because *Sheu* describes **gate insulating layer 318** as being p-type doped, specifically doped with magnesium. See above §VI.B.2.a. With such configuration, having a p-doped layer below the gate, and above an AlGa_N barrier layer, *Sheu* discloses an enhancement mode device. See above §VI.B.2.a; Ex. 2009 ¶31 (“if a p-type gate material is present over the barrier layer, it can deplete the 2DEG under the gate to create an enhancement mode”).

[0190] Because a POSITA would have recognized *Sheu* discloses an enhancement-mode transistor when **gate insulating layer 318** is p-type doped with magnesium, to a POSITA it would have been obvious that in *Sheu/Kigami* “no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.” To a POSITA it would have been obvious that the p-type

doping in **gate insulating layer 318** would deplete the 2DEG below the gate at zero bias.

ii. Interpretation ii: “compensated GaN layer” is included in a larger “semi-insulating III-N layer”

[0191] Under the second interpretation, the *Sheu/Kigami* combination also renders obvious “a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias” as recited in the claim.

[0192] *Sheu* discloses a gate contact by describing a **gate 316** and the *Sheu/Kigami* combination discloses the compensated GaN layer by describing portions of **gate insulating layer 318** with higher hydrogen concentration where hydrogen from *Kigami*'s hydrogenation passivate *Sheu*'s magnesium dopants. See above §VI.B.2.g. In the *Sheu/Kigami* combination, therefore, *Sheu*'s **gate insulating layer 318** and **gate 316** constitute a “gate comprising a gate contact and the compensated GaN layer,” as recited in [13f].

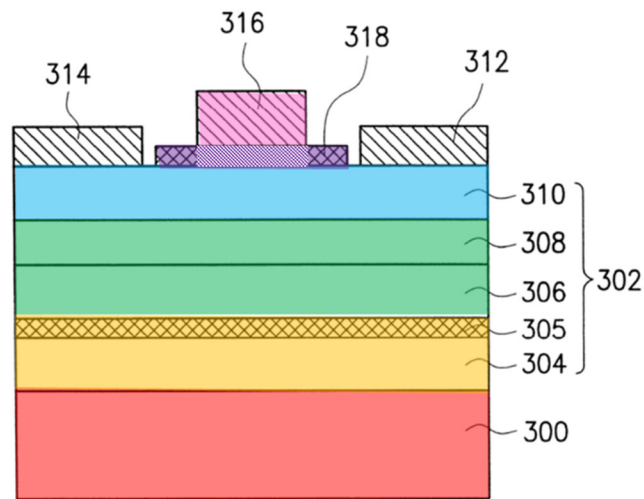


FIG. 6

Sheu, Fig. 6 (Annotated)

[0193] Further, as noted above, while the *Sheu/Kigami* combination does not explicitly disclose “wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias,” such feature would have been obvious because the *Sheu/Kigami* combination results in an enhancement mode device. When doped with magnesium and iron, *Sheu*’s **gate insulating layer 318** is “a p-type gate material [that] is present over the barrier layer[and] can deplete the 2DEG under the gate to create an enhancement mode.” Ex. 2009 ¶31. With such configuration, *Sheu* discloses an enhancement mode device when **gate insulating layer 318** is co-doped with magnesium and iron. See above §VI.B.2.a. To a

POSITA it would have been obvious that the p-type doping in **gate insulating layer 318** would deplete the 2DEG below the gate at zero bias.

3. Independent Claim 14

a. [14p] A compensated gate enhancement mode MISFET transistor comprising:

[0194] The *Sheu/Kigami* combination discloses “A compensated gate enhancement mode MISFET transistor,” as recited in [14p].

[0195] As noted above regarding [13p], *Sheu/Kigami* discloses a “compensated gate enhancement mode ... transistor” by disclosing layer 318 is p-type doped with magnesium and subject to *Kigami*'s hydrogenation. See above §VI.B.2.a. Additionally, the *Sheu/Kigami* combination discloses its transistors being MISFETs. *Sheu*, pp. 4-5. *Sheu* discloses that it seeks a “metal-insulating layer-semiconductor field effect transistor (MISFET) [that] has good electrical characteristics.” *Sheu*, pp. 4-5.

[0196] And as shown below, *Sheu* discloses the MIS transistor structure disclosing a metal (gate 316), on an insulating layer (gate insulating layer 318), on a semiconductor (barrier layer 310).

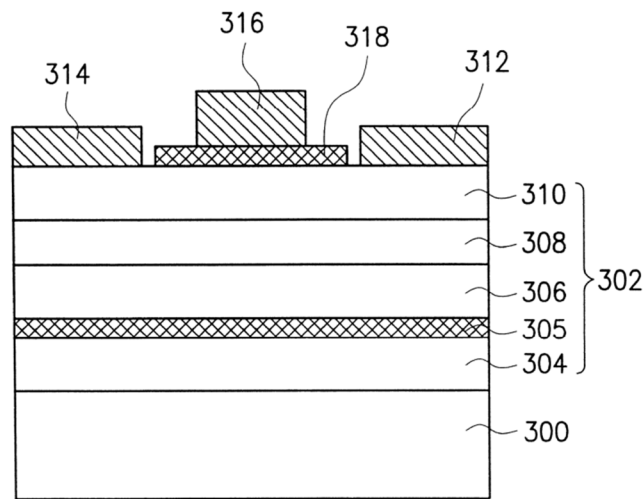


FIG. 6

Sheu, Figure 6

[0197] Therefore, *Sheu/Kigami* discloses a “compensated gate enhancement mode MISFET transistor.”

b. [14a] a III-N barrier layer beneath a gate contact,

[0198] *Sheu* meets [14a] by disclosing a “**barrier layer 310**” that is beneath the “**gate 316**.” *Sheu*, p. 10. As Fig. 6 illustrates below, *Sheu* discloses a **barrier layer 310** located beneath **gate 316**.

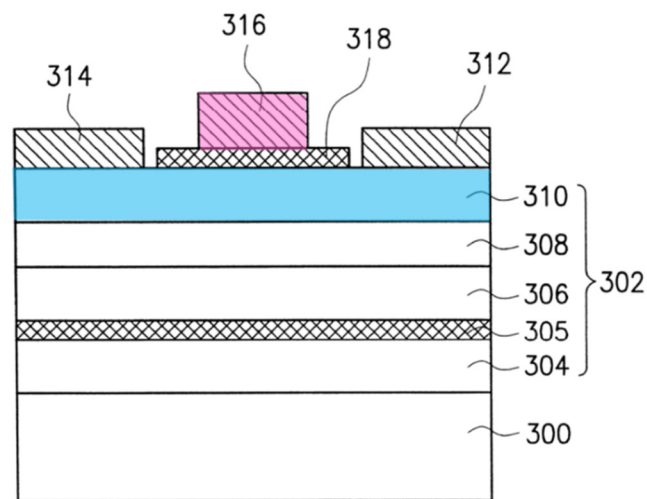


FIG. 6

***Sheu*, Figure 6 (Annotated)**

c. [14b] a drain contact, a source contact,

[0199] The *Sheu/Kigami* combination discloses “a drain contact, a source contact,” as recited in [14b] by disclosing “a source 312, a drain 314.” *Sheu*, p. 9.

Fig. 6 below shows the source 312 and the drain 314 in *Sheu*'s transistor.

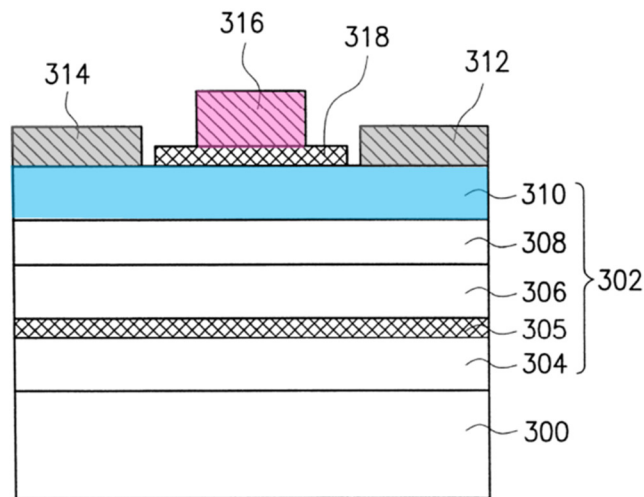


FIG. 6

Sheu, Figure 6 (Annotated)

- d. [14c.1] a semi-insulating III-N layer between the barrier layer and the gate contact,

[0200] Limitations [14c.1] and [13e.1] both require “a semi-insulating III-N layer.” As explained in [13e.1], the **gate insulating layer 318** in the *Sheu/Kigami* combination renders obvious the claimed “semi-insulating III-N layer” under either interpretation of “wherein the semi-insulating III-N layer comprises a compensated GaN layer.” See above §VI.B.2.f.

[0201] Limitation [14c.1] additionally requires that the “semi-insulating III-N layer is *between the barrier layer and the gate contact*.” As shown below, *Sheu* discloses that **gate insulating layer 318** is between **gate 316** and **barrier layer 310**.

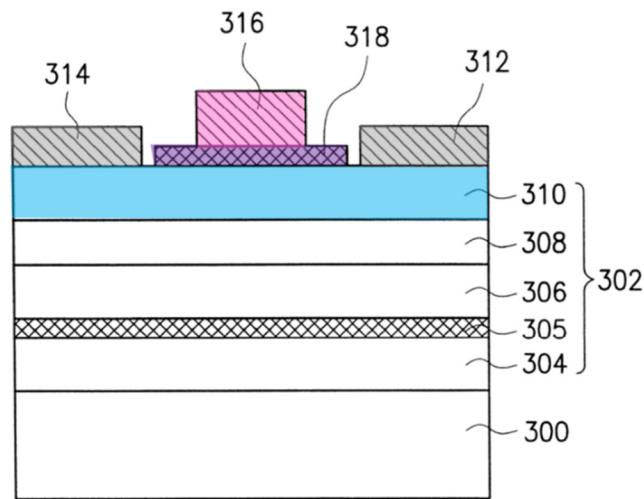


FIG. 6

Sheu, Figure 6 (Annotated)

- e. **[14c.2] wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and,**

[0202] Elements [14c.2] and [13e.2] are the same. As I explained in [13e.2],

Sheu/Kigami render obvious this limitation under either interpretation of [14c.2].

See above §VI.B.2.g.

- f. **[14d] a gate comprising the gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.**

[0203] Limitations [14d] and [13f] are the same. As I explained in [13f],

Sheu/Kigami render obvious this limitation under either interpretation of [14c.2].

See above §VI.B.2.h.

VII. MATERIALS CONSIDERED

[0204] In forming my opinions, I read and considered the '294 patent and its prosecution history, the exhibits listed in the Exhibit List filed with the Petition for *inter partes* review of the '294 patent, as well as any other materials referenced herein. I have reviewed the following at least the following documents:

Exhibit	Description
Ex. 1001	U.S. Patent No. 8,350,294 B2 to Lidow et al. ("the '294 patent")
Ex. 1002	Prosecution History of the '294 Patent (" <i>Prosecution History</i> ")
Ex. 1005	U.S. Patent Application Publication No. US 2007/0164315 A1 to Smith et al. (" <i>Smith</i> ")
Ex. 1006	U.S. Patent Application Publication No. US 2008/0087915 A1 to Uemoto et al. (" <i>Uemoto</i> ")
Ex. 1007	Japanese Patent Publication No. JP2006-253224 A to Kigami et al.
Ex. 1008	Certified English Translation of Japanese Patent Publication No. JP2006-253224 A (" <i>Kigami</i> ")
Ex. 1009	Translator's Declaration for Certified English Translation of JP 2006-253224 A to Kigami et al.
Ex. 1010	Umesh K. Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, vol. 90, no. 6 (June 2002), pp. 1022-1031 (" <i>Mishra</i> ").
Ex. 1011	Excerpts of Rüdiger Quay, <i>Gallium Nitride Electronics</i> , vol. 96, Springer Science & Business Media (2008) (" <i>Quay</i> ").

Exhibit	Description
Ex. 1012	Excerpts of Stephen J. Pearton et al., <i>Gallium Nitride Processing for Electronics, Sensors and Spintronics</i> , Springer Science & Business Media (2006) (“ <i>Pearton</i> ”).
Ex. 1013	U.S. Patent Application Publication No. US 2004/0012015 A1 to Saxler (“ <i>Saxler015</i> ”)
Ex. 1014	X. Hu et al., <i>Enhancement mode AlGaIn/GaN HFET with selectively grown pn junction gate</i> , Electronics Letters, vol. 36, no. 8 (2000), pp. 753-754 (“ <i>Hu</i> ”).
Ex. 1015	Excerpts of Chang Soo Suh, Enhancement-Mode GaN-Based HEMTs for High-Voltage Switching Applications (Dec. 2008) (Ph.D. dissertation, University of California, Santa Barbara) (“ <i>Suh</i> ”).
Ex. 1016	U.S. Patent Application Publication No. US 2005/0145874 A1 to Saxler (“ <i>Saxler874</i> ”)
Ex. 1017	Chris G. Van de Walle et al., “Hydrogen in III-V Nitrides,” <i>Semiconductors and Semimetals</i> , vol. 57 (1998), pp. 157-184 (“ <i>Van de Walle</i> ”).
Ex. 1018	Shuji Nakamura et al., <i>Hole Compensation Mechanism of P-Type GaN Films</i> ,” Japanese Journal of Applied Physics, vol. 31 (1992), pp. 1258-1266 (“ <i>Nakamura</i> ”).
Ex. 1019	Complainant's Proposed Constructions & Respondents' Proposed Constructions in related International Trade Commission investigation: <i>In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same</i> , Inv. No. 337-TA-1366, dated September 5, 2023 (“ <i>ITC Constructions</i> ”).
Ex. 1020	U.S. Patent No. 5,985,687 to Bowers et al. (“ <i>Bowers</i> ”)

Exhibit	Description
Ex. 1021	U.S. Patent Application Publication No. 2002/0167023 A1 to Chavarkar et al. (" <i>Chavarkar</i> ")
Ex. 1022	U.S. Patent Application Publication No. 2003/0102482 A1 to Saxler (" <i>Saxler482</i> ")
Ex. 1023	Shuji Nakamura – Biographical, NobelPrize.org, Nobel Prize Outreach AB 2023, www.nobelprize.org/prizes/physics/2014/nakamura/biographical/ (last visited Aug. 28, 2023) (" <i>Biographical Nakamura</i> ")
Ex. 1024	Excerpts of Vasco Matias, Defect characterization of Europium implanted Gallium Nitride (2008) (Ph.D. dissertation, KU University, Belgium) (" <i>Matias</i> ").
Ex. 1031	Exhibit 28 to Verified Complaint in International Trade Commission <i>Certain Semiconductor Devices, And methods Of Manufacturing Same And Products Containing the Same</i> . Inv. No. 337-TA-1366.
Ex. 1032	Exhibit RX-0255 in Inv. No. 337-TA-1366. Book: E. Fred Schubert. Doping in III-V semiconductors. AT&T Bell Laboratories, New Jersey. (1993)
Ex. 1034	Excerpts of Revised and Corrected Transcript, Open Sessions, Inv. No. 337-TA-1366
Ex. 1035	Taiwanese Patent Publication No. TW200414540A to Sheu et al.
Ex. 1036	Certified English Translation of Taiwanese Patent Office Publication No. TW200414540A (" <i>Sheu</i> ")
Ex. 1037	Translator's Declaration for Certified English Translation of TW200414540A.

Exhibit	Description
Ex. 1038	C. S. Suh et al., "p-GaN/AlGaIn/GaN Enhancement-Mode HEMTs," 2006 64th Device Research Conference, June 2006, pp. 163-164 (" <i>Suh2006</i> ")

[0205] I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

VIII. CONCLUSION

[0206] For the reasons set forth above, in my opinion, claims 13 and 14 are not supported by the patent and a POSITA would have faced undue experimentation to make the claimed transistors. It is my further opinion that a person of ordinary skill in the art would have found claims 13-14 of the '294 patent obvious over the prior art.

[0207] In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

[0208] I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 4, 2024

By: James R. Shealy
James Richard Shealy, Ph.D.