



# GaN-Based Lateral and Vertical Devices

# 15

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## Abstract

In the last decade, GaN has emerged as an excellent material for application in power electronics. The wide energy gap of gallium nitride (3.4 eV) enables high-temperature operation, while the large breakdown field (3.3 MV/cm, 11 times higher than silicon) allows to reach kV-range operation while maintaining a low on-resistance. Thanks to the high mobility of the two-dimensional electron gas at the AlGaN/GaN interface, lateral GaN transistors have a very low on-resistance; commercial products are already on the market, and new technologies are being developed, targeting the 650 V/900 V ranges. Recently, the attention toward vertical GaN transistors has constantly increased: a vertical layout allows to substantially increase current density while taking advantage of the wide bandgap and high breakdown field of GaN. Vertical transistors based on GaN are expected to find application in converters with medium high power levels (>5 to 10 kW), once the technology reaches maturity.

This chapter reviews the main properties of GaN-based materials and devices. The first part focuses on the main challenges related to the growth of high-quality GaN epitaxial stacks. The second and the third parts focus on GaN lateral and vertical devices, respectively. Finally, the fourth section describes the trapping and degradation

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processes that limit the performance and the reliability of GaN transistors, and the related physical mechanisms. This chapter represents an ideal guide for a reader willing to enter the world of GaN devices.

### Keywords

GaN · Technology · Gallium nitride · Reliability · Transistor · III-V

## 15.1 GaN Material and Epitaxy

When GaN-based white LED's became the technology to beat for lighting applications after some major technological hurdles were overcome, such as the development of a workable epitaxy regime [1], scientific interest was aroused to use this material system also for purely electronic applications. By taking advantage of the strong polarization fields in the III-nitrides, which limit the performance of quantum well-based light emitters because of the quantum confined Stark effect [2], a unique structure for transistor channels was devised: the GaN/AlGaIn high electron mobility transistor (HEMT) [3]. These lateral transistor devices can handle very large power densities due to the combination of the good transport properties on the one hand and of the excellent voltage handling capabilities on the other hand, courtesy of the material's high bandgap and critical electrical field. From epitaxy point of view, these two types of applications are characterized by a number of distinct differences.

For opto-electronics, the substrate of choice is sapphire, as it is optically transparent, relatively easy to perform hetero-epitaxy on and can be reused several times by taking advantage of the laser lift-off technique [4]. For electronic applications, sapphire has a major shortcoming in terms of its low thermal conductivity which causes trouble with thermal dissipation in high power density devices. Instead, the traditional choice for substrates for electronic applications is SiC, while in the recent years Si has become a very popular choice as well.

A second major difference between the two types of application is the range of alloys that is typically used. For the bulk of lighting applications, LEDs need to cover the visible range of the optical spectrum which is done by using InGaIn alloys in combination with n- and p-doped GaN layers. Because of the volatility of Indium and the miscibility issues in InGaIn alloys [5], epitaxy of such layers is performed at relatively low temperatures, roughly between 700 °C and 900 °C for MOCVD processes. For electronic applications, the critical electric field of the materials is an important parameter, which scales directly with the bandgap of the semiconductor materials. As a result, layers stacks for electronic applications typically consist of AlGaIn alloys that require a rather different epitaxial regime, e.g., characterized

by the higher growth temperatures (above 1000 °C when grown by MOCVD) to obtain the best material quality.

Obviously, the layer stack designs differ significantly as well: p-i-n diodes for LEDs as opposed to the undoped HEMT hetero-structures for lateral transistors.

### 15.1.1 Typical Layer Stacks for Lateral GaN Power Transistors

The lack of availability of native GaN substrates in large wafer diameters and at reasonable cost forces the GaN community to use hetero-epitaxy to grow III-nitride materials on foreign substrates, such as sapphire, silicon, or silicon carbide. The intrinsic mismatches between substrate and epitaxial materials, for instance, in terms of lattice constant or thermal expansion coefficient, prevent the direct growth of the active HEMT layers on top of the substrate. Instead, a relatively complex buffer stack needs to be inserted in between. Figure 15.1 shows the typical construction of the epitaxial layer stack, together with the most commonly used implementations. We will discuss the different variations below.

### 15.1.2 Substrates, Nucleation, and Strain Management

For electronic applications, typically two substrate types are used: silicon carbide (SiC) and silicon (see Table 15.1). Sapphire, which is the substrate of choice for the LED business, is not used because of its low thermal conductivity that becomes a reliability issue for transistors that operate at and dissipate high power densities.

### 15.1.3 Growth on SiC Substrates

For most RF applications, SiC is used as a substrate, first because of its relatively low lattice mismatch with GaN that allows a very simple nucleation and buffer structure and secondly because of its high thermal conductivity. In practice, the layer stack as depicted in Fig. 15.1 is simplified to consist of a thin AlN nucleation layer, a GaN-based confinement layer (typically unintentionally doped or Fe-doped) with a thickness of roughly 1 μm and the active channel/barrier layer combination.

Most SiC substrates are wafered from SiC bulk crystals that are grown using the Physical Vapor Transport (PVT) method [6]. The latter operates at temperatures exceeding 2000 °C, provides low growth velocities, and is thus very energy intensive. The typical crystals that can be obtained by PVT are typically only 20–30 cm long and yield only a limited number of wafers. As a result, SiC wafers are 20–50 times more expensive than their Silicon counterparts.

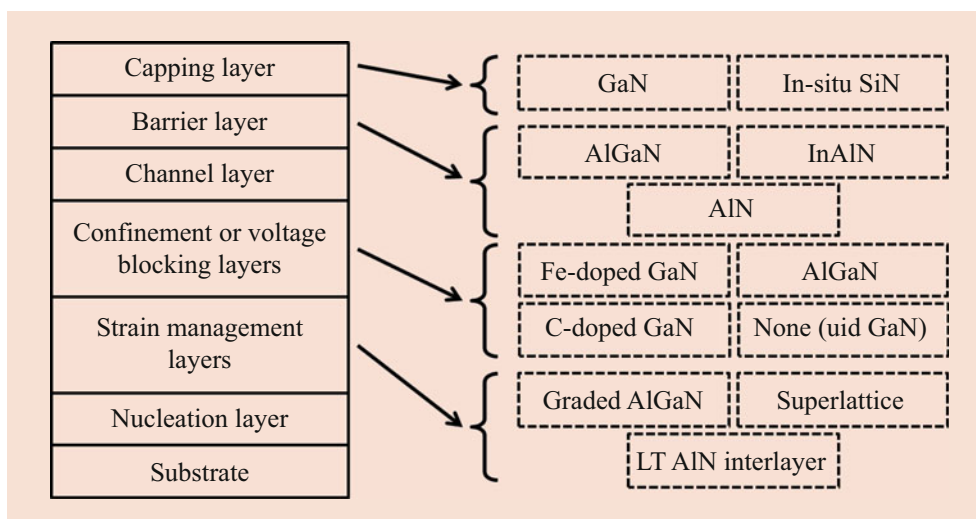


**Fig. 15.1** Layer stack variations for GaN electronics

**Table 15.1** Properties of commonly used substrate materials

| Substrate materials                                | GaN  | SiC   | Sapphire | Si    |
|----------------------------------------------------|------|-------|----------|-------|
| Lattice constant (Å)                               | 3.19 | 3.08  | 4.76     | 5.43  |
| Mismatch to GaN                                    | 0    | −3.6% | 33.0%    | 41.3% |
| Thermal expansion coefficient (10 <sup>−6</sup> K) | 5.59 | 4.3   | 7.3      | 3.59  |
| Mismatch to GaN                                    | 0    | 30.0% | −23.4%   | 55.7% |
| Thermal conductivity (W/cmK)                       | 1.3  | 4.9   | 0.23     | 1.4   |

Moreover, scaling the diameter of the crystal boule has been proven difficult. Only recently has the industry made the step from 4" to 6" diameters, with however still some quality issues remaining to be solved for the outer ring of the 6" substrates. 200 mm SiC has been demonstrated but is currently not commercially available in large quantities.

#### 15.1.4 Growth on Si Substrates

Over the last 15 years, a lot of effort has been spent to develop an epitaxy process to grow GaN directly on Si substrates (Krost). Being able to work on Si is very appealing: it is obviously the material of choice on which the bulk of the semiconductor industry is built (e.g., for logic and memory applications). Si manufacturing technology is extremely mature (yields well above 95%), very cost effective and capable of mass production (hundreds of thousands of wafers per month). Besides the cost advantage compared to SiC, one of the main drivers to select Si substrates is that it allows for much more easy integration of GaN-based devices with circuitry manufactured in Silicon-based CMOS. This is due to ease of back-side processing (e.g., wafer thinning or through-Si-via processing using the Bosch process) as well as

due to the fact that there is no mismatch in material properties (thermal expansion coefficient being a good example).

Unfortunately, the hetero-epitaxy of GaN on Si comes with a plethora of challenges. For starters, the electronically most suitable type of GaN comes in a hexagonal close packed crystal structure (also called Wurtzite), which doesn't match the crystal structure of Si: the face-centered cubic crystal structure. The typical technical work-around is to use the triangular symmetry of the <111> plane of the Si.

Although many epitaxial techniques exist such as molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE), or liquid phase epitaxy (LPE), almost all production of GaN epitaxial layers is performed by a technique called metal-organic chemical vapor deposition (MOCVD) or metal-organic vapor phase epitaxy (MOVPE). In this technique, the growth temperature for high-quality GaN or AlGaIn layers is above 1000 °C. At these temperatures, Ga attacks the Si substrate because of the eutectic lowering of the melting point of the materials; a phenomenon called Ga melt-back of Si [7]. As a result, one cannot directly grow GaN on Si, but one needs to insert a layer of a different material. As on SiC, the solution is to grow an AlN nucleation layer that not only constitutes a good starting crystal for consecutive epitaxial growth but that also protects the Si from Ga-containing molecules in the vapor phase. Different solutions with other intermediary layers exist such as the use of 3C-SiC or rare earth oxides, but these lack the elegance and simplicity of using an in situ grown layer.

The nucleation process is an important one, because the extended defects that originate in this layer tend to propagate as threading dislocations through the entire layer stack that is built on top. Because of the reactivity of both species and the strong bond strength between aluminum and nitrogen, the growing AlN has low surface mobility and as a result,

the growth occurs by the formation of many separate AlN islands that laterally expand and coalesce. The locations where the islands meet are a source for many kinds of 1D and 2D extended defects. For the same reasons as mentioned above, AlN easily reverts to a three-dimensional growth mode (Volmer-Weber or Stanski-Krastanov) thus forming pyramids, rather than the preferred two-dimensional layer-by-layer growth mode (Frank-van der Merwe). This easily leads to surface roughening.

It has been shown that the properties of the interface between the Si and the AlN is of major importance both for high-voltage power switching as well as for RF power applications. In the former case, lateral conductivity along this interface causes the premature breakdown of lateral devices (as will be explained in Sect. 15.2 of this chapter), whereas for the latter case, the conductive interface causes RF losses for propagating signals and efficiency degradation in amplifiers.

There are more issues with GaN-on-Si epitaxy. As indicated in Table 15.1, GaN and Si have rather different thermal expansion coefficients. Even when one manages to employ the nucleation techniques as described above to grow high-quality GaN material, the cool-down step of over 1000 °C after epitaxy induces a substantial amount of tensile stress in the GaN epilayers, proportional to the thickness thereof. This is especially critical for high-voltage applications where the vertical voltage rating scales linearly with the thickness of the epilayer stack, requiring for instance a more than 5  $\mu\text{m}$  thick layer stack for a 650 V rated device. Without controlling this issue, GaN-on-Si wafers tend to have significant bow and warp and are prone to the formation of cracks or even wafer breakage [8].

Over the years, several solutions were proposed to compensate for this tensile strain formation. They are all based on the principle of designing a buffer that generates an equal amount of compressive stress. In this way, it is possible to manufacture GaN-on-Si wafers that are perfectly flat; yet it is important to understand that such flat wafers are never stress-free but merely well stress-compensated. There is a second implication as well: the total amount of compressive stress that may be generated by the buffer is limited by the onset of plastical deformation of the Silicon substrate. This means that, depending on the thickness of the Silicon substrate, there is an upper limit to the total thickness of the III-nitride epilayer that can be grown on top.

The first type of strain management buffer is based on graded AlGaIn layers. On top of the AlN nucleation layer, AlGaIn layers are deposited where the Al composition is reduced, either continuously or in discrete steps, from 100% (AlN) down to 0% (GaIn). In this configuration, AlGaIn layers with lower Al content have a larger lattice constant than the AlGaIn material beneath, and the pseudomorphic growth of the former forces them to be compressed. Because of the

finite composition range of the AlGaIn and the presence of strain relaxation effects, the maximum layer thickness that can be deposited in this way is limited to 6–7  $\mu\text{m}$ .

An alternative approach consists of the use of the so-called low-temperature AlN interlayers. Here the GaN layer growth is repeatedly interrupted to introduce a thin AlN layer that is grown at very low temperatures (e.g., 700 °C). In these conditions, the AlN will not build up strain internally because of the even further reduced surface mobility, and it very quickly relaxes to its native in-plane lattice constant (3.11 Å) which is lower than the one of the GaN (3.19 Å). Then, in a next step under “normal” growth conditions, the growth of the GaN is continued and generates compressive strain in a similar way as described above. This process can be repeated several times. The main drawback of this approach is the poor quality of the AlN interlayers themselves (due to the low growth temperature) which can impact the electrical behavior of the layer stack, for instance, in terms of leakage current or trapping effects.

The second alternative approach which is today widely employed for high voltage power switching applications is the use of strained superlattice (SSL) buffers. These consist of a large number of repetitions (e.g., 100–150 times) of a bilayer made up out of 5–20 nm thin AlN and (Al)GaIn layers. By keeping the thicknesses of the individual layers below their critical thickness, the total strain of the superlattice can be controlled by varying the ratio between the thicknesses of the two constituent layers.

### 15.1.5 Back-Barrier Selection

Besides the chemical and mechanical considerations, the layers below the HEMT heterostructure also play an important electrical role. This is obviously the case in the devices’ off-state, where the electric field extends into and causes a depletion of the buffer layers where it induces electrical stress that may lead to leakage and time-dependent breakdown effects. However, the presence of traps in the buffer layers can also lead to a degradation of the devices’ on-state behavior: the so-called current collapse (see further, e.g., Figs. 15.8 and 15.9). The electrical requirements for the buffer layers directly under the GaN channel layer also depend on the application.

GaN-on-Si is attracting a lot of interest for power switching applications especially for devices rated at 600 V or 650 V. One of the requirements of the circuit designers is that there are no floating potential nodes, which implies that also the substrate is grounded. As a result the GaN-on-Si stack has to be capable of handling about twice the rated voltage to be able to cope with inductive voltage spikes and to guarantee a reasonable lifetime. The total voltage is split over the strain

management layers (that are typically designed with only the strain aspect in mind) and over the voltage blocking layers.

One attractive implementation for the voltage blocking layers is to use impurity-doped GaN. One can for instance increase the resistivity of GaN by incorporating deep acceptor levels in the form of Carbon-doping. In an MOCVD process, carbon is available from the source molecules for the group III elements (e.g., from methyl groups), so by modifying the thermodynamic growth conditions, the amount of Carbon that is incorporated in the epilayers can be tuned. Alternatively, one can opt for a dedicated dopant source gas for carbon, such as ethylene or methane, to allow a wider parameter space for the epitaxial conditions. Substantial amounts of work have been performed by various groups to understand and control the effect of such Carbon doping. Moens et al. showed that a layer stack as described above can be modelled as a leaky dielectric [9], with two regimes of current conduction below and above a certain critical voltage. One concern with deep acceptor levels is that they may serve as a trapping state causing current collapse. Also in this respect, different models have been proposed. Uren et al. showed the importance of charge redistribution between the 2DEG and the carbon-doped layer [10], while Verzellesi et al. [11] described the effect of how the carbon is incorporated into the crystal lattice on its trapping behavior.

For RF applications, one of the main device features is the use of short gate lengths which create very high electric field peaks at the drain edge of the gate that can cause punch-through [12]. When using a thick (i.e., more than 200–300 nm) unintentionally doped GaN channel layer with the gate pinched off, the 2DEG carriers may be pushed out of the quantum well and still travel from drain to source through the lower part of the GaN channel layer. This induces a bias-dependent off-state leakage current and a degradation of the sub-threshold slope. To prevent this effect, the carriers need to be better confined into the 2DEG quantum well by modifying the layer stack directly under the (thinned) GaN channel.

The most effective method, inspired by similar approaches in AlGaAs/GaAs HEMT technology, is the use of an AlGaN back-barrier just below the GaN channel layer. Even the use of AlGaN layers with Al content as low as 5% creates a very high-energy barrier for 2DEG electrons, based partly on the bandgap discontinuity but mostly on the polarization charge at the AlGaN/GaN back interface [13]. This makes the AlGaN back-barrier the most suitable configuration for very high frequency operation (e.g., W-band) where very short sub-100 nm gate lengths are used [14]. There is also a major drawback: the thermal conductivity of ternary AlGaN alloys is significantly lower than that of either GaN or AlN [15], so for a given power dissipation, the peak channel temperature will be significantly higher than in the case of using GaN-based confinement layers.

To limit the punch-through effect in thick GaN channel layers, one method is to use Fe-doping to compensate for the intrinsic n-type background of GaN material. Fe is a deep acceptor in GaN that makes the layer highly resistive. Fe-doped GaN buffers are the de facto standard for GaN on SiC epiwafers used for RF applications. However, iron is not allowed in Si CMOS processing foundries where Fe contamination levels should be below  $5 \times 10^{10}/\text{cm}^2$ , which severely limits its usefulness for GaN-on-Si wafers. Fe also has a long diffusion tail in GaN, making it impossible to make abrupt interfaces between the Fe-doped buffer and the UID GaN channel layer. Finally, there are some reports that link Fe-doping with a trap with activation energy of approximately 0.6 eV [16].

Triggered by the promising results and understanding obtained for power switching, the use of carbon-doped buffers is also being introduced for RF applications. On a device level, the impact of the buffer is evaluated mainly in terms of off-state leakage and subthreshold behavior, the absence of current collapse and the capability to dissipate large power densities. Carbon-doped GaN confinement layers have been compared directly to AlGaN back-barrier designs with favorable outcome [17].

### 15.1.6 HEMT Heterostructures

Even though the above explains the importance of the nucleation and buffer layers, it is obvious that in GaN epiwafers for electronics an important role is reserved for the channel and barrier layers of the HEMT heterostructure. The underlying physics behind the formation of the 2DEG in such structures are reviewed in Sect. 15.2 of this chapter and have also been described in an excellent way elsewhere [3].

The work-horse heterostructure both for power switching and RF applications is still the combination of a thin AlGaN barrier layer on top of a GaN channel layer. The thickness of the barrier layer typically ranges from 10 to 30 nm, with Aluminum content between 15% and 30%. This yields a two-dimensional electron gas with an electron density of between  $6 \times 10^{12}/\text{cm}^2$  and  $1.5 \times 10^{13}/\text{cm}^2$  and associated electron mobility above  $1800 \text{ cm}^2/\text{Vs}$ . The fine-tuning of the structural parameters depends on a wide range of criteria and applications such as maximized electron mobility, improved reliability [18], or reduced electron density to allow e-mode operation through the local depletion of the channel by a p-type (Al)GaN layer under the gate [19].

The AlGaN/GaN heterostructure benefits from a piezoelectric polarization component that adds up to the spontaneous polarization field of the AlGaN layer. As a result, adding more strain to the AlGaN layer by increasing the Aluminum content is beneficial for the number of carriers that are contained in the 2DEG. However during epitaxy,

a growing strained layer only remains pseudomorphic to the underlying lattice until a so-called critical thickness is reached [20, 21] after which the strained layer starts to relax, e.g., by the creation of misfit dislocations [22]. It was shown that for AlGaIn/GaN heterostructures, strain relaxation can also occur by the formation of V-grooves in the AlGaIn layer, caused by the preferential out-diffusion of Gallium from the ternary material [23]. By adding a thin layer of SiN during the epitaxy, this mechanism can be suppressed and the relaxation temporarily postponed [24] until another relaxation mechanism sets in. Thus, not only does in-situ SiN provide a rather effective surface passivation [25], it also allows for the epitaxial growth of aluminum-rich AlGaIn barriers.

The most extreme case of this barrier configuration consists of a pure AlN barrier layer grown on top of the GaN channel layer, as AlN has the widest bandgap and the highest polarization coefficients of the InAlGaIn alloys, making it theoretically the best choice for the HEMT heterostructure. As an example, an AlN barrier layer with a thickness of only 4 nm capped with 10 nm of in situ SiN yields a 2DEG density of  $2.15 \times 10^{13}/\text{cm}^2$  with an associated electron mobility of about  $1000 \text{ cm}^2/\text{Vs}$ . These data points make this structure very interesting for RF purposes because it allows bringing the gate electrode very close to a densely populated 2DEG, which results in a much improved transconductance of the transistor [26].

One drawback of using AlGaIn barrier layers is that the use of strained barrier layers may have a detrimental effect on device reliability [27]. Fortunately, it is also possible to create strain-free HEMT heterostructures, by combining the GaN channel with a lattice-matched InAlN barrier layer [28]. For an indium composition of about 17%, InAlN has the same lattice constant as GaN but a significantly higher bandgap energy of 4.4 eV. Because both InN and AlN have higher polarization fields than GaN, a 2DEG is still induced at the interface between InAlN barrier and GaN channel due to spontaneous polarization only. For example, for a lattice-matched InAlN barrier layer with a thickness of 6 nm with thin cap of SiN, the authors have obtained a 2DEG density of  $1.65 \times 10^{13}/\text{cm}^2$ , which is about 50% higher than for a standard 20 nm  $\text{Al}_{25}\text{Ga}_{75}\text{N}$  barrier layer. One remarkable property is that the electron mobility in this InAlN/GaN heterostructure is as high with a value of  $1800 \text{ cm}^2/\text{Vs}$ , much higher than what can be obtained with the AlN barriers with values around  $1000 \text{ cm}^2/\text{Vs}$ . As a result, InAlN have the lowest sheet resistance of any HEMT configuration, in this case around  $220 \text{ }\Omega/\text{sq}$ . compared to typical values of  $350 \text{ }\Omega/\text{sq}$ . or above for AlGaIn-based heterostructures. Values as low as  $170 \text{ }\Omega/\text{sq}$ . have been reported for thicker InAlN barriers [29].

Recently, a new nitride alloy ScAlN was proposed as an alternative barrier material [30]. Even though results are

still scarce, an 2DEG electron density of  $3 \times 10^{13}/\text{cm}^2$  was reported for layer structures grown by MBE [31].

## 15.2 Lateral Devices Architectures

The first lateral gallium nitride device was reported for microwave applications in the late 1990s [32]. Subsequently, RF architectures expertise has been basically adapted for power and switching applications because of their high off-state breakdown strength combined with an excellent channel conductivity. These GaN-based switches would offer greater efficiency, power handling, and other performance attributes compared to the well-established, widely available silicon MOSFET power devices. The superior electron mobility means that a GaN transistor will have a smaller size for a given on-resistance and breakdown voltage than a silicon (Si) semiconductor. Thus, GaN also offers extremely fast switching speed and excellent reverse-recovery performance, critical for low-loss, high-efficiency performance. Furthermore, despite their large lattice mismatch (about 14%), high-quality GaN growth can be achieved on cost-effective Si substrate using advanced techniques to accommodate the strain issues. Although GaN on SiC substrates are generally advantageous for high power devices because of the high thermal conductivity and lower lattice mismatch, the growth on Si substrates is more promising for power applications because of the scalability of wafer diameters to 200 mm and more and due to the comparably low price level. The ability of power semiconductor devices to enhance the power electronics performance/cost figure of merit can be simplified by its own price/performance figure of merit, namely, dependent on the switching power loss, ohmic power loss, and the cost, where the switching power loss reflects the thermal limitation, most often achieved through increasing switching frequency and subsequent reduction in output filter components. Therefore, in addition to efficiency improvements, the use of GaN semiconductors instead of state of the art silicon-based devices for power electronic systems allows the reduction of size/weight of the conversion subsystems, due to significant reduction in cooling system requirements.

The structure of a common AlGaIn/GaN high electron mobility transistor (HEMT) appears in Fig. 15.2 along with the band diagram. At the heterojunction between the AlGaIn barrier and the GaN channel, the two materials discontinuity in polarization leads to carrier diffusion. The AlGaIn free electrons are attracted to the GaN channel and create an accumulation of charges at the interface of both layers. At the thermodynamic equilibrium, a discontinuity of the conduction band at the AlGaIn/GaN interface is observed. This discontinuity forms triangular potential well. Confine in a very small area, those electrons create a two-dimensional electron gas (2DEG) enabling a high charge density conduction between

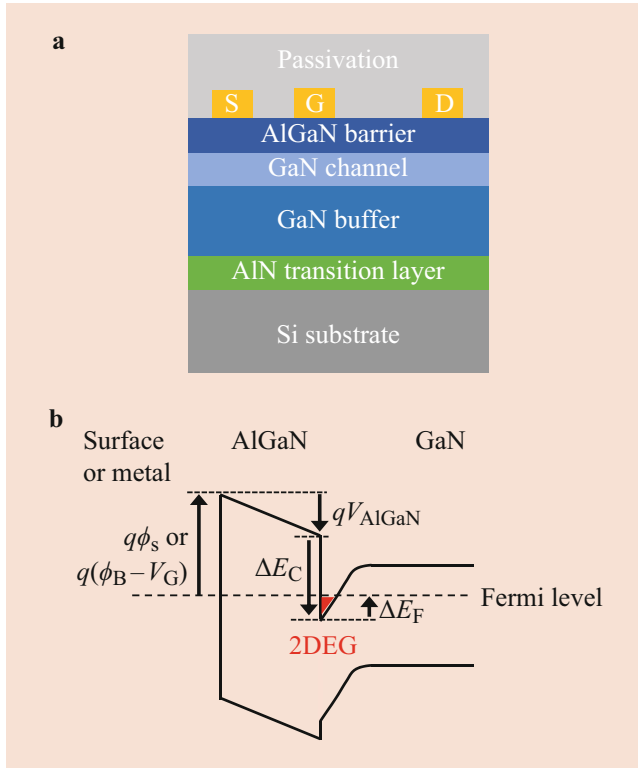


**Fig. 15.2** (a) Cross section of an AlGaIn/GaN HEMT associated with (b) his band diagram

the drain and the source. Unlike GaAs HEMTs, GaN HEMTs do not require any electron doping to create the 2DEG at the interface between the barrier and the channel. Indeed, the creation of the 2DEG is the result of the piezoelectric and spontaneous polarizations inherent of the AlGaIn/GaN heterostructure. The electron density in the 2DEG is directly dependent on the nature and the thickness of the material used as barrier layer [33, 34]. The high electron confinement at the interface allows reducing the electron scattering, which leads to an electron mobility typically ranging from 900 and 2200 cm<sup>2</sup>/Vs [35, 36].

In more detail, all the contributions leading to the formation of the channel can be computed as follows, referring to Fig. 15.3a for the device structure and dimensions, to Fig. 15.3b for the charge distribution and to Fig. 15.2b for the band diagram, and assuming Ga-face polarity. For thick AlGaIn layers, the surface potential  $q\phi_s$  is pinned by the surface donor levels located at the upper barrier surface and is almost equivalent to the donor energy depth  $E_D$ . Due to the lattice mismatch between AlGaIn, and GaN, the thinner AlGaIn barrier is submitted to tensile strain; therefore the total polarization charge  $-\sigma_P(\text{AlGaIn})$  at the AlGaIn surface is the sum of the spontaneous polarization  $-\sigma_{SP}(\text{AlGaIn})$  and piezoelectric polarization  $-\sigma_{PE}(\text{AlGaIn})$  contribution

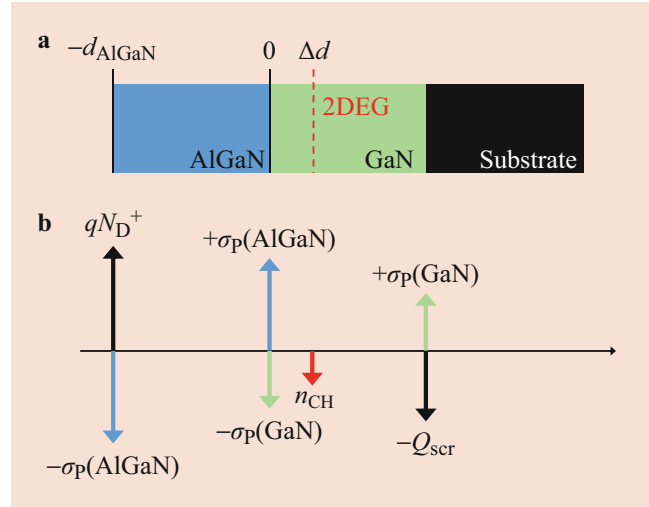


**Fig. 15.3** (a) Schematic structure of a GaN HEMT for the calculation of the channel charge density and (b) charge distribution in the device. The AlN transition layer is not considered for easier understanding

$$-\sigma_P(\text{AlGaIn}) = -\sigma_{SP}(\text{AlGaIn}) - \sigma_{PE}(\text{AlGaIn}) \quad (15.1)$$

An additional positive charge contribution  $N_D^+$  is present at the surface, caused by the unscreened fixed positive charge left by the ionized donors. If the AlGaIn layer is thick enough, the Fermi level will reach the donor state level, and the electrons will be stimulated into the conductive band and swiped toward the other side by the force of the polarization-induced electric field. Once contacting with a GaN layer, electrons will flow into the GaN side because of the drop of the Fermi level. The electrons will accumulate at the interface and contribute to the formation of the 2DEG. At the interface between the barrier and the channel region, the net polarization charge  $-\sigma_P(\text{net})$  is the sum of the contribution by the AlGaIn and the GaN layers,  $\sigma_P(\text{AlGaIn})$  and  $-\sigma_P(\text{GaN})$ , respectively,

$$\sigma_P(\text{net}) = \sigma_P(\text{AlGaIn}) - \sigma_P(\text{GaN}) \quad (15.2)$$

Given the stronger spontaneous polarization field in AlGaIn with respect to GaN, the net charge is a positive number. This positive net charge leads to the presence of an electron distribution in the channel region close to the hetero-interface. We assume that this charge density  $qn_{CH}$  is distributed as a two-dimensional charge layer at a distance  $\Delta d$  from the AlGaIn/GaN interface, where  $\Delta d$  is the center of the charge distribution. Starting from the AlGaIn surface, we can follow the profile of the lower edge of the conduction band from the Fermi level in the metal to the Fermi level in the GaN buffer and write

$$\phi_s - V_{\text{AlGaN}} - \frac{\Delta E_C}{q} + \frac{\Delta E_F}{q} = 0 \quad (15.3)$$

where  $\Delta E_C$  is the conduction band energy discontinuity at the hetero-interface,  $\Delta E_F$  the distance between the Fermi level and the lower edge of the conduction band at the interface, and  $V_{\text{AlGaN}}$  the potential across the AlGaN region

$$V_{\text{AlGaN}} = \frac{|\sigma_P(\text{net}) - qn_{\text{CH}}| \cdot d_{\text{AlGaN}}}{\varepsilon} \quad (15.4)$$

$\Delta E_F$  can be expressed as

$$\Delta E_F = \frac{qn_{\text{CH}}}{\varepsilon} \cdot \Delta d \quad (15.5)$$

The electron channel density  $n_{\text{CH}}$  is then

$$n_{\text{CH}} = \frac{\sigma_P(\text{net}) \cdot d_{\text{AlGaN}} - \varepsilon(\phi_s - \Delta E_C/q)}{qD} \quad (15.6)$$

where

$$D = d_{\text{AlGaN}} + \Delta d \quad (15.7)$$

is the distance between the AlGaN surface and the channel location. In a complete HEMT structure, a gate metal is deposited on top of the AlGaN barrier, which can be used to vary the AlGaN surface potential. When a bias  $V_G$  is applied to the gate contact, the surface potential  $\phi_s$  equals  $\phi_B - V_G$ , where  $\phi_B$  is the barrier height of the metal-semiconductor junction, and therefore we obtain

$$n_{\text{CH}}(V_G) = \frac{\sigma_P(\text{net}) \cdot d_{\text{AlGaN}} - \varepsilon(\phi_B - V_G - \Delta E_C/q)}{qD} \quad (15.8)$$

Concluding, at the interface between the gallium nitride buffer and the substrate, we have the positive polarization charge of the gallium nitride  $+\sigma_P(\text{GaN})$  and an additional screening charge  $-Q_{\text{scr}}$  to ensure charge neutrality in the full structure.

The high electron mobility combined to the high density of charges in the 2DEG enable very low on-state resistances ( $R_{\text{ON}}$ ). Up to 650 V voltage range, GaN devices can thus be foreseen as the best choice as compared its counterparts considering a proven high level of reliability. At higher-voltage operation, this technology is basically limited by the Si substrate. This limitation will be detailed later in this chapter. However, increasing the blocking voltage of GaN lateral devices would pave the way for more efficient devices beyond 1 kV applications [37, 38].

## 15.2.1 Applications

Silicon-based devices such as MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistor) or IGBTs (Insulated-Gate Bipolar Transistor) have been extremely successful and represent the present standard for power switches in power applications – AC/DC supplies, DC/DC supplies, and motor controls – ranging from just tens of watts up to hundreds and even thousands of watts. They have seen continual improvements in key parameters such as on-resistance  $R_{\text{DS(ON)}}$ , voltage ratings, switching speed, packaging, and other attributes. However, the rate of improvements in these MOSFETs has leveled off, as their performance is now close to the theoretical limit as determined by the underlying fundamental physics of these materials and processes. In this frame, GaN lateral devices have a growing impact on the current power market. Indeed, due to its impressive intrinsic characteristics (shown Fig. 15.4), GaN material has a truly predisposition for high-voltage and high-speed switching applications as confirmed by many market reports for low and mid-voltage range (<600 V) in a short term.

GaN could impact a wide range of applications using various operating voltage. For instance, GaN presents a unique palette of viable solutions for both high power and medium power applications that can power the next generation cars efficiently and economically. Hybrid vehicles represent today a growing market where companies are significantly investing. The emergence of wireless power is another key application enabled by GaN. Eventually, the entire home can be equipped with transmitters and repeaters that will power the lights, TV, and other household appliances wirelessly. GaN transistors will support this rapidly emerging application. Another good example is the use of GaN components in an extremely small x-ray machine that fits in the size of a pill. In this case, GaN's superior performance to obtain 10–100 times higher resolution so diseases can be detected earlier, more accurately and less expensively. Also, in addition to its ability to survive in a harsh environment, the small size, and high efficiency of GaN device make them very attractive for use in space application. GaN is inherently radiation tolerant. Unlike silicon, where special fabrication techniques and special packaging is needed to shield semiconductors from the effects of radiation, GaN's natural properties make it relatively immune to these harmful rays.

## 15.2.2 State-of-the-Art

The specific on-state resistance of any semiconductor devices used for power electronic applications is one of the key performance parameters. An ideal power switching device should have a high breakdown voltage to cope for the off-state condition with a sufficient margin while its on-state

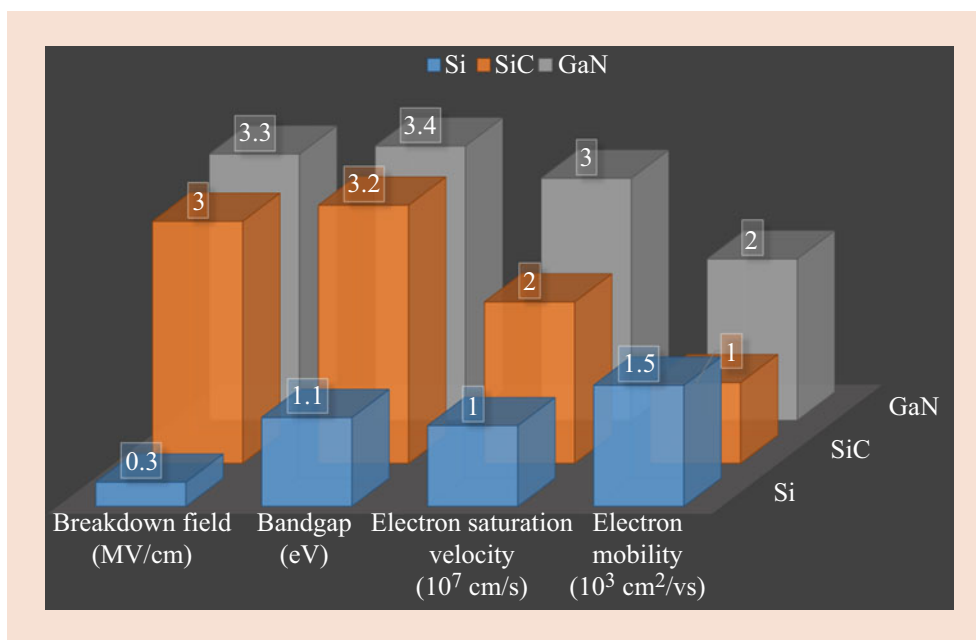


**Fig. 15.4** Comparison of intrinsic characteristics of GaN, Si, and SiC material

resistance should be as small as possible. This request translates into the trade-off situation depicted in Fig. 15.4. High breakdown devices require extended drift regions, e.g., the distance between gate and drain needs to be sufficiently large. This means that the increase of the breakdown voltage induces resistive elements that are added to the device thus increasing the on-state resistance. As shown in Fig. 15.5, the optimum on-state resistance for each types of devices follows specific theoretical limits, which have been calculated for unipolar devices. In fact, as power switching devices are operated in the linear (mobility controlled) region at on-state, the on-state resistance increases with breakdown voltage practically in a quadratic dependency. Accordingly, GaN devices have an advantage over Si devices by theoretically at least three orders of magnitude. They even outperform SiC devices.

It can be noticed that many large companies are devoted to the development of GaN power devices. A wide range of commercial GaN power devices are already commercialized. This reflects the potential short-term market penetration of these emerging devices. Nevertheless, several hurdles still need to be overcome such as the cost that needs to be reduced in order to be competitive with Si-based devices while delivering superior performance; the reliability of normally-off GaN devices and in particular the control of the dynamic on-resistance up to high temperature; the integration and associated packaging that needs to be implemented without sacrificing the performances; and the sourcing that needs to be increased to allow high acceptance of this technology from the industry. Furthermore, higher voltage range ( $>1.2$  kV),

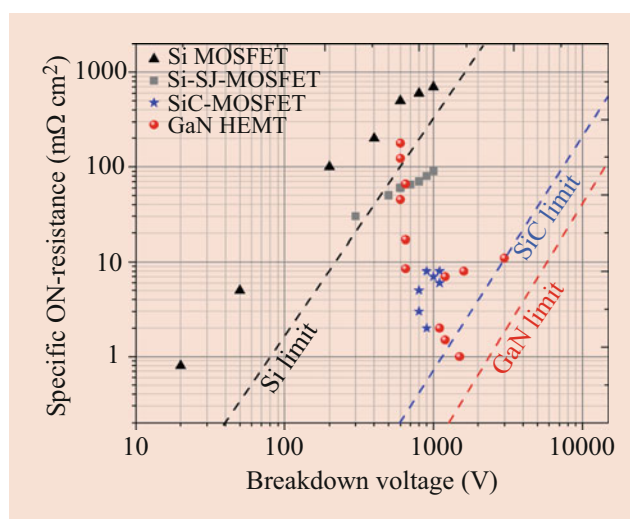


**Fig. 15.5** Specific on-resistance as a function of the breakdown voltage of various materials

limited currently to below 1 kV would extend the impact of GaN lateral devices for power applications.

### 15.2.3 Limitations of GaN Lateral Devices

As discussed previously, GaN lateral devices are already showing attractive performances as compared to silicon technology [39–41]. However, the operating voltage of GaN devices is limited to below 1 kV, which is significantly lower

than the full potential of this technology. One of the main technological bottlenecks include:

- The parasitic conduction at the buffer/Si substrate interface under high voltage
- The dynamic  $R_{ON}$  issues
- The normally-on behavior

### Parasitic Conduction Under High Voltage

Many different physical effects are limiting the high voltage performance of GaN devices. They all have to be taken into account when developing high voltage GaN devices. The breakdown voltage is often defined as the voltage level at which the drain current of the pinched-off transistors is exceeding a normalized value of  $1 \mu\text{A}$  per mm device width. The main sources of leakage for an AlGaIn/GaN HEMT device are represented in Fig. 15.6. Device breakdown mainly depends on the specific epitaxial design of the buffer layer, its material quality, the lateral geometrical design of the devices, and their passivation technique. The latter issues are mainly dependent on processing technology, whereas the former parameters are due to the GaN/AlGaIn epitaxial design, the material properties and the interfacing between GaN/AlGaIn material technologies and processing. Some mechanisms, for example, surface arcing between adjacent conductive structures with a large potential difference are known from standard power electronic device technologies.

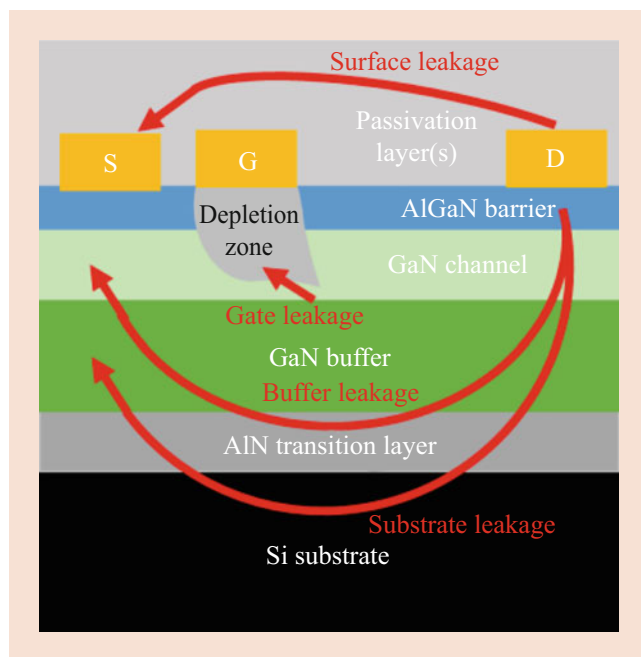


**Fig. 15.6** Representation of the main sources of leakage for a HEMT AlGaIn/GaN device on Si substrate

These mechanisms can be harnessed by applying adapted passivation and encapsulation schemes.

Buffer leakage current is due to the injection of charge carriers into the buffer under high bias. This phenomenon is commonly called punch-through effects [42]. In this case, if the channel is closed by a sufficiently negative gate bias, electrons are bypassing the gate control region via the buffer. Several solutions have been developed to overcome this issue by the use for instance of carbon or Fe-doped buffer [44–45] or an AlGaIn back barrier [46].

In off-state condition, the gate polarization creates a large depletion region, and the electrons can flow from the gate to the drain, most probably due to electron injection across the gate barrier. As these effects are triggered by high electric field strength, particularly at the drain side edge of the gate or close to the drain electrode, field plates can suppress this effect and thus shift the breakdown voltage to higher values.

A strong limitation of GaN lateral devices grown on silicon substrate is the parasitic conduction at the buffer/Si substrate interface under high voltage. Figure 15.7 shows the breakdown voltage (BV) defined for a leakage current of  $1 \mu\text{A}/\text{mm}$ , for various epitaxial thicknesses as a function of the gate-drain voltage distance ( $L_{GD}$ ). If the leakage currents are suppressed by suitable technological means, GaN HEMTs BV scales with increasing  $L_{GD}$ . Thus,  $L_{GD}$  determines the maximum allowable operation voltage. For small  $L_{GD}$  (typically  $<15 \mu\text{m}$ ), the breakdown voltage monotonically increases, generally indicating a breakdown mechanism that is triggered by properties directly influenced by  $L_{GD}$  scaling. In this case, breakdown occurs between the drain side edge of the gate and the channel region with a simultaneous increase of gate and drain current. On the other hand, for higher  $L_{GD}$ , BV saturates with respect to the epitaxial total thickness. Detailed investigations have shown that the dominating current flow at breakdown condition is now originating from the source, flowing vertically through the buffer to the conductive substrate and back to the drain terminal.

Therefore, increasing the epitaxial thickness allows improving BV. However, buffer thickness typically above  $6\text{--}7 \mu\text{m}$  with low bow is extremely difficult to achieve on large wafer diameters and often leads to higher defect density and eventually cracks. Another way to reduce the parasitic conduction at the buffer/Si substrate interface [48–50] is to locally remove the substrate and subsequently replace by a wider bandgap material. This approach will be described later in this chapter.

### Dynamic $R_{ON}$ Issues

GaN-based power transistors can only gain market acceptance if they demonstrate switching properties superior to

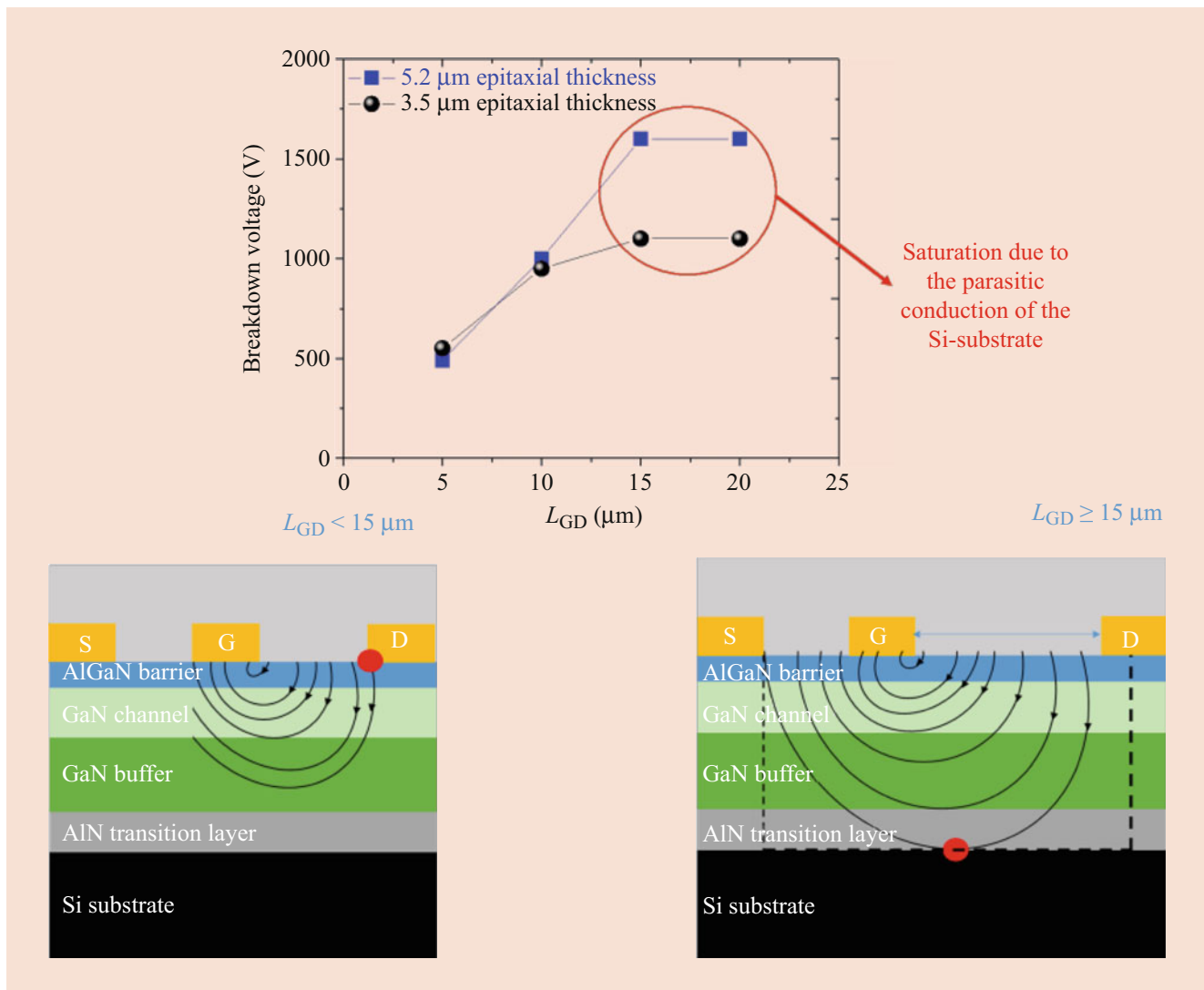


**Fig. 15.7** Breakdown voltage comparison of AlGaIn/GaN HEMTs with various epitaxial thicknesses as a function of the gate-drain distance [47]

competing technologies. Due to trapping effects the static on-state resistance  $R_{on\_stat}$  may increase upon dynamic switching of the device leading to a degraded dynamic on-state resistance ( $R_{on\_dyn}$ ). This effect is also known from GaN microwave transistors. As power switching devices are never driven into saturation for most of the switching sequence (only dynamically during a switching event), the dynamic change of the on-state resistance is taken as a criterion to quantify the dynamic trapping effects. As shown in Fig. 15.8, this parasitic effect can cause a strong degradation of the dynamic on-state resistance, which often scales with device switching voltage and thus significantly challenges high voltage GaN switching applications.

The trapping effects in the device structure responsible of the degradation of the dynamic  $R_{ON}$  are commonly represented by negative electric charges located in different

areas: near the surface (usually process induced) and into the buffer layers (poor interface quality, doping compensation, etc.) [52–53]. Figure 15.9 depicts the mechanism of the traps and the degradation of the dynamic  $R_{ON}$  during switching. Trapping can take place at various places, in the epitaxial layers, at passivation semiconductor interfaces or even at interfaces between different passivation layers. In consequence, electron transport in the channel region immediately after switching from one condition to another is impeded by negatively charged traps until they are emptied. This leads to increased switching losses, reduced system efficiency, and explains time dependence of  $R_{on\_dyn}$ . An optimized buffer design avoiding deep trapping with a proper surface passivation and the use of field plates to spread the peak electric field are some essential countermeasures towards optimized power switching.

### 15.2.4 Pushing the Limits of Lateral GaN Devices: Enhancement of the Blocking Voltage

One of the main challenges with GaN-on-Si lateral devices is the enhancement of the blocking voltage. Several parameters still limit today the device operation for higher voltage

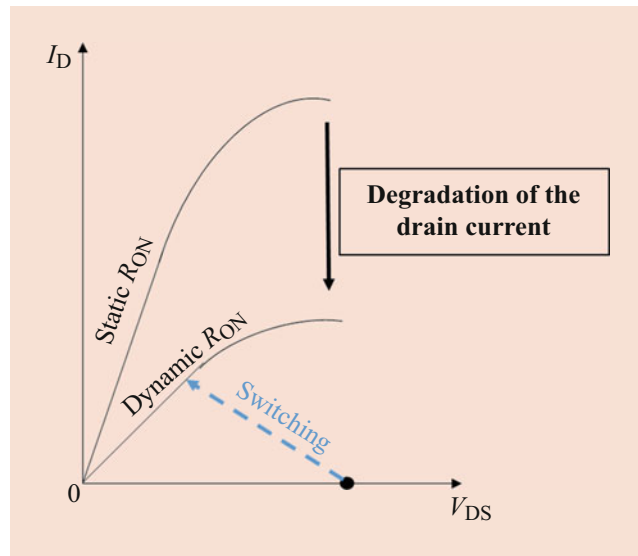


**Fig. 15.8** Degradation of the dynamic  $R_{ON}$  during switching of a GaN HEMT

(silicon substrate, epitaxial structure thickness). One way to increase the breakdown is the use of thicker buffer layers. Advanced architectures based on AlN/GaN superlattices or thick (up to 7  $\mu\text{m}$ ) quasi-carbon-free buffer combined with strain-management interlayers have been developed successfully. A key point is that regardless of the chosen approach, buffer trapping should be avoided.

An example of electrical characteristics from a thick and excellent buffer crystal quality showing low leakage current and state-of-the-art vertical breakdown voltage above 1400 V ( $\sim 2$  MV/cm) appears in Fig. 15.10 [54]. Furthermore, substrate ramp measurements reveal very low trapping effects up to 1.2 kV (Fig. 15.10b). It has been indeed shown that ramping the substrate to a high (negative) potential allows to reproduce the off-state operation under the drain contact in a transistor. In this case, any buffer charge trapping or storage will be visible in the substrate ramp characteristics.

Another promising solution to increase the blocking voltage of GaN-on-Si lateral devices is the local substrate removal (LSR). This method consists in a selective silicon substrate removal around the device and subsequent replacement by an ultra-wide bandgap followed by a backside metallization [49] as described in Fig. 15.11.

Aluminum nitride (AlN) deposited by PVD is a promising dielectric in this frame since it has a low mismatch with the nucleation layers, a significant breakdown field above 4 MV/cm and offers a cost effective manufacturing technology scalable to large wafer diameter [55]. The LSR

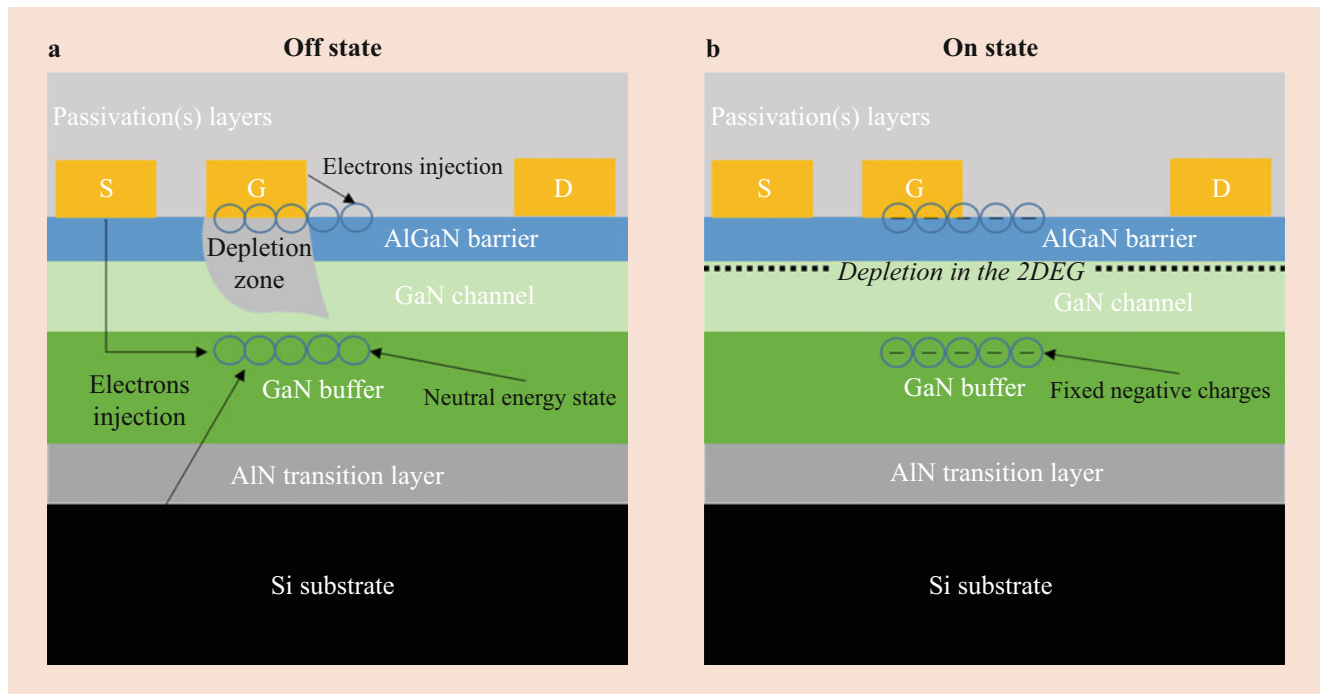


**Fig. 15.9** Illustration of the influence of the trapping effect on the  $R_{ON}$  of a GaN HEMT during switching (a) off state (b) on state

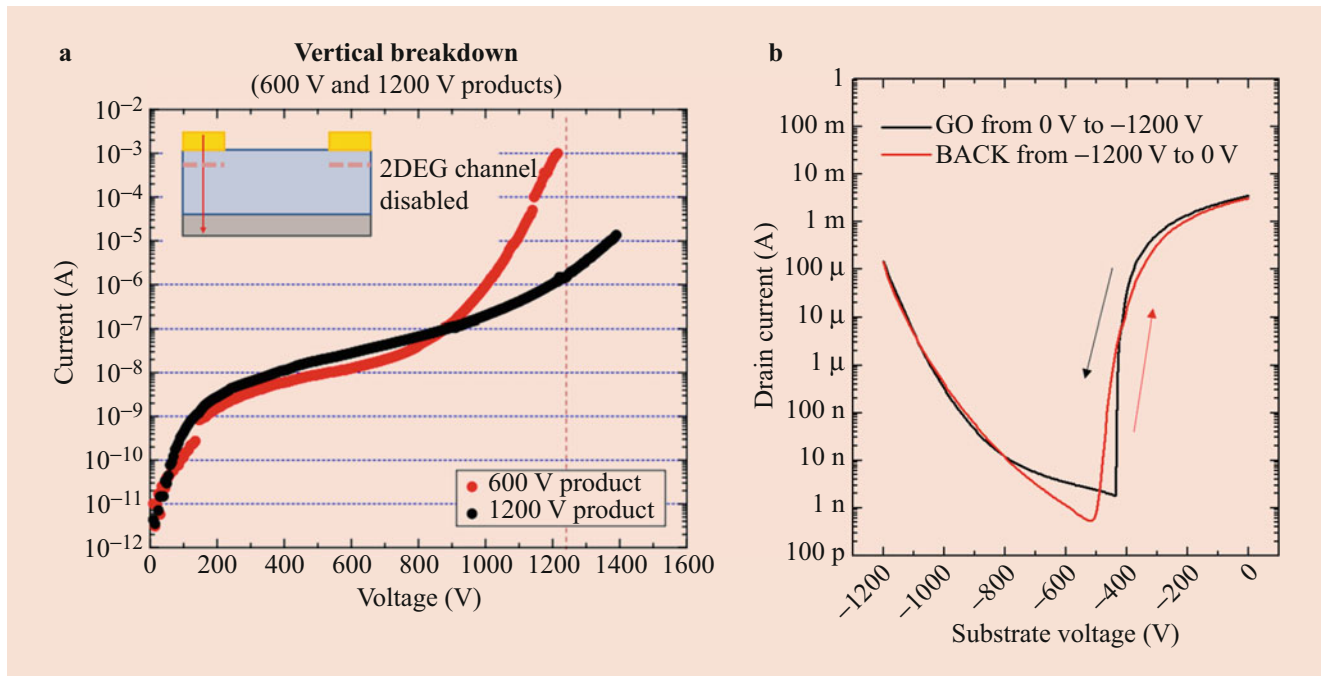


**Fig. 15.10** (a) Vertical breakdown voltage and (b) substrate ramp measurement up to 1.2 kV of GaN-based heterostructure

technique combined with 15  $\mu\text{m}$  thick AlN layer resulted in state-of-the-art GaN-based HEMTs with remarkably low off-state leakage current ( $<1 \mu\text{A}/\text{mm}$ ) beyond 3 kV while maintaining a low specific on-resistance about  $10 \text{ m}\Omega\cdot\text{cm}^2$  (Fig. 15.12). The comparison of these devices without LSR confirms that the drain leakage current flows essentially at the AlN nucleation layer/Si substrate interface. Furthermore, significant recovery of the maximum current density after the backside metallization enabled to reduce the self-heating. It can also be pointed out that this approach do not induce additional charge trapping. The integrity of a trap-free buffer is thus not affected by the substrate removal while extending significantly the bias operation capability.

### 15.2.5 Normally-Off GaN Lateral Devices

Normally-off configuration is an essential prerequisite for power applications in order to reduce the power consumption and keep a simple gate drive configuration. Many approaches have been demonstrated toward normally-off GaN lateral transistors. The general approach is to shift the conduction band of the channel region controlled by the gate above the Fermi level at zero gate bias and thus to obtain a positive threshold voltage. For power applications threshold voltage ( $V_{\text{TH}}$ ) ranges above +1 V are desirable to ensure safe operation conditions, while the on-state resistance should be kept as low as possible.

### MISHEMTs

The main advantage of the MISHEMT (*Metal Insulator Semiconductor HEMT*) structure is that a high threshold voltage levels can be obtained. A gate recessing is combined with gate dielectric isolator techniques to avoid gate leakage increase (Fig. 15.13). However, interface charges subsequent to the gate recess etching and dielectric deposition still plague this type of devices. The choice of the insulator has a strong impact on the interface traps. For instance, some studies showed that the use  $\text{Al}_2\text{O}_3$  induces negative charges, while  $\text{HfO}_2$  gives rise to positive charges [56].

### $\text{F}^-$ Ion Implant under the Gate

Another possibility to achieve normally-off operation on a GaN HEMT is the use of ion implantation by plasma Fig. 15.14. This method was first demonstrated in 2006 [57] showing positive  $V_{\text{TH}}$ . The fluorine  $\text{F}^-$  ion implantation into the AlGaIn barrier layer localized under the gate makes use of the natural strong electronegativity of the  $\text{F}^-$  ion to deplete the DEG as charge neutrality is ensured. A trade-off between the mobility/ $R_{\text{ON}}$  degradation and higher  $V_{\text{TH}}$  positive shift exists depending on the plasma condition such as time and power used. Furthermore, the device reliability under high voltage still needs to be demonstrated for this approach. For instance, several groups have shown a strong dependence of the amount of fluorine ion implantation on the increase of the current collapse and the annealing temperature [58] leading to a threshold voltage instability.

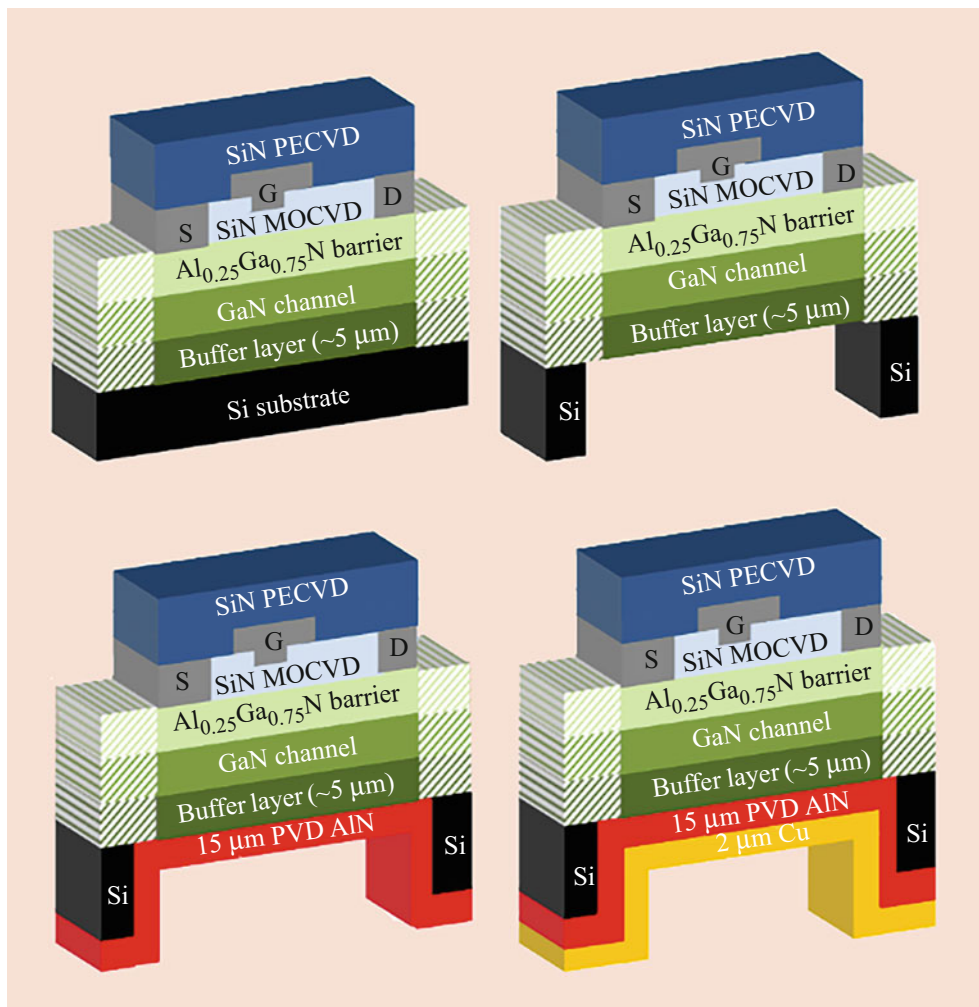


**Fig. 15.11** Cross section describing the fabrication of the local substrate removal approach

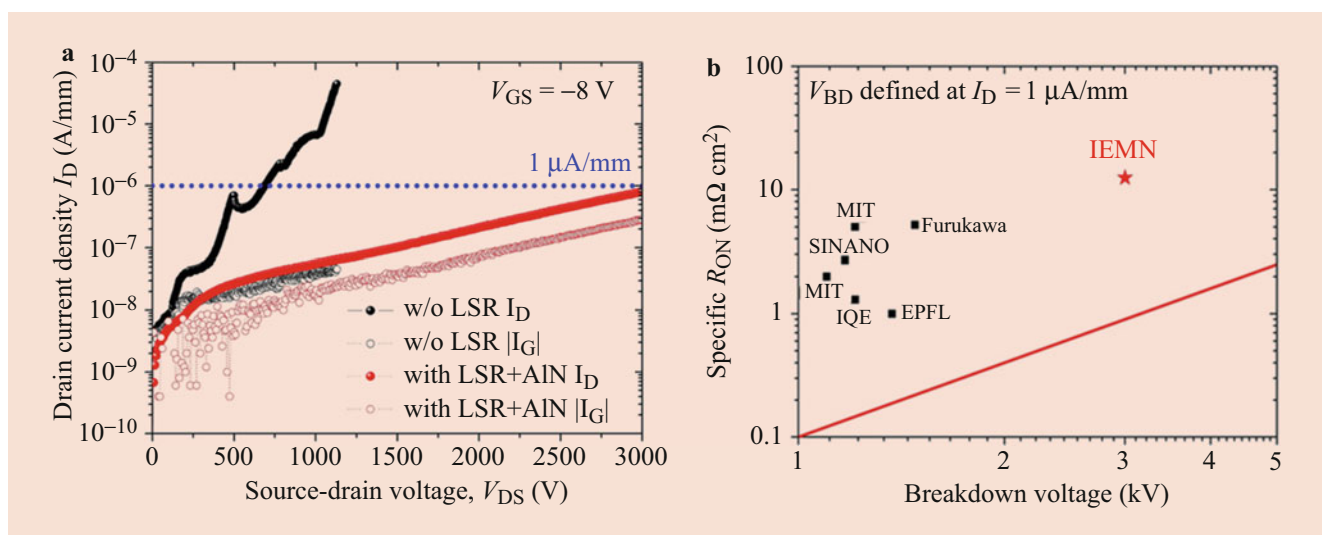


**Fig. 15.12** (a) Off-state leakage current characteristics of AlGaN/GaN MISHEMTs with and without LSR/thick AlN deposition. (b) Benchmark of GaN-on-Si HEMTs with blocking voltage defined at an off-state

leakage current of 1  $\mu\text{A}/\text{mm}$ . (Reprinted from E. Dogmus et al. [55] under the terms of the Creative Commons Attribution 4.0 license (CC-BY) <http://creativecommons.org/licenses/by/4.0/>)

### The Cascode Circuit

Normally-off behavior can also be obtained by connecting a standard normally-off Si MOSFET optimized for low-voltage operation and a high-voltage GaN normally-on transistor in cascode configuration (Fig. 15.15). In this hybrid configuration, the Si MOSFET is used to control the GaN HEMT gate with only positive gate voltage through the Si MOSFET resulting in a normally-off overall behavior. On-state and off-state properties should be determined by the GaN device, whereas the normally-off property is due to the Si device. The packaged cascode configuration looks

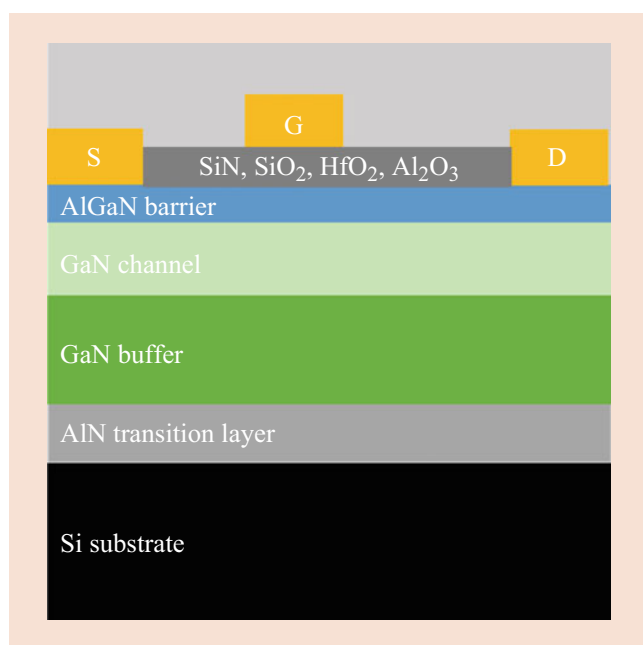


**Fig. 15.13** Cross-section of a MISHEMT

like a high-voltage normally-off transistor. It combines the advantages of a large gate threshold voltage and gate voltage swing (feature of the Si normally-off transistor), a high breakdown voltage and a comparably low on-state resistance related to the normally-on GaN HEMT. Combining these two devices brings several drawbacks: the input capacitance is determined by the Si-MOSFET and therefore comparably high slowing down the switching speed [59]. Furthermore, the Si MOSFET limits strongly the overall temperature operation offered by the GaN technology. Nevertheless, several manufacturers are pursuing the commercialization of the cascode design.

### P-GaN

The first demonstration of p-AlGaIn or p-GaN under the gate in order to achieve normally-off operation has been realized by Panasonic in 2007 [60] despite the challenge of p-doping (Magnesium) of GaN material. Figure 15.16 describes the band diagrams with and without a p-GaN cap layer. At zero gate bias, the p-GaN layer is depleted leaving back a fixed negative charge which in turn depletes the channel. When the positive gate bias increases further, holes are injected into the pn heterojunction, which results in a higher drain current of the device.

In practice, a careful epilayer design needs to be used in order to achieve a positive threshold voltage. One of the key parameter is the concentration of Mg in the p-GaN layer. Some studies have shown that a concentration in the range of  $2 \times 10^{19} \text{ cm}^{-3}$  is necessary [62] with a trade-off with defect density increase in the case of higher Mg concentration. A second important parameter to be considered is the Al content into the  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  barrier layer. A lower electron density into the 2DEG resulting from a reduced Al content favors a stronger depletion and thus higher pinch-off voltage.

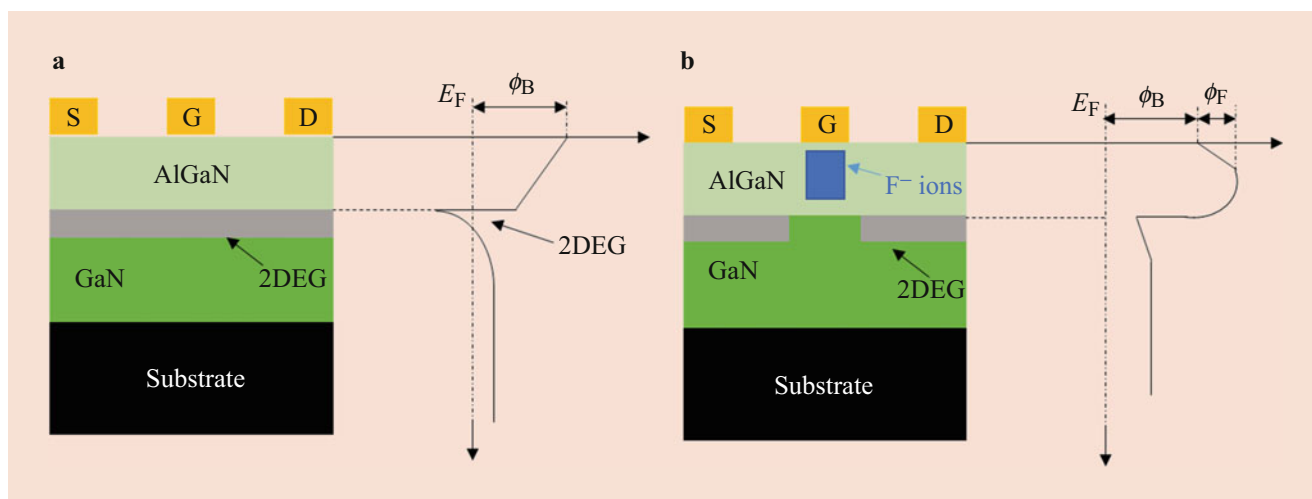


**Fig. 15.14** Cross section of a conventional AlGaIn/GaN HEMT and an AlGaIn/GaN HEMT with  $\text{F}^-$  ion implant under the gate associated to their conduction band profiles

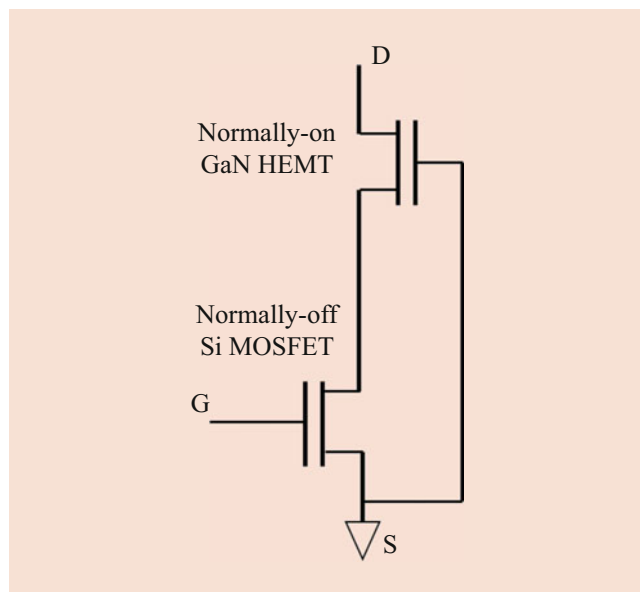


**Fig. 15.15** Cascode type hybrid integration of GaN normally-on and Si normally-off device

### Processing of GaN Lateral Devices

A conventional Schottky gate D-mode and p-GaN E-mode GaN HEMT device structures are schematically shown in Fig. 15.17. The process modules for the GaN HEMT device fabrication include the ohmic contact formation for source and drain, device isolation, p-GaN gate contact or MIS gate, surface passivation, and interconnects. The source and drain metal stacks facilitate the ohmic contacts. In order to avoid cross-contamination with Si processes in production lines, Au-free metallizations have to be used. The gate contact is deposited on top of a high-quality dielectric for the D-mode GaN HEMTs. In the case of E-mode, the p-GaN layer should be removed except under the gate area. The dry etching is widely used for this step. One of the key factors to achieve high performance device and high yield is the etching selectivity of GaN over AlGaIn. The commonly used  $\text{Cl}_2/\text{BCl}_3$  plasma results in a poor selectivity. Fluorine-based chemistry etching technique has been reported to provide better selectivity. The etching of compound semiconductor films containing Al can be optimized in Cl-based plasmas by adding F-containing gases. For instance, the  $\text{BCl}_3/\text{SF}_6$  selective dry etching on AlGaIn/GaN allows decreasing the AlGaIn etching rate resulting from the formation of non-volatile  $\text{AlF}_3$  residues on AlGaIn surface. Actually, the  $\text{AlF}_3$  reduces the etching efficiency of chlorine enabling a selective etching of GaN over AlGaIn. To further enhance the etching selectivity, a thin AlN etch stop layer can be inserted between the p-GaN and AlGaIn layers improving the  $V_{\text{TH}}$  uniformity. Finally, the surface passivation (especially of the sidewalls) plays a crucial role for proper device operation in order to prevent the current collapse and related large dynamic on-resistances.

### Future Prospects

GaN power switching devices will play an important role in future power electronic applications due to their outstanding properties. With the continuous progress of manufacture technology, GaN power devices with high breakdown voltage, high temperature resistance, low conduction losses, and high output power should penetrate large markets soon. In particular, the increasing need of higher efficiency will make GaN devices extremely attractive. The collection of data shows that the newest generations of the emerging GaN power switching definitely outperform their Si competitors. It is now the time to convert prototype devices to highly mature industrial devices. Nevertheless, the better performance/cost ratio than available devices needs to be realized by proving their reliability to a large extend. Furthermore, higher switching frequency and higher operating temperatures translate indeed in smaller passive components and cooling systems, which would benefit any power applications. However, the main challenge will be the lack of passive components, advanced packaging technologies, and circuit designs for handling such small dies with their fast-switching characteristics at the converter level. This may postpone the introduction of GaN devices for some applications in a short term. On the other hand, in several applications (e.g., mobile applications in transportation systems, power supplies for notebooks, and communication units), there is a high pressure to reduce the power converter's size and weight while increasing the efficiency.

## 15.3 Vertical Devices Architectures

Power electronics is a highly discussed topic of our century. As we prepare ourselves to address the next-generation power requirements, we make a note of the changing landscape of power generation and delivery. With the rollout of renewables as sources for electricity, more and more electronics are getting connected to the source side and load side of our grid. The trend will only continue upwards. This suggests higher power device integration to the grid which to a device engineer translates to finding solutions that are power dense. Besides grid, there are several applications, extending from automotive to robotics and touching our daily lives, which require a more efficient power conversion unit. Every power conversion unit requires a solid-state switch to perform their job.

Silicon-based power electronics have served us well. However, it is time for wide bandgap semiconductors to address the issues of high-power electronics, where higher power density is a key driver. Vertical GaN technology is one of the pillars that would prove its worth in the coming years in delivering the appropriate performance over cost benefit that the market is looking for. In this chapter,

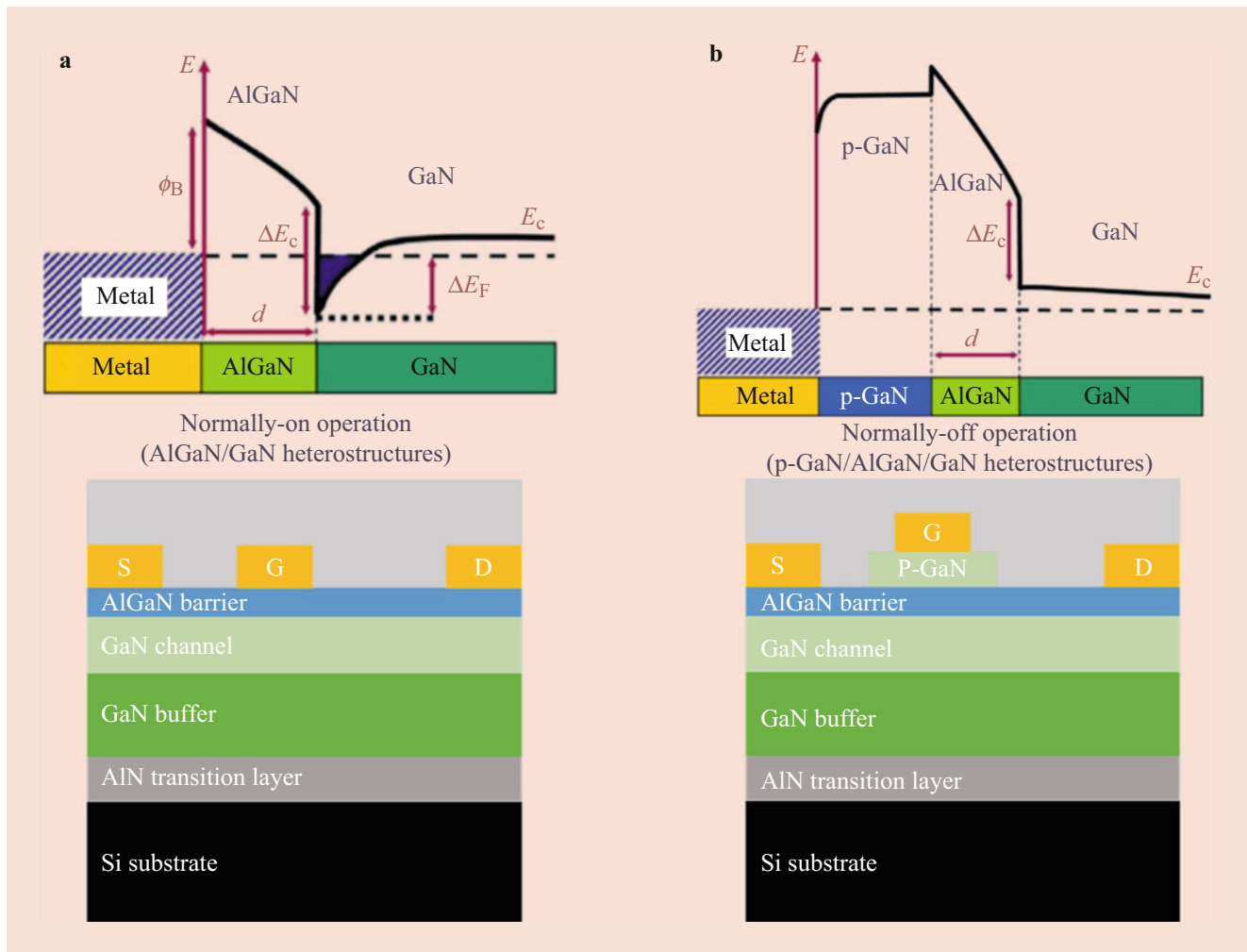


**Fig. 15.16** (a) Band diagram of an AlGaN/GaN normally-on HEMT and (b) a p-GaN/AlGaN/GaN HEMT [61]. (Reprinted from G. Greco et al. [61], 2018, Copyright (2018), with permission from Elsevier)

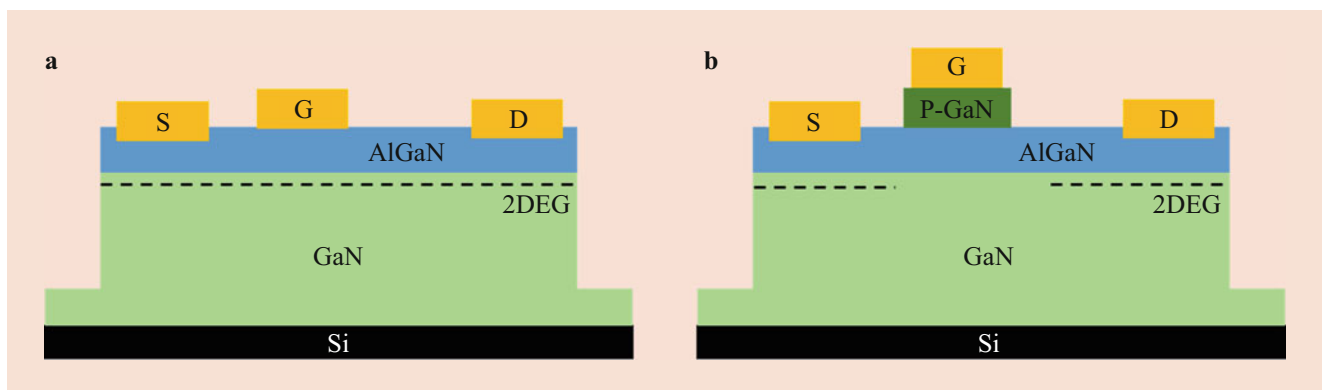


**Fig. 15.17** D-mode GaN device structure (a) and p-GaN E-mode device structure (b)

we go over vertical devices in GaN like Current aperture vertical electron transistor (CAVET), vertical Metal Oxide Field Effect transistor (v-MOSFET), and Static Induction

transistor (SIT) [63]. But before we go over the devices, we will discuss about TCAD models that we found extremely valuable to predict device performance during our research.

### 15.3.1 Device/Circuit Hybrid Modeling

For power semiconductor devices, technology computer-aided design (TCAD) simulation is a vital tool to accurately predict the behavior and optimize the design of devices. For the well-proven practice of Si-based devices, there are reliable simulation platforms that include process, device, and circuit (system) models. However, due to the maturing nature of the GaN technology, there are very few available device simulation tools. Due to the expensive manufacturing of GaN devices, it becomes even more important to develop an accurate and reliable TCAD modeling for GaN devices to predict device behaviors.

A flowchart of the device/circuit hybrid modeling approach is shown in Fig. 15.18 [64]. Before the development of the model, a 700 V AlGaIn/GaN HEMT was fabricated. Based on the extracted data from the fabricated HEMT, we developed a physics-based device model for it, and then integrated it with a circuit model to study the dynamic characteristics and power losses of the HEMT. Using this device-circuit-integrated model, we can start with 2D drift-diffusion modeling of the device and build all the way up to its circuit implementation to evaluate its switching performance. The method of using a hybrid model should give us an inexpensive and accurate way to project and benchmark the

performance that can be extended to any GaN-based power transistors.

### 15.3.2 Physics Models for GaN

#### Drift-Diffusion Model

The TCAD device simulation uses the drift-diffusion model, which solves the Poisson and current continuity equations. The equations are shown as

$$\nabla^2 \varphi = \frac{q(n - p + N_A - N_D)}{\epsilon_s}, \quad (15.9)$$

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q} \nabla \cdot \vec{J}_n, \quad (15.10)$$

where  $\varphi$  is the electrostatic potential,  $q$  is the electron charge,  $n$  is the free electron density,  $p$  is the free hole density,  $N_A$  is the ionized acceptor density,  $N_D$  is the ionized donor density,  $G_n$  is the regeneration rate for electron,  $U_n$  is the recombination rate of electron, and  $\vec{J}_n$  is the electron current density.

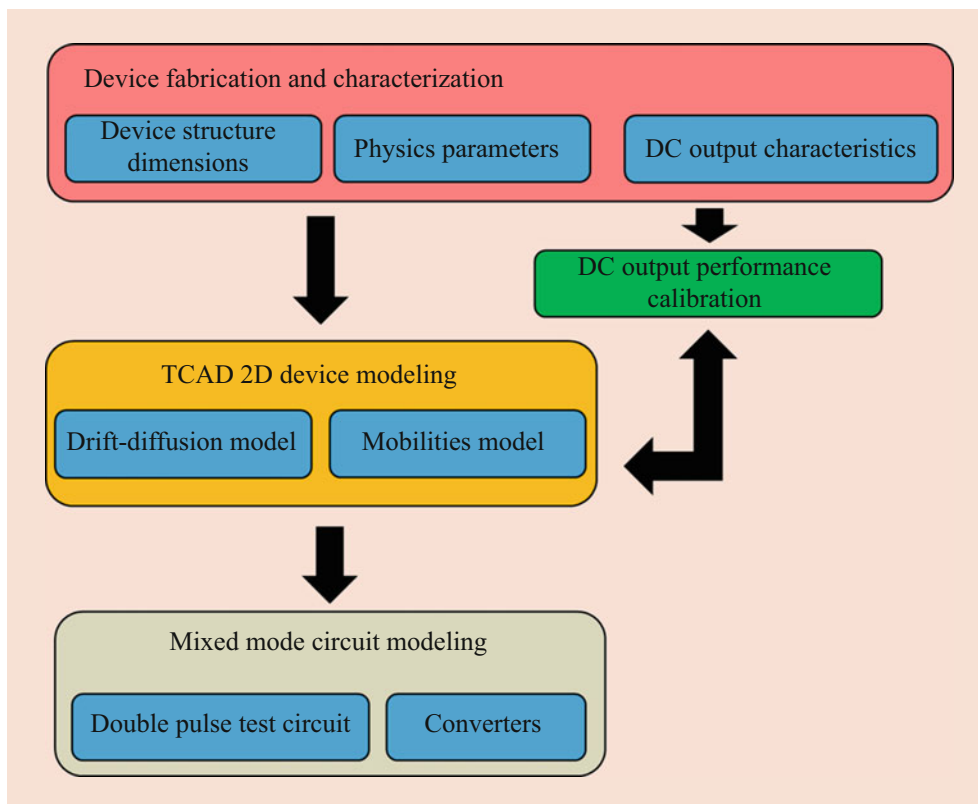


**Fig. 15.18** The flowchart of simulation methodology

## B. Polarization

The non-centrosymmetric compound crystals exhibit polarity along the axes of (0001) of GaN. Two types of polarization existence in the AlGaIn/GaN heterostructure: the strain-induced piezoelectric polarization  $P_{PE}$  and the spontaneous polarization  $P_{SP}$ . The amount of the polarization induced sheet charge density can be written as [65]

$$|\sigma(x)| = \left| 2 \frac{a(0) - a(x)}{a(x)} \left\{ e_{31}(x) - e_{33}(x) \frac{C_{13}(x)}{C_{33}(x)} \right\} + P_{SP}(x) - P_{SP}(0) \right|, \quad (15.11)$$

where the  $x$  is Al mole fraction in AlGaIn, the lattice constant  $a(x)$  is given by  $a(x) = (-0.0077x + 0.3189)$  nm;  $a(t) = (-0.0077t + 0.3189)$  nm elastic constants  $c_{13}(x)$  and  $c_{33}(x)$  can be written as  $c_{13}(x) = (5x + 103)$  GPa and  $c_{33}(x) = (-32x + 405)$  GPa, respectively; piezoelectric constants  $e_{33}(x)$  and  $e_{31}(x)$  can be expressed as  $e_{33}(x) = (0.73x + 0.73)$  C/m<sup>2</sup> and  $e_{31}(x) = (-0.11x - 0.49)$  C/m<sup>2</sup>, respectively; and the spontaneous polarization  $P_{sp}(x)$  is given by  $P_{sp}(x) = (-0.052x - 0.029)$  C/m<sup>2</sup>.

## Electron Mobility

Electron mobility is a key parameter to determine the conductivity of a given semiconductor. A number of theoretical and experimental studies have been performed to understand the electron mobility in GaN. In a recent report, a dual model, one for low-field and the other for high field, was observed to well fit to the reported theoretical and experimental data [66]. The low field electron mobility is given according to the doping and temperature-dependent Arora model [66]:

$$\mu_0(T, N) = \mu_{\min} \left( \frac{T}{300} \right)^{\beta_1} + \frac{(\mu_{\max} - \mu_{\min}) \left( \frac{T}{300} \right)^{\beta_2}}{1 + \left[ \frac{N}{N_{\text{ref}} \left( \frac{T}{300} \right)^{\beta_3}} \right]^{\alpha (T/300)^{\beta_4}}}, \quad (15.12)$$

$T$  is temperature,  $\mu_{\min}$ ,  $\mu_{\max}$ ,  $\beta_1$ ,  $\beta_2$ ,  $\beta_3$ ,  $\beta_4$ , and  $\alpha$  are parameters that can be determined by experiment.

Due to the unique energy band diagram, GaN shows a negative differential region in the field-velocity curve for electrons at very high fields. This is caused by the movement of high-energy electrons from lower  $\Gamma$  valley to the higher M and L valleys, where electrons have higher effective mass, reducing the velocity. The transferred electron effect model was found to have a reasonable fit to the tendencies observed for the experimental and theoretical data [66].

**Table 15.2** Mobility model parameters used in GaN device simulation [66–68]

| Parameters         | Values                              |
|--------------------|-------------------------------------|
| $\mu_{\min}$       | 115 cm <sup>2</sup> /Vs             |
| $\mu_{\max}$       | 1800 cm <sup>2</sup> /Vs            |
| $\beta_1$          | −1.5                                |
| $\beta_2$          | −1.5                                |
| $\beta_3$          | 3.02                                |
| $\beta_4$          | 0.81                                |
| A                  | 0.8                                 |
| $N_{\text{ref}}$   | $7 \times 10^{16}$ cm <sup>−3</sup> |
| $v_{n,\text{sat}}$ | $1.9064 \times 10^7$ cm/s           |
| $E_C$              | $1.7 \times 10^5$ V/cm              |
| $n_1$              | 4.19                                |
| $n_2$              | 0.885                               |
| A                  | 5.64                                |

$$\mu(T, N) = \frac{\mu_{n0}(T, N) + v_{n,\text{sat}} \frac{E^{n_1-1}}{E_C^{n_1}}}{1 + a \left[ \frac{E}{E_C} \right]^{n_2} + \left[ \frac{E}{E_C} \right]^{n_1}}, \quad (15.13)$$

The parameters used in GaN simulation are listed in Table 15.2.

## Device Modeling Calibration

The TCAD simulated device was identical in design with the fabricated device, the structure of which is shown in Fig. 15.19. An excellent agreement between the experimental and the simulated data was obtained by optimizing the physical parameters to replicate GaN's physical parameters. We repeated the optimization until a satisfactory fit of the experimental and simulated data was obtained as illustrated in Fig. 15.20.

Figure 15.21 shows the capacitances in a single E-mode device, the output capacitance ( $C_{\text{oss}}$ ), input capacitance ( $C_{\text{iss}}$ ), and reverse capacitance ( $C_{\text{rss}}$ ) can be written as

$$C_{\text{oss}} = C_{\text{GD}} + C_{\text{DS}} \quad (15.14)$$

$$C_{\text{iss}} = C_{\text{GS}} + C_{\text{DS}} \quad (15.15)$$

$$C_{\text{rss}} = C_{\text{GD}} \quad (15.16)$$

In a cascoded configuration, the D-mode GaN device is cascoded with an E-mode Si MOSFET to render the combination into a normally-off device. The capacitance distribution is shown in Fig. 15.22. Capacitances labeled

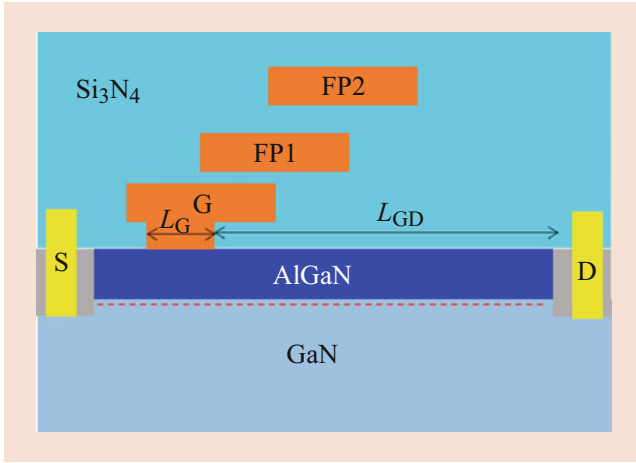


**Fig. 15.19** HEMT structure used in the simulation. The HEMT has three field plates (FP) with a gate to drain distance  $L_{GD} = 10 \mu\text{m}$ , gate length  $L_G = 2 \mu\text{m}$ . (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

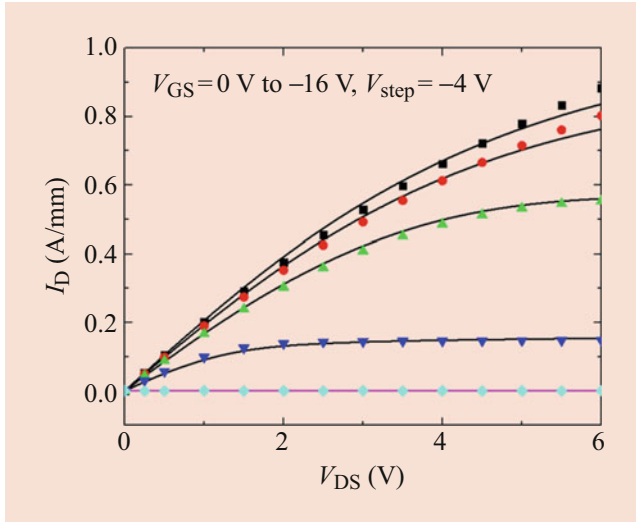


**Fig. 15.20** A comparison of HEMT IV characteristics between simulation (dot curves) and experiment (solid curves). (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

with a subscript “1” and “2” represent for Si MOSFET and AlGaIn/GaN HEMT, respectively.

In this cascoded configuration, the output capacitance ( $C_{oss}$ ), input capacitance ( $C_{iss}$ ), and reverse capacitance ( $C_{rss}$ ) can be written as [64]

$$C_{iss} = C_{GS1} + \frac{C_{GD1} (C_{GS2} + C_{DS1} + C_{DS2})}{C_{GD1} + C_{GS2} + C_{DS1} + C_{DS2}}, \quad (15.17)$$

$$C_{oss} = C_{GD2} + \frac{C_{DS2} (C_{GD1} + C_{DS1} + C_{GS2})}{C_{GD1} + C_{DS1} + C_{GS2} + C_{DS2}}, \quad (15.18)$$

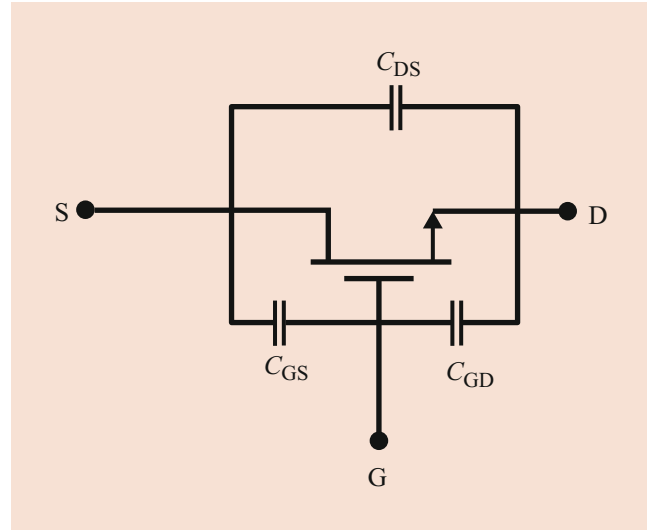


**Fig. 15.21** Capacitance distribution in a single power MOSFET

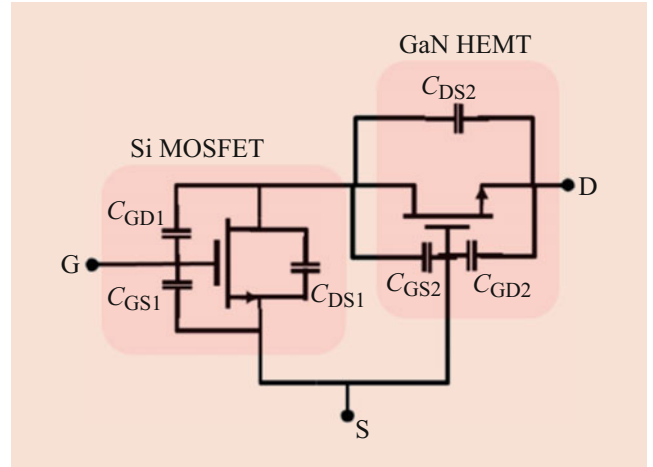


**Fig. 15.22** Capacitance distribution in a cascoded HEMT. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

$$C_{rss} = \frac{C_{DS2} C_{GD1}}{C_{GD1} + C_{DS2}}, \quad (15.19)$$

The  $C$ - $V$  characteristics, which determine the switching performance of a power transistor, was obtained from the simulation and is shown in Fig. 15.23.

Figure 15.24 shows a double pulse test circuit with an inductive load that is widely used in the evaluation of power devices. The free-wheeling diode was assumed to be ideal, and a current source was adopted instead of the inductor to simplify the simulation. The Si MOSFET has a voltage rating of 30 V and  $R_{ON}$  of 20 mΩ. One of the highlights of this work is the successful incorporation of the parasitic inductance in the cascoded device. The parasitic inductances in our model were  $L_G = 2 \text{ nH}$ ,  $L_S = 10 \text{ nH}$ , and  $L_D = 1.9 \text{ nH}$  [64].

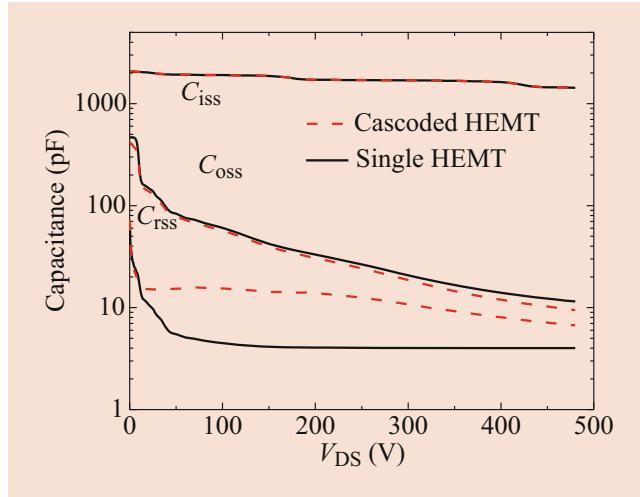


**Fig. 15.23** C-V characteristics in the cascoded HEMT and single E-mode HEMT

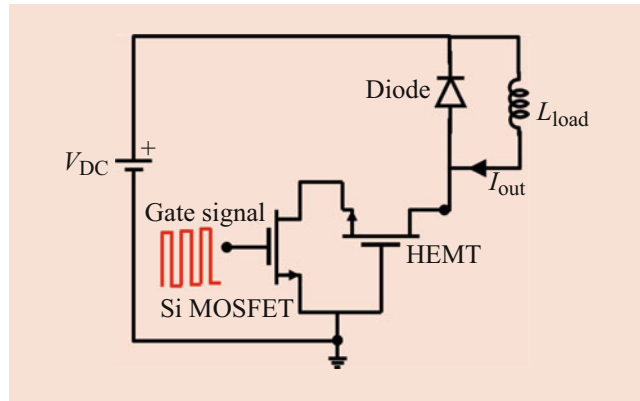


**Fig. 15.24** Test circuit used in the simulation. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

Figure 15.25a shows the turn-on switching characteristics of a 600 V cascoded HEMT, with a total on-state resistance  $R_{ON}$  of 290 m $\Omega$ . The resistance and the capacitance characteristics discussed in the previous section applies to the particular device discussed in this section. A  $V_{DS}$  of 480 V,  $I_D$  of 5.5 A and external gate resistance  $R_G$  of 2  $\Omega$  were used in this simulation.

From the waveforms shown in Fig. 15.8a, the turn-on delay time  $t_{d(on)}$  is 5 ns, and rise time  $t_r$  is 3 ns, showing a turn-on  $\Delta v/\Delta t$  of  $\sim 120$  kV/ $\mu$ s. Figure 15.25b shows the power loss during the turn-on transient, the total energy loss is 37  $\mu$ J.

From the waveforms of Fig. 15.26a, the turn-off delay time  $t_{d(off)}$  is 12.5 ns, and fall time  $t_f$  is 4 ns, giving a turn-off  $\Delta v/\Delta t = \sim 95$  kV/ $\mu$ s. The power loss shown in Fig. 15.26b indicates a turn-off switching loss of 3  $\mu$ J.

For the validation of the device-circuit integrated model, we chose a commercially available HEMT (Transphorm TPH3002LD) to perform the simulation. We first simulated

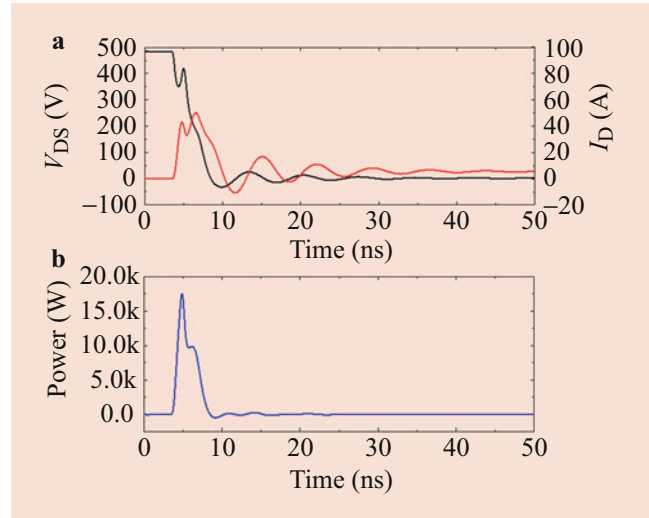


**Fig. 15.25** (a) Simulated turn-on switching waveforms of the cascoded HEMT; (b) power loss during the turn-on switching

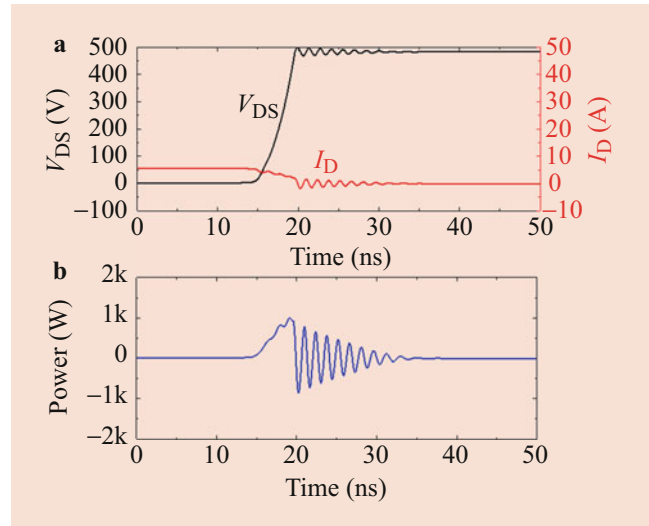


**Fig. 15.26** (a) Simulated turn-off switching waveforms of the cascoded HEMT; (b) power loss during the turn-off switching

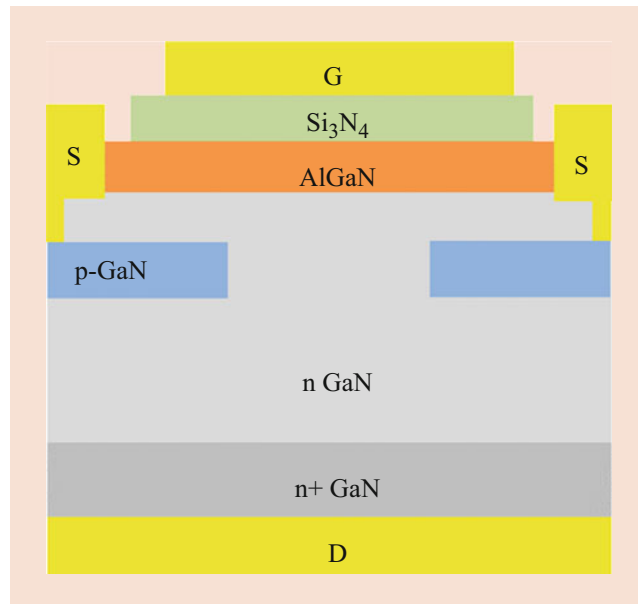
the HEMT and then tested it in a cascode configuration to replicate TPH3002LD, using the same circuit as shown in Fig. 15.24. A comparison between TPH3002LD and our simulated device is shown in Table 15.3. A reasonable agreement was obtained as evident from Table 15.3, now confirming both drift-diffusion and circuit model, and hence our hybrid modeling technique. The reasonable agreement of the TPH3002LD with our simulated data built and reassured a reliable platform to now apply for any GaN power device and project its switching performance.

### Modeling of Vertical GaN Devices

Using the device-circuit-integrated model built in the Silvaco's MixedMode platform and calibrated using GaN

**Table 15.3** Comparison of the simulated and commercial GaN cas-coded HEMT

| Parameters            | Transphorm<br>TPH3002LD | Simulated GaN<br>cas-coded HEMT | Test conditions                                                                 |
|-----------------------|-------------------------|---------------------------------|---------------------------------------------------------------------------------|
| $V_{BR}$ (V)          | 600                     | 700                             |                                                                                 |
| $V_{TH}$ (V)          | 1.8                     | 2                               |                                                                                 |
| $R_{ON}$ ( $\Omega$ ) | 0.29                    | 0.29                            |                                                                                 |
| $Q_G$ (nC)            | 9.3                     | 13                              | $V_{DS} = 100$ V,<br>$V_{GS} = 0-4.5$ V,<br>$I_D = 5.5$ A                       |
| $t_{d(on)}$ (ns)      | 7                       | 5                               | $V_{DS} = 480$ V,<br>$V_{GS} = 0-10$ V,<br>$I_D = 5.5$ A,<br>$R_G = 2$ $\Omega$ |
| $t_r$ (ns)            | 3                       | 3                               |                                                                                 |
| $t_{d(off)}$ (ns)     | 11                      | 12.5                            |                                                                                 |
| $t_f$ (ns)            | 4.5                     | 4                               |                                                                                 |
| $C_{oss(tr)}$ (pF)    | 63                      | 50.9                            | $V_{GS} = 0$ V,<br>$V_{DS} = 480$ V                                             |
| $C_{oss(er)}$ (pF)    | 36                      | 28                              |                                                                                 |
| $C_{oss}$ (pF)        | 26                      | 18                              | $V_{GS} = 0$ V,<br>$V_{DS} = 400$ V,<br>$f = 1$ MHz                             |
| $C_{iss}$ (pF)        | 785                     | 1631                            |                                                                                 |
| $C_{rss}$ (pF)        | 3.5                     | 3                               |                                                                                 |

**Fig. 15.27** Schematic of a normally-on CAVET

HEMTs [64], the switching performance of the vertical GaN transistor was analyzed. In this section, a current aperture vertical electron transistor (CAVET) was used, since this device was one of the most developed vertical GaN devices. The structure of the CAVET is shown in Fig. 15.27.

Figure 15.27 shows the schematic of a normally-on CAVET. A thick n-GaN with  $10^{16}$   $\text{cm}^{-3}$  doping was designed to form the drift region on a conductive GaN ( $10^{18}$   $\text{cm}^{-3}$ ) substrate. 0.4  $\mu\text{m}$ -thick p-type current blocking layers (CBLs) were implemented with a doping density of  $3 \times 10^{17}$   $\text{cm}^{-3}$  to block current from flowing through any other path other than the designed aperture ( $N_D = 3 \times 10^{17}$   $\text{cm}^{-3}$ ). AlGaIn/GaN channel was defined on top of the CBL and the aperture to conduct electrons from the source through a high mobility 2D channel obtained at the hetero-interface. Sources contacting the 2D electron gas were designed on either side of the gate at a distance of 2  $\mu\text{m}$ . The p-GaN CBLs were connected to the source to provide a discharge path for any electrons trapped in the p-type layer.

CAVETs are normally-on devices similar to GaN HEMTs. Techniques that are typically applied to HEMTs can be applied to CAVETs to render it normally-off. We adopted a cascoded CAVET approach in this work to achieve normally-off operation, where the cascode was designed with a low-voltage Si MOSFET. The cascoded CAVET was subjected to switching operation, and detailed performance matrix was generated.

Figure 15.28 shows the cascode configuration designed with a low-voltage normally-off Si MOSFET as the input and a high-voltage normally-on CAVET as the output. The current paths of the forward conduction are labeled with the arrows in Fig. 15.28a. In the forward conduction, the total on-state resistance ( $R_{on}$ ) is the sum of the MOSFET  $R_{on}$  and the CAVET  $R_{on}$ . In the reverse conduction cycle (shown in Fig. 15.28b), the current flows through the body diode of the Si MOSFET and the CAVET channel. It is important to note that the body diode of the CAVET does not conduct current at any time of the operation.

Figure 15.29 shows the turn-on switching characteristics of a 1.2 kV cascoded CAVET, with a total on-state resistance  $R_{ON}$  of 80 m $\Omega$ . A  $V_{DS}$  of 800 V,  $I_D$  of 20 A and external gate resistance  $R_G$  of 2.5  $\Omega$  were used in this simulation. Before we discuss the results a close-up look at the turn-on event in a switching cycle will be befitting. The turn-on event can be divided into three stages [64].

In the first stage, when a  $V_{GS}$  is applied to the gate electrode, the gate current  $I_G$  starts charging the Si MOSFET gate to source capacitor  $C_{GS\_MOS}$ . As a result, Si MOSFET gate to source voltage  $V_{GS\_MOS}$  increases.

Once the  $V_{GS\_MOS}$  reaches the threshold voltage of Si MOSFET, in the second stage, the MOSFET channel is turned on, and channel current increases. The Si MOSFET channel current discharges three capacitors: Si MOSFET gate to drain capacitor  $C_{GD\_MOS}$ , Si MOSFET drain to source capacitor  $C_{DS\_MOS}$ , and GaN CAVET gate to source capacitor  $C_{GS\_CAVET}$ , as a result of which, MOSFET drain to source voltage  $V_{DS\_MOS}$  decreases, and the CAVET source to gate voltage  $V_{SG\_CAVET}$  decreases as well.

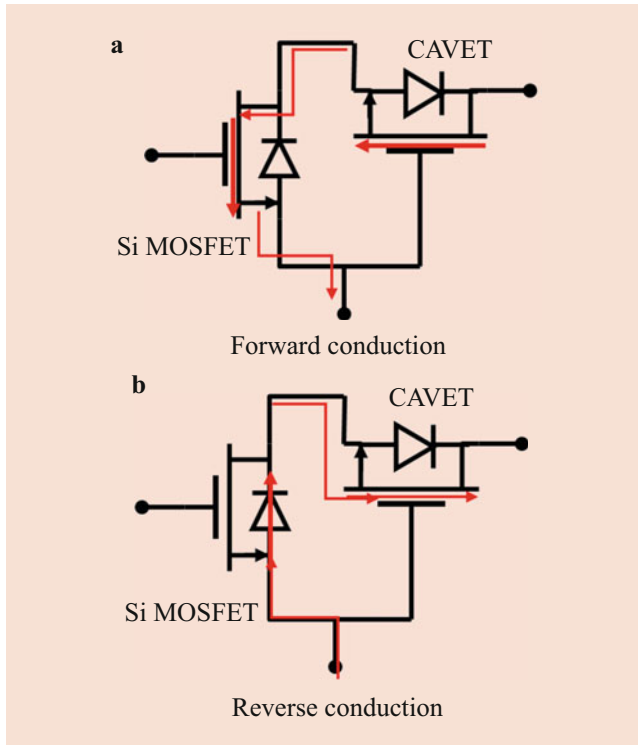


**Fig. 15.28** (a) Forward conduction of the cascoded CAVET; (b) reverse conduction of the cascoded CAVET

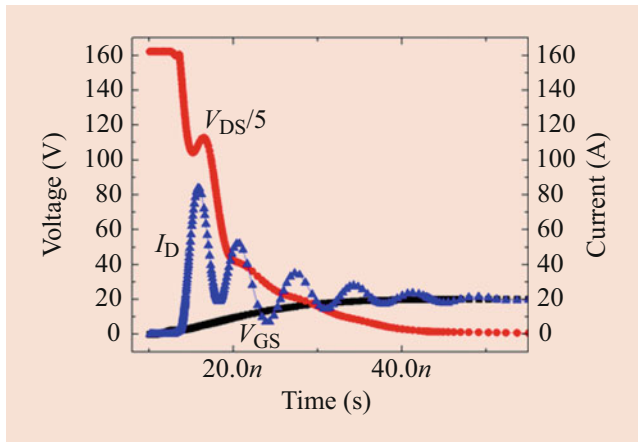


**Fig. 15.29** Simulated turn-on switching waveforms of the cascoded CAVET. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

Third, when  $V_{SG\_CAVET}$  reaches the threshold voltage of GaN CAVET, CAVET channel current increases, and this current start discharging the GaN CAVET drain to source capacitor  $C_{DS\_CAVET}$  and GaN CAVET gate to drain capacitor  $C_{GD\_CAVET}$ , reducing  $V_{DS\_CAVET}$  further.

From the waveforms shown in Fig. 15.29, the turn-on delay time  $T_{on-delay}$  is 2 ns, and rise time  $T_r$  is 16 ns, showing

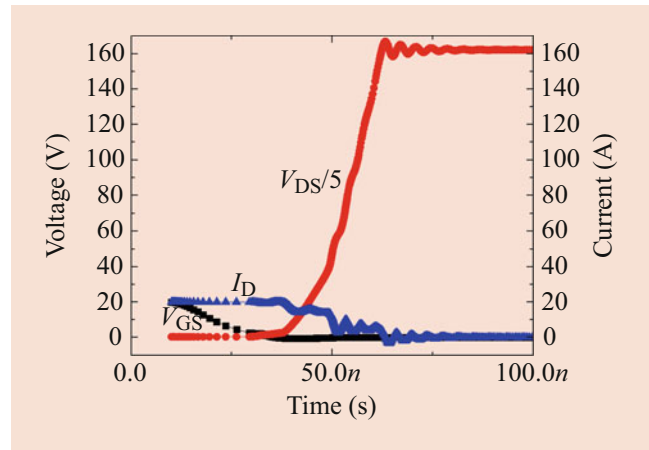


**Fig. 15.30** Simulated turn-off switching waveforms of the cascoded CAVET. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

a turn-on  $\Delta v/\Delta t$  of 40 kV/ $\mu$ s. The total gate charge of the CAVET is 88 nC.

The turn-off switching waveforms are shown in Fig. 15.30. Similar to the turn-on transient, the turn-off phenomenon can be subdivided into three stages.

First, when the applied MOSFET  $V_{GS}$  changes from on to off state (from 10 V to 0 V), the Si MOSFET gate to source capacitor  $C_{GS\_MOS}$  is discharged and as a consequence, Si MOSFET channel current decreases, which is smaller than the operation current (output current in current source), and the excess current charges the MOSFET drain to source capacitor  $C_{DS\_MOS}$ , increasing  $V_{DS\_MOS}$ . Since the GaN CAVET source to gate capacitor  $C_{SG\_CAVET}$  is in parallel with  $C_{DS\_MOS}$ , the voltage  $V_{SG\_CAVET}$  also increases.

Next, when  $V_{SG\_CAVET}$  increases, the channel current in CAVET decreases, as a result, the channel current is smaller than the output current. The excess current starts charging CAVET drain to source capacitor  $C_{DS\_CAVET}$  and gate to drain capacitor  $C_{GD\_CAVET}$ , as a result,  $V_{DS\_CAVET}$  increases.

When  $V_{SG\_CAVET}$  reaches a value smaller than the threshold voltage of CAVET, the channel is completely pinched off, and the remaining gate current continues to charge the capacitors:  $C_{GD\_MOS}$ ,  $C_{DS\_MOS}$ ,  $C_{GD\_CAVET}$ , and  $C_{DS\_CAVET}$ , further raising the  $V_{DS\_MOS}$  and  $V_{DS\_CAVET}$ .

From the waveforms of Fig. 15.30, the turn-off delay time  $T_{off-delay}$  is 29.5 ns, and fall time  $T_f$  is 18 ns, giving a turn-off  $\Delta v/\Delta t = 35.6$  kV/ $\mu$ s.

Table 15.4 shows the comparison of CREE SiC MOSFET (CREE Inc.), simulated SiC MOSFET, and simulated cascoded CAVET with the same voltage and current rating. The switching performance agreement between CREE and simulated SiC MOSFETs provides the competency of the model. When compared to standard SiC MOSFET, cascoded CAVET has faster switching time, and lower switching loss, hence enabling higher frequency operation.

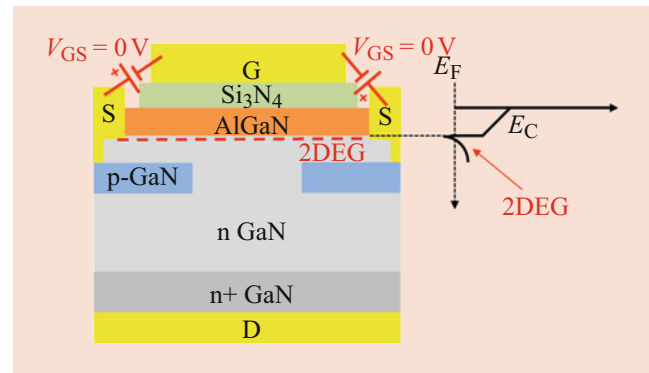
**Table 15.4** Switching performance comparison of SiC MOSFET and GaN CAVET

| Parameters             | Cree SiC MOSFET (CREE Inc.) | Simulated SiC MOSFET [64] | Simulated GaN CAVET [64] |
|------------------------|-----------------------------|---------------------------|--------------------------|
| $V_{BR}$ (kV)          | 1.2                         | 1.2                       | 1.2                      |
| $R_{on}$ (m $\Omega$ ) | 80                          | 80                        | 80                       |
| $t_{off-delay}$ (ns)   | 40                          | 55                        | 29.5                     |
| $t_f$ (ns)             | 38                          | 25                        | 18                       |
| $t_{on-delay}$ (ns)    | 13                          | 10                        | 2                        |
| $t_r$ (ns)             | 24                          | 27                        | 16                       |
| $Q_G$ (nC)             | 90.8                        | 157                       | 88                       |
| $E_{off}$ ( $\mu$ J)   | 305                         | 312                       | 57                       |
| $E_{on}$ ( $\mu$ J)    | 305                         | 304                       | 152                      |
| $E_{ts}$ ( $\mu$ J)    | 610                         | 616                       | 209                      |

### 15.3.3 A Review of CAVET

CAVETs are vertical GaN vertical devices that take full advantage of the polarization-based two-dimensional electron gas (2DEG) in its design. Comprised of a 2DEG induced channel to carry the current, a CAVET needs a thick homoepitaxially grown drift region to hold the blocking voltage. There have been two types of approach in fabricating CAVETs: (1) planar CAVET and (2) trench CAVET. The planar CAVET has an AlGaIn/GaN 2DEG channel in the c-plane, which has high electron density and high mobility. The trench CAVET adopts the semi-polar plane as the channel, the density of the electrons depends on the slope of trench sidewalls.

The first GaN CAVET based on a sapphire substrate was developed in 2004 [69]. The device structure began with a p-GaN/n-GaN/n<sup>+</sup>GaN epilayers. An aperture region was etched and an AlGaIn/GaN HEMT structure was regrown by MOCVD to refill the aperture region and served as the channel as well. The design of the first GaN CAVET was for radio frequency (RF) applications. Several years later in 2008, the first power GaN CAVET based on bulk GaN substrate was reported with the CBL formed by Mg-ion implantation [70]. The device process began with the MOCVD grown n-GaN on conductive bulk GaN substrate; then, the selective area Mg-ion-implantation was implemented to form the CBL to block current from the aperture region other than any other paths. The top AlGaIn/GaN structure was regrown by MBE. The first high-voltage CAVET with switching characteristics was demonstrated by Chowdhury et al. with a 300 V breakdown voltage and a  $R_{on,sp}$  of 2.2 m $\Omega$ •cm<sup>2</sup> [71]. A significant progress in the device development was realized with the demonstration of 1.5 kV JFET (a variant of CAVET) on bulk substrate by H. Nie et al. in 2014 from Avogy Inc. [72].

**Fig. 15.31** Cross section of an on-state GaN CAVET and the conduction band diagram

### 15.3.4 Operation Principle of the CAVET

A CAVET is a unique design where the best properties that GaN offers are best utilized. Polarization doping is one of these properties which is leveraged in a CAVET design. Due to the positive polarization charge located at the AlGaIn/GaN interface, a triangular quantum well is formed, and electrons are attracted (shown in Fig. 15.31). The high-density electrons are confined in the triangular quantum well, forming the 2DEG. Under a zero-gate bias, the channel is conductive due to the 2DEG, the device is in the on-state. During on-state of the CAVET, the electrons from the source go through the 2DEG channel, the aperture and the drift region and are finally collected by the drain electrode. The overlap between the gate electrode and the CBL is the effective gate length that offers channel modulation.

Like in a HEMT, in order to pinch off the 2DEG channel in a CAVET, a negative gate bias is required. At the off-state, the electrons in the channel are depleted by the gate potential. The p-n junction formed by p-type (or Mg-implanted) CBL and drift region blocks the off-state voltages. Figure 15.29 shows the schematic of a planar CAVET where the CBL (shown as p-GaN) is formed using an ion implantation process of GaN with Mg ions. During the on-state, the voltage applied between the source and the drain drops across the channel. The design must ensure that the aperture is more conductive than the channel. Under the off-state, the depletion region is extended into the drift layer to sustain the drain to source voltage. Besides forcing the current flow through the aperture and blocking any parasitic current flow from drain to source, the CBL also needs to be conductive enough to prevent charge trapping which may lead to current collapse. From our experiments [73, 74], we found that CAVETs with Al-implanted CBL was dispersive, whereas CAVETs with Mg-implanted CBL were dispersionless. CAVETs with ion-implanted CBL require regrowth of AlGaIn/GaN channel. The regrown channel and the aperture

are grown on the planar surface where CBL is formed by ion implantation. One significant challenge in the ion-implanted process was the out-diffusion of Mg from the CBL to the regrown layers causing the channel to get totally wiped off. Although several tactics were employed, one of those being using a thin AlN diffusion-stopper layer [73, 74], the most successful technique was achieved through the regrowth of the channel through a lower temperature MBE regrowth that led to the successful CAVETs. In an alternative approach MOCVD grown p-type layers were used to form the CBL. This is the basic building block for a Trench CAVET which is discussed next.

### 15.3.5 Trench CAVET

The conventional GaN CAVET typically uses Mg-implanted p-GaN for the CBL. A major fabrication challenge is posed by Mg out-diffusion during the regrowth process. First, the channel resistance can go very high due to the diffusion of Mg species into the channel, thereby depleting 2DEG. To prevent the diffusion of Mg into the regrown channel the regrowth temperature of the channel in a CAVET is restricted, making it rely on low-temperature growth processes. Low-temperature MOCVD regrowth process does not typically result into a high-quality material. MBE regrowth although has proven to be successful in arresting Mg diffusion, there are concerns on the formation of vertical highly conductive paths under metal-rich growth conduction, causing shorts in the device. An MBE-regrown channel requires exposure of the sample to the atmosphere for prolonged interval, and process limitations make it challenging to remove environmental contaminants from the regrowth interface. Low-temperature flow modulation epitaxy by MOCVD may be considered an alternative, but it is not yet understood whether the material quality produced in such a fashion that can support high-current and high-voltage devices.

A solution to the aforementioned problem was proposed by introducing a trench gate structure into the conventional CAVET, as shown in Fig. 15.32 [75, 76]. Instead of using Mg-implanted p-GaN for the CBL, the trench CAVET adopts MOCVD-grown Mg-doped p-GaN as the CBL material. The trench CAVET utilizes the regrown AlGaIn/GaN on the trench sidewall as the channel. The trench sidewall angle determines the polarization scale of the channel: a 90-degree angle indicates a non-polar plane, and a 45-degree angle indicates a semi-polar plane. The threshold voltage in a trench CAVET can be adjusted by the trench sidewall angle. The functioning of a trench CAVET is similar to a trench MOSFET, except for the AlGaIn/GaN channel. In a conventional trench MOSFET, the channel is formed by inversion layer between the oxide and the p-type semiconductor. The electron mobility in the inversion layer is typically below

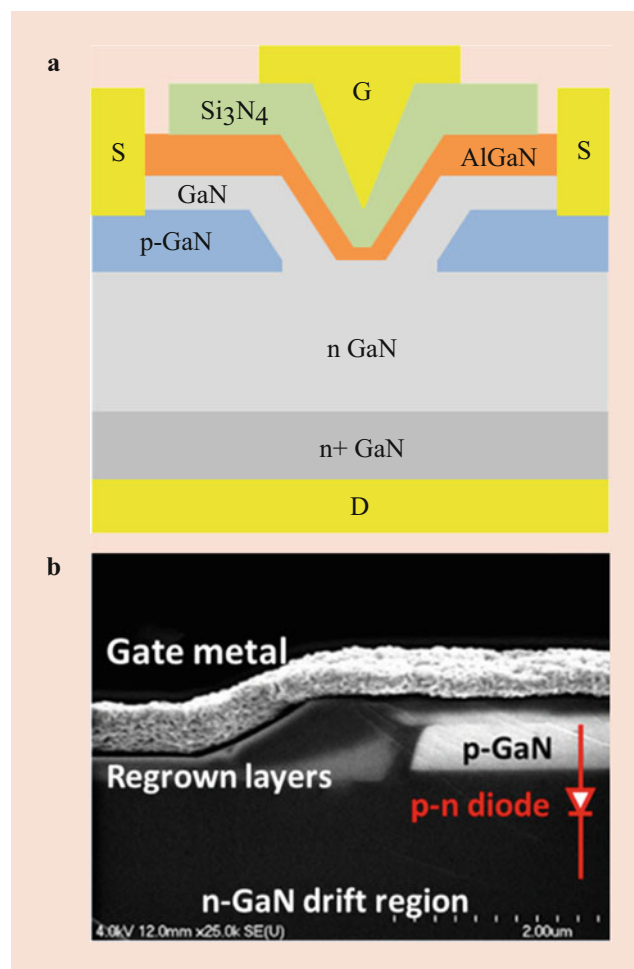


**Fig. 15.32** (a) Schematic illustrations of the trench CAVET. (b) SEM image showing a buried p-n junction which blocking voltage in the off-state. (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [75])

50 cm<sup>2</sup>/Vs, limited by the interface roughness scattering. However, in a trench CAVET, the channel is formed by the 2DEG, which takes the advantage of the high mobility in the HEMT structure. Ideally, the channel mobility in a trench CAVET can be as high as 1690 cm<sup>2</sup>/Vs [77].

In GaN, a robust oxide technology is not available yet. However, thanks to the development of GaN HEMT in the last decade, the in situ grown Si<sub>3</sub>N<sub>4</sub> on AlGaIn/GaN structure has low interface traps, which is essential to the device reliability. A trench CAVET takes the advantage of the matured HEMT gate dielectric technology to suppress gate leakage.

The first metal-insulator-semiconductor (MIS) gate trench CAVET was reported by Ji et al. in 2016 on bulk GaN substrates [75]. The device had a breakdown voltage of 225 V limited by the gate-to-drain breakdown. By using a thicker gate dielectric layer and a low damage RIE trench etch, a high breakdown voltage of 880 V was obtained in 2018 [76]. A low hysteresis of ~0.1 V was achieved by using high-quality in situ Si<sub>3</sub>N<sub>4</sub> gate dielectric (Figs. 15.33, 15.34, and 15.35).

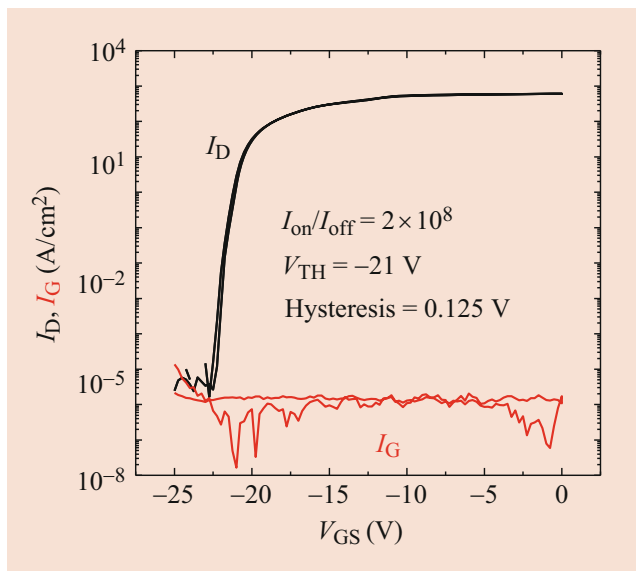


**Fig. 15.33** Double-swept  $I_D$ - $V_{GS}$  transfer characteristics of the fabricated trench CAVET [76]. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [76])

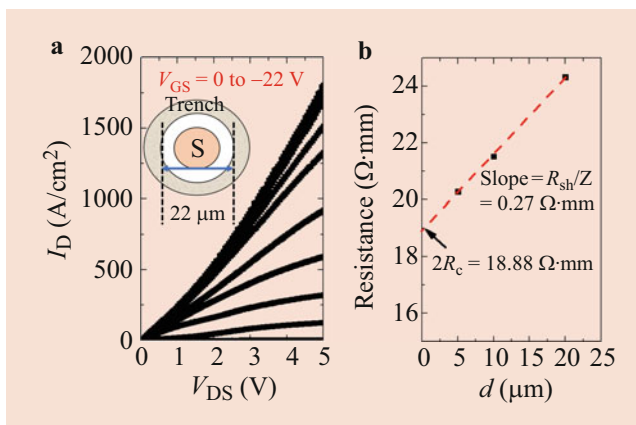


**Fig. 15.34** (a)  $I_D$ - $V_{DS}$  characteristics of the fabricated trench CAVET. (b) Analysis of contact resistance [76]. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [76])

The p-GaN gate structure is widely used in normally-off lateral GaN HEMTs. Due to the high electron density of 2DEG induced by the polarization charge, the threshold voltage of p-GaN gated HEMT is typically less than 2 V. However, a more positive threshold voltage can be realized in a p-GaN gated trench CAVET with the channel formed at the semi-polar plane. This was first demonstrated by Shibata et al. in 2016 [77]. Based on a p-n epitaxial structure on bulk GaN substrate, a “V”-shaped trench was formed using inductively coupled plasma (ICP) etching, the p-GaN/AlGaN/GaN triple layers were regrown over the trench by MOCVD. Because the channel locates at the semi-polar plane instead of the c-plane, the threshold voltage shifted toward the positive side by 1.5 V. A high positive threshold voltage of 2.5 V was

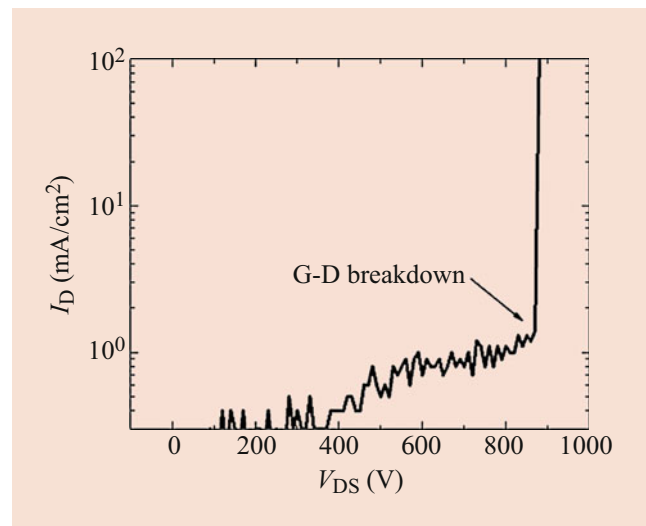


**Fig. 15.35** Off-state characteristics of the fabricated trench CAVET [76]. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [76])

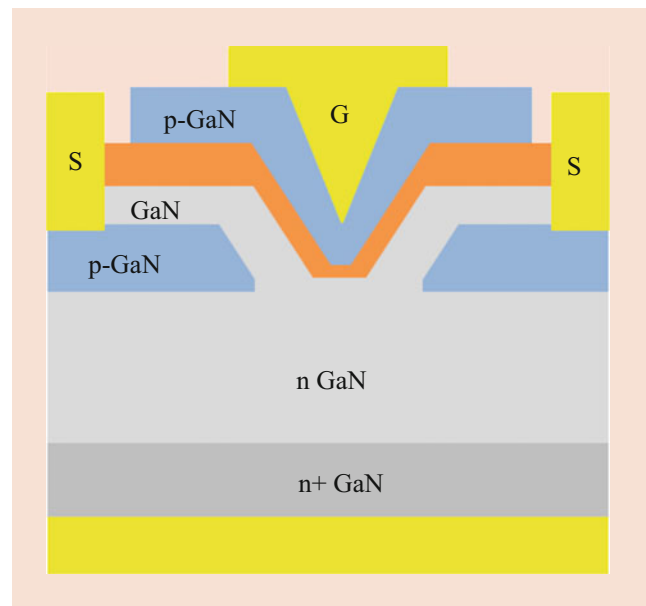


**Fig. 15.36** Trench CAVET with a p-GaN gate layer [77]

demonstrated with 1700 V blocking capability on a 13  $\mu\text{m}$ -thick drift region offering a low specific on-resistance of 1  $\text{m}\Omega\text{-cm}^2$  (Fig. 15.36).

### 15.3.6 Vertical MOSFETs

Vertical GaN MOSFETs are the other branch of devices, showing a promising performance by offering a normally-off solution, thereby overcoming a significant drawback of any GaN HEMT-based design.

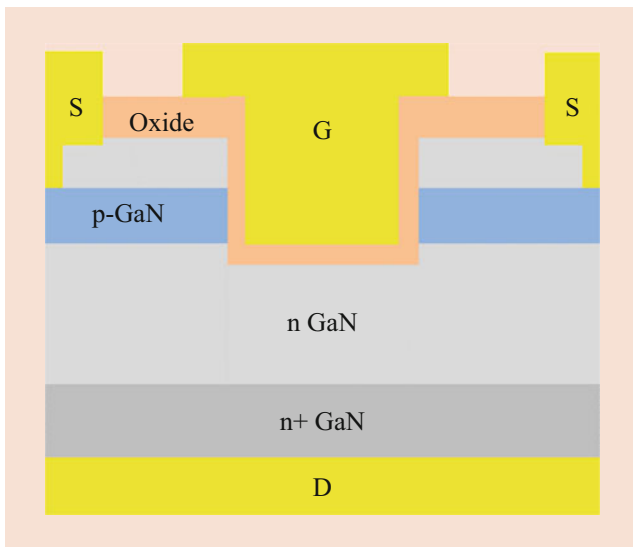


**Fig. 15.37** Structure of GaN MOSFET

There are two types of MOSFET reported so far (1) non-regrowth-based MOSFET and (2) regrowth-based MOSFET (OGFET). In this section, both devices will be introduced.

Since the development of dry etch technology in the early 1990s, the trench MOSFET has been a dominant device structure for power electronics. To date, both Si- and SiC-based trench MOSFET have been commercialized and shown excellent performance. However, because of the absence of bulk GaN substrate, the GaN-based trench MOSFET was not available until 2004–2005. In 2007, the first GaN MOSFET was reported by Otake et al. [78], the device has a high threshold voltage of 5.1 V. After 7 years of intense research, a 1.6 kV device was developed by Oka et al. in 2014 [79].

Figure 15.37 shows the structure of a vertical GaN MOSFET. A key feature of these devices, the p-n junction between source and drain is formed by p-base and n-drift regions. The device breakdown voltage is determined by the reverse characteristics of the main p-n junction. A n+ source region is created partially on top of the p-base region, while the junction between the n+ source region and the p-base region is connected to the source contact to improve the breakdown voltage by eliminating the n-p-n open base effect. The channel located at the etched sidewall is formed by the inversion layer of the MOS structure.

Compared to the CAVET structure, there are two basic advantages of the MOSFET: (1) the MOSFET is a reliable normally-off device with a high threshold voltage over 2 V; (2) regrowth can be avoided which makes the process less challenging, reducing the cost and turnaround time. Such advantages of the MOSFET make it an attractive design for vertical GaN transistors. However, for GaN MOSFET, the biggest challenge lies in the channel electron mobility of

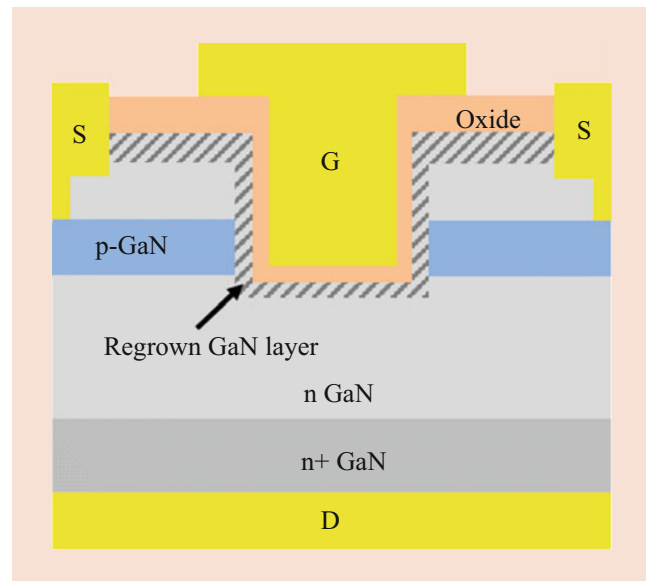


**Fig. 15.38** Structure of GaN OGFET. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [168])

the device. During on-state, the electrons flow through the inversion layer of the sidewall MOS structure, the channel electron mobility is limited by the surface roughness and impurity scattering. Another issue along with the poor channel property is the device reliability. The GaN MOSFET cannot be widely recognized without a strong reliability.

### 15.3.7 Regrowth-Based Vertical MOSFET (OGFET)

GaN OGFET is a modified structure based on the conventional trench MOSFET. Compared to the conventional trench MOSFET, the OGFET has two features: (1) an unintentional doped (UID) GaN interlayer is used as the channel region, which enhances the channel electron mobility to reduce the Coulomb scattering by the dopants; (2) the oxide is in situ grown by MOCVD, which reduces the interface states and improves the gate oxide reliability. The novelty of the OGFET is enhancing the channel electron mobility without sacrificing the normally-off behavior.

The working principle of the OGFET is similar to the MOSFET. Under a zero  $V_{GS}$ , the electrons in the GaN interlayer (shaded region in Fig. 15.38) are depleted by the p-GaN base region making the OGFET go to its off-state. The energy band diagram and the simulated electron contour are shown in Fig. 15.39. The p-n diode formed by the p-GaN base region and the n-GaN drift region is used to hold the high off-state blocking voltage. The electric field distribution along the p-GaN base region and the n-GaN drift region is shown in Fig. 15.40.

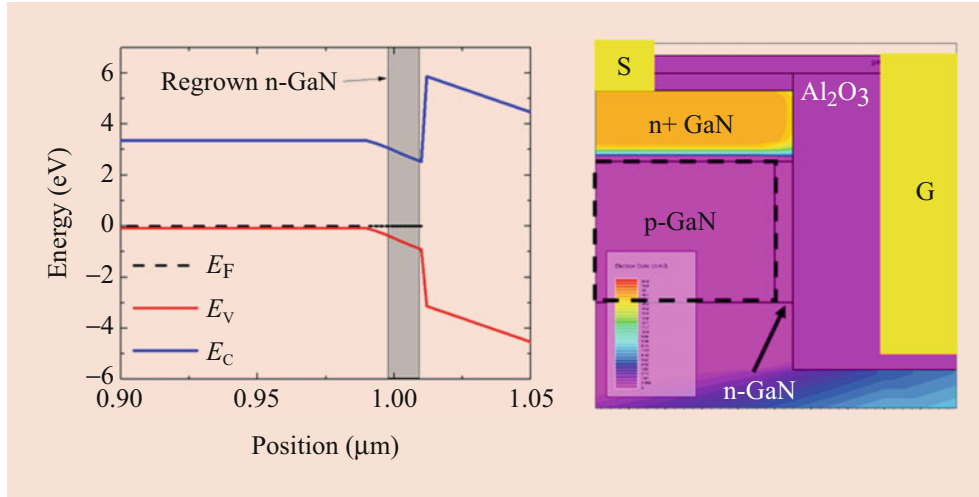


**Fig. 15.39** Energy band diagram and the electron distribution of the OGFET in off-state

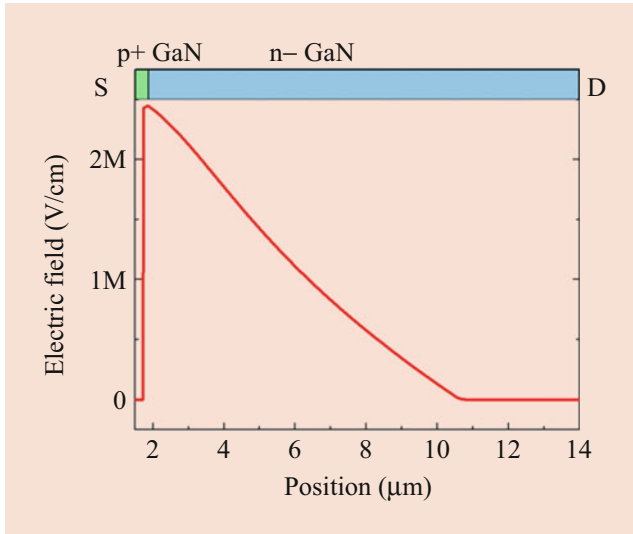


**Fig. 15.40** Electric field distribution along the drift region

Under a positive  $V_{GS} > \text{threshold}$ , electrons are accumulated in the UID GaN insert layer, and the transistor is in its on-state. The energy band diagram and the electron concentration is shown in Fig. 15.41. Because of the enhanced channel electron mobility, the OGFET has smaller  $R_{on,sp}$  compared to the conventional trench MOSFET.

In 2016, Gupta et al. reported the first OGFET results based on the sapphire substrates, the device showed a 60%  $R_{on,sp}$  reduction while maintaining the threshold voltage  $> 2$  V [80]. In 2017, Gupta et al. demonstrated an OGFET on bulk GaN substrates with a breakdown voltage of 990 V and a low  $R_{on,sp}$  of  $2.6 \text{ m}\Omega\cdot\text{cm}^2$  [81]. In the same year, Ji et al. demonstrated a high-performance OGFET with a breakdown voltage over 1.43 kV with a low  $R_{on,sp}$  of  $2.2 \text{ m}\Omega\cdot\text{cm}^2$  [82]. The  $I$ - $V$  characteristics of the fabricated OGFET are shown

in Fig. 15.26. Figure 15.27 shows the transfer  $I_D$ - $V_{GS}$  characteristics and the gate leakage. The threshold voltage,  $V_{TH}$ , defined at a current level of  $10^{-4} \text{ A/cm}^2$  ( $I_{on}/I_{off} = 10^6$ ), obtained was 4.7 V (when  $V_{GS}$  sweeps up). A clockwise hysteresis of  $\Delta V_{TH}$  of 0.3 V was observed. Low sub-threshold slope of 283 mV/decade was measured from  $I_D = 10^{-5} \text{ A/cm}^2$  to  $10^{-2} \text{ A/cm}^2$ . The off-state characteristics of the fabricated devices are shown in Fig. 15.42 (Figs. 15.43 and 15.44).

### 15.3.8 Static Induction Transistor

Static induction transistor is another form of vertical devices, in which current flows vertically through a short channel as shown in Fig. 15.45 [83, 84]. From the equivalent circuit, the overall transconductance,  $G'_m$ , is described by intrinsic transconductance,  $G_m$ , and series channel resistance,  $r_s$ , to be  $G'_m = G_m / (1 + r_s \cdot G_m)$ . The small distance between gate and source induces  $r_s \rightarrow 0$ , so that  $G'_m \rightarrow G_m$ . Consequently, SIT shows a triode-like non-saturating output property, not following square-law behavior shown in the pentode-like FET, which has  $r_s \cdot G_m \gg 1$ , leading to  $G'_m \rightarrow 1/r_s$ . The drain current is controlled by electrostatically induced potential energy barrier, that is why the transistor is named, depending on the gate and drain bias. With no gate bias, the drain current is simply defined by the effective cross-sectional area of the channel ( $A_{eff}$ ), which is related to the depletion width formed at the junctions, so that  $I_d = q A_{eff} v_d N_d$ , where  $q$  is electron charge,  $v_d$  is electron velocity, and  $N_d$  is electron density. As applying more negative gate bias, the depletion width increases further and merges at pinch-off, developing the electrostatic barrier in the channel. The minimum barrier height ( $\Phi_0$ ), saddle point, now depends on the drain bias through the drain induced barrier lowering (DIBL) as shown

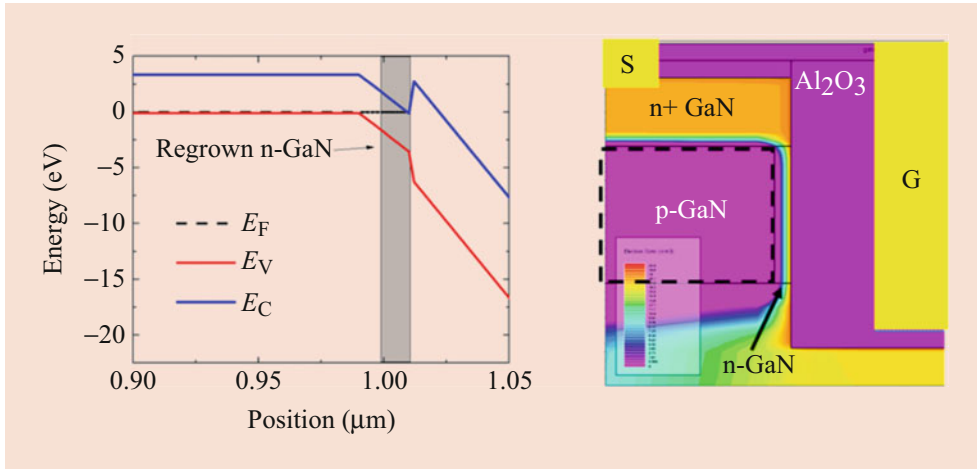


**Fig. 15.41** Energy band diagram and the electron distribution of the OGFET in on-state

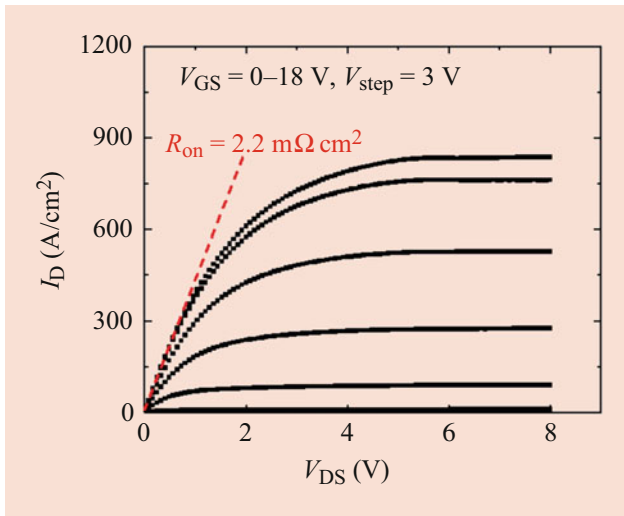


**Fig. 15.42** I-V characteristics of fabricated OGFET with saturation current density of 850 A/cm² and  $R_{on,sp}$  of 2.2 mΩ·cm². (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [82])

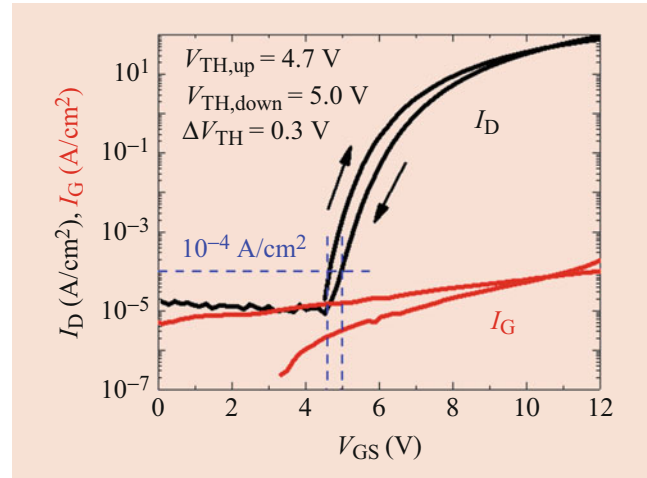


**Fig. 15.43** Transfer characteristics of the fabricated OGFET (black curves) and gate leakage (red curves). The threshold voltages of sweep up and down were 4.7 V and 5 V (defined at a current level of 10<sup>−4</sup> A/cm²). The sub-threshold slope was 283 mV/decade measured from 10<sup>−5</sup> A/cm² to 10<sup>−2</sup> A/cm². (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [82])

in Fig. 15.46, governing the electron flow in a manner of thermionic emission, so  $I_d$  can be described as,

$$I_d = I_0 \exp \left\{ \frac{q}{kT} (\Phi_0 - \alpha V_d) \right\}, \quad (15.20)$$

where  $\alpha$  is DIBL coefficient. As increasing drain bias, space charge limited conduction is dominant in the current flow, and the electron velocity becomes saturated. Under high gate and drain bias, the current can be modified as

$$I_d = 2A_{\text{eff}} \epsilon_s v_{\text{sat}} \frac{V_d}{L^2}, \quad (15.21)$$

where  $\epsilon_s$  is permittivity,  $v_{\text{sat}}$  is saturation velocity, and  $L$  is channel length. This linear relationship between  $I_d$  and  $V_d$  together with small channel resistance provide benefits to power devices.

The SIT design has been developed from buried-gate to recessed-gate structures using various materials such as SiC and GaN [85–88]. Figure 15.47 presents the output and transfer characteristic of the GaN SIT. By using a Schottky junction, the SIT was fabricated without any p-type GaN or gate dielectrics, which involve difficulty in the activation and reliability. The current density and on-resistance are estimated to be 0.65 kA cm<sup>−2</sup> and 1.48 mΩcm². It is also shown the off current increase as applying larger  $V_d$  because

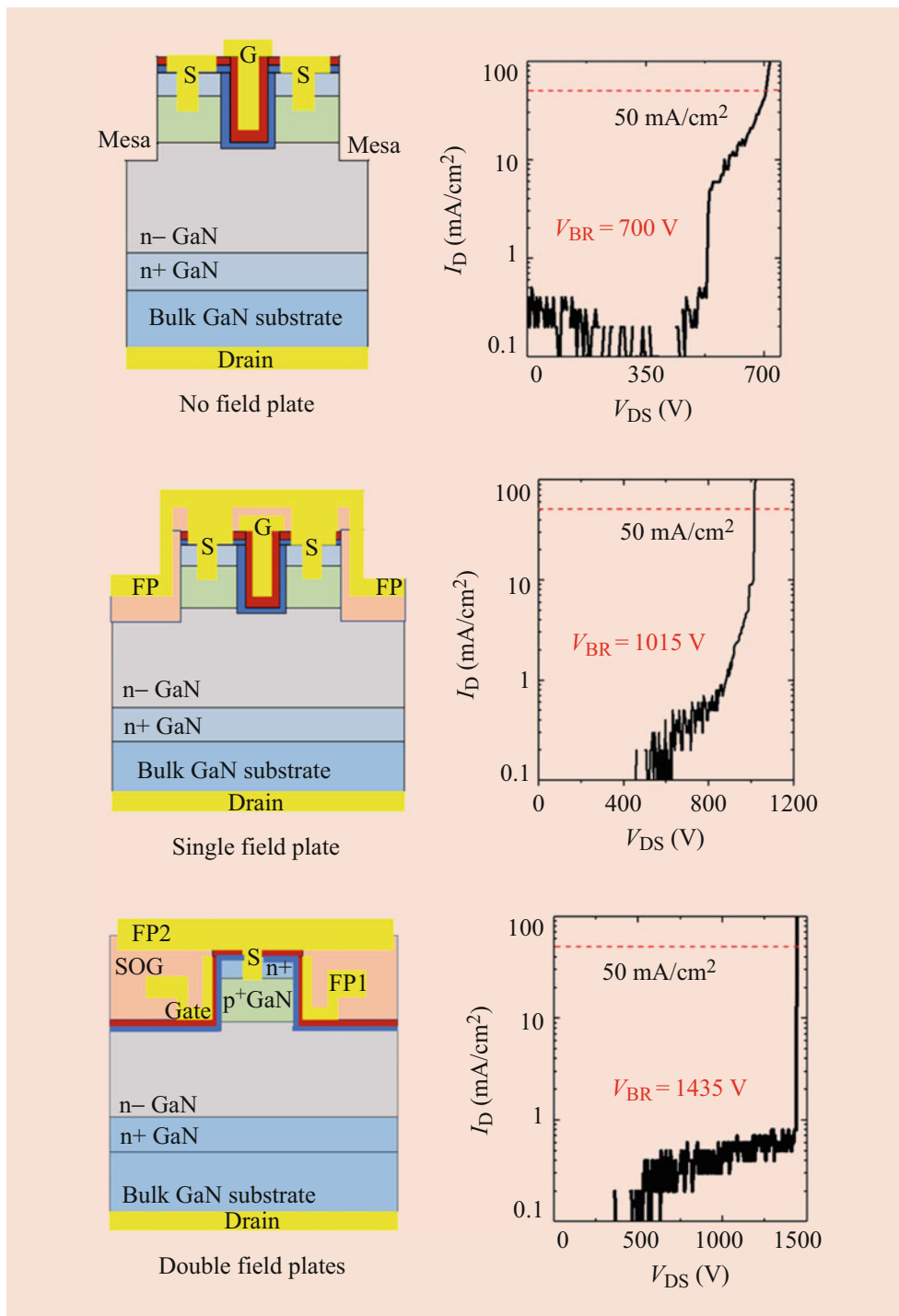


**Fig. 15.44** Off-state characteristics of the fabricated OGFETs with no field plate (mesa etch only), single field plate, and double field plates. With the help of the double-field-plate structure, a 1.4 kV breakdown

voltage was achieved [82]. (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [82])

the potential barrier height becomes lower, allowing the thermionic electrons to pass through the barrier.

SITs in GaN form a useful set of devices where without any p-type layers or any gate oxide, one can realize a transistor.

### 15.3.9 Conclusions on GaN Vertical Transistors

In this chapter, we have discussed the importance of TCAD models in GaN. We went through the details of setting up a model that gives us a scope to study devices inside a

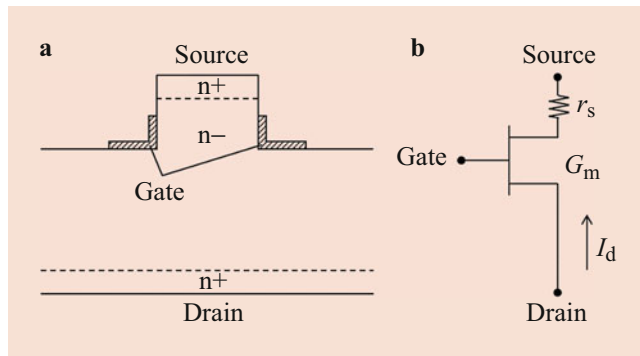


**Fig. 15.45** (a) Schematic cross-section of static induction transistor and (b) its equivalent circuit

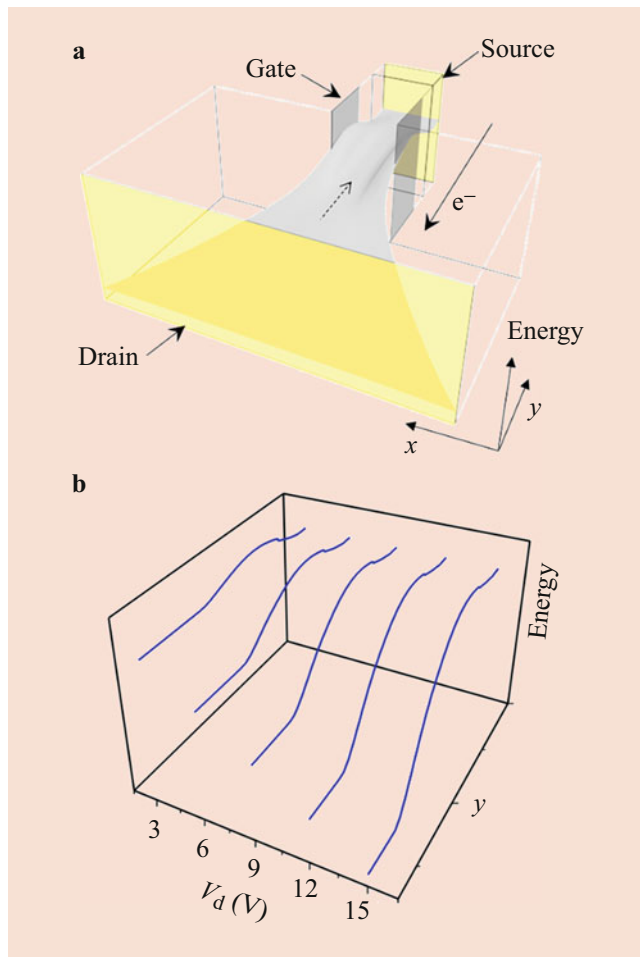


**Fig. 15.46** (a) Schematic diagram of potential distribution in SIT. (b) Dependence of the minimum barrier height, which is pointed by a dashed arrow in (a), on the drain bias

power converter application. We went through the operation principles of three important variations of vertical devices possible in GaN. CAVET, MOSFET, and SITs, discussed in this chapter, come with their unique advantages and limitations. In terms of their applications, all three flavors of

vertical device would play a significant role. In our view, a SIT is suited for 200–600 V application, a CAVET is best suited for operations up to 900 V and above 900 V, v-MOSFETs are the best candidates. Besides playing a role as a potential power electronic switch, SITs can be used for RF amplification application, making it quite versatile.

## 15.4 Parasitics and Reliability

In this section, we discuss the main parasitic mechanisms that limit the performance of GaN-based devices, with a specific focus on charge trapping. In addition, we describe the most relevant degradation processes and their impact on device characteristics and lifetime.

### 15.4.1 Charge-Trapping in GaN-Based Power HEMTs

GaN power devices have unique properties compared to conventional silicon transistors. Specifically, GaN transistors take advantage of the high mobility of the 2-dimensional electron gas and have a very low on-resistance. As an example, commercially available devices can have an on-resistance of 25 mΩ for a 60 A transistors, see [89]. In addition, the breakdown field of GaN (3.3 MV/cm) is more than 10 times higher than that of silicon, and this enables high voltage operation [90]; kV-range devices have already been demonstrated, thus clearing the way for 1200 V GaN-based technology [91]. Finally, GaN is a wide-bandgap semiconductor ( $E_g = 3.4$  eV), and for this reason devices based on GaN can be operated at high temperatures (functional operation was demonstrated up to 900 °C, see [92] for details). The fact that GaN can operate at such high temperatures and electric fields may pose significant limitations in terms of trapping and reliability. In this section, we will focus mostly on charge trapping processes, which may limit the dynamic performance of the devices.

In absence of defects, the two-dimensional electron gas of a HEMT should always have a high mobility; unfortunately, when GaN devices are fabricated, point and extended defects are inevitably incorporated in the material.

Defects in GaN may be intrinsic or extrinsic: intrinsic defects include vacancies, self-interstitials and antisites, and their presence is strongly influenced by the growth conditions. Extrinsic defects originate from impurities introduced by growth (such as carbon, hydrogen, oxygen), dopants (such as magnesium, silicon, carbon), or external contaminants. Surface defects can also play a role, especially at interfaces, in presence of a non-optimized passivation.

Several papers have been published on defects in GaN: a comprehensive list of relevant references in this field can be

found in [93]. Here we list the most common defects, along with some key publications on the topic.

- Nitrogen vacancies have been identified and studied in several GaN-based devices, with relatively shallow activation energy, in the upper half of the bandgap ( $E_C - 0.09$  eV/ $E_C - 0.27$  eV) [94–97].
- Mg-related acceptors are typically located 0.16–0.20 eV above the valence band and may be present both in GaN-based optoelectronic devices and in normally-off transistors with p-GaN gate [98].
- Nitrogen antisite defects have been detected in GaN samples and devices in the energy range between  $E_C - 0.5$  eV and  $E_C - 0.62$  eV [96, 99–103].
- Iron and iron-related defects have been investigated by Silvestri et al. and detected at  $E_C - 0.72$  eV [104, 105].
- Gallium vacancies (that have been correlated to the presence of yellow luminescence in GaN, see [106] and references therein) typically have activation energies in the range  $E_V + 0.85$ / $E_V + 0.94$  eV (see [107, 108]).
- Substitutional carbon (or carbon at nitrogen site,  $C_N$ ) has been also indicated as a source for yellow luminescence in GaN [109].  $C_N$  is typically located at  $E_V + 0.9$  eV and plays an important role in determining the electrical properties of GaN-based transistors [110].

Dislocations have been found to significantly impact on the density and concentration of deep levels in GaN-based materials and devices; recent papers have described the activation energy of defects whose concentration increases with dislocation density (see for instance [95, 111, 112]).

In a GaN power HEMT, traps may be present at several locations within the device structure and several mechanisms may lead to charge trapping. With reference to Fig. 15.48, we discuss briefly the following processes:

1. The trapping of charge in the gate stack (mechanism 1 in Fig. 15.48); this process results in a shift of threshold voltage, whose sign depends on the type of trapped carrier. Trapping of electrons induces a positive threshold voltage shift and may be particularly severe for metal-insulator-semiconductor (MIS) structures, as discussed in several recent reports (see, for instance, [113–117]). In the case of MIS structures, electrons can be trapped at high positive gate bias, being injected at the dielectric/semiconductor interface, or in the dielectric itself [116]. GaN power transistors with a p-GaN gate may also suffer from hole trapping, that leads to a negative threshold voltage shift when the devices are submitted to positive gate stress [90, 118].
2. The trapping of hot-electrons within the AlGaIn barrier or in the GaN channel/buffer layers (mechanism 2 in Fig. 15.48). This process can impact the on-resistance of the devices and worsens the performance of the transistors [119, 120].
3. The ionization of buffer traps; this process is prevalent when the devices are in the off-state, and the buffer is significantly depleted (mechanism 3 in Fig. 15.48). Ionization of buffer traps can be promoted by the injection from the silicon-substrate [10, 110, 121].
4. The injection of electrons at surface states located in the access regions (mechanism 4 in Fig. 15.48), with consequent increase in the resistivity of the access regions [122]. This effect can be mitigated through the optimization of the surface treatments and passivation.

### 15.4.2 Methods to Investigate Charge-Trapping Phenomena

In power devices, the gate-drain spacing is much longer than the gate length and the gate-source spacing. Trapping in the gate-drain access region can significantly lower the on-resistance of the devices, leading to the so-called dynamic  $R_{on}$  issue. Trapping under the gate may lead to positive- or negative-threshold bias instabilities (PBTi or NBTi). The de-trapping time-constants of known traps in GaN are in the range between 1  $\mu$ s and 100–1000 s, depending on the temperature and activation energy [93]. As a consequence, a careful optimization of the material and interface properties is needed in order to ensure that power GaN HEMTs can reach operating frequencies in the range 100 kHz–10 MHz, needed for the applications [123, 124].

Several techniques have been proposed for the investigation of trap properties in GaN-based transistors. We discuss here one of the most commonly adopted, the drain-current transient (DCT) spectroscopy, which is quite similar to current deep-level transient spectroscopy (I-DLTS). A typical schematic of the measurement setup is reported in Fig. 15.49, as presented by Bisi et al. in [125]. The gate and the drain are driven by two independent pulse generators, whose output is amplified by two power amplifiers. The devices are biased through a resistive load ( $R_{sense}$  in Fig. 15.49); the drain-source voltage ( $V_{DS}$ ) is measured through a voltage probe, while the drain current ( $I_{DS}$ ) is measured through a high voltage differential probe. Both probes are connected to an oscilloscope, controlled by a computer. Such systems can be used both on device and on wafer level, for the dynamic characterization of the transistors up to 600–1200 V. Typically, transient measurements are carried out after a double-pulsed measurement has been performed, to evaluate the total increase in dynamic  $R_{on}$  induced by trapping. The measurement sequence for DCT is as follows: the devices are first kept in a trapping bias point (e.g., in the off-state, point

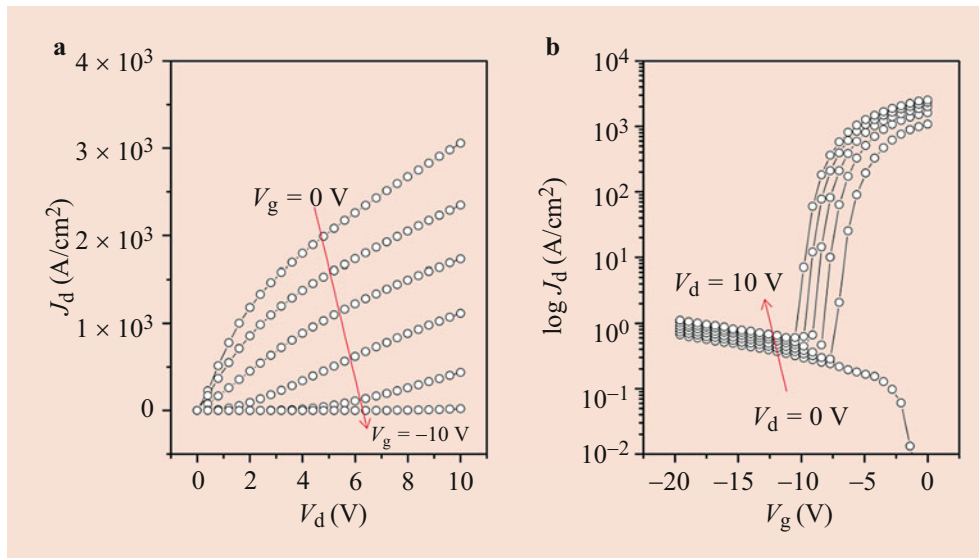


**Fig. 15.47** (a) Output characteristic of the GaN SIT. The  $V_g$  was applied from 0 to  $-10$  V in a step of  $-2$  V. (b) Corresponding semilog transfer curve. The  $V_d$  biased from 0 to 10 V in 2 V steps

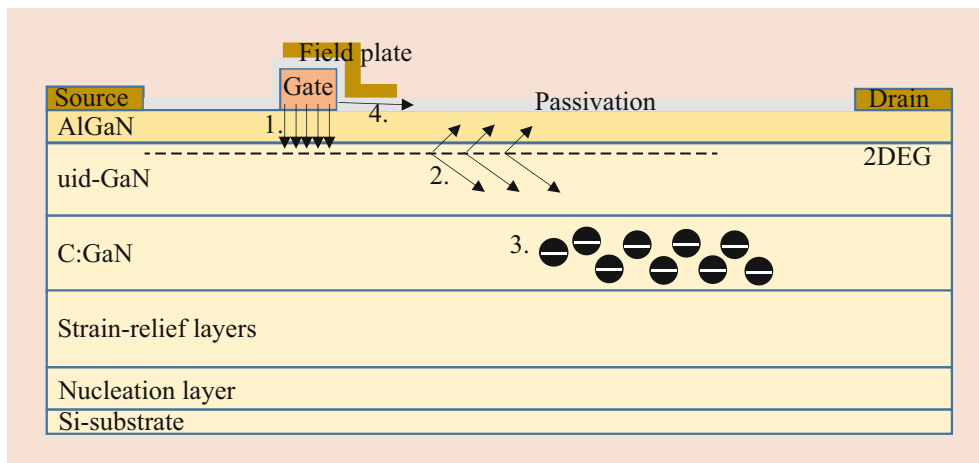


**Fig. 15.48** Schematic representation of a GaN-based power HEMT, showing different possible locations for traps and trapping processes. (1) Trapping in the gate stack; (2) injection of hot-electrons in the barrier

or in the buffer; (3) ionization of acceptors in the buffer; (4) injection of carriers at surface states

F in Fig. 15.49b), for a relatively long time (10–100 s). This ensures filling of all traps. Then, devices are turned-on, with the aim of reaching a bias point in the linear regime (point M in Fig. 15.49b). The evolution of the current transient during the turn-on phase is measured, and the changes in dynamic on-resistance are probed.

Figure 15.50 reports the results of double-pulsed measurements carried out on a GaN transistor; trapping was induced by exposing this device to off-state conditions. As can be noticed (Fig. 15.50a), increasing stress bias induced a significant increase in on-resistance. The physical properties of the traps responsible for the increase in dynamic- $R_{on}$  were extrapolated by means of  $R_{on}$ -transient measurements

(Fig. 15.50b). As can be noticed, right after turn-on the value of on-resistance is significantly higher than the reference value (at 100 s), and a gradual recovery transient is observed with increasing times from 1  $\mu$ s to 100 s. Figure 15.50c reports the derivatives of the drain-current transients with respect to logarithmic time ( $dR_{on}/\log(t)$ , DCT spectral plot). The position of the peaks of these curves are related to the time constant of the traps, while the peak height is related to trap density.

Plots like Fig. 15.50c give only a qualitative idea of the trapping and de-trapping processes and provide a visual representation of the mechanisms. A more quantitative investigation can be done by stretched- or multi-exponential

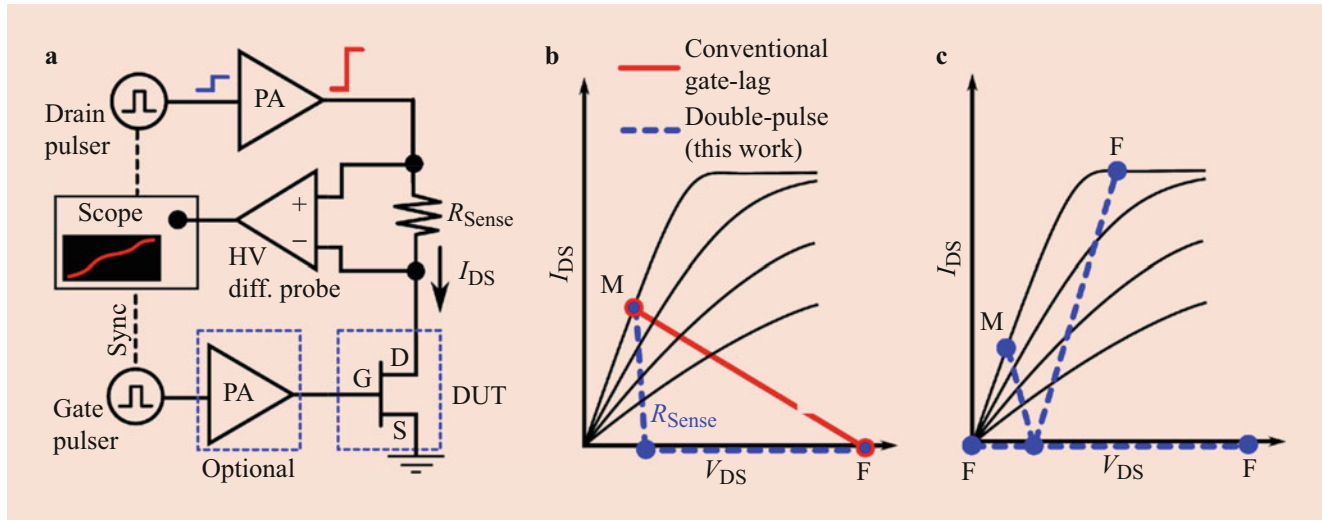


**Fig. 15.49** (a) Conceptual schematic diagram of the proposed high-voltage double-pulsed system, including the low-voltage pulse generators, the high-speed power amplifiers, the high-voltage differential probe devoted to the current probing, and the oscilloscope. (b) Comparison between the conventional fixed- $V_{DD}$  gate-lag technique and the proposed double-pulsed technique. The latter allows the releasing of

the load-line constrains and the de-coupling of Filling/Measuring (F/M) bias-pairs. (c) Examples of filling and measuring bias-points which would require negative load-resistors, achievable only with the proposed double-pulsed technique. (© 2014 IEEE. Reprinted, with permission, from [125])

fitting of the de-trapping transients, that permit to extrapolate the time-constants of the de-trapping processes [120]. In a recent paper [93], Bisi et al. presented a comprehensive comparison of three different methods for the extrapolation of time-constants from drain-current transients: (i) fitting of transients by polynomial function and subsequent extrapolation of  $\tau$  from the peaks of the derivative curves  $dR_{ON}/\log(t)$ ; (ii) the fitting of the current transients as the sum of 100 exponentials with fixed time constants and variable amplitudes; and (iii) the fitting by means of a stretched multi-exponential function

$$I_{DS}(t) = I_{DS,final} - \sum_i^N A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \quad (15.22)$$

where the fitting parameters represent the amplitude of the individual exponentials ( $A_i$ ) and the related time constant ( $\tau$ ) and stretching factors ( $\beta_i$ ) [126]. The stretching factor is introduced to take into account the non-ideality of the de-trapping processes, that can deviate from pure exponential due to (a) the presence of multiple deep levels; (b) a high density of defect states, that leads to the creation of mini-bands [127, 128]; (c) the fact that transients originate from the presence of defect states in alloys, such as AlGaN, which lead to multiple defect signatures [129]; and (d) de-trapping can be governed by non-purely thermal processes, such as hopping or tunneling [130, 131]. All the three techniques described above can provide an estimate of the time constants and be used for the extrapolation of the Arrhenius

plot of the traps. However, a recent paper [93] indicated that the time constants extrapolated by polynomial fitting and fixed-time constant exponential can be significantly different from those extrapolated by stretched exponential fitting, since several traps feature a non-purely exponential behavior. Care must be taken to identify, case by case, the most suitable technique for the study of the de-trapping transients and for the identification of the related time constants.

For GaN power devices, the de-trapping kinetics are investigated in the linear regime, i.e., with a low  $V_{DS}$  (e.g., 0.5–1 V). For this reason, the activation energy is not strongly influenced by Poole-Frenkel effects, i.e., by a field-assisted change in the de-trapping barrier. However, if de-trapping transients are measured in the saturation region, a higher field may be present, that can modify the de-trapping kinetics. For more information on the role of Poole-Frenkel phenomena one can refer to [132], that shows that in presence of electric field, the de-trapping barrier decreases by an amount  $\Delta\phi_{PF}$ , proportional to the square root of the electric field  $F$  according to

$$\Delta\phi_{PF} = \left(\frac{q^3}{\pi\epsilon}\right)^{\frac{1}{2}} \sqrt{F} = \beta\sqrt{F} \quad (15.23)$$

As a consequence, the ionization energy ( $E_i$ ) of a trap is modified with respect to the zero-field value  $E_i(0)$  according to

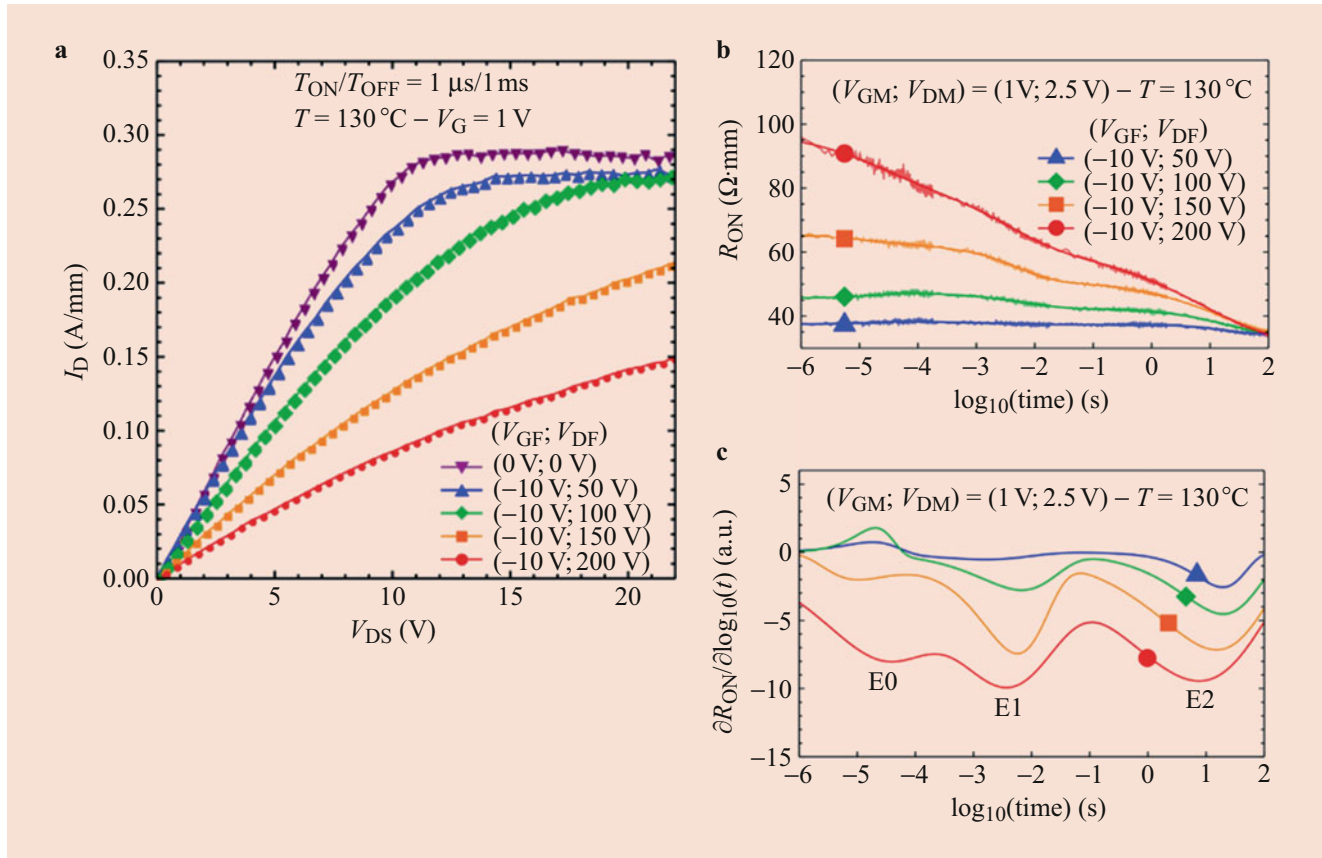


**Fig. 15.50** (a) Double-pulsed  $I_D$ - $V_D$  characterization with high-voltage off-state ( $V_{GF}$ ;  $V_{DF}$ ) quiescent-bias-points. As the quiescent drain-voltage is increased from 50 to 200 V, the device experiences a dramatic increase of the dynamic  $R_{ON}$ . (b) Time-resolved dynamic  $R_{ON}$  recovery transients, and (c) derivative of the stretched-exponential

fit-functions, employed to extrapolate the three distinct deep-levels signatures. Three dominant charge (de)trapping process can be identified. As the filling drain-voltage is increased from 50 to 200 V, the increase of peak-amplitudes, ascribed to charge-trapping magnitude, can be observed. (© 2014 IEEE. Reprinted, with permission, from [125])

$$E_i(F) = E_i(0) - \beta\sqrt{F} \quad (15.24)$$

It is worth noticing that traps located in a  $10^6$  V/cm field region can have an activation energy 0.2–0.25 eV smaller than the zero-field energy (see [132] for details).

When analyzing the de-trapping transients, one should also consider the impact of self-heating effects on the extracted activation energy: Chini et al. [133] demonstrated that if devices have a significant self-heating during the de-trapping phase, this can lead to a wrong estimation of the activation energy. By calibrating the temperature data taking into account device self-heating, one can correct the Arrhenius plots and obtain a reliable estimation of the activation energy of the traps. This requires a careful estimation of the thermal resistance of the devices, which must be done on the very same wafer prober used for the DCT analysis. A reliable on-wafer technique for such estimation was proposed by Joh et al. in [134].

### 15.4.3 Performance and Characteristics of GaN Devices and Challenges

So far we have discussed about the typical traps present in AlGaN/GaN power devices, and about the methods to investigate these traps. Now we will focus on the performance and characteristics of GaN devices.

Figure 15.51 reports the dependence of on-resistance on the trapping voltage and temperature for a GaN (lateral) power HEMT. The used measurement conditions range between 0 V and 600 V (voltage) and between  $30^\circ C$  and  $150^\circ C$  (temperature), which are consistent with real-life operation. Dynamic  $R_{on}$  has a non-monotonic trend with off-state voltage, in the whole measurement range. An explanation for this behavior can be given based on previous papers [10, 126] and on Fig. 15.51b: at low trapping voltages (<200 V), the buffer (carbon-doped) is partly depleted, thus resulting in the accumulation of negative charge. This increases dynamic-

$R_{\text{on}}$  with respect to the de-trapped conditions. In the buffer, the carbon acceptors have energy equal to  $E_V + 0.9$  eV. At higher voltages, the increase in vertical (drain-substrate) leakage leads to a re-distribution of charge within the stack. Also, band-to-band conduction may lead to the storage of positive charges at the interface with the strain-relief layer (Fig. 15.51b). As a consequence, for voltages higher than 300 V a decrease in dynamic- $R_{\text{on}}$  is observed (Fig. 15.51a). Remarkably, the value of dynamic- $R_{\text{on}}$  after stress at 600 V is almost equal to the value under rest-condition, indicating that current technologies have a negligible dynamic- $R_{\text{on}}$  increase at high voltage. The interplay between the increase and decrease in dynamic  $R_{\text{on}}$  can be affected by temperature, as shown in Fig. 15.51a.

From the discussion above, it is clear that there are two strategies to reduce the dynamic- $R_{\text{on}}$  in high-voltage GaN transistors. A first approach is to minimize the influence of carbon doping on 2DEG concentration; this can be achieved through optimization of the level of C-doping and of the thickness of the undoped GaN. A second approach is the optimization of the leakage through the unintentionally doped GaN layer; this can favor the redistribution of charge through the structure, without increasing the vertical leakage current too much. Thanks to the continuous optimization of the growth and processing parameters, it is now possible to fabricate devices with zero dynamic- $R_{\text{on}}$  both at room temperature and high temperature (see an example in Fig. 15.52, up to

600 V, 150 °C). In [126], drain current transient measurements were carried out to identify the properties of the traps responsible for dynamic- $R_{\text{on}}$ . The authors commented that activation energies in the range 0.6–0.9 eV are typically ascribed to acceptors in GaN [135, 136]. It is worth noticing that lateral and vertical charge redistribution can take place during  $R_{\text{on}}$  measurements, thus slightly changing the activation energy of defects with respect to what expected from theoretical calculations (see details in [137]).

So far, we only discussed charge trapping mechanisms induced by the off-state field. During real-life operation, GaN transistor cross also another regime which is relevant in terms of trapping, the semi-on state. Typically, semi-on conditions are reached during the switching transient, e.g., when in a boost power converter the transistor is switched from off- to on-state. During this transition, there is a short interval during which a high drain voltage and a high drain current are simultaneously present. This leads to the presence of hot-electrons, which can favor charge trapping within the structure of the devices. One strategy for investigating the impact of hot-electrons in a hard switching event is to artificially create hard switching conditions by tuning the overlap between the drain and gate waveform. In [138], Rossetto et al. investigated the impact of soft- and hard-switching conditions on the dynamic- $R_{\text{on}}$  of AlGaN/GaN power HEMTs. They used a custom setup that permits to modify the overlapping between drain and gate waveforms

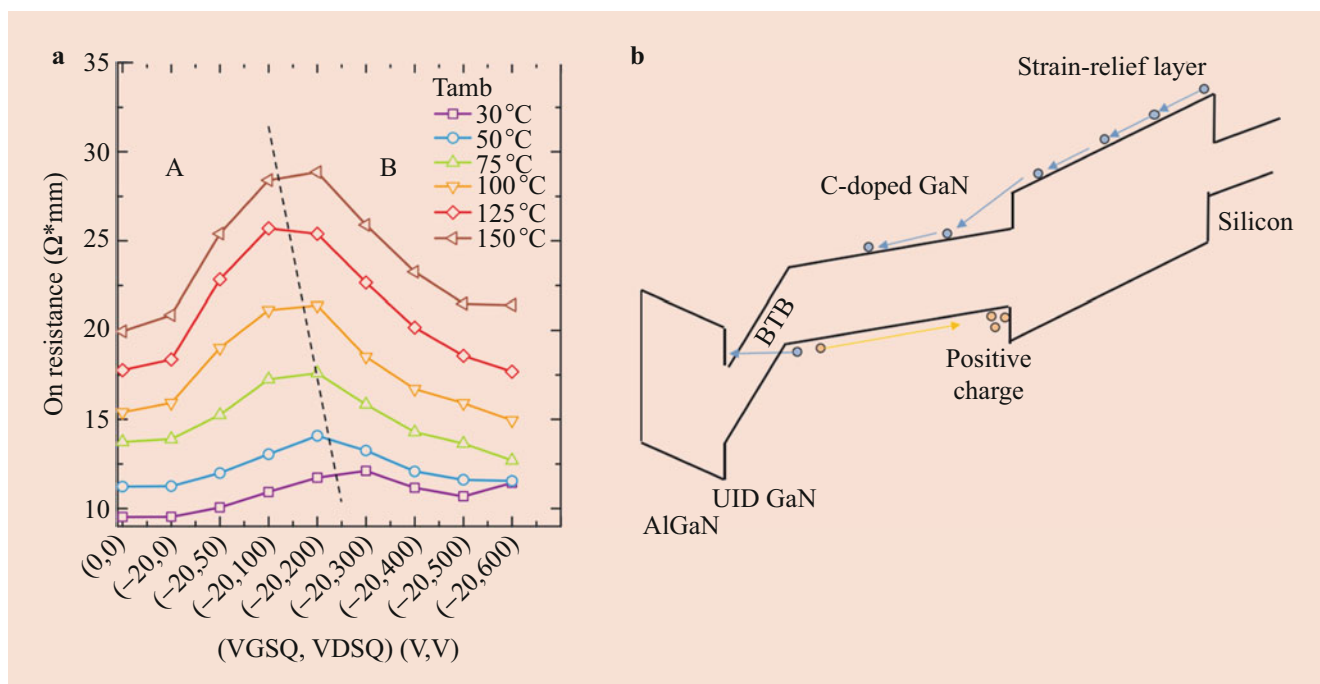


**Fig. 15.51** (a) Dependence of dynamic- $R_{\text{on}}$  (as measured from pulsed I-V measurements) on trapping voltage and temperature. (b) Schematic representation of the mechanisms responsible for non-monotonic

dynamic- $R_{\text{on}}$  as a function of trapping voltage. (Reused from [126], doi: <https://doi.org/10.1016/j.mssp.2017.10.009>, Creative Commons Attribution License (CC BY) <http://creativecommons.org/licenses/by/4.0/>)

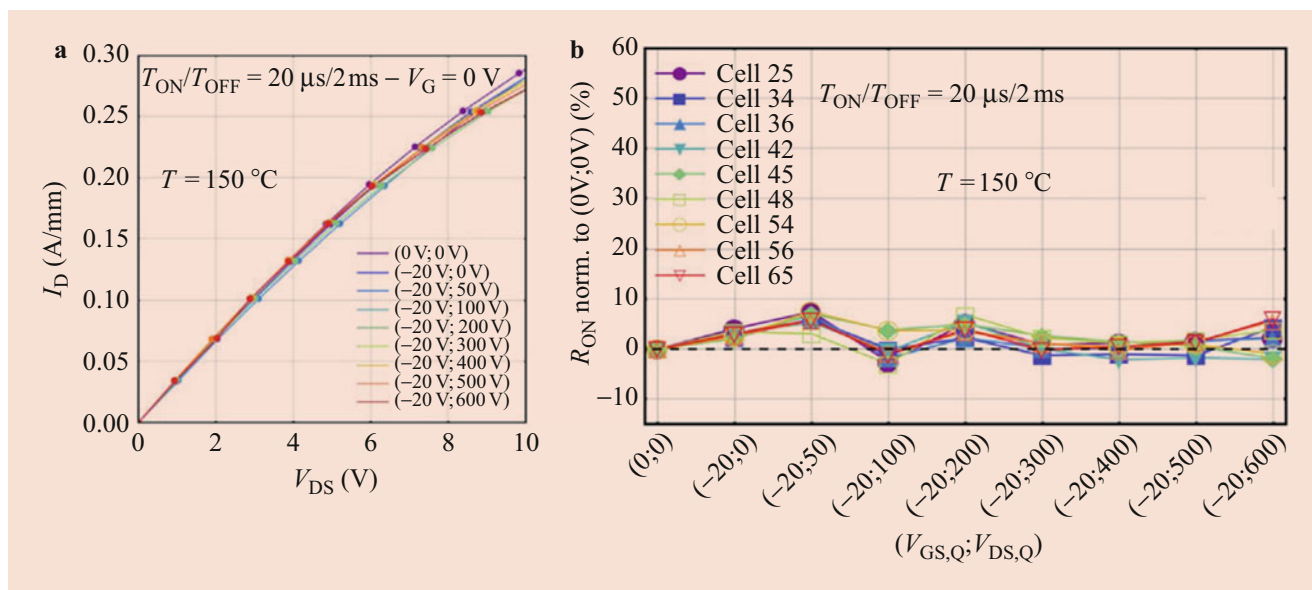


**Fig. 15.52** (a, b) Results of pulsed-IV measurements carried out on an optimized device up to  $V_{DS,Q} = 600$  V, at high temperature. The plot on (b) represents the dependence of dynamic- $R_{on}$  (normalized to the value measured with no trapping bias) on trapping voltage. Each line

refers to an individual device on the wafer. (Reused from [126], Creative Commons Attribution License (CC BY) <http://creativecommons.org/licenses/by/4.0/>)

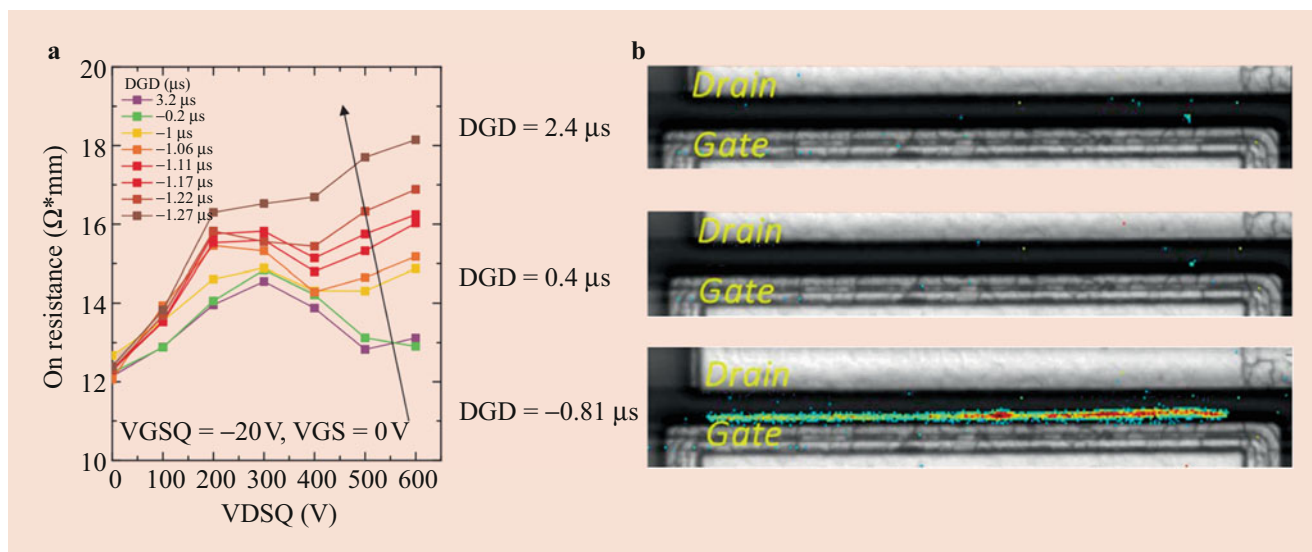


**Fig. 15.53** (a) Dependence of dynamic- $R_{on}$  on the trapping voltage  $V_{DSQ}$  and on the overlapping between the gate and drain waveforms. (b) EL patterns measured during soft and hard switching

transitions. (Reused from [126], doi: <https://doi.org/10.1016/j.mssp.2017.10.009>, Creative Commons Attribution License (CC BY) <http://creativecommons.org/licenses/by/4.0/>)

used to induce charge trapping. The results of their study demonstrated that the investigated samples have a small dynamic- $R_{on}$  up to  $V_{DS} = 600$  V in soft switching. On the other hand, a significant increase in dynamic- $R_{on}$  was observed in hard switching. A representation of this phenomenon is reported in Fig. 15.53a, which shows that the dynamic- $R_{on}$  vs off-state voltage curves change as a function of the parameter DGD (drain-gate delay). This parameter represents the time interval between a drain voltage equal to

$V_{DSQ}/2$  and a gate level equal to the threshold voltage  $V_{TH}$ . Therefore DGD is positive for soft-switching transitions and negative for hard-switching transitions. As can be noticed, for  $DGD < 0$  (hard switching) the dynamic- $R_{on}$  is significantly enhanced compared to soft-switching ( $DGD > 0$ ). The hard switching intervals reached in Fig. 15.53a ( $\mu\text{s}$  range) are significantly longer than in real-life operation (where a slew rate of 10–100 V/ns is more realistic), thus corresponding to an extremely stressful scenario.

The increased dynamic- $R_{on}$  measured in hard switching conditions is ascribed to the trapping of hot-electrons within the devices. A confirmation of the presence of hot-electrons was obtained by means of electroluminescence measurements (Fig. 15.53b). No EL signal was measured in soft switching, since no current flows through the devices during the switching transition. On the contrary, under hard switching conditions, EL signal was detected on the whole channel width, with a peak on the drain-side gate edge.

A further mechanism of charge trapping is related to the gate stack; in several cases,  $V_{th}$  instabilities have been reported for GaN-based power transistors, causing negative- or positive-threshold bias instability (NBTI or PBTI). The physical origin of such  $V_{th}$  shifts are strongly dependent on the gate architectures (e.g., metal-insulator semiconductor, Schottky-gate, p-type gate, etc.).

In MIS-transistors [113–117], threshold voltage instabilities are due to the trapping of electrons at the interface between dielectric and semiconductor or to the injection of charge inside the dielectric [116].

More recent papers indicated that also normally-off GaN power transistors can suffer from threshold voltage instabilities [90, 118, 139, 140]; different mechanisms have been indicated as responsible for the positive and negative threshold voltage instabilities in GaN-based transistors with p-type gate. In [140], the authors suggested that a positive threshold voltage shift may be detected after stressing the devices at  $V_{GS} = 1$  V (see Fig. 15.54a, b). This  $V_{th}$  variation

was ascribed to the injection of electrons from the 2DEG to the AlGaIn barrier, which may occur once the 2DEG has been formed (see Fig. 15.54c). For higher voltages, the accumulation of positive charges (holes) in the AlGaIn barrier and/or at the passivation/AlGaIn interface can induce a negative shift in threshold voltage (Fig. 15.54). Another paper [139] investigated the role of hole accumulation in the p-GaN (causing a negative threshold voltage shift) and hole depletion in the p-GaN (causing a positive threshold voltage shift). This chapter indicated that an unbalance between the hole tunneling current through the Schottky barrier and the thermionic emission on the AlGaIn barrier can significantly change the total charge in the p-GaN, thus resulting in  $V_{th}$  shift.

Finally, one of the latest trends in GaN technology is the development of vertical transistors. In several cases, an MOS approach is used, in order to ensure a high robustness and a good threshold current. Recently, only few papers on the stability and reliability of GaN-on-GaN vertical devices have been published [141–144]. As an example, we refer here to the results presented in [144]. In this paper, the authors investigated the stability of the threshold voltage of GaN-on-GaN vertical fin field-effect transistors (VFETs). The results of threshold voltage transients indicated the existence of two different trapping processes (Fig. 15.55a). At low voltages, a negative shift in threshold voltage was observed; this effect was ascribed to the de-trapping of electrons from the  $Al_2O_3$  insulator, induced by a low positive bias. At high voltages

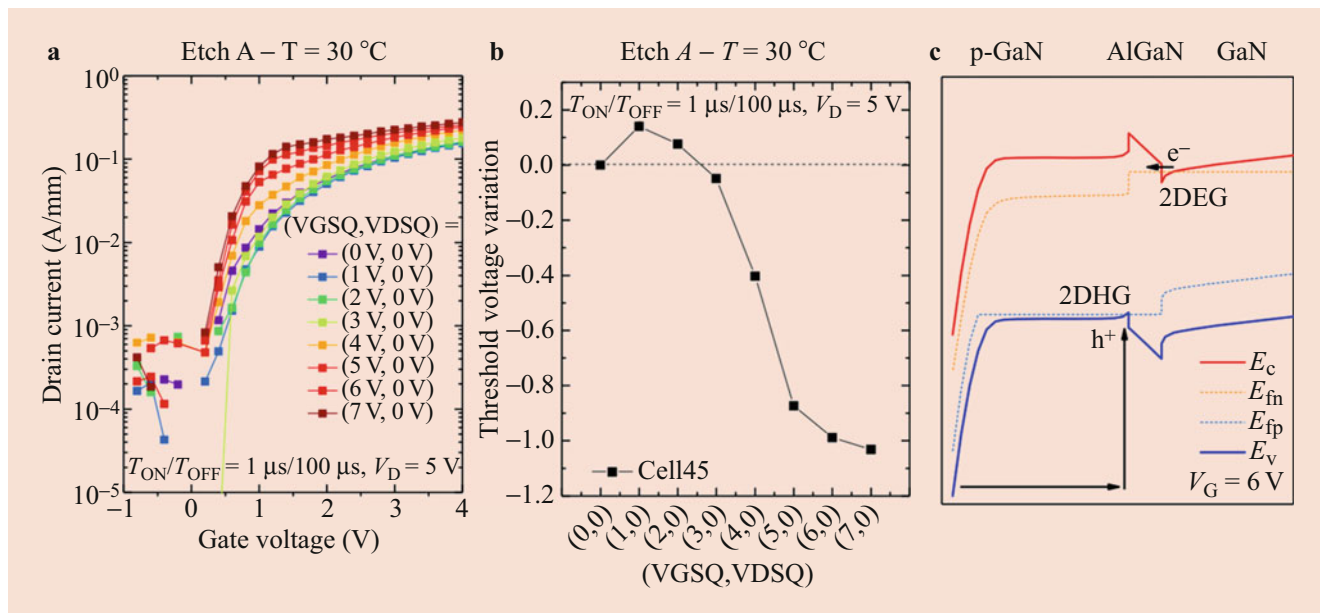


**Fig. 15.54** (a) drain current versus gate voltage after different forward gate voltage stress; (b) pinch-off voltage variation versus forward gate voltage stress; (c) band diagram under the region at  $V_G = 6$  V (simulated with Sentaurus provided by Synopsis). Two mechanisms are reported:

(1) injection of electrons from the 2DEG towards the AlGaIn barrier; (2) accumulation of positive charges (holes), injected from the gate. (Reprinted from [140] Copyright 2018, with permission from Elsevier)

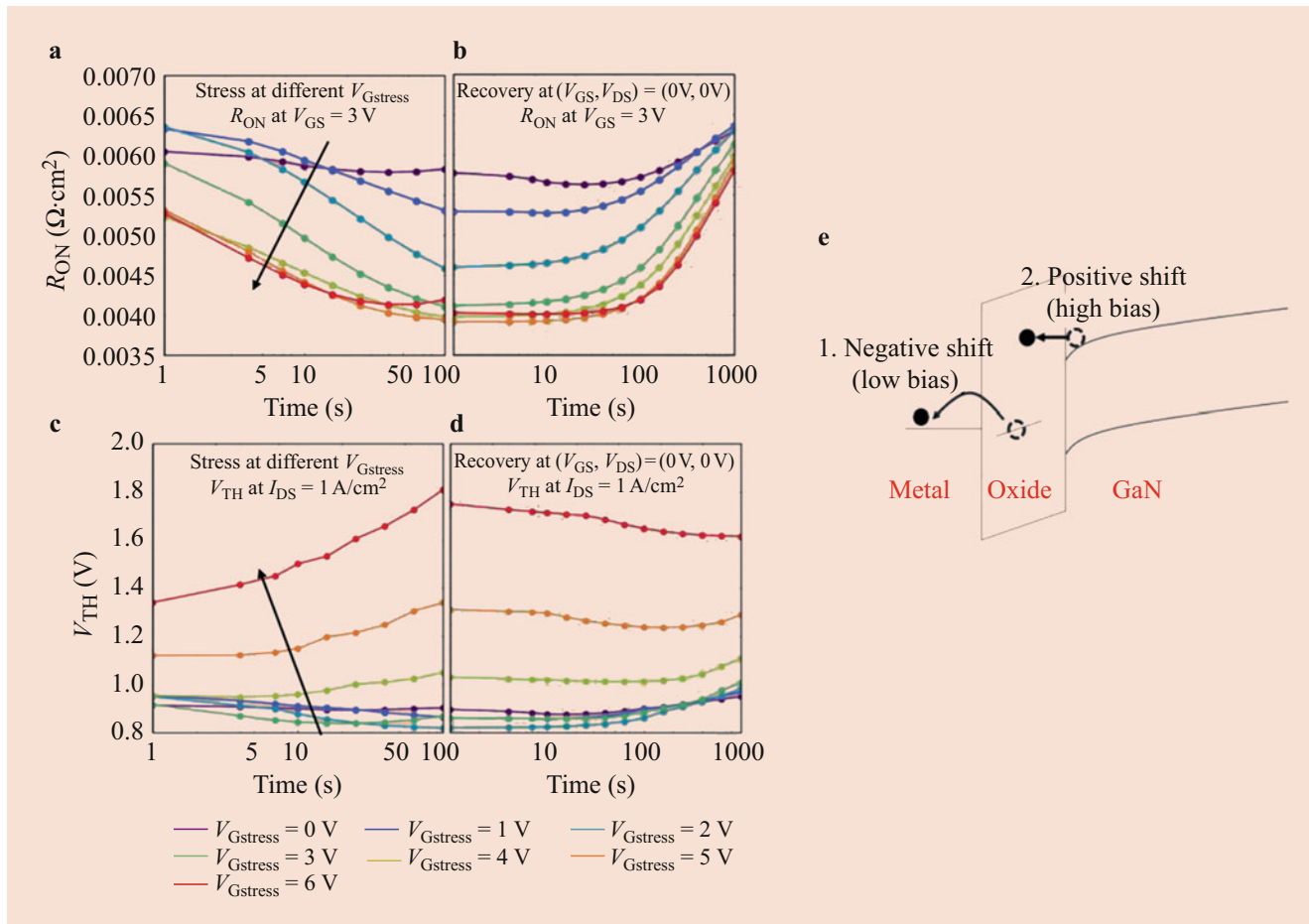


**Fig. 15.55** (a, b) On-resistance and (c, d) threshold voltage variation during 100 s of (a), (c) stress at different  $V_{Gstress}$  and 1000 s of (b), (d) recovery (all terminals at zero voltage) at  $T_{amb} = 25^\circ\text{C}$ . The  $R_{ON}$  decrease is a recoverable process. At low stress voltages ( $V_{GS} < 2$  V) a negative recoverable  $\Delta V_{TH}$  is observed; for high stress voltages

( $V_{Gstress} > 2$  V) a positive  $\Delta V_{TH}$  is induced, not recoverable in 1000 s. (e) Schematic representation of the two mechanisms responsible for (1) negative and (2) positive threshold voltage shift. The two mechanisms take place at low and high stress voltage, respectively. (© 2017 IEEE. Reprinted, with permission, from [144])

( $\geq 5$  V), a substantial positive threshold voltage shift was observed. This process is due to the injection of electrons from the channel to the insulator. The recovery of this second process was found to be slow. A schematic representation of the two processes is given in Fig. 15.55b; see [144] for details.

#### 15.4.4 Reliability Issues of GaN-Based Power HEMTs

Thanks to the unique material properties of GaN, AlGaN/GaN transistors may be subject to extremely high stress conditions during operation. GaN devices are currently targeting the 600–650 V market segment [89], but research is ongoing to extend to 1200 V and beyond. Current levels can be higher than 50 A on a single component, while – at least for the moment – specifications are quite relaxed for the maximum junction temperature (see, for instance, [89,

145] showing a maximum  $T_j = 150^\circ\text{C}$ ). For E-mode devices, also the maximum gate voltage/current are critical in terms of reliability. In some cases, the maximum gate-to-source voltage is specified in the datasheet (see, for instance, [89], indicating a limit of +7 V), while in some other cases the maximum gate leakage current is defined (see for instance [145], indicating a maximum gate current of 50 mA). Finally, during a switching event GaN power transistors can reach high levels of instantaneous power dissipation; for a representative example, the reader may refer to the results reported by Bahl et al. in [146], showing that in a boost converter, a significant current/voltage overlap is observed during the turn-on phase; peak currents around 15 A were observed when switching from 400 V, resulting in high power densities and hot carrier effects.

Studying the reliability of GaN transistors is a necessary step for the development of this technology. In this section, we describe the most common failure mechanisms that limit

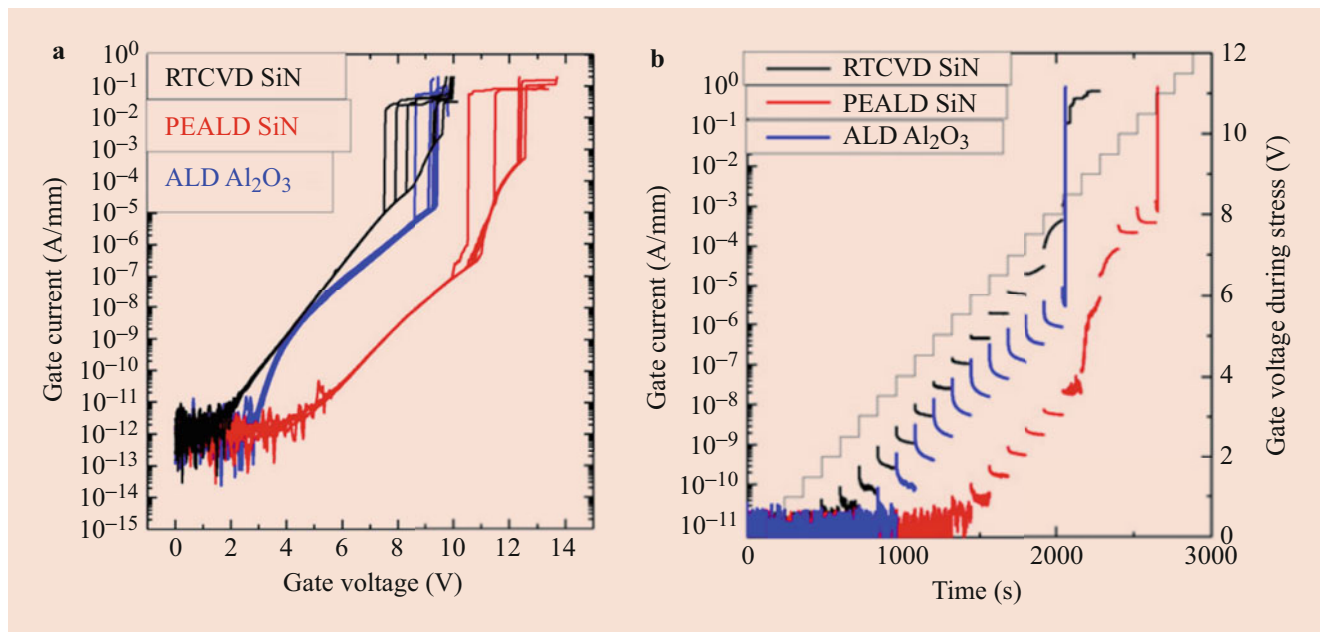


**Fig. 15.56** (a) Current-voltage breakdown measurements on devices with different gate insulators: RTCVD SiN (black line); PEALD SiN (red line); and ALD Al<sub>2</sub>O<sub>3</sub> (blue line). (b) Gate current monitored during step stress with drain and source terminals grounded ( $V_D = V_S = 0$  V) and increasing  $V_G$  in devices with different gate

insulators: RTCVD SiN (black solid line), PEALD SiN (red solid line), and ALD Al<sub>2</sub>O<sub>3</sub> (blue solid line). Corresponding gate voltage applied during the step stress is reported with a staircase curve. (Reprinted from [147], Copyright 2015, with permission from Elsevier)

the reliability of GaN power devices, along with a description of the related root causes.

#### 15.4.5 Gate-Stack Reliability

As discussed above, the two most studied technologies for the fabrication of the gate are metal-insulator-semiconductor (MIS) and p-GaN gate. The threshold voltages of commercial GaN HEMTs are around 1.1–1.3 V [89, 145], and a certain overdrive is required. For instance, the datasheet of [89] indicates a gate drive range from 0 V to 6 V. For this reason, it is important to evaluate the stability and reliability of GaN transistors at high positive gate voltage and to define proper ways to extrapolate acceleration factors and lifetime.

For insulated-gate devices, the time-dependent failure of the gate dielectric is one of the most relevant degradation process. This mechanism is similar to what has been detected and studied in silicon devices and leads to a catastrophic failure of the gate when a prolonged high-voltage stress is applied to the samples.

As a representative example, we refer here to the case of partially recessed GaN HEMTs with insulated gate. In [147], Meneghesso et al. studied the breakdown voltage of three different wafers of transistors with a residual AlGaN thickness of 3.7 nm, having three different gate insulators:

a 15 nm SiN layer deposited by rapid thermal chemical vapor deposition (RTCVD); a 15 nm SiN layer deposited by plasma-enhanced atomic layer deposition (PEALD); and a 15 nm Al<sub>2</sub>O<sub>3</sub> layer, deposited by atomic layer deposition (ALD). The results of this study indicated that devices with PEALD-SiN insulator have a leakage more than three orders of magnitude lower than the two other wafers (Fig. 15.56a). In addition, devices with PEALD-deposited SiN were found to have a higher robustness at positive gate voltage (average failure voltage = 11.9 V), compared to RTCVD-SiN and Al<sub>2</sub>O<sub>3</sub> (8.65 V and 9.25 V, respectively).

The breakdown voltage evaluated by a simple dc sweep is not fully representative of the real device robustness under long-term stress; typically, step-stress experiments and constant-voltage stress tests are carried out with the aim of analyzing the failure distributions and the related statistics. Figure 15.56b reports the results of a step-stress experiment carried out on one device per wafer; gate voltage was increased by 0.5 V every 120 s, while monitoring the electrical parameters. For positive stress voltages (and above threshold), the 2DEG is fully formed, and a high electric field builds across the residual AlGaN layer and the gate insulator. Such field is rather uniform, since the metal and the 2DEG act as the two plates of a capacitor. As can be noticed, the properties and quality of the dielectric strongly influence the overall reliability of the devices. In addition, the samples with

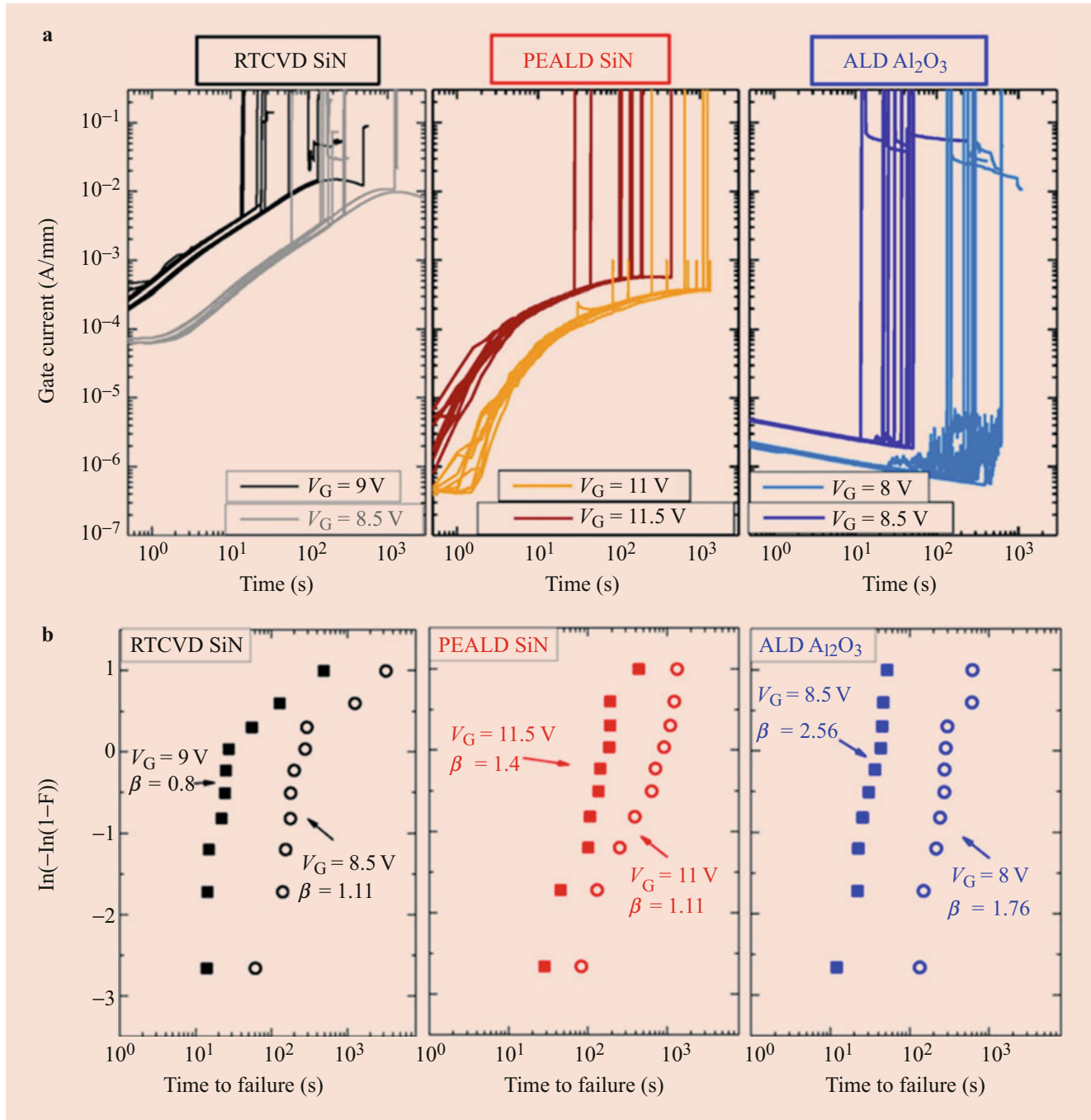


**Fig. 15.57** (a) TDDDB measurements performed on devices with different insulating layers: RTCVD SiN (black line), PEALD SiN (red line), and ALD Al<sub>2</sub>O<sub>3</sub> (blue line). (b) Weibull plot on devices with different

insulating layers: RTCVD SiN (black line), PEALD SiN (red line), and ALD Al<sub>2</sub>O<sub>3</sub> (blue line). (Reprinted from [147], Copyright 2015, with permission from Elsevier)

PEALD SiN and RTCVD SiN show a sudden increase in gate leakage at the end of the stress experiment.

Representative results on the effect of constant-voltage stress on the gate leakage of insulated-gate HEMTs are shown in Fig. 15.57. In Fig. 15.57a, we report the variation of gate leakage during a constant voltage stress (ten devices

per stress condition, two voltages per insulating material). As expected, by increasing stress voltage a decrease in time-to-failure is observed. Time-to-failure is generally Weibull-distributed (see the Weibull plots in Fig. 15.57). In the example reported in Fig. 15.57b, the shape parameter  $\beta$  does not strongly depend on stress voltage and is around 1.1–1.5, i.e.,

indicative of intrinsic failure. A more detailed analysis of the failure of MIS-HEMTs and related TDDb was given by Wu et al. in [148]. The authors of this chapter demonstrated that the Weibull distribution scales with gate width, confirming the hypothesis on intrinsic failure. In addition, they extrapolated the lifetime to 0.01% of failures at 150 °C, 20 years ( $W_g = 36 \text{ mm}$ ), giving voltages of 4.9 V (power law) or 7.2 V (exponential law).

In a recent paper [149], Warnock and del Alamo discussed the physical origin of progressive breakdown (PBD) in high-voltage GaN-based MIS-HEMTs. They observed PBD, characterized by a rapid increase in gate leakage noise, taking place before hard breakdown. They indicated that the degradation does not take place at the AlGaIn/GaN interface. Their results were found to be consistent with those obtained on silicon MOSFETs [150], supporting the percolation model to explain PBD and hard breakdown.

The time-dependent breakdown of dielectrics can be critical also for vertical GaN devices. Several vertical transistor structures have been recently proposed: the current aperture vertical electron transistor (CAVET) [71], which is based on the use of a current-blocking layer, used to stop vertical current flow through any path other than the aperture to the drain; the V-MOSFET or trench-MOSFET (also modified in the recent OG-FET layout) [81], where a buried p-type GaN layer is used to increase the threshold voltage of the devices; and the vertical fin power-FET [151] and vertical nanowire-FET [152], where current flow is accurately controlled through the use of nanometer-size channels. In most cases, a dielectric is placed under the gate; this dielectric layer can be exposed to high electric fields, especially when the devices are in on-state.

An example of this has been presented by Ruzzarin et al. in [143]. The authors of this paper studied the stability and degradation of vertical fin power-FETs submitted to positive gate stress. The analyzed devices have a vertical metal/insulator/semiconductor layout, where the semiconductor is *n*-type. When submitted to positive gate stress, an accumulation layer is formed in the semiconductor, at the interface with the dielectric. At high gate bias ( $>7 \text{ V}$ ), the field in the 15 nm dielectric becomes high and can favor a time-dependent breakdown of the oxide. Specifically, a soft failure was observed at a stress voltage equal to  $V_{\text{Gstress}} = 7.25 \text{ V}$  (corresponding to an abrupt increase in gate leakage, Fig. 15.58). A catastrophic failure was detected at  $V_{\text{Gstress}} = 8.75 \text{ V}$  ( $\sim 6 \text{ MV/cm}$  in the gate insulator,  $\text{Al}_2\text{O}_3$ ).

Results of simulations (Fig. 15.59) indicated that in vertical fin power-FET at high drain voltage the electric field peaks at the corner of the dielectric. This is supposed to be the region where failure takes place at high drain bias, in the off-state. Strategies for reducing the field in the material

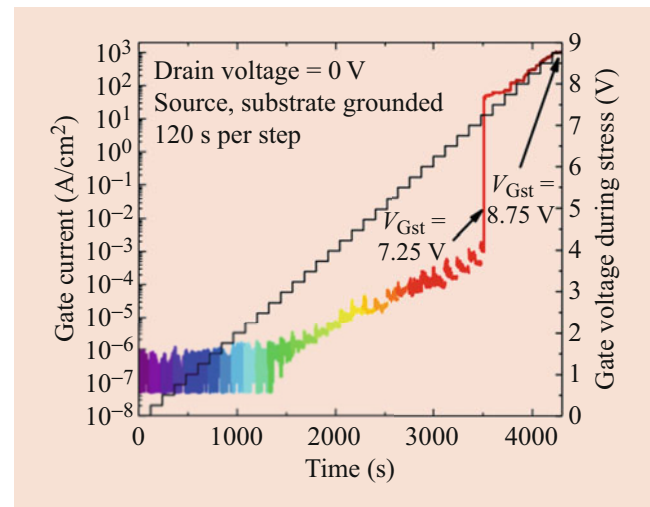


**Fig. 15.58** Step stress performed with  $V_{\text{Dstress}} = 0 \text{ V}$  and by increasing the  $V_{\text{Gstress}}$  by 0.25 V each 120 s of stress. A positive gate stress induces a permanent increase in gate current, for stress voltages higher than 7.25 V, due to the breakdown of the gate dielectric. The catastrophic failure occurs at  $V_{\text{Gstress}} = 8.75 \text{ V}$ . (© 2018 IEEE. Reprinted, with permission, from [143])

can be adopted to significantly improve the robustness of the transistors at high drain bias.

For devices with p-GaN gate, different degradation mechanisms have been proposed over the past years. The metal/p-GaN interface can be either Ohmic or Schottky [153]. The second approach allows to substantially reduce the leakage at the gate. When a Schottky junction is created on p-GaN, the resulting stack can be modeled as the back-to-back combination of two diodes. The first results from the metal/p-GaN Schottky junction, and the second is represented by the p-GaN/i-AlGaIn interface [154]. Wu et al. [155] analyzed the forward-bias breakdown mechanisms in Schottky metal/p-GaN gate HEMTs. They demonstrated a positive temperature dependency of the gate breakdown voltage, with a coefficient equal to  $5 \times 10^{-3} \text{ C/V}$ . They demonstrated that – on average – the breakdown voltage at 200 °C is 1 V higher than at 25 °C. They explained this positive temperature dependence by considering the avalanche multiplication in the space charge region that is present at the metal/p-GaN junction. The electrons can transfer to the p-GaN and be accelerated by the high field in the depleted region. Further, they were able to observe the presence of avalanche luminescence, suggesting that high gate voltages may lead to the generation of electron-hole pairs.

Tapajna et al. [156] analyzed the effect of forward stress on normally-off p-GaN/AlGaIn/GaN HEMTs. They indicated that the time-dependence of the gate current increase is consistent with percolation process. By using the Weibull statistics, they estimated the maximum gate voltage

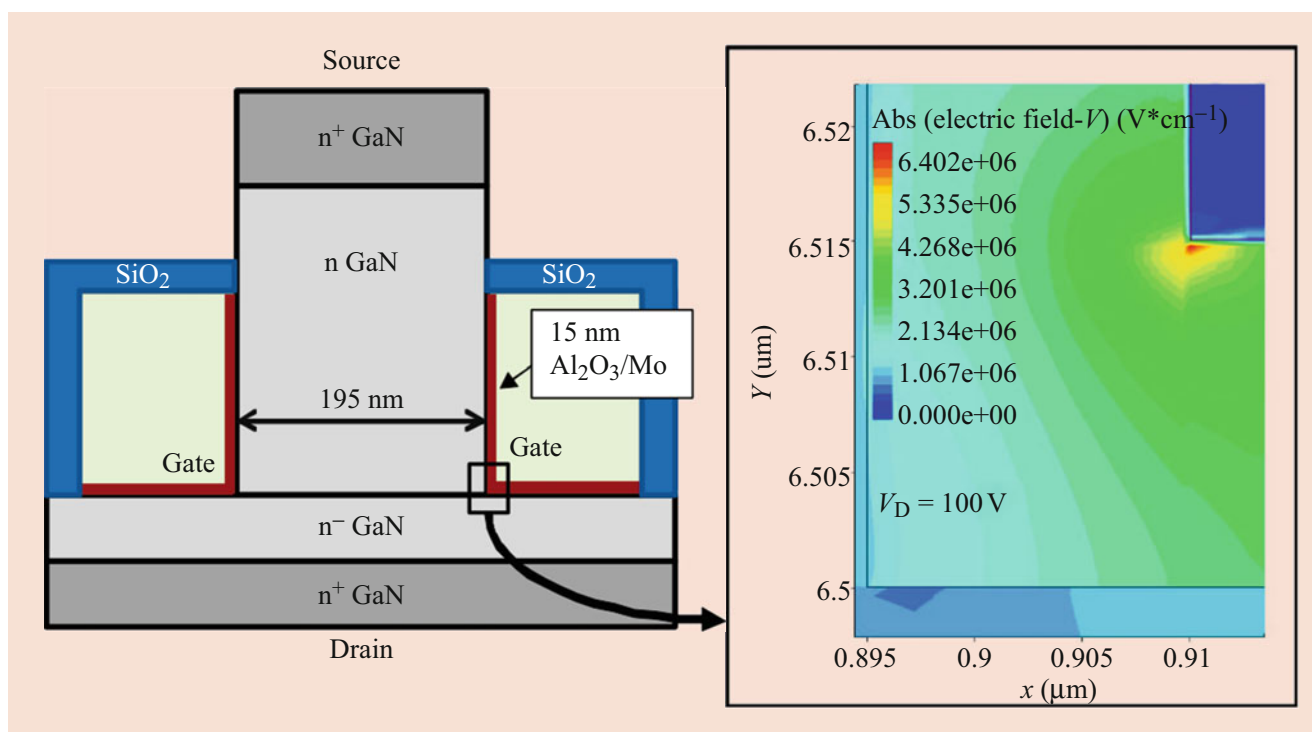


**Fig. 15.59** Simulation of the electric field at the dielectric/GaN channel interface at higher drain voltages (in the real device the fin corners are not exactly  $90^\circ$  corners). (© 2018 IEEE. Reprinted, with permission, from [143])

for long-term operation. In addition, they demonstrated that the observed degradation process has a low activation energy.

Tallarico et al. [154] demonstrated that the time-to-failure of GaN-on-Si power HEMTs with p-type gate follows a Weibull distribution. Also, they suggested that the time-to-failure is a function of the initial gate leakage, with higher gate leakage corresponding to a shorter lifetime. They suggested that breakdown is related to the creation of a percolation path in the p-GaN layer.

Rossetto et al. [153] analyzed the influence of the Mg doping concentration on the robustness of AlGaIn/GaN HEMTs at positive gate overstress. They proposed a method to separately investigate two different processes, namely, (a) a field-driven breakdown of the metal/p-GaN Schottky junction, induced by TLP test with short pulses. High Mg doping correspond to higher junction fields, thus resulting in lower failure voltages. (b) A current-driven process detected during long-term stress, ascribed to the accumulation of charge at the p-GaN/AlGaIn interface [157]. For this process, an increase in Mg doping was found to improve the stability.

In a more recent paper, Masin et al. [158] demonstrated that GaN-HEMTs with p-GaN gate can show a time-to-failure with positive temperature coefficient, when submitted to positive gate stress. They ascribed degradation to the accumulation of holes at the p-GaN/AlGaIn interface. This

is supposed to increase the injection of electrons from 2DEG to p-GaN, which are then accelerated by the electric field. This eventually leads to defect generation and breakdown.

#### 15.4.6 Off-State Reliability

Another relevant regime where GaN transistors can undergo significant stress is off-state bias, i.e., (for e-mode devices) a null gate voltage and a high (up to 600–650 V) drain voltage. Recent papers have investigated the impact of high off-state bias on the electrical characteristics of GaN transistors (see, e.g., [159–165]). Under off-state conditions, two main factors can promote the degradation of the devices. First, the high lateral field, between gate and drain, can promote a failure of the devices in proximity of the top epitaxial and/or passivation layers. In this case, we refer to “lateral breakdown,” since the mechanism originates from the lateral field. Second, in off-state conditions a high bias is present also between drain and substrate. This creates a significant vertical field, which may lead to the “vertical breakdown” of the epitaxial stack.

An example of lateral breakdown was reported in [161–163]. Here the authors demonstrated the existence of time-dependent dielectric breakdown in GaN-based high electron mobility transistors (HEMTs) submitted to stress in off-state bias. Specifically, they demonstrated that under off-state

stress at 600–700 V the devices can show a time-dependent failure, which was ascribed to the failure of the SiN dielectric at the edge of the gate overhang, on the drain side. A representative example of this failure process is shown in Fig. 15.60a: the variation of drain current during stress in off-state with  $V_{DS} = 600$  V is reported on ten identical samples. All the analyzed devices reached a catastrophic failure, i.e., a sudden increase in drain current. Time-to-failure (TTF) was found to have an exponential dependence on stress bias.

This was explained by considering the existence of a field-dependent degradation process. In addition, TTF was found to be Weibull-distributed (see, for instance, Fig. 15.60b), with a  $\beta$  around 0.5. Such a value is indicative of an extrinsic failure mechanism. Degradation was then ascribed to the time-dependent breakdown of the dielectric under the gate overhang. Numerical simulations were carried out to support this hypothesis. As shown in Fig. 15.61, the electric field in the nitride peaks at the edge of the gate overhang

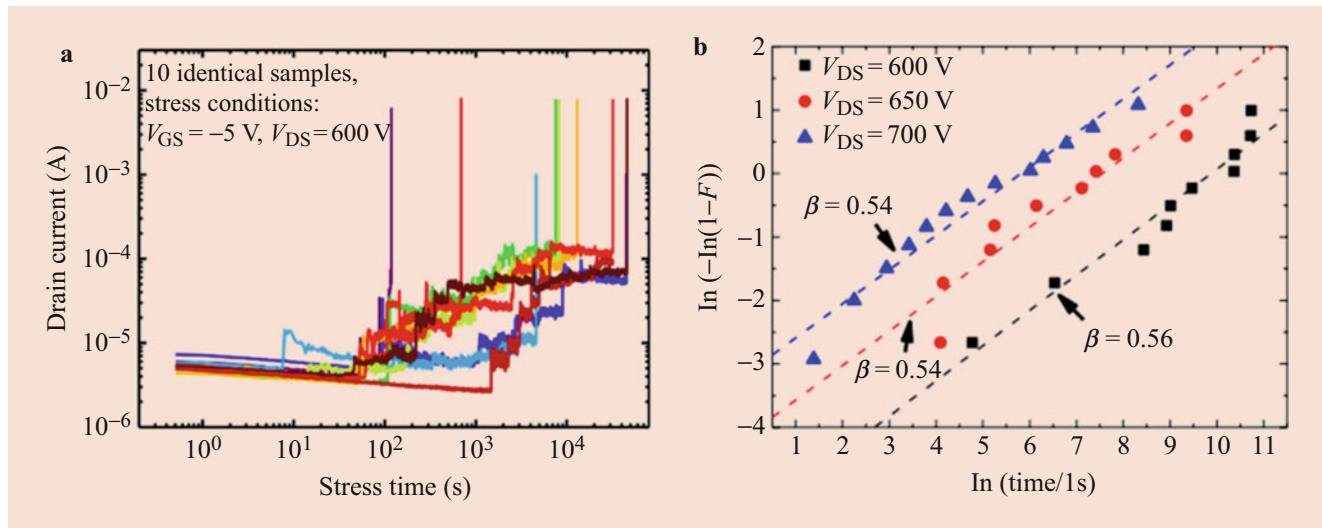


**Fig. 15.60** (a) Results of constant voltage stress experiments carried out on a set of ten identical devices; the stress conditions are  $V_{GS} = -5$  V,  $V_{DS} = 600$  V. Only drain current is reported for

clarity. (b) Weibull-distribution for three sets of devices stressed with  $V_{GS} = -5$  V, and increasing  $V_{DS}$  (600, 650, and 700 V). (© 2015 IEEE. Reprinted, with permission, from [163])

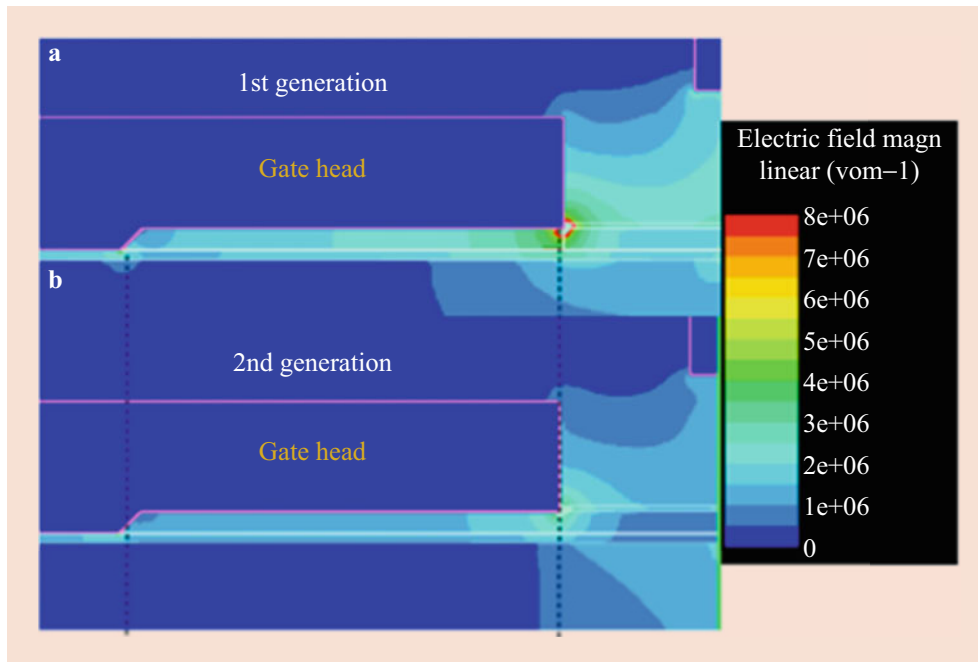


**Fig. 15.61** (a) Simulated electric field distribution close to the gate edge for a device of Gen-1. (b) Simulated electric field distribution close to the gate edge for a device of Gen-2. (© 2015 IEEE. Reprinted, with permission, from [163])

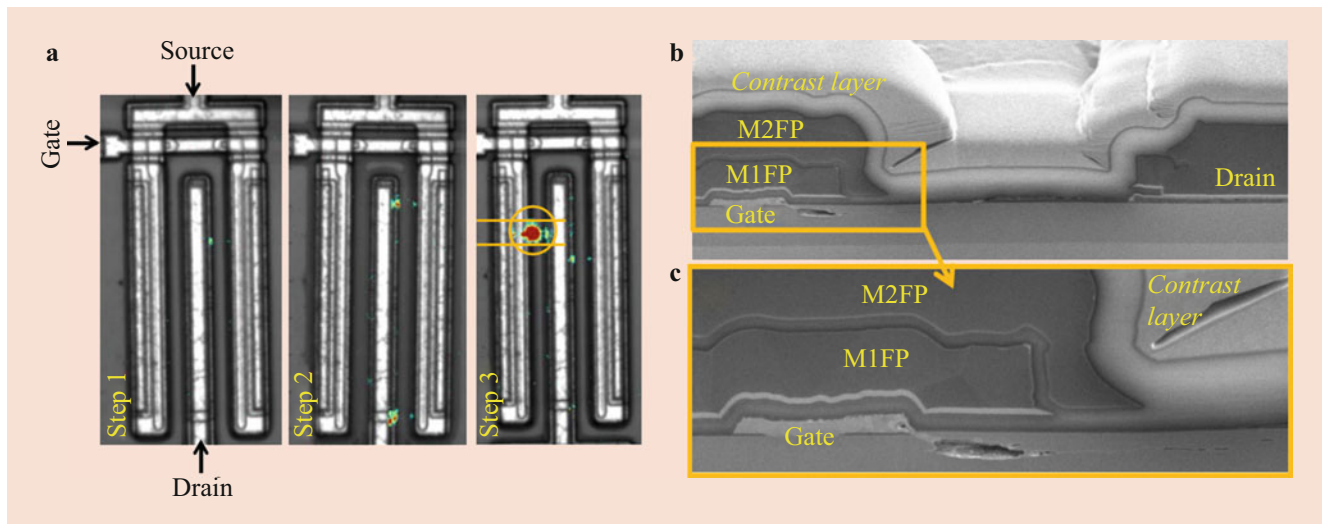


**Fig. 15.62** (a) Emission microscopy evaluated during stress with  $V_{GS} = -5$  V and  $V_{DS} = 600$  V. The three frames are referred to increasing stress times. The portion cut for the TEM evaluation is highlighted in yellow. (b) TEM performed on a cross section corresponding to the

hot spot indicated in (a), after the constant voltage test, showing a severe degradation in the gate side/edge. (c) Enlargement of the damaged portion of the device. (© 2017 IEEE. Reprinted, with permission, from [161])

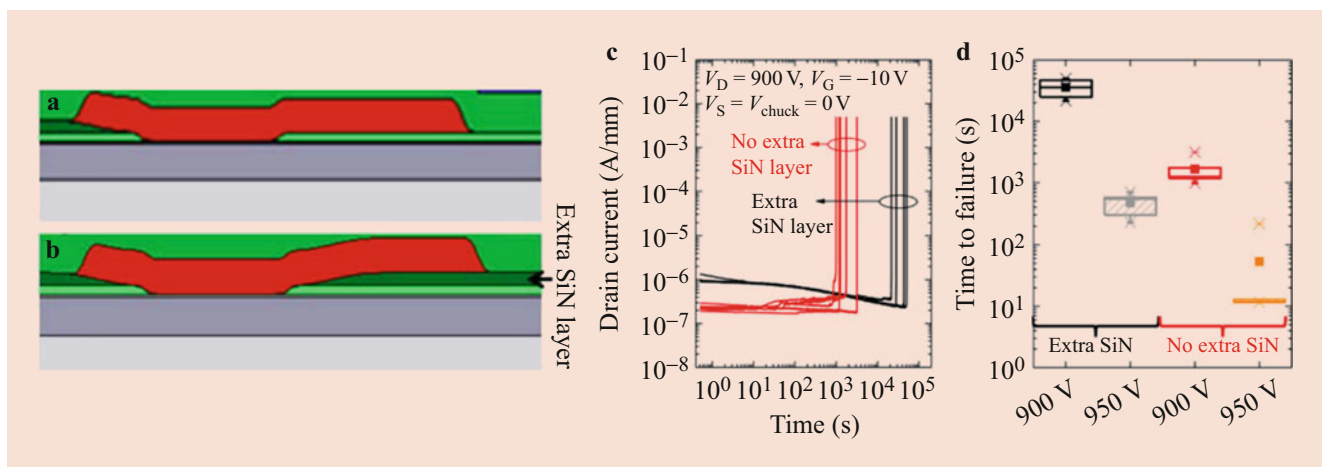


**Fig. 15.63** Schematic of the variation in the device geometry, showing a structure (a) without and (b) with an extra SiN layer. An additional SiN layer is introduced in order to reduce the electric field at the edge of the gate. (c) Constant voltage test at  $V_D = 900$  V, demonstrating that the

extra nitride layer increases time to failure by one order of magnitude. (d) Box chart showing the measured time to failure in devices with and without extra SiN layer stressed at  $V_D = 900$  V and  $V_D = 950$  V. (© 2017 IEEE. Reprinted, with permission, from [161])

and can reach values around 6 MV/cm at  $V_{DS} = 600$  V. A physical evidence of this hypothesis was obtained by TEM evaluation [161]. First, emission microscopy was performed in off-state conditions, to identify the presence of hot spots (Fig. 15.62). Then, cross sections were prepared by Focused Ion Beam (FIB) and then observed by Transmission Electron Microscopy (TEM, Fig. 15.62). The results demonstrated that degradation is effectively located at the drain-side gate edge. Stress induced the generation of a shunt-path between the gate head and the 2DEG, across the SiN/AlGaN stack. Such a degradation process is extrinsic (in the sense that it involves a material other than GaN, i.e., SiN). In [161], the authors proposed to add a graded layer of silicon nitride under

the head of the gate to improve device reliability (Fig. 15.63). Figure 15.63 reports the results of a constant voltage stress experiment: the presence of the extra SiN layer can increase the TTF by one order of magnitude.

After discussing the extrinsic breakdown mechanisms induced by off-state stress (see above), we discuss here the intrinsic breakdown mechanisms related to the GaN material itself. Recent papers (see, for instance, [160, 165]) studied the robustness of the buffer stack submitted to high off-state conditions. To separately evaluate lateral and vertical breakdown, two-terminal stress experiments are typically carried out. The devices are stressed from drain to substrate, and this results in a significant vertical field. At industrial level,

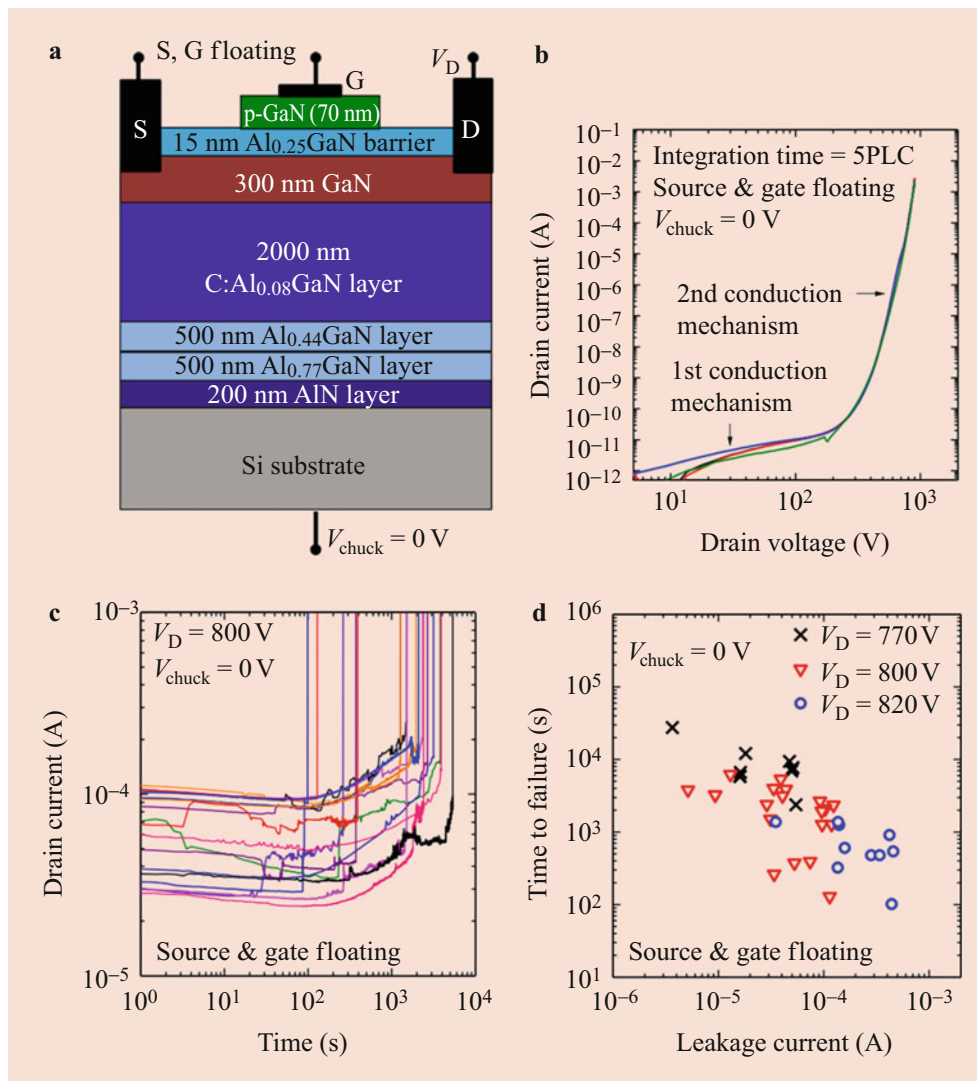


**Fig. 15.64** (a) Schematic representation of the device under test. (b) Drain- controlled vertical leakage current measurement. The measurements were stopped at breakdown. (c) Drain current monitored

during a constant voltage stress ( $V_D = 800$  V). (d) TTF dependence on the initial leakage for three drain bias levels applied during the constant voltage stress. (© 2017 IEEE. Reprinted, with permission, from [160])

results on buffer reliability can be obtained also by means of high-voltage off-state stress (HVOS) [165], a condition where a high voltage is applied to the drain, with substrate and source grounded and gate in pinch-off.

Recently, Borga et al. demonstrated that GaN can show a time-dependent vertical breakdown that can result in a sudden increase in vertical leakage current [160]. The study was carried out on devices having the schematic structure reported in Fig. 15.64a, that are designed for 200 V operation. Before the execution of the stress tests experiments, the vertical (2-terminal) leakage current was characterized (see Fig. 15.64b): two conduction mechanisms were identified, with a change in slope around  $V_D = 300$  V. Such behavior was explained by considering that for low vertical bias ( $<200$  V)

conduction is nearly ohmic and possibly assisted by dislocations. For higher voltages ( $>300$  V) the depletion of the buffer results in the ionization of defects. Poole-Frenkel effects are favored, and an increase in vertical leakage is observed at high bias.

Figure 15.64c reports the results of a constant voltage stress test carried out on 18 identical devices with a vertical voltage of 800 V. After an initial stage where the leakage is stable, devices show first an increase in the noise superimposed to leakage current and then a sudden increase in vertical leakage. This is similar to the behavior of dielectrics under time-dependent breakdown testing, typically explained by the defect-percolation model. Figure 15.64d shows the time-to-failure (TTF) and leakage current measured on three

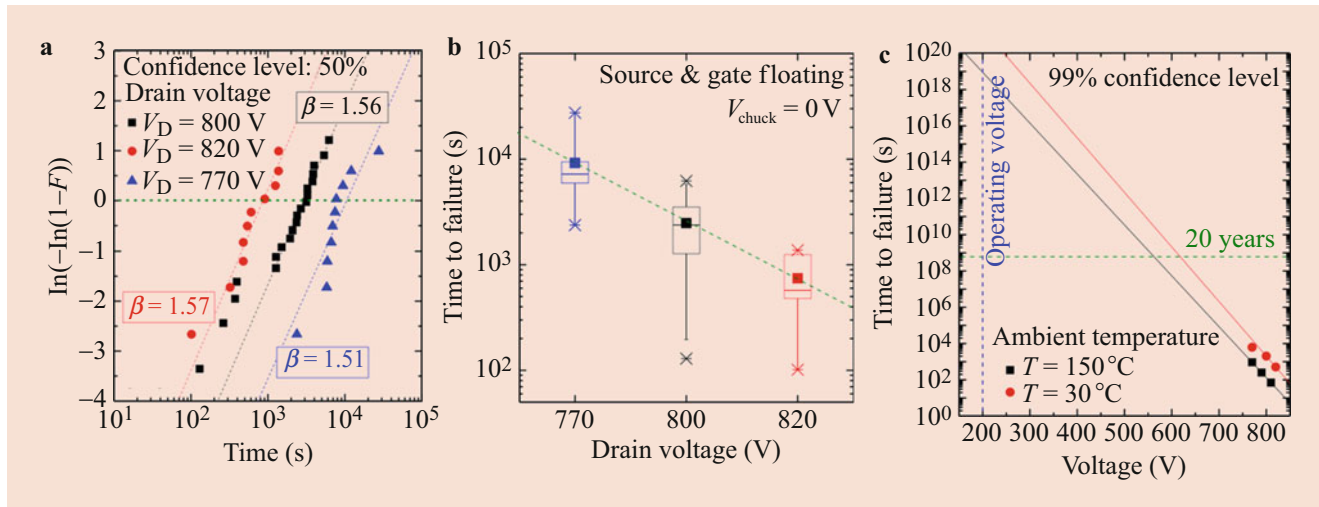


**Fig. 15.65** (a) Weibull plot of the constant voltage stress. (b) TTF dependence on the applied drain voltage (box chart). (c) TTF dependence on the drain voltage applied at ambient temperature of 30 °C and 150 °C.

Each point represents the Weibull scale factor with a confidence level of 99%. (© 2017 IEEE. Reprinted, with permission, from [160])

sets of samples stressed at different voltages. As expected, by increasing stress bias a decrease in TTF and an increase in leakage current are detected.

A further similarity with dielectric breakdown comes from the fact that TTF is Weibull-distributed. For reference, one can look at Fig. 15.65a, which reports the Weibull plots obtained by stress at three different voltage levels. Figure 15.65b indicates that TTF has an exponential dependence on stress voltage and supports the hypothesis that the degradation mechanism is field-dependent. In addition, a low thermal activation (0.25 eV) was measured.

The time-dependent breakdown of GaN does not represent a major limitation for this material. For the 200 V technology analyzed in [160], the maximum voltage for 20 years lifetime with 1% failure rate is around 560 V.

### 15.4.7 Stability in Semi-on Conditions

In several real-life application scenarios, GaN-based transistors can be operated under hard switching conditions. A basic example is the case of a boost power converter, where the simultaneous presence of high current and high voltage can take place during the turn-on phase of the devices. It is therefore important to evaluate the stability of the devices not only under soft switching, but also under the more dangerous hard switching regime.

Recently, the interest toward the hard switching behavior of GaN HEMTs has significantly increased. As an example, we mention here three recent papers on the topic, that significantly contributed to the understanding of the trapping/degradation processes under hard switching, i.e., [138, 166, 167].

In [167], Joh et al. investigated the current collapse in GaN-based HEMTs by a novel setup, capable of controlling independently the gate and drain pulses. They suggested that the current collapse can improve under hard switching, due to the generation of holes through impact ionization. The hypothesis in [167] is that in hard switching, if there is a substantial overlap between voltage and current waveforms, hot carriers are produced (in density proportional to  $I_D \cdot \exp(-a/V_{DG})$ ) and can generate holes via impact ionization. Such holes can compensate the electrons trapped at the surface of the devices.

A similar setup was used by Rossetto et al. in [138], see a representative schematic in Fig. 15.66. Here the drain-gate-delay (the time interval between  $V_D = V_{DSQ}/2$  and  $V_G = V_{TH}$ ) is changed to generate hard switching events. In this paper, the authors showed that hard switching conditions may lead to an increase in dynamic-on resistance. They ascribed this effect to the fact that during the switching events, channel electrons are accelerated and consequently trapped within the devices.

A comprehensive description of the reliability of GaN-based transistors under hard switching tests was presented by Tanaka et al. in [166]. In this chapter, the authors presented the results of dynamic high-temperature operation life (D-HTOL) tests, carried out on transistors used in half-bridge configuration. They used a frequency of 6.6 kHz, an input voltage of 480 V and a switching current of 10 A. In addition, they compared two different kinds of transistors, the GITs and the HD-GITs, during the D-HTOL test. Here the HD-GIT is the hybrid-drain-embedded gate injection transistor, namely, a GIT where a pdrain is formed over a thick AlGaIn barrier to suppress current collapse. The authors of this paper

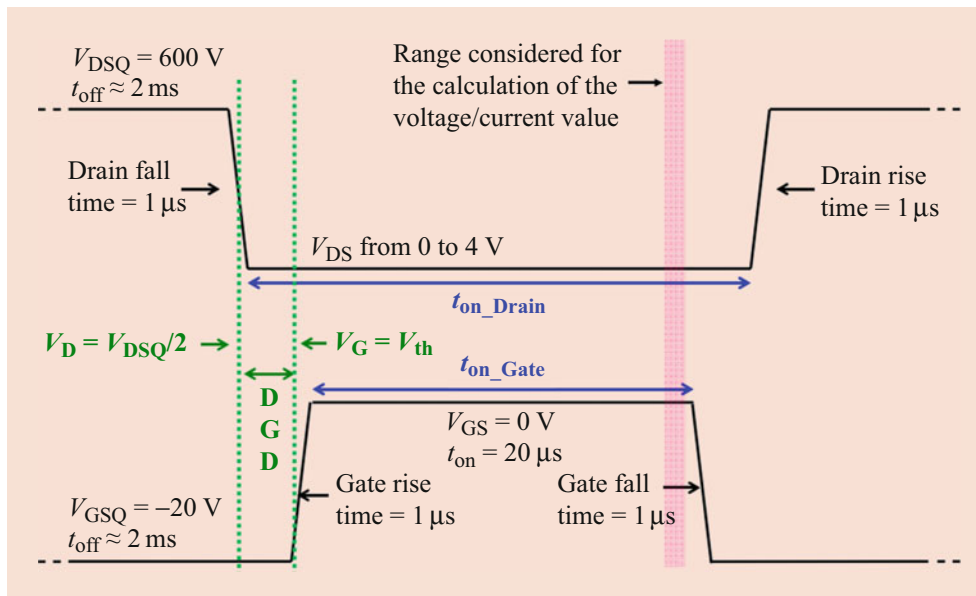


**Fig. 15.66** Representative schematic of the drain and gate pulses applied during the analysis of the dynamic ON-resistance. The DGD is defined as the time range between  $V_D = V_{DSQ}/2$  and  $V_G = V_{TH}$ . The

range of the pulse considered for the calculation of the current–voltage curve is highlighted in shaded pink. (© 2017 IEEE. Reprinted, with permission, from [138])

demonstrated that in the GIT the maximum switching voltage decreases as the switching current increases; eventually, for high switching currents, the maximum switching voltage becomes lower than the rated voltage. On the other hand, HD-GITs do not fail even under the most severe hard switching conditions ( $V_{DS} = 640$  V,  $I = 27$  A). Thermal runaway is not the primary reason for GIT breakdown. On the contrary, the better reliability of HD-GITs is explained by the injection of holes from pdrain. Such holes can compensate the hole emission from the GaN epilayer under high off-state stress and the capture of hot electrons under semi-on state. Tanaka et al. [166] suggested that the hot electron trapping at the surface of the GIT can trigger the destructive breakdown; a positive-feedback loop is created, that may lead to the sudden shift of the EL position from the gate edge to the drain edge.

## 15.5 Conclusions

The continuous progress of GaN technology makes gallium nitride an ideal candidate for the development of advanced power semiconductor devices. Exciting challenges in growth and fabrication have already been faced, and GaN transistors are ready to start playing a major role in power conversion.

Within this chapter, we have discussed the main properties of GaN and of GaN-based devices, with focus on four aspects: epitaxial growth, lateral device technology, GaN vertical devices, charge trapping, and reliability issues.

This chapter is a useful reference for the readers willing to approach GaN technology and for experts in the field desiring

an up-to-date discussion of the most relevant technological challenges and issues.

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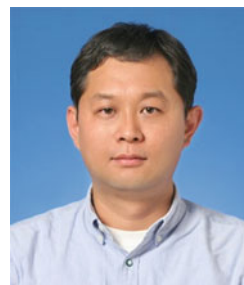
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