

Case No: IPR2023-01381
Patent No. 8,350,294

Petitioner's Demonstrative Exhibits

**Innoscence (Zhuhai) Technology Company, Ltd., and
Innoscence America, Inc.
v. Efficient Power Conversion Corporation**

December 18, 2024

**INNOSCIENCE EXHIBIT 1050
INNOSCIENCE v. EPC
IPR2023-01381**

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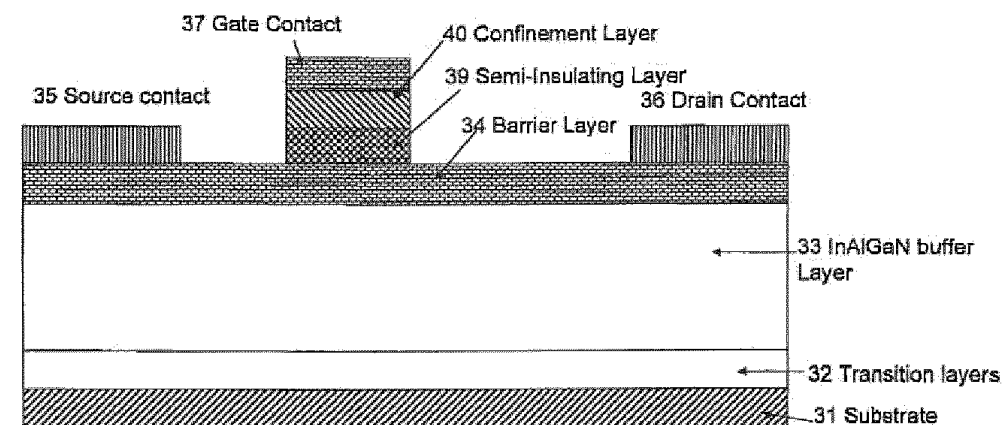
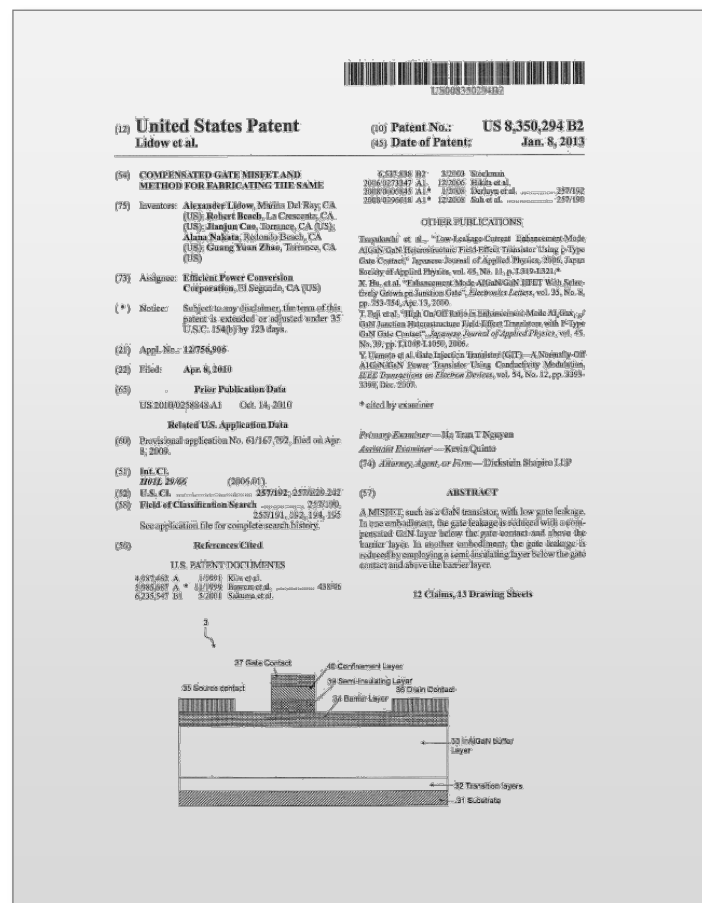
Overview of the '294 Patent and the Admitted Prior Art

The patent describes and claims a Gallium Nitride (GaN) transistor with a purported lower gate leakage

(54) COMPENSATED GATE MISFET AND METHOD FOR FABRICATING THE SAME

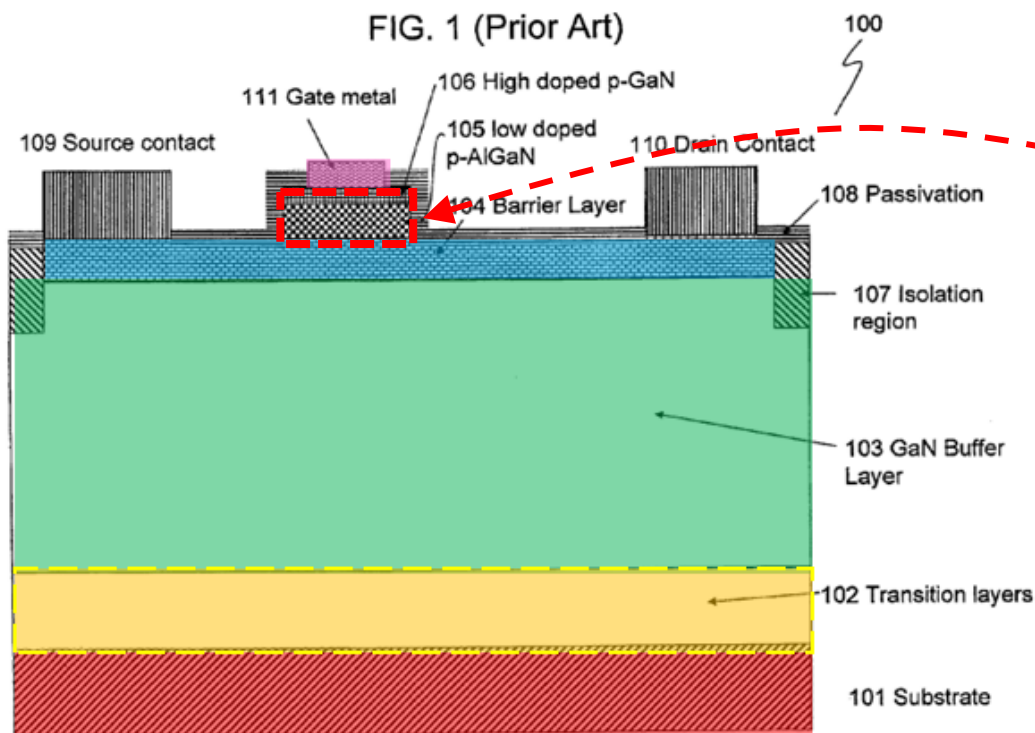
(57) ABSTRACT

A MISFET, such as a GaN transistor, with low gate leakage. In one embodiment, the gate leakage is reduced with a compensated GaN layer below the gate contact and above the barrier layer. In another embodiment, the gate leakage is reduced by employing a semi-insulating layer below the gate contact and above the barrier layer.

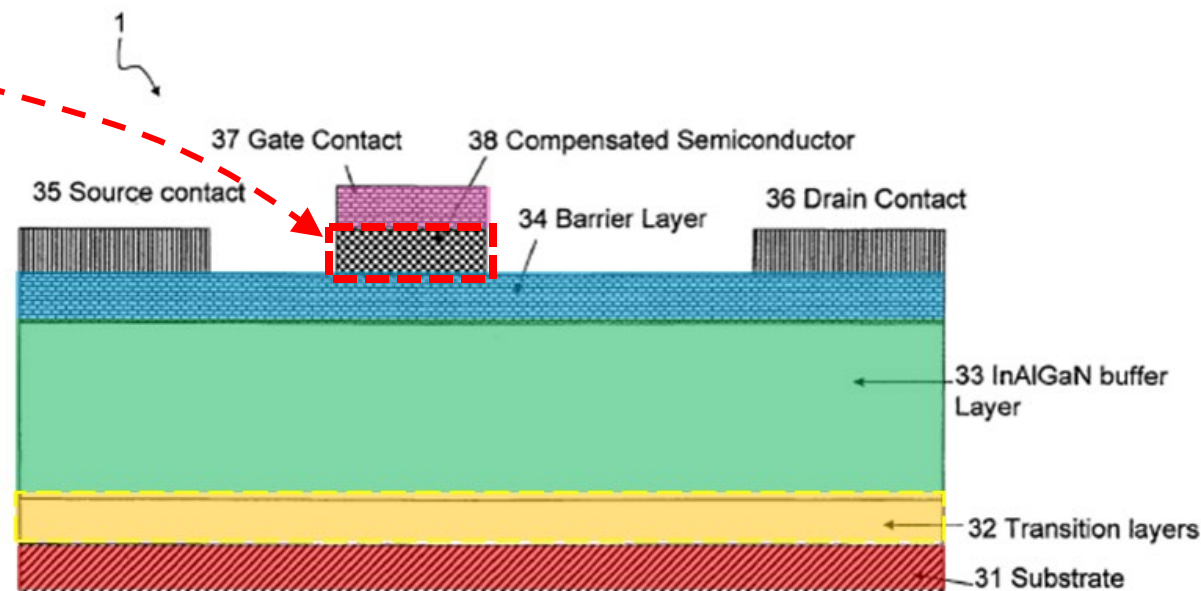


Patent admits most elements were known/conventional; only modification is changing the cap layer

Purportedly modified cap layer to be “compensated” or “semi-insulating;” other elements admitted in Prior Art



EX. 1001 at Fig. 1

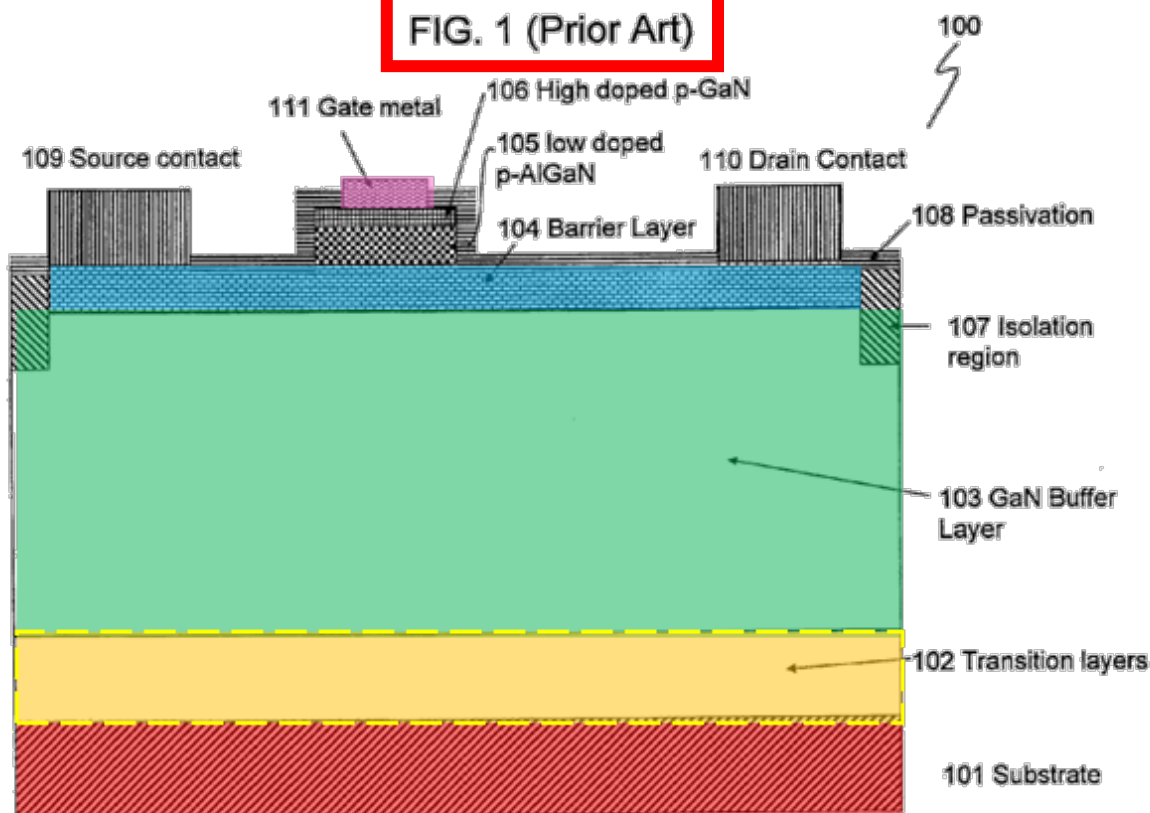


EX. 1001 at Fig. 2

FIG. 2

Prior art already has claimed **substrate**,
transition, **buffer**, **barrier**, and **gate contact**

FIG. 1 (Prior Art)



Ex. 1001, Fig. 1

1. A column III Nitride transistor comprising:
a substrate,
a set of III-N transition layers above the substrate,
a III-N buffer layer above the set of transition layers,
a III-N barrier layer above the buffer layer,
a compensated GaN layer above the barrier layer, and
a gate contact above the compensated GaN layer.

Ex. 1001, Claim 1

1. A column III Nitride transistor comprising:
a substrate,
a set of III-N transition layers above the substrate,
a III-N buffer layer above the set of transition layers,
a III-N barrier layer above the buffer layer,
a compensated GaN layer above the barrier layer, and
a gate contact above the compensated GaN layer.

2. The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.

3. The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.

7. A column III Nitride transistor comprising:
a substrate,
a set of III-N transition layers above the substrate,
a III-N buffer layer above the set of transition layers,
a III-N barrier layer,
a semi-insulating III-N layer above the barrier layer, and
a confinement layer above the semi-insulating III-N layer.

8. The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V.

9. The transistor of claim 7, wherein the confinement layer is made of SiN, SiO2, Al2O3, HfO2, Ga2O3, or InAlGaN.

Most elements, including dependent claims, are undisputed; dispute focuses on “compensated” or “semi-insulating”

- Compensated layer Disputed
- Conventional passivation Undisputed
- Conventional acceptors Undisputed

- Semi-insulating layer Disputed
- Conventional deep dopants Undisputed
- Conventional insulators Undisputed

Patent Owner cancelled other claims (4-6, 10-12) in the non-contingent motion to amend

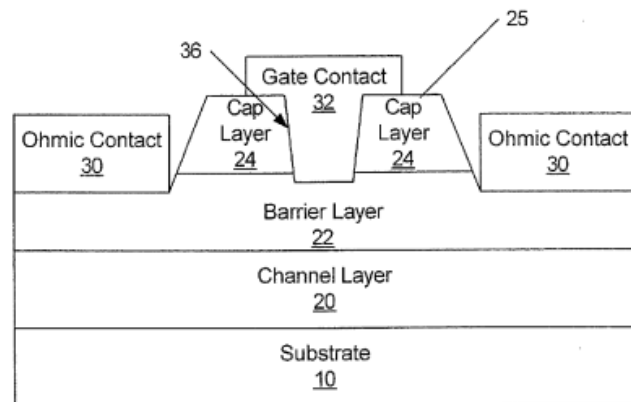
Ex. 1001, Claims 1-3 and 7-9

Paper No. 31 at 1.

Invalidity Grounds

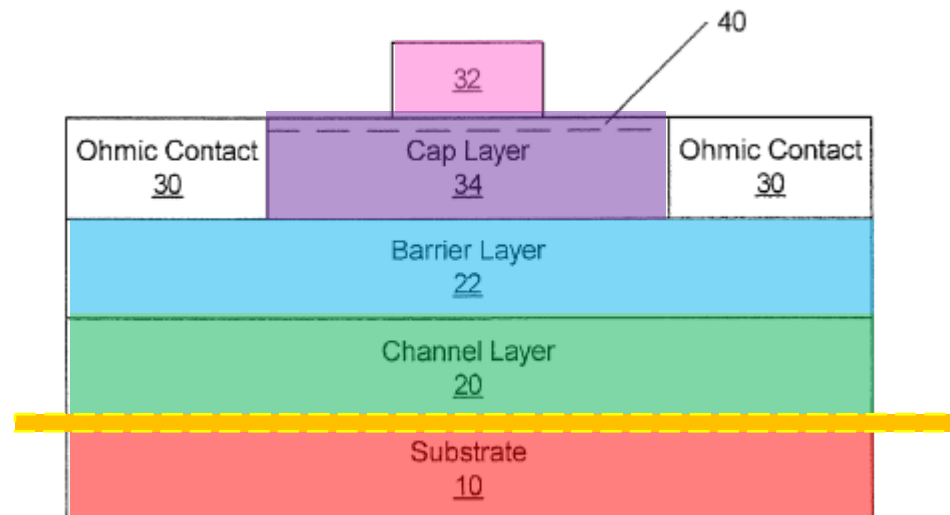
Two invalidity grounds (one with 3 parts), three references, all are undisputed prior art

Grounds	Challenged Claims	Basis	Prior Art
1A	1-12	§ 103	<i>Smith</i>
1B	1-12	§ 103	<i>Smith and Kigami</i>
1C	1-12	§ 103	<i>Smith and Uemoto</i>
2	1-12	§ 103	<i>Uemoto and Smith</i>



Smith discloses GaN transistors with all the conventional layers, and a cap layer that can be formed as “compensated” or “semi-insulating”

- Prior art §102(b)/(e): Published July 19, 2007
- Does not specify enhancement or depletion
- Discloses GaN HEMT transistors with multiple combinations capping layers.

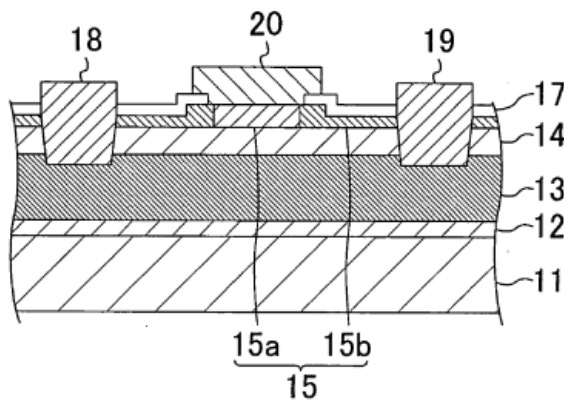


Ex. 1005 at Fig. 2 (annotated)

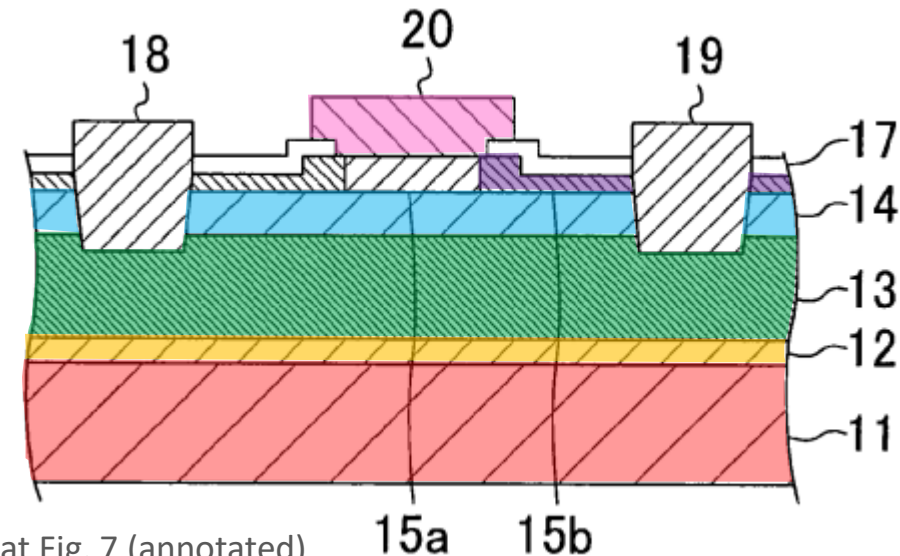
Uemoto discloses GaN transistors with all the conventional layers and a H diffused layer where H passivates Mg. That layer is “compensated” and can be “semi-insulating”

 US 2008/0087915 A1	
(19) United States	(10) Pub. No.: US 2008/0087915 A1
(12) Patent Application Publication	(43) Pub. Date: Apr. 17, 2008
Uemoto et al.	
(54) NITRIDE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME	Publication Classification
(76) Inventors: Yasuhiro Uemoto, Shiga (JP); Masahiro Hikita, Hyogo (JP); Tetsuo Ueda, Osaka (JP); Tsuyoshi Tanaka, Osaka (JP); Daisuke Ueda, Osaka (JP)	(51) Int. Cl. H01L 21/336 (2006.01) H01L 29/772 (2006.01) H01L 31/00 (2006.01)
Correspondence Address: MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096	(52) U.S. CL. 257/192; 438/285; 257/E29.242; 257/E21.409
(21) Appl. No.: 11/878,352	(57) ABSTRACT
(22) Filed: Jul. 24, 2007	A nitride semiconductor device includes: a first nitride semiconductor layer; a second nitride semiconductor layer formed on the first nitride semiconductor layer and having a wider band gap than the first nitride semiconductor layer; and a third nitride semiconductor layer formed on the second nitride semiconductor layer. A region of the third nitride semiconductor layer located below the gate electrode is formed with a control region having a p-type conductivity, and a region of the third nitride semiconductor layer located between the gate electrode and each of the source electrode and the drain electrode is formed with a high resistive region having a higher resistance than the that of the control region.
(30) Foreign Application Priority Data Oct. 12, 2006 (JP) 2006-278913	

- Prior Art §102(a)/(e): Published April 17, 2008
- Enhancement mode
- Discloses a device with the “compensated GaN layer” formed to minimize gate leakage current using H diffusion film



Ex. 1006 at Cover



Ex. 1006 at Fig. 7 (annotated)

JP 2006-253224 A 2006.9.21

(19) 日本国特許庁 (JP)		(12) 公開特許公報 (A)		(11) 特許出願公開番号 特開2006-253224 (P2006-253224A)	
		(43) 公開日 平成18年9月21日 (2006.9.21)			
(51) Int. Cl.		F 1		テーマコード (参考)	
H 01 L 29/786 (2006.01)		H 01 L 29/78 618 B		5 F 1 0 2	
H 01 L 21/22 (2006.01)		H 01 L 21/22 C		5 F 1 1 0	
H 01 L 21/324 (2006.01)		H 01 L 21/324 C		5 F 1 4 0	
H 01 L 29/78 (2006.01)		H 01 L 29/78 3 0 1 B			
H 01 L 29/812 (2006.01)		H 01 L 29/78 618 G			
		審査請求 未請求 請求項の数 10 O L (全 15 頁) 最終頁に続く			
(21) 出願番号 特願2005-64397 (P2005-64397)		(71) 出願人 000003609			
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		番地の1 株式会社豊田中央研究所内			
				最終頁に続く	

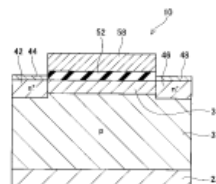
(54) 【発明の名称】 半導体装置とその製造方法

(57) 【要約】

【課題】 窒化ガリウム (Ga N) を利用する半導体装置において、M I S型のゲート構造の閾値電圧を低減すること。

【解決手段】 マグネシウムを含む窒化ガリウム (Ga N) の半導体層 3 2と、その半導体層 3 2にゲート絶縁膜 5 2を介して対向しているゲート電極 5 8を備えている半導体装置 1 0である。半導体層 3 2のうちのゲート電極 5 8が対向している領域に、水素原子が局所的に偏在している局所的領域 3 4が形成されていることを特徴としている。局所的領域 3 4ではマグネシウムが不活性化されている。

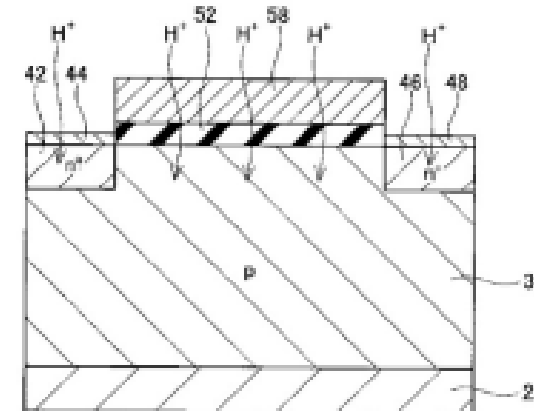
【選択図】 図 1



Ex. 1008 at Cover

Kigami discloses a technique for the specific issue of locally introducing H in GaN transistors to passivate dopants and increase resistivity

- Prior Art §102(a)/(e): Published September 21, 2006
- Enhancement mode
- Discloses a technique for localized passivation of Mg dopants in HEMTs using H plasma to increase resistance



Ex. 1008 at Fig. 5

Claim Construction / Interpretation

1. Construction of “compensated GaN layer” (claim 1, [1e])
2. Construction of “a gate contact above the compensated GaN layer” (claim 1, [1f])
3. Interpretation of claims 1-3 as directed to enhancement-mode transistor

2. Construction for “compensated GaN layer”

1. Compensated GaN layer
2. Gate Contact Above
3. Enhancement Mode

Claim Term	Petitioner	Patent Owner
“Compensated GaN Layer”	“a doped GaN layer formed with a step to passivate its impurities”	“a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).”

ITC and Board (at institution) rejected EPC’s proposal to restrict “compensated GaN” to be “gate material”

Ex. 1049 at 18-19; Ex. 2022 §IV.B.

ITC construed “compensated GaN” with a broader construction (the portion in green), which the prior art grounds meet

Ex. 1049 at 16-20; Ex. 2022 at §IV.B.

ITC did not adopt the private parties' proposed construction adopting instead a different, broader construction using "cancel electric effects"

UNITED STATES INTERNATIONAL TRADE COMMISSION Washington, D.C.	
In the Matter of	
CERTAIN SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING SAME AND PRODUCTS CONTAINING THE SAME	Investigation No. 337-TA-1366
COMMISSION OPINION	

"Commission has determined to expressly adopt the construction proposed by OUII and construe '**compensated GaN layer**' to mean '**a GaN layer in which one type of impurity cancels the electric effects of another type of impurity.**'"

Ex. 1049 at 16-17

ITC noted it would be improper to require
“Compensated GaN layer” to be part of the gate

“[T]here is nothing in that disclosure that requires the ‘compensated GaN layer’ to be a part of the gate contact. ... Thus, **it would be improper to limit the invention as EPC argues** absent clear direction in the intrinsic evidence to do so.”

Ex. 1049 at 19

UNITED STATES INTERNATIONAL TRADE COMMISSION Washington, D.C.	
In the Matter of	
CERTAIN SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING SAME AND PRODUCTS CONTAINING THE SAME	Investigation No. 337-TA-1366
COMMISSION OPINION	

Comparing “Compensated GaN” constructions

1. Compensated GaN layer
2. Gate Contact Above
3. Enhancement Mode

ITC’s construction uses “cancels electrical effects” (like EPC’s) but is broader, removing “gate material” and not using Innoscence’s “step”

Broader than Petitioner and Patent Owner

Claim Term	Petitioner	Patent Owner	ITC
“Compensated GaN Layer”	“a doped GaN layer formed with a step to passivate its impurities”	“a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).”	“a GaN layer in which one type of impurity cancels the electric effects of another type of impurity ”

At institution the Board, like the ITC, rejected EPC's construction incorporating "gate material"

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

Conclusion

For the reasons set forth above, and after review of the claims, written description, and prosecution history cited by the parties, we do not construe "compensated GaN layer" to require a "compensated GaN gate material." And, for the reasons discussed above, we need not address at this time whether a "compensated GaN layer" is a product-by-process limitation or includes materials that are compensated using methods other than hydrogen passivation.

Paper No. 11 at 15

At institution, Board didn’t adopt an express construction finding Grounds met “compensated GaN” under any construction for purposes of institution

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD
AND
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EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY MCGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

In view of the foregoing, Petitioner demonstrates sufficiently for purposes of institution that Smith teaches or suggests a “compensated GaN layer” under either parties’ construction of that term. Petitioner also sufficiently demonstrates for purposes of institution that Smith teaches or suggests every other limitation of claim 1. Thus, Petitioner demonstrates a reasonable likelihood that the subject matter of claim 1 would have been obvious over Smith.

Paper No. 11 at 19

We do not construe “compensated GaN layer” to require a layer that is part of the gate, or operates in conjunction with gate electrode 20 to turn the transistor on and off. And, as shown in Figure 7 of Uemoto, a portion of element 15b is above second nitride layer 14 and below gate contact 20. Ex. 1006, Fig. 7. Accordingly, on this record, Petitioner demonstrates sufficiently for purposes of institution that Uemoto discloses a “compensated GaN layer.”

Paper No. 11 at 28

“Compensated GaN” Met under any construction

1. Compensated GaN layer
2. Gate Contact Above
3. Enhancement Mode

As the ITC construction is broader, the Grounds also meet the “compensated GaN” under the ITC construction

Claim Term	Petitioner	Patent Owner	ITC
“Compensated GaN Layer”	“a doped GaN layer formed with a step to passivate its impurities”	“a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).”	“a GaN layer in which one type of impurity cancels the electric effects of another type of impurity ”

Broader than Petitioner and Patent Owner

- Because the ITC construction is similar to EPC’s but broader (removing “gate material”) the grounds meet the ITC construction under the same rationale as in the Petition

Need not construe if unnecessary to determine invalidity

1. Compensated GaN layer

2. Gate Contact Above

3. Enhancement Mode

Like at institution, if the Board finds Petitioner's grounds meet "compensated GaN" under any construction, Board need not expressly construe



"[B]ecause no express construction is needed for our decision, we do not construe them. See *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017)."

PNC Bank, N.A. v. United Servs. Auto. Ass'n, No. IPR2021-01073, Paper 72, 13 (P.T.A.B. Jan. 19, 2023).

“Compensated GaN”: Conclusion

1. Compensated GaN layer

2. Gate Contact Above

3. Enhancement Mode

Claim Term	Conclusion
“Compensated GaN Layer”	- Not restricted to “GaN gate material” as EPC proposes - No need expressly construe if unnecessary for patentability

As the ITC and the Board (at institution) concluded, “compensated GaN layer” is not restricted to “gate material”

Like at institution, express construction is only required if necessary, but here the grounds meet “compensated GaN layer” under any construction

Construction of element [1f]

1. Compensated GaN layer
2. Gate Contact Above
3. Enhancement Mode

Claim Term	Petitioner	Patent Owner
"A Gate Contact Above the Compensated GaN Layer"	No construction, Plain & Ordinary	"a gate comprised of a gate contact and the compensated GaN layer"

EPC asks to rewrite [1f] attempting again to limit the "compensated" layer to be part of the gate

OUII Rep at 20 (citing JX-0014 ('294 patent) at cl. 1). That is, there is nothing in that disclosure that requires the "compensated GaN layer" to be a part of the gate contact. Figure 2 (depicted above) that EPC relies on also shows "compensated GaN layer" 38 and gate contact 37 as separate and distinct structures. Thus, it would be improper to limit the invention as EPC argues absent clear direction in the intrinsic evidence to do so. *Hill Rom Servs., Inc. v. Stryker Corp.*, Ex. 1049 at 19

The ITC already declined to limit "compensated GaN layer" to be part of the gate finding there is nothing in the disclosure that supports such narrow construction

“Gate contact above” Has a Plain Meaning

1. Compensated GaN layer

2. Gate Contact Above

3. Enhancement Mode

As Dr. Shealy explained, EPC’s rewriting of [1f] is unwarranted, a POSITA would have readily understood the meaning of “gate contact” and “above” with its ordinary meaning

[012] The proposed construction would entirely rewrite [1f]. I find no support in the claims or the specification of the ’294 patent to rewrite [1f] as EPC and Dr. Schubert propose. The terms “a gate contact” and “above” in [1f] would have been clear to a POSITA, they have an ordinary meaning. A POSITA would have readily understood what is a “gate contact.” And a POSITA would have also readily understood what it means for the gate contact to be “above” a different layer using the ordinary meaning of “above”—i.e., being higher than.

Ex. 1033 at ¶12

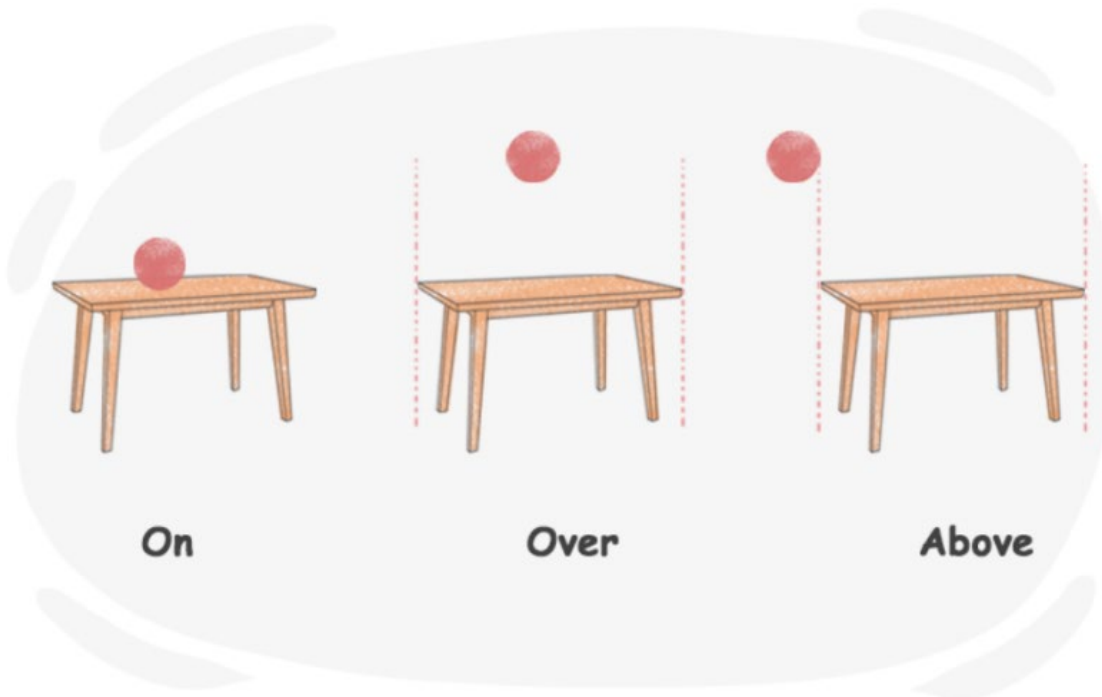
“Above” Has a Plain Meaning as “Higher Than”

1. Compensated GaN layer

2. Gate Contact Above

3. Enhancement Mode

[1f]: “A Gate Contact **Above** the Compensated GaN Layer”



prepositions of direction and place

Ex. 1027 at 3

“Above” has a plain meaning (e.g., higher than) without limitations on being in contact or directly on. This term need not be construed

EPC insists on “compensated GaN” being part of the gate

1. Compensated GaN layer

2. Gate Contact Above

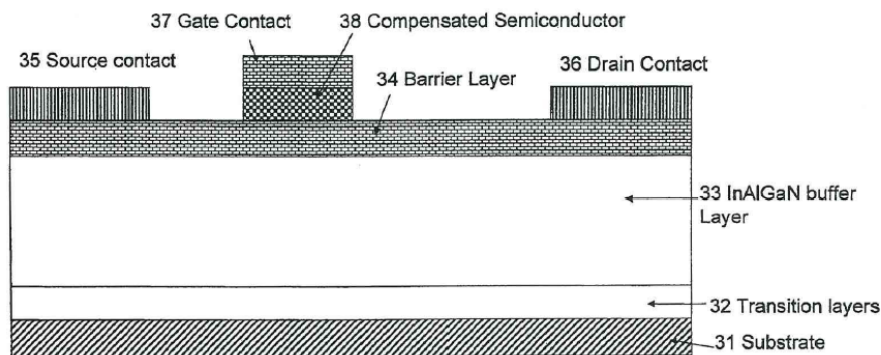
3. Enhancement Mode

EPC seeks to rewrite [1f] based on a figure

Incorrect

Figure 2 is not “an embodiment” of the compensated GaN invention of the ‘294 patent – it **is the invention**.

Paper 32 at 5



Ex. 1001 at Fig. 2

FIG. 2

EPC seeks to rewrite [1f] based on “goals of the invention”

Incorrect

... Petitioner contorts the plain meaning of “a gate contact above the compensated GaN layer,” so that the claims cover transistors that do not meet the **goals of the invention**, make it clear that a proper construction specifying that the gate contact and compensated GaN layer are part of a gate structure, is necessary.

Paper 18 at 8

EPC's figure-based construction contradicts the patent

1. Compensated GaN layer

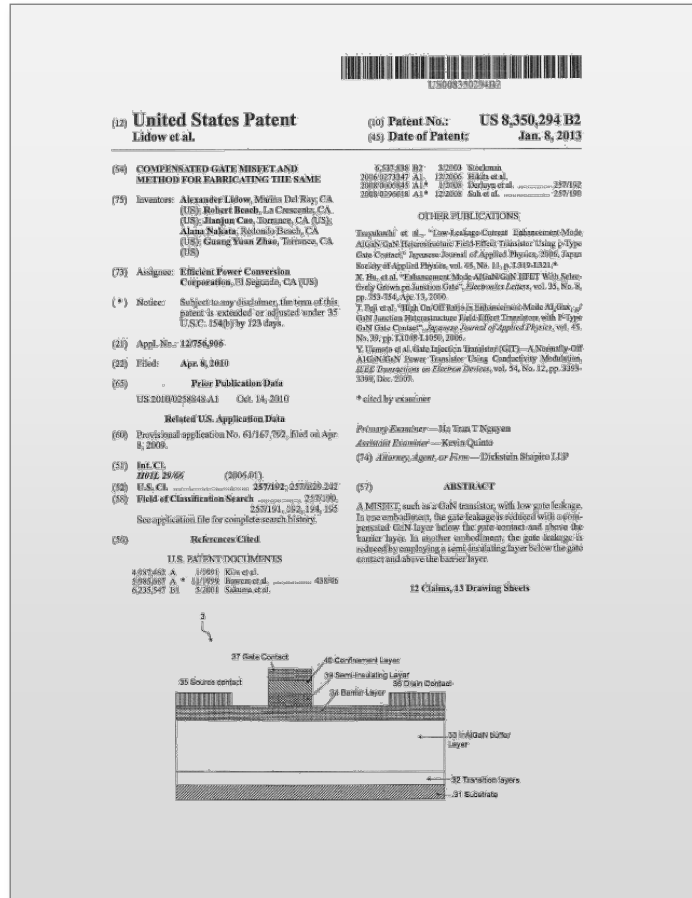
2. Gate Contact Above

3. Enhancement Mode

The patent contradicts EPC, stating the invention should not be limited based on description or drawings. EPC “gate contact” improperly limits to an example

“The above description and **drawings are only to be considered illustrative** of specific embodiments, which achieve the features and advantages described herein. **Modifications and substitutions to specific process conditions can be made.** Accordingly, the embodiments of the invention are not considered as being limited by the foregoing description and drawings.”

Ex. 1001 at 5:3-9



EPC's figure construction is a “cardinal sin”

1. Compensated GaN layer

2. Gate Contact Above

3. Enhancement Mode

EPC's reading of the claim to be limited by patent drawings and descriptions, requiring the “compensated GaN” layer to be part of the gate based on Fig. 2, is the “cardinal sin of patent law.”



“The Texas Digital court explained that it advanced the methodology set forth in that opinion in an effort to combat what this court has termed “one of the ***cardinal sins of patent law—reading a limitation from the written description into the claims.***”

Phillips v. AWH Corp., 415 F.3d 1303, 1320 (Fed. Cir. 2005).

EPC's "goals of the invention" contradicts the law

1. Compensated GaN layer

2. Gate Contact Above

3. Enhancement Mode

EPC's constructions ignoring the claim and rewriting [1f] based on "goals of the invention" "violates nearly every tenet of claim construction"



"The district court properly determined that 'claim construction is a ***function of the words of the claim not the 'purpose' of the invention,***' and that Source's construction '***violates nearly every tenet of claim construction*** and amounts to a wholesale judicial rewriting of the claim.'"

Source Vagabond Sys. Ltd. v. Hydrapak, Inc., 753 F.3d 1291, 1301 (Fed. Cir. 2014)

This difference between layers and other components is reflected in the '294 patent specification. For example, Figure 7 of the '294 patent illustrates “a compensated semiconductor layer 38 over the barrier layer 34” before any gate structures are formed:

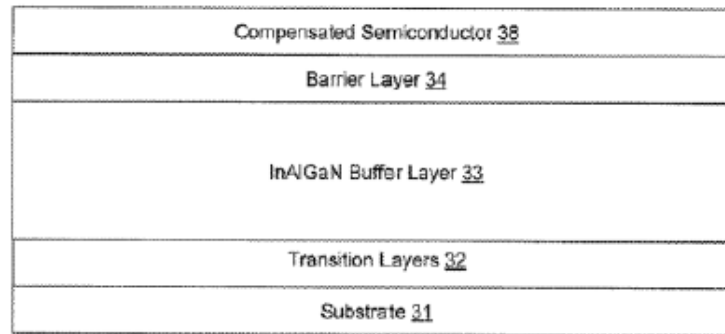


FIG. 7

See '294 patent at Fig. 7, 3:30-31. The patent states that this compensated layer can be a compensated GaN layer. *Id.* at 3:7-17. Thus, it would be incorrect to conclude, as EPC appears to, that the '294 patent exclusively describes a compensated GaN layer as being associated with a gate.

Ex. 2022 at 20

At the ITC, the ALJ declined to limit “compensated GaN layer” to be part of the gate, finding EPC’s interpretation incorrect because the patent does not describe compensated GaN exclusively as part of the gate

“Gate contact above”: Conclusion

1. Compensated GaN layer
2. Gate Contact Above
3. Enhancement Mode

Claim Term	Conclusion
“Compensated GaN Layer”	- Not restricted to “GaN gate material” as EPC proposes - No need expressly construe if unnecessary for patentability
“A Gate Contact Above the Compensated GaN Layer”	- “Compensated GaN” need not be comprised in the gate - No need construe “above” because the term has plain and ordinary meaning

No need to
construe “above” it
has a plain meaning

Like ITC, reject limiting
compensated GaN to be
part of the gate

3. Interpretation as enhancement mode

1. Compensated GaN layer
2. Gate Contact Above
3. Enhancement Mode

Claim Term	Petitioner	Patent Owner
?	Not limited to enhancement-mode devices	Directed to enhancement-mode transistor

Without identifying any term to construe, EPC proposes to limit the claims to e-mode devices

Similarly, claim 1 of the '294 patent is directed simply to a "column III Nitride transistor," with no limitation of its mode of operation. '294 patent at claim 1. To limit claim 1 to an enhancement mode transistor on this record would commit "one of the cardinal sins of patent law—reading a limitation from the written description into the claims"—and I decline to do so. See *Phillips*, 415 F.3d at 1320 (quoting *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1340 (Fed.Cir.2001).

Ex. 2022 at 94

The ITC ALJ already declined EPC's e-mode interpretation because it would be one of the "cardinal sins" of claim construction

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

EPC argues claims are limited to
enhancement mode but as the Board noted,
claim 1 is more broadly directed to “column
III Nitride,” not enhancement mode

First, although the title of the '294 patent is
directed to a “Compensated Gate MISFET,”
claim 1 is more broadly directed to “[a]
column III Nitride transistor.” Ex. 1001,
5:12, code (54).

Paper No. 11 at 13.

EPC's enhancement mode interpretation is incorrect

1. Compensated GaN layer

2. Gate Contact Above

3. Enhancement Mode

The claim is not limited to enhancement mode devices, even EPC's expert (Dr. Schubert) admits the patent describes both E-mode and D-mode operations

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,

Petitioner, v.

EFFICIENT POWER CONVERSION CORPORATION,

Patent Owner.

IPR2023-01381
U.S. Patent No. 8,350,294

Declaration of E. Fred Schubert, PhD.

“The '294 Patent describes improvements to conventional E-mode and **D-mode** GaN transistors. See Ex. 1001 at 1:13-18, 4:55-57.”

Ex. 2009 ¶48

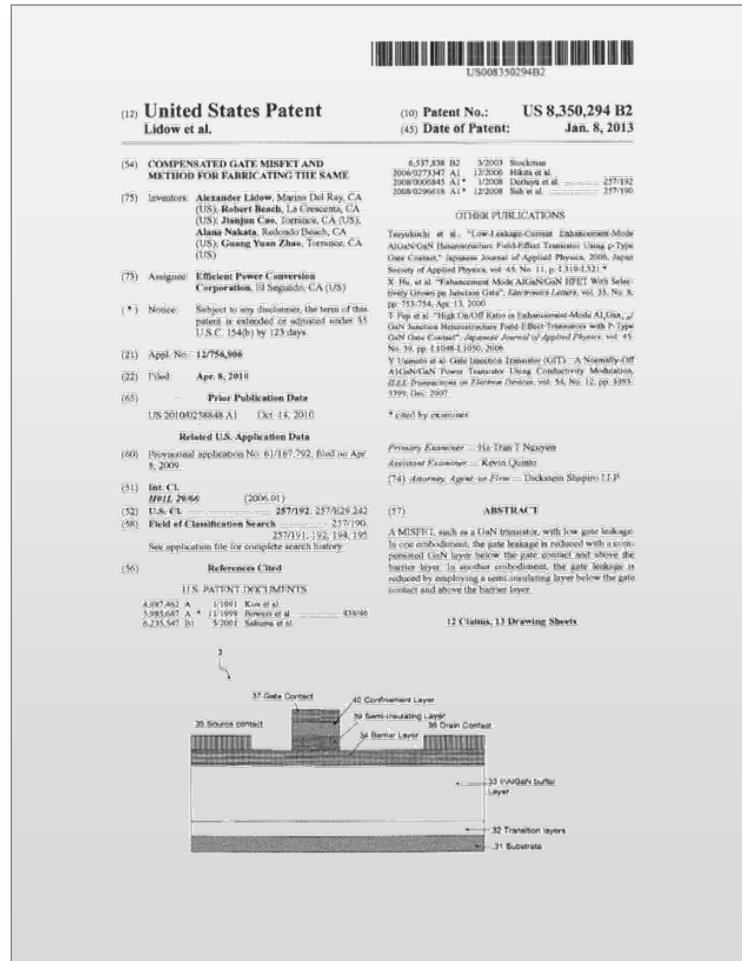
EPC's "interpretation" contradicts the specification

- 1. Compensated GaN layer
- 2. Gate Contact Above
- 3. Enhancement Mode

EPC's proposed enhancement-mode "interpretation" contradicts embodiments in the specification

"By appropriate application of gate voltage, **the device can be changed to a depletion mode device**, such that it is on at 0V on the gate."

Ex. 1001 at 4:55-60



Similarly, claim 1 of the '294 patent is directed simply to a “column III Nitride transistor,” with no limitation of its mode of operation. '294 patent at claim 1. To limit claim 1 to an enhancement mode transistor on this record would commit “one of the cardinal sins of patent law—reading a limitation from the written description into the claims”—and I decline to do so. See *Phillips*, 415 F.3d at 1320 (quoting *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1340 (Fed.Cir.2001)).

Having established that claim 1 is not limited to an enhancement-mode device, the relevant task is to compare the structure identified in the claim to the structure disclosed in Beach189, not to resolve disputes about how the structure in Beach189 could be used hypothetically. See *In re Schreiber*, 128 F.3d at 1477. Accordingly, I need not resolve whether Beach189 discloses a transistor that could be operated as an enhancement-mode device.¹³

Ex. 2022 at 94

At the ITC, the ALJ declined to limit claims to enhancement-mode devices concluding “claim 1 is not limited on an enhancement-mode device”

1. Compensated GaN layer
2. Gate Contact Above
3. Enhancement Mode

Claim Term	Conclusion
“Compensated GaN Layer”	- Not restricted to “GaN gate material” as EPC proposes - No need expressly construe if unnecessary for patentability
“A Gate Contact Above the Compensated GaN Layer”	- “Compensated GaN” need not be comprised in the gate - No need construe “above” because the term has plain and ordinary meaning

All these conclusions are consistent with the ITC Opinion

Interpretation	Conclusion
Claims 1-3	- Not limited to enhancement-mode devices.

Ground 2

Why are we starting with Ground 2?

Because unlike Smith, invalidity based on Uemoto was litigated at the ITC. The ITC already resolved the key issues on Uemoto streamlining issues here.

ITC did not opine about the Smith grounds

	Challenged Claims	Basis	Prior Art
1A	1-12	§ 103	Smith
1B	1-12	§ 103	Smith and Kigami
1C	1-12	§ 103	Smith and Uemoto
2	1-12	§ 103	Uemoto and Smith

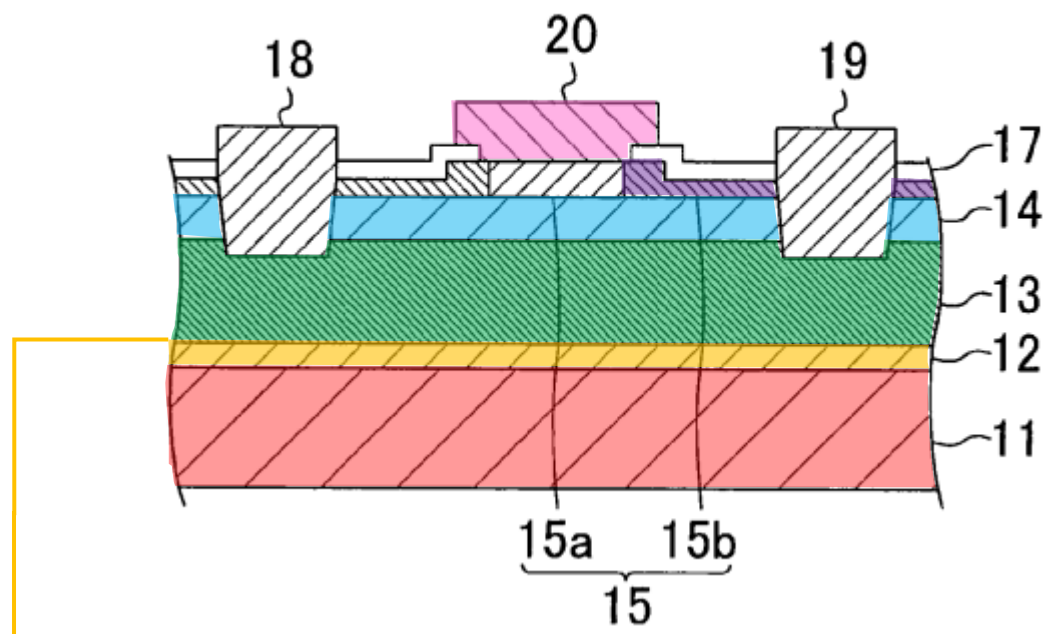
ITC opined about Uemoto by itself (without Smith) and only for claims 1-3

Ground 2: Overview and disputed elements

EPC only disputes the “compensated GaN” [1e] and the position of the “compensated GaN” in [1f], no dispute for other elements

- Not Disputed
- Not Disputed
- Not Disputed
- Not Disputed
- Not Disputed
- Disputed
- Disputed Position
- Not Disputed
- Not Disputed

1p	A column III-Nitride transistor comprising:
1a	a substrate,
1b	a set of III-N transition layers above the substrate,
1c	a III-N buffer layer above the set of transition layers,
1d	a III-N barrier layer above the buffer layer,
1e	a compensated GaN layer above the barrier layer, and
1f	a gate contact above the compensated GaN layer.
2	The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
3	The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.



Undisputed: multiple transition layers in combination with Smith.

Uemoto discloses the same materials/doping

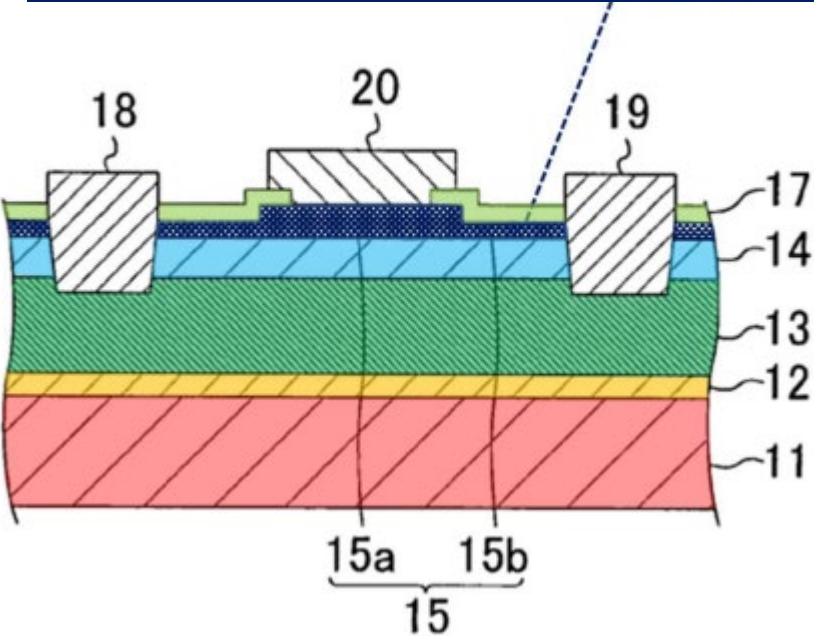
'294 Patent	Uemoto
"a substrate 31 that may comprise, for example, <u>silicon Si</u> , silicon carbide SiC or sapphire." Ex. 1001 at 2:57-59	"a substrate 11 is made of <u>silicon</u> and its principal plane is the (111) plane." Ex. 1006 [0031]
" Transition layers 32 may comprise, for example, <u>AlN</u> or AlGa _N , with a thickness of between 0.1 to 1.0 μm." Ex. 1001 at 1:56-2:2	"A buffer layer 12 of <u>AlN</u> having a thickness of 100 nm is formed on the principal plane of the substrate 11." Ex. 1006 [0031]
"A buffer layer 33 separates the transition layers 32 from a barrier layer 34 . The buffer layer 33 is preferably formed of <u>InAlGa_N</u> with <u>any concentration of In and Al (including 0% In and/or Al)</u> and has a thickness between 0.5 and 3 μm. " Ex. 1001 at 2:63-66	"A first nitride semiconductor layer 13 of undoped <u>GaN</u> having a thickness of 2 μm." Ex. 1006 [0032]
"The barrier layer 34 is formed of <u>AlGa_N</u> and has a thickness between 0.005 and 0.03 μm and an Al percentage of about 10% to 50%." Ex. 1001 at 2:66-7:1	"a second nitride semiconductor layer 14 of undoped <u>Al_{0.15}Ga_{0.85}N</u> having a thickness of 25 nm." Ex. 1006 [0032]
" Compensated semiconductor layer 38 preferably comprises <u>AlGa_N</u> or <u>GaN</u> with a deep level passivated p-type impurity such as, for example, <u>Mg</u> , Zn, Be, Cd, or Ca." Ex. 1001 at 3:10-14	" a third nitride semiconductor layer 15 is formed which is made of <u>Al_{0.15}Ga_{0.85}N</u> doped with magnesium (<u>Mg</u>) and has a thickness of 200 nm" and "the third nitride semiconductor layer may be made of <u>GaN</u> without Al." Ex. 1006 [0033], [0054]
"A gate contact 37 , formed of for example, Ta, Ti, TiN, W, or WSi ₂ , and having a thickness of between 0.05 and 1.0 μm, is provided between the source and drain contacts." Ex. 1001 at 3:4-7	"The gate electrode 20 is made of palladium (Pd), and comes into ohmic contact with the control region 15 a." Ex. 1006 [0034]

Uemoto is very close: same layer arrangement, same description of materials & dopants

EPC disputes the Uemoto ground meets the “semi-insulating” limitation [7e], no dispute for other limitations

Not Disputed	7p	A column III Nitride transistor comprising:
Not Disputed	7a	a substrate,
Not Disputed	7b	a set of III-N transition layers above the substrate,
Not Disputed	7c	a III-N buffer layer above the set of transition layers,
Not Disputed	7d	a III-N barrier layer,
Disputed	7e	a semi-insulating III-N layer above the barrier layer, and
Not Disputed	7f	a confinement layer above the semi-insulating III-N layer.
Not Disputed	8	The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V..
Not Disputed	9	The transistor of claim 7, wherein the confinement layer is made of SiN, SiO2, Al2O3, HfO2, Ga2O3, or InAlGaN.

Semi-insulating from Smith’s co-doping (e.g., adding deep dopants)



'294 Patent	Uemoto
“ Semi-insulating layer 39 may comprise, for example, AlGaN or GaN, with deep level impurity atoms, for example, C, Fe, Mn, Cr, V, or Ni. ” Ex. 1001 at 3:57-59.	“a third nitride semiconductor layer 15 is formed which is made of $Al_{0.15}Ga_{0.85}N$ doped with magnesium (Mg) and has a thickness of 200 nm.” Ex. 1006 [0033]
“a confinement layer is placed above the semi-insulating layer and below the gate contact layer. This confinement layer can be composed of AlGaN, SiN, SiO2, or other insulating material. ” Ex. 1001 at 4:33-35	“a hydrogen diffusion film 17 for supplying hydrogen. It is sufficient that the hydrogen diffusion film 17 is deposited by, for example, a plasma enhanced CVD method and made of silicon nitride (SiN). ” Ex. 1006 [0063]

Uemoto is close: same layer arrangement, same description of materials, different doping. The patent describes “C, Fe, Mn, Cr, V, or Ni,” Uemoto describes only “Mg.” But using another dopant in Uemoto was obvious as demonstrated by the undisputed Uemoto/Smith combination

Ground 2: The ITC Opinion

ITC did not opine about the Smith grounds

	Challenged Claims	Basis	Prior Art
1A	1-12	§ 103	Smith
1B	1-12	§ 103	Smith and Kigami
1C	1-12	§ 103	Smith and Uemoto
2	1-12	§ 103	Uemoto and Smith

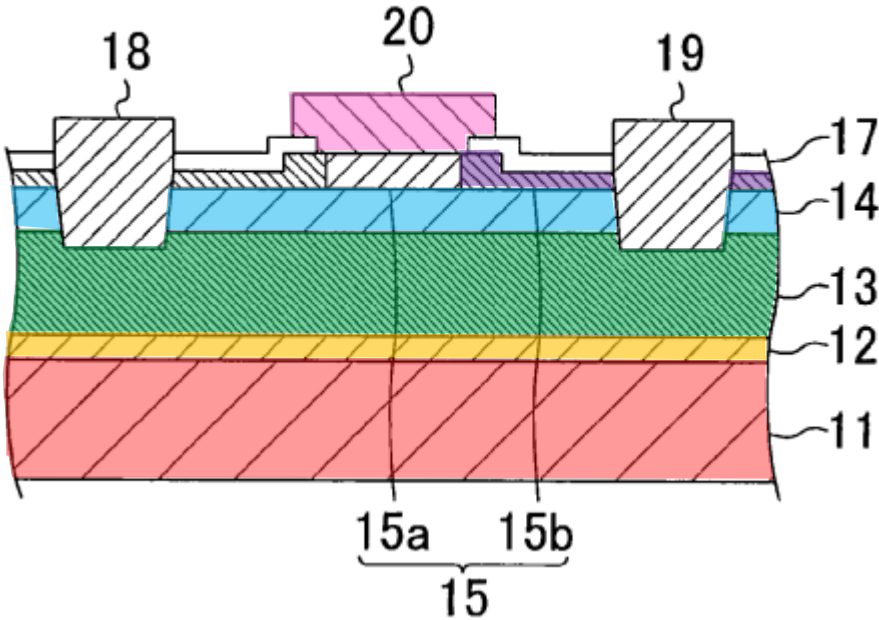
ITC opined about Uemoto by itself (without Smith) and only for claims 1-3

ITC Opinion

1p	A column III-Nitride transistor comprising:
1a	a substrate,
1b	a set of III-N transition layers above the substrate,
1c	a III-N buffer layer above the set of transition layers,
1d	a III-N barrier layer above the buffer layer,
1e	a compensated GaN layer above the barrier layer, and
1f	a gate contact above the compensated GaN layer.
2	The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
3	The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.



ITC found Uemoto *by itself* anticipated (§102) all elements in claims 1-3 but for the “set of III-N transition layers”



Applying a “clear and convincing” standard, ITC found Uemoto by itself did not meet the “set of III-N transition layers”

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

CERTAIN SEMICONDUCTOR DEVICES, AND
METHODS OF MANUFACTURING SAME AND
PRODUCTS CONTAINING THE SAME

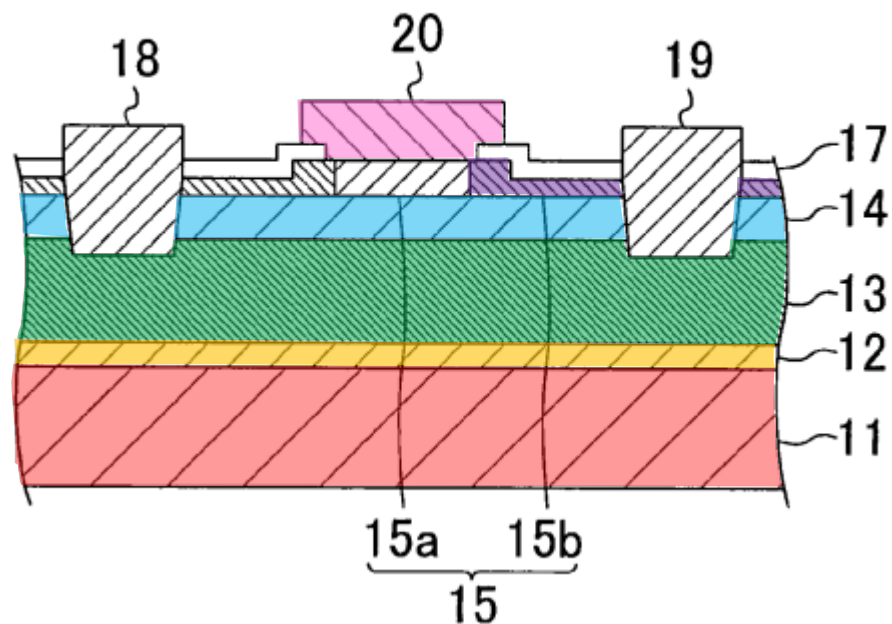
INV. NO. 337-TA-1366

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND

For all of the reasons noted in the anticipation analysis above, and after considering the objective indicia of non-obviousness discussed later, I find Uemoto does not teach or suggest transition layers. I further determine Innoscence has not met its burden to adduce “clear and convincing evidence” that an ordinary artisan at the time of the invention “would have had reason to attempt to make” the Uemoto device with the required set of transition layers. *See PharmaStem Therapeutics*, 491 F.3d at 1360. All three asserted claims of the '294 patent require the set of transition layers missing from Uemoto. Accordingly, I find Innoscence has failed to present an affirmative defense that claims 1, 2, and 3 are invalid under 35 U.S.C. § 103 as obvious in view of Uemoto.

Ex. 2022 at 87

Here ground 2 is not Uemoto by itself, Ground 2 is Uemoto + Smith using Smith to include multiple transition layers. This addresses the ALJ's concerns



To the extent *Uemoto* does not explicitly disclose [1b] (e.g., disclosing a single **buffer layer**), the combination of *Uemoto* and *Smith* renders [1b] obvious. *Shealy*, [0235]. *Smith* discloses a transistor with “strain balancing **transition layer(s)**.” *Smith*, [0070]; *supra* §VIII.D.3. As discussed above, a POSITA would have found it obvious to incorporate *Smith*’s multiple transition layers in *Uemoto*’s device, rendering [1b] obvious. *Shealy*, [0235]; *supra* §VIII.A.1.

Paper No. 1 at 70

EPC does not challenge, and waived any argument against, this Uemoto + Smith combination

The ITC found Uemoto failed to anticipate only one element [1b], but [1b] is undisputed in Ground 2 (Uemoto + Smith) and the combination is also undisputed

ITC Opinion Uemoto

1p	A column III-Nitride transistor comprising:
1a	a substrate,
1b	a set of III-N transition layers above the substrate,
1c	a III-N buffer layer above the set of transition layers,
1d	a III-N barrier layer above the buffer layer,
1e	a compensated GaN layer above the barrier layer, and
1f	a gate contact above the compensated GaN layer.
2	The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
3	The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.



Disputed Issues for Ground 2

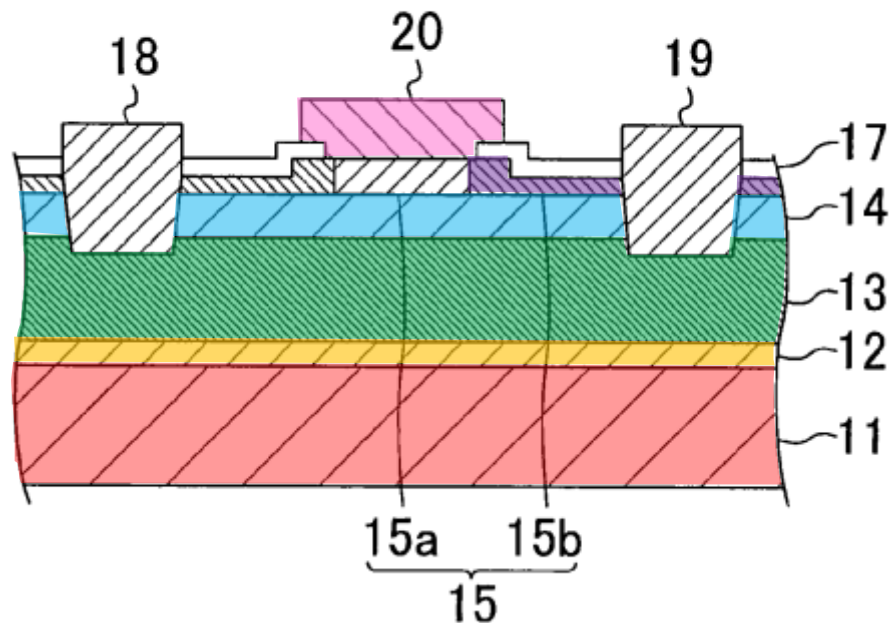
Not Disputed	1p	A column III-Nitride transistor comprising:
Not Disputed	1a	a substrate,
Not Disputed	1b	a set of III-N transition layers above the substrate,
Not Disputed	1c	a III-N buffer layer above the set of transition layers,
Not Disputed	1d	a III-N barrier layer above the buffer layer,
Disputed	1e	a compensated GaN layer above the barrier layer, and
Disputed Position	1f	a gate contact above the compensated GaN layer.
Not Disputed	2	The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
Not Disputed	3	The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.



Ground 2: 2 combinations of Uemoto with Smith

Not Disputed

Ground 2: Modifying Uemoto to include the strain balancing transition layers that Smith (incorporating Saxler015) describes prevent cracking



EPC does not dispute, and waived any argument against, the proposed use of Smith's transition layers

Smith [0070]

“Optional buffer, nucleation and/or **transition layers** (not shown) may be provided on the substrate 10. For example, an AlN buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Additionally, **strain balancing transition layer(s) may also be provided as described**, for example, in commonly assigned U.S. Patent Publication No. [Saxler015].”

Ex. 1005 ¶[0070]

1. Analogous art: Both describe III-Nitride transistors

Same transistors → Obvious to combine

2. KSR known technique applied to known device: Smith's transition layers technique for appropriate crystal structure transition.

Known technique, known device
→ Obvious to combine

3. KSR's some teaching, suggestion, motivation (TSM): Smith teaches transition layers improve robustness in devices like Uemoto's

Uemoto/Smith some TSM →
Obvious to combine

4. Reasonable expectation of success: Transition layers were conventional, POSITA had reasonable expectation of success in incorporating Smith's transition layers

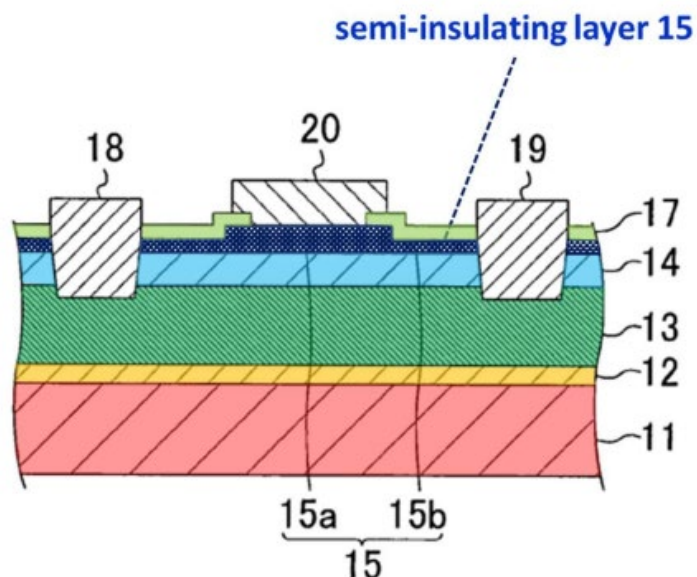
Expectation of success to include
transition layers → Obvious to
combine

5. EPC does not dispute

EPC does not dispute the combination →
Obvious to combine

Combination 2: Applying Smith's co-doping (claim 7)

Ground 2: Applying Smith's co-doping to Uemoto. Smith (incorporating Saxler874) describes co-doping as beneficial to improve predictability and minimize variations between processing runs



Smith ¶[0085] (Saxler874 ¶[0018])

Embodiments of the present invention may utilize **co-doping of a Group III nitride layer** with a shallow level dopant and a deep level dopant **to provide a predictable characteristic of a semi-insulating Group III nitride layer.**

Ex. 1005 ¶[0085] (Ex. 1016 ¶[0018])

EPC does not dispute, and waived any argument against, the proposed use of Smith's co-doping in Uemoto

1. Analogous art: Both describe III-Nitride transistors

Same transistors → Obvious to combine

2. KSR substitution of doping techniques: Substituting Uemoto's Mg doping with Smith's co-doping

Simple substitution → Obvious to combine

3. KSR's some teaching, suggestion, motivation (TSM): Smith teaches co-doping would reduce variations between runs

Uemoto/Smith some TSM → Obvious to combine

4. Reasonable expectation of success: POSITA had reasonable expectation of success in incorporating Smith's co-doping

Expectation of success to make a semi-insulating co-doped layer → Obvious to combine

5. EPC does not dispute

EPC does not dispute the combination → Obvious to combine

Ground 2: Outstanding Issues

Issue	EPC's Argument	Correct Resolution
For Claim 1: Does Uemoto's layer 15b meet the "compensated GaN"? ITC resolved	Uemoto's layer 15b is not "compensated GaN" because it does not deplete the 2DEG	As EPC's expert admitted twice, Uemoto's layer 15b is "compensated GaN." EPC's 2DEG argument is completely divorced from the claim.
For Claim 1: Does Uemoto meet the position requirement of gate contact "above" the "compensated GaN"? ITC resolved	"above" should be interpreted as being part of the "functional gate."	In Uemoto the gate is plainly "above" layer 15b. EPC's arguments is divorced from the claims and based on its improper construction.
For Claim 7: Does Uemoto/Smith disclose the "semi-insulating" layer?	Smith only teaches regions of different dopant concentrations and there is no motivation to use Saxler's co-doping in Smith	Smith expressly discloses co-doping for nitride layers, like Uemoto's layer 15, improve stability. Saxler874 is part of Smith, there is no combination.

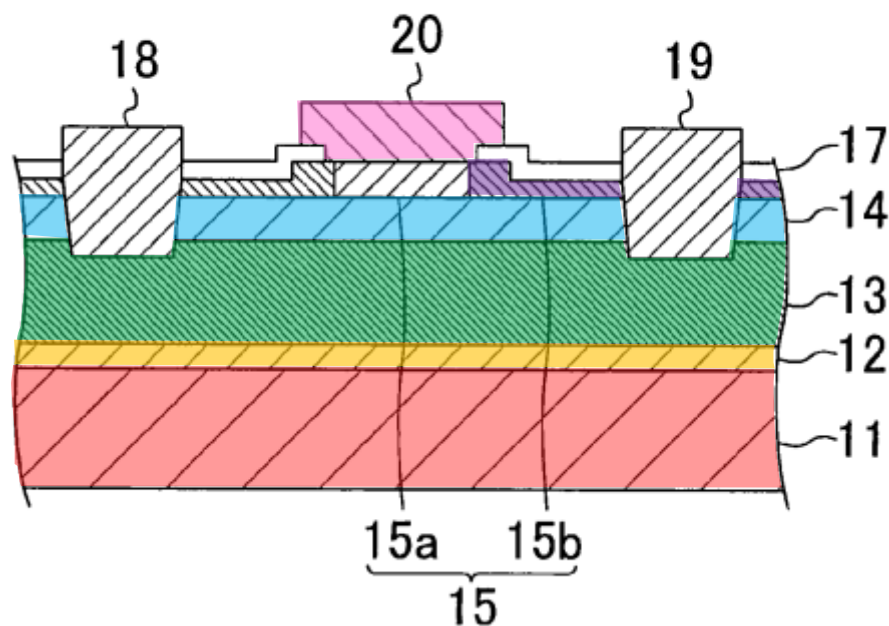
Issue 1: Uemoto's layer 15b meets "compensated GaN"

1. "Compensated GaN"

2. Position of the compensated layer

3. Semi-insulating layer

Uemoto's 15b has Mg passivated with intentionally introduced H to increase resistivity meeting "compensated GaN" under any construction



Uemoto

"a **high resistive region 15 b** in which **Mg is not activated** to offer a higher resistance than the control region 15 a."

Ex. 1006 ¶[0033]

Referring to FIG. 7, in the transistor according to the third embodiment, the top of the third nitride semiconductor layer 15 is formed with not a hydrogen diffusion barrier film but a hydrogen diffusion film 17 for supplying hydrogen.... **hydrogen from the hydrogen diffusion film 17 is supplied** during a thermal treatment **for selectively inactivating impurities.**

Ex. 1006 ¶[0063]

As EPC's expert admitted Uemoto's 15b has Mg and H, is passivated, and is non-conductive: "it meets the claim term compensated gallium nitride"

EPC's expert admitted 15b admission that 15b is claimed compensated GaN

EPC's expert at ITC Hearing

THE WITNESS: Your Honor, I would express it in a slightly different way.

CHIEF JUDGE CHENEY: Please do.

THE WITNESS: So layer 15b is gallium nitride, contains magnesium and hydrogen, is passivated, and is non-conductive. So in that sense, it meets the claim term "compensated gallium nitride."

But its location is in the wrong place. Layer 15b is in the wrong place. It should be in a different place if it would serve as the compensated gallium nitride layer that is claimed in the '294 patent.

Ex. 2017, 1034:1-7

1. "Compensated GaN"

2. Position of the compensated layer

3. Semi-insulating layer

**As EPC's expert admitted again Uemotos' 15b has Mg passivated with H:
"that's the compensated gallium nitride layer"**

**EPC's expert admitted 15b
is the compensated GaN
"we're looking for"**

EPC's expert at ITC Hearing

Now, we can -- we can focus in on layer 15B and say, let us look at layer 15B in isolation. Let us disconsider the surroundings and let us just look what layer 15B is and layer 15B is gallium nitride. It is doped with magnesium and it is passivated by hydrogen. So if we look at layer 15B in isolation then one could say that's the compensated gallium nitride layer we're looking for. However, in my opinion we cannot look at layer 15B in isolation.

Ex. 2016, 964:1-7

1. "Compensated GaN"

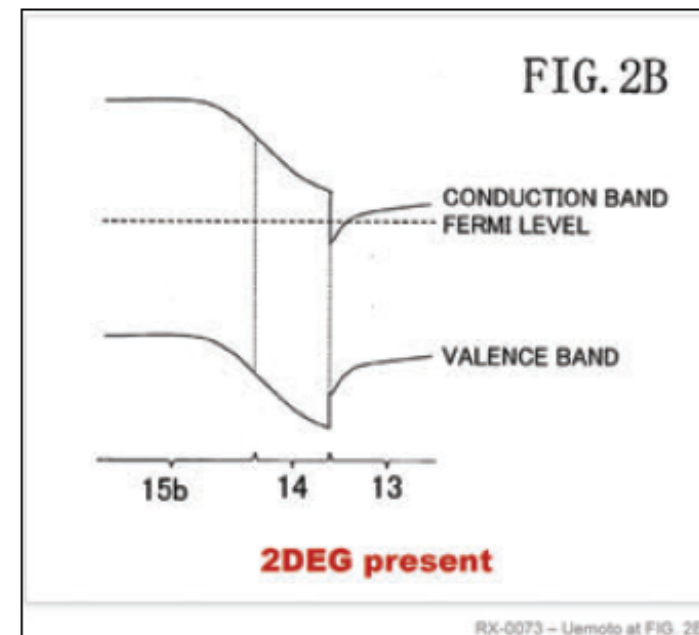
2. Position of the compensated layer

3. Semi-insulating layer

EPC's Incorrect Argument

By contrast, as shown in Figure 2B of *Uemoto* below, the Fermi level of high resistive region 15b, which Petitioner alleges corresponds to the compensated GaN layer of claim 1, is in the conduction band. Ex. 2016 at 961:22-962:21. This means that the 2DEG is present and not depleted under high resistive region 15b,

Paper No. 18 at 51



Uemoto at FIG. 2B (annotated)

EPC's 2DEG distinction contradicts its own expert admission that layer 15b is the compensated GaN ...

... but nothing in the claim requires a 2DEG functionality, the claim does not require the "compensated GaN" have no 2DEG

EPC's argument Uemoto's 15b does not deplete 2DEG

Incorrect

1. "Compensated GaN"

2. Position of the compensated layer

3. Semi-insulating layer

As the ITC judge concluded, EPC's 2DEG requirement is not required by the claim, based on an improper construction, and irrelevant because "claim 1 does not recite a particular manner of operating the transistor"

CALJ's Opinion

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

CERTAIN SEMICONDUCTOR DEVICES, AND
METHODS OF MANUFACTURING SAME AND
PRODUCTS CONTAINING THE SAME

INV. NO. 337-TA-1366

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND

Chief Administrative Law Judge Clark S. Cheney

(July 5, 2024)

characteristics"). Claim 1 does not recite a particular manner of operating the transistor it claims.

Thus, even if Dr. Schubert is correct that the transistor of Uemoto operates differently than the transistors disclosed in the '294 patent, "[i]t is well settled" that the relevant question for anticipation is whether the claimed structure was known, not whether the prior art shows the claimed structure being used for a particular function. See *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

Considering the plain and ordinary meaning of "compensated GaN," the intrinsic evidence cited by the parties, expert testimony, and the arguments of the parties, I find Innoscence has shown that Uemoto discloses limitation [1e].

Ex. 2022 at 81

Issue 2: Uemoto's meets position requirement

1. "Compensated GaN"

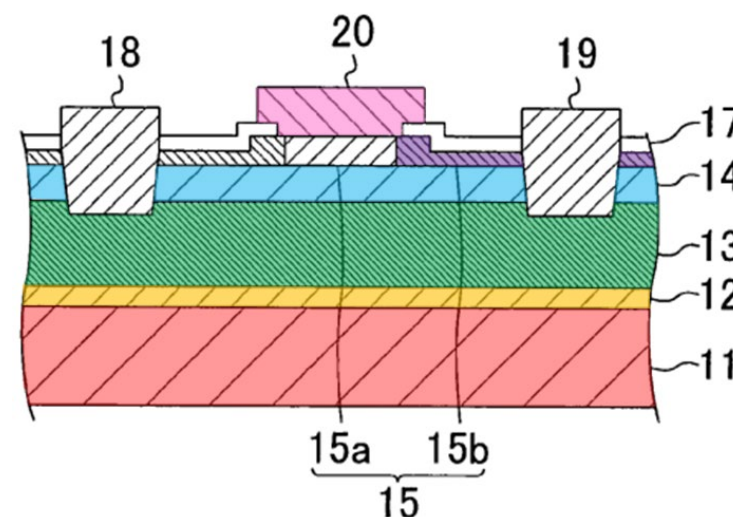
2. Position of the compensated layer

3. Semi-insulating layer

In Uemoto the "Gate electrode 20" is plainly above layer 15b. In Uemoto [1f]: "a gate contact [gate electrode 20] above the compensated GaN layer [layer 15b]."



Ex. 1027 at 3

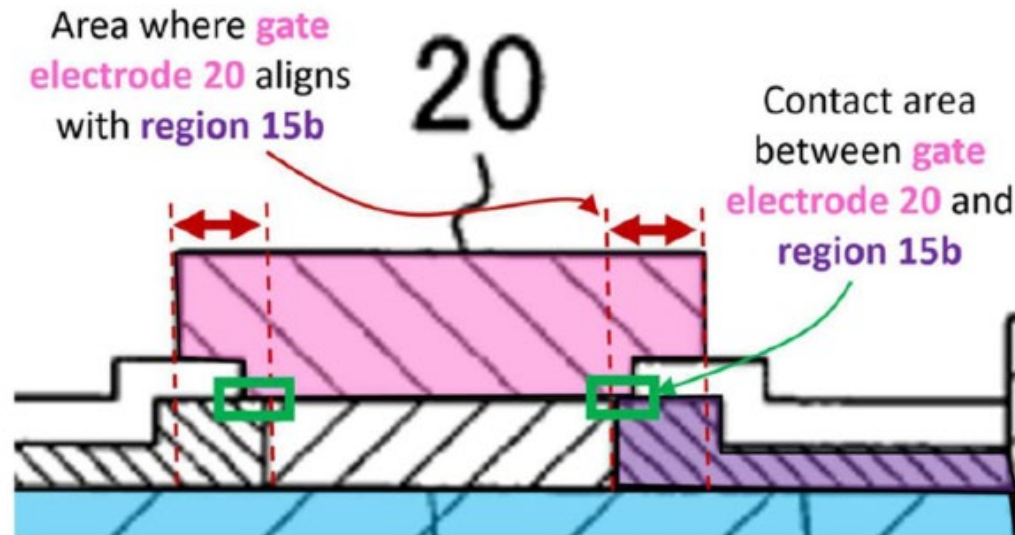


Just like the ball is above the table,
gate electrode 20 is above layer 15b

Uemoto's 15b is even, partially, directly below and in contact

1. "Compensated GaN"
2. Position of the compensated layer
3. Semi-insulating layer

Uemoto describes **gate electrode 20**—at least partially—directly on top and in contact with **region 15b**.

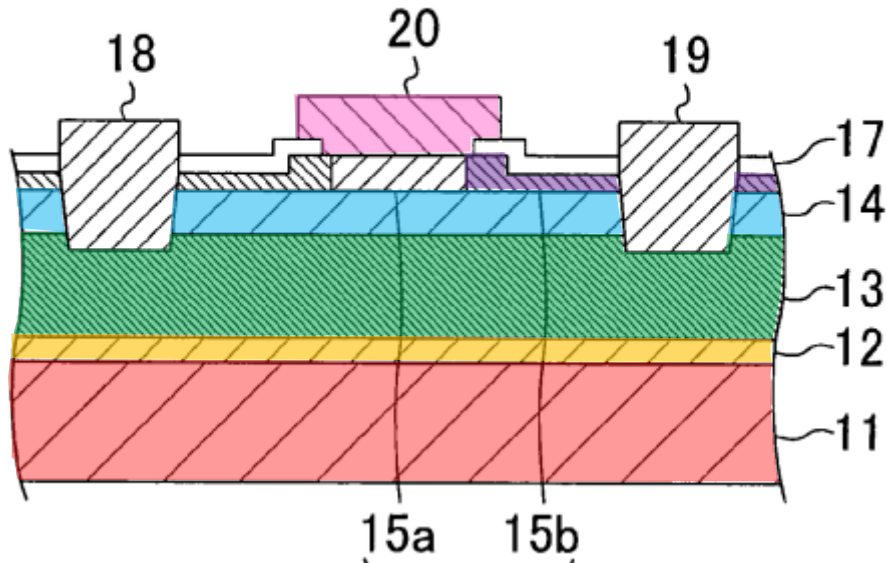


Not required in the claim, but in addition to disclosing gate electrode 20 “above” layer 15b, Uemoto also shows 20 directly on top and in contact with 15b

EPC's expert admits gate electrode is above 15b

1. "Compensated GaN"
2. Position of the compensated layer
3. Semi-insulating layer

EPC's expert admits gate electrode 20 is above region 15b (even if a small region)



There is no need for "narrative support" and arguments about functionality are divorced from the claim

EPC's expert at ITC Hearing

The 2DEG is present underneath 15B, which is the opposite of what is being taught by the '294 patent and the last bullet point concerns Dr. Lebby's magnified image where he magnifies a particular region of Uemoto and he says at this particular location, at this particular location if we look at the physical structure, and if we look at the structure, the gate electrode is above a small region of layer 15B and so I would say there is a very small region or a sliver of region 15B that Dr. Lebby identifies being under the gate electrodes 20 and I have two points about that.

The first one is I do not see narrative support in Uemoto for that suggestion and also the claim requires that there is a compensated gallium nitride layer below the gate electrodes and a person of skill in the art would not identify this tiny region, this sliver of being a layer as claimed in the '294 patent.

Ex. 2016 at 965:3-19

1. "Compensated GaN"

2. Position of the compensated layer

3. Semi-insulating layer

Well-settled, going even back to CCPA and in the MPEP, that features shown in prior art drawings need not be described in the specification to be prior art disclosure



When the reference is a utility patent, ***it does not matter that the feature shown is unintended or unexplained in the specification***. The drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art. *In re Aslanian*, 590 F.2d 911, 200 USPQ 500 (CCPA 1979).

Manual of Patent Examining Procedure (MPEP) §2125 (Drawings as Prior Art)

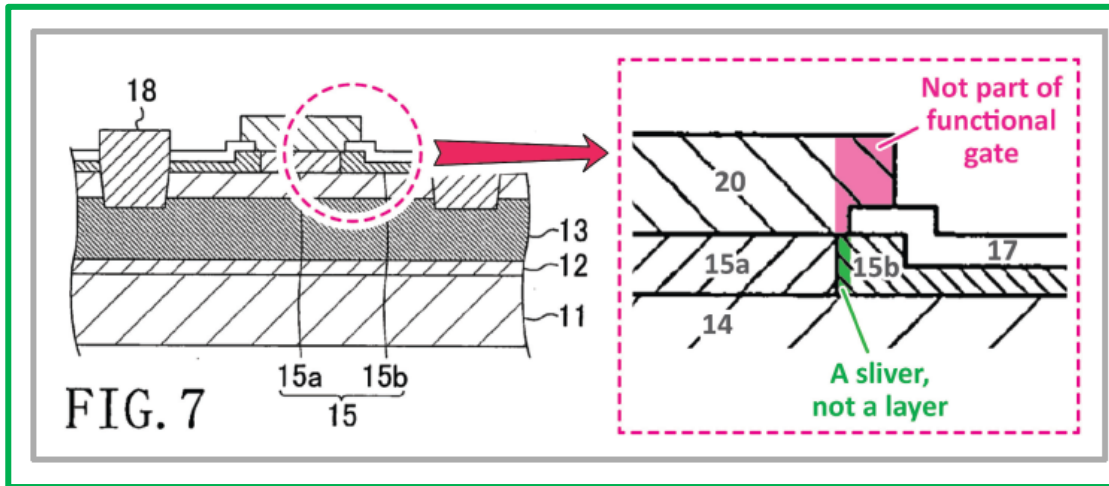
EPC's argument layer 15b is not part of the "functional" gate

Incorrect

1. "Compensated GaN"
2. Position of the compensated layer
3. Semi-insulating layer

As the ITC Judge concluded, EPC's "functional gate" distinction is "not persuasive" because the claim only requires one layer "above" the other; the claim is directed to structure, not function

EPC Incorrect Argument



Paper No. 32 at 21

CALJ's Opinion

vs.

EPC's position is not persuasive. Figure 7 of Uemoto shows that layer 20 is located on a higher plane than layer 15b, and the two layers are visibly in contact. EPC's own expert Dr. Schubert also admitted that "if we look at the structure, the gate electrode is above a small region of layer 15B" in Uemoto. See Tr. at 965:3-13 (Schubert). Nothing in Uemoto casts any doubt on the positional relationship between gate contact 20 and GaN layer 15b shown in Figure 7.

Ex. 2022 at 83

Even EPC's drawing shows electrode 20 is above layer 15b, EPC's arbitrary distinction of "functional gate" is not borne in the record

Uemoto does not disclose semi-insulating, but Smith discloses a method for forming cap layers with co-doping: a “method[] of fabricating Semi-insulating Group III nitride layers.”

Smith [0085]

...the doped region 40 is doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co. The dopant may be incorporated into the **cap layer 34** during deposition or growth of the cap layer 34, 34' ... Techniques for co-doping Group III-nitride materials are described, for example, in U.S. patent application Ser. No. [Saxler874], filed Jan. 7, 2004 entitled “**CO-DOPING FOR FERMIL LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES**,” the disclosure of which is incorporated herein as if set forth in its entirety.

Ex.1005 ¶[0085]

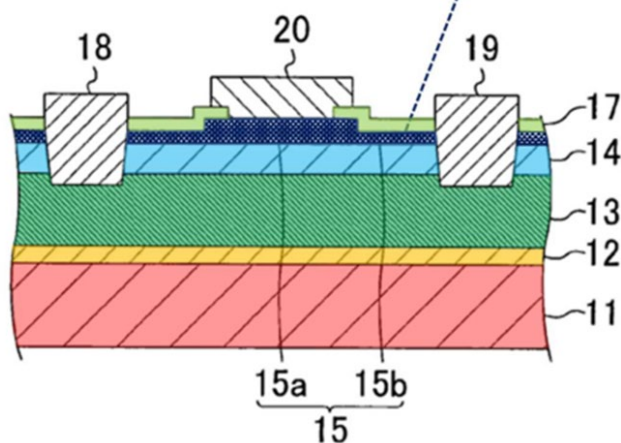
Saxler874 [0005]

Embodiments of the present invention provide Semi-insulating Group III nitride Semiconductor layers and **methods of fabricating Semi-insulating Group III nitride layers.**

Ex.1016 ¶[0005]

As Dr. Shealy explains, to a POSITA it was obvious to use Smith's co-doping in Uemoto to "form a stable semi-insulating layer"

Semi-insulating from Smith's co-doping (e.g., adding deep dopants)



EPC doesn't argue against the combination or the motivation to combine

[0224] In my opinion, a person of ordinary skill in the art would have acknowledged that *Smith's* process doping techniques to form a stable semi-insulating layer would be advantageous to *Uemoto*. *Uemoto* also aims to reduce leakage current and improve the device's fabrication. *Uemoto*, [0061], [0079]. A person of ordinary skill in the art would have identified that the leakage and fabrication improvements *Smith* discloses with its semi-insulating layers would be beneficial and applicable to *Uemoto*. In my opinion, a person of ordinary skill in the art would have identified *Uemoto's* transistor as a base device that would be improved with *Smith's* teachings. And a person of ordinary skill in the art would have recognized that *Smith's* doping methods could be applied in *Uemoto*, because both references disclose the same materials and similar structure.

Ex. 1033 ¶[0224]

EPC argues Smith's co-doping is different than Saxler874's and Innoscence did not provide a motivation to apply Saxler874 to Smith

EPC's description of Saxler874 co-doping

The portion of *Saxler874* on which the Petitioner relies does not state or suggest that any type of co-doping results in a semi-insulating Group III nitride layer, as Petitioner implies. Rather, in [0005], *Saxler874* discloses:

Embodiments of the present invention provide semi-insulating Group III nitride semiconductor layers and methods of fabricating semi-insulating Group III nitride layers. In certain embodiments of the present invention, fabrication of a semi-insulating Group III nitride layer includes doping a Group III nitride layer with a shallow level p-type dopant and doping the Group III nitride layer with a deep level dopant.

To the extent this disclosure teaches creating a semi-insulating layer using co-doping, a POSA would understand this disclosure to mean that co-doping a shallow level p-type dopant and a deep level dopant is what would result in the semi-insulating layer. Ex. 2009 at ¶ [189].

Paper No. 18 at 18-19

EPC notes Saxler874 teaches making a semi-insulating layer

EPC's description of Smith co-doping

Conversely, in the context of ¶ [0085], where *Smith* incorporates *Saxler874* by reference, *Smith* at most teaches regions of different dopant concentrations ("In such a case, the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34''"). There is no suggestion that a p-type dopant be co-doped with a deep level dopant. And Petitioner has provided no motivation as to why a POSA would use that type of co-doping in *Smith*. Ex. 2009 at ¶ [190].

Paper No. 18 at 19

EPC believes Saxler874 would need to be combined with Smith

But Saxler874 & Smith are the same

1. Smith discloses Compensated GaN layer

2. Smith discloses Semi-insulating layer

Saxler874 and Smith cannot disclose different co-doping because they are the same. There is no need to modify Smith with Saxler874 for a semi-insulating cap; Smith incorporates Saxler874's co-doping for semi-insulating cap layers

Smith [0085]

Techniques for **co-doping Group III-nitride materials** are described, for example, in U.S. patent application Ser. No. 10/752,970 [**Saxler874**], filed Jan. 7, 2004 entitled "CO-DOPING FOR FERMI LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES," the disclosure of which is **incorporated herein as if set forth in its entirety**.

Ex. 1005 ¶[0085]



"Incorporation by reference provides 'a method for integrating material from various documents into a host document[. . . by citing such material in a manner that makes clear that the material is **effectively part of the host document as if it were explicitly contained therein**.'

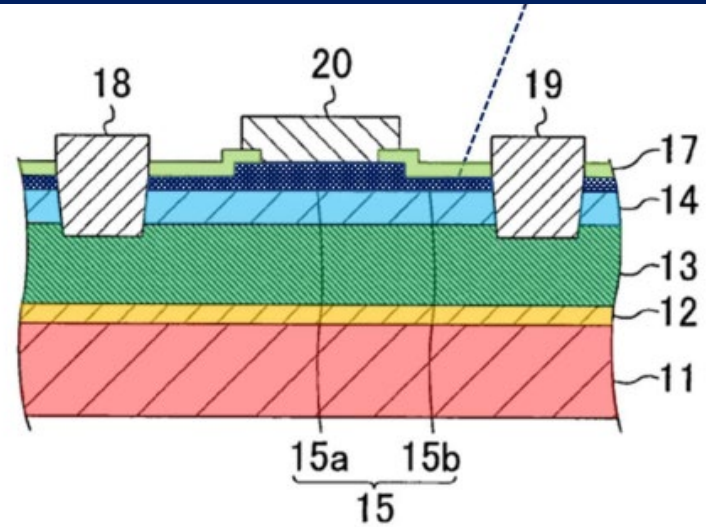
Advanced Display Sys., Inc. v. Kent State Univ., 212 F.3d 1272, 1282 (Fed. Cir. 2000)."

Paice LLC v. Ford Motor Co., 881 F.3d 894, 906–07 (Fed. Cir. 2018)

Smith (incorporating Saxler874) expressly teaches co-doping that results in a semi-insulating layer and there is no dispute about the application of Smith to Uemoto

Not Disputed	7p	A column III Nitride transistor comprising:	✓
Not Disputed	7a	a substrate,	✓
Not Disputed	7b	a set of III-N transition layers above the substrate,	✓
Not Disputed	7c	a III-N buffer layer above the set of transition layers,	✓
Not Disputed	7d	a III-N barrier layer,	✓
Disputed	7e	a semi-insulating III-N layer above the barrier layer, and	⊗
Not Disputed	7f	a confinement layer above the semi-insulating III-N layer.	✓
Not Disputed	8	The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V..	✓
Not Disputed	9	The transistor of claim 7, wherein the confinement layer is made of SiN, SiO2, Al2O3, HfO2, Ga2O3, or InAlGaN.	✓

Semi-insulating from Smith's co-doping (e.g., adding deep dopants)



Uemoto/Smith meet the only disputed limitation

Issue	EPC's Argument	Correct Resolution
For Claim 1: Does Uemoto's layer 15b meet the "compensated GaN"?	Uemoto's layer 15b is not "compensated GaN" because it does not deplete the 2DEG	As EPC's expert admitted twice, Uemoto's layer 15b is "compensated GaN." EPC's 2DEG argument is completely divorced from the claim.
For Claim 1: Does Uemoto meet the position requirement of gate contact "above" the "compensated GaN"?	"above" should be interpreted as being part of the "functional gate."	In Uemoto the gate is plainly "above" layer 15b. EPC's arguments is divorced from the claims and based on its improper construction.
For Claim 7: Does Uemoto/Smith disclose the "semi-insulating" layer?	Smith only teaches regions of different dopant concentrations and there is no motivation to use Saxler's co-doping in Smith	Smith expressly discloses co-doping for nitride layers, like Uemoto's layer 15, improve stability. Saxler874 is part of Smith, there is no combination.

ITC resolved

ITC resolved

Yes. Even EPC expert admitted

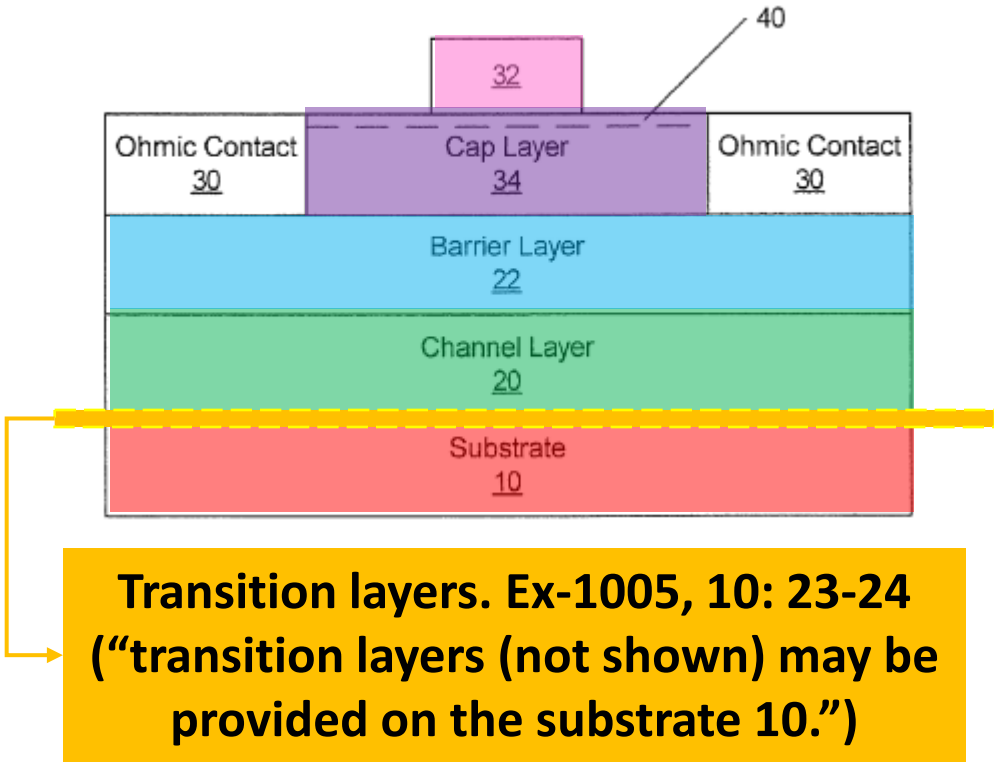
Yes. Electrode 20 is plainly "above" 15b

Yes. Combination's co-doping makes the layer semi-insulating

Ground 1: Overview & Disputed Elements

Not Disputed	1p	A column III-Nitride transistor comprising:
Not Disputed	1a	a substrate,
Not Disputed	1b	a set of III-N transition layers above the substrate,
Not Disputed	1c	a III-N buffer layer above the set of transition layers,
Not Disputed	1d	a III-N barrier layer above the buffer layer,
Disputed	1e	a compensated GaN layer above the barrier layer, and
Not Disputed	1f	a gate contact above the compensated GaN layer.
Not Disputed	2	The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
Not Disputed	3	The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.

EPC disputes the Smith grounds meet the “compensated GaN” limitation, no dispute in other limitations



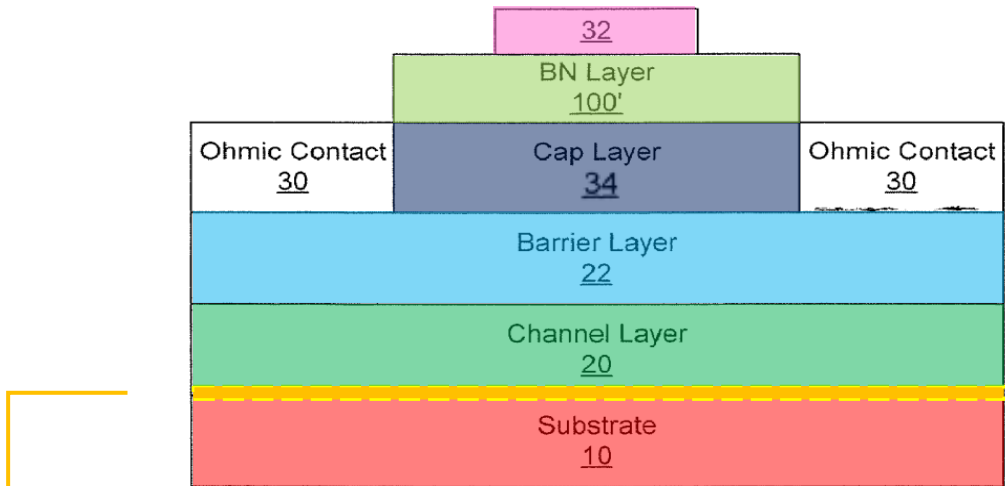
Smith discloses the same materials/doping for each element

'294 Patent	Smith
"a substrate 31 that may comprise, for example, silicon Si, silicon carbide <u>SiC</u> or sapphire." Ex. 1001 at 2:57-59	" substrate 10 is provided on which nitride based devices may be formed. In particular embodiments of the present invention, the substrate 10 may be a semi-insulating <u>silicon carbide (SiC)</u> substrate that may be, for example, 4H polytype of silicon carbide." Ex. 1005 [69]
" Transition layers 32 may comprise, for example, <u>AlN</u> or AlGaN, with a thickness of between 0.1 to 1.0 μm ." Ex. 1001 at 1:56-2:2	"Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate 10 . For example, an <u>AlN</u> buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Additionally, strain balancing transition layer(s) may also be provided as described, for example, in commonly assigned U.S. Patent Publication No. 2003/0102482A1." Ex. 1005 [0070]
"A buffer layer 33 separates the transition layers 32 from a barrier layer 34 . The buffer layer 33 is preferably formed of <u>InAlGaN</u> with <u>any concentration of In and Al (including 0% In and/or Al)</u> and has a thickness between 0.5 and 3 μm ." Ex. 1001 at 2:63-66	"the channel layer 20 is a Group III-nitride, such as <u>$\text{Al}_x\text{Ga}_{1-x}\text{N}$ where $0 \leq x < 1$</u> , provided that the energy of the conduction band edge of the channel layer 20 is less than the energy of the conduction band edge of the barrier layer 22 at the interface between the channel and barrier layers . In certain embodiments of the present invention, $x=0$, indicating that the channel layer 20 is <u>GaN</u> . The channel layer 20 may also be other Group III-nitrides such as InGaN, <u>AlInGaN</u> or the like." Ex. 1005 [0074]
"The barrier layer 34 is formed of <u>AlGaN</u> and has a thickness between 0.005 and 0.03 μm and an Al percentage of about 10% to 50%." Ex. 1001 at 2:66-7:1	"the barrier layer 22 is AlN, AlInN, <u>AlGaN</u> or AlInGaN with a thickness of between about 0.1 nm and about 40 nm." Ex. 1005 [0075]
" Compensated semiconductor layer 38 preferably comprises <u>AlGaN</u> or <u>GaN</u> with a deep level passivated p-type impurity such as, for example, <u>Mg, Zn, Be, Cd, or Ca</u> ." Ex. 1001,3:10-14	"The cap layer 34, 34' may be a <u>GaN</u> based cap layer, such as a <u>GaN</u> layer and/or an <u>AlGaN</u> layer as described, for example, in the patents and patent application incorporated by reference herein. In some embodiments of the present invention, the doped region 40 is doped with p-type dopant, such as <u>Mg, Be, Zn, Ca and/or C</u> ." Ex. 1005 [0085]
"A gate contact 37 , formed of for example, Ta, Ti, TiN, <u>W</u> , or <u>WSi₂</u> , and having a thickness of between 0.05 and 1.0 μm , is provided between the source and drain contacts." Ex. 1001 at 3:4-7	"The gate contact 32 may also be formed on the cap layer 24' as illustrated in FIG. 1B and may be fabricated using conventional fabrication techniques. ... conventional materials capable of making a Schottky contact to a nitride based semiconductor material may be used, such as Ni, Pt, NiSix, Cu, Pd, Cr, <u>W</u> and/or <u>WSiN</u> ." Ex. 1005 [0082]

Smith is very close: same layer arrangement, same description of materials & dopants

Not Disputed	7p	A column III Nitride transistor comprising:
Not Disputed	7a	a substrate,
Not Disputed	7b	a set of III-N transition layers above the substrate,
Not Disputed	7c	a III-N buffer layer above the set of transition layers,
Not Disputed	7d	a III-N barrier layer,
Disputed	7e	a semi-insulating III-N layer above the barrier layer, and
Not Disputed	7f	a confinement layer above the semi-insulating III-N layer.
Not Disputed	8	The transistor of claim 7, wherein the semi-insulating III-N layer contains deep acceptor type dopant atoms selected from the group consisting of C, Fe, Mn, Cr and V..
Not Disputed	9	The transistor of claim 7, wherein the confinement layer is made of SiN, SiO2, Al2O3, HfO2, Ga2O3, or InAlGaN.

EPC disputes the Smith grounds meet the “semi-insulating” limitation [7e], no dispute for other limitations



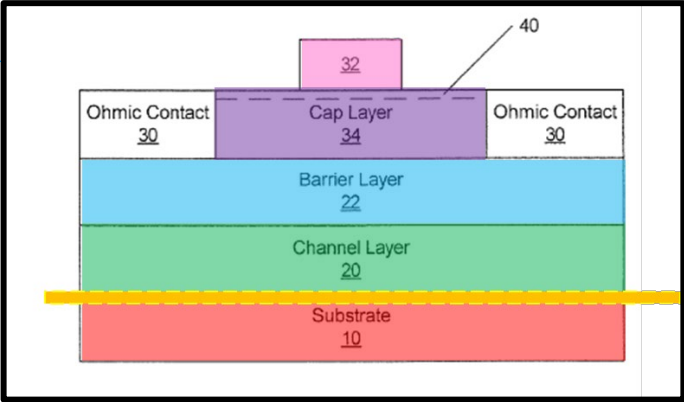
Transition layers. Ex-1005, 10: 23-24

'294 Patent	Smith
“Semi-insulating layer 39 may comprise, for example, AlGa_N or Ga_N, with deep level impurity atoms, for example, <u>C, Fe, Mn, Cr, V, or Ni.</u>” Ex. 1001 at 3:57-59.	“The cap layer 34, 34' may be a <u>GaN</u> based cap layer, such as a <u>GaN</u> layer and/or an <u>AlGa_N</u> layer as described, for example, in the patents and patent application incorporated by reference herein. In some embodiments of the present invention, the doped region 40 is doped with p-type dopant, such as Mg, Be, Zn, Ca and/or C ... In further embodiments of the present invention, the doped region 40 is doped with a deep level dopant, such <u>as Fe, C, V, Cr, Mn, Ni and/or Co.</u>” Ex. 1005 [0089] “the doped region 40 may be provided by a region of increased dopant concentration over the concentration of dopant in the remainder of the cap layer 34, 34'. Techniques for co-doping Group III-nitride materials are described, for example, in U.S. patent application Ser. No. <u>10/752,970</u> filed Jan. 7, 2004 entitled '<u>CO-DOPING FOR FERMİ LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES.</u>'” Ex. 1005 [0085]
“a confinement layer is placed above the semi-insulating layer and below the gate contact layer. This confinement layer can be composed of AlGa_N, <u>SiN, SiO₂, or other insulating material.</u>” Ex. 1001 at 4:33-35	“the graphitic BN passivation layer 100, 100' is a non-single crystal layer. The graphitic and/or amorphous BN passivation layer 100, 100' may be provided as a single layer or may be multiple layers and may be incorporated with layers of other materials, such as <u>SiN or SiO_x.</u>” Ex. 1005 [0090]

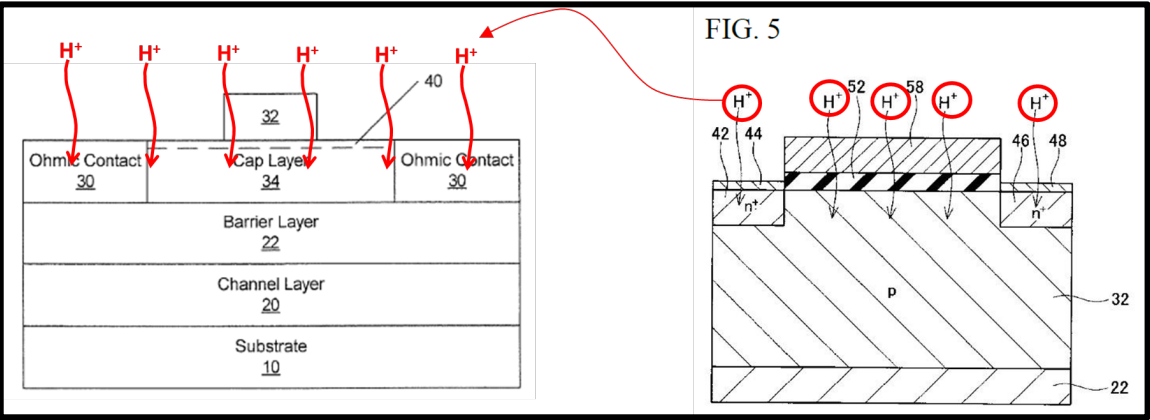
Smith is very close: same layer arrangement, same description of materials, dopants

Grounds	Challenged Claims	Basis	Prior Art
1A	1-12	§ 103	Smith
1B	1-12	§ 103	Smith and Kigami
1C	1-12	§ 103	Smith and Uemoto
2	1-12	§ 103	Uemoto and Smith

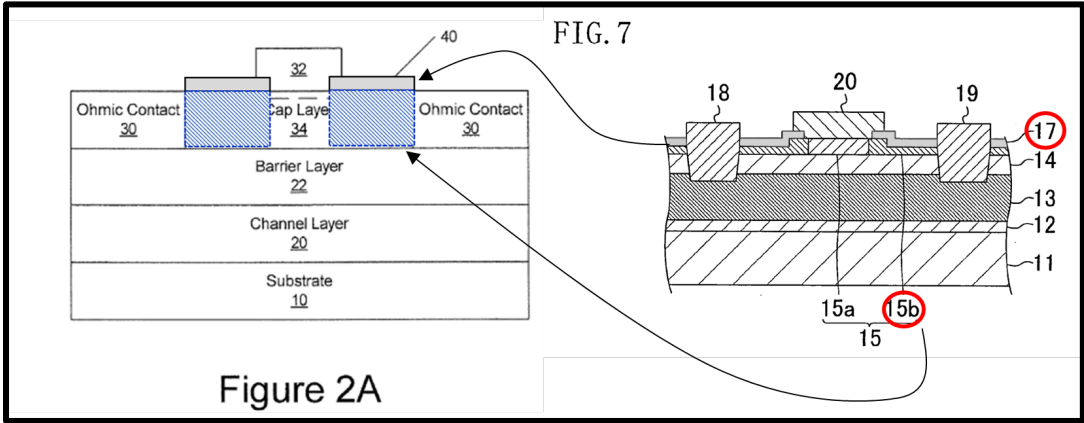
1A: Smith “as grown”



1B: Smith + Kigami’s hydrogenation



1C: Smith + Uemoto’s resistive regions



Ground 1A: Smith + POSITA's knowledge

Issue	EPC's Argument	Correct Resolution
Claim 1: Does Smith meet the "compensated GaN layer"?	Smith does not disclose compensation, and POISTA would "likely have included an anneal/activation" to remove H	POSITA knew Smith's cap layer 34 would be H passivated "as-grown," meeting the "compensated GaN" constructions. Smith does not support EPC's speculation of a "likely" activation
Claim 7: Does Smith meet the "semi-insulating III-N layer"?	Smith's co-doping only teaches regions of different dopant concentrations and there is no motivation to use Saxler874's co-doping in Smith	Smith and Saxler874 teach the same co-doping that expressly makes cap layer semi-insulating. Saxler874 is part of Smith it is not a combination that requires motivation to combine.

1. Smith discloses Compensated GaN layer

2. Smith discloses Semi-insulating layer

Jpn. J. Appl. Phys. Vol. 31 (1992) pp. 1258–1266
Part 1, No. 5A, May 1992

Hole Compensation Mechanism of P-Type GaN Films

Shuji NAKAMURA, Naruhito IWASA, Masayuki SENO and Takashi MUKAI

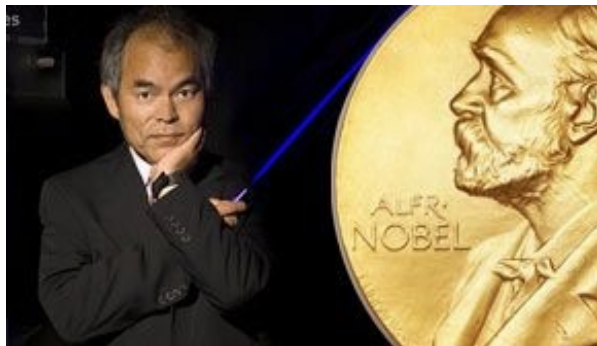
Nichia Chemical Industries, Ltd., 491 Oka, Kaminaka, Anan, Tokushima 774

(Received January 13, 1992; accepted for publication February 15, 1992)

Low-resistivity p-type GaN films, which were obtained by N₂-ambient thermal annealing or low-energy electron-beam irradiation (LEEBI) treatment, showed a resistivity as high as $1 \times 10^6 \Omega \cdot \text{cm}$ after NH₃-ambient thermal annealing at temperatures above 600°C. In the case of N₂-ambient thermal annealing at temperatures between room temperature and 1000°C, the low-resistivity p-type GaN films showed no change in resistivity, which was almost constant between $2 \Omega \cdot \text{cm}$ and $8 \Omega \cdot \text{cm}$. These results indicate that atomic hydrogen produced by NH₃ dissociation at temperatures above 400°C is related to the hole compensation mechanism. A hydrogenation process whereby acceptor-H neutral complexes are formed in p-type GaN films was proposed. The formation of acceptor-H neutral complexes causes hole compensation, and deep-level and weak blue emissions in photoluminescence.

KEYWORDS: p-type GaN, thermal annealing, hydrogenation, atomic hydrogen, Hall measurement, photoluminescence

Ex. 1018 at 1



POSITA knew, since the 90s, reported by Nobel prize winner Nakamura: “as-grown” GaN films are already hydrogen passivated.

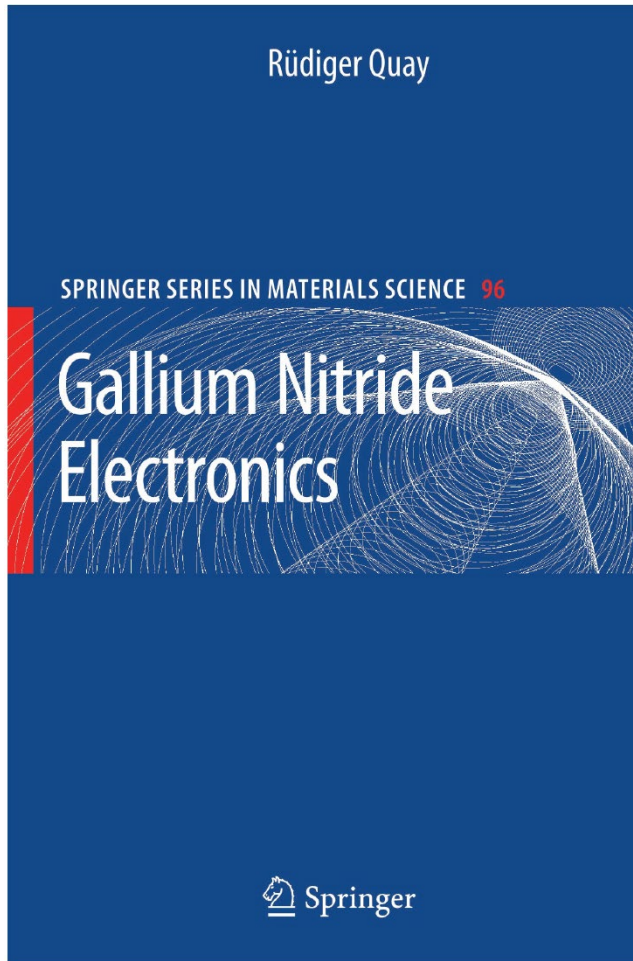
11(c) and 11(a)). Therefore, it is speculated that **as-grown GaN films are hydrogen passivated**, and the above-mentioned proposal of the hydrogenation process occurs during GaN growth by means of MOCVD. The resistivities of Mg-doped GaN films of Figs. 11(a), 11(b) and 11(c) were $1 \times 10^6 \Omega \cdot \text{cm}$, $2 \Omega \cdot \text{cm}$ and $1000 \Omega \cdot \text{cm}$, respectively. The resistivity of the sample in Fig. 11(c) is smaller in comparison than that of Fig. 11(a). It is probable that the hydrogenation process is not perfect, i.e., hydrogen passivation may only occur near the immediate surface of GaN film because diffusion of atomic hydrogen from the surface into the bulk is minimal. If optimum conditions for microwave plasma treatment in hydrogen passivation of p-type GaN films can be found, resistivity will become higher.

Ex. 1018 at 10

“As-grown” passivation well-known even in textbooks

1. Smith discloses Compensated GaN layer

2. Smith discloses Semi-insulating layer



Ex. 1011 at 1

Firmly established (even in 2008 textbook) that p-GaN grown with MOCVD results in “as grown” H passivated layers.

cies is also discussed in [3.160]. It has further been found in GaN and the related materials AlN, InN, InGaN, InAlN, AlGaIn, that hydrogen is present in relatively high concentrations in as-grown samples, especially in p-type GaN [3.148]. It has been shown experimentally that the amount of oxygen present during material growth can have a strong influence on the background conductivity, indicating that it is a shallow donor in GaN. Carbon can also be a significant residual impurity in MOCVD-grown nitrides. Its

Ex. 1011 at 135

- Large thermal activation energy of 120–200 meV [3.54]
- Hydrogen passivation of MOCVD-grown GaN:Mg [3.143, 3.160] and
- Significant Mg reactor memory leading to broad Mg profiles, reported, e.g., in [3.62, 3.186]

Ex. 1011 at 136

Smith expressly discloses growing cap layer 34 with “MOCVD-grown GaN:Mg.” Smith [0087]

1. Smith discloses Compensated GaN layer 2. Smith discloses Semi-insulating layer

POSITA knew Smith’s “as-grown” cap layer would be H passivated meeting the “cancels the electrical effects” construction

Broader than Petitioner and Patent Owner

Claim Term	Petitioner	Patent Owner	ITC
“Compensated GaN Layer”	“a doped GaN layer formed with a step to passivate its impurities”	“a semiconductor GaN gate material in which one type of impurity (for example, donor) cancels the electrical effects of the other type of impurity (for example, acceptor).”	“a GaN layer in which one type of impurity cancels the electric effects of another type of impurity ”

- Smith’s cap layer is p-GaN grown MOCVD (making it H passivated “as-grown”)
- Smith’s cap layer “as grown” is a layer in which “one type of impurity” **(the innate H)** cancels the electrical effects of another type of impurity **(the passivated dopant)**.

EPC's speculation Smith requires activation

Incorrect

1. Smith discloses Compensated GaN layer

2. Smith discloses Semi-insulating layer

As the Board noted, EPC's speculation of required activation contradicts Smith description of an optional process

Trials@uspto.gov
571-272-7822

Paper 11
Date: March 20, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY MCGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

As noted by Patent Owner, Smith discloses embodiments in which a passivation layer, such as the MgN passivation layer disclosed in U.S. Patent No. 6,498,111, is provided on the transistors depicted in Figures 1A and 1B of Smith and an optional annealing step is performed in the presence of oxygen to remove hydrogen. Ex. 1005 ¶ 83. Smith's disclosure that the annealing step to remove hydrogen is optional, however, tends to cut against Patent Owner's argument that one of ordinary skill in the art would have necessarily sought to remove any hydrogen present in cap layer 34 from the embodiments depicted in Figures 2A and 2B. *Id.*

Paper No. 11 at 19

Paper No. 26 at 13

EPC's speculation Smith requires activation

Incorrect

1. Smith discloses Compensated GaN layer

2. Smith discloses Semi-insulating layer



US 20070164315A1

(19) **United States**
(12) **Patent Application Publication** (10) **Pub. No.: US 2007/0164315 A1**
Smith et al. (43) **Pub. Date: Jul. 19, 2007**

(54) **CAP LAYERS INCLUDING ALUMINUM NITRIDE FOR NITRIDE-BASED TRANSISTORS AND METHODS OF FABRICATING SAME**

(75) **Inventors:** Richard Peter Smith, Carrboro, NC (US); Adam William Saxler, Durham, NC (US); Scott T. Sheppard, Chapel Hill, NC (US)

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(73) **Assignee:** Cree, Inc.

(21) **Appl. No.:** 11/684,747
(22) **Filed:** Mar. 12, 2007

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/996,249, filed on Nov. 23, 2004.

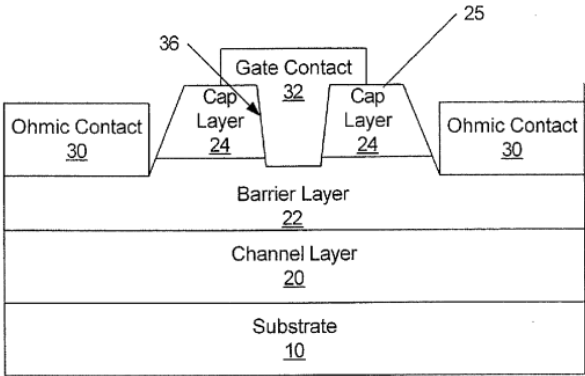
Publication Classification

(51) **Int. CL**
H01L 29/739 (2006.01)
H01L 31/00 (2006.01)

(52) **U.S. CL** 257/194

(57) **ABSTRACT**

High electron mobility transistors are provided that include a non-uniform aluminum concentration AlGaN based cap layer having a high aluminum concentration adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided. High electron mobility transistors are provided that include a cap layer having a doped region adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided. Graphitic BN passivation structures for wide bandgap semiconductor devices are provided. SiC passivation structures for Group III-nitride semiconductor devices are provided. Oxygen anneals of passivation structures are also provided. Ohmic contacts without a recess are also provided.



EPC's speculation that Smith requires activation contradict Smith's description of a non-conductive cap layer

The level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant “surface” state but not so high as to provide introduce traps or leakage paths by becoming a conductive layer.

Ex. 1005 ¶[0087]

Not becoming conductive = non
conductive = not required activation

Smith expressly discloses cap layer being formed with co-doping that is a “method[] of fabricating Semi-insulating Group III nitride layers.”

Smith [0085]

...the doped region 40 is doped with a deep level dopant, such as Fe, C, V, Cr, Mn, Ni and/or Co. The dopant may be incorporated into the **cap layer 34** during deposition or growth of the cap layer 34, 34' ... Techniques for co-doping Group III-nitride materials are described, for example, in U.S. patent application Ser. No. [Saxler874], filed Jan. 7, 2004 entitled “**CO-DOPING FOR FERMIL LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES**,” the disclosure of which is incorporated herein as if set forth in its entirety.

Ex.1005 ¶[0085]

Saxler874 [0005]

Embodiments of the present invention provide Semi-insulating Group III nitride Semiconductor layers and **methods of fabricating Semi-insulating Group III nitride layers.**

Ex.1016 ¶[0005]

EPC's argument of motivation to combine *Saxler874* & *Smith*

Incorrect

1. Smith discloses Compensated GaN layer

2. Smith discloses Semi-insulating layer

Saxler874 and Smith do not disclose different co-doping because they are the same. There is no need to modify Smith with Saxler for a semi-insulating cap; Smith itself discloses Saxler's co-doping for semi-insulating cap layers

Smith [0085]

Techniques for **co-doping Group III-nitride materials** are described, for example, in U.S. patent application Ser. No. 10/752,970 [**Saxler874**], filed Jan. 7, 2004 entitled "CO-DOPING FOR FERMIL LEVEL CONTROL IN SEMI-INSULATING GROUP III NITRIDES," the disclosure of which is **incorporated herein as if set forth in its entirety**.

Ex. 1005 ¶[0085]



"Incorporation by reference provides 'a method for integrating material from various documents into a host document[. . . by citing such material in a manner that makes clear that the material is ***effectively part of the host document as if it were explicitly contained therein.***' Advanced Display Sys., Inc. v. Kent State Univ., 212 F.3d 1272, 1282 (Fed. Cir. 2000)."

Paice LLC v. Ford Motor Co., 881 F.3d 894, 906–07 (Fed. Cir. 2018)

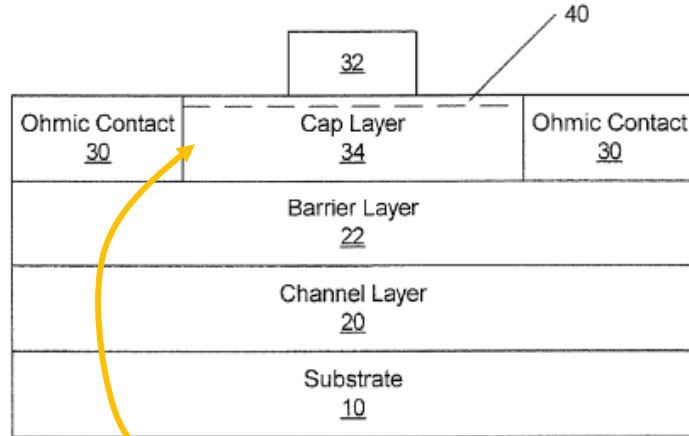
EPC's argument that only region 40 is doped

Incorrect

1. Smith discloses Compensated GaN layer

2. Smith discloses Semi-insulating layer

Smith does not limit doping only to region 40 describing embodiments with cap layer is doped throughout



Smith's teaches cap layer 34 doped throughout

EPC argument

Smith only discloses that layer 40, not cap layer 34, is doped with p-type dopants

and is non-conductive. Ex. 1005 at [0085] – [0089]. And layer 40 is only at the surface of cap layer 34,

Paper No. 32 at 15

Smith [0085]

vs. In some embodiments of the present invention, the cap layer 34 has a dopant incorporated throughout the cap layer 34, 34'.

Ex.1005 ¶[0085]

Issue	EPC's Argument	Correct Resolution
Claim 1: Does Smith itself meet the "compensated GaN layer"?	Smith does not disclose compensation, and POSITA would "likely have included an anneal/activation" to remove H	POSITA knew Smith's cap layer 34 would be H passivated "as-grown," meeting the "compensated GaN" constructions. Smith does not support EPC's speculation of a "likely" activation
Claim 7: Does Smith itself meet the "semi-insulating III-N layer"?	Smith only teaches regions of different dopant concentrations and there is no motivation to use Saxler's co-doping in Smith	Smith expressly discloses co-doping for cap layer 34, doping throughout the cap, and that co-doping is a method for fabricating semi-insulating III-N layers. Saxler is part of Smith it is not a combination that requires motivation to combine

Yes. Compensated "as grown"

Yes. Semi-insulating with co-doping

Grounds 1B: Smith + Kigami

Ground 1B: Applying Kigami's known localized H passivation technique to Smith's known device making cap layer 34 doped but not conductive

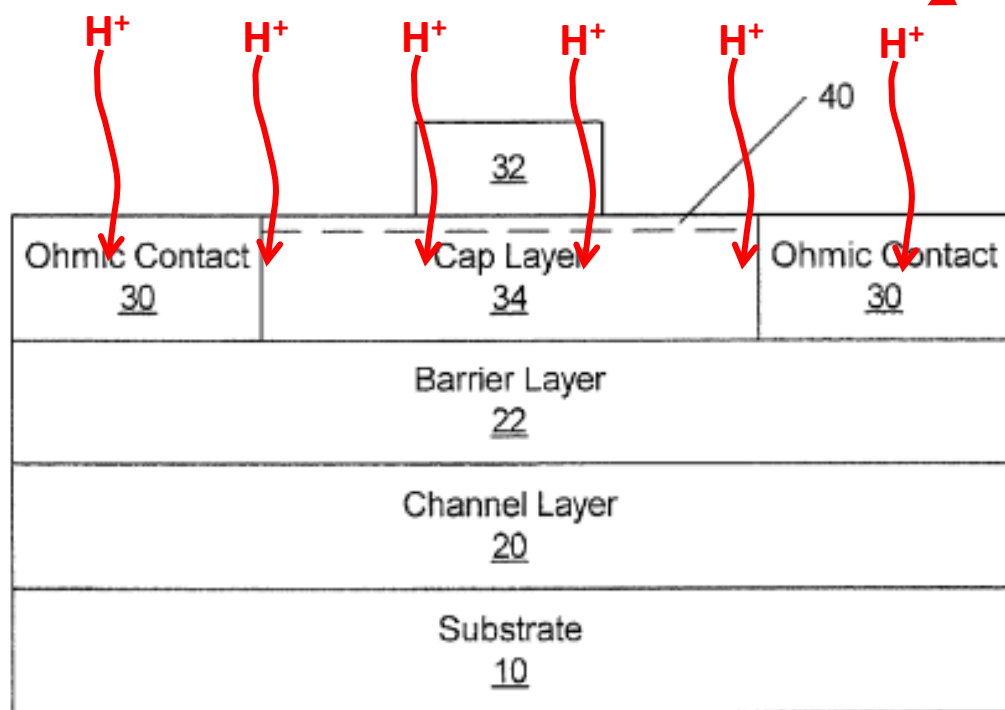
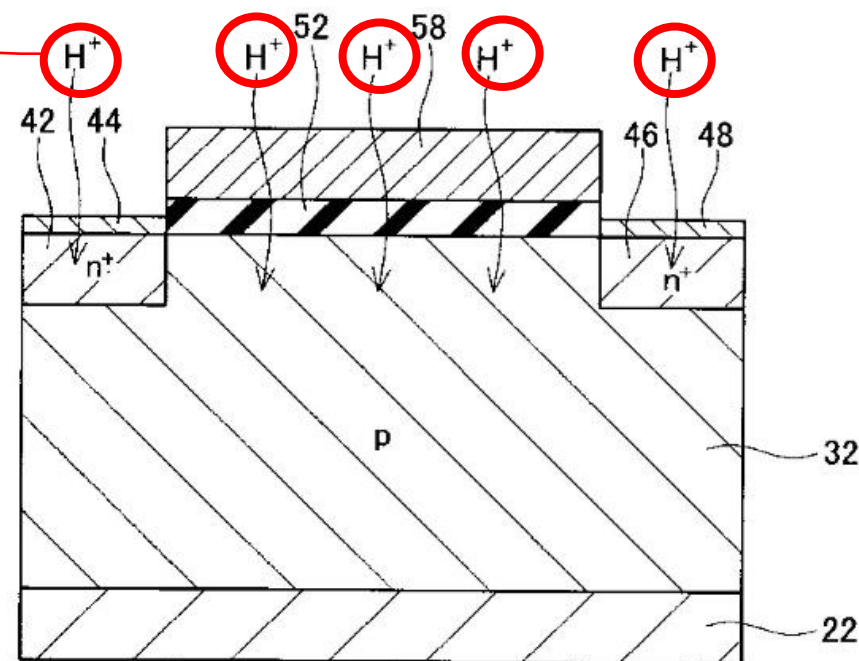


FIG. 5



In ground 1B, cap layer 34 meets the “compensated GaN” under any construction

Issue	EPC’s Argument	Correct Resolution
Motivation to combine: Why would a POSITA use Kigami’s technique to intentionally passivate dopants in Smith’s cap layer 34?	POSITA would have found passivating Smith’s cap layer dopants counterintuitive	A POSITA would have used Kigami’s technique to control the level of doping in Smith’s cap layer 34 and prevent too much doping that turned the layer conductive

1. Analogous art: Both describe GaN HEMTs
2. KSR known technique applied to known device: Kigami's known technique is applied to Smith's known device
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
4. Reasonable expectation of success: POSITA had reasonable expectation that Kigami's technique would further Smith's goals of doped but not conductive
5. Answer to the Board's question
6. EPC's counter arguments are incorrect

Smith and Kigami are analogous art, they both specifically describing techniques for fabricating GaN HEMTs

Smith ¶[0031]

Some embodiments of the present invention provide Group III-nitride **HEMTs** including a Group III-nitride based channel layer and a Group III-nitride based barrier layer on the channel layer.

Ex. 1005 ¶[0031]

Kigami ¶[0010]

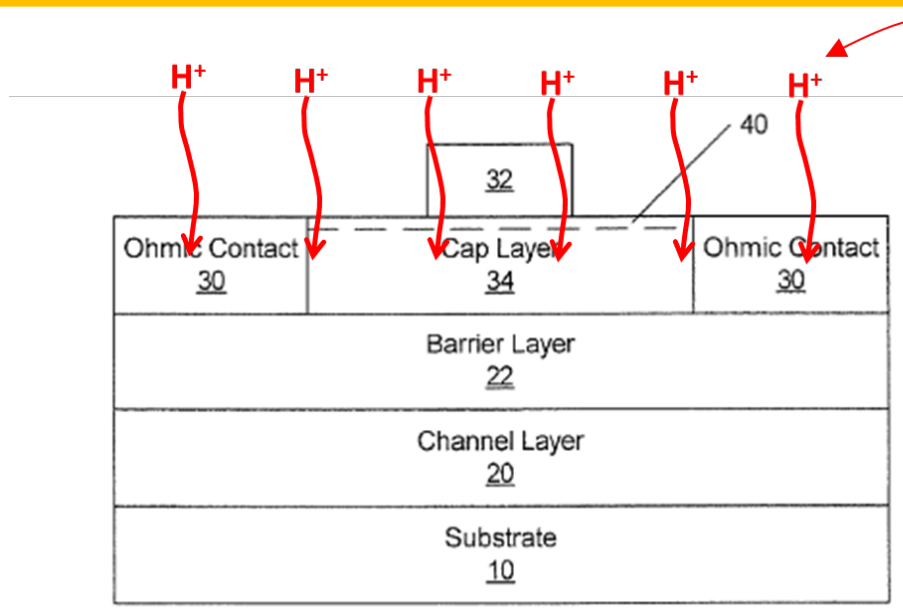
The present invention can be embodied in a semiconductor device having a **HEMT** (high-electron-mobility transistor) structure.

Ex. 1008 ¶[0010]

Applying Kigami's technique to Smith's device

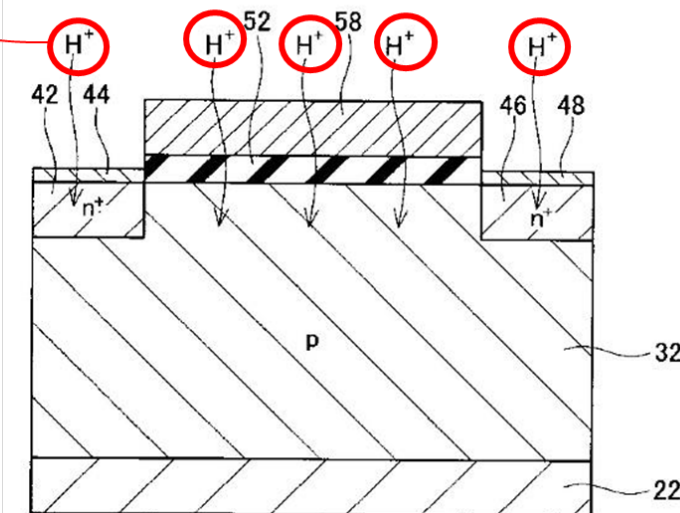
1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

Smith/Kigami is applying a known technique (Kigami's hydrogenation technique to control conductivity) to a known device (Smith's transistor) ready for improvement (reducing leakage by controlling level of doping) to yield predictable results (reduction of cap layer's conductivity)



Known device ready to make layer nonconductive

FIG. 5



Known technique to make layer nonconductive

Some TSM to use Kigami's technique in Smith

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

Kigami expressly suggests applying its technique in devices that like Smith use Mg dopants and seek to locally reduce active dopants.

Smith uses Mg as p-type impurity stating "p-type dopants may be Mg."

Ex. 1005 ¶[0087]

[0012]

The p-type impurity preferably is magnesium.

As mentioned above, because the magnesium diffusion rate is extremely high, it is difficult to form a III-V group compound semiconductor in which the magnesium concentration is locally lowered. In the present invention, by forming a composite with the hydrogen atoms, the magnesium is inactivated. By locally inactivating the magnesium, a region can be formed in which the concentration of the "activated magnesium" is locally low. Even if the concentration of the "activated magnesium" is set low locally, because the concentration of the magnesium itself is the same as that of other regions, magnesium does not diffuse in from other regions. The present invention is particularly useful in situations in which magnesium is used as a p-type impurity.

Ex. 1008 ¶[0012]

Some TSM to use Kigami's technique in Smith

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

Kigami expressly suggests applying its technique to improve HEMT speed and threshold, complementing Smith's objectives

Smith [0005]

A device of particular **interest for high power and/or high frequency applications** is the High Electron Mobility Transistor (HEMT), which, in certain cases, is also known as a modulation doped field effect transistor (MODFET).

Ex. 1005 ¶[0005]

Kigami suggests using its technique to improve the same device performance Smith targets

Kigami [0029]

By forming the local region 34, in which hydrogen is unevenly distributed, at the junction interface between the gate-insulating film 52 and the semiconductor layer 32, the interface energy level can be reduced. **The effects of stabilized threshold voltage, increased switching speed, and the like are obtained**

Ex. 1008 ¶[0029]

Dr. Shealy explained POSITA would have expected success implementing Kigami's suggested technique in Smith because H passivation was a well-known technique to control doping in GaN

EPC does not dispute this expectation of success

transistor with a reasonable expectation of success. By April 2009, the earliest priority for the '294 patent, it was well-known that hydrogen passivated impurities in GaN layers and affected the layer's conductivity. *Prosecution History*, 88. *Kigami* also provides experimental data showing the effect of introducing hydrogen atoms in transistor performance. *Kigami*, [0028], Fig. 6. And *Kigami* explains the mechanisms for hydrogen diffusion and impurity passivation, detailing how the hydrogen diffusion would be performed. *Kigami*, [0022]-[0026], Fig. 5. In view of its general knowledge about doping and passivation, and in view of *Kigami*'s disclosure, it is my opinion that a person of ordinary skill in the art would have had a reasonable expectation of success in modifying *Smith* with *Kigami*'s hydrogen incorporation technique.

Ex. 1003 ¶133

Question: Why a POSITA would have used Kigami to passivate Smith?

We question Petitioner's proposed combination. In the embodiment depicted in Figure 2A of Smith, dopants are added to cap layer 34 to form doped region 40, in which the concentration of dopants is higher than in the rest of cap layer 34. Ex. 1005 ¶¶ 85, 87. This increased concentration of dopants is "used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents." *Id.* ¶ 87. Petitioner's proposed combination would intentionally passivate the very dopants that Smith seeks to add to cap layer 34 to alter its electrical characteristics. We question whether Petitioner adequately explains why one of ordinary skill in the art would have used Kigami's methods to produce a cap layer with the opposite dopant configuration than desired in Smith.

Paper No. 11 at 24

Paper No. 26 §V.C

Answer: To control the level of doping in the cap layer so it is doped but not conductive.

Clarification: Kigami's passivation does not change to opposite dopant configuration, it reduces the doping level.

The level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant 'surface' state *but not so high as to provide introduce traps or leakage paths by becoming a conductive layer.*

Smith, [0087] (emphasis added). *Smith* explains that some doping causes desirable effects, but too much doping make the layer conductive causing undesirable effects. *Id.* A POSITA seeking that "sweet spot" doping, would have found it obvious to passivate dopants to reduce doping level keeping the cap layer nonconductive. Pet., 38-40; Ex. 1033, [075]-[079]. Tailoring the level of doping in the cap layer (e.g., through dopant passivation) would be consistent with *Smith*. Ex. 1033, [072], [090].

Paper No. 26 at 16

Five elements in the record that support the answers

- a) **Smith:** Some doping is good, too much is not
- b) **Schubert:** H implantation was “widely used” to tailor properties
- c) **Shealy:** Kigami can tailor the level of doping post-fabrication
- d) **Nakamura:** Hydrogenation controls doping and resistivity
- e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants

Smith: Some doping is good, too much is not

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

- a) **Smith:** Some doping is good, too much is not
- b) **Schubert:** H implantation was “widely used” to tailor properties
- c) **Shealy:** Kigami can tailor the level of doping post-fabrication
- d) **Nakamura:** Hydrogenation controls doping and resistivity
- e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants

Smith supports the answer because it asks to control the level of doping to be in a “sweet spot” (sufficiently high ... but no so high)



Smith [0087] (description of p-type cap layer)

“P-type dopants may be used to screen the channel region from surface states, pin the surface energy level at a predictable and desired level to reduce and/or minimize trapping effects and to reduce leakage currents. The level of doping should be sufficiently high so as to reduce leakage current in embodiments without a recessed gate and be the dominant ‘surface’ state but not so high as to provide introduce traps or leakage paths by becoming a conductive layer.”

Ex. 1005 ¶[0087]

Smith: Some doping is good, too much is not

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

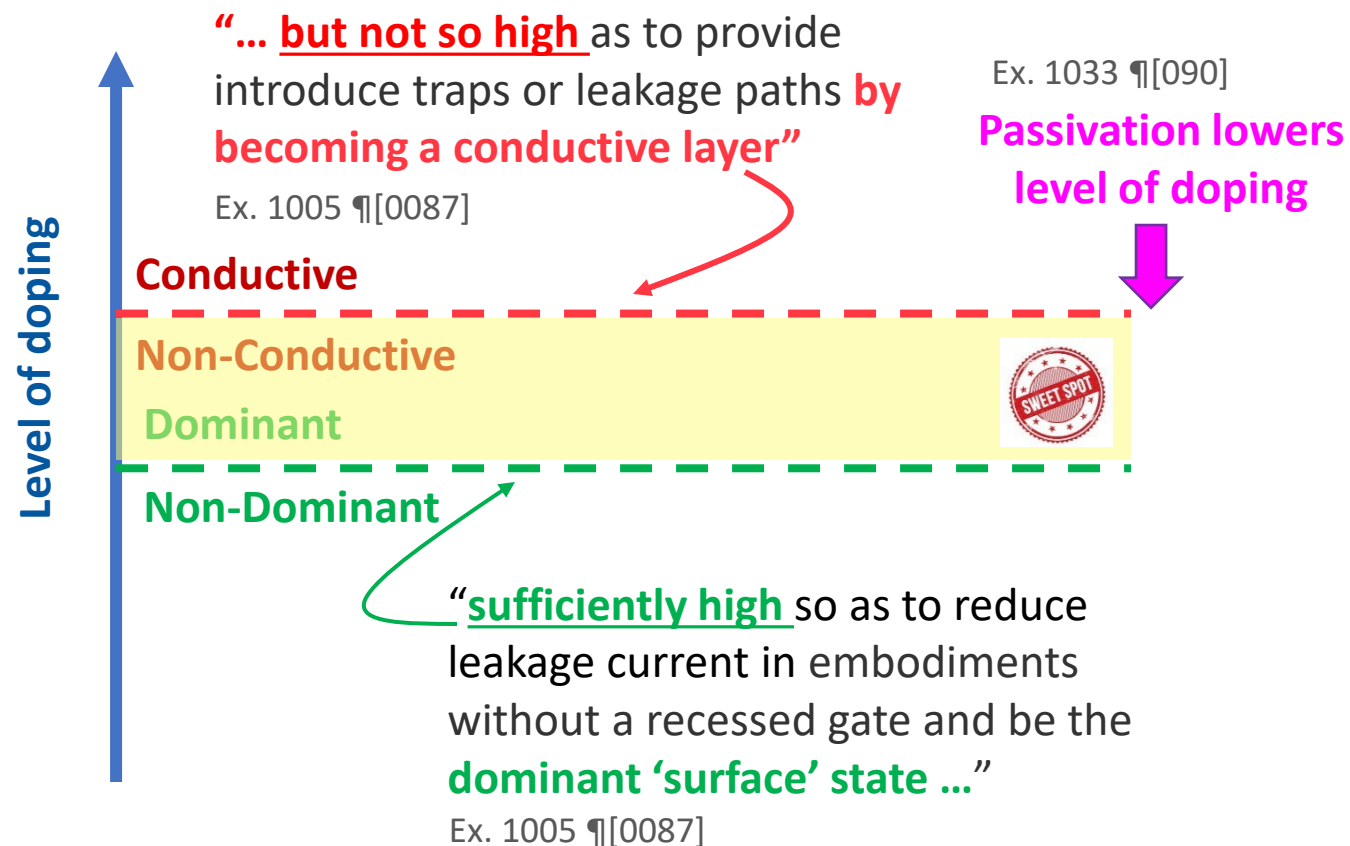
a) **Smith:** Some doping is good, too much is not

b) **Schubert:** H implantation was “widely used” to tailor properties

c) **Shealy:** Kigami can tailor the level of doping post-fabrication

d) **Nakamura:** Hydrogenation controls doping and resistivity

e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants



Record shows Kigami’s passivation helps reaching this sweet spot of doped without becoming conductive (below red line, above green)

Schubert: H implantation “widely used” to tailor properties

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

a) **Smith:** Some doping is good, too much is not

b) **Schubert:** H implantation was “widely used” to tailor properties

c) **Shealy:** Kigami can tailor the level of doping post-fabrication

d) **Nakamura:** Hydrogenation controls doping and resistivity

e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants

Schubert: H passivation after doping to “tailor the electrical properties of thin films”

Doping in III–V Semiconductors

E. F. SCHUBERT

CAM
SEMICON
MICROEL



Finally, hydrogen can also passivate group-IV acceptors such as C or Ge. Chevallier et al. (1988) proposed an atomic model in which the hydrogen is bound to the group-IV acceptor and is in a BC position between the group-IV acceptor and one of its group-III neighbors.

9.3.2 Hydrogen incorporation by implantation

Hydrogen implantation is a process that is widely used to render III–V semiconductors highly resistive. Semi-insulating properties with resistivities $\leq 10^7 \Omega \text{ cm}$ can be achieved by hydrogen implantation as well. The implantation process allows one to choose the implantation depth which provides high flexibility to tailor the electrical properties of thin films.

Ex. 1032 at 406

EPC’s own expert wrote a book in 1993 describing H passivation after doping increases resistance and allows tailoring electrical properties (like doping)

- a) **Smith:** Some doping is good, too much is not
- b) **Schubert:** H implantation was “widely used” to tailor properties
- c) **Shealy:** Kigami can tailor the level of doping post-fabrication
- d) **Nakamura:** Hydrogenation controls doping and resistivity
- e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants

Kigami allows “tailoring of the level of doping post-fabrication” because “hydrogen ions can pass through the gate electrode” facilitate achieving the “sweet spot” even after the device is fabricated

conductive). *Smith* ¶[0087]. Indeed, a POSITA would have recognized *Kigami*’s technique as highly desirable to achieve *Smith*’s “sweet spot” because it allows tailoring of the level of doping post-fabrication and after the placement of the gate electrode. *Kigami* discloses that with its technique “hydrogen ions can pass through the gate electrode 58 and the gate-insulating film 52” and “the region into which the hydrogen atoms are to be introduced, the concentration distribution of the hydrogen atoms to be introduced, and the like can be adjusted.” *Kigami* ¶[0026]. A POSITA would have recognized these characteristics of *Kigami*’s technique highly beneficial when seeking *Smith*’s level of doping “sweet spot.” A POSITA would have recognized that *Kigami*’s technique ability to control the passivation even after the device is fabricated and a gate electrode is formed, would facilitate achieving the “sweet spot” level of doping *Smith* asks for (e.g., allowing iterative hydrogenation and testing). Ex. 1033 ¶[090]-[092]



- a) **Smith:** Some doping is good, too much is not
- b) **Schubert:** H implantation was “widely used” to tailor properties
- c) **Shealy:** Kigami can tailor the level of doping post-fabrication
- d) **Nakamura:** Hydrogenation controls doping and resistivity
- e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants

Passivating dopants does not change to opposite doping configuration (e.g., p-type does not become n-type) it only reduces the level of doping: “the cap layer remains with its original doping configuration”

[092] Importantly, contrary to Dr. Schubert’s suggestion, when applying *Kigami*’s technique to *Smith*, the cap layer remains with its original doping configuration because the hydrogen acts as a passivation agent, it does not change the doping configuration. For example, if *Smith* is p-type doped, as described in paragraph [0087], applying *Kigami*’s hydrogenation would not change the doping to the opposite configuration (n-type). Rather, *Kigami*’s hydrogenation would only reduce the active p-type dopants by locally inactivating some of the p-type dopants. Introducing hydrogen using *Kigami*’s method in *Smith* would not change it to an opposite dopant configuration (in the example before the doping of the cap layer would remain p-type) but it would decrease doping levels, raise layer resistivity, and facilitate control of doping to achieve *Smith*’s level of doping “sweet spot.”



- a) **Smith:** Some doping is good, too much is not
- b) **Schubert:** H implantation was “widely used” to tailor properties
- c) **Shealy:** Kigami can tailor the level of doping post-fabrication

d) Nakamura: Hydrogenation controls doping and resistivity

- e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants

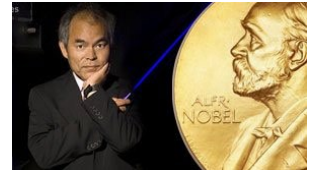
Nakamura reported how a hydrogenation process (like Kigami’s) controls the level of doping in p-GaN with the “formation of acceptor-H neutral complexes” that “causes high resistivity” (i.e., consistent with Smith’s goal of doped but non-conductive)

Hole Compensation Mechanism of P-Type GaN Films

Shuji NAKAMURA, Naruhito IWASA, Masayuki SENOH and Takashi MUKAI

Nichia Chemical Industries, Ltd., 491 Oka, Kaminaka, Anan, Tokushima 774

(Received January 13, 1992; accepted for publication February 15, 1992)



Low-resistivity p-type GaN films, which were obtained by N₂-ambient thermal annealing or low-energy electron-beam irradiation (LEEBI) treatment, showed a resistivity as high as $1 \times 10^6 \Omega \cdot \text{cm}$ after NH₃-ambient thermal annealing at temperatures above 600°C. In the case of N₂-ambient thermal annealing at temperatures between room temperature and 1000°C, the low-resistivity p-type GaN films showed no change in resistivity, which was almost constant between 2 $\Omega \cdot \text{cm}$ and 8 $\Omega \cdot \text{cm}$. These results indicate that atomic hydrogen produced by NH₃ dissociation at temperatures above 400°C is related to the hole compensation mechanism. **A hydrogenation process whereby acceptor-H neutral complexes are formed in p-type GaN films was proposed.** The formation of acceptor-H neutral complexes causes hole compensation, and deep-level and weak blue emissions in photoluminescence.

KEYWORDS: p-type GaN, thermal annealing, hydrogenation, photoluminescence

Before hydrogenation of InP:Zn, the resistivity of this p-type InP epilayer was 0.04 $\Omega \cdot \text{cm}$. **After hydrogenation, the resistivity became higher** than $10^5 \Omega \cdot \text{cm}$. Also, the PL spectra showed a difference between states before and after hydrogenation.^{17,22)} This was interpreted as being

Ex. 1018 at 1



Ex. 1018 at 10

- a) **Smith:** Some doping is good, too much is not
- b) **Schubert:** H implantation was “widely used” to tailor properties
- c) **Shealy:** Kigami can tailor the level of doping post-fabrication
- d) **Nakamura:** Hydrogenation controls doping and resistivity

- e) **Kigami:** Teaches passivating after doping improves transistors and is “particularly useful” when using Mg dopants

Kigami not only teaches the technique, it provides “some TSM” to use the technique in devices with Mg (like Smith)

Kigami provides an adjustable technique for localized H passivation allowing control of both region and concentration, consistent with Smith’s goal of doped but not conductive

As shown in FIG. 5, the hydrogen gas is ionized, and a portion of those hydrogen ions (H^+) pass through the gate electrode 58 and the gate-insulating film 52. As needed, the region into which the hydrogen atoms are to be introduced, the concentration distribution of the hydrogen atoms to be introduced, and the like can be adjusted by forming in advance on the front-surface side of the semiconductor device 10 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these.

Adjust concentration / region

Ex. 1008 ¶[0026]

hydrogen atoms, the magnesium is inactivated. By locally inactivating the magnesium, a region can be formed in which the concentration of the “activated magnesium” is locally low. Even if the concentration of the “activated magnesium” is set low locally, because the concentration of the magnesium itself is the same as that of other regions, magnesium does not diffuse in from other regions. The present invention is particularly useful in situations in which magnesium is used as a p-type impurity.

Ex. 1008 ¶[0012]



- a) **Counterintuitive:** To passivate after doping a layer
- b) **Different layer:** Kigami's passivated layer is not the same as the cap layer
- c) **Only region 40 is doped:** Only region 40 in cap layer 34 is doped

EPC argues against the combination incorrectly contending: (a) it would be counterintuitive, (b) Kigami is not passivating a cap layer, and (c) that only region 40 in cap layer 34 is doped

Other EPC arguments hinged on the already refuted claim construction

EPC's argument that passivating is counterintuitive

Incorrect

noscience

1. Analogous

2. Apply technique

3. TSM

4. Expectation

5. Board Question

6. Rebuttal to EPC

6a) Counterintuitive

Record shows it was not “counterintuitive” to dope and then passivate. It was “widely used,” consistent with Smith’s target level of doping, and specifically considered useful in situations using Mg as dopants

Schubert’s book

“The possibility of rendering III-V semiconductors semi insulating by **hydrogen implantation** made this technique **very attractive** for device applications.”

Ex. 1029 at 406

Smith [0087]



Kigami [0012]

“In the present invention, by forming a composite with the hydrogen atoms, the magnesium is inactivated. By **locally inactivating the magnesium**, a region can be formed in which the concentration of the ‘activated magnesium’ is locally low....

The present invention is **particularly useful in situations in which magnesium is used as a p-type** impurity”

Ex. 1008 ¶[0012]

EPC's argument that Kigami passivates a different layer

Incorrect

ce

1. Analogous

2. Apply technique

3. TSM

4. Expectation

5. Board Question

6. Rebuttal to EPC

6b) Different layer

EPC argument that Kigami's layer would not be "functional in place of cap layer 34" is misdirected, Smith/Kigami does not replace layers, it applies a technique

EPC incorrect argument of substitution

2012 at 21:4-23:20. Nothing in *Kigami* discloses or suggests that its hydrogen-treated p-type GaN layer would be suitable below the gate contact or that a compensated GaN layer including Mg dopants and hydrogen would be acceptable or functional **in place of the cap layer 34** of *Smith*. Ex. 2009 at ¶ [154]. A POSA would therefore not seek to combine the teachings of *Smith* with *Kigami*, to "apply Paper No. 18 at 43

Kigami's technique is adjustable

into the front-surface side of the semiconductor layer 32. Because the size of hydrogen ions (H^+) is small, the hydrogen ions can pass through the gate electrode 58 and the gate-insulating film 52. **As needed, the region into which the hydrogen atoms are to be introduced, the concentration distribution of the hydrogen atoms to be introduced, and the like can be adjusted** by forming in advance on the front-surface side of the semiconductor device 10 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these.
Ex. 1018 ¶[0026]

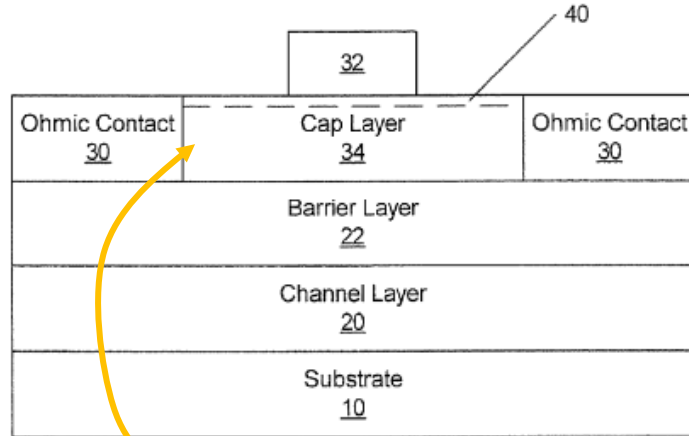
Kigami technique is not limited to one layer, Kigami expressly states its technique allows adjusting where the H is introduced and the H concentration

EPC's argument that only region 40 is doped

Incorrect

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC 6c) Only doped region 40

Smith does not limit doping only to region 40 describing embodiments with cap layer is doped throughout



Smith's teaches cap layer 34 doped throughout

EPC argument

Smith only discloses that layer 40, not cap layer 34, is doped with p-type dopants

and is non-conductive. Ex. 1005 at [0085] – [0089]. And layer 40 is only at the surface of cap layer 34,

Paper No. 32 at 15

Smith [0085]

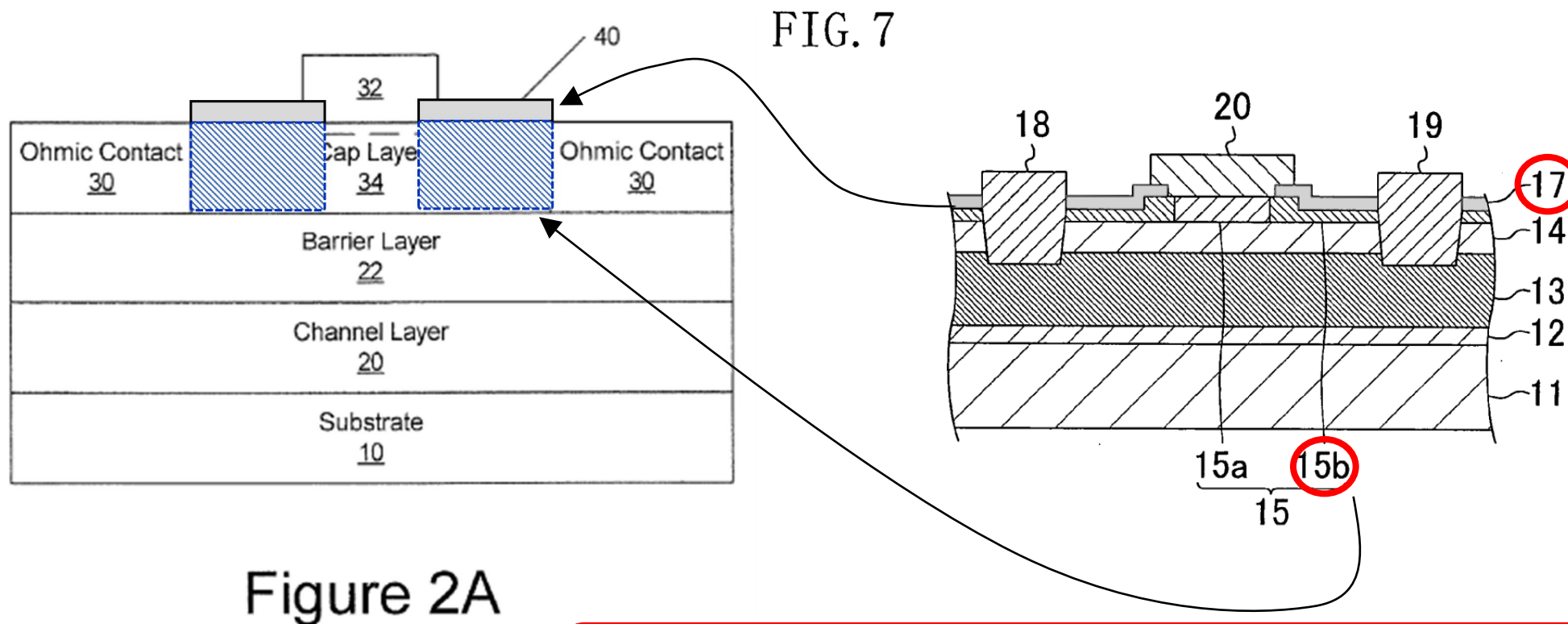
vs. In some embodiments of the present invention, the cap layer 34 has a dopant incorporated throughout the cap layer 34, 34'.

Ex.1005 ¶[0085]

1. Analogous art: Both describe GaN HEMTs
Same transistors → Obvious to combine
2. KSR known technique applied to known device: Kigami's known technique is applied to Smith's known device
Known technique, known device → Obvious to combine
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
Smith/Kigami some TSM → Obvious to combine
4. Reasonable expectation of success: POSITA had reasonable expectation that Kigami's technique would further Smith's goals of doped but not conductive
Expectation to make layer doped and nonconductive → Obvious to combine
5. Answer to the Board's question
Passivate after doping to control doping level to be in the "sweet spot" → Obvious to combine
6. EPC's counter arguments are incorrect
Passivation was not "counter intuitive" but "widely used" and the combination doesn't substitute layers → Obvious to combine

Ground 1C: Smith + Uemoto

Adding Uemoto's H diffusion film (17) to Smith forming high resistive layers with H passivating Mg to reduce gate leakage



In ground 1C, resistive regions in cap layer 34 meet the “compensated GaN” layer

Issue	EPC’s Argument	Correct Resolution
Motivation to combine: Why would a POSITA apply Uemoto’s teachings to Smith?	Uemoto and Smith are concerned with different issues. There would not be on motivation to combine.	A POSITA would have been motivated to incorporate Uemoto’s high- resistivity region 15b into smith to reduce leakage

1. Analogous art: Both describe GaN HEMTs
2. KSR's use of known technique to improve similar devices in the same way.
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine.
4. Reasonable expectation of success: POSITA had reasonable expectation that Kigami's technique would further Smith's goals of doped but not conductive
5. EPC's counter arguments are incorrect

Smith and Uemoto are analogous art, they both specifically describe techniques for fabricating GaN transistors with reduced gate leakage

Smith ¶[0008]

Some embodiments of the **present invention provide Group III-nitride high electron mobility transistors** and methods of fabricating Group III-nitride high electron mobility transistors

Ex. 1005 ¶[0008]

Uemoto ¶[0005]

The **present invention relates to nitride semiconductor transistors and their fabrication methods**. In particular, the present invention relates to normally-off type nitride semiconductor transistors applicable to power switching devices, and their fabrication methods.

Ex. 1006 ¶[0005]

Using Uemoto's technique to Improve Smith's similar device

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

Smith/Uemoto is using a known technique (Uemoto's H diffusion for high resistive regions) to improve similar devices (Smith's transistor) in the same way (adding high resistive regions to reduce leakage)

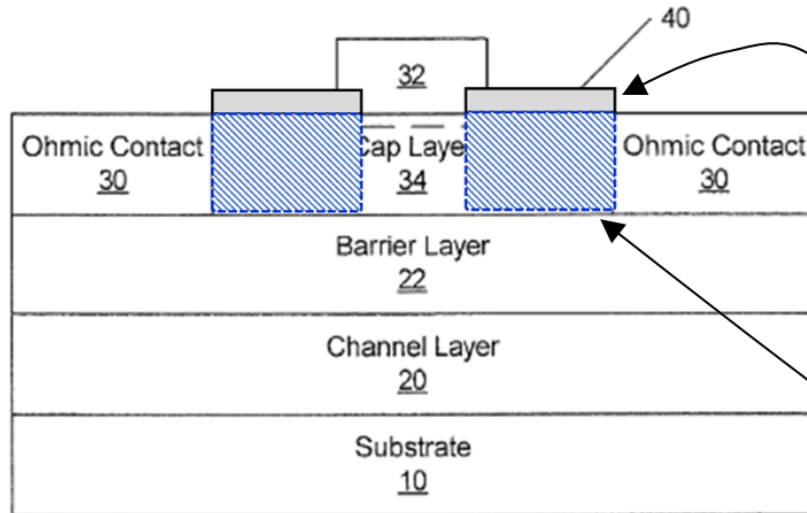
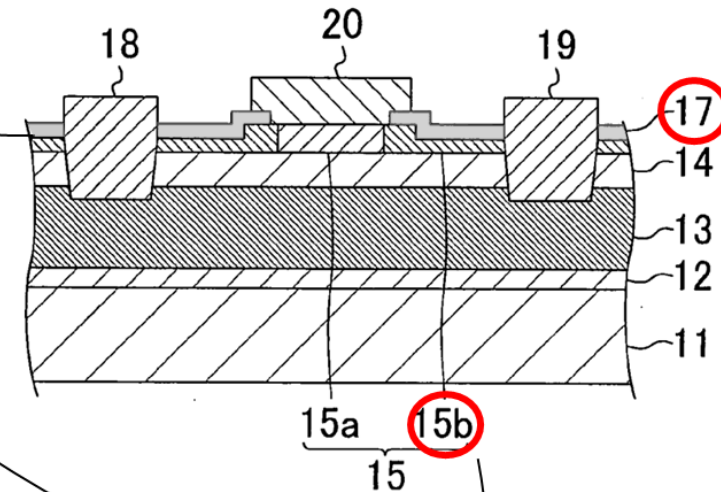


Figure 2A

Smith's similar III-N transistor

FIG. 7



Uemoto's known technique to improve III-N transistor

Some TSM to use Uemoto's H diffusion in Smith

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

Uemoto suggests applying its technique when seeking to reduce gate leakage, Smith also seeks to reduce gate leakage

Smith [0087]

The level of doping should be sufficiently high so as **to reduce leakage current** in embodiments without a recessed gate and be the dominant “surface” state but not so high as to provide introduce traps or leakage paths by becoming a conductive layer.

Ex. 1005 ¶[0087]

Uemoto [0059]

As the resistance of the high resistive region 15 b between the control region 15 a and the drain electrode 19 is higher, **a greater amount of leakage current between the gate and the drain can be reduced.**

Ex. 1006 ¶[0059]

Uemoto and Smith seek the same goal:
reduce gate leakage

Uemoto expressly suggests applying its technique to “power transistors,” Smith describes a power transistor

Smith [0005]

A device of particular interest for **high power and/or high frequency applications** is the **High Electron Mobility Transistor (HEMT)**, which, in certain cases, is also known as a modulation doped field effect transistor (MODFET).

Ex. 1005 ¶[0005]

Uemoto [0079]

Accordingly, for example, **the present invention is useful for a nitride semiconductor transistor such as a power transistor** with a high breakdown voltage, and for its fabrication method.

Ex. 1006 ¶[0079]

As Dr. Shealy explains, a POSITA would have expected success implementing Uemoto's suggested incorporation of a H diffusion film to Smith because H passivation was a well-known mechanism to selectively resistivity and control leakage

[0140] Additionally, it is my opinion that a person of ordinary skill in the art would have incorporated *Uemoto's* hydrogen diffusion film technique to *Smith* with a reasonable expectation of success. The mechanisms and effects of hydrogen incorporation into doped GaN layers had been well-established by 2009. *Prosecution History*, 88. And *Uemoto* provides both experimental data and theoretical analyses that support the use of the hydrogen diffusion film to selectively increase resistivity and improve transistor characteristics. *Uemoto*, [0038], [0049], Figs. 4-8. In view of its general knowledge and *Uemoto's* disclosure, a person of ordinary skill in the art would have incorporated *Uemoto's* hydrogen diffusion technique to *Smith* with a reasonable expectation of success.

Ex. 1003 ¶140

EPC's argument that passivating is counterintuitive

Incorrect

innoscience

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

Record contradicts EPC argument that passivating dopants was counterintuitive, passivating was “widely used” to “tailor the electrical properties,” consistent with Smith of having a nonconductive layer.

EPC's expert 1993 book

Smith [0087]



“Hydrogen also **passivates shallow acceptors** in III-V semiconductors.”

Ex. 1029 at 401

“**Hydrogen implantation** is a process that is **widely used** to render III-V semiconductors highly resistive.”

Ex. 1029 at 402

Uemoto [0065]

“As shown in FIG. 9, by setting the hydrogen concentration in **the hydrogen diffusion film** at $1 \times 10^{20} \text{ cm}^{-3}$ or higher, Mg inactivation **can be promoted to raise the resistivity.**”

Ex. 1029 ¶ [0065]

Incorrect

EPC concedes Smith/Uemoto both seek to “reduce leakage.”
But EPC incorrectly argues no motivation to combine because there are “two different types of leakage current;” KSR precedent contradicts EPC

EPC's incorrect argument

Specifically, Smith adds dopants “to reduce leakage current” in region 40 of the gate, not in the underlying cap layer 34. Ex. 1005 ¶ [0047]. Uemoto provides high resistive layer 15b to allegedly reduce leakage current between the gate and drain. Ex. 1006 ¶ [0059]. Smith and Uemoto are directed to two different types of leakage current, and a POSITA would not be motivated to combine the two teachings, and would not arrive at the ‘294 patent if the teachings were combined.

Paper No. 32 at 19

1. Analogous 2. Known technique 3. TSM 4. Expectation 5. Rebuttal to EPC

Admittedly, Smith/Uemoto address the gate leakage current problem in the same nitride transistors, this is “precisely the reason that there’s a motivation to combine under KSR”



“That Kabemoto and Bauman address the ***same problem*** and that Bauman’s cache was a known way to address that problem ***is precisely the reason that there's a motivation to combine under KSR*** and our precedent.”

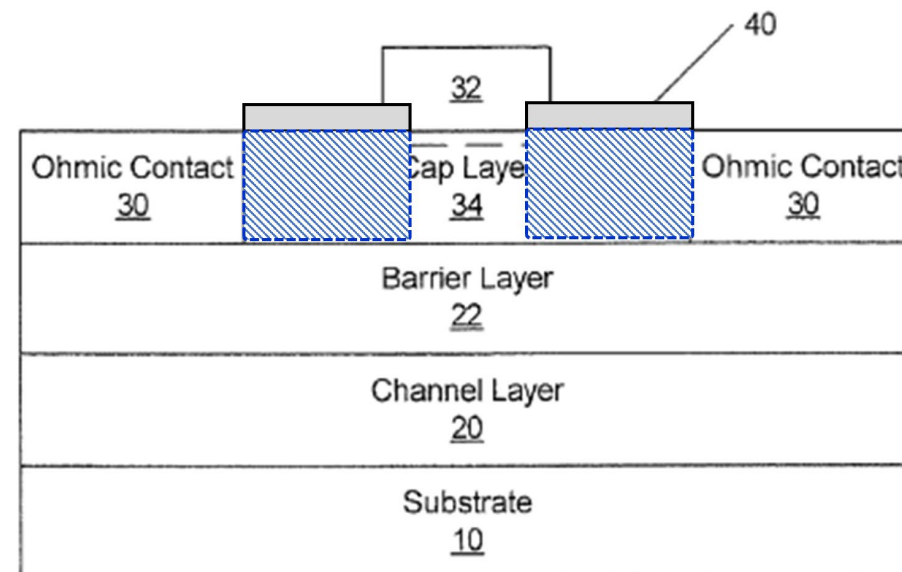
Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

In the combination gate 32 is plainly "above" the blue resistive regions. EPC's argument is based on its improper construction

EPC's incorrect argument

But Petitioner's proposed resulting transistor does not disclose "a gate contact above the compensated GaN layer," as properly construed. That is, Petitioner's proposed transistor does not have a gate contact and compensated GaN layer that are part of the same gate structure. For example, as can be seen in the figure above, the blue portions of Petitioner's modified FIG. 2A correspond to the alleged compensated GAN layer. That layer is not part of the gate structure and does not reduce gate capacitance, a critical goal of the '294 patent. Ex. 2009 at ¶ [166].

Paper 18 at 49



1. Analogous art: Both describe GaN HEMTs Same transistors → Obvious to combine
2. KSR's use of known technique to improve similar devices in the same way. Known technique, known device
→ Obvious to combine
3. KSR's some teaching, suggestion, motivation (TSM) in the prior art to modify or combine. Smith/Uemoto TSM → Obvious
to combine
4. Reasonable expectation of success: POSITA had reasonable expectation that Kigami's technique would further Smith's goals of doped but not conductive Expectation to increase
resistance → Obvious to combine
5. EPC's counter arguments are incorrect Passivation was not "counter intuitive" but
"widely used" → Obvious to combine

Secondary Considerations of Non-obviousness

EPC's website and article focus on “mature, efficient, and low cost supply chain” and “packaging limitations,” not the claimed features

EPC's Website

Gallium Nitride Transistors Hit the Market

(/epc/products/gan-fets-and-ics) In June 2009, EPC delivered the first commercial enhancement-mode GaN (eGaN®) transistors. These new devices were manufactured in a Taiwanese foundry designed to produce standard silicon integrated circuits creating a mature, efficient, and low cost supply chain, making its GaN transistors extraordinarily reliable and affordable. Today EPC offers more than 100 products that address a \$13 Billion market (/epc/products/gan-fets-and-ics).

Ex. 2020 at 5

Semi Article

The Americas SEMI award was presented to Dr. Alex Lidow, Ph.D., for innovation in power device technology enabling commercialization of GaN devices with performance and cost advantages over silicon. Silicon-based devices were reaching their limits in speed and efficiency, prompting Lidow to develop Gallium Nitride (GaN) technologies, but high cost limited its commercial success. Lidow led the GaN development activity at International Rectifier and continued that work at Efficient Power Conversion Corporation (EPC), a company he co-founded in 2007. EPC introduced the first commercial enhancement mode GaN power transistors in 2009. Challenges from resolving packaging limitations to establishing a low-cost supply chain were overcome through persistence, paving the way for the successful commercialization of GaN power devices.

Ex. 2021 at 1

EPC's exhibits fail to even mention the purportedly innovative “compensated” or “semi-insulating” features of the claims

Dr. Shealy: EPC's "first commercialization" is not based on the features in the claims but on "supply chain," "cost fabrication,"

Dr. Shealy: EPC focus on features like reduced leakage and switching efficiency are not unique to the invention

[0110] Instead of focusing on the unique features of the claim, Dr. Schubert seems to have focused on the device commercialization and the alleged introduction of the "first commercial enhancement-mode GaN transistors in 2009." Ex. 2009 ¶194. But this first commercialization is not based on the unique features of the claims. This is confirmed with the documents Dr. Schubert cited. For example, Exs. 2020 and 2021 discuss supply chain, packing limitations, and low-cost fabrication. They do not even mention a "Compensated Gate MISFET" as in the patent. These leads me to conclude that the commercialization Dr. Schubert relies on is not linked to the unique features of the claims but to other features like production costs and supply chain issues. Dr. Schubert also cites to "some of the industrial praise EPC gathered over the years." Ex. 2009 ¶197. But this alleged industrial praise has nothing to do with the unique features of the '294 patent claims.

Ex. 1033 ¶110.

The ITC judge found commercial success not attributable to the invention, general in nature, and “not tied specifically to the invention”

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

CERTAIN SEMICONDUCTOR DEVICES, AND
METHODS OF MANUFACTURING SAME AND
PRODUCTS CONTAINING THE SAME

INV. NO. 337-TA-1366

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND

Chief Administrative Law Judge Clark S. Cheney

(July 5, 2024)

“[T]o accord substantial weight to secondary considerations in an obviousness analysis, . . .

‘there must be a legally and factually sufficient connection between the evidence and the patented invention.’” *Fox Factory, Inc. v. SRAM, LLC.*, 944 F.3d 1366, 1373 (Fed. Cir. 2019). I find EPC

has not persuasively shown that its commercial success is attributable to the invention of claim

1 in the '294 patent. The news articles and awards praising EPC's innovation are general in

nature and do not evidence a link to the features of the patented invention. See CIB at 120. The

testimony cited by EPC is primarily directed to GaN transistors, and not tied specifically to the

invention of the '294 patent. See, e.g., Tr. at 1009:18-1011:15 (Schubert). The lack of a nexus

is even more pronounced when evaluating the distinct inventions of claims 2 and 3. I do

not find EPC's evidence of commercial success and industry praise to have any material effect on

the obviousness analysis.

Ex. 2022 at 101

Issue	Conclusion	ITC resolved: rejecting EPC's proposals
Construction	a. "compensate GaN": Like ITC reject EPC's "gate material" b. EPC's rewriting of [1f]: Like ITC reject EPC's "part of the gate" argument. c. E-mode interpretation: Like ITC reject EPC's "cardinal sin" interpretation	
Ground 2: Uemoto/Smith	a. As the ITC concluded, Uemoto anticipates disputed element [1e] b. The element ITC found not anticipated [1b], is undisputed in Ground 2 c. Smith (incorporating Saxler874) expressly teaches layers being formed co-doped and semi-insulating [7e], combination is undisputed.	ITC confirmed: Uemoto/Smith meet disputed elements
Grounds 1 Smith Smith/Kigami Smith/Uemoto	a. Smith's cap layer can be: compensated "as grown" (meets [1e]) and semi-insulating with co-doping (meets [7e]). b. Smith/Kigami was obvious to combine and meet [1e] c. Smith/Uemoto was obvious to combine and meet [1e]	Smith (alone or combined) meet disputed elements
Secondary considerations	EPC's secondary considerations lack nexus	Not relevant for lacking nexus

Opposition to motion to amend

New limitations mixing requirements for “semi-insulating layer” comprising “compensated layer” and “no 2DEG at 0V”

Claim 13 (Substitute for claim 4)

13. An enhancement mode [A] column III Nitride transistor comprising:
a substrate,
a set of III-N transition layers above the substrate,
a III-N buffer layer above the set of transition layers,
a III-N barrier layer above the buffer layer, [and]
a semi-insulating III-N layer above the barrier layer, wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

Paper No. 17 at Appx. A

Claim 14 (Substitute for claim 10)

14. A compensated gate enhancement mode MISFET transistor comprising:
a III-N barrier layer beneath a gate contact,
a drain contact,
a source contact, and
a semi-insulating III-N layer between the barrier layer and the gate contact, wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and a gate comprising the gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

Paper No. 17 at Appx. A

4 arguments: if the Board finds any of these true, the motion to amend should be denied

§112 Issues	
1. Lack Enablement	Patent does not enable the competing “ semi-insulating ” and “ no 2DEG ” limitations in the new claims
2. Written description, Broadening	Patent does not support semi-insulating layer that is compensated , they are distinct, and the new claims impermissibly expand semi-insulating layer

If the claims comply with §112, they are necessarily obvious under §103

§103 Issues	
3. Smith	New claims are obvious in view of Smith and Kigami, Uemoto
4. Sheu	New claims are obvious in view of Sheu and Kigami

Lack of enablement

EPC admits experimentation beyond the specification's disclosure is required "to make its disclosure enabling."

But EPC incorrectly argues the "patent provides adequate guidance as to the direction of experimentation."

EPC's "adequate guidance as to the direction of experimentation"

The '294 patent provides adequate guidance as to the direction of experimentation to make its disclosure enabling. For example, the '294 patent discloses that the compensated semiconductive layer 38 has a "high doping level... lead[ing] to enhancement mode device" (EX1001, 3:16-17) where "the 2DEG region is depleted, i.e. removed, below the gate at zero applied gate bias" (EX1001, 1:47-50). As previously noted, a POSITA would understand from this disclosure that the Mg acceptor concentration must be sufficiently high to deplete the 2DEG. For example, the Mg density (per cm^2) must be greater than the 2DEG electron density (per cm^2) so that the entire 2DEG under the gate can be depleted. EX2024, ¶ 30.

Paper No. 31 (EPC's Reply MTA) at 10

But the “direction” fails to teach how to make a device having the competing “semi-insulating” and “no 2DEG” requirements

2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted, i.e. removed, below the gate at zero applied gate bias, the device can be an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

Ex. 1001 at 1:43-54

Advantageously, the high doping level of compensated layer 38 leads to enhancement mode devices. In addition, using a compensated semiconductor layer 38 leads to low gate leakage during device operation. Finally, the insulating nature of compensated layer 38 reduces the gate capacitance of the device.

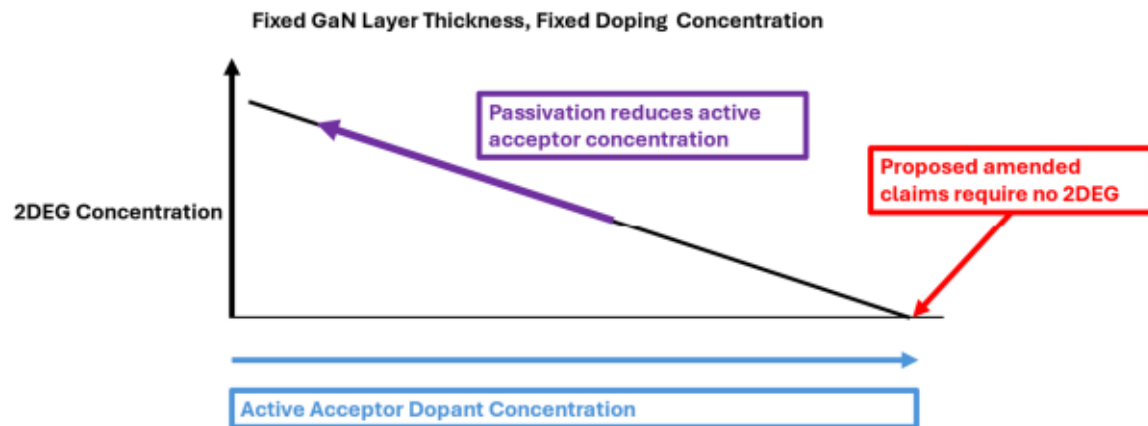
Ex. 1001 at 3:16-21

Paper No. 37 at 2-4

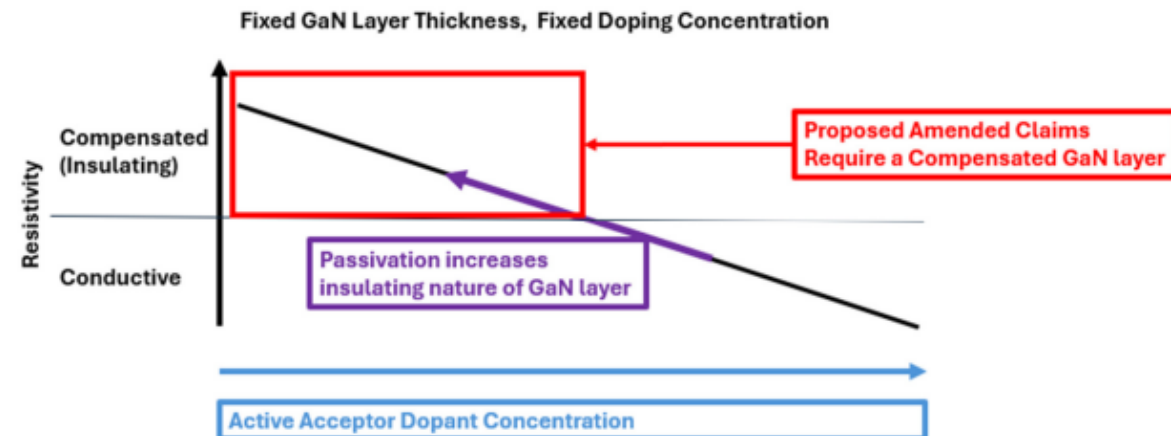
undue experimentation. The patent provides no guidance on GaN layer thickness, doping, and passivation to meet the combined goals of depleting the 2DEG to make an enhancement mode device while also being “compensated.” In view of the tradeoffs between doping, passivation, and GaN layer thickness, the ’294 patent does not enable how to achieve “no two-dimensional electron gas (2DEG) region [] below the gate at zero volts applied gate bias” when the gate structure also includes a “semi-insulating III-N layer compris[ing] a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen” as recited in claims 13 and 14. The patent likewise does not provide any guidance on how to be a MISFET and enhancement mode.

Ex. 1039 (Shealy) at [048]

Multiple parameters: Thickness, Doping Concentration, Resistivity, 2DEG concentration, and Active Dopant. The "direction" in the patent fails to provide any of these details on how to make a device with the contradictory "semi-insulating III-N layer" and "no 2DEG exists" requirements.



Ex. 1039 [044]



Ex. 1039 [045]

Claimed "no 2DEG" requires high active dopant concentration ...

Ex. 1039 [053]-[055]

... but high active dopant concentration makes the layer conductive, the opposite of semi-insulating (requiring low active dopant)

Ex. 1039 [049]-[052]

Claim 13 (Substitute for claim 4)

13. An enhancement mode [A] column III Nitride transistor comprising:
a substrate,
a set of III-N transition layers above the substrate,
a III-N buffer layer above the set of transition layers,
a III-N barrier layer above the buffer layer, [and]
a semi-insulating III-N layer above the barrier layer, wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
a gate comprising a gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

No “direction” how to make a device with both “semi-insulating III-N layer” and “no 2DEG exists”

Ex. 1039 (Shealy) [056]-[064].

“Semi-insulating” requires low concentration (not depleting 2DEG)

Ex. 1039 [053]-[055].

“no 2DEG” requires high concentration (making it conductive)

Ex. 1039 [049]-[052].

Low

Active dopant concentration

High

Paper No. 27 at 8-10 (citing Ex. 1039 (Shealy) §V).

- 1. Routine Procedure:** EPC incorrectly argues a POSITA could make the new claims with a “routine procedure”
- 2. Two energies:** EPC incorrectly argues energy gains in the device would enable the claims

Without anything in the patent teaching how to make the device in the new claims, EPC resorts to arguing the new claims could be made with a “routine procedure” and an extrinsic “two energy gains” theory.

Both these theories for enablement are admittedly not in the patent, and they fail to enable the new claims

EPC resorts to a “routine procedure”

1. Routine Procedure

2. Energy gains

EPC argues the patent conveys a goal that can be achieved with a “**routine procedure**” of increasing p-type doping

EPC argument for enablement

Alleged conveyed goal:
“sufficiently high”

Case No. IPR2023-01381
U.S. Patent No. 8,350,294

at 8-9, citing *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). Here, not only would any experimentation be routine, but also the specification provides a reasonable amount of guidance. EX2024, ¶ 28. A POSITA would appreciate the teachings of the '294 patent that the acceptor concentration needs to be sufficiently high to deplete the 2DEG. As a result, a POSITA would experimentally increase the p-type doping concentration until the 2DEG is depleted. Increasing the p-type doping concentration is a routine procedure that cannot be characterized as undue experimentation. *Id.*

Paper No. 31 at 9

Alleged “routine procedure”:
increase doping

But EPC's "routine procedure" does not enable the claims

1. Routine Procedure 2. Energy gains

Merely increasing doping would not allow making the new claims because it would make the layer conductive, opposite of semi-insulating

"Semi-insulating" requires low concentration (not depleting 2DEG)

EPC's "routine procedure" makes the layer conductive, moving away from the "semi-insulating III-V layer"

"no 2DEG" requires high concentration (making it conductive)

Ex. 1039 [053]-[055].

Ex. 1039 [049]-[052].

Low

Active dopant
concentration

increasing doping

High

The alleged goal of “sufficiently high” is not enablement

1. Routine Procedure 2. Energy gains

EPC argument for enablement

reasonable amount of guidance. EX2024, ¶ 28. A POSITA would appreciate the teachings of the '294 patent that the acceptor concentration needs to be sufficiently high to deplete the 2DEG. As a result, a POSITA would experimentally increase the p-type doping concentration until the 2DEG is depleted. Increasing the p-type doping concentration is a routine procedure that cannot be characterized as undue experimentation. *Id.*

EPC argues that a POSITA would appreciate acceptor concentration “needs to be sufficiently high to deplete the 2DEG.” But stating a goal fails to enable.

But how high is sufficient?
How can POSITA find when is “sufficiently high”?
How is sufficiently high but nonconductive?
The patent is silent

Conveying a goal of “sufficiently high” is not enablement

1. Routine Procedure

2. Energy gains

Finding what is “sufficiently high” would be a “research assignment” and “[t]hat is not enablement”



“These two approaches amount to little more than two **research assignments**. ... They leave a scientist about where Sawyer and Man left Edison: forced to engage in ‘painstaking experimentation’ to see what works. 159 U.S., at 475, 1257*1257 16 S.Ct. 75. **That is not enablement**. More nearly, it is ‘a hunting license.’ *Brenner v. Manson*, 383 U.S. 519, 536, 86 S.Ct. 1033, 16 L.Ed.2d 69 (1966).”

Amgen Inc. v. Sanofi, 598 U.S. 594, 614 (2023)

Even EPC has argued balancing the competing requirements in the new claims was “entirely unexpected” and “a direction completely contrary to conventional wisdom at the time of the invention,” this is the opposite of “**routine procedure**”

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01381
U.S. Patent No. 8,350,294

PATENT OWNER’S RESPONSE

Compellingly, none of the asserted prior art remotely suggests a transistor with a compensated gate. This is because the compensated gate invention of the ‘294 patent, which achieves two technical effects having opposite requirements for electrical conductivity, was entirely unexpected and went in a direction completely contrary to conventional wisdom at the time of the invention.

Paper No. 18 at 1

EPC's "two energy gains" theory is incorrect

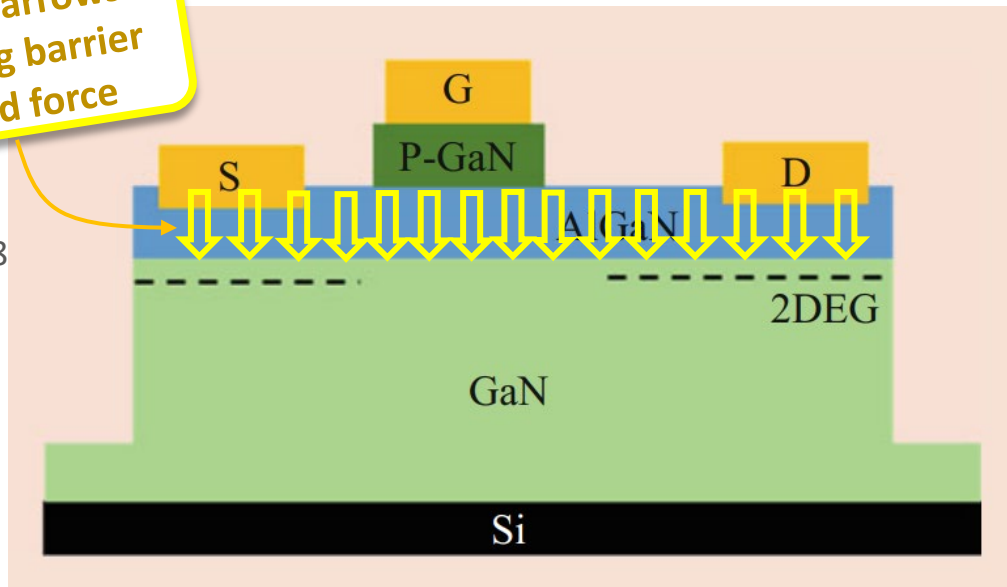
1. Routine Procedure

2. Energy gains

EPC's then resorts to an extrinsic theory of enablement based on "energy gains." But that theory is unsupported and scientifically "impossible" because a barrier separates the 2DEG from the p-GaN

Added arrows showing barrier E-field force

Ex. 2017 at 1145:1-1146:8



Incorrect

EPC: "the acceptors in the p-GaN layer ... accept electrons from the 2DEG"

Paper No. 31 at 7

Correct

Ex. 1043: AlGaIn creates "a very high-energy barrier for 2DEG electrons" electrons cannot cross. The 2DEG is depleted from "fixed negative charge."

Ex. 1043 (Meneghini) at 5-7, 15.

Not a single publication supports EPC's theory of electrons crossing the barrier

The mechanisms for depletion has nothing to do with "energy gains" or 2DEG electrons crossing the barrier.

GaN-Based Lateral and Vertical Devices

15

Matteo Meneghini , Srabanti Chowdhury, Joff Derluyn, Farid Medjdoub, Dong Ji, Jaeyi Chun , Riad Kabouche, Carlo De Santi, Enrico Zanoni, and Gaudenzio Meneghesso

P-GaN

The first demonstration of p-AlGaN or p-GaN under the gate in order to achieve normally-off operation has been realized by Panasonic in 2007 [60] despite the challenge of p-doping (Magnesium) of GaN material. Figure 15.16 describes the band diagrams with and without a p-GaN cap layer. At zero gate bias, the p-GaN layer is depleted leaving back a fixed negative charge which in turn depletes the channel. When the positive gate bias increases further, holes are injected into the pn heterojunction, which results in a higher drain current of the device.

Ex. 1043 (Meneghini) at 15

New concepts for normally-off power Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT)

Saleem Hamady

1.7.4.4. P-GaN Gate HEMT

The schematic cross-section of the normally-off p-GaN gate HEMT is shown in figure 1.25. In this structure, the lift in the conduction band is not due to p-doping of the cap layer (which is the case in the p-AlGaN cap) but rather to the discontinuity in the polarization between the barrier and the cap layers. This discontinuity creates a negative bound charge at the p-GaN/AlGaN interface, which lifts up the triangular well at the AlGaN/GaN interface and causes normally-off operation. The p-doping though still helps in increasing the forward gate voltage [39]–[44].

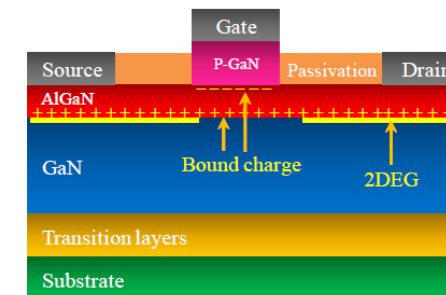


Figure 1.25 Schematic cross-section of the normally-off p-GaN gate HEMT using a p-GaN cap layer

Ex. 1047 (Hamady) at 15

1. Routine Procedure 2. Energy gains

The barrier prevents 2DEG electrons crossing, otherwise the device would not work

And then, secondly, even if the electrons were present, the electron barrier layer, the AlGa_N layer -- we call it a barrier layer because it's an electron and hole barrier layer. It doesn't allow the flow of electrons in holes across it, it blocks them from the pGa_N.

Ex. 2017 at 1145:56-1146:2

And what I mean by that is the force is pushing the electrons down. It is literally trying to keep the electrons from moving up toward the surface or toward the AlGa_N layer. I'm sorry, toward --

Ex. 2017 at 1147:20-23

PAPER

Exploring the impact of AlGa_N barrier thickness and temperature on normally-on Ga_N HEMT performance

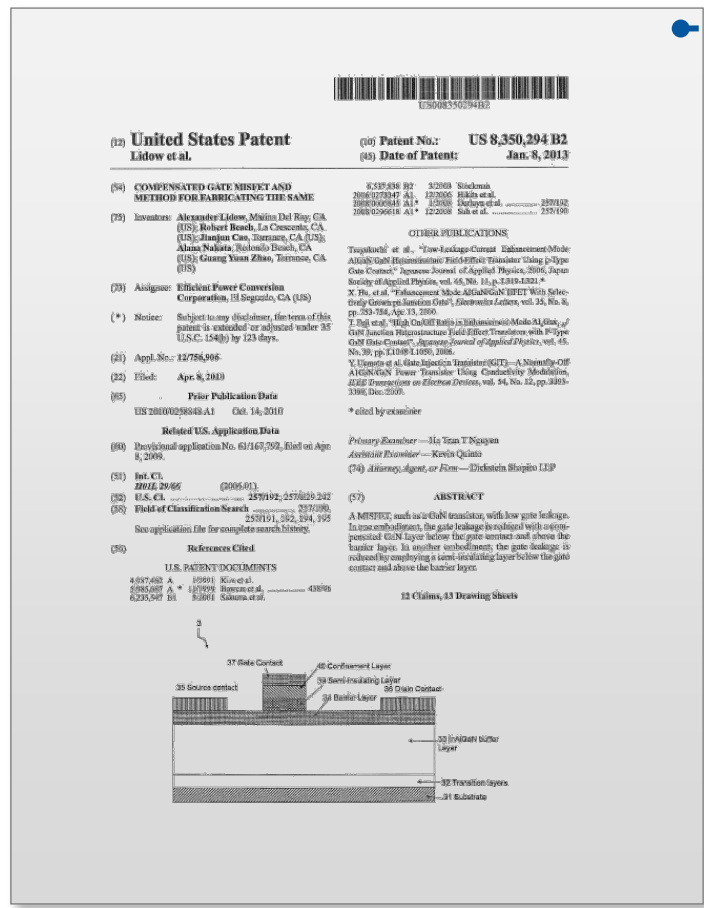
Wagma Hidayat and Muhammad Usman 

Faculty of Engineering Sciences, Ghulam Ishaq Khan Institute of Engineering Sciences and Technology, Topi, Swabi, Khyber Pakhtunkhwa, Pakistan

Over the past few years, Gallium Nitride (Ga_N) power transistors have accomplished enormous strides [12]. Due to sufficient polarization-driven surface charge at the heterojunction, undoped AlGa_N/Ga_N double-layers are favored. AlGa_N barrier in Ga_N HEMTs is employed to keep electrons contained in a two-dimensional electron gas (2DEG) layer at the AlGa_N barrier's junction with the Ga_N channel. The device's ability to effectively regulate electron mobility is made possible by this confinement. The selection of AlGa_N for the

Ex. 1044 at 1

Critically Board need not resolve the specific mechanism: the patent does not describe any of the “two energy gains” or how they would make the new claims.



“Two energy gains” or EPC’s (incorrect) 2DEG depletion mechanism: completely absent in the patent

If the “energy gains” is what allows a POSITA to make the new claims, the patent fails the enablement requirement

The statute requires the patent specification to provide “full, clear, concise, and exact terms.” If “two energy gains” is what enables the new claims, the specification is not providing a “full” description to make the new claims



“But in allowing that much tolerance, courts cannot detract from the ***basic statutory requirement that a patent's specification describe the invention ‘in such full, clear, concise, and exact terms as to enable any person skilled in the art’ to ‘make and use’ the invention.*** §112(a).”

Amgen Inc. v. Sanofi, 598 U.S. 594, 614 (2023)

Board asked about the *Wands* factors, they all point to non-enablement

- (1) the quantity of experimentation necessary,
- (2) the amount of direction or guidance presented,
- (3) the presence or absence of working examples,
- (4) the nature of the invention,
- (5) the state of the prior art,
- (6) the relative skill of those in the art,
- (7) the predictability or unpredictability of the art,
- and
- (8) the breadth of the claims

In re Wands, 858 F.2d 731, 737 (Fed. Cir. 1988)

(1), (8): Without guidance, achieving the full scope of the new claims would require undue experimentation (even if possible)

Not enabled

(2), (3): Patent provides no direction on how to make the new claims. The patent does not provide a single working example for a doping level or a device configuration

Not enabled

(4)-(7): The fact experts disagree on principles demonstrate a complex nature and unpredictability. Even EPC has argued invention was “entirely unexpected”

Not enabled

§112 Challenge	
1. Lack Enablement	Patent does not enable the competing “ semi-insulating ” and “ no 2DEG ” limitations in the new claims
2. Written description, Broadening	Patent does not support semi-insulating layer that is compensated , they are distinct, and the new claims impermissibly expand semi-insulating layer

True =
MTA denied

§103 Challenge	
3. Smith	New claims would be obvious in view of Smith and other prior art
4. Sheu	New claims would be obvious in view of Sheu

Written description and claim broadening

In the patent, the semi-insulating layer is different, used “in place of,” the compensated layer.

FIG. 10 shows a GaN transistor 2 according to a second embodiment of the present invention. GaN transistor 2 is similar to GaN transistor 1 (FIG. 2), except that GaN transistor 2 has a semi-insulating layer 39 in place of the compensated semiconductor layer 38 (FIG. 2). Semi-insulating layer

Ex. 1001 at 3:54-57

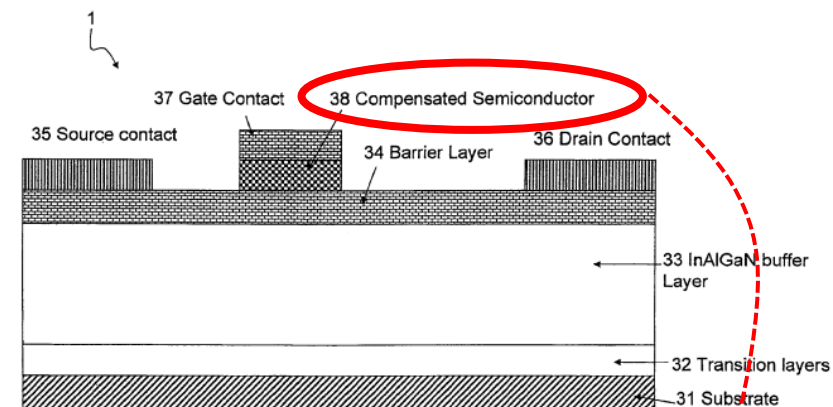


FIG. 2

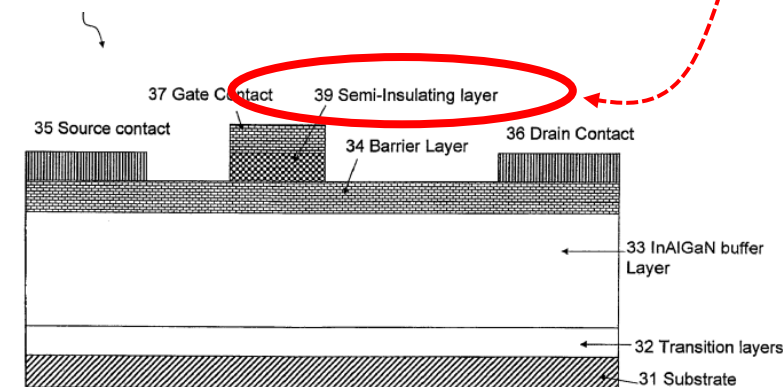


FIG. 10

Ex. 1001 at Figs. 2, 10.

The patent consistently describes semi-insulating layer (39) different from compensated layer (38) that is the sole difference between transistors 1 & 2

“How a layer that is composed entirely of semi-insulating material would not also be a semi-insulating layer?”

Trials@uspto.gov
571-272-7822

Paper: 29
Date: October 1, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD. and
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY MCGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

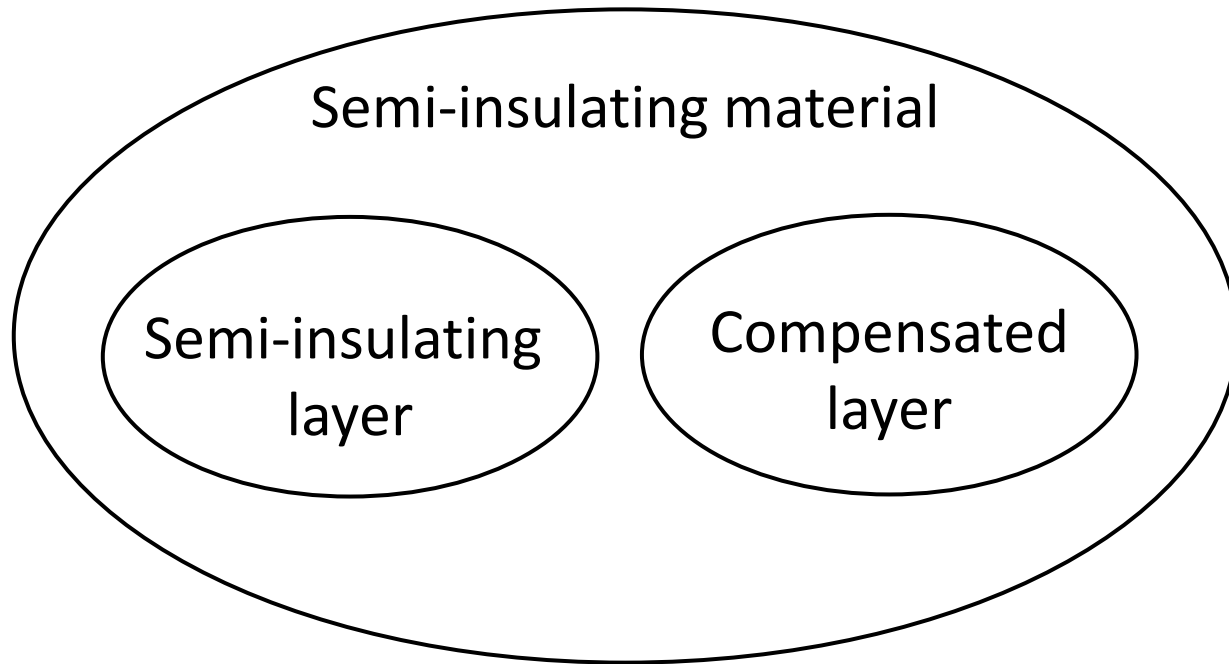
PRELIMINARY GUIDANCE
PATENT OWNER'S MOTION TO AMEND

compensated layer 38 has the electrical property of being semi-insulating, “does not mean it is or is part of ‘semi-insulating layer 39.’” Opp. 8. Petitioner does not persuasively explain, however, **how a layer that is composed entirely of a semi-insulating material would not also be a semi-insulating layer.** Thus, it would appear that the '294 patent contemplates a compensated semiconductor layer with dopants passivated by hydrogen that is also a semi-insulating layer.

After considering the parties' arguments and evidence, and on this record, we question whether Petitioner has sufficiently called into question Patent Owner's evidence that proposed substitute claims 13 and 14 are adequately supported by the written description of the '294 patent and its priority applications. This question is best resolved on a complete trial record.

Paper No. 29 at 8

In the patent a semi-insulating material is not necessarily semi-insulating layer it can be something else (e.g., the compensated layer)



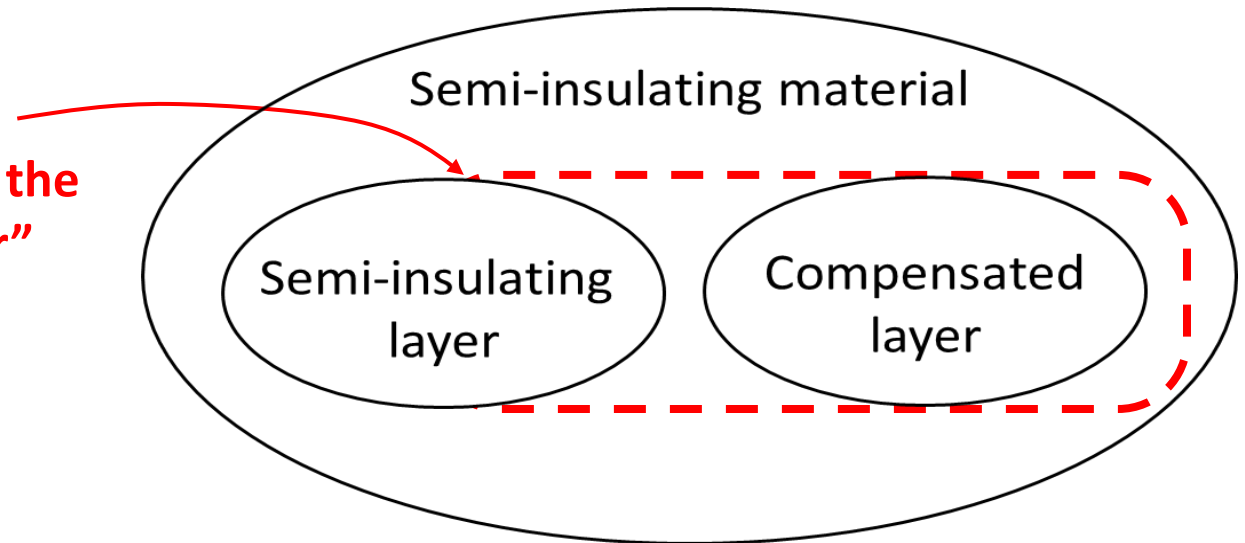
"GaN transistor 2 is similar to GaN transistor 1 (FIG. 2), except that GaN transistor 2 has a **semi-insulating layer 39** in place of the **compensated semiconductor layer 38** (FIG. 2)."

Ex. 1001 at 3:54-57

The patent consistently describes semi-insulating layer (39) is different, used "in place of," from compensated layer (38)

The new claimed expand the scope of the original “semi-insulating III-V layer” to encompass something it did not before, the “compensated GaN layer”

New claims improperly broaden the scope of “semi-insulating layer”



“This argument misstates the test for broadening. ‘[A] claim is broadened if it is broader in any respect than the original claim, even though it may be narrowed in other respects.’” *In re Rogoff*, 46 CCPA 733, 261 F.2d 601, 603 (1958);

In re Cuzzo Speed Techs., LLC, 793 F.3d 1268, 1283 (Fed. Cir. 2015).

§112 Challenge	
1. Lack Enablement	Patent does not enable the competing “ semi-insulating ” and “ no 2DEG ” limitations in the new claims
2. Written description, Broadening	Patent does not support semi-insulating layer that is compensated , they are distinct, and the new claims impermissibly expand semi-insulating layer

True =
MTA denied

True =
MTA denied

§103 Challenge	
3. Smith	New claims would be obvious in view of Smith and other prior art
4. Sheu	New claims would be obvious in view of Sheu

Obviousness Analysis

Assuming that the §112 written description, and enablement requirements are satisfied, the claims are necessarily obvious.

Issue	§112 Challenge
1. Lack Enablement	Patent does not enable the competing “ semi-insulating ” and “ no 2DEG ” limitations in the new claims
2. Written description, Broadening	Patent does not support semi-insulating layer that is compensated , they are distinct, and the new claims impermissibly expand semi-insulating layer

If enabled:

Making a transistor with no 2DEG and semi-insulating cap was a “routine procedure.” Paper No. 31 at 8-9. Then new claims are obvious.

If written description supports:

“compensated GaN layer is a semi-insulating III-N layer.” Paper No. 31 at 3. Then new claims are obvious.

If the patent provided “adequate guidance” for enablement (as EPC alleges), then the new claims are necessarily obvious in view of the prior art because the prior art provides more information (or “guidance”) to make the new claims than the patent

If the patent’s guidance is “adequate” for a “routine procedure” ...

The '294 patent provides adequate guidance as to the direction of experimentation to make its disclosure enabling. For example, the '294 patent discloses that the compensated semiconductive layer 38 has a “high doping level... lead[ing] to enhancement mode device” (EX1001, 3:16-17) where “the 2DEG region is depleted, i.e. removed, below the gate at zero applied gate bias” (EX1001, 1:47-50). As previously noted, a POSITA would understand from this

Paper No. 31 at 10

... the claim is necessarily obvious

LP, 750 F. Supp. 2d 616, 624 (E.D. Va. 2010). Here, the severe deficiencies in the '294 patent contrast the prior art. And finding the patent enables the “no 2DEG” limitation requires finding the new claims were obvious. If, increasing doping until depleting the 2DEG was “routine,” the new claims are necessarily obvious over the prior art. Finding enablement without finding obviousness would be incongruent.

Paper No. 37 at 14

Disclosure about cap layer prior art vs. the '294 patent

Information	Prior Art	294 Patent
1. Cap layer thickness	“may have a thickness of from about 2 nm to about 500 nm.” Ex. 1005 (Smith) [0087]	None
2. Cap layer doping region	“doped region 40 extends into the cap layer 34’ from about 30 Å to about 5000 Å.” Ex. 1005 [0087]	None
3. Cap layer doping concentration	“dopant concentration of from about 10 ¹⁶ to about 10 ²² cm ⁻³ .” Ex. 1005 [0087]	None
4. For critical issue on contradicting limitations: Method for adjusting cap layer passivation	Region and concentration of H “can be adjusted by forming in advance on the front-surface side of the semiconductor device 10 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these.” Ex. 1008 (Kigami) [0026] “hydrogen diffusion film 17 is supplied during a thermal treatment for selectively inactivating impurities.” Ex. 1006 (Uemoto) [0063]	None Only describes: “exposing the device to ammonia or hydrogen plasma at a high temperature,” without selectivity or adjustments

The prior art provides more guidance on how to make and adjust the passivated cap layer. If a “routine procedure” enabled the patent with its limited “adequate guidance,” the claims must be obvious

Enablement requires practicing the full scope, obviousness requires only one embodiment.

Here, the prior art disclosure is more robust than the patent.

If the patent enables the new claims (i.e., the full scope) with its limited disclosure, the prior art must teach at least an embodiment within the new claims rendering them obvious.

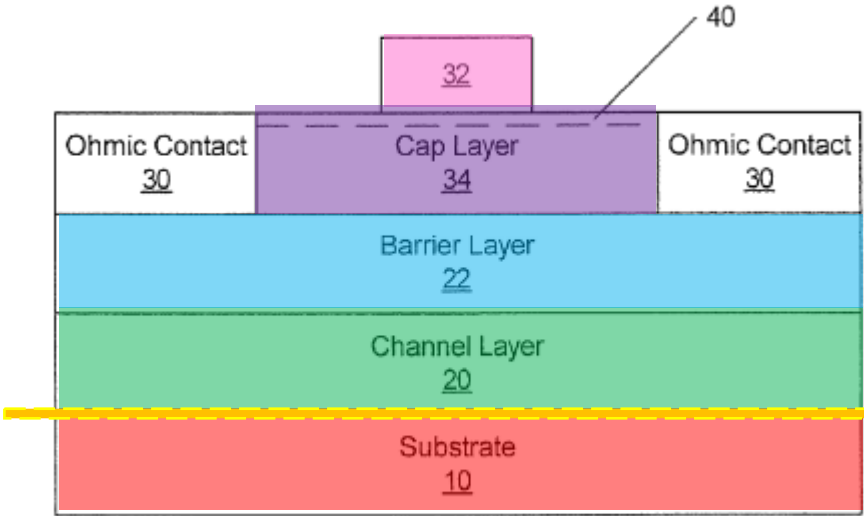
Enablement and obviousness are different. Enablement addresses whether a POSITA can make and use the claims' full scope. *Nat'l Recovery Techs., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1195-96 (Fed. Cir. 1999). But to invalidate the claims under § 103, the prior art need only render obvious *an* embodiment within the claim scope. *In re Mraz*, 455 F.2d 1069, 1073 (C.C.P.A. 1972); *DNT, LLC v. Sprint Spectrum, LP*, 750 F. Supp. 2d 616, 624 (E.D. Va. 2010) (“[I]t is possible for a claim to be obvious because of various prior art references while still non-enabled given severe deficiencies in the claim specification.”). Further, a reference is presumed operable for purposes of invalidity when it discloses the challenged claims. *In re Sasse*, 629 F.2d 675, 681 (C.C.P.A. 1980); *In re Stauffer*, 290 Fed. Appx. 327, 333 (Fed. Cir. 2008) (claims obvious over disclosure “effectively identical” to patent). And enablement of a prior art reference under § 103 is held to a lower standard than § 112. *Impax Labs. Inc. v. Aventis Pharms. Inc.*, 468 F.3d 1366, 1381-82 (Fed. Cir. 2006) (“[P]roof of efficacy is not required.”).
Paper No. 27 at 19

Obviousness in view of Smith

Disputed	13p	13. An enhancement mode column III Nitride transistor comprising:
Not Disputed	13a	a substrate,
Not Disputed	13b	a set of III-N transition layers above the substrate,
Not Disputed	13c	a III-N buffer layer above the set of transition layers,
Not Disputed	13d	a III-N barrier layer above the buffer layer,
Disputed	13e	a semi-insulating III-N layer above the barrier layer, wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
Disputed	13f	a gate comprising a gate contact and the compensated GaN layer, wherein no two dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

EPC disputes the Smith grounds meet the “compensated GaN” [13e] and “enhancement mode” limitations [13p, 13f]

Paper No. 31 at §V.B-V.E.

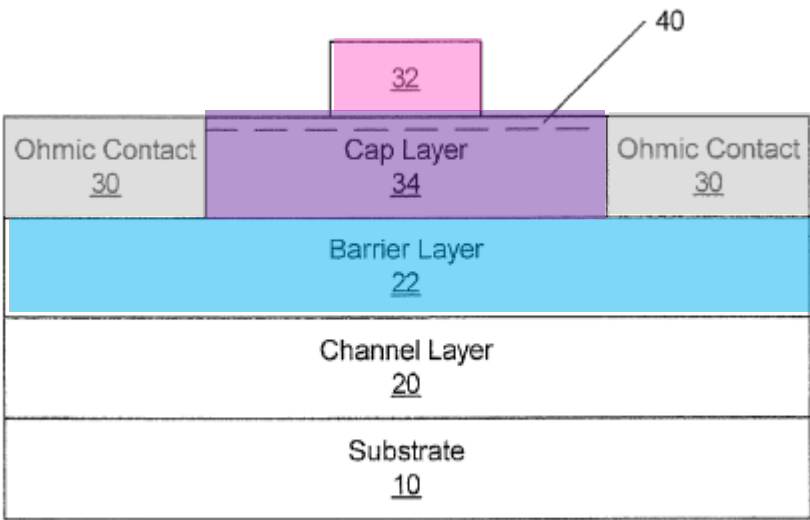


“Compensated GaN” is the same dispute discussed for Grounds 1A-1C. The remaining issue is on e-mode.

Disputed	14p	A compensated gate enhancement mode MISFET transistor comprising:
Not Disputed	14a	a III-N barrier layer beneath a gate contact,
Not Disputed	14b	a drain contact,
Not Disputed	14c	a source contact, and
Disputed	14d	a semi-insulating III-N layer between the barrier layer and the gate contact, wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
Disputed	14e	a gate comprising the gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias

EPC disputes the Smith grounds meet the “compensated GaN” [14d] and “enhancement mode” limitations [14p, 14e]

Paper No. 31 at §V.B-V.E.



“Compensated GaN” is the same dispute discussed for Grounds 1A-1C. The remaining issue is on e-mode.

**The Board accurately identified the outstanding issue of e-mode asking:
Does Smith disclose a sufficient amount of non-passivated acceptors to
result in no 2DEG at 0V (i.e. enhancement mode)?**

Trials@uspto.gov
571-272-7822

Paper: 29
Date: October 1, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD. and
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY MCGRAW, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

PRELIMINARY GUIDANCE
PATENT OWNER'S MOTION TO AMEND

We question whether Petitioner has sufficiently demonstrated at this stage that Smith discloses a sufficient amount of non-passivated acceptor type dopants to result in no two-dimensional electron gas (2DEG) region below a gate at zero volts applied gate bias (e.g., an enhancement mode device (Ex. 1001, 1:47–50)), as proposed substitute claims 13 and 14 recite. Petitioner sufficiently demonstrated for purposes of institution that hydrogen would be present in cap layer 34 of Smith. Inst. Dec. 19. Petitioner did not quantify, however, how much hydrogen would be present in this layer, as such evidence was not required to show the layer was a compensated GaN layer. *See* Pet. 39–40. But without knowledge of the level of hydrogen present in cap layer 34, it is unclear how one of ordinary skill in the art could conclude that sufficient non-passivated acceptors are present in cap layer 34, or doped region 40, to *completely* remove the 2DEG layer. *See* Ex. 1005 ¶ 87 (identifying the concentration of p-type dopants, but not the level of naturally present hydrogen).

Paper No. 29 at 11

If the patent provides “adequate guidance” for a “**routine procedure**” to enable the new claims, the new claims are obvious because the prior art provides more guidance and specific methods

Dr. Shealy explains why and how Smith’s information would make no 2DEG obvious (particularly if a “**routine procedure**” is what enables the new claims)

Dr. Shealy’s Obviousness

[0115] Further, when passivating the cap layer with hydrogen to reduce gate leakage with well-known hydrogen passivation methods, which would have been obvious over *Smith* alone and/or in view of *Kigami* and *Uemoto*, a POSITA would have sought to use the thickness, doping, and arrangement *Smith* discloses while maintaining an active dopant concentration that resulted in “no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias” in [13f]—and function as an enhancement mode device. A POSITA would have been motivated to do so to realize the benefits of enhancement mode devices, including reduced power consumption and suitability for high power applications (e.g., use of a p-GaN below gate contact provides higher threshold voltage and added safety in power switching, high power applications). *Suh2006*, 1.

Ex. 1039 [0115]

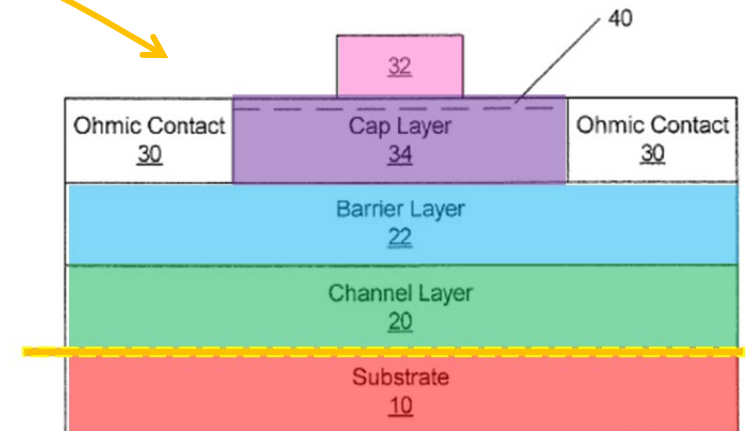
If patent's "guidance" with a "routine procedure" of increasing doping enabled **no 2DEG** limitation, the prior art disclosure is necessarily sufficient because the prior art teaches more than the patent

Information	Prior Art	294 Patent
1. Cap layer thickness	"may have a thickness of from about 2 nm to about 500 nm." Ex. 1005 (Smith) [0087]	None
2. Cap layer doping region	"doped region 40 extends into the cap layer 34' from about 30 Å to about 5000 Å." Ex. 1005 [0087]	None
3. Cap layer doping concentration	"dopant concentration of from about 10^{16} to about 10^{22} cm^{-3} ." Ex. 1005 [0087]	None
4. For critical issue on contradicting limitations: Method for adjusting cap layer passivation	Region and concentration of H "can be adjusted by forming in advance on the front-surface side of the semiconductor device 10 a material through which hydrogen ions can easily pass, a material through which it is difficult for hydrogen ions to pass, or a combination of these." Ex. 1008 (Kigami) [0026] "hydrogen diffusion film 17 is supplied during a thermal treatment for selectively inactivating impurities." Ex. 1006 (Uemoto) [0063]	None Only describes: "exposing the device to ammonia or hydrogen plasma at a high temperature," without selectivity or adjustments

If enabling, EPC's "routine procedure" would also need to apply to the prior art, which provides more "guidance" and information for an enhancement mode device

EPC's description of the "routine procedure" for enablement would need to apply for obviousness

reasonable amount of guidance. EX2024, ¶ 28. A POSITA would appreciate the teachings of the '294 patent that the acceptor concentration needs to be sufficiently high to deplete the 2DEG. As a result, a POSITA would experimentally increase the p-type doping concentration until the 2DEG is depleted. Increasing the p-type doping concentration is a routine procedure that cannot be characterized as undue experimentation. *Id.*



Paper No. 31 at 9

EPC's "routine procedure" and "energy gains" is entirely based on extrinsic evidence and the prior knowledge of a POSITA

Because the patent fails to provide key information to make the new claims, the new claims can be non-enabled and still be obvious

Information	Prior Art	294 Patent
1. Cap layer thickness	"may have a thickness of from about 2 nm to about 500 nm." Ex. 1005 (Smith) [0087]	None
2. Cap layer doping region	"doped region 40 extends into the cap layer 34' from about 30 Å to about 5000 Å." Ex. 1005 [0087]	None
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"As Defendants noted, it is possible for a claim *to be obvious because of various prior art references while still non-enabled given severe deficiencies in the claim specification.*"

DNT, LLC v. Sprint Spectrum, LP, 750 F. Supp. 2d 616, 624 (E.D. Va. 2010).

EPC's erroneous arguments

- 1. Depletion mode:** EPC incorrectly argues Smith is limited to depletion mode
- 2. Not operate:** EPC incorrectly argues Smith would not operate in e-mode

Paper No. 31 at 12-15

EPC incorrectly contends: (1) Smith is only depletion mode, and (2) Smith would not operate as an enhancement mode device

Other EPC arguments regarding compensation (e.g., that passivation is counterintuitive) addressed above

1. Depletion mode b. Not Operate

EPC is wrong that Smith is depletion mode.

Smith does not specify depletion or enhancement mode operation and EPC argument that Smith is not “fairly considered” e-mode based on its structure in Fig. 2 is unsupported

But EPC arbitrarily drew gaps small, nothing in Smith requires small gaps, or a d-mode operation.

EPC essentially argues the cap layer is too wide to be “fairly considered” e-mode

EPC's argument

[059]. That is not the case. Even if the cap layer of FIG. 2A was not in direct contact with both ohmic contacts, so that a small gap existed between the cap layer and the ohmic contacts, Smith still would not be fairly considered to be directed to an enhancement mode transistor. EX2024, ¶ 34. For example, even with a small gap between the cap layer and the ohmic contacts, if the transistor of FIG. 2A were setup to have no 2DEG below the gate at zero volts bias, when a positive voltage is applied to the gate, the 2DEG would only replenish generally directly beneath the gate. *Id.* Because the access regions are significantly wider than the small gaps between the cap layer and ohmic contacts, they would remain depleted of free electrons, and the transistor would be inoperable. *Id.*

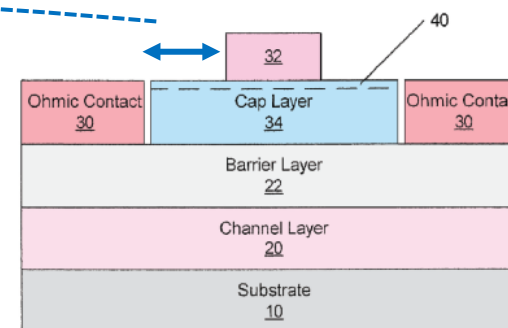


Figure 2A

EX1005, FIG. 2A (modified).

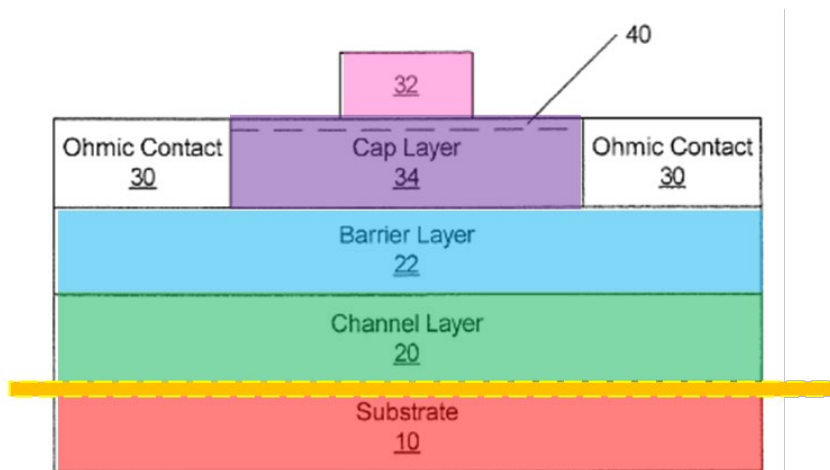
Smith is not limited to d-mode, has the structure of e-mode

a. Depletion mode

b. Not Operate

There is no requirement for cap layer to be narrow.
Smith's architecture is the same even EPC's expert recognizes as characteristic of enhancement mode

EPC's expert description of e-mode



Same
structure

Has a p-type material (cap layer 34) over the barrier layer (barrier layer 22) "it can deplete the 2DEG ... create an enhancement-mode transistor"
no reason to limit Smith to d-mode

31. A GaN transistor can include a variety of structures. The transistor is supported by the substrate that provides a stable mechanical support for the thin epitaxial layers grown on the substrate.⁴ The following layers in some transistors can be epitaxially grown on the substrate to achieve certain properties of the desired transistor: a nucleation layer(s) that nucleates epitaxial growth on the substrate. A buffer layer, for example, a GaN buffer layer, serves as the host material for the 2DEG electron channel located between the source and drain. A barrier layer, for example, an AlGaN barrier layer as described as an embodiment of the '294 patent, can be grown on top of the buffer layer and has the purpose of inducing the 2DEG in the GaN buffer layer. On top of the barrier layer, a p-type GaN (p-GaN) gate semiconductor can be grown. Importantly, if a p-type gate material is present over the barrier layer, it can deplete the 2DEG under the gate to create an enhancement mode, i.e., normally "OFF", transistor.

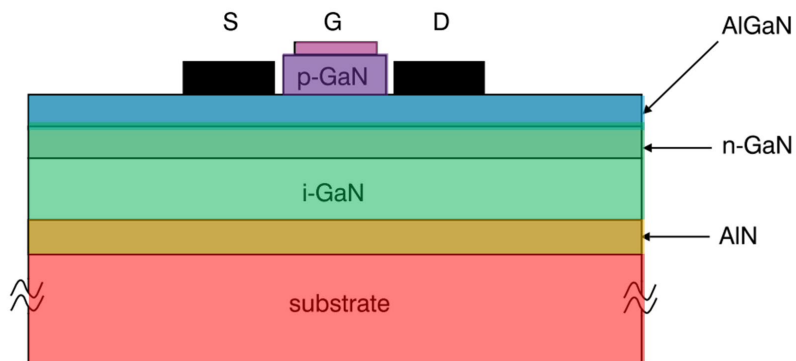
Smith has the same p-type layer for e-mode

a. Depletion mode

b. Not Operate

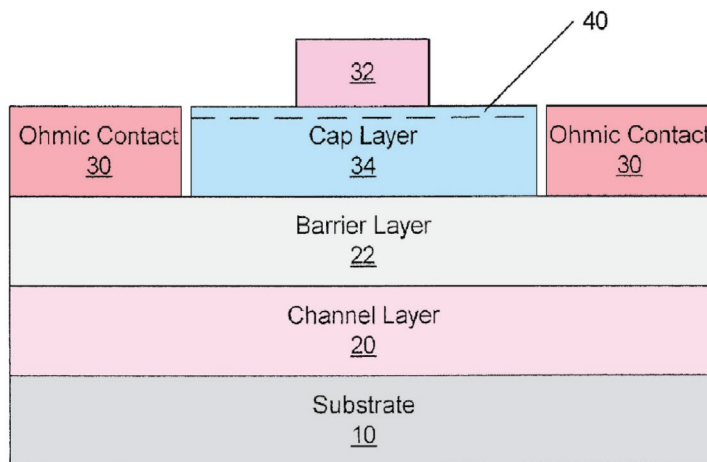
Even EPC's interpretation of Smith (with small gaps between ohmic contacts and capping layers) has the same architecture of the typical e-mode device matching the same configuration as Hu (first e-mode device) and the 294 patent

Hu



Ex. 1014 at 1

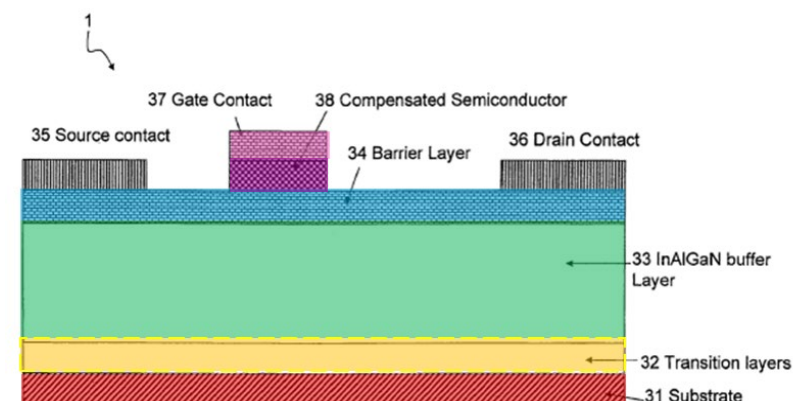
Smith (as EPC modified*)



*Nothing limits the gaps to be "small"

Paper No. 31 at 13

294 patent



Ex. 1001 at Fig. 2

FIG. 2

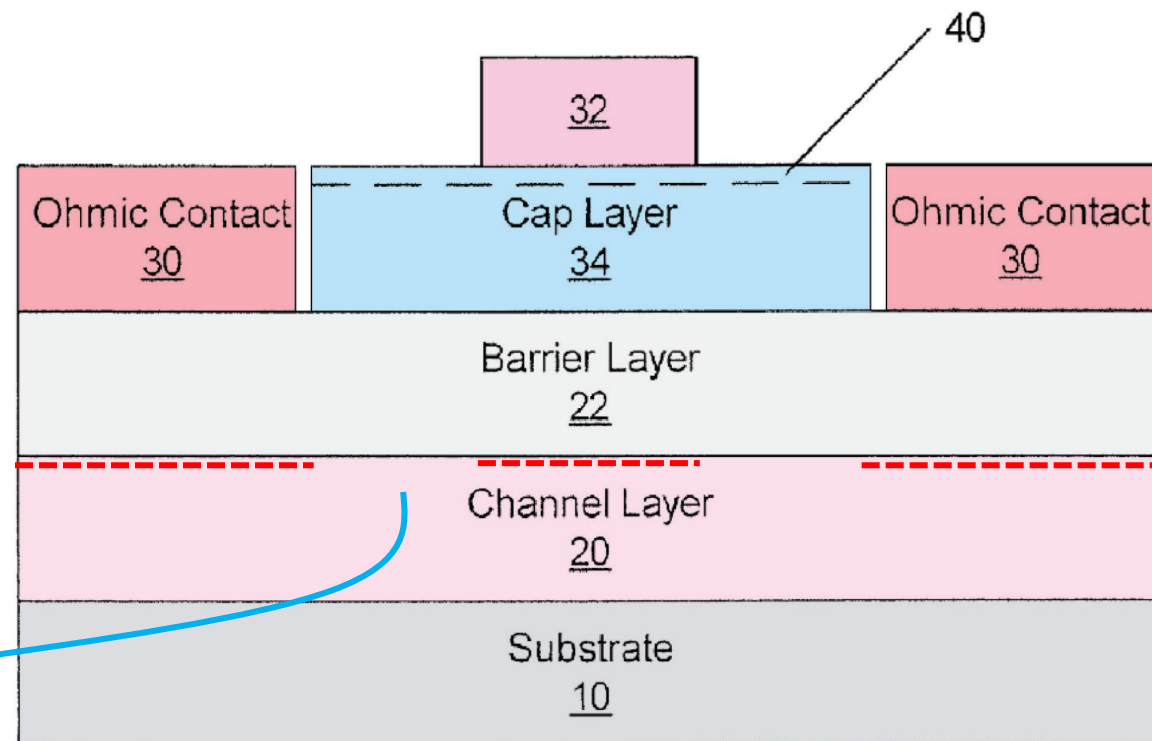
Same cap layer structure: All of these can be e-mode.
No reason to limit Smith to d-mode.

a. Depletion mode

b. Not Operate

EPC's argument

at 32. But even if Smith's transistor were modified so that no 2DEG exists below the gate at zero volts applied gate bias, it would still not work as an enhancement mode transistor (e.g., because the 2DEG would not be replenished enough to turn the transistor on upon application of a positive gate voltage). EX2024, ¶¶ 38-40.



EPC argues 2DEG would have discontinuities because cap layer is wider

But EPC *arbitrarily* drew gaps small, and EPC's operability argument is both irrelevant and incorrect

a. Depletion mode

b. Not Operate

Obviousness case law is clear: references need not enable their own disclosure because a POSITA can modify



“In general, a prior art reference asserted under § 103 ***does not necessarily have to enable its own disclosure***, i.e., be ‘self-enabling,’ to be relevant to the obviousness inquiry. See *Symbol Techs., Inc. v. Opticon, Inc.*, 935 F.2d 1569, 1578 (Fed. Cir. 1991) (‘While a reference must enable someone to practice the invention in order to anticipate under § 102(b), ***a non-enabling reference may qualify as prior art for the purpose of determining obviousness*** under § 103.’).”

Raytheon Techs. Corp. v. Gen. Elec. Co., 993 F.3d 1374, 1380 (Fed. Cir. 2021).

a. Depletion mode

b. Not Operate

Drs. Shealy & Lebby: EPC's argument that 2DEG is not replenished close to contacts is scientifically incorrect, "the electric field would not be limited to below the gate."

[065] Instead, I agree with the explanation Dr. Michael Lebby provided, which Dr. Schubert seems to criticize in his declaration. Ex. 2009 ¶122. I agree with Dr. Lebby's explanation that applying sufficient voltage would affect the entire channel, not only below the gate as Dr. Schubert argues. And a POSITA would have known how to select the voltage to permit reconstituting the entire 2DEG channel. Dr. Schubert argues Dr. Lebby's explanation "is scientifically inaccurate." Ex. 2009 ¶122. But he does not explain why. I agree with Dr. Lebby that when applying a voltage to the gate electrode, the electric field would not be limited to below the gate it would reach other regions. And the larger the gate voltage applied, the greater magnitude and reach of the electric field emanating from the gate electrode for inducing a 2DEG. Ex. 1033 [065]-[066]

While Dr. Schubert presented no support, Drs. Shealy and Lebby modifications of dimensions and voltages are supported by the known "design space of a p-GaN capped." Ex. 1015 (PhD thesis from 2008)

Enhancement-Mode GaN-Based HEMTs for High-Voltage Switching Applications

A Dissertation submitted in partial satisfaction

of the requirements

for the Doctoral

degree in Electrical and

Computer

In chapter 4, modification of surface barrier height by insertion of a p-GaN cap layer is described. The design space of a p-GaN capped AlGaIn/GaN HEMT is presented. Insertion of a thin, fully depleted p-GaN cap layer below the gate was tried to deplete the 2DEG below for enhancement-mode operation. The fabrication and the performances of high- V_{BD} devices with source-connected field-plates are presented. The design, fabrication and the performance of devices scaled to large dimensions are also presented. Performances of p-GaN capped devices were improved by using an AlN interlayer and the design space of p-GaN/AlGaIn/AlN/GaN HEMTs is also presented.

Ex. 1015 at 13, 66-69

If the “routine procedure” is enabling the new claims, they are obvious over the prior art because the prior art teaches more. EPC’s d-mode and not operation arguments fail

Issue	§112 Challenge
1. Lack Enablement	Patent does not enable the competing “semi-insulating” and “no 2DEG” limitations in the new claims
2. Written description, Broadening	Patent does not support semi-insulating layer that is compensated, they are distinct, and the new claims impermissibly expand semi-insulating layer

If enabled by “routine” must be obvious

Issue	§103 Challenge
3. Smith	New claims would be obvious in view of Smith and other prior art
4. Sheu	New claims would be obvious in view of Sheu

True = MTA denied

Obviousness in view of Sheu

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申請日期: 92	IPC分類
申請案號: 92101440	H01L 29/92, 21/5232
(以上各欄由本局填註)	
發明專利說明書 200114540	
發明名稱	場效電晶體結構及其製程
中文	Field effect transistor and method of fabricating the same
英文	
發明人 (共2人)	姓名 (中文) 1. 許進恭 2. 賴軍志 姓名 (英文) 1. Jinn-Kong Sheu 2. Wei-Chih Lai 國籍 (中英文) 1. 中華民國 TW 2. 中華民國 TW 住所 (中文) 1. 台南縣將軍鄉將軍村70號 2. 嘉義縣大林鎮水源路46巷38號 住所 (英文) 1. No. 70, Jiang-Jiun Tsuen, Jiang-Jiun Shiang, Tainan County, Taiwan, R.O.C. 2. No. 38, Lane 46, Shueiyuan Rd., Dalin Jen, Chiai, Taiwan 622.
申請人 (共1人)	名稱或姓名 (中文) 1. 元坤光電科技股份有限公司 名稱或姓名 (英文) 1. South Epitaxy Corporation 國籍 (中英文) 1. 中華民國 TW 住所 (中文) 1. 台南科學工業園區台南縣新市鄉大順九路16號 (本地址與前向貴局申請者相同) 住所 (英文) 1. No. 16, Da-Shun 9 Rd., Hsin-Shun Hsiang, Tainan Science-Based Industrial Park, Taiwan, R.O.C. 代表人 (中文) 1. 鄭朝元 代表人 (英文) 1. Chao-yuan Cheng

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第 1 頁

Page 1 of 24

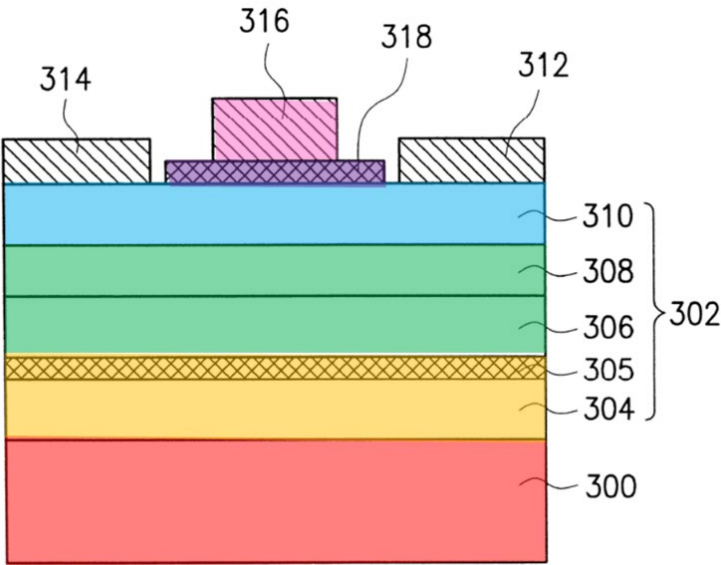
INNOSCIENCE EXHIBIT 1035
INNOSCIENCE v. EPC
IPR2023-01381

Ex. 1036 at Cover

Sheu is similar to Smith but expressly shows the p-GaN directly below the gate

Sheu discloses GaN transistors with all the conventional layers and a cap layer directly and only below the gate and formed to be insulating

- Prior art §102(b)/(e): Published August 1, 2004
- Discloses GaN HEMT transistors with a GaN insulating layer in the gate structure for a MISFET.

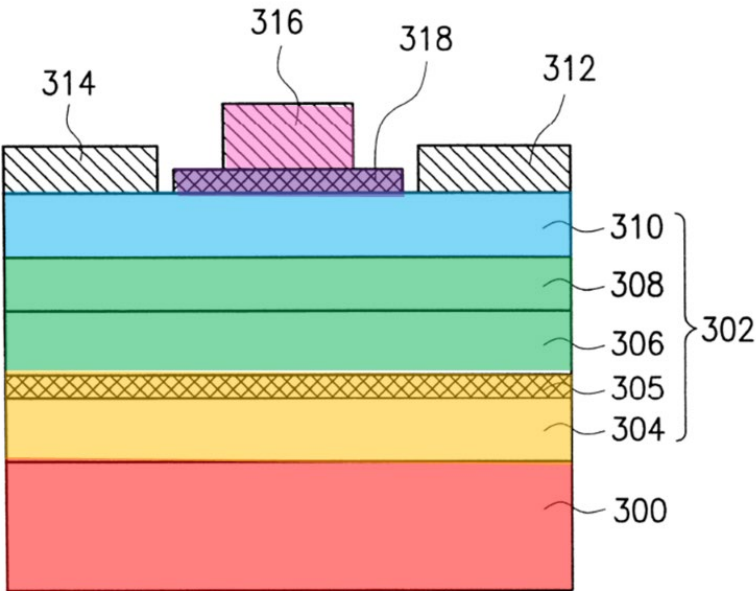


Ex. 1036 at Fig. 7 (annotated)

Disputed	13p	An enhancement mode column III Nitride transistor comprising:
Not Disputed	13a	a substrate,
Not Disputed	13b	a set of III-N transition layers above the substrate,
Not Disputed	13c	a III-N buffer layer above the set of transition layers,
Not Disputed	13d	a III-N barrier layer above the buffer layer,
Disputed	13e	a semi-insulating III-N layer above the barrier layer, wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
Disputed	13f	a gate comprising a gate contact and the compensated GaN layer, wherein no two dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias.

EPC disputes the Sheu/Kigami meet the “compensated GaN” [13e] and “enhancement mode” limitations [13p, 13f]

Paper No. 31 at 12-18



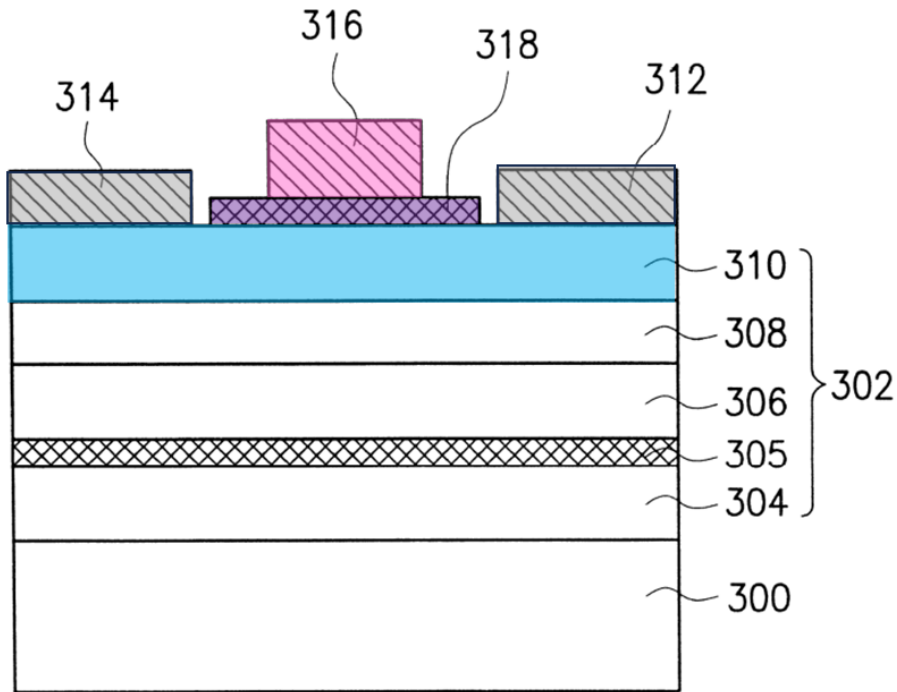
Ex. 1036 at Fig. 7 (annotated)

Disputed	14p	A compensated gate enhancement mode MISFET transistor comprising:
Not Disputed	14a	a III-N barrier layer beneath a gate contact,
Not Disputed	14b	a drain contact,
Not Disputed	14c	a source contact, and
Not Disputed	14d	a semi-insulating III-N layer between the barrier layer and the gate contact, wherein the semi-insulating III-N layer comprises a compensated GaN layer containing acceptor type dopant atoms passivated with hydrogen, and
Disputed	14e	a gate comprising the gate contact and the compensated GaN layer, wherein no two-dimensional electron gas (2DEG) region exists below the gate at zero volts applied gate bias

Paper No. 27 at 46-49

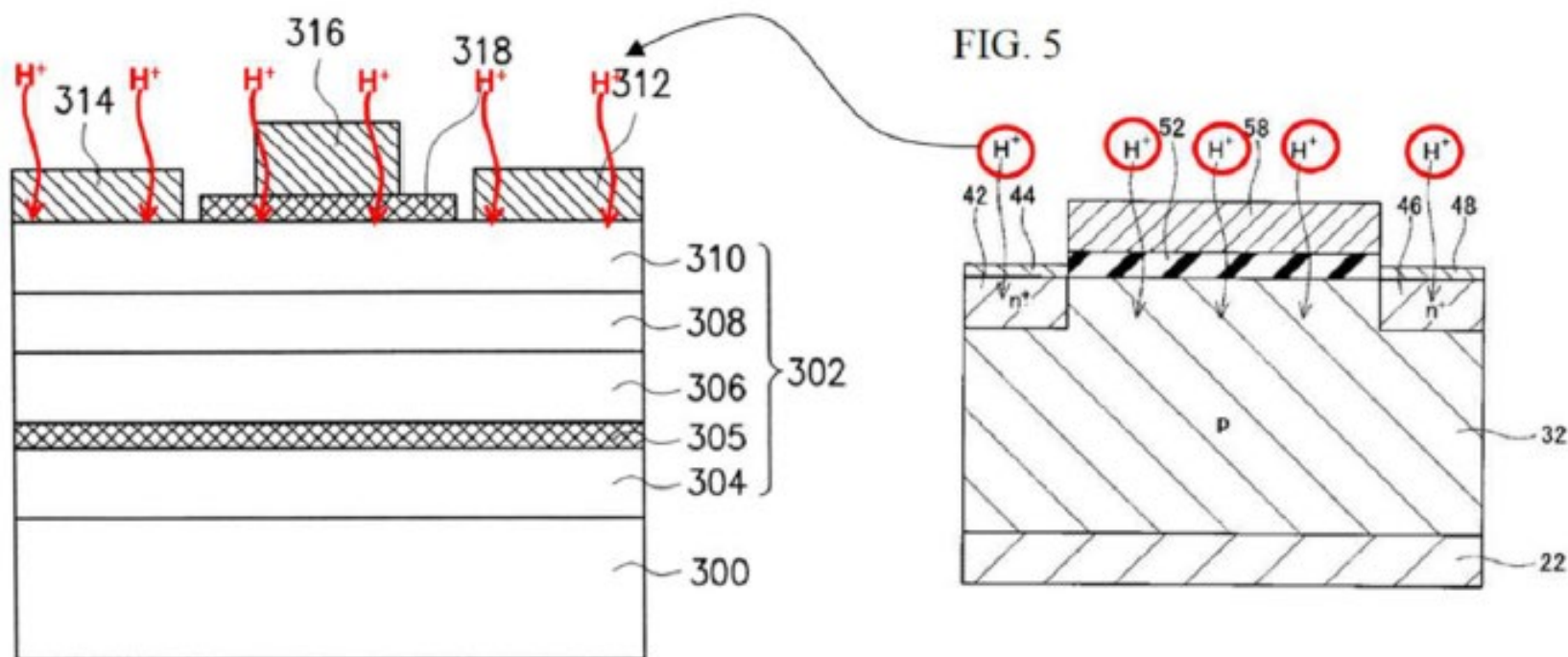
EPC disputes the Sheu grounds meet the “compensated GaN” [14d] and “enhancement mode” limitations [14p, 14e]

Paper No. 31 at 12-18



Ex. 1036 at Fig. 7 (annotated)

Applying Kigami's known localized H passivation technique to Sheu's known device making layer 318 p-doped but not conductive

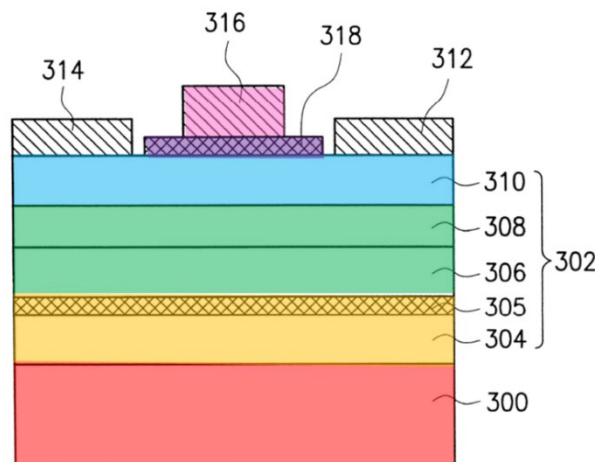


In ground 1B, cap layer 34 meets the “compensated GaN” under any construction

Issue	EPC's Argument	Correct Resolution
1. Is Sheu limited to depletion mode devices?	POSITA would appreciate Sheu discloses a depletion mode, not an enhancement mode transistor.	No. Sheu does not specify enhancement or depletion mode operation and it has the same architecture of the typical p-GaN enhancement mode device.
2. Motivation to combine: Why would a POISTA use Kigami passivation in Sheu?	There is no motivation to combine because Sheu and Kigami have different gate structure and Sheu's layer "may be originally n-type"	A POSITA would have been motivated to employ Kigami's technique

1. Enhancement/depletion 2. Motivation to Combine

Sheu does not specify depletion or enhancement mode operation. Instead, its architecture is the same even EPC's expert recognizes as characteristic of enhancement mode



Has a p-type material (layer 318) over the barrier layer (layer 310) "it can deplete the 2DEG ... create an enhancement-mode transistor"

EPC's expert description of e-mode

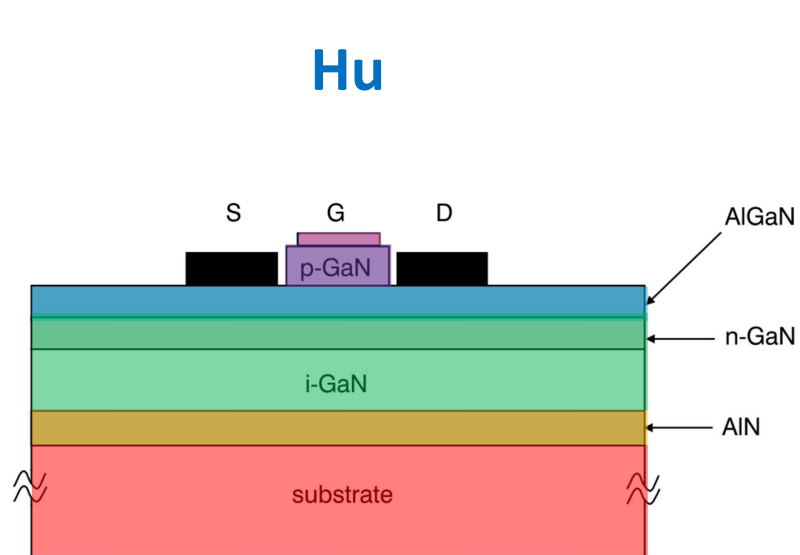
31. A GaN transistor can include a variety of structures. The transistor is supported by the substrate that provides a stable mechanical support for the thin epitaxial layers grown on the substrate.⁴ The following layers in some transistors can be epitaxially grown on the substrate to achieve certain properties of the desired transistor: a nucleation layer(s) that nucleates epitaxial growth on the substrate. A buffer layer, for example, a GaN buffer layer, serves as the host material for the 2DEG electron channel located between the source and drain. A barrier layer, for example, an AlGaN barrier layer as described as an embodiment of the '294 patent, can be grown on top of the buffer layer and has the purpose of inducing the 2DEG in the GaN buffer layer. On top of the barrier layer, a p-type GaN (p-GaN) gate semiconductor can be grown. Importantly, if a p-type gate material is present over the barrier layer, it can deplete the 2DEG under the gate to create an enhancement mode, i.e., normally "OFF", transistor.

Ex. 2009 [031]

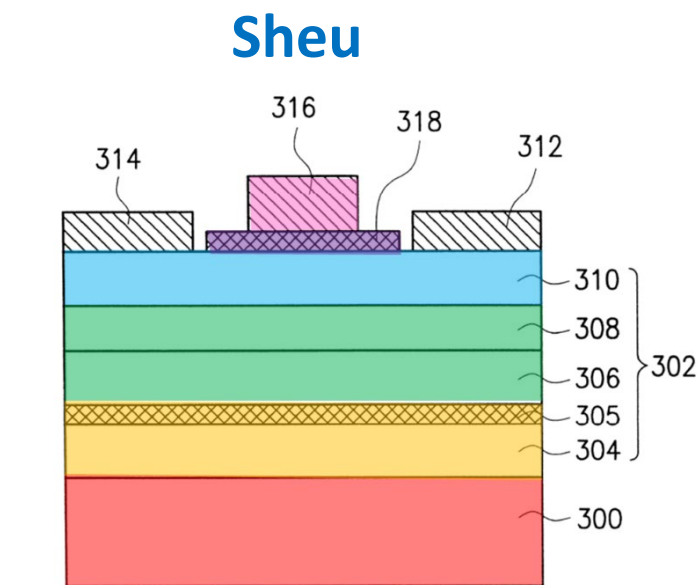
Sheu has the same enhancement-mode architecture

1. Enhancement/depletion 2. Motivation to Combine

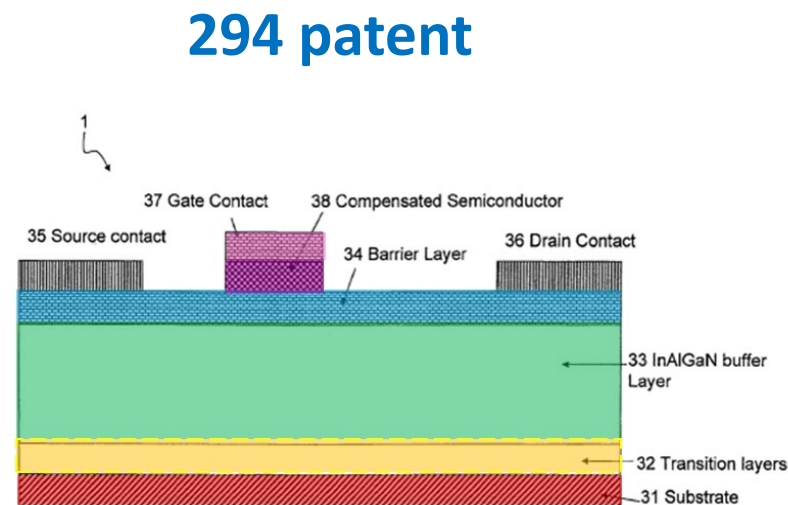
Sheu has the same architecture of the typical e-mode device matching the same configuration as Hu (first e-mode device) and the 294 patent



Ex. 1014 at 1



Ex. 1036 at Fig. 6



Ex. 1001 at Fig. 2 FIG. 2

Same cap layer structure: All of these can be e-mode.
No reason to limit Sheu to d-mode.

Sheu's FIG. 4 does not limit it to d-mode

1. Enhancement/depletion 2. Motivation to Combine

Sheu's FIG. 4 applies to a different embodiment (FIG. 1 and 3 vs. FIG. 6) and does not limit to depletion operation because it only shows "reverse voltage" and "gate leakage current." It also shows no current at 0V (consistent with e-mode)

FIG. 4 shows a diagram of a relationship between reverse bias voltage and gate leakage current in the field effect transistor of FIGS. 1 and 3. Referring to FIG. 4, curve A is a relationship between the reverse bias voltage and the gate leakage current of a conventional gallium nitride field effect transistor without the gate insulating layer, while curve B is a relationship between the reverse bias voltage and the gate leakage current of the gallium nitride field effect transistor with a GaN-based gate insulating layer of high resistance value in this embodiment. From the FIG. 4, it can be clearly seen that by comparison between the gate leakage current of the conventional gallium nitride field effect transistor and the gate

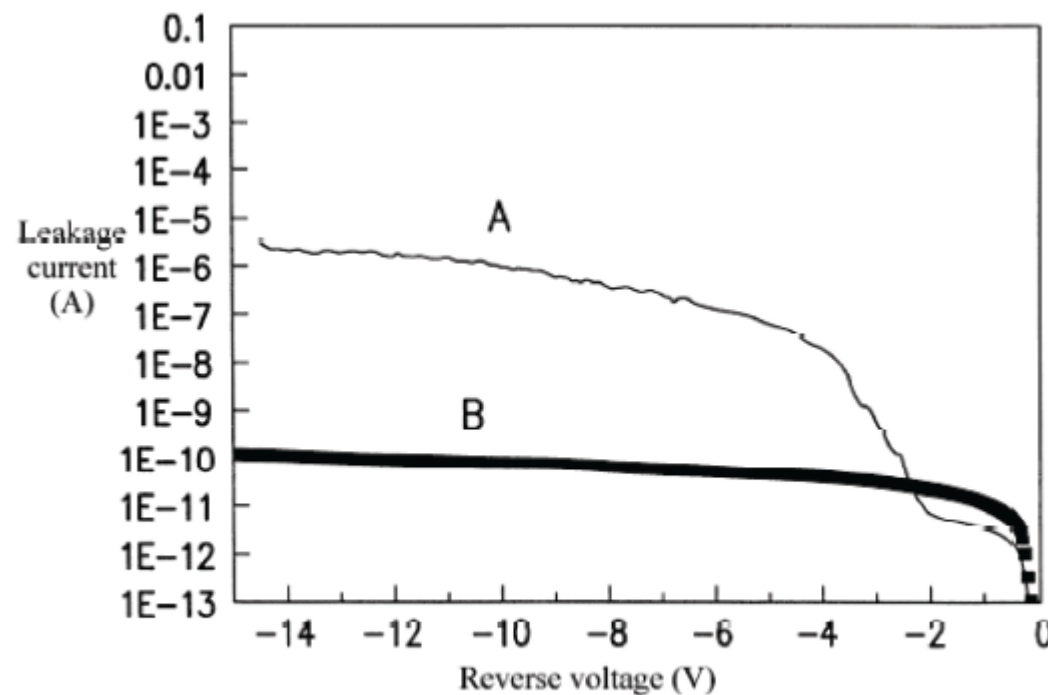


FIG. 4

1. Analogous art: Both describe III-nitride transistors
2. KSR known technique applied to known device: Kigami's known technique is applied to Sheu's known device
3. KSR's some teaching, suggestion, motivation (TSM) in Kigami to modify or combine.
4. Reasonable expectation of success: POSITA had reasonable expectation that Kigami's technique would further Sheu's goals of doped but not conductive
5. Answer to the Board's question
6. EPC's counter arguments are incorrect

Sheu and Kigami are analogous art, they both specifically describe techniques for fabricating MIS GaN transistors and both seek to improve breakdown voltage

Sheu, p. 4

This practice attempts to improve the lattice matching characteristics between the gate insulating layer and the substrate, so that the **metal-insulating layer-semiconductor field effect transistor (MISFET) has good electrical characteristics**

Ex. 1038 at 4

Kigami ¶[0009]

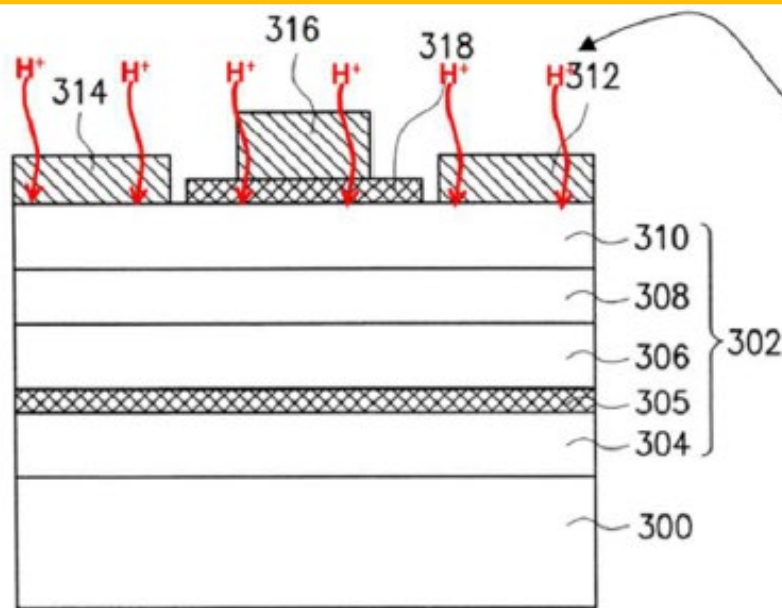
It is possible to obtain an **MIS-type gate structure** that has a combination of a low threshold voltage and a high withstand voltage.

Ex. 1038 [0009]

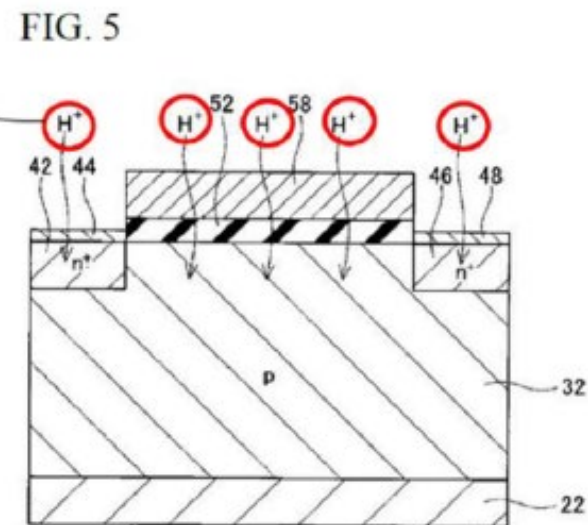
Applying Kigami's technique to Sheu's device

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

Sheu/Kigami is applying a known technique (Kigami's hydrogenation technique to control conductivity) to a known device (Sheu's transistor) ready for improvement (improving robustness by increasing resistance) to yield predictable results (increasing the resistance of layer 318)



Known device ready to make layer 318 nonconductive



Known technique to make layer nonconductive

Some TSM to use Kigami's technique in Sheu

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

Kigami expressly suggests applying its technique in devices that like Sheu use Mg dopants and seek a doped but nonconductive layer

[0012]

The p-type impurity preferably is magnesium.

As mentioned above, because the magnesium diffusion rate is extremely high, it is difficult to form a III-V group compound semiconductor in which the magnesium concentration is locally lowered. In the present invention, by forming a composite with the hydrogen atoms, the magnesium is inactivated. By locally inactivating the magnesium, a region can be formed in which the concentration of the "activated magnesium" is locally low. Even if the concentration of the "activated magnesium" is set low locally, because the concentration of the magnesium itself is the same as that of other regions, magnesium does not diffuse in from other regions. The present invention is particularly useful in situations in which magnesium is used as a p-type impurity.

Ex. 1008 [0012]

Sheu uses Mg as p-type impurity

Some TSM to use Kigami's technique in Sheu

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

Kigami expressly suggests applying its technique to improve transistor frequency and robustness, complementing Sheu's objective

Sheu, p. 10

the GaN-based insulating layer mentioned above can also be used as an insulating buffer layer between a semiconductor epitaxial layer and the substrate, which can effectively eliminate the side-gating effect or the back-gating effect, and output conductance is substantially reduced, which is **more conducive to high-frequency operation.**

Ex. 1036 at 4

Paper No. 27 at 36-37

Kigami [0029]

By forming the local region 34, in which hydrogen is unevenly distributed, at the junction interface between the gate-insulating film 52 and the semiconductor layer 32, the interface energy level can be reduced. **The effects of stabilized threshold voltage, increased switching speed, and the like are obtained**

Ex. 1008 at [0029]

Kigami suggests using its technique to improve the device robustness Sheu targets

POSITA would have expected success implementing Kigami's suggested technique in Sheu because H passivation was a well-known technique to make layers doped but nonconductive

[0141] Furthermore, in my opinion a POSITA would have reasonably expected to succeed in applying *Kigami's* hydrogenation process to *Sheu's* transistor. By the priority date of the '294 patent, it was well-known how hydrogen-passivated magnesium in GaN layers affects the layer's conductivity. The passivation of magnesium with hydrogen had been known since the early 1990s. Ex. 1018. *Kigami* also provides experimental data showing the effect of hydrogen passivation on transistor performance. *Kigami*, [0028], Fig. 6. And *Kigami* also explains the mechanisms for hydrogen diffusion and impurity passivation, detailing how the hydrogen diffusion would be performed and how it would affect the magnesium dopants. *Kigami*, [0022]-[0026], Fig. 5. Given the general knowledge about doping and hydrogen passivation in p-type GaN, and *Kigami's* disclosures, a POSITA would have reasonably expected to succeed in applying *Kigami's* hydrogenation techniques to *Sheu's* device structure, and specifically layer 318, when seeking to control the layer's resistivity.

Ex. 1039 at [0141]

In its preliminary guidance, the Board understood Sheu's "enhancing" of resistance is lowering the resistance so: "why would a POSITA use Kigami to increase the resistance?"

Trials@uspto.gov
571-272-7822

Paper: 29
Date: October 1, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD. and
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01381
Patent 8,350,294

Before JON B. TORNQUIST, JEFFREY W.
KIMBERLY McGRAW, Administrative Patent Judge,
TORNQUIST, Administrative Patent Judge.

PRELIMINARY GUIDANCE
PATENT OWNER'S MOTION TO AMEND

Short answer: the Board's preliminary understating of Sheu was incorrect, Sheu (like Kigami) seeks high resistivity.

We have concerns at this stage whether Petitioner has sufficiently articulated why one of ordinary skill in the art, at the time of the invention, would have passivated Sheu's gate insulating layer 318 in view of Kigami's teachings. Sheu teaches that its gate insulating layer 318 "may also have a dopant to *enhance* the resistance value of the GaN-based gate insulating layer 318." Ex. 1036, 10 (emphasis added). Given that Sheu teaches adding dopant, such as magnesium, we understand Sheu's teaching of "enhance[ing] the resistance value" as a teaching to lower gate insulating layer 318's resistance value. *Id.* Conversely, Kigami teaches inactivating p-type impurities via hydrogen atoms so "the resistance of the III-V group compound semiconductor is *made high*." Ex. 1008 ¶ 7 (emphasis added). As a result, Kigami's purpose for its passivation technique may be inapposite to Sheu's objective for its gate insulating layer 318. Should Patent Owner further pursue proposed substitute claims 13 and 14, we encourage the parties to address this issue further.

Paper No. 29 at 15

EPC agrees. Paper No.31 at 22: "dopants themselves that enhance the resistance value, which a POSITA would understand to mean may increase the resistance value."

Answer: Sheu's "enhancing" is increasing the resistance

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC

When Sheu describes "enhancing" the resistance of layer 318, Sheu is not describing lowering resistance, Sheu describes increasing the layer resistance to have "good insulating characteristics;" this squarely aligns with Kigami's passivation

Sheu targets "good insulation"

In the present invention, a GaN-based material is employed as the gate insulating layer, which has good lattice matching characteristics with the GaN-based semiconductor layer, and has good insulation characteristics after being doped with appropriate dopants (metals such as carbon, magnesium and iron). Therefore, the field effect transistor of the present invention has superior electrical characteristics.

Ex. 1036 at 6

Sheu describes the co-doping (C, Mg, Fe)

Similar to the previous embodiment, the GaN-based gate insulating layer 318 in this embodiment may also have a dopant to enhance the resistance value of the GaN-based gate insulating layer 318 (about 109 ohms to 1012 ohms/□), such as metal such as carbon, magnesium, iron or a combination of these materials, and these dopants (metals such as carbon, iron, and magnesium) are, for example, doped in the epitaxy process.

Ex. 1036 at 10

Paper No. 37 at 15-16

Kigami techniques improves insulating (resistance is higher)

[0007]

The present inventors observed the use of a phenomenon described in Non-Patent Document 2. In Non-Patent Document 2, it is reported that, when hydrogen atoms exist in a III-V group compound semiconductor that contains a p-type impurity, the hydrogen atoms form a composite with the p-type impurity that exists in the vicinity, the p-type impurity is inactivated, and the resistance of the III-V group compound semiconductor is made high, and it reports the need to remove the hydrogen atoms from the III-V group compound semiconductor. On the other hand, in the present invention, the phenomenon in which the p-type impurity is inactivated by hydrogen atoms is actively utilized. By utilizing the

Ex. 1008 [0007]

Sheu's "enhancing" is consistent with Kigami's passivation → Both seek to increase resistivity

- a) **Different gate structure:** EPC incorrectly argues Sheu and Kigami have “entirely different” gate
- b) **Originally n-type:** EPC incorrectly argues Sheu needs active dopants because it was originally n-type

Paper No. 31 at 18-23

Other EPC arguments regarding compensation (e.g., counterintuitive) addressed above

EPC incorrectly contends Sheu has an “entirely different” gate structure than Kigami and could not be passivated because it “may be originally n-type”

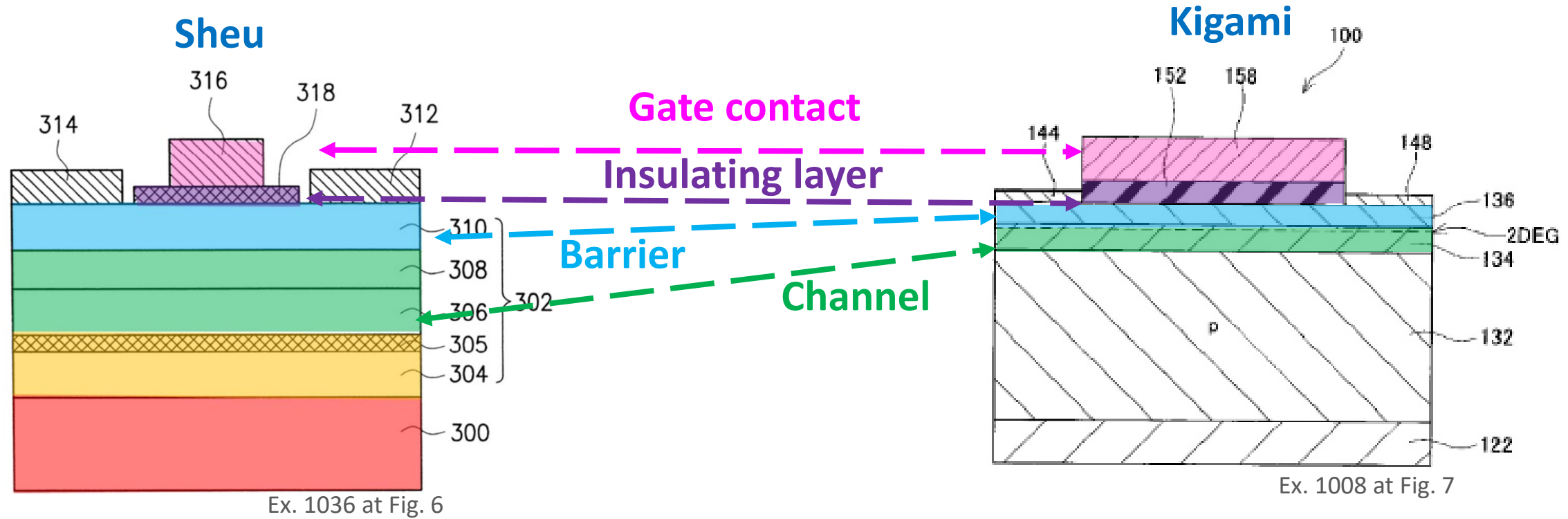
EPC's argument of "entirely different" gate structure

Incorrect

science

- 1. Analogous
- 2. Apply technique
- 3. TSM
- 4. Expectation
- 5. Board Question
- 6. Rebuttal to EPC
- 6a) Diff. Gate Structure

EPC challenges the combination arguing gate structures are "entirely different" because Kigami's channel is hydrogenated. But the two devices have very similar gate structure with: **gate**, **insulating layer**, **barrier**, and **channel** in the same order and arrangement



EPC's argument of "may be originally n-type"

Incorrect

1. Analogous 2. Apply technique 3. TSM 4. Expectation 5. Board Question 6. Rebuttal to EPC 6b) Originally n-type

Nothing supports EPC speculation that layer 318 "may be originally n-type," Sheu instead specifies 318 is doped p-type and deep-level dopants

Sheu does not reference compensation or passivation with hydrogen at all, but rather states that one or more dopants (carbon, magnesium, and/or iron) may be used "to enhance the resistance value" of the GaN layer 318. EX1036 at 10; EX2024, ¶ 55. That is, it is the dopant that enhances the resistance value, which a POSITA would mean may increase the resistance value. EX2024, ¶ 55. The reason adding a p-type dopant, such as Mg, would increase the resistance is that the gate insulating layer may be originally n-type.

EPC Speculation

Passivating those dopants with hydrogen would negate the purpose for which Sheu introduced dopants in its device and go against its teachings. *Id.* Accordingly, a POSITA would not be motivated to combine Sheu and Kigami, under either of Petitioner's claim constructions. *Id.* Paper No. 31 at 22.

Similar to the previous embodiment, the GaN-based gate insulating layer 318 in this embodiment may also have a dopant to enhance the resistance value of the GaN-based gate insulating layer 318 (about 109 ohms to 1012 ohms/□), such as metal such as carbon, magnesium, iron or a combination of these materials, and these dopants (metals such as carbon, iron, and magnesium) are, for example, doped in the epitaxy process.

Ex. 1036 at 10.

Nothing indicates layer 318 being "originally n-type." Instead layer 318 is doped with p-type and deep-level dopants. Kigami would not "negate the purpose" but control resistivity passivating Mg.

1. Analogous art: Both describe III-nitride transistors Same transistors → Obvious to combine
2. KSR known technique applied to known device: Kigami's known technique is applied to Sheu's known device Known technique, known device → Obvious to combine
3. KSR's some teaching, suggestion, motivation (TSM) in Kigami to modify or combine. Sheu/Kigami TSM → Obvious to combine
4. Reasonable expectation of success: POSITA had reasonable expectation that Kigami's technique would further Sheu's goals of doped but not conductive Expectation to increase resistance → Obvious to combine
5. Answer to the Board's question Both Kigami and Sheu increase resistance → Obvious to combine
6. EPC's counter arguments are incorrect Sheu/Kigami have Similar gate structure → Obvious to combine

Issue	EPC's Argument	Correct Resolution
1. Is Sheu limited to depletion mode devices?	POSITA would appreciate Sheu discloses a depletion mode, not an enhancement mode transistor.	Sheu does not specify enhancement or depletion mode operation and it has the same architecture of the typical p-GaN enhancement mode device.
2. Motivation to combine: Why would a POISTA use Kigami passivation in Sheu?	There is no motivation to combine because Sheu and Kigami have different gate structure and Sheu's layer "may be originally n-type"	A POSITA would have been motivated to employ Kigami's technique

No. Sheu not limited to d-mode

Analogous art, two KSR rationales, expectation of success

If the “routine procedure” is enabling the new claims, they are obvious over the prior art because the prior art teaches more. EPC’s different structure and n-type doping fail

Issue	§112 Challenge
1. Lack Enablement	Patent does not enable the competing “semi-insulating” and “no 2DEG” limitations in the new claims
2. Written description, Broadening	Patent does not support semi-insulating layer that is compensated, they are distinct, and the new claims imperm expand semi-insulating layer

If enabled by “routine” must be obvious

Issue	§103 Challenge
3. Smith	New claims would be obvious in view of Smith and other prior art
4. Sheu	New claims would be obvious in view of Sheu

True = MTA denied

True = MTA denied

Appendix

At the ITC Innoscence presented 2 grounds of invalidity:

(1) Uemoto by itself

(2) Beach189, not an issue in this IPR, with Kigami for claims 2-3

Ground	Primary ref	Claim 1 (compensated GaN)	Claim 2 (H passivation)	Claim 3 (Mg doping)
1	Uemoto	(alone)	(alone)	(alone)
2	Beach189	(alone)	(w/ Kigami)	(w/ Kigami)

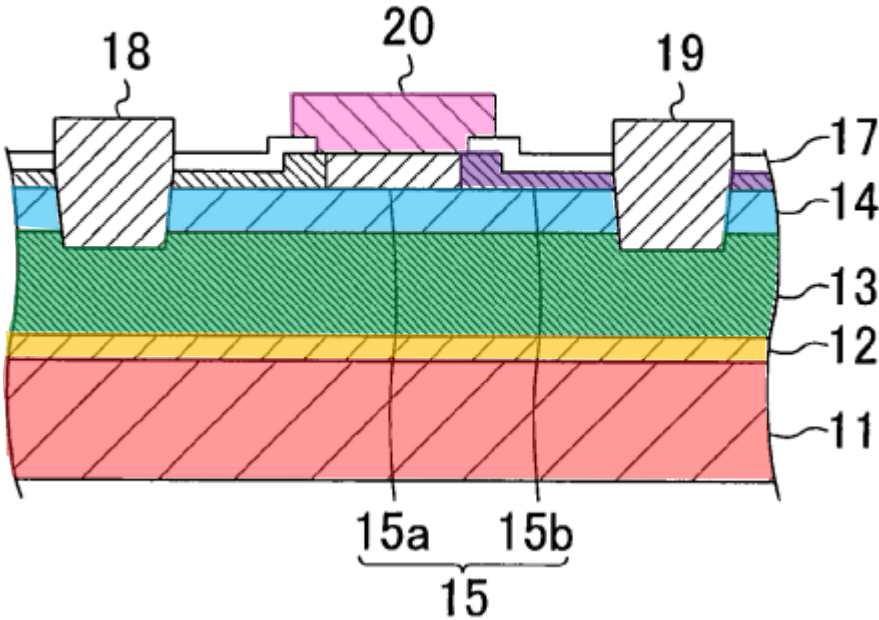
Only claims 1-3 at issue, Beach189
had an inequitable conduct issue

ITC Opinion

1p	A column III-Nitride transistor comprising:
1a	a substrate,
1b	a set of III-N transition layers above the substrate,
1c	a III-N buffer layer above the set of transition layers,
1d	a III-N barrier layer above the buffer layer,
1e	a compensated GaN layer above the barrier layer, and
1f	a gate contact above the compensated GaN layer.
2	The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.
3	The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.



ITC found Uemoto *by itself* anticipated (102) all elements in claims 1-3 but for the “set of III-N transition layers”



Applying a “clear and convincing” standard, ITC found Uemoto by itself did not meet the “set of III-N transition layers” [1b]

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

CERTAIN SEMICONDUCTOR DEVICES, AND
METHODS OF MANUFACTURING SAME AND
PRODUCTS CONTAINING THE SAME

INV. NO. 337-TA-1366

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND

For all of the reasons noted in the anticipation analysis above, and after considering the objective indicia of non-obviousness discussed later, I find Uemoto does not teach or suggest transition layers. I further determine Innoscence has not met its burden to adduce “clear and convincing evidence” that an ordinary artisan at the time of the invention “would have had reason to attempt to make” the Uemoto device with the required set of transition layers. *See PharmaStem Therapeutics*, 491 F.3d at 1360. All three asserted claims of the '294 patent require the set of transition layers missing from Uemoto. Accordingly, I find Innoscence has failed to present an affirmative defense that claims 1, 2, and 3 are invalid under 35 U.S.C. § 103 as obvious in view of Uemoto.

Ex. 2022 at 87

ITC Opinion

1p	A column III-Nitride transistor comprising:	✓
1a	a substrate,	✓
1b	a set of III-N transition layers above the substrate,	✓
1c	a III-N buffer layer above the set of transition layers,	✓
1d	a III-N barrier layer above the buffer layer,	✓
1e	a compensated GaN layer above the barrier layer, and	✓
1f	a gate contact above the compensated GaN layer.	✓
2	The transistor of claim 1, wherein the compensated GaN layer contains acceptor type dopant atoms passivated with hydrogen.	✗
3	The transistor of claim 2, where the acceptor type atoms are selected from the group consisting of Mg, Zn, Be and Ca.	✗

ITC found Beach189 anticipated claim 1. But found it did not meet claims 2 and 3 disagreeing with a Beach189/Kigami combination

Applying a “clear and convincing” standard, agreed compensation was “well-known” ... but argued there was an “unrestricted world of compensation”

Ignored Kigami's teaching that its technique allows adjusting the region where H is introduced (at [0026]) improperly limiting Kigami to a single passivation layer arguing it “cast doubt” on the combination

required by claim 2. Although EPC's witness Dr. Lidow established that “compensating a semiconductor is a well-known idea,” Tr. at 280:7-16 (Lidow), the record also establishes that a GaN layer doped with magnesium could “just as easily” be compensated with oxygen or silicon, see Tr. at 390:5-391:7 (Beach). Innoscence has not shown “by clear and convincing evidence” that an ordinary artisan at the time of the invention “would have had reason to attempt to make” the Beach189 field plate device with GaN having a dopant compensated by hydrogen as opposed to some other element to arrive at the invention described in claim 2. See *PharmaStem Therapeutics*, 491 F.3d at 1360. In fact, Innoscence's stated motivation to combine—because “Beach189 does not specify any particular method for forming the disclosed compensated GaN field plate”—would leave the artisan with an unrestricted world of compensation choices, not lead the artisan to the specific compensation process in Kigami. See RIB at 42.

Additionally, EPC's expert Dr. Schubert opined that Kigami discloses hydrogen passivation below a gate insulator to reduce threshold voltage, which is further down in the semiconductor structure than the compensated GaN layer recited in the '294 patent and field plate of Beach189. Tr. 957:17-958:17 (Schubert); CDX-0003 at slide 18; Kigami ¶ [0004]. This casts additional doubt on a motivation to apply Kigami's compensation method to Beach189.

In requiring that obviousness showed preference of “compensated by hydrogen as opposed to some other element,” the ITC misapprehended the law which only requires a “suitable option,” not the best option



“Our precedent, however, ***does not require that the motivation be the best option, only that it be a suitable option*** from which the prior art did not teach away. See *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed.Cir.2013); *Bayer Healthcare Pharm., Inc. v. Watson Pharm., Inc.*, 713 F.3d 1369, 1376 (Fed.Cir.2013).”

PAR Pharm., Inc. v. TWI Pharms., Inc., 773 F.3d 1186, 1197-98 (Fed. Cir. 2014);

ITC found:

- (1) Uemoto did not meet [1b] failing to invalidate the claims
- (2) Beach189 invalidates claim 1 but not claims 2-3, disagreeing with the combination

Ground	Primary ref	Claim 1 (compensated GaN)	Claim 2 (H passivation)	Claim 3 (Mg doping)
1	Uemoto	(alone) Not invalid, only missing [1b]	(alone) Not invalid	(alone) Not invalid
2	Beach189	(alone) Invalid	(w/Kigami) Not invalid	(w/Kigami) Not invalid

CNIPA determinations have limited relevance

EPC relies on CNIPA for its obviousness and enablement conclusion, but CNIPA applies a different law, evaluated different claims, it is “of limited relevance to the instant proceedings”



“the Board considered that the decision does not involve the U.S. patents at issue in these proceedings, is not based on U.S. law, and ***is thus of limited relevance to the instant proceedings.***”

Smith & Nephew, Inc. v. Convatec Techs., Inc., IPR2013-00097, Paper 76 (PTAB Feb. 24, 2014)