UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	08/29/2017	9748347	200371-00053	7150

24998 7590 08/09/2017

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 64 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jianjun Cao, Torrance, CA;
Efficient Power Conversion Corporation, ElSegundo, CA;
Alexander Lidow, Marina Del Rey, CA;
Alana Nakata, Redondo Beach, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/447,069	07/30/2014	2822	730	200371-00053	16	3

CONFIRMATION NO. 7150

CORRECTED FILING RECEIPT

24998
Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

OC000000088893936

Date Mailed: 07/10/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jianjun Cao, Torrance, CA;
Alexander Lidow, Marina Del Rey, CA;
Alana Nakata, Redondo Beach, CA;

Applicant(s)

Efficient Power Conversion Corporation, ElSegundo, CA;

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This application is a CIP of 13/838,792 03/15/2013 PAT 8890168
which is a DIV of 12/756,960 04/08/2010 PAT 8404508
which claims benefit of 61/167,777 04/08/2009
This application 14/447,069
claims benefit of 61/860,976 08/01/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/07/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/447,069**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PART B–FEE(S) TRANSMITTAL

Complete and send this form, together with the applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22314-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note Use Block 1 for any change of address)

24998
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's Name)
(S-signature)
(Date)

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
14/447,069	07/30/2014	Jianjun Cao	E0101.0053	7150

TITLE OF INVENTION: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

APPLN: TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480.00			$495.00	07/05/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
J. C. Niesz	2822	

1. Change of correspondence address or indication of "Fee Address" (37CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered attorney or agent. If no name is listed, no name will be printed

1. Blank Rome LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

1a. NAME OF ASSIGNEE: Efficient Power Conversion Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): El Segundo, California

Please check the appropriate assignee categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 5

4b. Payment of Fees(s): **(Please first reapply and previously paid fee shown above)**
☐ A check is enclosed
☒ Payment be credit card. Form PTO-2038 is attached
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 23-2185 (enclose an extra copy of this form)

5. Change of Entity Status (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature  Date June 28, 2017

Typed or printed name Stephen A. Soffen Registration No. 31,063

PTOL-85 Part B (06-14) Approved for use through 10/31/2016 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

200371.00053/105851323

Docket No.: E0101.0053
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: J. C. Niesz

REQUEST FOR CORRECTED FILING RECEIPT

Office of Initial Patent Examination's Filing Receipt Corrections
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant hereby requests that a corrected Filing Receipt be issued in the above-identified patent application. The official Filing Receipt received by Applicant, a copy of which is attached hereto, has an error in the Title.

The title should read, --GATE WITH SELF-ALIGNED LEDGE[[D]] FOR ENHANCEMENT MODE GaN TRANSISTORS--. A Request for Corrected Filing Receipt requesting correction of the title was originally filed on January 23, 2015 (copy attached).

Applicant additionally requests that all pertinent U.S. Patent and Trademark Office records relating to the subject application be changed to reflect this correction.

200371.00053/105851399

Dated: June 28, 2017

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

Docket No.: E0101.0032
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit:

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: N/A

REQUEST FOR CORRECTED FILING RECEIPT

Office of Initial Patent Examination
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants hereby request that a corrected Filing Receipt be issued in connection with the above-identified patent application. The Domestic Application was omitted from the official Filing Receipt received by Applicants. The Domestic Application should read as the following:

This appln claims benefit of 61/860,976 08/01/2013

The official Filing Receipt received by Applicant has an incorrect title. The title should read as the following:

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

A marked-up copy of the official Filing Receipt showing the error and necessary correction is attached.

Applicant additionally requests that all pertinent U.S. Patent and Trademark Office records relating to the subject application be changed to reflect this correction.

Dated: January 23, 2015

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
1825 Eye Street NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/447,069	07/30/2014	2811	730	E0101.0032.US	16	3

CONFIRMATION NO. 7150

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

FILING RECEIPT

OC000000070079080

Date Mailed: 08/07/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jianjun Cao, Torrance, CA;
Alexander Lidow, Marina Del Rey, CA;
Alana Nakata, Redondo Beach, CA;

Applicant(s)

Efficient Power Conversion Corporation, ElSegundo, CA

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Applications for which benefit is claimed - ~~None.~~ This appln claims benefit of 61/860,976 08/01/2013
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/07/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/447,069**

Projected Publication Date: 02/04/2016

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

Title

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

Electronic Acknowledgement Receipt	
EFS ID:	21298362
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Deborah Proctor
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	23-JAN-2015
Filing Date:	30-JUL-2014
Time Stamp:	18:02:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		E01010032.pdf	2205240 829312d606bdc7e636a20967821d95d74250915c	yes	39

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	3
	Other Reference-Patent/App/Search documents	4	5
	Foreign Reference	6	34
	Request for Corrected Filing Receipt	35	39
Warnings:			
Information:			
	Total Files Size (in bytes):	2205240	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet

Inventor Information

Inventor Number::	1
Given Name::	Jianjun
Family Name::	Cao
City of Residence::	Torrance
State or Province of Residence::	CA
Country of Residence::	US
Street of mailing address::	5323 Bindewald Rd.
City of mailing address::	Torrance
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90505-8712

Inventor Number::	2
Given Name::	Alexander
Family Name::	Lidow
City of Residence::	Marina Del Rey
State or Province of Residence::	CA
Country of Residence::	US
Street of mailing address::	129 Channel Pointe Mall
City of mailing address::	Marina Del Rey
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90292

Inventor Number::	3
Given Name::	Alana
Family Name::	Nakata
City of Residence::	Redondo Beach
State or Province of Residence::	CA
Country of Residence::	US
Street of mailing address::	611 N. Irena Avenue, Unit M
City of mailing address::	Redondo Beach
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90277-2968

Correspondence Information

Correspondence Customer Number::	24998

Application Information

Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R?::	None
Sequence submission?::	None
Computer Readable Form (CRF)?::	No
Title::	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

Attorney Docket Number::	E0101.0032.US
Request for Early Publication?::	No
Request for Non-Publication?::	No
Total Drawing Sheets:	6
Small Entity?::	Yes
Petition included?::	No
Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2::	No
Authorization to Permit Access to the Instant Application by the Participating Offices::	No
This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013::	No

Representative Information

Representative Customer Number::	24998

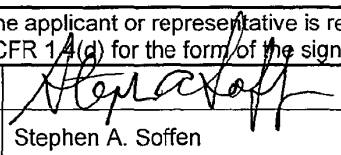
Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This application	An application claiming the benefit under 35 USC 119(e)	61/860,976	08/01/13

Applicant Information

Applicant Type::	Assignee
Organization Name::	Efficient Power Conversion Corporation
Street of mailing address::	909 N. Sepulveda Boulevard
	Suite 230
City of mailing address::	El Segundo
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90245

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.			
Signature		Date	July 30, 2014
Name (Print/Type)	Stephen A. Soffen	Registration No. (Attorney/Agent)	31,063

Electronic Patent Application Fee Transmittal				
Application Number:	14447069			
Filing Date:	30-Jul-2014			
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS			
First Named Inventor/Applicant Name:	Jianjun Cao			
Filer:	Stephen A. Soffen/Cheryl de Lopez			
Attorney Docket Number:	200371-00053			
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	480	480

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	5	3	15
		Total in USD ($)		**495**

Electronic Acknowledgement Receipt	
EFS ID:	29638078
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	200371-00053
Receipt Date:	28-JUN-2017
Filing Date:	30-JUL-2014
Time Stamp:	16:08:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$495
RAM confirmation Number	062917INTEFSW16092900
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		issuefeeOFRp053.pdf	422576 c412da03162e1725da9fbf757a9534b4e07f3fe7	yes	13
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Issue Fee Payment (PTO-85B)		1	1	
	Request for Corrected Filing Receipt		2	13	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32343 976e894b0a96dac59150872b68856fe63c87bb25	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	454919		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24998 7590 04/05/2017

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER
NIESZ, JAMIE C

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/05/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

TITLE OF INVENTION: GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/05/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24998 7590 04/05/2017
Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

TITLE OF INVENTION: GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/05/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
NIESZ, JAMIE C	2822	257-194000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 04/05/2017

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
NIESZ, JAMIE C	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/05/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/447,069	Applicant(s) CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed February 16, 2017*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *12,13 and 16*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JAMIE C NIESZ/
Primary Examiner, Art Unit 2822

DETAILED ACTION

1. This office action is in response to the Amendment filed February 16, 2017.

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. The application has been amended as follows:

In the claims:

Claim 12. A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

forming a GaN layer;

forming a barrier layer on the GaN layer;

depositing source and drain contacts on the barrier layer;

depositing a p-type gate material on the barrier layer;

depositing a gate metal on the p-type gate material;

forming a photoresist over the gate metal;

etching the gate metal and the p-type gate material, wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type

gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

Allowable Subject Matter

5. Claim 12, 13 and 16 are allowed.

6. The following is an examiner's statement of reasons for allowance:

7. Regarding claim 12, the prior art of record fails to disclose "wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal," as shown in Applicant's Figs. 6B and 6C, in combination with the rest of the limitations in the claim. These limitations, in the method as claimed in claim 12, are neither anticipated nor made obvious by the prior art of record, in the Examiner's opinion.

8. Claims 13 and 16 depend from claim 12 and are therefore also found allowable.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE C. NIESZ whose telephone number is (303)297-4333. The examiner can normally be reached on Monday through Friday 10-6 EST.

11. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMIE C NIESZ/
Primary Examiner
Art Unit 2822

Notice of References Cited	Application/Control No. 14/447,069	Applicant(s)/Patent Under Reexamination CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2006/0273347 A1	12-2006	Hikita; Masahiro	H01L29/7783	257/192
*	B	US-2006/0157735 A1	07-2006	Kanamura; Masahito	H01L29/42316	257/194
*	C	US-2009/0072272 A1	03-2009	Suh; Chang Soo	H01L29/1066	257/194
*	D	US-2010/0258843 A1	10-2010	Lidow; Alexander	H01L29/1066	257/192
*	E	US-2004/0119110 A1	06-2004	Park, Sung-Chul	H01L21/28273	257/315
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	Art Unit
	JAMIE C NIESZ	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/42316 and H01L 21/283	Dec. 14, 2015	JCN
H01L 29/42316 and H01L 21/283	Jan. 31, 2017	JCN
H01L 29/42316 and H01L 21/283	March 20, 2017	JCN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	194	Dec. 14, 2015	JCN
257	194	Jan. 31, 2017	JCN
257	194	March 20, 2017	JCN

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search EAST (see search history)	Dec. 14, 2015	JCN
Updated Text Search EAST (see search history)	Nov. 15, 2016	JCN
Inventor Search EAST	Nov. 15, 2016	JCN
Updated Text Search EAST (see search history)	Jan. 31, 2017	JCN
Updated Text Search EAST (see search history)	March 20, 2017	JCN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Interference Search EAST (see search history)	Dec. 14, 2015	JCN
	Updated Interference Search EAST (see search history)	Jan. 31, 2017	JCN
	Updated Interference Search EAST (see search history)	March 20, 2017	JCN

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BIB DATA SHEET

CONFIRMATION NO. 7150

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/447,069	07/30/2014 RULE	257	2822	E0101.0032.US

APPLICANTS

Efficient Power Conversion Corporation, ElSegundo, CA;

INVENTORS

Jianjun Cao, Torrance, CA;
Alexander Lidow, Marina Del Rey, CA;
Alana Nakata, Redondo Beach, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 13/838,792 03/15/2013 PAT 8890168
which is a DIV of 12/756,960 04/08/2010 PAT 8404508
which claims benefit of 61/167,777 04/08/2009
This application 14/447,069 07/30/2014
claims benefit of 61/860,976 08/01/2013

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
08/07/2014

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /Jamie C Niesz/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	6	16	3

ADDRESS

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403
UNITED STATES

TITLE

GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

FILING FEE RECEIVED		
730	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	**Art Unit**
	JAMIE C NIESZ	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2015	12/14/2015	11/15/2016	01/31/2017	03/20/2017				
	1	÷	N	-	-	-				
	2	÷	N	-	-	-				
	3	÷	N	-	-	-				
	4	÷	N	-	-	-				
	5	÷	N	-	-	-				
	6	÷	N	-	-	-				
	7	÷	N	-	-	-				
	8	÷	N	-	-	-				
	9	÷	N	-	-	-				
	10	÷	N	-	-	-				
	11	÷	N	-	-	-				
1	12	÷	✓	✓	✓	=				
2	13	÷	✓	✓	✓	=				
	14	÷	✓	✓	✓	-				
	15	÷	✓	✓	O	-				
3	16	÷	✓	✓	✓	=				
	17			✓	-	-				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"14447069"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/11 12:23
S2	5	("20090004872" | "20100258843" | "20130168743" | "6730552" | "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2015/12/11 12:35
S3	18	(GaN) and enhancement and (isotropically with gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:57
S4	264	(photoresist or resist) same (isotropically with gate with etch$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S5	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S6	5935	(H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S7	3	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S9	4	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:29
S10	4	"13838792"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:30
S11	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:15
S12	1	tw "201314898"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:16

S13	2	(cao or lidow or nakata).in. and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:19
S14	4	"20130075788"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 13:50
S15	3	"20060273347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 13:58
S16	162	20070254418|20060192218|6833161|6537838|6001716|20080116492|5474946|7470941	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:00
S17	43	(20070254418|20060192218|6833161|6537838|6001716|20080116492|5474946|7470941) and (sheppard or kyono or wang or stockman or liao or wu or ajit or micovic).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:01
S18	1096	(gate with ledge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S19	54	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S20	8	"6730552"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:18
S21	4	jp "2011142182"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:22
S22	11	cn "101022128"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S23	26	"7576373"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S24	6	jp "2008159681"	US-	ADJ	ON	2017/01/27

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT			14:28
S25	5	jp "2008091392"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:30
S26	8	"20080079023"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:33
S27	105	(gate with ledge) and barrier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 16:01
S28	181	(gate with ledge).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:15
S29	7	(gate with ledge).ab. and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:17
S30	3913	gate and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:19
S31	2637	barrier and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:19
S32	1068	barrier and 2DEG and (etch$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:19
S33	1032	2DEG and (pattern$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 11:40
S34	479	2DEG and (pattern$4 with gate with (resist or mask or photoresist or photo-resist))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 11:40
S35	22	"11856687"	US-	ADJ	ON	2017/01/30

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT			12:05
S36	6	2DEG and (cap near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:06
S37	13	2DEG and (p-type gate material)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:09
S38	4	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:24
S39	888	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:24
S42	108	"5985687"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:10
S43	2	us-5985687-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:10
S44	2	us-20080006845-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S45	2	us-20080296618-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S46	2	us-20060273347-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S47	2	us-6537838-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S48	2	us-6235547-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:19
S49	2	us-4987462-$.did.	US-PGPUB;	ADJ	ON	2017/01/31 09:19

			USPAT; USOCR; EPO; JPO; DERWENT			
S50	7	"12756960"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 09:16
S51	5	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 09:29
S52	5	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:28
S53	55	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:33
S54	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:38
S55	220	2DEG and (p-type near2 gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/03/20 10:38

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	0	(GaN and gate metal and Photoresist and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2015/12/14 12:01
S40	11	(GaN and barrier and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:21
S41	3	(GaN and barrier and ledges and photoresist).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:23
S56	4	(GaN and barrier and ledges and photoresist).clm.	US-PGPUB; USPAT	ADJ	ON	2017/03/20 10:42

3/20/2017 10:44:43 AM
C:\Users\jniesz1\Documents\EAST\Workspaces\14447069.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	**Art Unit**
	JAMIE C NIESZ	2822

CPC						
Symbol					**Type**	**Version**
H01L		29	/	42316	F	2013-01-01
H01L		21	/	283	I	2013-01-01
H01L		29	/	66462	I	2013-01-01
H01L		29	/	7786	I	2013-01-01
H01L		29	/	1066	I	2013-01-01
H01L		29	/	2003	I	2013-01-01
H01L		21	/	28587	I	2013-01-01
H01L		29	/	205	I	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 3	
/JAMIE C NIESZ/ Primary Examiner.Art Unit 2822 (Primary Examiner)	03/20/2017 (Date)	O.G. Print Claim(s) 12	O.G. Print Figure 6c

U.S. Patent and Trademark Office — Part of Paper No. 20170316

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	**Art Unit**
	JAMIE C NIESZ	2822

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
257	194	H	0	1	L	29 / 66 (2006.01.01)					
CROSS REFERENCE(S)											
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										

NONE (Assistant Examiner) (Date)		**Total Claims Allowed:** 3	
/JAMIE C NIESZ/ Primary Examiner.Art Unit 2822 (Primary Examiner)	03/20/2017 (Date)	O.G. Print Claim(s) 12	O.G. Print Figure 6c

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	**Art Unit**
	JAMIE C NIESZ	2822

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2														
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	11														
1	12														
2	13														
	14														
	15														
3	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 3	
/JAMIE C NIESZ/ Primary Examiner.Art Unit 2822 (Primary Examiner)	03/20/2017 (Date)	O.G. Print Claim(s) 12	O.G. Print Figure 6c

U.S. Patent and Trademark Office Part of Paper No. 20170316

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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US

CONFIRMATION NO. 7150

24998
Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

PUBLICATION NOTICE

OC000000089284296

Title:GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

Publication No.US-2017-0047414-A9
Publication Date:02/16/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Docket No.: E0101.0053
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 | Confirmation No.: 7150

Filed: July 30, 2014 | Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GAN TRANSISTORS | Examiner: J. C. Niesz

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated February 6, 2017, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Electronic Acknowledgement Receipt	
EFS ID:	28375097
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	16-FEB-2017
Filing Date:	30-JUL-2014
Time Stamp:	12:07:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		amendmentp053.pdf	83987 796dbf12935d2c9fe708498fdb678603a252c3d3	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	3	3
	Claims	2	2
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	83987	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Claims 12, 13 and 16 are pending in the present application. Independent claim 12 has been amended. Claims 14 and 15 have been canceled.

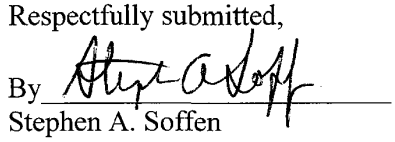
Claims 12-14 and 16 are rejected under 35 U.S.C. 103 as obvious over Hikita et al. (US 2006/0273347) in view of Kanamura et al. (US 2006/0157735). Claim 15, which depends from claim 14, which in turn depends from independent claim 12, is indicated to contain allowable subject matter.

Applicant accepts the allowable subject matter of claim 15, and accordingly has amended independent claim 12 to incorporate the subject matter of claims 14 and 15, and these two claims have now been canceled. The application is therefore submitted to be in condition for allowance.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 23-2185, under Order No. E0101.0053.

Dated: February 16, 2017

Respectfully submitted,

By 

Stephen A. Soffen
Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

AMENDMENTS TO THE CLAIMS

Claims 1-11. (Canceled)

12. (Currently amended) A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

forming a GaN layer;

forming a barrier layer on the GaN layer;

depositing source and drain contacts on the barrier layer;

depositing a p-type gate material on the barrier layer;

depositing a gate metal on the p-type gate material;

forming a photoresist over the gate metal;

etching the gate metal and the p-type gate material, wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and

etching the gate metal to form pair of ledges on the p-type gate material below the gate metal.

13. (Previously presented) The method according to claim 12, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.

Claims 14-15. (Canceled)

16. (Previously presented) The method according to claim 12, wherein the pair of ledges of the p-type gate material are self-aligned.

17. (Canceled)

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/447,069	Filing Date 07/30/2014	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/16/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 3	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
RENEE M. COLLINS

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 02/06/2017

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER
NIESZ, JAMIE C

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
02/06/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

#IPDocketing-DC@BlankRome.com

Office Action Summary	Application No. 14/447,069	Applicant(s) CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *12-16* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *12-14 and 16* is/are rejected.

8)☒ Claim(s) *15* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Request for Continued Examination (RCE) filed December 30, 2016.

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 14, 2016 has been entered.

Priority

4. Prior-filed applications, Applicant Nos. 13/838,792, 12/759,960, and 61/167,777, now provided adequate support for the claims, as amended. Accordingly, claim 12 and its dependents are entitled to the benefit of the above noted prior-filed applications.

Claim Rejections - 35 USC § 112

5. The rejection of claim 17 under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, has been obviated by amendment and is therefore withdrawn.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 12-14 and 16 are rejected under 35 U.S.C. 103 as being unpatentable over Hikita et al. (U.S. Patent Pub No. 2006/0273347) in view of Kanamura et al. (U.S. Patent Pub. No. 2006/0157735).

8. Regarding claim 12, Hikita discloses a method for manufacturing an enhancement-mode GaN transistor (Figs. 8A-8F), the method comprising:

forming a GaN layer (Fig. 8A, 403);

forming a barrier layer (Fig. 8A, 404) on the GaN layer (403);

depositing a p-type gate material (Fig. 8A, 405 and 406) on the barrier layer (404);

depositing a gate metal (Fig. 8F, 411) on the p-type gate material (405 and 406);

etching (Fig. 8B) the p-type gate material (405 and 406); and

forming a pair of ledges (Fig. 8F) on the p-type gate material (405 and 406) below the gate metal (411).

9. Hikita, however, does not specifically disclose forming a photoresist over the gate metal, etching the gate metal, and etching the gate metal to form the pair of ledges.

Attention is brought to the Kanamura reference, which discloses a similar method of forming a gate electrode (Fig. 6A) comprising depositing the gate metal (24) on a material (4); forming a photoresist (not shown) over the gate metal (24, ¶ [0053]); etching the gate metal (24, ¶ [0054]); and etching the gate metal (24) to form a pair of ledges on the material (4) below the gate metal (24, see Fig. 6A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method disclosed by Hikita to include forming a photoresist over the gate metal, etching the gate metal, and etching the gate metal to form the pair of ledges, as taught by Kanamura, since photolithography is a common patterning method which would allow the gate electrode to be easily formed to the desired size and shape.

10. Regarding claim 13, Kanamura discloses wherein the step of etching the gate (24) metal comprises etching the gate metal (24) to reduce a width of the gate metal (24), and Hikita disclose wherein the width of the gate metal (411) is less than a width of the p-type gate material (405 and 406).

11. Regarding claim 14, Hikita further discloses depositing source and drain contacts (409 and 410) on the barrier layer (404).

12. Regarding claim 16, Hikita and Kanamura disclose wherein the pair of ledges of the p-type gate material (Hikita, 405 and 406) are self-aligned (due to the patterning of the gate metal by Kanamura).

Allowable Subject Matter

13. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Regarding claim 15, the prior art of record fails to disclose "forming side surfaces of the p-type gate material that extend horizontally towards the source contact and the drain contact, respectively" in combination with the rest of the limitations in claims 15, 14 and 12.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE C. NIESZ whose telephone number is (303)297-4333. The examiner can normally be reached on Monday through Friday 10-6 EST.

16. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMIE C NIESZ/
Primary Examiner
Art Unit 2822

Notice of References Cited	Application/Control No. 14/447,069	Applicant(s)/Patent Under Reexamination CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2006/0273347 A1	12-2006	Hikita; Masahiro	H01L29/7783	257/192
*	B	US-2006/0157735 A1	07-2006	Kanamura; Masahito	H01L29/42316	257/194
*	C	US-2009/0072272 A1	03-2009	Suh; Chang Soo	H01L29/1066	257/194
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	**Art Unit**
	JAMIE C NIESZ	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2015	12/14/2015	11/15/2016	01/31/2017					
	1	÷	N	-	-					
	2	÷	N	-	-					
	3	÷	N	-	-					
	4	÷	N	-	-					
	5	÷	N	-	-					
	6	÷	N	-	-					
	7	÷	N	-	-					
	8	÷	N	-	-					
	9	÷	N	-	-					
	10	÷	N	-	-					
	11	÷	N	-	-					
	12	÷	✓	✓	✓					
	13	÷	✓	✓	✓					
	14	÷	✓	✓	✓					
	15	÷	✓	✓	O					
	16	÷	✓	✓	✓					
	17			✓	-					

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"14447069"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/11 12:23
S2	5	("20090004872" | "20100258843" | "20130168743" | "6730552" | "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2015/12/11 12:35
S3	18	(GaN) and enhancement and (isotropically with gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:57
S4	264	(photoresist or resist) same (isotropically with gate with etch$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S5	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S6	5935	(H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S7	3	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S9	4	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:29
S10	4	"13838792"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:30
S11	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:15
S12	1	tw "201314898"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:16

S13	2	(cao or lidow or nakata).in. and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:19
S14	4	"20130075788"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 13:50
S15	3	"20060273347"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 13:58
S16	162	20070254418|20060192218|6833161|6537838|6001716|20080116492|5474946|7470941	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:00
S17	43	(20070254418|20060192218|6833161|6537838|6001716|20080116492|5474946|7470941) and (sheppard or kyono or wang or stockman or liao or wu or ajit or micovic).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:01
S18	1096	(gate with ledge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S19	54	(gate with ledge) and (GaN or III-V)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:03
S20	8	"6730552"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:18
S21	4	jp "2011142182"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:22
S22	11	cn "101022128"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S23	26	"7576373"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:26
S24	6	jp "2008159681"	US-	ADJ	ON	2017/01/27

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT			14:28
S25	5	jp "2008091392"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:30
S26	8	"20080079023"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 14:33
S27	105	(gate with ledge) and barrier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/27 16:01
S28	181	(gate with ledge).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:15
S29	7	(gate with ledge).ab. and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:17
S30	3913	gate and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:19
S31	2637	barrier and 2DEG	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:19
S32	1068	barrier and 2DEG and (etch$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 09:19
S33	1032	2DEG and (pattern$4 with gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 11:40
S34	479	2DEG and (pattern$4 with gate with (resist or mask or photoresist or photo-resist))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 11:40
S35	22	"11856687"	US-	ADJ	ON	2017/01/30

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT			12:05
S36	6	2DEG and (cap near3 self-aligned)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:06
S37	13	2DEG and (p-type gate material)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:09
S38	4	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:24
S39	888	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/30 12:24
S42	108	"5985687"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:10
S43	2	us-5985687-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:10
S44	2	us-20080006845-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S45	2	us-20080296618-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:11
S46	2	us-20060273347-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S47	2	us-6537838-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:18
S48	2	us-6235547-$.did.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2017/01/31 09:19
S49	2	us-4987462-$.did.	US-PGPUB;	ADJ	ON	2017/01/31 09:19

			USPAT; USOCR; EPO; JPO; DERWENT					

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	0	(GaN and gate metal and Photoresist and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2015/12/14 12:01
S40	11	(GaN and barrier and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:21
S41	3	(GaN and barrier and ledges and photoresist).clm.	US-PGPUB; USPAT	ADJ	ON	2017/01/30 12:23

1/31/2017 3:14:04 PM
C:\Users\jniesz1\Documents\EAST\Workspaces\14447069.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	Art Unit
	JAMIE C NIESZ	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/42316 and H01L 21/283	Dec. 14, 2015	JCN
H01L 29/42316 and H01L 21/283	Jan. 31, 2017	JCN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	194	Dec. 14, 2015	JCN
257	194	Jan. 31, 2017	JCN

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search EAST (see search history)	Dec. 14, 2015	JCN
Updated Text Search EAST (see search history)	Nov. 15, 2016	JCN
Inventor Search EAST	Nov. 15, 2016	JCN
Updated Text Search EAST (see search history)	Jan. 31, 2017	JCN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Interference Search EAST (see search history)	Dec. 14, 2015	JCN
	Updated Interference Search EAST (see search history)	Jan. 31, 2017	JCN

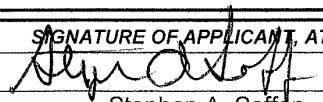
PTO/SB/30 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Request for Continued Examination (RCE) Transmittal		
Address to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450	Application Number	14/447,069-Conf. #7150
	Filing Date	July 30, 2014
	First Named Inventor	Jianjun Cao
	Art Unit	2822
	Examiner Name	J. C. Niesz
	Attorney Docket Number	E0101.0053

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. [X] Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
     - i. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. [X] Other Amendment filed December 14, 2016
   - b. [ ] Enclosed
     - i. [ ] Amendment/Reply
     - ii. [ ] Affidavit(s)/Declaration(s)
     - iii. [ ] Information Disclosure Statement (IDS)
     - iv. [ ] Other _____
2. Miscellaneous
   - a. [ ] Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   - b. [ ] Other _____
3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   - a. [X] The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 23-2185 .
     - i. [X] RCE fee required under 37 CFR 1.17(e)
     - ii. [ ] Extension of time fee (37 CFR 1.136 and 1.17)
     - iii. [ ] Other _____
   - b. [ ] Check in the amount of $ _____ enclosed
   - c. [X] Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED			
Signature		Date	December 30, 2016
Name (Print/Type)	Stephen A. Soffen	Registration No.	31,063

200371.00053/104657386

Electronic Patent Application Fee Transmittal					
Application Number:	14447069				
Filing Date:	30-Jul-2014				
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS				
First Named Inventor/Applicant Name:	Jianjun Cao				
Filer:	Stephen A. Soffen/Cheryl de Lopez				
Attorney Docket Number:	E0101.0032.US				
Filed as Small Entity					
Filing Fees for Utility under 35 USC 111(a)					
Description		**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:					
Pages:					
Claims:					
Miscellaneous-Filing:					
Petition:					
Patent-Appeals-and-Interference:					
Post-Allowance-and-Post-Issuance:					
Extension-of-Time:					

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1st Request	2801	1	600	600
		Total in USD ($)		**600**

Electronic Acknowledgement Receipt	
EFS ID:	27938149
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	30-DEC-2016
Filing Date:	30-JUL-2014
Time Stamp:	12:18:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$600
RAM confirmation Number	010317INTEFSW12190300
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	RCEp032.pdf	115100 e0f485a4c58cae2eac1cfbe6bbdf32eaf2edfaee	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30531 501cc1a9b59dc5fd74db991b475cfe44a7b9168d	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	145631		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/447,069	Filing Date 07/30/2014	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/30/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 5	Minus	** 20	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CHRISTINE MOLLISH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 12/21/2016

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER
NIESZ, JAMIE C

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
12/21/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

#IPDocketing-DC@BlankRome.com

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 14/447,069	**Applicant(s)** CAO ET AL.	
	Examiner JAMIE C. NIESZ	**Art Unit** 2822	**AIA (First Inventor to File) Status** Yes

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 14 December 2016 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: The amendment filed December 14, 2016 changes the scope of the claim and therefore requires further consideration and search. Accordingly, the amendment has not been entered and the Applicant's arguments are moot. .
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed: .
    Claim(s) objected to: .
    Claim(s) rejected: .
    Claim(s) withdrawn from consideration: .

/JAMIE C NIESZ/
Primary Examiner, Art Unit 2822

DO NOT ENTER: /J.C.N/

12/18/2016

Docket No.: E0101.0053
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 | Confirmation No.: 7150

Filed: July 30, 2014 | Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GAN TRANSISTORS | Examiner: J. C. Niesz

AMENDMENT AFTER FINAL ACTION UNDER 37 C.F.R. § 1.116

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated November 22, 2016, finally rejecting claims 12-17, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Docket No.: E0101.0053
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 | Confirmation No.: 7150

Filed: July 30, 2014 | Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GAN TRANSISTORS | Examiner: J. C. Niesz

AMENDMENT AFTER FINAL ACTION UNDER 37 C.F.R. § 1.116

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated November 22, 2016, finally rejecting claims 12-17, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

AMENDMENTS TO THE CLAIMS

Claims 1-11. (Canceled)

12. (Currently amended) A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

forming a GaN layer;

forming a barrier layer on the GaN layer;

depositing a p-type gate material on the barrier layer;

depositing a gate metal on the p-type gate material;

forming a photoresist over the gate metal;

etching the gate metal and the p-type gate material; and

~~isotropically~~ etching the gate metal to form pair of ledges on the p-type gate material below the gate metal.

13. (Currently amended) The method according to claim 12, wherein the step of ~~isotropically~~ etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.

14. (Original) The method according to claim 12, further comprising depositing source and drain contacts on the barrier layer.

15. (Previously presented) The method according to claim 14, wherein the step of etching the p-type material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

16. (Previously presented) The method according to claim 12, wherein the pair of ledges of the p-type gate material are self-aligned.

17. (Canceled)

REMARKS

Claims 12-16 are pending in the present application. Claims 12 and 13 have been amended. Claim 17 has been canceled.

Claim 12 has been amended to delete the term "isotropically," such that claim 12, and dependent claims 13-16, are now fully supported by the disclosure in parent application Lidow et al. (US 2010/0258843). As noted by the Examiner on pages 4-5 of the Office Action, Lidow et al. discloses each and every feature of the claimed invention except for "isotropically" etching the gate metal to form a pair of ledges. Since independent claim 12 now simply recites "etching" the gate metal, which is disclosed in Fig. 10 and paragraphs [0044] and [0045] of Lidow et al., independent claim 12 is now fully supported and enabled by Lidow et al., and is entitled to the claimed priority, thereby eliminating Lidow et al. as prior art. The prior art rejection of claims 12-17 under 35 U.S.C. 103 as obvious over Lidow et al. in view of Park (US 2004/0119110) is therefore no longer proper, and should be withdrawn.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

The Director is hereby authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 23-2185, under Order No. E0101.0053.

Dated: December 14, 2016

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

Electronic Acknowledgement Receipt	
EFS ID:	27796789
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	14-DEC-2016
Filing Date:	30-JUL-2014
Time Stamp:	17:07:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		amendmentp053.pdf	97841 6700e011928075a4243450e3fb02e87764c0ce7f	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	97841	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/447,069	Filing Date 07/30/2014	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	16 minus 20 =	* 0	X $40 =	**0**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	* 0	X $210 =	**0**
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	**0**

APPLICATION AS AMENDED – PART II

AMENDMENT	12/14/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 5	Minus	** 20	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
GERALDINE STANLEY

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 11/22/2016

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER
NIESZ, JAMIE C

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
11/22/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

#IPDocketing-DC@BlankRome.com

Office Action Summary	Application No. 14/447,069	Applicant(s) CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *12-17* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *12-17* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *2/26/2016*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Amendment filed March 18, 2016.

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

3. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, 365(c), or 386(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 119(e), 120, and 121 as follows:

4. The later-filed application must be an application for a patent for an invention which is also disclosed in the prior application (the parent or original nonprovisional application or provisional application). The disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of 35 U.S.C. 112(a) or the first paragraph of pre-AIA 35 U.S.C. 112, except for the best mode requirement. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994)

5. The disclosures of the prior-filed applications, Application Nos. 13/838,792, 12/759,960, and 61/167,777, fail to provide adequate support or enablement in the manner provided by 35 U.S.C. 112(a) or pre-AIA 35 U.S.C. 112, first paragraph for one or more claims of this application. **Accordingly, claim 12 and its dependents are not entitled to the benefit of the above noted prior filed applications.**

Claim Objections

6. The objections to claims 15 and 16 have been obviated by amendment and are therefore withdrawn.

Claim Rejections - 35 USC § 112

7. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

8. The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 17 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

10. Claim 17 recites “after the step of isotropically etching the gate material.” This limitation, however, is unclear because the gate material is not isotopically etched. The limitation in question will therefore instead be read as “after the step of isotropically etching the gate *metal*.”

Claim Rejections - 35 USC § 103

11. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any

correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

12. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

13. **Claims 12-17** are rejected under 35 U.S.C. 103 as being unpatentable over Lidow et al. (U.S. Patent Pub. No. 2010/0258843) in view of Park (U.S. Patent Pub. No. 2004/0119110).

14. Regarding claim 12, Lidow discloses a method for manufacturing an enhancement-mode GaN transistor (Fig. 10), the method comprising:

forming a GaN layer (13),

forming a barrier layer (14) on the GaN layer (13);

depositing a p-type gate material (15) on the barrier layer (14);

depositing a gate metal (17) on the p-type gate material (15);

forming a photoresist (¶ [0026]) over the gate metal (17);

etching the gate metal (17) and the p-type gate material (15, ¶ [0026]); and

etching the gate metal (17) to form pair of ledges on the p-type gate material (15) below the gate metal (17, ¶ [0044]).

15. Lidow, however, does not specifically disclose wherein etching the gate metal to form a pair of ledges comprises isotopically etching. Attention is brought to the Park reference, which discloses a method comprising: depositing a gate material (Fig. 3, 107) on a substrate (101); depositing a gate layer (Fig. 3, 109) on the gate material (107); forming a photoresist (Fig. 3, 112) over the gate layer (109); etching the gate layer (109) and the gate material (107, see Fig. 4); and isotropically etching the gate layer (Fig. 5, 109) to form pair of ledges on the gate material (107) below the gate layer (109, ¶ [0040]). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method disclosed by Lidow to include wherein etching the gate metal to form a pair of ledges comprises isotopically etching, as taught by Park, in order to selectively etch the sidewalls of the gate metal with respect to the p-type gate material.

16. Regarding claim 13, Lidow discloses wherein the step of [isotropically] etching the gate metal (17) comprises etching the gate metal (17) to reduce a width of the gate metal (17), such that the width of the gate metal (17) is less than a width of the p-type gate material (15, see Fig. 10 and ¶ [0044]).

17. Regarding claim 14, Lidow further discloses depositing source (20) and drain (19) contacts on the barrier layer (14).

18. Regarding claim 15, Lidow discloses wherein the step of etching the p-type material (15) comprises forming side surface of the p-type gate material (15) that extend horizontally towards the source contact (20) and the drain contact (19), respectively, and contact the barrier layer (14; see Fig. 10).

19. Regarding claim 16, Lidow discloses wherein the pair of ledges of the p-type gate material (15) are self-aligned.

20. Regarding claim 17, Park further discloses removing the photoresist (112) after the step of isotropically etching the gate [metal] (109, see Fig. 6 and ¶ [0041]).

Response to Arguments

21. Applicant's arguments filed March 18, 2016 have been fully considered but they are not persuasive.

22. The Applicant submits that “upon granting of the petition [for Unintentionally Delayed Domestic Benefit Claim], Lidow is not prior art” (see Page 5 filed March 18, 2016). However, this is incorrect. As noted above, prior-filed applications 13/838,792, 12/759,960, and 61/167,777, fail to provide adequate support or enablement in the manner provided by 35 U.S.C. 112(a) or pre-AIA 35 U.S.C. 112, first paragraph for claim 12 of the instant application. Specifically, the step of "isotropically etching the gate metal” does not have support. Accordingly, claim 12 and its dependents are not entitled to the benefit of the above noted prior filed applications. Instead, the effective filing date of claim 12 is the date of provisional application 61/860,976, i.e., August 1, 2013. Therefore, Lidow, U.S. Patent Pub. No. 2010/0258843, remains a proper 102(b) reference.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE C. NIESZ whose telephone number is (303)297-4333. The examiner can normally be reached on Monday through Friday 10-6 EST.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMIE C NIESZ/
Primary Examiner, Art Unit 2822

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	Art Unit
	JAMIE C NIESZ	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/42316 and H01L 21/283	Dec. 14, 2015	JCN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	194	Dec. 14, 2015	JCN

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search EAST (see search history)	Dec. 14, 2015	JCN
Updated Text Search EAST (see search history)	Nov. 15, 2016	JCN
Inventor Search EAST	Nov. 15, 2016	JCN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Interference Search EAST (see search history)	Dec. 14, 2015	JCN

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"14447069"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/11 12:23
S2	5	("20090004872" | "20100258843" | "20130168743" | "6730552" | "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2015/12/11 12:35
S3	18	(GaN) and enhancement and (isotropically with gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:57
S4	264	(photoresist or resist) same (isotropically with gate with etch$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S5	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S6	5935	(H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S7	3	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S9	4	"14447069"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:29
S10	4	"13838792"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 12:30
S11	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:15
S12	1	tw "201314898"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:16
S13	2	(cao or lidow or nakata).in. and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2016/11/15 14:19

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	0	(GaN and gate metal and Photoresist and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2015/12/14 12:01

11/15/2016 2:19:52 PM
C:\Users\jniesz1\Documents\EAST\Workspaces\14447069.wsp

Used in Lieu of PTO/SB/08A/B
(Based on PTO 10-07 version)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	14/447,069
				Filing Date	July 30, 2014
				First Named Inventor	Jianjun Cao
				Art Unit	2822
(Use as many sheets as necessary)				Examiner Name	Niesz, Jamie C
Sheet	1	of	1	Attorney Docket Number	E0101.0032

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	BA	TW 201232779	08-01-2012			√
	BB	TW 201314898	04-01-2013			√

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

√ **English language abstract also enclosed.**

Examiner Signature	/JAMIE C NIESZ/	Date Considered	11/15/2016

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.C.N/

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	Art Unit
	JAMIE C NIESZ	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2015	12/14/2015	11/15/2016						
	1	÷	N	-						
	2	÷	N	-						
	3	÷	N	-						
	4	÷	N	-						
	5	÷	N	-						
	6	÷	N	-						
	7	÷	N	-						
	8	÷	N	-						
	9	÷	N	-						
	10	÷	N	-						
	11	÷	N	-						
	12	÷	✓	✓						
	13	÷	✓	✓						
	14	÷	✓	✓						
	15	÷	✓	✓						
	16	÷	✓	✓						
	17			✓						

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US

CONFIRMATION NO. 7150

24998
Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

PUB REQUEST ACCEPTANCE LETTER

OC000000087081909

Date Mailed: 11/09/2016

NOTICE OF ACCEPTANCE OF PUBLICATION REQUEST

The request for voluntary publication, amended publication, early publication, redacted publication, republication, corrected publication or revised publication has been received for this application. The request, including payment of any necessary fee(s), is in compliance with 37 CFR 1.215, 1.217, 1.219 or 1.221.

The projected publication date is 02/16/2017.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dterry/

Office of Petitions: Routing Sheet



Application No. 14/447,069

This application is being forwarded to your office for further processing. A decision has been rendered on a petition filed in this application, as indicated below. For details of this decision, please see the document PET.OP.DEC filed on the same date as this document.

- [x] **GRANTED**
- [ ] **DISMISSED**
- [ ] **DENIED**

Office of Petitions: Decision Count Sheet

Mailing Month

Application No. 14447069

14447069

For US serial numbers: enter number only, no slashes or commas. Ex: 10123456

For PCT: enter "51+single digit of year of filing+last 5 numbers", Ex. for PCT/US05/12345, enter 51512345

Deciding Official: KAREN CREASY

Count (1) - Palm Credit 14/447,069

Decision: GRANT

FINANCE WORK NEEDED

☐ Select Check Box for YES

GRANT

Decision Type: 535 - 37 CFR 1.78(a)(3) & (a)(6) UNINTENTIONAL DELAY

535

Notes:

Count (2)

Decision: n/a

FINANCE WORK NEEDED

☐ Select Check Box for YES

Decision Type: NONE

Notes:

Count (3)

Decision: n/a

FINANCE WORK NEEDED

☐ Select Check Box for YES

Decision Type: NONE

Notes:

Initials of Approving Official (if required)

If more than 3 decisions, attach 2nd count sheet & mark this box ☐

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Office of Petitions Internal Document - Ver. 5.0

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 11/04/2016

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER
NIESZ, JAMIE C

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
11/04/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

#IPDocketing-DC@BlankRome.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of	:	
Jianjun Cao et al	:	
Application No. 14/447,069	:	DECISION DISMISSING PETITIONS
Filed: July 30, 2014	:	UNDER 37 CFR 1.78(c) AND (e)
Attorney Docket No. E0101.0032.US	:	

This is a decision on the renewed petition filed October 18, 2016, which is being considered under 37 CFR §§ 1.78(c) and 1.78(e), to accept an unintentionally delayed claim under 35 U.S.C. §§ 119(e) and 120 for the benefit of priority to the prior-filed provisional and nonprovisional applications set forth in the concurrently filed Application Data Sheet (ADS).

The petitions are **GRANTED.**

A petition for acceptance of a claim for late priority under 37 CFR §§ 1.78(c) and 1.78(e) is only applicable to those applications filed after the expiration of the period specified in 37 CFR §§ 1.78(a)(4) and 1.78(d)(3). In addition, the petition under 37 CFR §§ 1.78(c) and 1.78(e) must be accompanied by:

(1) the reference required by 35 U.S.C. §§ 120 and 119(e) and 37 CFR §§ 1.78(d)(2) and 1.78(a)(3) of the prior-filed application, which must be filed in an Application Data Sheet, unless previously submitted;
(2) the petition fee set forth in § 1.17(m); and
(3) a statement that the entire delay between the date the claim was due under 37 CFR §§ 1.78(d)(3) and 1.78(a)(4) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional.

Additionally, the instant nonprovisional application must be pending at the time of filing of the reference to the prior-filed provisional application, as required by 37 CFR 1.78(c).

Further, the nonprovisional application claiming the benefit of the prior-filed provisional application must have been filed within twelve months of the filing date of the prior-filed provisional application.

All the above requirements having been satisfied, the late claim for benefit of priority under 35 U.S.C. §§ 120 and 119(e) is accepted as being unintentionally delayed.

Petitioner is advised that this decision grants the petition to accept the unintentionally delayed domestic benefit claim to the prior filed application(s) because the petition requirements of 37 CFR §§ 1.78(c) and 1.78(e) and the formal requirements for claiming domestic benefit (see MPEP 211.01 et. seq.) have been met. This acceptance should not be construed as meaning that this application is entitled to the benefit of the prior-filed application(s). Whether a claimed invention in a nonprovisional application is entitled to the benefit of the filing date of a prior-filed application on the basis of the disclosure thereof is determined during examination if it becomes necessary to do so (e.g., intervening reference and interference proceeding). See MPEP 211.05.

A corrected Filing Receipt, which includes the priority claim to the prior-filed applications, accompanies this decision on petition.

Any questions concerning this matter may be directed to the undersigned at (571) 272-3208. All other inquiries concerning either the examination procedures or status of the application should be directed to the Technology Center.

This application is being forwarded to Technology Center Art Unit 2822 for consideration by the examiner of the claim under 35 U.S.C. §§ 119(e) and 120 of the prior-filed provisional and nonprovisional applications.

/KOC/
Karen Creasy
Paralegal Specialist
Office of Petitions

ATTACHMENT : Corrected Filing Receipt

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/447,069	07/30/2014	2822	730	E0101.0032.US	16	3

CONFIRMATION NO. 7150

CORRECTED FILING RECEIPT

24998
Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

Date Mailed: 11/01/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jianjun Cao, Torrance, CA;
Alexander Lidow, Marina Del Rey, CA;
Alana Nakata, Redondo Beach, CA;

Applicant(s)

Efficient Power Conversion Corporation, ElSegundo, CA;

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This application is a CIP of 13/838,792 03/15/2013 PAT 8890168
which is a DIV of 12/756,960 04/08/2010 PAT 8404508
which claims benefit of 61/167,777 04/08/2009
This application 14/447,069
claims benefit of 61/860,976 08/01/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/07/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/447,069**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No
** **SMALL ENTITY** **
Title

GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Docket No.: E0101.0032

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: J. C. Niesz

REQUEST FOR RECONSIDERATION OF DECISION DISMISSING PETITION FOR UNINTENTIONALLY DELAYED DOMESTIC BENEFIT CLAIM

Mail Stop Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant hereby respectfully requests reconsideration of the Decision on Petition mailed October 13, 2016, dismissing the Petition for Unintentionally Delayed Domestic Benefit Claim.

In the Petition, pursuant to 37 CFR § 1.78, Applicant respectfully requests correction of the application to include a claim for domestic priority. The claim for priority is as follows:

> This is a continuation in part of U.S. Patent Application Ser. No. 13/838,792, filed Mar. 15, 2013, now U.S. Pat. No. 8,890,168, which is a division of U.S. Patent Application Ser. No. 12/756,960, filed Apr. 8, 2010, now U.S. Pat. No. 8,404,508, which claims priority to U.S. Provisional Patent Application Ser. No. 61/167,777, filed Apr. 8, 2009. This application also claims priority to U.S. Provisional Patent Application Ser. No. 61/860,976, filed Aug. 1, 2013.

A Corrected ADS with the updated information and with the benefit claim to the provisional application underlined is submitted herewith. Applicant submits that the entire delay between the date the claim was due under 37 C.F.R. 1.78(a)(2)(ii) and the date in which this petition is filed was unintentional and that the petition was filed immediately upon discovery.

Dated: October 18, 2016

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

Corrected Application Data Sheet

Inventor Information

Inventor Number::	1
Given Name::	Jianjun
Family Name::	Cao
City of Residence::	Torrance
State or Province of Residence::	CA
Country of Residence::	US
Street of mailing address::	5323 Bindewald Rd.
City of mailing address::	Torrance
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90505-8712

Inventor Number::	2
Given Name::	Alexander
Family Name::	Lidow
City of Residence::	Marina Del Rey
State or Province of Residence::	CA
Country of Residence::	US
Street of mailing address::	~~129 Channel Pointe Mall~~ 138 Maybery Rd.
City of mailing address::	~~Marina Del Rey~~ Santa Monica

State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	~~90292~~ 90402

Inventor Number::	3
Given Name::	Alana
Family Name::	Nakata
City of Residence::	Redondo Beach
State or Province of Residence::	CA
Country of Residence::	US
Street of mailing address::	611 N. Irena Avenue, Unit M
City of mailing address::	Redondo Beach
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90277-2968

Correspondence Information

Correspondence Customer Number::	24998

Application Information

Application No.::	14/447,069
Filing Date::	07/30/2014
Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R?::	None

Sequence submission?::	None
Computer Readable Form (CRF)?::	No
Title::	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS
Attorney Docket Number::	E0101.0032.US
Request for Early Publication?::	No
Request for Non-Publication?::	No
Total Drawing Sheets:	6
Small Entity?::	Yes
Petition included?::	~~No~~Yes
Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2::	No
Authorization to Permit Access to the Instant Application by the Participating Offices::	No
This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013::	No

Representative Information

Representative Customer Number::	24998

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This application	Continuation-in-part of	13/838,792	03/15/2013
13/838,792	Division of	12/756,960	04/08/2010
12/756,960	An application claiming the benefit under 35 USC 119(e)	61/167,777	04/08/2009
This application	An application claiming the benefit under 35 USC 119(e)	61/860,976	08/01/2013

Applicant Information

Applicant Type::	Assignee
Organization Name::	Efficient Power Conversion Corporation
Street of mailing address::	909 N. Sepulveda Boulevard Suite 230
City of mailing address::	El Segundo
State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90245

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.			
Signature	/Stephen A. Soffen/	Date	October 18, 2016
Name (Print/Type)	Stephen A. Soffen	Registration No. (Attorney/Agent)	31,063

Electronic Acknowledgement Receipt	
EFS ID:	27251027
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Cheryl de Lopez
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	18-OCT-2016
Filing Date:	30-JUL-2014
Time Stamp:	16:23:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		requestreconsiderationpetp0032.pdf	136689 eeeeea3d89324f6ba38cfc785e5965b9c8403544	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Petition for review by the Office of Petitions	1	2
	Application Data Sheet	3	6
Warnings:			
Information:			
	Total Files Size (in bytes):	136689	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 10/13/2016

Blank Rome LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER
FEENEY, BRETT A

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
10/13/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

#IPDocketing-DC@BlankRome.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of	:	
Jianjun Cao et al	:	
Application No. 14/447,069	:	DECISION DISMISSING PETITIONS
Filed: July 30, 2014	:	UNDER 37 CFR 1.78(c) AND (e)
Attorney Docket No. E0101.0032.US	:	

This is a decision on the petition filed March 18, 2016, which is being considered under 37 CFR §§ 1.78(c) and 1.78(e), to accept an unintentionally delayed claim under 35 U.S.C. §§ 119(e) and 120 for the benefit of priority to the prior-filed provisional and nonprovisional applications set forth in the concurrently filed Application Data Sheet (ADS).

The petitions are **DISMISSED.**

A petition for acceptance of a claim for late priority under 37 CFR §§ 1.78(c) and 1.78(e) is only applicable to those applications filed on or after December 18, 2013 and after the expiration of the period specified in 37 CFR §§ 1.78(a)(4) and 1.78(d)(3). In addition, the petition under 37 CFR §§ 1.78(c) and 1.78(e) must be accompanied by:

(1) the reference required by 35 U.S.C. §§ 120 and 119(e) and 37 CFR §§ 1.78(d)(2) and 1.78(a)(3) of the prior-filed application, which must be filed in an Application Data Sheet, unless previously submitted;
(2) the petition fee set forth in § 1.17(m); and
(3) a statement that the entire delay between the date the claim was due under 37 CFR §§ 1.78(d)(3) and 1.78(a)(4) and the date the claim was filed was unintentional. The Director may require additional where there is a question whether the delay was unintentional.

The petition does not comply with item (1).

The above identified application was filed on July 30, 2014. Therefore, applicant's attention is directed to the below provided by MPEP 601.05(a):

II.CORRECTING AND UPDATING AN ADS OR INFORMATION OTHERWISE OF RECORD

"37 CFR 1.76(c) provides the procedure for correcting and updating not only an application data sheet (ADS), but also information otherwise of record (e.g., information provided on the most recent filing receipt). Any ADS filed after the filing date of the application is considered a corrected (or updated) ADS even if an ADS was not previously submitted. Such a corrected ADS must identify the information that is being changed with underlining for insertions and strike-through or brackets for text removed, except that

identification of information being changed is not required for an ADS included with an initial submission under 35 U.S.C. 371. In general, the identification of the information being changed should be made relative to the most recent filing receipt. A corrected ADS may be submitted until payment of the issue fee to either correct or update information in a previously submitted application data sheet, or in an inventor's oath or declaration under 37 CFR 1.63, 1.64 , or 1.67, or otherwise of record. See 37 CFR 1.76(c)(1). However, inventorship changes must comply with the requirements of 37 CFR 1.48, foreign priority and domestic benefit information changes must comply with 37 CFR 1.55 and 1.78, and correspondence address changes must comply with 37 CFR 1.33(a). Note also that any request to correct or update the name of the applicant, or change the applicant, must comply with 37 CFR 1.46(c)."

The benefit claim to the provisional application (61/860,976 filed August 1, 2013) was never made of record, and needs to be underlined.

The ADS submitted with the petition on March 18, 2016, fails to identify the above information. Therefore, the ADS is improper, and the reference set forth in the ADS cannot be accepted.

Any request for reconsideration of this decision must be accompanied by a proper ADS, which includes the required reference.

Further correspondence with respect to this matter should be delivered through one of the following mediums:

By mail:	Mail Stop PETITIONS Commissioner for Patents Post Office Box 1450 Alexandria, VA 22313-1450
By hand:	Customer Service Window Mail Stop Petitions Randolph Building 40l Dulany Street Alexandria, VA 22314
By fax:	(571) 273-8300 ATTN: Office of Petitions
By internet:	EFS-Web[1]

[1] www.uspto.gov/ebc/efs_help.html (for help using EFS-Web call the Patent Electronic Business Center at (866) 217-9197)

Any questions concerning this matter may be directed to the undersigned at (571) 272-3208.

/KOC/
Karen Creasy
Paralegal Specialist
Office of Petitions

Office of Petitions: Decision Count Sheet

Mailing Month

Application No. 14447069

14447069

For US serial numbers: enter number only, no slashes or commas. Ex: 10123456

For PCT: enter "51+single digit of year of filing+last 5 numbers", Ex. for PCT/US05/12345, enter 51512345

Deciding Official: KAREN CREASY

Count (1) - Palm Credit 14/447,069

Decision: DISMISSED

FINANCE WORK NEEDED

☐ Select Check Box for YES

DISMISSED

Decision Type: 535 - 37 CFR 1.78(a)(3) & (a)(6) UNINTENTIONAL DELAY

535

Notes:

Count (2)

Decision: n/a

FINANCE WORK NEEDED

☐ Select Check Box for YES

Decision Type: NONE

Notes:

Count (3)

Decision: n/a

FINANCE WORK NEEDED

☐ Select Check Box for YES

Decision Type: NONE

Notes:

Initials of Approving Official (if required)

If more than 3 decisions, attach 2nd count sheet & mark this box ☐

Printed on: *10/11/2016*

Office of Petitions Internal Document - Ver. 5.0

Office of Petitions: Routing Sheet



Application No. 14/447,069

This application is being forwarded to your office for further processing. A decision has been rendered on a petition filed in this application, as indicated below. For details of this decision, please see the document PET.OP.DEC filed on the same date as this document.

☐ **GRANTED**

☒ **DISMISSED**

☐ **DENIED**

Docket No.: E0101.0032/P032
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: J. C. Niesz

PETITION FOR UNINTENTIONALLY DELAYED DOMESTIC BENEFIT CLAIM

Mail Stop Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR § 1.78, Applicant for the above-referenced application respectfully requests correction of its domestic claim of priority. The priority is as follows:

> This application is a continuation in part of U.S. Patent Application Ser. No. 13/838,792, filed Mar. 15, 2013, now U.S. Pat. No. 8,890,168, which is a division of U.S. Patent Application Ser. No. 12/756,960, filed Apr. 8, 2010, now U.S. Pat. No. 8,404,508, which claims priority to U.S. Provisional Patent Application Ser. No. 61/167,777, filed Apr. 8, 2009. This application also claims priority to U.S. Provisional Patent Application Ser. No. 61/860,976, filed Aug. 1, 2013.

A supplemental ADS with the updated information is submitted herewith, along with the small entity fee as specified by 37 C.F.R. 1.17(m). Applicant submits that the entire delay between the date the claim was due under 37 C.F.R. 1.78(a)(2)(ii) and the date in which this petition is filed was unintentional and that the petition was filed immediately upon discovery.

The fee of $850.00 under 37 C.F.R. 1.17 (m) in payment of this petition for delayed submission of a priority or benefit claim is submitted herewith by credit card payment.

Dated: March 18, 2016

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

Corrected Application Data Sheet

Inventor Information

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Correspondence Information

Correspondence Customer Number::	24998

Application Information

Application No.::	14/447,069
Filing Date::	07/30/2014
Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R?::	None

Sequence submission?::	None
Computer Readable Form (CRF)?::	No
Title::	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS
Attorney Docket Number::	E0101.0032.US
Request for Early Publication?::	No
Request for Non-Publication?::	No
Total Drawing Sheets:	6
Small Entity?::	Yes
Petition included?::	~~No~~Yes
Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2::	No
Authorization to Permit Access to the Instant Application by the Participating Offices::	No
This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013::	No

Representative Information

Representative Customer Number::	24998

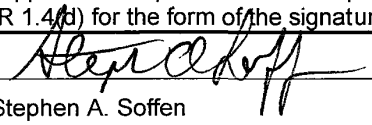
Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This application	Continuation-in-part of	13/838,792	03/15/2013
13/838,792	Division of	12/756,960	04/08/2010
12/756,960	An application claiming the benefit under 35 USC 119(e)	61/167,777	04/08/2009
This application	An application claiming the benefit under 35 USC 119(e)	61/860,976	08/01/2013

Applicant Information

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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.			
Signature		Date	March 18, 2016
Name (Print/Type)	Stephen A. Soffen	Registration No. (Attorney/Agent)	31,063

Electronic Patent Application Fee Transmittal					
Application Number:	14447069				
Filing Date:	30-Jul-2014				
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS				
First Named Inventor/Applicant Name:	Jianjun Cao				
Filer:	Stephen A. Soffen/Kanessa Howard				
Attorney Docket Number:	E0101.0032.US				
Filed as Small Entity					
Filing Fees for Utility under 35 USC 111(a)					
Description		**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:					
Pages:					
Claims:					
Miscellaneous-Filing:					
Petition:					
Pet. Delay Sub or Restore Priority-Claim		2454	1	850	850
Patent-Appeals-and-Interference:					
Post-Allowance-and-Post-Issuance:					

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**850**

Electronic Acknowledgement Receipt	
EFS ID:	25243757
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Kanessa Howard
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	18-MAR-2016
Filing Date:	30-JUL-2014
Time Stamp:	16:12:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$850
RAM confirmation Number	3036
Deposit Account	232185
Authorized User	GREENBAUM, MICHAEL C.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		E0101_0032_Amendment_Petition_Priority_Claim_ADS.pdf	284024 1170cd34e911178f7b954c2ed165483c4f8eae00	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Specification	2	2
Claims	3	4
Applicant Arguments/Remarks Made in an Amendment	5	6
Petition for review by the Office of Petitions	7	8
Application Data Sheet	9	12

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30847 b021258aa2741e8cbbc2862594e762ab8715c177	no	2

Warnings:

Information:

Total Files Size (in bytes):	314871

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: E0101.0032/P032
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: J. C. Niesz

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated December 18, 2015, please amend the above-identified U.S. patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 5 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0001] of the specification as follows:

This application is a continuation-in-part of U.S. Patent Application Ser. No. 13/838,792, filed Mar. 15, 2013, now U.S. Pat. No. 8,890,168, which is a division of U.S. Patent Application Ser. No. 12/756,960, filed Apr. 8, 2010, now U.S. Pat. No. 8,404,508, which claims the benefit of U.S. Provisional Application No. 61/167,777, filed Apr. 8, 2009. This application also claims the benefit of U.S. Provisional Application No. 61/860,976, filed on August 1, 2013, the entire disclosure of which is hereby incorporated by reference

AMENDMENTS TO THE CLAIMS

Claims 1-11. (Canceled)

12. (Original) A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

forming a GaN layer;

forming a barrier layer on the GaN layer;

depositing a p-type gate material on the barrier layer;

depositing a gate metal on the p-type gate material;

forming a photoresist over the gate metal;

etching the gate metal and the p-type gate material; and

isotropically etching the gate metal to form pair of ledges on the p-type gate material below the gate metal.

13. (Original) The method according to claim 12, wherein the step of isotropically etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.

14. (Original) The method according to claim 12, further comprising depositing source and drain contacts on the barrier layer.

15. (Currently amended) The method according to claim ~~12~~14, wherein the step of etching the p-type material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

16. (Currently amended) The method according to claim 12, wherein the pair of ~~horizontal~~ ledges of the p-type gate material are self-aligned.

17. (New) The method according to claim 12, further comprising removing the photoresist after the step of isotropically etching the gate material.

REMARKS

Claim Status

Claims 12-16 are pending in the application. Non-elected claims 1-11 have been canceled. Claims 15 and 16 are presently amended, and claim 17 is newly added. Claim 17 is supported at least by paragraph [0028] of the specification. No new matter is introduced. Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

Claim Rejections under 35 U.S.C. § 103

Claims 12-16 stand rejected under 35 U.S.C. § 103 as being obvious over U.S. Patent Application Publication No. 2010/0258843 to Lidow et al. ("Lidow") in view of U.S. Patent Application Publication No. 2004/0119110 to Park ("Park"). This rejection is respectfully traversed.

In conjunction with this response, Applicant concurrently submits a Petition for Unintentionally Delayed Domestic Benefit Claim. As corrected, the present application claims priority to the cited Lidow reference. Accordingly, Applicant respectfully submits that, upon granting of the petition, Lidow is not prior art.

Remaining reference Park fails to disclose or suggest all of the limitations of independent claim 12, and is not relied on as doing so. Park fails to disclose or suggest at least "forming a GaN layer," "forming a barrier layer on the GaN layer," and "depositing a p-type gate material on the barrier layer," as recited by independent claim 12. Accordingly, Applicant respectfully requests that the rejection be withdrawn and the claim be allowed.

Claims 13-17 depend from claim 12 and are allowable along with claim 12, as well as on their own merit. Park fails to disclose or suggest "wherein the step of isotropically etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material," as recited by dependent claim 13, "depositing source and drain contacts on the barrier layer," as recited by dependent claim 14,

"wherein the step of etching the p-type material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer," as recited by dependent claim 15, and "wherein the pair of horizontal ledges of the p-type gate material are self-aligned," as recited by dependent claim 16. Accordingly, Applicant respectfully requests that the rejections be withdrawn and the claims be allowed.

Conclusion

In view of the above amendments and remarks, Applicant believes the pending application is in condition for allowance.

Dated: March 18, 2016

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/447,069	Filing Date 07/30/2014	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/18/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 6	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LINDA A. WISE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Used in Lieu of PTO/SB/08A/B
(Based on PTO 10-07 version)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	14/447,069
				Filing Date	July 30, 2014
				First Named Inventor	Jianjun Cao
				Art Unit	2822
(Use as many sheets as necessary)				Examiner Name	Niesz, Jamie C
Sheet	1	of	1	Attorney Docket Number	E0101.0032

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	BA	TW 201232779	08-01-2012			√
	BB	TW 201314898	04-01-2013			√

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

√ English language abstract also enclosed.

Examiner Signature		Date Considered	

Espacenet

Bibliographic data: TW201314898 (A) — 2013-04-01

Semiconductor device and fabrication method

Inventor(s): TOMABECHI SHUICHI [JP] ± (TOMABECHI, SHUICHI)

Applicant(s): FUJITSU LTD [JP] ± (FUJITSU LIMITED, ; TRANSPHORM JAPAN, INC)

Classification: - international:***H01L21/336; H01L29/778***
- cooperative: **H01L29/1029**; **H01L29/66462**; **H01L29/7787**; H01L29/2003

Application number: TW20120128759 20120809

Priority number (s): JP20110213471 20110928

Also published as: TWI463656 (B) US2013075788 (A1) US8962409 (B2) KR20130034587 (A) KR101394206 (B1) more

Abstract of TW201314898 (A)

A method for fabricating a semiconductor device is disclosed. The method includes sequentially forming a first semiconductor layer, a second semiconductor layer and a semiconductor cap layer containing a p-type impurity element on a substrate, forming a dielectric layer having an opening after the forming of the semiconductor cap layer, forming a third semiconductor layer containing a p-type impurity element on the semiconductor cap layer exposed from the opening of the dielectric layer, and forming a gate electrode on the third semiconductor layer.

(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201314898 A1
(43)公開日： 中華民國 102 (2013) 年 04 月 01 日

(21)申請案號：101128759 (22)申請日： 中華民國 101 (2012) 年 08 月 09 日
(51)Int. Cl.： *H01L29/778 (2006.01)* *H01L21/336 (2006.01)*
(30)優先權：2011/09/28 日本 2011-213471
(71)申請人：富士通股份有限公司 (日本) FUJITSU LIMITED (JP)
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(72)發明人：苫米地秀一 TOMABECHI, SHUICHI (JP)
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申請實體審查：有 申請專利範圍項數：18 項 圖式數：12 共 46 頁

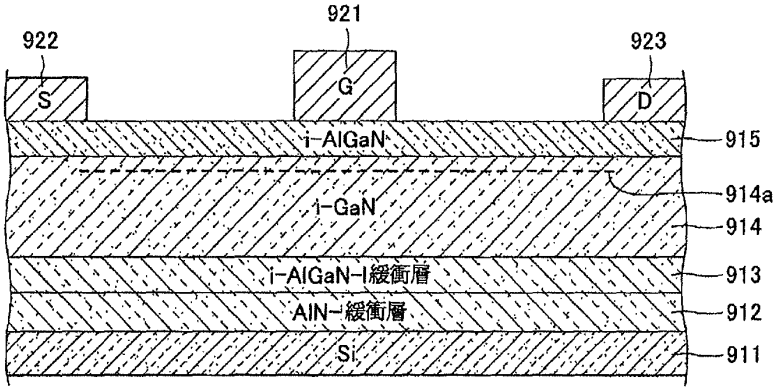
(54)名稱

半導體裝置及製造方法

SEMICONDUCTOR DEVICE AND FABRICATION METHOD

(57)摘要

一種用於製造半導體裝置的方法被揭露。該方法包括相繼地在一基體上形成一第一半導體層、一第二半導體層與一包含一 p-型雜質元素的半導體頂蓋層；在該半導體頂蓋層的形成之後形成一具有一開孔的介電層；在從該介電層之開孔露出的半導體頂蓋層上形成一包含一 p-型雜質元素的第三半導體層；及在該第三半導體層上形成一閘極電極。



911：基體
912：緩衝層
913：緩衝層
914：電子轉移層
914a：2DEG
915：電子捐獻層
921：閘極電極
922：源極電極
923：汲極電極

六、發明說明：

【發明所屬之技術領域】

發明領域

於此中所討論的實施例是有關於一種半導體裝置及其製造方法。

【先前技術】

發明背景

諸如氮化鎵(GaN)、氮化鋁(AlN)、與氮化銦(InN)般的氮化物半導體，或者一種由一由GaN、AlN、與InN形成之混合晶體形成的材料通常具有一寬能隙(wide band gap)。這些材料是被使用作為一高功率電子裝置、一短波長發光裝置或其類似。在這些當中，關於場效電晶體(FET)，特別地，關於高電子遷移率電晶體(HEMT)的技術業已被發展作為高功率裝置(例如，專利文件1)。包括氮化物半導體的一高電子遷移率電晶體(HEMT)可以被使用作為一高功率與高效率放大器、一高功率切換裝置、及其類似。

具有氮化物半導體的該HEMT通常包括一形成於一基體上的氮化鋁鎵/氮化鎵(AlGaN/GaN)異質結構(heterostructure)，在其中，一GaN層作用如一電子轉移層。注意的是，該基體可以是由藍寶石、碳化矽(SiC)、氮化鎵(GaN)、矽(Si)、及其類似形成。

該GaN，其是為一種氮化物半導體，包括一高飽和電子速率或一寬能隙。因此，該GaN能夠獲得優越的抗壓性並展現優異的電氣特性。此外，該GaN被定向在一與一c-

軸平行的[0001]方向上。據此，當該AlGaN/GaN異質結構被形成時，壓電極化(piezoelectric polarization)會由因在該AlGaN與GaN之間之晶格常數上之差異而起的晶格應力(lattice strain)而被誘發。結果，一高濃度二維電子氣(highly-concentrated two-dimensional electron gas (2DEG))會被產生在該GaN層的介面附近。

更明確地，一習知HEMT的範例是配合第1圖來作說明。具有第1圖之結構的HEMT包括形成在一基體911上的一(AlN)緩衝層912、一i-AlGaN緩衝層913、一電子轉移層914及一電子捐獻層915。該HEMT更包括在該電子捐獻層915上的一閘極電極921、一源極電極922與一汲極電極923。藉由如此之結構，2DEG 914a會產生於該電子轉移層914內在該在形成電子轉移層914之i-GaN與形成電子捐獻層915之i-AlGaN之間的介面附近。

從安全的觀點，最好的是諸如高功率與高效率放大器或高功率切換裝置般的功率裝置具有當偏壓是在一零電壓時能夠關掉電流流動的常關特性。然而，在第1圖中所示的習知例子中，產生在該介面的2DEG包括高濃度電子。因此，為了該電流流動的關閉，一負偏壓必須被施加到該閘極電極921。據此，使用GaN的裝置可以實現一超過一使用Si之裝置之極限的低開啟-電阻(on-resistance)。然而，會是難以讓使用GaN的裝置應用到一反相器作為一功率裝置。

因此，為了讓該具有AlGaN/GaN異質結構的HEMT處於一常關狀態，是必須藉由減少正好在該閘極電極921下面之

2DEG 914a的電子來把一臨界電壓轉移到正側。該臨界電壓可以藉由依據該使該AlGaN薄膜變薄或者降低Al成份來得到之極化效應來控制2DEG的產生來被轉移到正側。然而，藉著以上的方法，開啟-電阻會由於2DEG電子的減少而增加。

此外，作為一種用於使該具有AlGaN/GaN異質結構之HEMT處於一常關狀態的方法，具有該具有一p-GaN層正好層疊在該閘極電極下面之AlGaN/GaN異質結構的HEMT是被揭露(例如，專利文件2)。在這結構中，於電子轉移層中之2DEG電子的濃度會由於從正好在該閘極電極下面之p-GaN層注入的電洞而降低。據此，該臨界電壓會轉移到正側來在沒有增加該開啟-電阻之下使該具有該AlGaN/GaN異質結構的HEMT處於一常關狀態。

相關技術文件

專利文件1：日本早期公開專利公告第2002-359256號

專利文件2：日本早期公開專利公告第2008-98434號

為了讓具有該具有p-GaN層之AlGaN/GaN異質結構的HEMT在沒有增加開啟-電阻之下處於一常關狀態，會是重要的是在該p-GaN層之正好在閘極電極下面之區域內產生大量的電洞。通常，該p-GaN層是由一藉著金屬有機氣相外延(metal organic vapor phase epitaxy (MOVPE))來長成的鎂-摻雜(Mg-doped)GaN層來形成。然而，在該GaN層之內的Mg是與氫鍵結，而因此，緊在該生成之後在該GaN層之內的Mg未電氣地激活來產生電洞。據此，熱處理通常是在一

氮大氣之下對該Mg-摻雜GaN層進行俾可從該GaN層除去氫，其會激活在該GaN層之內的Mg來變成p-型。然而，即使曾試圖形成該Mg-摻雜GaN層以致於一方面僅該Mg-摻雜GaN層之一正好在該閘極電極下面的區域被激活而另一方面其他區域維持未激活，在該激活區域與該未激活區域之間的邊界會由於加熱狀態或其類似而變動。據此，製成之HEMT的良率會被降低，而製成之HEMT的一致性會被降低。明確地，當該Mg-摻雜GaN層的厚度為了保證該Mg-摻雜GaN的常關狀態而被增加時，以上的結果會顯著地呈現。

此外，該GaN的晶體結構是為一六角形吳氏結構(hexagonal wurtzite structure)，其缺少在c-軸方向上的反向對稱(inversion symmetry)。因此，該GaN展現自發極性(spontaneous polarization)。此外，當該晶體結構被拉緊(strained)時，該GaN展現壓電極化。據此，該GaN會產生一內部場(internal field)。該內部場已知是比藉由摻雜一雜質元素來產生的電場強。通常，該GaN層的表面是為一Ga表面。因此，以Ga穩定表面生長，該GaN層的表面包括負壓電電荷而該GaN層的後表面包括一正電氣層。據此，氫(質子)會由於該內部場的效應而難以在表面方向上通過。這會降低Mg的激活速率，其使它難以產生電洞。結果，會是難以讓該Mg-摻雜GaN層處於常關狀態。

據此，是希望提供一種製造方法和一種使用像是GaN或其類似般之氮化物半導體作為半導體材料的半導體裝置，其能夠在沒有增加開啟-電阻之下展現高一致性和常關

狀態。

【發明內容】

發明概要

根據該等實施例之一特徵，一種用於製造半導體裝置的方法被提供。該方法包括相繼地在一基體上形成一第一半導體層、一第二半導體層和一包含p-型雜質元素的半導體頂蓋層；在該半導體頂蓋層的形成之後形成一具有一開孔的介電層；在該從介電層之開孔露出之半導體頂蓋層上形成一包含p-型雜質元素的第三半導體層；及在該第三半導體層上形成一閘極電極。

本發明之目的和優點將會藉著在後附之申請專利範圍中所特別指出的元件與組合來被實現與達成。

要了解的是，前面的大致說明以及後面的詳細描述皆是為範例與解釋而已並非是本發明的限制。

該等實施例的其他目的和優點將會部份在後面的說明中陳述，而部份將會由於該說明而顯而易見，或者可以藉由本發明的實施而獲悉。

圖式簡單說明

第1圖是為一描繪一使用GaN之習知高電子遷移率電晶體(HEMT)的結構圖；

第2圖是為一描繪一第一實施例之半導體裝置的結構圖；

第3A、3B和3C圖是為描繪該第一實施例之半導體裝置之製造方法的製程圖；

第4A和4B圖是為描繪該第一實施例之半導體裝置之製造方法的製程圖；

第5圖是為一描繪該第一實施例之半導體裝置之閘極電壓與汲極電流的特性圖；

第6圖是為一描繪該第一實施例之另一半導體裝置的結構圖；

第7圖是為一描繪一第二實施例之半導體裝置的結構圖；

第8A、8B和8C圖是為描繪該第二實施例之半導體裝置之製造方法的製程圖；

第9圖是為一描繪該第二實施例之半導體裝置之製造方法的製程圖；

第10圖是為一描繪一第三實施例之分離半導體封裝體的說明圖；

第11圖是為該第三實施例之電源供應單元的電路圖；及

第12圖是為一描繪該第三實施例之高功率放大器的結構圖。

【實施方式】

較佳實施例之詳細說明

在後面，較佳實施例是配合該等附圖來作描述。注意的是，完全相同的組件是設有相同的標號而且同一的組件的重覆說明是被省略。

[第一實施例]

[半導體裝置]

一第一實施例的半導體裝置是配合第2圖作描述。該第一實施例的半導體裝置包括相繼地形成於一基體11上的一第一緩衝層12、一第二緩衝層13、一作用如一第一半導體層的電子轉移層14、一作用如一第二半導體層的電子捐獻層15和一較低Mg-摻雜GaN層16。注意的是，作用如一半導體頂蓋層的該較低Mg-摻雜GaN層16是由一p-型雜質-摻雜氮化物半導體層形成。一較高Mg-摻雜GaN層17是由一p-型雜質-摻雜氮化物半導體層形成而且是作用如該第三半導體層。該較高Mg-摻雜GaN層17是形成在該較低Mg-摻雜GaN層16上正好在該閘極電極31下面。此外，一介電層21是形成於該較低Mg-摻雜GaN層16之一不包括該較低Mg-摻雜GaN層之一形成有該較高Mg-摻雜GaN層17之區域的區域內。該閘極電極31是經由一絕緣薄膜22來形成在該較高Mg-摻雜GaN層17上。該源極電極32和該汲極電極33被形成以致於該源極電極32與該汲極電極33變成與該較低Mg-摻雜GaN層16接觸。

在這實施例中，該基體11是由一Si基體形成，該第一緩衝層12是由氮化鋁(AlN)形成，而該第二緩衝層13是由氮化鋁鎵(AlGaN)形成。此外，作用如該第一半導體層的該電子轉移層14是由i-GaN形成而作用如該第二半導體層的該電子捐獻層15是由i-AlGaN形成。此外，該介電層21是由一包含氧化物或氮化物的介電材料形成。如此之材料的範例包括SiO_2。該絕緣薄膜22可以作用如一閘極絕緣薄膜而且

可以藉著原子層沉積(ALD)來由一像是氧化鋁般的絕緣體形成。

在這實施例中，作用如一半導體頂蓋層的該較低Mg-摻雜GaN層16包括一p-GaN區域16a和一高阻抗區域16b。該p-GaN區域16a是正好形成在該閘極電極31下面。據此，該高阻抗區域16b是形成在該較低Mg-摻雜GaN層16(即，該半導體頂蓋層)之一不包括一正好在該閘極電極31下面之區域的區域內。注意的是，該雜質元素Mg被激活而被激活的Mg是為在該p-GaN區域16a內的一p-型。因此，該Mg被鍵結到在高阻抗區域16b內的氫以致於該雜質元素Mg不被激活。結果，該高阻抗區域16b具有比該p-GaN區域16a高的電阻率。作用如第三半導體層的該較高Mg-摻雜GaN層17是形成在該較低Mg-摻雜GaN層16的p-GaN區域16a內。因此，該雜質元素Mg被激活以致於該被激活Mg是為一p-型。結果，該高阻抗區域16b具有比該較低Mg-摻雜GaN層16之p-GaN區域16a之氫密度高的氫密度。

據此，在形成於該在電子轉移層14與電子捐獻層15之間之介面附近的2DEG 14a中，在沒有降低在一正好於高阻抗區域16a下面之區域中的電子密度之下，電子會僅從一個正好在該p-GaN區域16a下面的區域消除。據此，要在沒有增加在第一實施例之半導體裝置中之開啟-電阻之下實現一常關狀態會是有可能的。注意的是，在這實施例中，形成正好在閘極電極31下面的該較高Mg-摻雜GaN層17和該p-GaN區域16a是比該高阻抗區域16b厚。因此，正好在閘極

電極31下面之2DEG的電子會被可靠地消除。因此，要更可靠地在沒有增加在第一實施例之半導體裝置中之開啟-電阻之下高一致性地實現一常關狀態會是有可能的。

注意的是，在這實施例中，正好在該p-GaN區域16a及其類似下面的區域包括一個比該電子捐獻層15低的區域。正好在閘極電極31下面的區域包括一個比該p-GaN區域16a與該電子捐獻層15低的區域。

[半導體裝置的製造方法]

接著，該第一實施例之半導體裝置的製造方法是配合第3A至3C圖與第4A和4B圖來作說明。

初始地，如在第3A圖中所示，包括該第一緩衝層12、該第二緩衝13、該電子轉移層14、該電子捐獻層15、和該較低Mg-摻雜GaN層16的氮化物半導體層是藉由MOVPE來外延地長成在該基體11上。在這實施例中，該第一緩衝層12是由具有大約200 nm之厚度的AlN形成，而該第二緩衝層13是由具有大約600 nm之厚度的AlGaN形成。此外，該電子轉移層14是由具有大約1200 nm之厚度的GaN形成，而該電子捐獻層15是由具有大約20 nm之厚度的AlGaN形成。該較低Mg-摻雜GaN層16具有大約3 nm的厚度。

當這些氮化物半導體層是藉MOVPE來沉積時，三甲基鋁(TMA)是被用作Al的來源氣體，三甲基鎵(TMG)是被用作Ga的來源氣體，而氨(NH3)是被用作N的來源氣體。此外，環戊二烯鎂(Cp2Mg)是被用作Mg的來源氣體。注意的是，這些來源氣體是與作為載氣(carrier gas)的氫(H_2)一起被供

應到一MOVPE裝置的反應器。

此外，一用於形成該等氮化物半導體層的氨氣體是在100至10000 sccm的流速範圍下被供應，而一用於形成該等氮化物半導體層的生長壓力是在1000至1200℃的生長溫度範圍下在50至300 Torr下被施加。

該基體11可以是一藍寶石基體、一Si基體、和一SiC基體。在這實施例中，該SiC基體是被用作該基體11。

當該第二緩衝層13是被表示為$Al_xGa_{1-x}N$時，該第二緩衝層13被形成以致於該X值是0.4。即，該第二緩衝層13是形成如$Al_{0.4}Ga_{0.6}N$。

當該電子捐獻層15是被表示為$Al_xGa_{1-x}N$時，該電子捐獻層15被形成以致於該X值是在0.1至0.3的範圍內。在這實施例中，該電子捐獻層15被形成以致於該X值是0.2。即，該電子捐獻層15是形成如$Al_{0.2}Ga_{0.8}N$。此外，該電子捐獻層15可以是i-AlGaN或n-AlGaN。當該電子捐獻層15是n-AlGaN時，Si被摻雜作為一雜質元素。在這情況中，該Si被摻雜以致於Si的濃度是在1 x $10^{18}cm^{-3}$至1 x $10^{20}cm^{-3}$的範圍內，像是1 x $10^{19}cm^{-3}$般。在這情況中，SiH_4可以作為Si的來源氣體。

該較低Mg-摻雜GaN層16是由在5 x $10^{18}cm^{-3}$至5 x $10^{20}cm^{-3}$之雜質濃度範圍下被摻雜有Mg作為雜質元素的GaN形成。在這實施例中，該較低Mg-摻雜GaN層16被形成以致於Mg是在1 x $10^{19}cm^{-3}$的雜質濃度下被摻雜在GaN內作為雜質元素。注意的是，緊在被沉積之後該較低Mg-摻雜

GaN層16在其之薄膜內含有氫。因此，氫是鍵結至Mg以致於Mg未被激活。結果，該較低Mg-摻雜GaN層16展現高電阻率。

接著，如在第3B圖中所示，一介電層21是形成在該較低Mg-摻雜GaN層16之一表面之一個不包括一個形成有閘極電極31之區域的區域內。明確地，像是SiO_2般的介電層21是著濺鍍或其類似來沉積在該較低Mg-摻雜GaN層16的表面上以致於該介電層21的厚度是大約200 nm。隨後，一未在圖中顯示的光阻是施加到該介電層21的表面，而該施加有光阻的介電層21然後是利用曝光裝置來曝露於光線以供顯影，藉此形成一具有一對應於該形成有閘極電極31之區域之開孔之未在圖中顯示的光阻圖案。其後，該介電層21是藉濕蝕刻或乾蝕刻來從該較低Mg-摻雜GaN層16之表面之一未形成有光阻圖案的區域移除。結果，具有一對應於該形成有閘極電極31之區域之開孔21a的介電層21是利用SiO_2來形成。該光阻圖案然後是以有機溶劑或其類似來移除。注意的是，該介電層21可以是由SiN或其類似來形成。

接著，如在第3C圖中所示，得到的成品是在氮大氣下於400至1000℃的溫度範圍下加熱。據此，含在該較低Mg-摻雜GaN層16內的氫成分是在該較低Mg-摻雜GaN層16之表面之一對應於該未形成有介電層21之開孔21a的區域內排出。因此，該較低Mg-摻雜GaN層16之對應於開孔21a的區域被激活以致於該區域變成一p-型。結果，一p-GaN區域16a被形成。注意的是，在該較低Mg-摻雜GaN層16之表面

之形成有介電層21的區域內，氫的排出是被介電層21禁止。因此，氫未從該較低Mg-摻雜GaN層16之形成有介電層21的區域消除。據此，在該較低Mg-摻雜GaN層16的介電層21形成區域內，Mg與H的鍵結是保持以致於該Mg未被激活。結果，該高阻抗區域16b是形成在該較低Mg-摻雜GaN層16的介電層21形成區域內。在這實施例中，該較低Mg-摻雜GaN層16的厚度是極薄成大約3 nm。據此，晶體拉緊會是細微的而該內部場會是細微的。因此，含在該較低Mg-摻雜GaN層16之對應於該開孔21a之區域內的氫會經由該介電層21的開孔21a來希效地消除。此外，該較低Mg-摻雜GaN層16的厚度是極薄成大約3 nm。據此，含在該較低Mg-摻雜GaN層16內的氫會僅從該較低Mg-摻雜GaN層16之對應於該開孔21a的區域消除。據此，在p-GaN區域16a與高阻抗區域16b之間的介面可以是高可再生性地形成在一預定位置。有鑑於以上所述，最好的是，該Mg-摻雜GaN層16的厚度是大於或相等於3 nm而且是小於或相等於10 nm。因此，該p-GaN區域16a是形成在該較低Mg-摻雜GaN層16之一未形成有介電層21的區域內，而該高阻抗區域16b是形成在該較低Mg-摻雜GaN層16之一不包括一形成有介電層21之區域的區域內。在這實施例中，熱處理是藉由把介電層21形成層置於該MOVPE裝置內，以及把該MOVPE之充填有氮大氣的腔室加熱來進行。

接著，如在第4A圖中所示，該較高Mg-摻雜GaN層17是形成在該露出該較低Mg-摻雜GaN層16的p-GaN區域16a

內。更明確地，由於該較高Mg-摻雜GaN層17是選擇地藉MOVPE以外延生長來形成，晶體是僅在該露出該較低Mg-摻雜GaN層16的p-GaN區域內生長而少許的晶體是在該介電層21上生長。因此，該較高Mg-摻雜GaN層17是僅在該露出該較低Mg-摻雜GaN層16的p-GaN區域16a內形成。注意的是，該較高Mg-摻雜GaN層17可以由在5 x $10^{18}cm^{-3}$至5 x $10^{20}cm^{-3}$的雜質濃度範圍下摻雜有Mg的GaN形成。在這實施例中，該較高Mg-摻雜GaN層17是由在1 x $10^{19}cm^{-3}$的雜質濃度範圍下摻雜有Mg的GaN形成。

其後，該較高Mg-摻雜GaN層17是在氮大氣之下加熱來消除氫，其會把該較高Mg-摻雜GaN層17激活成p-型。在該較高Mg-摻雜GaN層17中，氫會從一個橫向於其之無產生內部場之薄膜表面的方向消除。即，氫會從該較高Mg-摻雜GaN層17的薄膜厚度方向消除。據此，較大量的氫會被有效地消除。

最好的是，該較高Mg-摻雜GaN層17的厚度範圍是50至200 nm。在這實施例中，該較高Mg-摻雜GaN層17的厚度是大約50 nm。最好的是，該較高Mg-摻雜GaN層17被形成以致於該較高Mg-摻雜GaN層17具有適足的厚度來供應較大量的電洞。此外，最好的是，該較高Mg-摻雜GaN層17被形成比該較低Mg-摻雜GaN層16厚。在這實施例中，該熱處理和該較高Mg-摻雜GaN層17的沉積可以在該MOVPE裝置的同一腔室之內被連續執行。因此，要防止粒子貼附到該長成有該較高Mg-摻雜GaN層17的p-GaN區域16a會是有

可能的。

接著，如在第4B圖中所示，一作用如閘極絕緣薄膜的絕緣薄膜22是形成在該較高Mg-摻雜GaN層17上而一閘極電極31是形成在該絕緣薄膜22上。此外，該介電層21是從形成有源極電極32與汲極電極33之對應的區域移除，而源極電極32與汲極電極33是形成在移除掉介電層21之對應的區域內。

該第一實施例的半導體裝置能夠以以上所述的製程製成。在該第一實施例的半導體裝置中，該較高Mg-摻雜GaN層17與該較低Mg-摻雜GaN層16的p-GaN區域16a是在一個經過該絕緣薄膜22正好在閘極電極31下面的區域內被激活，而因此，會有可能產生很多電洞。據此，2DEG 14a的電子可以在一個正好在閘極電極31下面的區域內消除，而閘極電壓可以如在第5圖中所示轉移在一正側，而結果，該第一實施例的半導體裝置可以被構築成處於一常關狀態。注意的是，在第5圖中，一虛線5A表示在第1圖中所示之結構HEMT的特性而一實線5B表示在第2圖中所示之這實施例之結構HEMT的特性。

在這實施例中，該較低Mg-摻雜GaN層16的高阻抗區域16b展現高電阻率。因此，該2DEG 14a的電子在一正好在該高阻抗區域16b下面的區域內可以被防止減少，而該開啟-電阻可以被防止增加。此外，該p-型較高Mg-摻雜GaN層17、該p-GaN區域16a和該高阻抗區域16b具有不同的厚度以致於在它們之間的邊界可以被清楚界定。據此，該第一實

施例的半導體裝置可以展現高良率與優異的一致性。

注意的是，在第3C圖中所示的熱處理中，當該較低Mg-摻雜GaN層16是薄時，供應之電洞的量會是相似的。據此，要在沒有執行熱處理之下得到展現相似之一致性的半導體裝置會是有可能的。

此外，以上所述的第一實施例描述該具有一包括絕緣薄膜22之結構的半導體裝置；然而，如在第6圖中所示，該第一實施例的半導體裝置可以具有一沒有絕緣薄膜22的結構。明確地，具有該沒有絕緣薄膜22之結構的半導體裝置可以藉由形成該具有在第4A圖中所示之較高Mg-摻雜GaN層17之結構而隨後在沒有形成該絕緣薄膜22之下於該較高Mg-摻雜GaN層17上形成閘極電極31來形成。

[第二實施例]

(半導體裝置)

接著，一第二實施例被說明。如在第7圖中所示，該第二實施例的半導體裝置包括相繼地形成於一基體11上的一第一緩衝層12、一第二緩衝層13、一作用如一第一半導體層的電子轉移層14和一作用如一第二半導體層的電子捐獻層15。一較高Mg-摻雜GaN層117是由一p-型雜質-摻雜氮化物半導體層形成而且是作用如該第三半導體層。該較高Mg-摻雜GaN層117是形成在該電子捐獻層15上正好在該閘極電極31下面。此外，一介電層21是形成在該電子捐獻層15之一不包括一形成有該較高Mg-摻雜GaN層117之區域的區域內。該閘極電極31是經由一絕緣薄膜22來形成在該較高

Mg-摻雜GaN層117上。該源極電極32與該汲極電極33被形成以致於該源極電極32與該汲極電極33變成與該電子捐獻層15接觸。

在這實施例中，該基體11是由一Si基體形成，該第一緩衝層12是由氮化鋁(AlN)形成，而該第二緩衝層13是由氮化鋁鎵(AlGaN)形成。此外，該作用如第一半導體層的電子轉移層14是由i-GaN形成而該作用如第二半導體層的電子捐獻層15是由i-AlGaN形成。此外，該介電層21是由一含氧化物或氮化物的介電材料形成。如此之一種材料的範例包括SiO_2。該作用如一閘極絕緣薄膜的絕緣薄膜22可以藉著原子層沉積(ALD)由一像是氧化鋁般的絕緣體形成。

在該第二實施例中，作用為該第三半導體層的該較高Mg-摻雜GaN層117是形成在一個正好在閘極電極31下面的區域內。因此，該雜質元素Mg被激活以致於被激活的Mg是一p-型。據此，該2DEG 14a是形成於該在電子轉移層14與電子捐獻層15之間的介面附近，而該等電子可以僅從該電子轉移層14之一正好在該較高Mg-摻雜GaN層117下面的區域消除。即，在沒有降低在該正好在一未形成有該較高Mg-摻雜GaN層117之區域下面之區域中的電子密度之下，該2DEG 14a的電子可以僅從一正好在一形成有該較高Mg-摻雜GaN層117之區域下面的區域消除。據此，在沒有增加開啟-電阻之下，該第二實施例的半導體裝置可以被構築來處於一常關狀態。

在該第二實施例的半導體裝置中，該p-型Mg-摻雜GaN

層117是形成正好在該閘極電極31下面。此外，雖然該介電層21是形成在一不包括該形成有閘極電極31之區域的區域內，一p-型區域是未形成。因此，正好在閘極電極31下面之該2DEG 14a的電子可以被可靠地消除。因此，要更可靠地在沒有該第二實施例之半導體裝置中之開啟-電阻之下高一致性地實現一常關狀態會是有可能的。

(半導體裝置的製造方法)

接著，該第一實施例之半導體裝置的製造方法是配合第8A至8C圖和第9圖來作說明。

初始地，如在第8A圖中所示，該第一緩衝層12、該第二緩衝層13、該電子轉移層14和該電子捐獻層15、以及該較低Mg-摻雜GaN層16是藉著MOVPE來在該基體11上外延地生長。在這實施例中，該第一緩衝層12是由具有大約200 nm之厚度的AlN形成，而該第二緩衝層13是由具有大約600 nm之厚度的AlGaN形成。此外，該電子轉移層14是由具有大約1200 nm之厚度的GaN形成，而該電子捐獻層15是由具有大約20 nm之厚度的AlGaN形成。

當這些氮化物半導體層是藉著MOVPE來沉積時，三甲基鋁(TMA)是被用作Al的來源氣體，三甲基鎵(TMG) (TMG)是被用作Ga的來源氣體，氨(NH3)是被用作N的來源氣體。此外，環戊二烯鎂(Cp2Mg)是被用作Mg的來源氣體。注意的是，這些來源氣體是與作為載氣(carrier gas)的氫(H_2)一起被供應到一MOVPE裝置的反應器。

此外，一用於形成該等氮化物半導體層的氨氣體是在

100至10000 sccm的流速範圍下被供應，而一用於形成該等氮化物半導體層的生長壓力是在1000至1200℃的生長溫度範圍下在50至300 Torr下被施加。

該基體11可以是一藍寶石基體、一Si基體、和一SiC基體。在這實施例中，該SiC基體是被用作該基體11。

當該第二緩衝層13是被表示為$Al_xGa_{1-x}N$時，該第二緩衝層13被形成以致於該X值是0.4。即，該第二緩衝層13是形成如$Al_{0.4}Ga_{0.6}N$。

當該電子捐獻層15是被表示為$Al_xGa_{1-x}N$時，該電子捐獻層15被形成以致於該X值是在0.1至0.3的範圍內。在這實施例中，該電子捐獻層15被形成以致於該X值是0.2。即，該電子捐獻層15是形成如$Al_{0.2}Ga_{0.8}N$。此外，該電子捐獻層15可以是i-AlGaN或n-AlGaN。當該電子捐獻層15是n-AlGaN時，Si被摻雜作為一雜質元素。在這情況中，該Si被摻雜以致於Si的濃度是在1 x $10^{18}cm^{-3}$至1 x $10^{20}cm^{-3}$的範圍內，像是1 x $10^{19}cm^{-3}$般。在這情況中，SiH_4可以作為Si的來源氣體。

接著，如在第8B圖中所示，一介電層21是形成在該電子捐獻層15之一表面之一個不包括一個形成有閘極電極31之區域的區域內。明確地，像是SiO_2般的介電層21是著濺鍍或其類似來沉積在該電子捐獻層15的表面上以致於該介電層21的厚度是大約200 nm。隨後，一未在圖中顯示的光阻是施加到該介電層21的表面，而該施加有光阻的介電層21然後是利用曝光裝置來曝露於光線以供顯影，藉此形成

一具有一對應於該形成有閘極電極31之區域之開孔之未在圖中顯示的光阻圖案。其後，該介電層21是藉濕蝕刻或乾蝕刻來從該電子捐獻層15之表面之一未形成有光阻圖案的區域移除。結果，具有一對應於該形成有閘極電極31之區域之開孔21a的介電層21是利用SiO_2來形成。然後，該光阻圖案然後是以有機溶劑或其類似來移除。注意的是，該介電層21可以是由SiN或其類似來形成。

接著，如在第8C圖中所示，該Mg-摻雜GaN層117是形成在一對應於該介電層21之開孔21a之露出該電子捐獻層15的區域內。更明確地，由於該Mg-摻雜GaN層117是藉著MOVPE以外延長成來選擇地形成，晶體是僅在一對應於該介電層21之露出該電子捐獻層15之開孔21a的區域內生長而少許的晶體是在該介電層21上生長。因此，該Mg-摻雜GaN層117可以僅在該露出電子捐獻層15的區域內形成。注意的是，該Mg-摻雜GaN層117可以由在$5 \times 10^{18}cm^{-3}$至$5 \times 10^{20}cm^{-3}$的雜質濃度範圍下摻雜有Mg的GaN形成。在這實施例中，該Mg-摻雜GaN層117是由在$1 \times 10^{19}cm^{-3}$的雜質濃度範圍下摻雜有Mg的GaN形成。

其後，該Mg-摻雜GaN層117是在氮大氣之下加熱來消除氫，其會把該Mg-摻雜GaN層117激活成p-型。在該Mg-摻雜GaN層117中，氫會從一個橫向於其之無產生內部場之薄膜表面的方向消除。即，氫會從該較高Mg-摻雜GaN層117的薄膜厚度方向消除。據此，較大量的氫會被有效地消除。注意的是，最好的是，該Mg-摻雜GaN層117的厚度範圍是

在50至200 nm的範圍內。在這實施例中，該較高Mg-摻雜GaN層117的厚度是大約50 nm。

接著，如在第9圖中所示，一作用如閘極絕緣薄膜的絕緣薄膜22是形成在該Mg-摻雜GaN層17上而一閘極電極31是形成在該絕緣薄膜22上。此外，該介電層21是從形成有源極電極32與汲極電極33之對應的區域移除，而源極電極32與汲極電極33是形成在移除掉介電層21之對應的區域內。

該第二實施例的半導體裝置能夠以以上所述的製程製成。在該第二實施例的半導體裝置中，該Mg-摻雜GaN層117是在一個經過該絕緣薄膜22正好在閘極電極31下面的區域內被激活，而因此，會有可能產生很多電洞。據此，2DEG 14a的電子可以在一個正好在閘極電極31下面的區域內消除，而閘極電壓可以轉移在一正側。結果，該第二實施例的半導體裝置可以被構築成處於一常關狀態。此外，該Mg-摻雜GaN層117未形成在一不包括該正好在閘極電極31下面之區域的區域內。因此，在該正好在閘極電極31下面之區域內之2DEG 14a的電子可以被防止減少，而該開啟-電阻可以被防止增加。在該第二實施例的半導體裝置中，該p-型Mg-摻雜GaN層117是形成在一正好在閘極電極31下面的區域內。因此，一未形成有該p-型Mg-摻雜GaN層117之區域的邊界可以被清楚界定。結果，製成之半導體裝置的一致性可以被改進而製成之半導體裝置的良率可以被提升。

此外，以上所述的第二實施例描述該具有一包括絕緣

薄膜22之結構的半導體裝置；然而，該第二實施例的半導體裝置可以具有一沒有絕緣薄膜22的結構。明確地，具有該沒有絕緣薄膜22之結構的半導體裝置可以藉由形成該包括在第8C圖中所示之Mg-摻雜GaN層117之結構而隨後在沒有形成該絕緣薄膜22之下於該Mg-摻雜GaN層117上形成閘極電極31來形成。

注意的是，該第二實施例之半導體裝置的其他結構與特徵是與該第一實施例之半導體裝置的那些相同。

[第三實施例]

接著，一第三實施例是作說明。該第三實施例描述一半導體封裝體、一電源供應單元以及一高頻放大器。

該第三實施例的半導體封裝體包括該第一實施例或該第二實施例之半導體裝置的分離封裝體，即，該分離封裝半導體封裝體。因此，該分離封裝半導體封裝體是配合第10圖來作說明。注意的是，第10圖示意地描繪該分離封裝半導體封裝體的內部結構。因此，在該分離封裝半導體封裝體之結構內之電極或其類似的佈置可以是與該第一實施例或該第二實施例之半導體裝置的不同。

初始地，一由GaN半導體材料製成的高電子遷移率電晶體(HEMT)半導體晶片410可以藉由切割在第一實施例或第二實施例中製成的半導體裝置來形成。該半導體晶片410是藉一像是錫般的固晶黏著劑430來固定至一導線架420上。注意的是，該半導體晶片410相當於第一實施例或第二實施例的半導體裝置。

隨後，一閘極電極411是藉導線431來連接到一閘極端子421。一源極電極412是藉導線432來連接到一源極端子422。一汲極電極413是藉導線433來連接到一源極端子423。注意的是，導線431,432和433是由像是鋁(Al)般的金屬材料形成。此外，在該第三實施例的半導體封裝體中，該閘極電極411是為一閘極電極墊，其是連接到該第一實施例或該第二實施例之半導體裝置的閘極電極31。此外，該源極電極412是為一源極電極墊，其是連接到該第一實施例或該第二實施例之半導體裝置的源極電極32。此外，該汲極電極413是為一汲極電極墊，其是連接到該第一實施例或該第二實施例之半導體裝置的閘極電極33。

隨後，所得到的產品是藉著像是轉移鑄模般的塑膠成型來以壓模樹脂(mold resin) 440密封。據此，使用該GaN半導體材料的該分離封裝HEMT半導體封裝體是被製成。

接著，該第三實施例的電源供應單元和高頻放大器是作說明。在第三實施例中的電源供應單元與高頻放大器是為使用在該第一實施例或該第二實施例中之半導體裝置的電源供應單元與高頻放大器。

初始地，在該第三實施例中的電源供應單元是配合第11圖作說明。在第三實施例中的電源供應單元460包括一高壓主要電路461、一低壓次要電路462和一配置在該主要電路461與該次要電路462之間的變壓器463。該主要電路461包括一交流(AC)電源供應器464、一個所謂的"橋式整流器電路(bridge rectifier circuit)"465、數個切換元件(在第11圖

之範例中四個切換元件) 466和一個切換元件467。該次要電路462包括數個切換元件(在第11圖之範例中三個切換元件)468。在第11圖的範例中，該第一實施例或該第二實施例的半導體裝置是被用作該主要電路461的該等切換元件466以及該切換元件467。注意的是，最好的是該主要電路461的該等切換元件466和該切換元件467是為常關半導體裝置。此外，在該次要電路462中所使用的該等切換元件使用一由矽形成的普通金屬絕緣半導體場效電晶體(MISFET)。

接著，在該第三實施例中的高頻放大器是配合第12圖作說明。在該第三實施例中的高頻放大器470可以應用作為一行動電話基地台的功率放大器。該高頻放大器470包括一數位預失真電路471、一混合器472、一功率放大器473和一定向耦合器474。該數位預失真電路471被構築來補償一輸入訊號的非線性應力。該混合器472被構築來把非線性應力被補償的該輸入訊號與一交流(AC)訊號混合。該功率放大器473被構築來把與該AC訊號混合的該輸入訊號放大。在第12圖的範例中，該功率放大器473包括該第一實施例或該第二實施例的半導體裝置。該定向耦合器474被構築來監視該輸入訊號或輸出訊號。在第12圖中所示的電路中，該混合器472可以把該輸出訊號與該AC訊號混合並且把該輸出訊號與該AC訊號的混合訊號供應到該數位預失真電路471。

根據該等揭示，使用一像是GaN或其類似般的氮化物半導體作為半導體材料來形成的半導體裝置以及用於製造

如此之半導體裝置的方法能夠在沒有增加開啟-電阻之下展現高一致性與一常關狀態。

於此中所述的所有例子和條件語言是傾向於為了幫助讀者了解本發明及由發明人所提供之促進工藝之概念的教育用途，並不是把本發明限制為該等特定例子和條件，且在說明書中之該等例子的組織也不是涉及本發明之優劣的展示。雖然本發明的實施例業已詳細地作描述，應要了解的是，在沒有離開本發明的精神與範疇之下，對於本發明之實施例之各式各樣的改變、替換、與變化是能夠完成。

【圖式簡單說明】

第1圖是為一描繪一使用GaN之習知高電子遷移率電晶體(HEMT)的結構圖；

第2圖是為一描繪一第一實施例之半導體裝置的結構圖；

第3A、3B和3C圖是為描繪該第一實施例之半導體裝置之製造方法的製程圖；

第4A和4B圖是為描繪該第一實施例之半導體裝置之製造方法的製程圖；

第5圖是為一描繪該第一實施例之半導體裝置之閘極電壓與汲極電流的特性圖；

第6圖是為一描繪該第一實施例之另一半導體裝置的結構圖；

第7圖是為一描繪一第二實施例之半導體裝置的結構圖；

第8A、8B和8C圖是為描繪該第二實施例之半導體裝置之製造方法的製程圖；

第9圖是為一描繪該第二實施例之半導體裝置之製造方法的製程圖；

第10圖是為一描繪一第三實施例之分離半導體封裝體的說明圖；

第11圖是為該第三實施例之電源供應單元的電路圖；及

第12圖是為一描繪該第三實施例之高功率放大器的結構圖。

【主要元件符號說明】

5A	虛線	22	絕緣薄膜
5B	實線	31	閘極電極
11	基體	32	源極電極
12	第一緩衝層	33	汲極電極
13	第二緩衝層	117	較高Mg-摻雜GaN層
14	電子轉移層	410	半導體晶片
15	電子捐獻層	411	閘極電極
16	較低Mg-摻雜GaN層	412	源極電極
16a	p-GaN區域	413	汲極電極
16b	高阻抗區域	420	導線架
17	較高Mg-摻雜GaN層	421	閘極端子
21	介電層	422	源極端子
21a	開孔	423	汲極端子

430	固晶黏著劑	470	高頻放大器
431	導線	471	數位預失真電路
432	導線	472	混合器
433	導線	473	功率放大器
440	壓模樹脂	474	定向耦合器
460	電源供應單元	911	基體
461	高壓主要電路	912	緩衝層
462	低壓次要電路	913	緩衝層
463	變壓器	914	電子轉移層
464	AC電源供應器	914a	2DEG
465	橋式整流器電路	915	電子捐獻層
466	切換元件	921	閘極電極
467	切換元件	922	源極電極
468	切換元件	923	汲極電極

201314898

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※申請案號：101128759

※申請日：101.8.9　　※IPC 分類：H01L 29/1078 2006.01

H01L 21/336 2006.01

一、發明名稱：（中文/英文）

半導體裝置及製造方法

SEMICONDUCTOR DEVICE AND FABRICATION METHOD

二、中文發明摘要：

一種用於製造半導體裝置的方法被揭露。該方法包括相繼地在一基體上形成一第一半導體層、一第二半導體層與一包含一p-型雜質元素的半導體頂蓋層；在該半導體頂蓋屠的形成之後形成一具有一開孔的介電層；在從該介電層之開孔露出的半導體頂蓋層上形成一包含一p-型雜質元素的第三半導體層；及在該第三半導體層上形成一閘極電極。

三、英文發明摘要：

A method for fabricating a semiconductor device is disclosed. The method includes sequentially forming a first semiconductor layer, a second semiconductor layer and a semiconductor cap layer containing a p-type impurity element on a substrate, forming a dielectric layer having an opening after the forming of the semiconductor cap layer, forming a third semiconductor layer containing a p-type impurity element on the semiconductor cap layer exposed from the opening of the dielectric layer, and forming a gate electrode on the third semiconductor layer.

七、申請專利範圍：

1.一種用於製造半導體裝置的方法，該方法包含：

於一基體上相繼地形成一第一半導體層、一第二半導體層和一含一p-型雜質元素的半導體頂蓋層；

在該半導體頂蓋層的形成之後形成一具有一開孔的介電層；

在該從介電層之開孔露出的半導體頂蓋層上形成一含有一p-型雜質元素的第三半導體層；及

在該第三半導體層上形成一閘極電極。

2.如申請專利範圍第1項所述之方法，更包含：

在該介電層的形成之後於一氮大氣之下進行一熱處理，其中，

該第三半導體層是在該熱處理已於該氮大氣之下進行之後被形成。

3.一種用於製造半導體裝置的方法，該方法包含：

於一基體上相繼地形成一第一半導體層和一第二半導體層；

在該第二半導體層的形成之後形成一具有一開孔的介電層；

在該從介電層之開孔露出的第二半導體層上形成一含有一p-型雜質元素的第三半導體層；及

在該第三半導體層上形成一閘極電極。

4.如申請專利範圍第1項所述之方法，其中

該第三半導體層的形成包括

沉積該第三半導體層，及

在該第三半導體層已沉積之後在一氮大氣之下進行熱處理。

5.如申請專利範圍第1項所述之方法，更包含：

在該第三半導體層上形成一絕緣層，其中

該閘極電極是經由該絕緣薄膜來形成在該第三半導體層上。

6.如申請專利範圍第1項所述之方法，其中

該p-型雜質元素是鎂(Mg)。

7.如申請專利範圍第1項所述之方法，其中

該第三半導體層是由金屬有機氣相外延(MOVPE)形成。

8.如申請專利範圍第1項所述之方法，更包含：

形成一源極電極和一汲極電極以致於該源極電極和該汲極電極變成與該第二半導體層或該半導體頂蓋層接觸。

9.一種半導體裝置，包含：

一形成於一基體上的第一半導體層；

一形成於該第一半導體層上的第二半導體層；

一形成於該第二半導體層上的半導體頂蓋層；

一形成於該半導體頂蓋層之一第一區域內的第三半導體層；

一形成於該第三半導體層上的閘極電極，該第三半導體層是形成在該半導體頂蓋層之位在該閘極電極下面的

第一區域內；及

一源極電極和一汲極電極被形成以致於該源極電極和該汲極電極變成與該第二半導體層或該半導體頂蓋層接觸，其中

該半導體頂蓋層和該第三半導體層是藉由摻雜一p-型雜質元素至一半導體材料來形成，且

該第三半導體層是為一p-型半導體層。

10.如申請專利範圍第9項所述之半導體裝置，其中

該半導體頂蓋層包括

一形成正好在該閘極電極下面的p-型區域，及

一形成於一不包括該p-型區域之區域內的高阻抗區域，該高阻抗區域具有比該p-型區域高的電阻率。

11.如申請專利範圍第10項所述之半導體裝置，其中

在該半導體頂蓋層之高阻抗區域內的氫濃度是比在該半導體頂蓋層之p-型區域內的氫濃度高。

12.如申請專利範圍第9項所述之半導體裝置，其中

該第一半導體層、該第二半導體層、該半導體頂蓋層和該第三半導體層是由一氮化物半導體形成。

13.如申請專利範圍第9項所述之半導體裝置，更包含：

一形成於該半導體頂蓋層之一不包括該形成有該第三半導體層之第一區域之第二區域內的介電層。

14.如申請專利範圍第13項所述之半導體裝置，其中

該介電層是由一含有二氧化矽(SiO_2)或氮化矽(SiN)的材料形成。

15.如申請專利範圍第9項所述之半導體裝置，其中

該p-型雜質元素是鎂(Mg)。

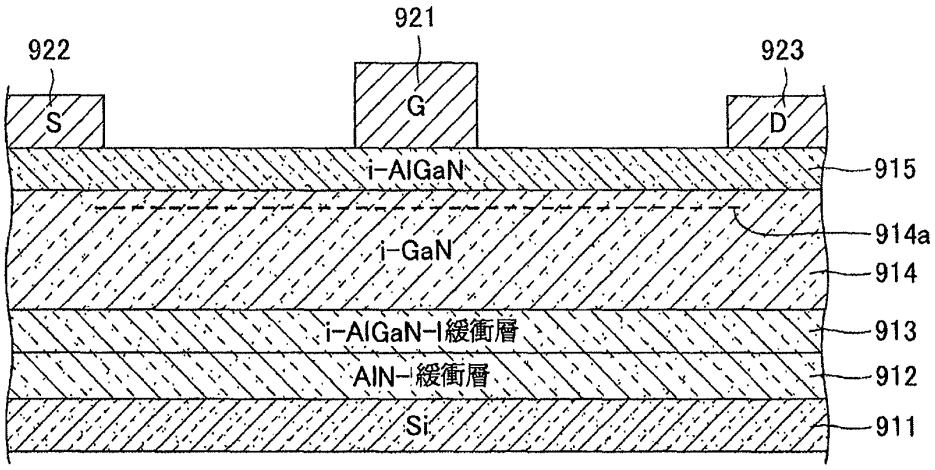
16.如申請專利範圍第9項所述之半導體裝置，更包含：

一形成在該第三半導體層與該閘極電極之間的絕緣薄膜。

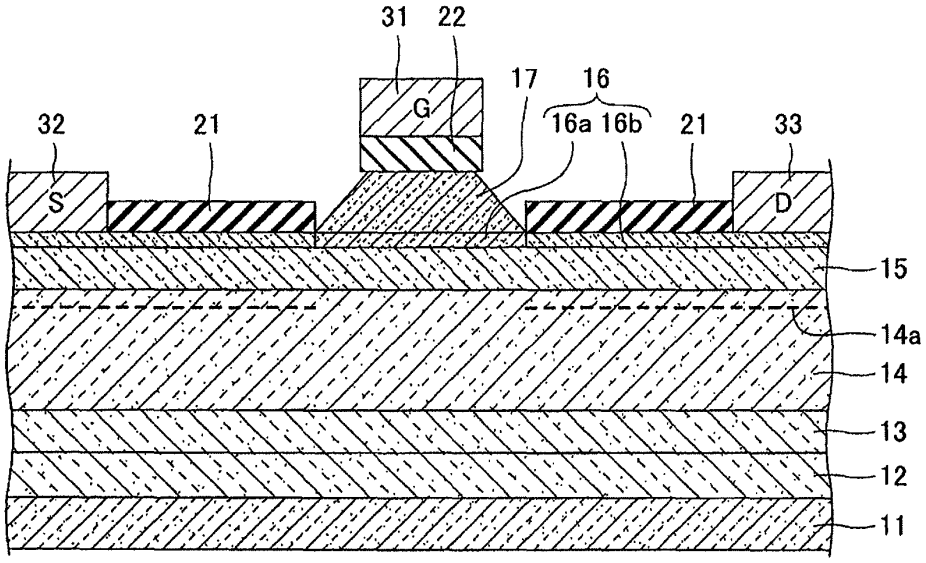
17.一種包含如在申請專利範圍第9項中所述之半導體裝置的電源供應單元。

18.一種包含如在申請專利範圍第9項中所述之半導體裝置的放大器。

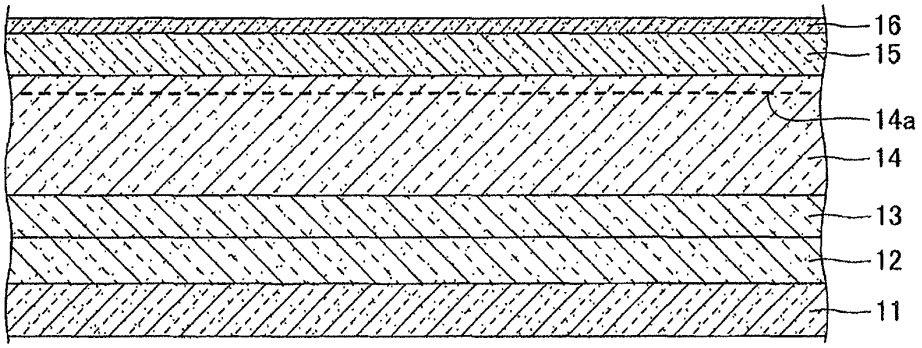
八、圖式：


921
922
923
S
G
D
i-AlGaN
915
914a
i-GaN
914
i-AlGaN-I緩衝層
913
AlN-緩衝層
912
Si
911

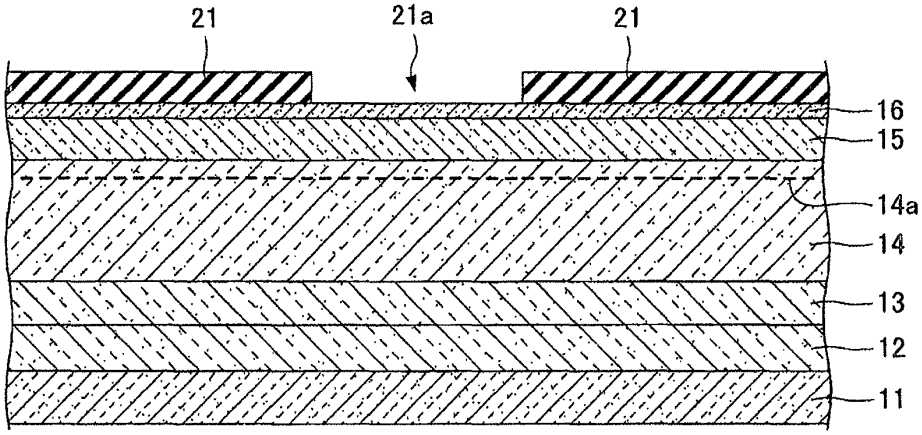
第1圖



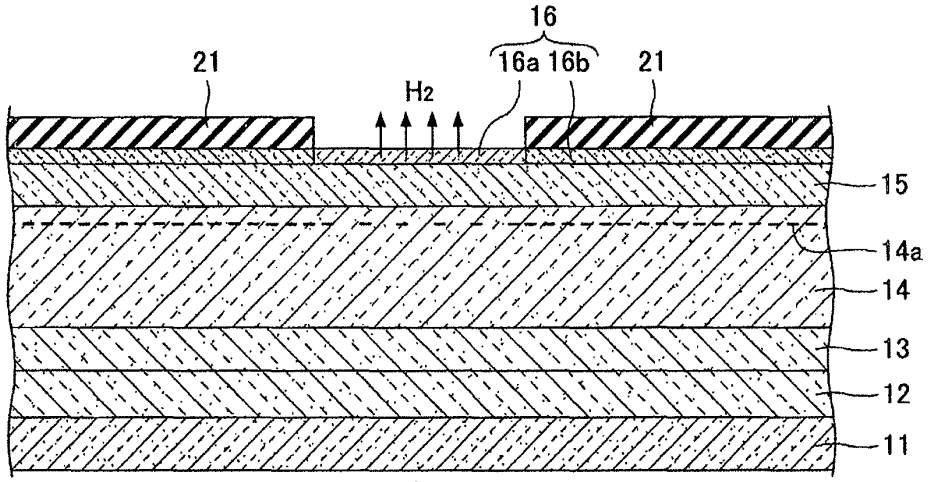
第2圖



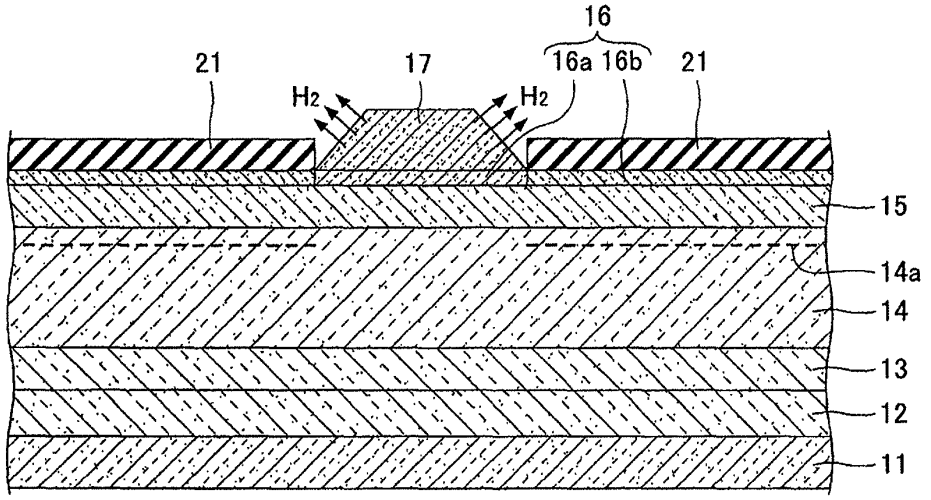
第3A圖



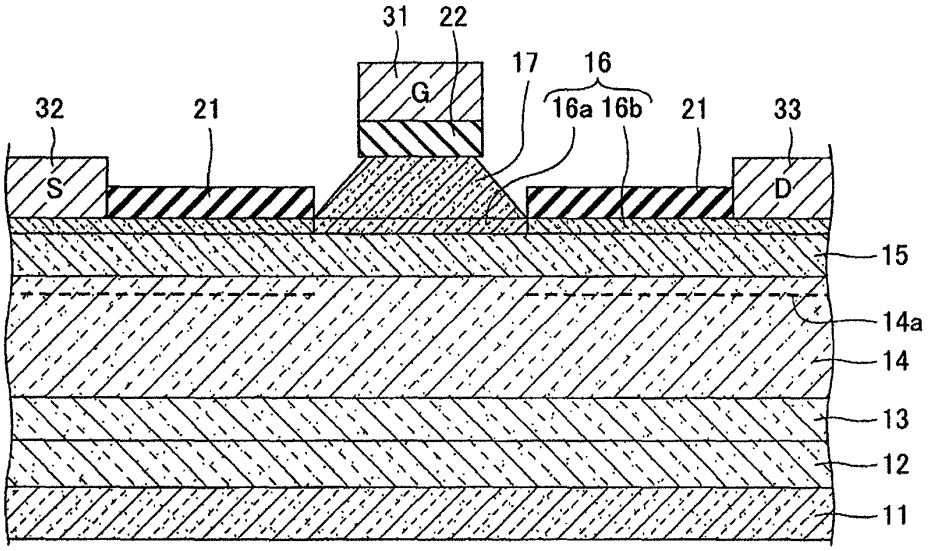
第3B圖



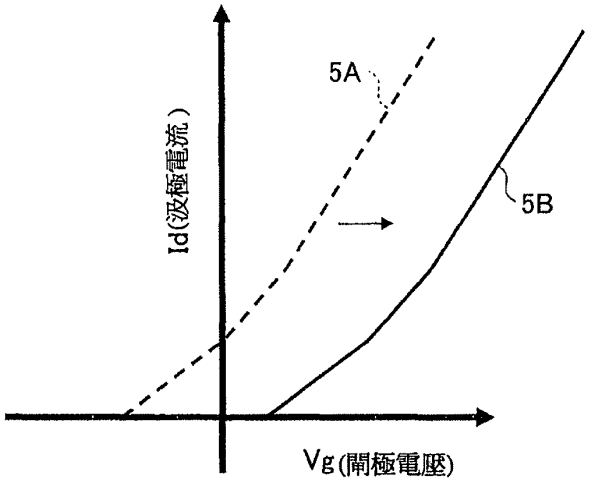
第3C圖


16
21
17
16a 16b
21
H2
H2
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14a
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12
11

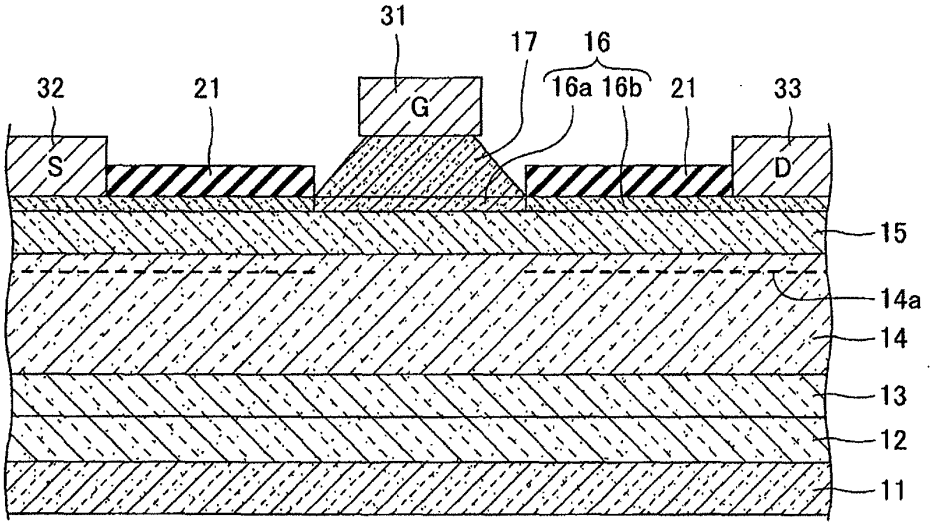
第4A圖


31
22
17
16
G
32
21
16a 16b
21
33
S
D
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14a
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12
11

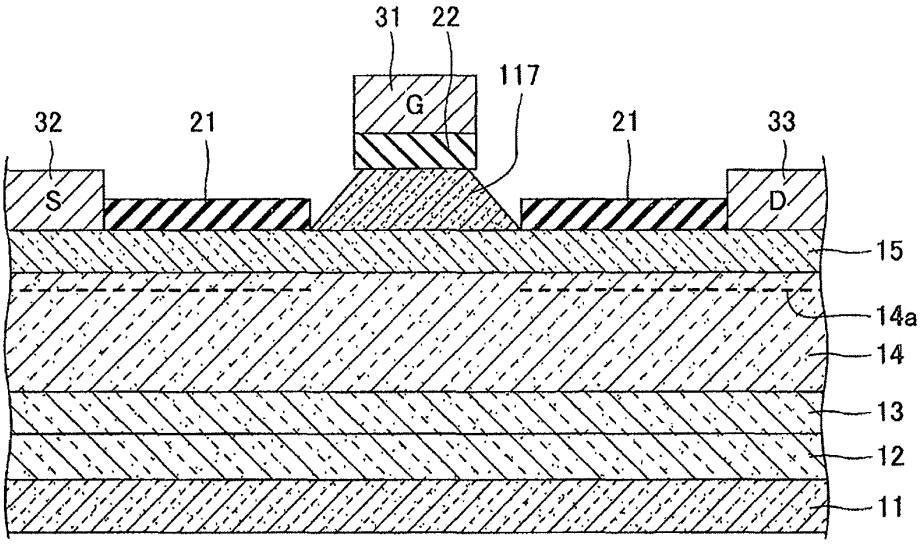
第4B圖



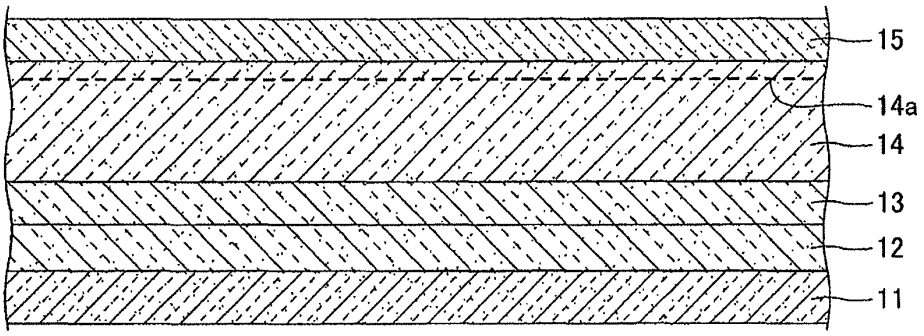
第5圖



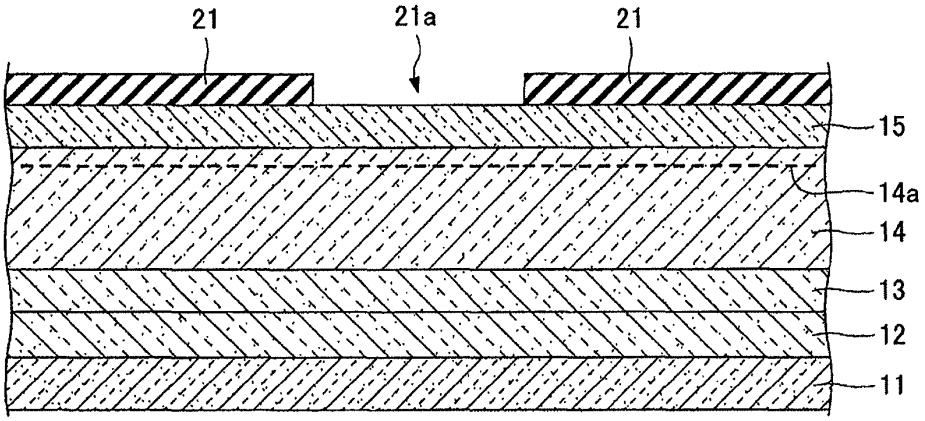
第6圖



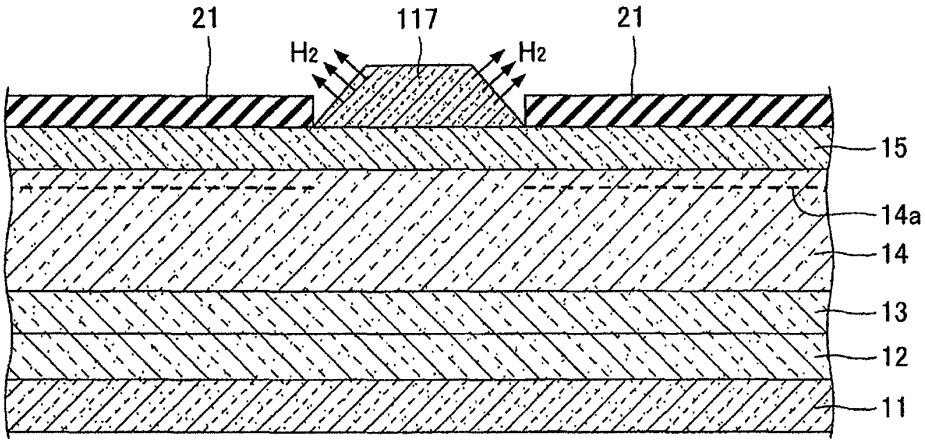
第7圖



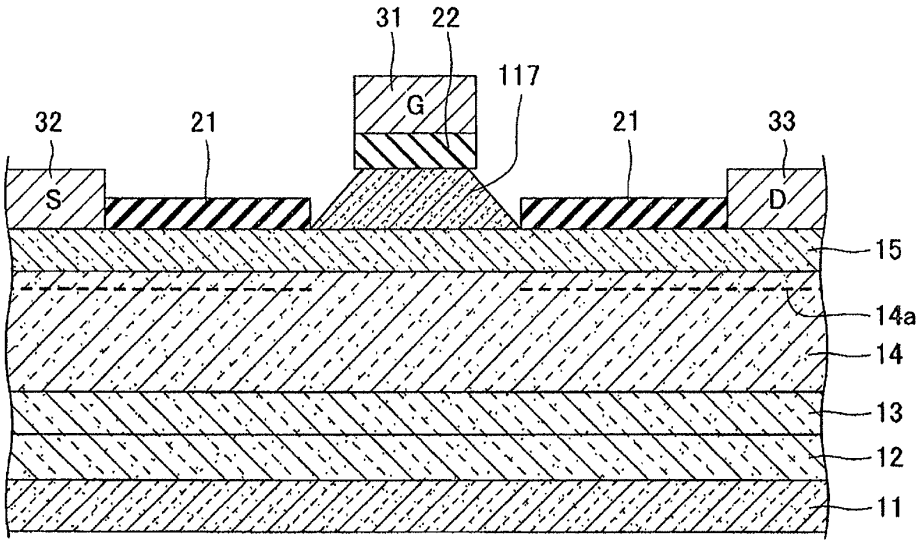
第8A圖



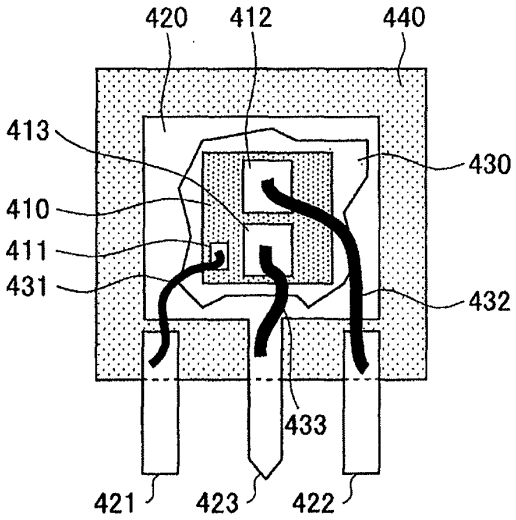
第8B圖



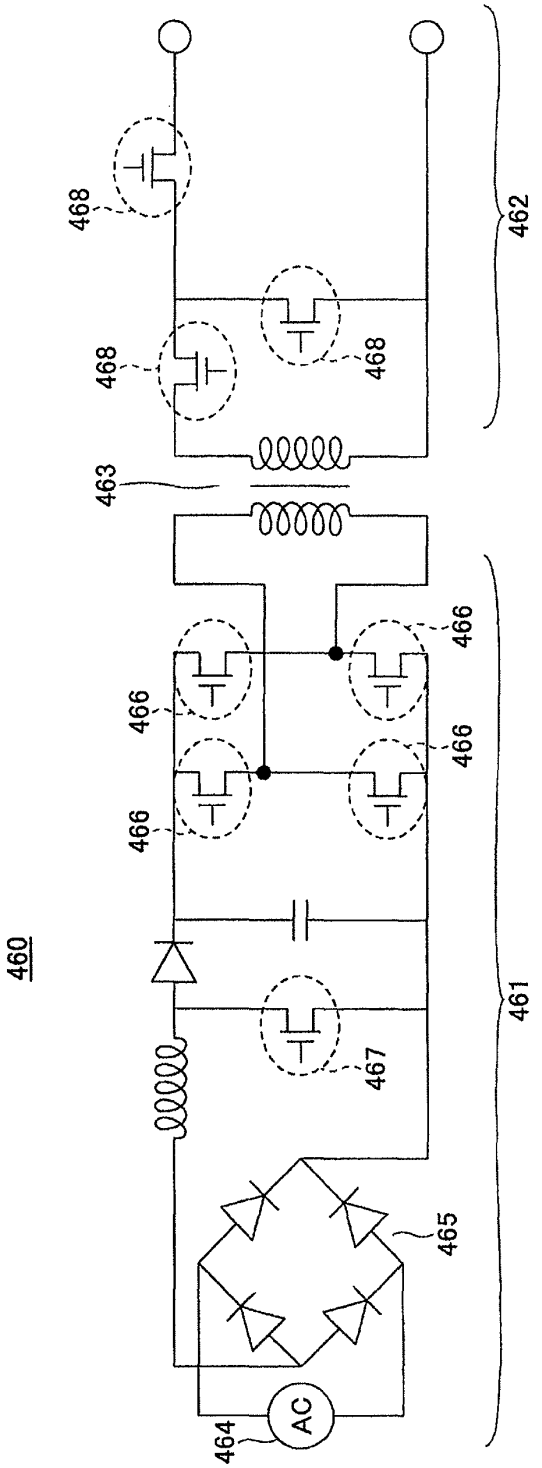
第8C圖



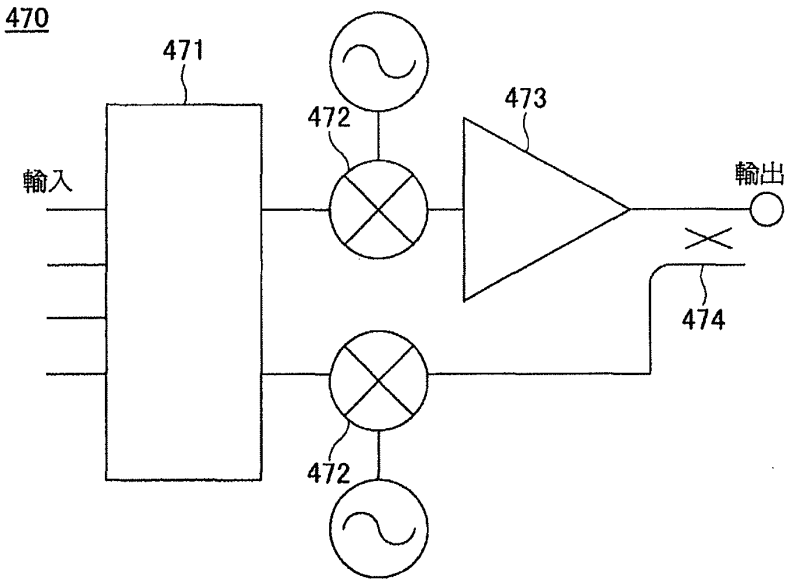
第9圖



第10圖



第11圖



第12圖

四、指定代表圖：

(一)本案指定代表圖為：第（ 1 ）圖。

(二)本代表圖之元件符號簡單說明：

911 基體
912 緩衝層
913 緩衝層
914 電子轉移層
914a 2DEG
915 電子捐獻層
921 閘極電極
922 源極電極
923 汲極電極

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

Espacenet

Bibliographic data: TW201232779 (A) — 2012-08-01

Enhancement-mode transistor and fabrication method thereof

Inventor(s): KALNITSKY ALEXANDER [US]; HSIUNG CHIH-WEN [TW]; TSAI CHUN-LIN [TW] + (KALNITSKY, ALEXANDER, ; HSIUNG, CHIH-WEN, ; TSAI, CHUN-LIN, ; HSIUNG, CHIH WEN, ; TSAI, CHUN LIN)

Applicant(s): TAIWAN SEMICONDUCTOR MFG [TW] + (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD)

Classification: - international:*H01L29/78; H01L29/80*
- cooperative: H01L21/0254; H01L21/0262; H01L29/1066; H01L29/2003; H01L29/205; H01L29/207; H01L29/42316; H01L29/66143; H01L29/66462; H01L29/7787

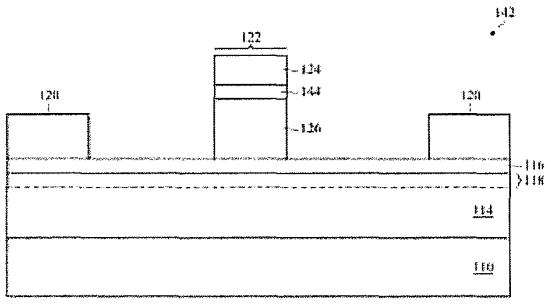
Application number: TW20110123820 20110706

Priority number (s): US201161437811P 20110131 ; US201113049699 20110316

Also published as: TWI462293 (B) US2012193637 (A1) US8895993 (B2) US2015325678 (A1) CN102623490 (A) more

Abstract of TW201232779 (A)

The present disclosure provides a semiconductor structure. The semiconductor structure includes a gallium nitride (GaN) layer on a substrate; an aluminum gallium nitride (AlGaN) layer disposed on the GaN layer; and a gate stack disposed on the AlGaN layer. The gate stack includes a III-V compound n-type doped layer; a III-V compound p-type doped layer adjacent the III-V compound n-type doped layer; and a metal layer formed over the III-V compound p-type doped layer and the III-V compound n-type doped layer.



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(12)發明說明書公開本 (11)公開編號：TW 201232779 A1
(43)公開日： 中華民國 101 (2012) 年 08 月 01 日

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(51)Int. Cl.： *H01L29/78 (2006.01)* *H01L29/80 (2006.01)*
(30)優先權：2011/01/31 美國 61/437,811
2011/03/16 美國 13/049,699
(71)申請人：台灣積體電路製造股份有限公司 (中華民國) TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD. (TW)
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(74)代理人：洪澄文；顏錦順
申請實體審查：有 申請專利範圍項數：10 項 圖式數：16 共 38 頁

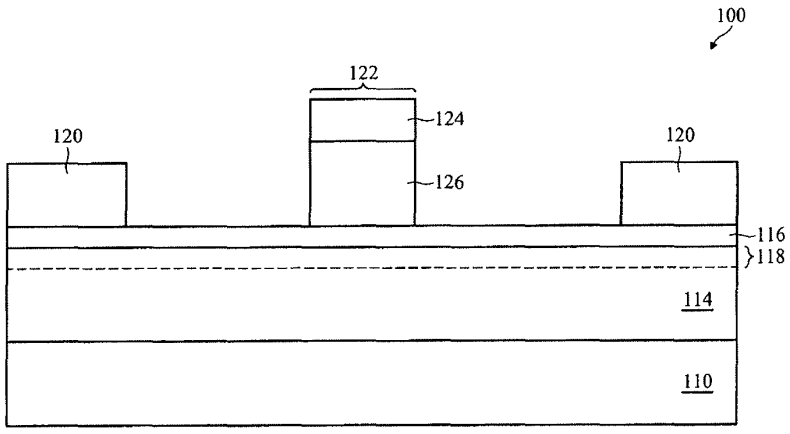
(54)名稱

增強型電晶體及其形成方法

ENHANCEMENT-MODE TRANSISTOR AND FABRICATION METHOD THEREOF

(57)摘要

本揭示提供半導體結構，包含氮化鎵(GaN)層設置在基底上，氮化鋁鎵(AlGaN)層設置在 GaN 層上，以及閘極堆疊設置在 AlGaN 層上。閘極堆疊包含 III-V 族化合物 n 型摻雜層，III-V 族化合物 p 型摻雜層鄰接 III-V 族化合物 n 型摻雜層，以及金屬層形成於 III-V 族化合物 p 型摻雜層和 III-V 族化合物 n 型摻雜層之上。



100：半導體結構
110：基底
114：緩衝層
116：阻障層
118：二維電子氣的薄層
120：源極與汲極特徵
122：閘極堆疊
124：金屬層
126：接面隔離特徵

六、發明說明：

【發明所屬之技術領域】

本發明係有關於半導體結構，特別有關於增強型電晶體及其製造方法。

【先前技術】

在半導體工業中，氮化鎵(GaN)由於其特性常被用來形成各種積體電路元件，例如高功率場效電晶體、高頻電晶體或高電子遷移率電晶體(high electron mobility transistors；HEMTs)。在一例子中，於積體電路中形成GaN增強型電晶體，當無偏壓(bias voltage)施加在對應的閘極上時，此增強型電晶體為常閉狀態。在傳統的 GaN 增強型電晶體中，閘極結構設計成具有 p 型摻雜蓋層形成於主動區上(例如可參閱美國專利公開號 US 2010/0258842)，然後在 p 型摻雜蓋層上形成金屬層，並設計成使用於偏壓。然而，當電晶體開啟時，在增強型電晶體中的這種閘極結構會承受大的閘極漏電，此大的閘極漏電將會限制電晶體的效能與安全操作範圍。因此，一種 GaN 增強型電晶體的結構及其形成方法，其能夠降低閘極漏電並克服上述問題是業界亟需的。

【發明內容】

在此所揭示的一實施例中提供半導體結構，此半導體結構包含氮化鎵(GaN)層設置在基底上，氮化鋁鎵(AlGaN)層設置在 GaN 層上，以及閘極堆疊設置在 AlGaN 層上。閘極堆疊包含 III-V 族化合物 n 型摻雜層，III-V 族化合物 p 型摻雜層鄰接 III-V 族化合物 n 型摻雜層，以

及金屬層形成於 III-V 族化合物 p 型摻雜層和 III-V 族化合物 n 型摻雜層之上。

在一實施例中，閘極堆疊更包含介電層設置在金屬層底下，且設置在 III-V 族化合物 n 型摻雜層和 III-V 族化合物 p 型摻雜層上方。在另一實施例中，閘極堆疊更包含介電層設置在金屬層、III-V 族化合物 n 型摻雜層與 III-V 族化合物 p 型摻雜層底下。半導體結構更包含另一 III-V 族化合物摻雜層，在另一實施例中，III-V 族化合物 n 型摻雜層包含 n 型 GaN 層，且 III-V 族化合物 p 型摻雜層包含 p 型 GaN 層。在另一實施例中，III-V 族化合物 n 型摻雜層以雜質進行摻雜，此雜質係選自於由矽與氧所組成的群組。在一實施例中，III-V 族化合物 p 型摻雜層以雜質進行摻雜，此雜質係選自於由鎂、鈣、鋅、鈹與碳所組成的群組。在另一實施例中，每個 III-V 族化合物 n 型摻雜層與 III-V 族化合物 p 型摻雜層的厚度範圍介於約 1nm 至約 100nm 之間，GaN 層為未摻雜或者非故意摻雜。半導體結構更包含源極和汲極特徵與 GaN 層、AlGaN 層以及閘極堆疊組合在一起，形成增強型電晶體。

在此所揭示的另一實施例中提供增強型電晶體，此增強型電晶體包含第一 III-V 族化合物層設置在基底上，第二 III-V 族化合物層直接設置在第一 III-V 族化合物層上，且第二 III-V 族化合物層的組成與第一 III-V 族化合物層不同，以及閘極堆疊設置在第二 III-V 族化合物層上，閘極堆疊包含一對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層，組合成二極體。在一實施例中，

基底包含藍寶石基底、矽基底與碳化矽基底的其中之一，第一 III-V 族化合物層包含氮化鎵(GaN)層，且第二 III-V 族化合物層包含氮化鋁鎵(AlGaN)層。在另一實施例中，閘極堆疊更包含金屬層設置於此對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層上，n 型摻雜 III-V 族化合物層包含 n 型摻雜氮化鎵(GaN)層，且 p 型摻雜 III-V 族化合物層包含 p 型摻雜氮化鎵(GaN)層。在另一實施例中，藉由實施熱退火製程，金屬層對於此對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層具有歐姆接面。在另一實施例中，閘極堆疊更包含絕緣材料層介於金屬層與此對 n 型摻雜 III-V 族化合物層和 p 型摻雜 III-V 族化合物層之間。在另一實施例中，閘極堆疊更包含絕緣材料層介於第二 III-V 族化合物層與此對 n 型摻雜 III-V 族化合物層和 p 型摻雜 III-V 族化合物層之間。此增強型電晶體更包含氮化鋁(AlN)層插入於第一與第二 III-V 族化合物層之間，此增強型電晶體更包含源極與汲極特徵，閘極堆疊插入於源極與汲極特徵之間，其中源極與汲極特徵包含金屬，其係選自於由鈦、鋁、鎳與金所組成的群組。在一實施例中，閘極堆疊更包含第三摻雜 III-V 族化合物層鄰接此對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層。

本揭示還提供形成增強型電晶體的方法，此方法包含形成第一 III-V 族化合物層在基底上，形成第二 III-V 族化合物層在第一 III-V 族化合物層上，其中第二 III-V 族化合物層與第一 III-V 族化合物層不同，形成閘極堆疊

以及形成源極與汲極特徵在第二 III-V 族化合物層上，且閘極堆疊插入於源極與汲極特徵之間。閘極堆疊的形成更包含形成二極體，其具有一對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層，以及形成金屬層在二極體上。

在此方法的各種實施例中，第一 III-V 族化合物層的形成包含形成未摻雜的氮化鎵(GaN)層，第二 III-V 族化合物層的形成包含形成氮化鋁鎵(AlGaN)層，且二極體的形成可包含形成 n 型氮化鎵(GaN)層，n 型氮化鎵(GaN)層以矽與氧的其中之一進行摻雜，以及形成 p 型氮化鎵(GaN)層，p 型氮化鎵(GaN)層以鎂、鈣、鋅、鈹與碳的其中之一進行摻雜。在另一實施例中，閘極堆疊的形成包含實施熱退火，藉此在二極體與金屬層之間形成歐姆接面。在另一實施例中，閘極堆疊的形成更包含在二極體與金屬層之間形成絕緣材料層。

為了讓本發明之上述目的、特徵、及優點能更明顯易懂，以下配合所附圖式，作詳細說明如下：

【實施方式】

以下的揭示內容提供許多不同的實施例或例子，藉此實行各種實施例的不同特徵，下述元件與排列方式的特定例子係用於簡化本揭示，這些例子僅作為示範，並非用於限定本揭示。另外，在以下揭示的各種例子中，可重複使用標號以及/或字母，這些重複的標號是用於簡化以及清楚地顯示本揭示，並非用於表示各種實施例以及/或各種狀態之間的關係。

第 1 圖顯示一實施例之具有氮化鎵(GaN)增強型電晶體的半導體結構 100 之剖面示意圖，第 2a 至 7a 圖顯示依據本揭示的各種實施例，合併在第 1 圖的半導體結構內的閘極結構之剖面示意圖，第 2b 至 7b 圖顯示依據本發明的各種實施例，分別具有第 2a 至 7a 圖的閘極結構之第 1 圖的半導體結構的示意圖。參閱第 1 圖、第 2a 至 7a 圖以及第 2b 至 7b 圖，半導體結構 100 及其形成方法描述如下。

參閱第 1 圖，半導體結構 100 包含藍寶石基底 110，此外，基底還可以是碳化矽(SiC)基底或矽基底，矽基底例如可以為(111)矽晶圓。

半導體結構 100 也包含異質接面(heterojunction)形成於兩個不同的半導體材料層之間，例如具有不同能帶隙(band gap)的材料層。例如，半導體結構 100 可包含非摻雜且相對窄的能帶隙通道層(non-doped relatively narrow-band gap channel layer)以及相對寬的能帶隙 n 型施子供給層(relatively wide-band gap n-type donor supply layer)。在一實施例中，半導體結構 100 包含第一 III-V 族化合物層(或稱為緩衝層)114 形成於基底 110 上，以及第二 III-V 族化合物層(或稱為阻障層)116 形成於緩衝層 114 上，緩衝層 114 與阻障層 116 是由週期表上第 III-V 族的元素所形成的化合物所構成，然而，緩衝層 114 與阻障層 116 彼此在組成上是不同的。鄰接阻障層 116 的緩衝層 114 為非摻雜或非故意摻雜(unintentionally doped；UID)，在本實施例的半導體結構 100 中，緩衝層

114 包含 GaN 層(也稱為 GaN 層 114)，阻障層 116 包含 AlGaN 層(也稱為 AlGaN 層 116)，GaN 層 114 與 AlGaN 層 116 彼此直接接觸，在基底 110 與緩衝層 114 之間通常存在過渡層，於第 1 圖中未繪出。

GaN 層 114 為未摻雜的型態，此外，GaN 層 114 還可以是非故意摻雜，非故意摻雜例如是因為用於形成 GaN 層 114 的前驅物所造成，使得 GaN 層 114 具有 n 型的輕摻雜。GaN 層 114 可使用含鎵的前驅物以及含氮的前驅物，藉由有機金屬氣相磊晶法(metal organic vapor phase epitaxy；MOVPE)磊晶長成，含鎵的前驅物包含三甲基鎵 (trimethylgallium ； TMG) 、三乙基鎵 (triethylgallium；TEG)或其他合適的化學品；含氮的前驅物包含氨(ammonia；NH_3)、叔丁胺(tertiarybutylamine；TBAm)、苯肼(phenyl hydrazine)或其他合適的化學品。在一例子中，GaN 層 114 的厚度範圍介於約 0.5μm 至約 10μm 之間。在另一例子中，GaN 層 114 的厚度為約 2μm。MOVPE 沈積法也稱為有機金屬化學氣相沈積法 (metal organic chemical vapor deposition；MOCVD)。

AlGaN 層 116 為非故意摻雜，此外，AlGaN 層 116 還可以具有從鄰近層導入的 n 型摻雜物，AlGaN 層 116 磊晶成長在 GaN 層 114 上，AlGaN 層 116 可使用含鋁的前驅物、含鎵的前驅物以及含氮的前驅物，藉由有機金屬氣相磊晶法(MOVPE)磊晶長成，含鋁的前驅物包含三甲基鋁 (trimethylaluminum ； TMA) 、三乙基鋁 (triethylaluminum；TEA)或其他合適的化學品；含鎵的前

驅物包含三甲基鎵(TMG)、三乙基鎵(TEG)或其他合適的化學品；含氮的前驅物包含氨(NH_3)、叔丁胺(TBAm)、苯肼(phenyl hydrazine)或其他合適的化學品。在一例子中，AlGaN 層 116 的厚度範圍介於約 5nm 至約 50nm 之間。在另一例子中，AlGaN 層 116 的厚度為約 15nm。

GaN 層 114 與 AlGaN 層 116 之間的能帶差異(band gap discontinuity)與壓電效應(piezo-electric effect)共同在 GaN 層 114 內產生具有高移動傳導電子的非常薄層 118，此非常薄層 118 稱為二維電子氣(two-dimensional electron gas；2-DEG)，其形成載子通道，二維電子氣的薄層 118 位於 AlGaN 層 116 與 GaN 層 114 的界面上。

半導體結構 100 也包含源極與汲極(S/D)特徵 120 形成於基底 110 上，並且與通道電性連接。源極與汲極(S/D)特徵 120 包含一種或一種以上的導電材料，例如 S/D 特徵 120 包含金屬，其係選自於由鈦、鋁、鎳與金所組成的群組。S/D 特徵 120 可藉由例如物理氣相沈積法(physical vapor deposition；PVD)或其他適當的技術形成，可在 S/D 特徵 120 上施加熱退火製程，使得 S/D 特徵 120 與 AlGaN 層 116 反應形成合金，藉此從 S/D 特徵 120 至通道產生有效的電性連接。在一例子中，熱退火使用快速熱退火(rapid thermal annealing；RTA)的設備與製程。

閘極堆疊 122 形成於阻障層 116 上，並且插入於源極與汲極(S/D)特徵 120 之間，閘極堆疊 122 包含導電材料層，例如金屬層 124，金屬層 124 作為閘極電極，其係

用於偏壓且與通道電性耦接。在各種例子中，金屬層 124 包含鎳或金。如果閘極堆疊 122 的金屬層設置成與 AlGaN 層 116 直接接觸，其形成的蕭特基二極體(Schottky diode)閘極會產生空乏型元件(depletion mode device)。

閘極堆疊 122 包含接面隔離特徵 126 設置在金屬層 124 底下，接面隔離特徵 126 包含至少一個 n 型摻雜半導體層與一個 p 型摻雜半導體層，兩者組合成二極體。在本實施例中，此至少一個 n 型摻雜半導體層與至少一個 p 型摻雜半導體層分別為 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層。更進一步地，本實施例之 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層分別為 n 型摻雜 GaN 層(或 n-GaN 層)與 p 型摻雜 GaN 層(或 p-GaN 層)，在閘極堆疊中的二極體提供接面隔離效果。

此外，接面隔離特徵 126 可以更包含另一 n 型摻雜 GaN 層、另一 p 型摻雜 GaN 層或兩者皆包含。每對鄰接的 n-GaN 層與 p-GaN 層之間會形成接面(或二極體)，在 n-GaN 層與 p-GaN 層之間的各種二極體配置成電性串連的狀態，這些二極體不僅在閘極電極與通道之間提供閘極漏電降低的隔離效果，並且在預期中也改善了元件的切換速度，其說明如下。由於各種二極體以串連方式耦接在一起，其對應的接面電容器也同樣地以串連方式耦接在一起，因此，串連在一起的接面電容器之總電容值將小於它們之中的任何一個，因此，元件切換速度會因為電容值的降低而改善。

在一實施例中，金屬層與二極體之間的界面為藉由

熱退火形成的歐姆接面，退火的溫度範圍介於約 800℃至約 900℃之間。在另一實施例中，金屬層與二極體之間的界面為蕭特基接面(Schottky contact)，在此例子中，形成閘極堆疊的製程沒有熱退火步驟。

在本實施例中，閘極堆疊 122、S/D 特徵 120 以及在緩衝層 114 中的 2-DEG 通道組合成增強型(E-mode)電晶體，當正電壓施加在閘極堆疊上產生足夠大的正向偏壓時，增強型電晶體被開啟，此種配置的電晶體也稱為增強型高電子遷移率電晶體(E-mode high electron mobility transistor；HEMT)。

第 2a 至 7a 圖顯示依據本揭示的各種概念所建構的半導體結構 100 之閘極堆疊 122 的各種實施例，在第 2a 圖所示的一實施例中，閘極堆疊 122 的接面隔離特徵 126 包含 p-GaN 層 130，以及 n-GaN 層 132 設置在 p-GaN 層 130 上，p-GaN 層 130 以 p 型摻雜物進行摻雜，例如為鎂、鈣、鋅、鈹、碳或前述之組合。在一實施例中，p-GaN 層 130 可藉由 MOCVD 或其他合適的技術形成。在另一實施例中，p-GaN 層 130 的厚度範圍介於約 1nm 至約 100nm 之間。n-GaN 層 132 以 n 型摻雜物進行摻雜，例如為矽、氧或前述之組合。在一實施例中，n-GaN 層 132 可藉由 MOCVD 或其他合適的技術形成。在另一實施例中，n-GaN 層 132 的厚度範圍介於約 1nm 至約 100nm 之間。

第 2b 圖顯示具有第 2a 圖的閘極堆疊 122 之半導體結構 100 的增強型電晶體之示意圖，在第 2b 圖

中，"G"、"S"以及"D"分別代表閘極、源極與汲極，在源極與汲極之間定義出 2-DEG 通道，二極體 138a 形成於 p-GaN 層 130 與具有 n 型摻雜物的阻障層 116 之間，第二個二極體 138b 形成於 p-GaN 層 130 與 n-GaN 層 132 之間，二極體 138a 與 138b 串連在一起，當元件切換速度增加的同時，從二極體 138a 和 138b 所產生的電容值也隨之降低。

在第 3a 圖所示之另一實施例中，閘極堆疊 122 的接面隔離特徵 126 與第 2a 圖的接面隔離特徵 126 相似，但更包含額外的 p-GaN 層 134 設置在 n-GaN 層 132 上，此額外的 p-GaN 層 134 與 n-GaN 層 132 形成另一二極體，提供額外的隔離效果。額外的 p-GaN 層 134 與 p-GaN 層 130 的組成及形成方式相似，例如 p-GaN 層 134 以 p 型摻雜物進行摻雜，p 型摻雜物例如為鎂、鈣、鋅、鈹、碳或前述之組合。

第 3b 圖顯示具有第 3a 圖的閘極堆疊 122 之半導體結構 100 的增強型電晶體之示意圖，符號"G"、"S"以及"D"分別代表閘極、源極與汲極，在源極與汲極之間定義出 2-DEG 通道，二極體 138a 形成於 p-GaN 層 130 與具有 n 型摻雜物的阻障層 116 之間，第二個二極體 138b 形成於 p-GaN 層 130 與 n-GaN 層 132 之間，第三個二極體 138c 形成於 n-GaN 層 132 與 p-GaN 層 134 之間，二極體 138a、138b 及 138c 串連在一起，當元件切換速度進一步增加的同時，從這些二極體的通道與閘極電極之間所產生的電容值也進一步降低。

在第 4a 圖所示之另一實施例中，閘極堆疊 122 的接面隔離特徵 126 與第 2a 圖的接面隔離特徵 126 相似，但更包含額外的 p-GaN 層 134 設置在 n-GaN 層 132 上，以及額外的 n-GaN 層 136 設置在 p-GaN 層 134 上。此額外的 p-GaN 層 134 和額外的 n-GaN 層 136 分別與 p-GaN 層 130 和 n-GaN 層 132 的組成及形成方式相似，例如 n-GaN 層 136 以 n 型摻雜物進行摻雜，n 型摻雜物例如為矽或氧。

第 4b 圖顯示具有第 4a 圖的閘極堆疊 122 之半導體結構 100 的增強型電晶體之示意圖，符號"G"、"S"以及"D"分別代表閘極、源極與汲極，在源極與汲極之間定義出 2-DEG 通道，二極體 138a 形成於 p-GaN 層 130 與具有 n 型摻雜物的阻障層 116 之間，第二個二極體 138b 形成於 p-GaN 層 130 與 n-GaN 層 132 之間，第三個二極體 138c 形成於 n-GaN 層 132 與 p-GaN 層 134 之間，第四個二極體 138c 形成於 p-GaN 層 134 與 n-GaN 層 136 之間，二極體 138a、138b、138c 和 138d 串連在一起，當元件切換速度藉此而進一步增加的同時，從這些二極體的通道與閘極電極之間所產生的電容值也進一步降低。

在第 5a 圖所示之一實施例中，閘極堆疊 122 的接面隔離特徵 126 包含 n-GaN 層 132，以及 p-GaN 層 130 設置在 n-GaN 層 132 上。第 5a 圖的閘極堆疊 122 與第 2a 圖的閘極堆疊 122 相似，但其中 p-GaN 層 130 和 n-GaN 層 132 的配置方式不同。p-GaN 層 130 以 p 型摻雜物進行摻雜，p 型摻雜物例如為鎂、鈣、鋅、鈹、碳或前述之組合。在一實施例中，p-GaN 層 130 可藉由 MOCVD 或

其他合適的技術形成。在另一實施例中，p-GaN 層 130 的厚度範圍介於約 1nm 至約 100nm 之間。n-GaN 層 132 以 n 型摻雜物進行摻雜，n 型摻雜物例如為矽、氧或前述之組合。在一實施例中，n-GaN 層 132 可藉由 MOCVD 或其他合適的技術形成，在另一實施例中，n-GaN 層 132 的厚度範圍介於約 1nm 至約 100nm 之間。

第 5b 圖顯示具有第 5a 圖的閘極堆疊 122 之半導體結構 100 的增強型電晶體之示意圖，二極體 138e 形成於 p-GaN 層 130 與 n-GaN 層 132 之間，其產生隔離效果，避免閘極漏電發生。

在第 6a 圖所示之另一實施例中，閘極堆疊 122 的接面隔離特徵 126 與第 3a 圖的接面隔離特徵 126 相似，但具有不同的配置方式，特別是 n-GaN 層 132 設置在阻障層 116 上，p-GaN 層 130 設置在 n-GaN 層 132 上，額外的 n-GaN 層 136 設置在 p-GaN 層 130 上。

第 6b 圖顯示具有第 6a 圖的閘極堆疊 122 之半導體結構 100 的增強型電晶體之示意圖，一個二極體 138e 形成於 p-GaN 層 130 與 n-GaN 層 132 之間，另一個二極體 138f 形成於 p-GaN 層 130 與 n-GaN 層 136 之間，二極體 138e 及 138f 串連在一起，這些二極體的通道與閘極電極之間所產生的電容提供隔離效果，避免閘極漏電發生，並且更進一步地提升元件的切換速度。

在第 7a 圖所示之另一實施例中，閘極堆疊 122 的接面隔離特徵 126 與第 4a 圖的接面隔離特徵 126 相似，但配置方式不同。第 7a 圖的閘極堆疊 122 包含 n-GaN 層

132 設置在阻障層 116 上，p-GaN 層 130 設置在 n-GaN 層 132 上，額外的 n-GaN 層 136 設置在 p-GaN 層 130 上，以及額外的 p-GaN 層 134 設置在額外的 n-GaN 層 136 上。每個 n-GaN 層與 p-GaN 層的組成及形成方式與第 4a 圖的閘極堆疊 122 中相對應的層相似，例如 n-GaN 層 136 以 n 型摻雜物進行摻雜，n 型摻雜物例如為矽或氧。

第 7b 圖顯示具有第 7a 圖的閘極堆疊 122 之半導體結構 100 的增強型電晶體之示意圖，符號"G"、"S"以及"D"分別代表閘極、源極與汲極，在源極與汲極之間定義出 2-DEG 通道，二極體 138e 形成於 n-GaN 層 132 與 p-GaN 層 130 之間，第二個二極體 138f 形成於 p-GaN 層 130 與額外的 n-GaN 層 136 之間，第三個二極體 138g 形成於 n-GaN 層 136 與額外的 p-GaN 層 134 之間，二極體 138e、138f 和 138g 串連在一起，當元件切換速度藉此而進一步增加的同時，從這些二極體的通道與閘極電極之間所產生的電容值也隨之降低。

在不同實施例中也可存在其他優點，例如對應的增強型電晶體的臨界電壓可藉由改變 n-p 二極體的摻雜以及/或厚度而調整。

第 8 圖顯示依據一個或一個以上的其他實施例，具有氮化鎵(GaN)增強型電晶體的半導體結構 140 之剖面示意圖，參閱第 8 圖、第 2a 至 7a 圖以及第 2b 至 7b 圖，半導體結構 140 以及其形成方法描述如下。

半導體結構 140 與第 1 圖的半導體結構 100 相似，但更包含介電材料層(或絕緣層)141 形成於阻障層 116

上，且介電材料層 141 設置在源極與汲極特徵 120 之間，此外，介電材料層 141 還形成於阻障層 116 與閘極堆疊 122 之間。介電材料層 141 包含介電材料，依據各種實施例，介電材料係選自於由氧化矽(silicon oxide；SiO_2)、氮化矽(silicon nitride；Si_3N_4)、氧化鋁(aluminum oxide；Al_2O_3)、氧化鉭(tantalum oxide；Ta_2O_5)、氧化鈦(titanium oxide；TiO_2)、氧化鋅(zinc oxide；ZnO_2)、氧化鉿(hafnium oxide；HfO_2)或前述之組合所組成的群組。在一實施例中，介電材料層 141 的厚度範圍介於約 3nm 至約 100nm 之間，介電材料層 141 可藉由任何適當的製造技術形成，例如 MOCVD、化學氣相沈積法(CVD)、物理氣相沈積法(PVD)、原子層沈積法(atomic layer deposition；ALD)或熱氧化法。介電材料層 141 提供更進一步的隔離效果，避免閘極漏電發生，並且更進一步地改善元件的切換速度。

閘極堆疊 122 與第 1 圖的閘極堆疊 122 相似，例如閘極堆疊 122 包含接面隔離特徵 126 設置在介電材料層 141 上，以及金屬層 124 設置在接面隔離特徵 126 上。此外，閘極堆疊 122 可具有依據第 2a 至 7a 圖所示之各種實施例的結構中的一種。

第 9 圖顯示具有氮化鎵(GaN)增強型電晶體的半導體結構 142 之一實施例的剖面示意圖，第 10 至 15 圖顯示依據本揭示的各種實施例，合併在第 9 圖的半導體結構內的閘極結構之剖面示意圖。參閱第 9 圖與第 10 至 15 圖，半導體結構 142 及其形成方法描述如下。

半導體結構 142 與第 1 圖的半導體結構 100 相似，但是閘極堆疊 122 更包含介電材料層(或絕緣層)144 設置在金屬層 124 與接面隔離特徵 126 之間，介電材料層 144 包含介電材料，依據各種實施例，介電材料係選自於由 SiO_2、Si_3N_4、Al_2O_3、Ta_2O_5、TiO_2、ZnO_2、HfO_2 或前述之組合所組成的群組。在一實施例中，介電材料層 144 的厚度範圍介於約 3nm 至約 100nm 之間，介電材料層 141 可藉由任何適當的製造技術形成，例如 MOCVD、CVD、PVD、ALD 或熱氧化法。介電材料層 144 提供更進一步的隔離，避免閘極漏電發生，並且更進一步地改善元件的切換速度。

第 10 至 15 圖顯示依據本揭示的各種概念，建構在半導體結構 142 的閘極堆疊 122 之各種實施例。在第 10 圖所示之一實施例中，閘極堆疊 122 與第 2a 圖的閘極堆疊 122 相似，但更包含介電材料層 144 設置在接面隔離特徵 126 與金屬層 124 之間，閘極堆疊 122 的接面隔離特徵 126 包含 p-GaN 層 130，以及 n-GaN 層 132 設置在 p-GaN 層 130 上，p-GaN 層 130 以 p 型摻雜物進行摻雜，p 型摻雜物例如為鎂、鈣、鋅、鈹、碳或前述之組合。在一實施例中，p-GaN 層 130 可藉由 MOCVD 或其他合適的技術形成。在另一實施例中，p-GaN 層 130 的厚度範圍介於約 1nm 至約 100nm 之間。n-GaN 層 132 以 n 型摻雜物進行摻雜，n 型摻雜物例如為矽、氧或前述之組合。在一實施例中，n-GaN 層 132 可藉由 MOCVD 或其他合適的技術形成。在另一實施例中，n-GaN 層 132 的厚度

範圍介於約 1nm 至約 100nm 之間。閘極堆疊 122 更包含介電材料層 144 設置在接面隔離特徵 126 上，以及金屬層 124 設置在介電材料層 144 上。

在第 11 圖所示之一實施例中，閘極堆疊 122 與第 3a 圖的閘極堆疊 122 相似，但更包含介電材料層 144 設置在接面隔離特徵 126 與金屬層 124 之間。

在第 12 至 15 圖所示之其他實施例中，閘極堆疊 122 分別與第 4a 至 7a 圖的閘極堆疊 122 相似，但更包含介電材料層 144 設置在接面隔離特徵 126 與金屬層 124 之間。在不同實施例中也可存在各種優點，這些優點包含避免閘極漏電、提升元件切換速度，以及藉由改變 n-p 二極體的摻雜以及/或厚度而調整相對應的增強型電晶體之臨界電壓。

第 16 圖顯示閘極漏電特性數據對閘極電壓的圖表，閘極漏電特性數據來自模擬結果，並且以閘極電流對閘極電壓的曲線表示。標式為"n/p-GaN 結構"的曲線對應至具有半導體結構 100、140 與 142 其中之一的 GaN 增強型電晶體的一例子之閘極漏電數據，標式為"p-GaN 結構"的曲線用來表示參考值，並且對應至只包含 p 型摻雜蓋層以及金屬層設置在其閘極堆疊中的 GaN 結構的一例子所模擬得到的閘極漏電數據。如圖所示，"n/p-GaN 結構"的閘極漏電電流大抵上會降低，並且其元件效能因此而改善。

雖然在本揭示中提供並說明各種實施例，在不脫離本揭示的精神下，也可使用其他選擇及實施例，例如，

半導體結構 100(或 140 或 142)的增強型電晶體可進一步包含氮化鋁(AlN)層設置在緩衝層 114 與阻障層 116 之間，在一實施例中，AlN 層選擇性地磊晶成長在緩衝層 114 上，AlN 層可使用含鋁的前驅物與含氮的前驅物，藉由有機金屬氣相磊晶法(MOVPE)磊晶成長，含鋁的前驅物包含三甲基鋁(TMA)、三乙基鋁(TEA)或其他合適的化學品；含氮的前驅物包含氨(NH_3)、叔丁胺(TBAm)、苯肼(phenyl hydrazine)或其他合適的化學品。在一例子中，AlN 層的厚度範圍介於約 5nm 至約 50nm 之間。

此外，AlN 層可以取代 AlGaN 層作為阻障層，在另一實施例中，各種 n-GaN 與 p-GaN 層的尺寸可依據元件的規格、效能以及電路需求而改變，例如，各種 n-GaN 與 p-GaN 層的厚度可依據臨界電壓或其他元件/電路的考量而調整。在另一實施例中，半導體結構 100(或 140 或 142)的閘極堆疊 122 可包含更多的 n-GaN 以及/或 p-GaN 層配置在接面隔離特徵 126 中。

雖然本發明已揭露實施例如上，然其並非用以限定本發明，在此技術領域中具有通常知識者當可瞭解，在不脫離本發明之精神和範圍內，當可做些許更動與潤飾。因此，本發明之保護範圍當視後附之申請專利範圍所界定為準。

【圖式簡單說明】

第 1 圖係顯示依據本發明之一實施例，具有氮化鎵(GaN)增強型電晶體的半導體結構之剖面示意圖。

第 2a 至 7a 圖係顯示依據本發明之各種實施例，在

第 1 圖的半導體結構內的閘極結構之剖面示意圖。

第 2b 至 7b 圖係顯示依據本發明之各種實施例，分別具有第 2a 至 7a 圖之閘極堆疊的第 1 圖之半導體結構的示意圖。

第 8 圖係顯示依據本發明之另一實施例，具有氮化鎵(GaN)增強型電晶體的半導體結構之剖面示意圖。

第 9 圖係顯示依據本發明之另一實施例，具有氮化鎵(GaN)增強型電晶體的半導體結構之剖面示意圖。

第 10 至 15 圖係顯示依據本發明之各種實施例，在第 9 圖的半導體結構內的閘極結構之剖面示意圖。

第 16 圖係顯示氮化鎵(GaN)增強型電晶體的閘極漏電特性數據的圖表。

【主要元件符號說明】

100、140、142～半導體結構；

110～基底；　　114～緩衝層；

116～阻障層；　　118～二維電子氣的薄層；

120～源極與汲極特徵；122～閘極堆疊；

124～金屬層；　　126～接面隔離特徵；

130、134～p-GaN 層；　132、136～n-GaN 層；

138a、138b、138c、138d、138e、138f、138g～二極體；

141、144～介電材料層。

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※申請案號：100123820

※申請日：　　※IPC 分類：H01L 29/778 (2006.01) H01L 29/80 (2006.01)

一、發明名稱：（中文/英文）

增強型電晶體及其形成方法

Enhancement-mode transistor and fabrication method thereof

二、中文發明摘要：

本揭示提供半導體結構，包含氮化鎵(GaN)層設置在基底上，氮化鋁鎵(AlGaN)層設置在 GaN 層上，以及閘極堆疊設置在 AlGaN 層上。閘極堆疊包含 III-V 族化合物 n 型摻雜層，III-V 族化合物 p 型摻雜層鄰接 III-V 族化合物 n 型摻雜層，以及金屬層形成於 III-V 族化合物 p 型摻雜層和 III-V 族化合物 n 型摻雜層之上。

三、英文發明摘要：

The present disclosure provides a semiconductor structure. The semiconductor structure includes a gallium nitride (GaN) layer on a substrate; an aluminum gallium nitride (AlGaN) layer disposed on the GaN layer; and a gate stack disposed on the AlGaN layer. The gate stack includes a III-V compound n-type doped layer; a III-V compound p-type doped layer adjacent the III-V compound n-type doped layer;

and a metal layer formed over the III-V compound p-type doped layer and the III-V compound n-type doped layer.

四、指定代表圖：

(一)本案指定代表圖為：第（1）圖。

(二)本代表圖之元件符號簡單說明：

100～半導體結構；

110～基底；

114～緩衝層；

116～阻障層；

118～二維電子氣的薄層；

120～源極與汲極特徵；

122～閘極堆疊；

124～金屬層；

126～接面隔離特徵。

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

七、申請專利範圍：

1.一種增強型電晶體，包括：

一第一 III-V 族化合物層，設置在一基底上；

一第二 III-V 族化合物層，直接設置在該第一 III-V 族化合物層上，且該第二 III-V 族化合物層的組成與該第一 III-V 族化合物層不同；以及

一閘極堆疊，設置在該第二 III-V 族化合物層上，其中該閘極堆疊包含一對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層組合成一二極體。

2.如申請專利範圍第 1 項所述之增強型電晶體，其中：

該基底包含一藍寶石基底、一矽基底與一碳化矽基底的其中之一；

該第一 III-V 族化合物層包含氮化鎵(GaN)層，其中該氮化鎵層為未摻雜或非故意摻雜；以及

該第二 III-V 族化合物層包含氮化鋁鎵(AlGaN)層。

3.如申請專利範圍第 2 項所述之增強型電晶體，其中該閘極堆疊更包含一金屬層設置於該對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層上；

該 n 型摻雜 III-V 族化合物層包含一 n 型摻雜氮化鎵(GaN)層；以及

該 p 型摻雜 III-V 族化合物層包含一 p 型摻雜氮化鎵(GaN)層。

4.如申請專利範圍第 3 項所述之增強型電晶體，其中該閘極堆疊更包含一絕緣材料層介於該金屬層或該第

二 III-V 族化合物層與該對 n 型摻雜 III-V 族化合物層和 p 型摻雜 III-V 族化合物層之間。

5.如申請專利範圍第 1 項所述之增強型電晶體，更包括氮化鋁(AlN)層插入於該第一與該第二 III-V 族化合物層之間。

6.如申請專利範圍第 1 項所述之增強型電晶體，更包括一源極與汲極特徵，該閘極堆疊插入於該源極與汲極特徵之間，其中該源極與汲極特徵包含一金屬，其係選自於由鈦、鋁、鎳與金所組成的群組。

7.如申請專利範圍第 1 項所述之增強型電晶體，其中該閘極堆疊更包含一第三摻雜 III-V 族化合物層鄰接該對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層。

8.一種形成增強型電晶體的方法，包括：

形成一第一 III-V 族化合物層在一基底上；

形成一第二 III-V 族化合物層在該第一 III-V 族化合物層上，其中該第二 III-V 族化合物層與該第一 III-V 族化合物層不同；

形成一閘極堆疊，包含：

形成一二極體，具有一對 n 型摻雜 III-V 族化合物層與 p 型摻雜 III-V 族化合物層；

形成一金屬層在該二極體上；以及

形成一源極與汲極特徵在該第二 III-V 族化合物層上，且該閘極堆疊插入該源極與汲極特徵之間。

9.如申請專利範圍第 8 項所述之形成增強型電晶體

的方法，其中：

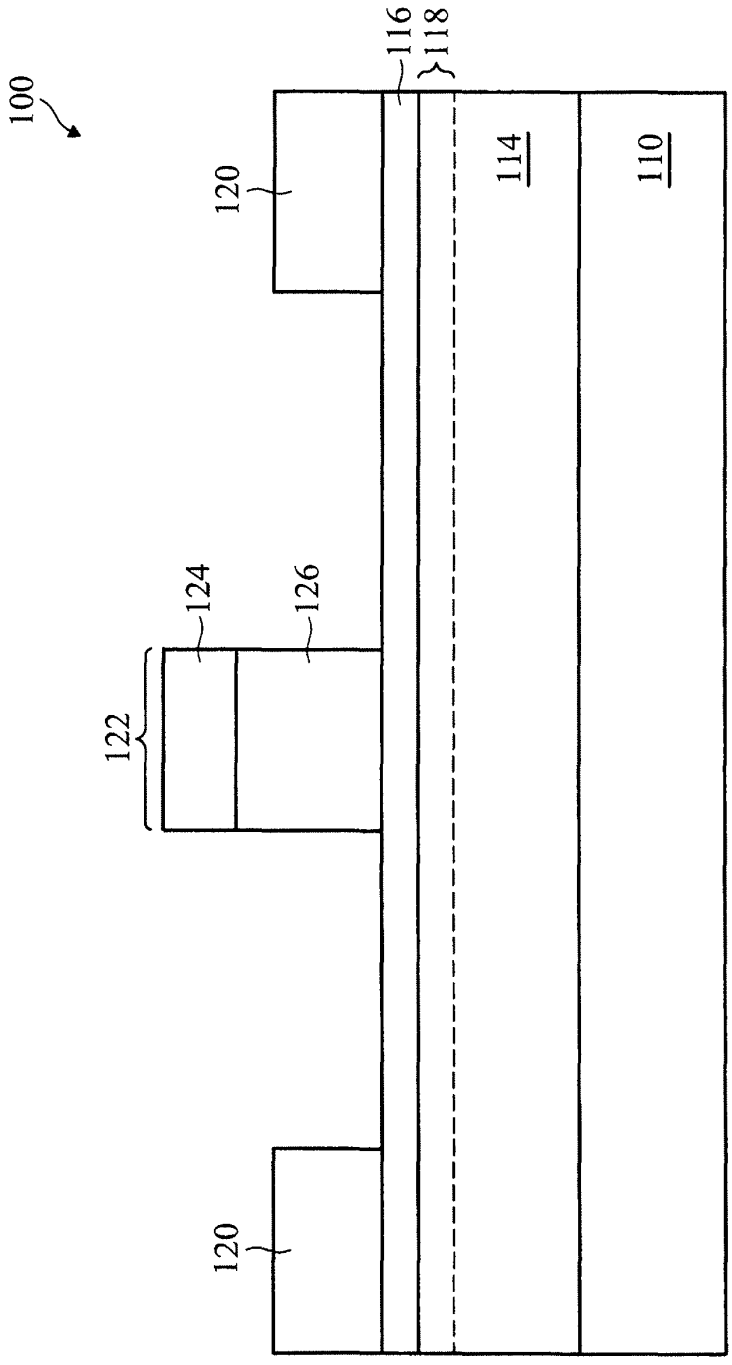
形成該第一III-V族化合物層的該步驟包含形成一未摻雜的氮化鎵(GaN)層；

形成該第二III-V族化合物層的該步驟包含形成氮化鋁鎵(AlGaN)層；以及

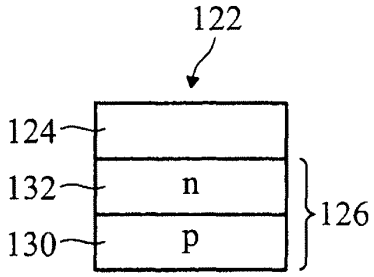
形成該二極體的該步驟包含形成一n型氮化鎵(GaN)層，該n型氮化鎵(GaN)層以矽與氧的其中之一進行摻雜，以及形成一p型氮化鎵(GaN)層，該p型氮化鎵(GaN)層以鎂、鈣、鋅、鈹與碳的其中之一進行摻雜。

10.如申請專利範圍第8項所述之形成增強型電晶體的方法，其中形成該閘極堆疊的該步驟包含實施一熱退火，在該二極體與該金屬層之間形成一歐姆接面。

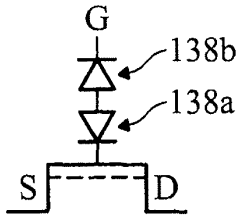
八、圖式：



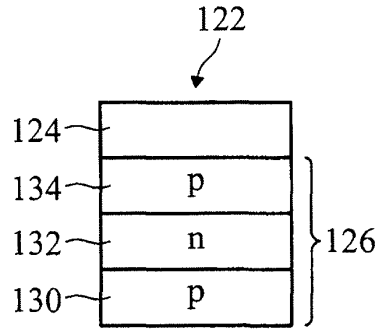
第 1 圖



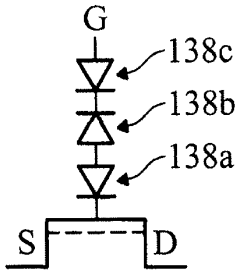
第 2a 圖



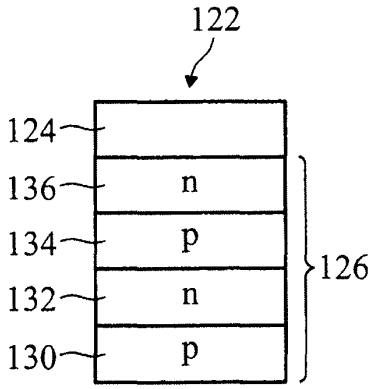
第 2b 圖



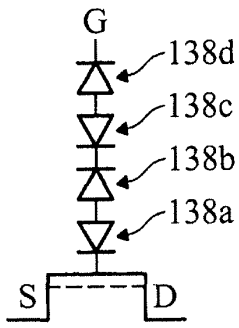
第 3a 圖



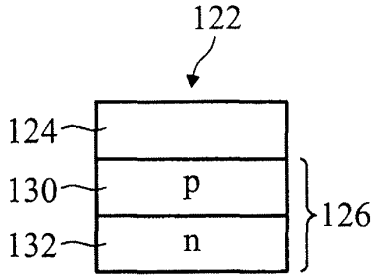
第 3b 圖



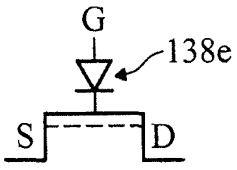
第 4a 圖



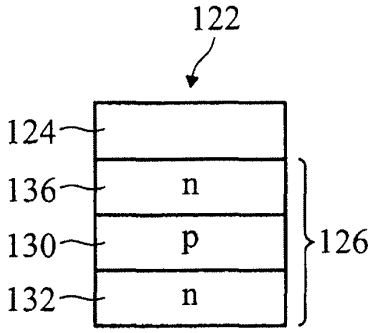
第 4b 圖



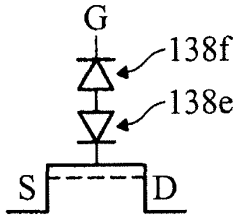
第 5a 圖



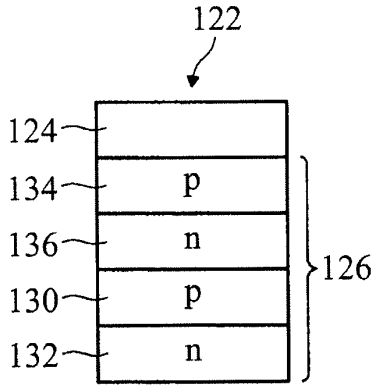
第 5b 圖



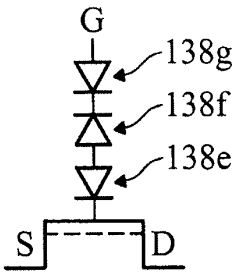
第 6a 圖



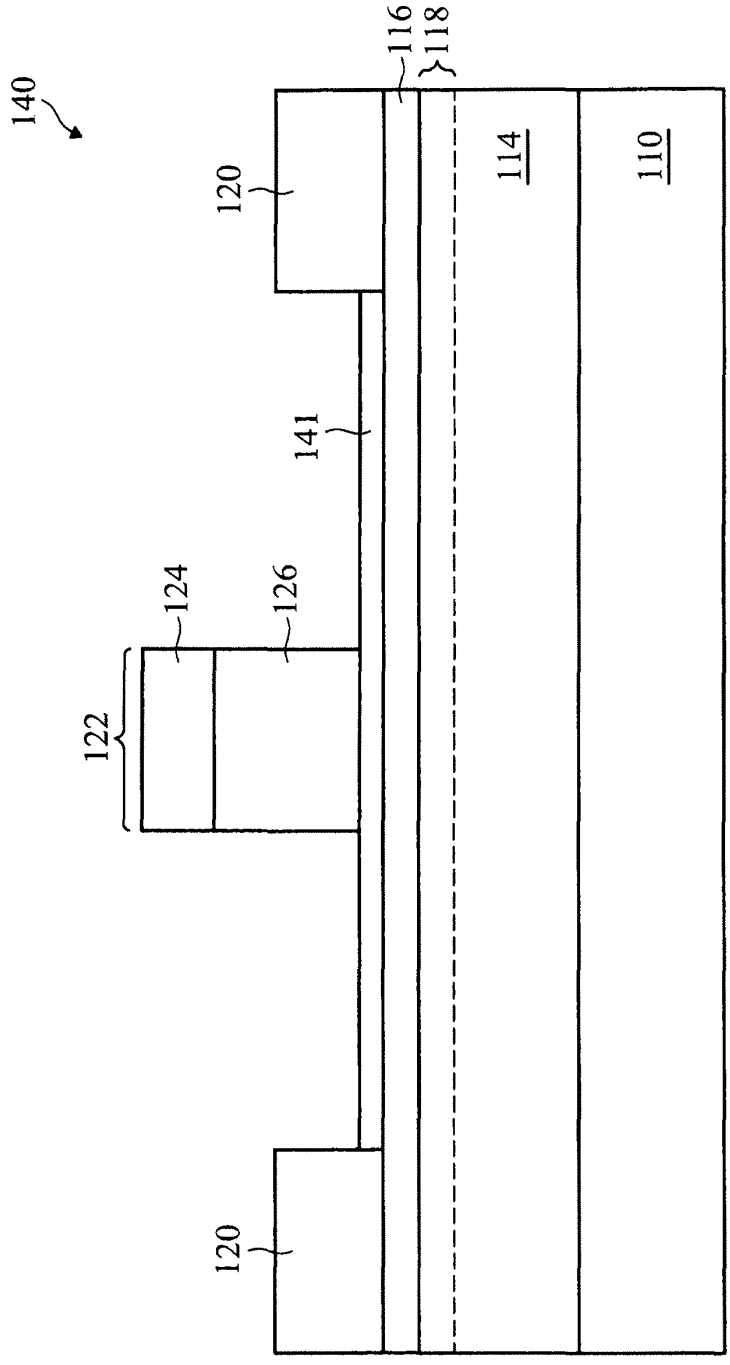
第 6b 圖



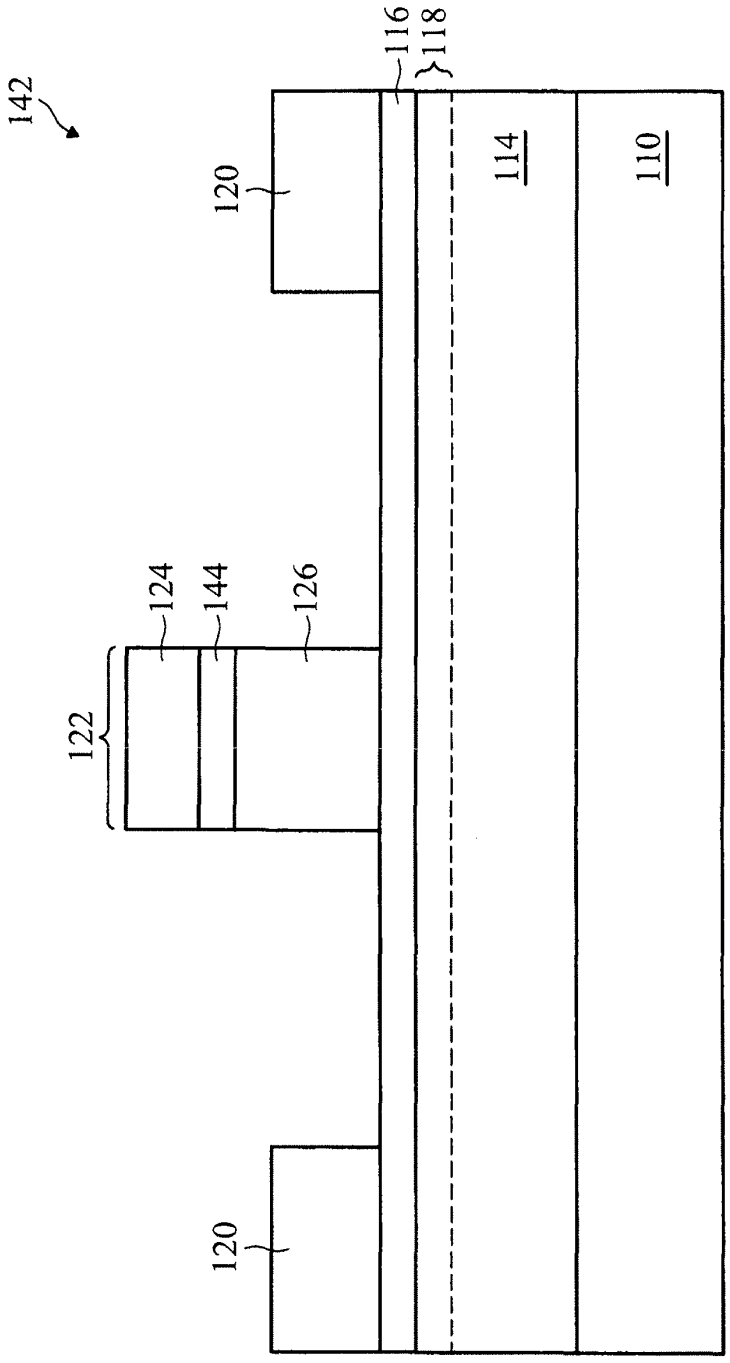
第 7a 圖



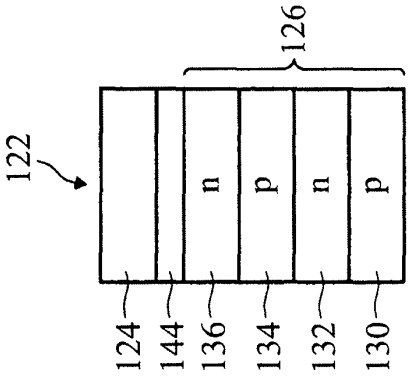
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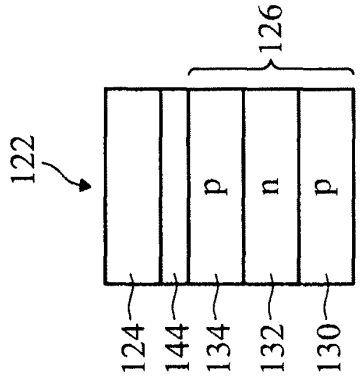
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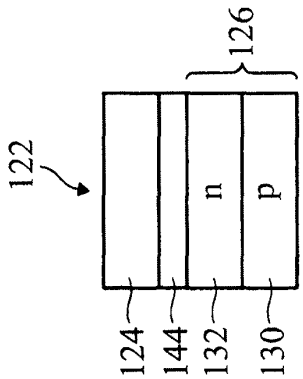
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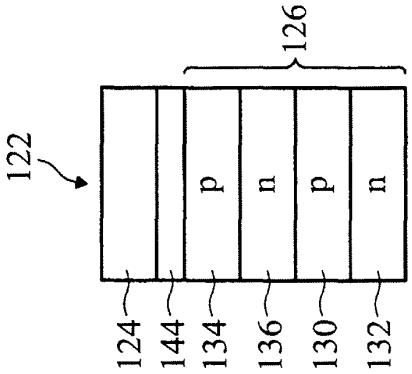
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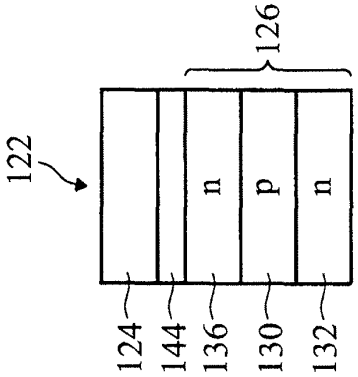
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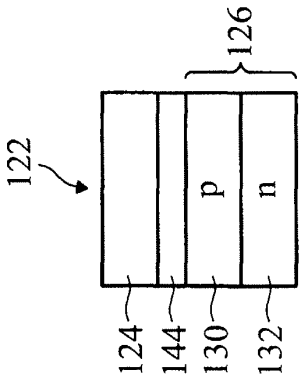
第 10 圖



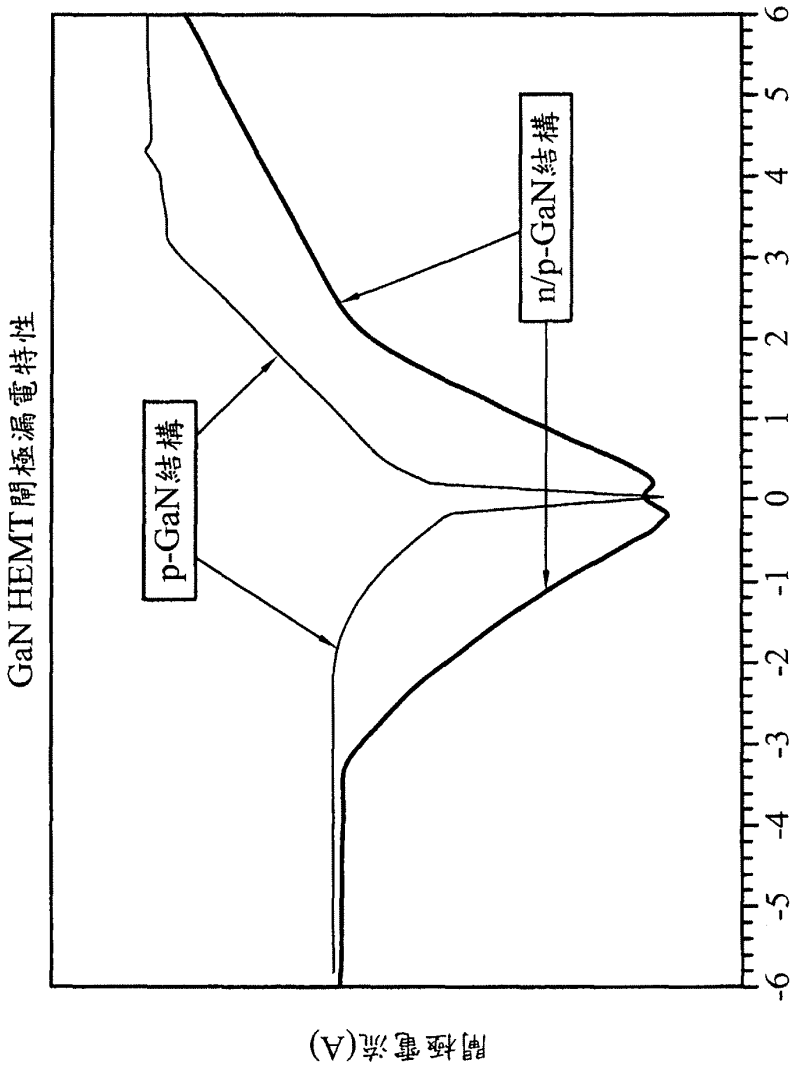
第 15 圖



第 14 圖



第 13 圖



第 16 圖

and a metal layer formed over the III-V compound p-type doped layer and the III-V compound n-type doped layer.

四、指定代表圖：

(一)本案指定代表圖為：第（1）圖。

(二)本代表圖之元件符號簡單說明：

100～半導體結構；

110～基底；

114～緩衝層；

116～阻障層；

118～二維電子氣的薄層；

120～源極與汲極特徵；

122～閘極堆疊；

124～金屬層；

126～接面隔離特徵。

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

Electronic Acknowledgement Receipt	
EFS ID:	25036077
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Lakisha Powell
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	26-FEB-2016
Filing Date:	30-JUL-2014
Time Stamp:	15:32:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		E0101-0032-IDS.pdf	3807532 6f3996ea4e44297fe490aca2ddff66fb072eb eb3	yes	97

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	3
	Other Reference-Patent/App/Search documents	4	12
	Foreign Reference	13	58
	Foreign Reference	59	97
Warnings:			
Information:			
	Total Files Size (in bytes):	3807532	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: E0101.0032
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Provisional Application of:
Jianjun Cao

Application No.: 14/447,069 | Confirmation No.: 7150

Filed: 7/30/2014 | Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GAN TRANSISTORS | Examiner: Niesz, Jamie C

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

Pursuant to 37 C.F.R. § 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed more than three months after the U.S. filing date, OR more than three months after the date of entry of the national stage of a PCT application, AND after the mailing date of the first Office Action on the merits, whichever occurs first, but before the mailing date of any of a Final Office Action, a Notice of Allowance (37 C.F.R. § 1.97(c)) or an action that otherwise closes prosecution in the application.

The references listed on the attached PTO/SB/08 form were cited in the Taiwanese Search issued December 11, 2015, in connection with corresponding Taiwanese application No.

103125846. U.S. references 2010/0258843 A1 and 6,730,552 were disclosed in an IDS filed on January 23, 2015, and are not listed on the PTO/SB/08 form.

Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

A summary/abstract translation of the non-English language references is enclosed.

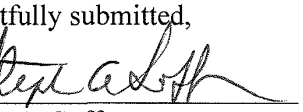
In accordance with 37 C.F.R. § 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98 and the Examiner is respectfully requested to consider the listed references.

Dated: February 25, 2016

Respectfully submitted,

By 

Stephen A. Soffen
Registration No.: 31,063
BLANK ROME LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US

CONFIRMATION NO. 7150

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

PUBLICATION NOTICE

OC000000080338773

Title:GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

Publication No.US-2016-0035847-A1
Publication Date:02/04/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 12/18/2015

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
NIESZ, JAMIE C	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
12/18/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing-DC@dicksteinshapiro.com

Office Action Summary	Application No. 14/447,069	Applicant(s) CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9 October 2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-16* is/are pending in the application.

5a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *12-16* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *30 July 2014* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *1/23/2015*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Election filed October 9, 2015.

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

3. Claims 1-11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on October 9, 2015.

Claim Objections

4. Claims 15 and 16 are objected to because of the following informalities:

5. Claim 15 recites “the source contact and drain contact” in the second and third lines of the claim. This limitation, however, lacks antecedent basis. Accordingly, claim 15 will instead be interpreted as dependent on claim 14.

6. Claim 16 recites “the pair of horizontal ledges” in the first line of the claim. This limitation, however, lacks antecedent basis and will instead be interpreted as "the pair of ledges."

7. Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

9. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

10. **Claims 12-16** are rejected under 35 U.S.C. 103 as being unpatentable over Lidow et al. (U.S. Patent Pub. No. 2010/0258843) in view of Park (U.S. Patent Pub. No. 2004/0119110).

11. Regarding **claim 12**, Lidow discloses a method for manufacturing an enhancement-mode GaN transistor (Fig. 10), the method comprising:

forming a GaN layer (13),

forming a barrier layer (14) on the GaN layer (13);

depositing a p-type gate material (15) on the barrier layer (14);

depositing a gate metal (17) on the p-type gate material (15);

forming a photoresist (¶ [0026]) over the gate metal (17);

etching the gate metal (17) and the p-type gate material (15, ¶ [0026]);

and

etching the gate metal (17) to form pair of ledges on the p-type gate material (15) below the gate metal (17, ¶ [0044]).

12. Lidow, however, does not specifically disclose wherein etching the gate metal to form a pair of ledges comprises isotopically etching. Attention is brought to the Park reference, which discloses a method comprising: depositing a gate material (Fig. 3, 107) on a substrate (101); depositing a gate layer (Fig. 3, 109) on the gate material (107); forming a photoresist (Fig. 3, 112) over the gate layer (109); etching the gate layer (109) and the gate material (107, see Fig. 4); and isotropically etching the gate layer (Fig. 5, 109) to form pair of ledges on the gate material (107) below the gate layer (109, ¶ [0040]). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method disclosed by Lidow to include wherein etching the gate metal to form a pair of ledges comprises isotopically etching, as taught by Park, in order to selectively etch the sidewalls of the gate metal with respect to the p-type gate material.

13. Regarding **claim 13**, Lidow discloses wherein the step of [isotropically] etching the gate metal (17) comprises etching the gate metal (17) to reduce a width of the gate metal (17), such that the width of the gate metal (17) is less than a width of the p-type gate material (15, see Fig. 10 and ¶ [0044]).

14. Regarding **claim 14**, Lidow further discloses depositing source (20) and drain (19) contacts on the barrier layer (14).

15. Regarding **claim 15**, Lidow discloses wherein the step of etching the p-type material (15) comprises forming side surface of the p-type gate material (15) that extend

horizontally towards the source contact (20) and the drain contact (19), respectively, and contact the barrier layer (14; see Fig. 10).

16. Regarding **claim 16**, Lidow discloses wherein the pair of ledges of the p-type gate material (15) are self-aligned.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE C. NIESZ whose telephone number is (303)297-4333. The examiner can normally be reached on Monday through Friday 10-6 EST.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMIE C NIESZ/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 14/447,069	Applicant(s)/Patent Under Reexamination CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2010/0258843 A1	10-2010	Lidow; Alexander	H01L29/1066	257/192
*	B	US-2004/0119110 A1	06-2004	Park, Sung-Chul	H01L21/28273	257/315
	C	US-				
	D	US-				
	E	US-				
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	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Used in Lieu of PTO/SB/08A/B
(Based on PTO 10-07 version)

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	14/447,069-Conf. #7150
Filing Date	July 30, 2014
First Named Inventor	Jianjun Cao
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	E0101.0032

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA*	2010/0258843 A1	10-14-2010	Lidow et al.	
	AB*	6,730,552	05-04-2004	Abadeer et al.	
	AC*	2013/0168743 A1	07-04-2013	Dove	
	AD*	7,939,880	05-10-2011	Kang et al.	
	AE*	2009/0004872 A1	01-01-2009	Okamoto	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	BA	JP 2011-142182 A	07-21-2011			√

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

√ English Language Abstract Also Enclosed

Examiner Signature	/Jamie Niesz/	Date Considered	12/14/2015

DSMDB-3312153 v1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.N./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 7150

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/447,069	07/30/2014 RULE	257	2822	E0101.0032.US

APPLICANTS

Efficient Power Conversion Corporation, ElSegundo, CA;

INVENTORS

Jianjun Cao, Torrance, CA;
Alexander Lidow, Marina Del Rey, CA;
Alana Nakata, Redondo Beach, CA;

** **CONTINUING DATA** **********

** **FOREIGN APPLICATIONS** **********

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** ** SMALL ENTITY **
08/07/2014

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/Jamie C Niesz/ Examiner's Signature	☐ Initials	CA	6	16	3

ADDRESS

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403
UNITED STATES

TITLE

GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

FILING FEE RECEIVED		
730	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	Art Unit
	JAMIE C NIESZ	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2015	12/14/2015							
	1	÷	N							
	2	÷	N							
	3	÷	N							
	4	÷	N							
	5	÷	N							
	6	÷	N							
	7	÷	N							
	8	÷	N							
	9	÷	N							
	10	÷	N							
	11	÷	N							
	12	÷	✓							
	13	÷	✓							
	14	÷	✓							
	15	÷	✓							
	16	÷	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	Art Unit
	JAMIE C NIESZ	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/42316 and H01L 21/283	Dec. 14, 2015	JCN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	194	Dec. 14, 2015	JCN

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search EAST (see search history)	Dec. 14, 2015	JCN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Interference Search EAST (see search history)	Dec. 14, 2015	JCN

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"14447069"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/11 12:23
S2	5	("20090004872" | "20100258843" | "20130168743" | "6730552" | "7939880").PN.	US-PGPUB; USPAT	ADJ	ON	2015/12/11 12:35
S3	18	(GaN) and enhancement and (isotropically with gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:57
S4	264	(photoresist or resist) same (isotropically with gate with etch$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S5	111	(photoresist or resist) same (isotropically with gate with etch$4 with (side or sidewall))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/13 17:59
S6	5935	(H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01
S7	3	((H01L29/42316 or H01L21/283).cpc. or (257/194).ccls.) and ((photoresist or resist) same (isotropically with gate with etch$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	ADJ	ON	2015/12/14 12:01

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	0	(GaN and gate metal and Photoresist and ledges).clm.	US-PGPUB; USPAT	ADJ	ON	2015/12/14 12:01

12/ 14/ 2015 12:02:33 PM
C:\ Users\ jniesz1\ Documents\ EAST\ Workspaces\ 14447069.wsp

Docket No.: E0101.0032.US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit: 2822

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: J. C. Niesz

RESPONSE TO RESTRICTION REQUIREMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

In response to the restriction requirement set forth in the Office Action mailed September 21, 2015, Applicant hereby elects Group II, claims 12-16 for continued examination.

Dated: October 9, 2015

Respectfully submitted,

By _____
Stephen A. Soffen
Registration No.: 31,063
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

DSMDB-3370227 v1

Electronic Acknowledgement Receipt	
EFS ID:	23748887
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Rhonda White
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	09-OCT-2015
Filing Date:	30-JUL-2014
Time Stamp:	19:56:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	E01010032restriction.pdf	27952 27491d46699093bfca68f6924b78963a2dc6724c	no	1
Warnings:					
Information:					

Total Files Size (in bytes):	27952

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/447,069	07/30/2014	Jianjun Cao	E0101.0032.US	7150

24998 7590 09/21/2015
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
NIESZ, JAMIE C	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
09/21/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing-DC@dicksteinshapiro.com
WelchScroggsA@dicksteinshapiro.com

Office Action Summary	Application No. 14/447,069	Applicant(s) CAO ET AL.	
	Examiner JAMIE C. NIESZ	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-16* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-16* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application filed July 30, 2014.

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11, drawn to a semiconductor device, classified in H01L 29/42316.

II. Claims 12-16, drawn to a method for manufacturing a semiconductor device, classified in H01L 21/283.

4. The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process, such as: the gate metal can be deposited through a mask to form a pair of ledges on the p-type gate material, rather than the gate metal being isotropically etched after it is formed.

5. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above

and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

The inventions belong to separate main groups/subgroups and therefore require separate consideration and/or search.

6. **Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined** even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

7. The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

8. Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

9. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

10. The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

11. In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an

allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMIE C. NIESZ whose telephone number is (303)297-4333. The examiner can normally be reached on Monday through Friday 10-6 EST.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMIE C NIESZ/
Primary Examiner
Art Unit 2822

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14447069	CAO ET AL.
	Examiner	**Art Unit**
	JAMIE C NIESZ	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2015								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
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	13	÷								
	14	÷								
	15	÷								
	16	÷								

Used in Lieu of PTO/SB/08A/B
(Based on PTO 10-07 version)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	14/447,069-Conf. #7150
				Filing Date	July 30, 2014
				First Named Inventor	Jianjun Cao
				Art Unit	N/A
(Use as many sheets as necessary)				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	E0101.0032

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA*	2010/0258843 A1	10-14-2010	Lidow et al.	
	AB*	6,730,552	05-04-2004	Abadeer et al.	
	AC*	2013/0168743 A1	07-04-2013	Dove	
	AD*	7,939,880	05-10-2011	Kang et al.	
	AE*	2009/0004872 A1	01-01-2009	Okamoto	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	BA	JP 2011-142182 A	07-21-2011			√

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

√ English Language Abstract Also Enclosed

Examiner Signature		Date Considered	

DSMDB-3312153 v1

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference E01010047PC	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2014/048826	International filing date *(day/month/year)* 30 July 2014	(Earliest) Priority Date *(day/month/year)* 01 August 2013
Applicant EFFICIENT POWER CONVERSION CORPORATION		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 5

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/048826

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L21/00 (2014.01)
CPC - H01L29/778 (2014.09)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L21/00 (2014.01)
USPC - 438/180, 438/229, 438/299, 438/320, 438/339, 438/364, 438/578

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC - H01L29/2003, H01L29/778, H01L29/7786, H01L29/7787 (2014.09) (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Patents, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X – Y	US 2010/0258843 A1 (LIDOW et al.) 14 October 2010 (14.10.2010) Entire Document	1-11 ------ 12-16
Y	US 6,730,552 B1 (ABADEER et al.) 04 May 2004 (04.05.2004) Entire Document	12-16
A	JP 2011-142182 A (FUJII et al.) 21 July 2011 (21.07.2011) Entire Document	1-16
A	US 2013/0168743 A1 (DOVE) 04 July 2013 (04.07.2013) Entire Document	1-16
A	US 7,939,880 B2 (KANG et al.) 10 May 2011 (10.05.2011) Entire Document	1-16
A	US 2009/0004872 A1 (OKAMOTO) 01 January 2009 (01.01.2009) Entire Document	1-16

☐ Further documents are listed in the continuation of Box C. ☐

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22 October 2014	14 NOV 2014
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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FIELD-EFFECT TRANSISTOR

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Applicant(s): SHARP KK ± (SHARP CORP)

Classification: **- international:*H01L21/28; H01L21/338; H01L27/095; H01L29/06; H01L29/41; H01L29/778; H01L29/812***

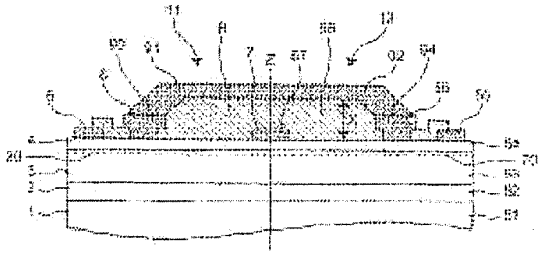
- cooperative:

Application number: JP20100001447 20100106

Priority number (s): JP20100001447 20100106

Abstract of JP2011142182 (A)

PROBLEM TO BE SOLVED: To provide a field-effect transistor which is unlikely to break even when applied with a high voltage. ;SOLUTION: The field-effect transistor includes first and second transistor portions 11 and 12 which are substantially identical to each other. The first transistor portion 11 includes a group-III nitride semiconductor layer structure including a heterojunction, a source electrode 5 and a drain electrode 7 disposed at an interval on the group-III nitride semiconductor layer structure, a gate electrode 6 having a field plate 91, and an insulator layer 8 disposed to cover the drain electrode 7. The field plate 91 extends in an eaves shape to cover the drain electrode 7. The second transistor portion 12 is disposed substantially plane-symmetrically with the first transistor portion 11. The group-III nitride semiconductor structure, insulator layer 8, and drain electrode 7 of the first transistor portion 11 are united with a corresponding structure or layer in the second transistor portion 12. ;COPYRIGHT: (C) 2011,JPO&INPIT



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H01L 29/812	***(2006.01)***	H01L	21/28	301B	
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審査請求 未請求　請求項の数 11　OL　（全 27 頁）　最終頁に続く

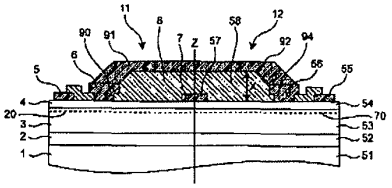
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最終頁に続く

(54)【発明の名称】電界効果トランジスタ

(57)【要約】
【課題】高電圧を印加しても壊れにくい電界効果トランジスタを提供すること。
【解決手段】この電界効果トランジスタは、略同一の第１、第２トランジスタ部１１，１２を備える。第１のトランジスタ部１１は、ヘテロ接合を含むIII族窒化物半導体層構造、III族窒化物半導体層構造上に間隔をおいて配置されたソース電極５およびドレイン電極７、フィールドプレート９１を有するゲート電極６、ドレイン電極７を被覆するように配置された絶縁体層８を有する。フィールドプレート９１は、ドレイン電極７を覆うようにひさし状に延在する。第２のトランジスタ部１２は、第１のトランジスタ部１１と略面対称に配置されている。第１のトランジスタ部１１のIII族窒化物半導体層構造、絶縁体層８およびドレイン電極７は、第２のトランジスタ部１２において対応する構造または層と一体化されている。
【選択図】図１



【特許請求の範囲】
【請求項１】
第１のトランジスタ部と、
上記第１のトランジスタ部と略同一の第２のトランジスタ部と
を備え、
上記第１のトランジスタ部および上記第２のトランジスタ部は、夫々
ヘテロ接合を含むIII族窒化物半導体層構造と、
上記III族窒化物半導体層構造上に間隔をおいて配置されたソース電極およびドレイン電極と、
上記III族窒化物半導体層構造上に上記ドレイン電極を被覆するように配置された第１の絶縁体層と、
上記ソース電極と上記ドレイン電極との間に、上記ソース電極および上記ドレイン電極に間隔をおいて位置するゲート電極本体と、上記第１の絶縁体層上に位置すると共に、上記ゲート電極本体から上記ドレイン電極に向けてひさし状に延びるフィールドプレートとを有するゲート電極と
を有し、
上記第１のトランジスタ部の上記III族窒化物半導体層構造と、上記第２のトランジスタ部の上記III族窒化物半導体層構造とは、一体化されており、
上記第１のトランジスタ部の上記第１の絶縁体と、上記第２のトランジスタ部の上記第１の絶縁体とは、一体化されており、
上記第１のトランジスタ部の上記ドレイン電極と、上記第２のトランジスタ部の上記ドレイン電極とは、一体化されており、
上記第１のトランジスタ部と、第２のトランジスタ部とは、略面対称に配置され、
上記第１のトランジスタ部の上記フィールドプレートと、上記第２のトランジスタ部のフィールドプレートとは、電気的に接続されていることを特徴とする電界効果トランジスタ。
【請求項２】
請求項１に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部の上記フィールドプレートと、上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面とのその上面の法線方向の最大の距離は、１ミクロン以上であることを特徴とする電界効果トランジスタ。
【請求項３】
請求項１または２に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部の上記フィールドプレートは、上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面から上記第１のトランジスタ部の上記フィールドプレートまでの上記上面の法線方向の距離が、上記第１のトランジスタ部の上記ゲート電極から上記第１のトランジスタ部の上記ドレイン電極に行くにしたがって連続的に大きくなる部分を有していることを特徴とする電界効果トランジスタ。
【請求項４】
請求項１から３までのいずれか一項に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部の上記フィールドプレートは、
上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面に略平行な状態で、その上面にその上面の法線方向に対向する第１の面を有する第１部分と、
上記法線方向において、上記第１部分の上記第１のトランジスタ部の上記III族窒化物半導体層構造側とは反対側に位置すると共に、上記上面に略平行な状態で上記上面に上記法線方向に対向する第２の面を有する第２部分と、
上記第１部分と上記第２部分とを連結する連結部と
を有し、
上記第１部分の延在方向の長さが、０．５μｍ以上かつ３μｍ以下であり、
上記第１の面と上記上面との上記法線方向の距離が、１０μｍ以上かつ５０μｍ以下で

あることを特徴とする電界効果トランジスタ。
【請求項５】
請求項１から４までのいずれか一項に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部の上記第１の絶縁体層は、誘電率が互いに異なる複数の層を有していることを特徴とする電界効果トランジスタ。
【請求項６】
請求項１から５までのいずれか一項に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部の上記ゲート電極と、上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面との間に第２の絶縁体層を備えることを特徴とする電界効果トランジスタ。
【請求項７】
請求項１から６までのいずれか一項に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部の上記III族窒化物半導体層構造の上記上面は、凹部を有し、
上記第１のトランジスタ部の上記ゲート電極は、上記凹部に上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面の法線方向に重なる位置に存在していることを特徴とする電界効果トランジスタ。
【請求項８】
請求項１から７までのいずれか一項に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部の上記III族窒化物半導体層構造は、
下層チャネル層と、
上記下層チャネル層の上面に配置された上層チャネル層と、
上記上層チャネル層の上面に配置されたバリア層と
を有し、
上記上層チャネル層は、上記バリア層および上記下層チャネル層のいずれよりも小さいバンドギャップを有していることを特徴とする電界効果トランジスタ。
【請求項９】
請求項１から８までのいずれか一項に記載の電界効果トランジスタにおいて、
上記第１のトランジスタ部および上記第２のトランジスタ部は、夫々導電性基板を備え
上記第１のトランジスタ部の上記導電性基板と、上記第２のトランジスタ部の上記導電性基板とは、一体化されており、
上記第１のトランジスタ部の上記III族窒化物半導体層構造は、上記第１のトランジスタ部の上記導電性基板上に配置されていることを特徴とする電界効果トランジスタ。
【請求項１０】
第１のトランジスタ部と、
上記第１のトランジスタと略同一の第２のトランジスタ部と
を備え、
上記第１のトランジスタ部および上記第２のトランジスタ部は、夫々
ヘテロ接合を含むIII族窒化物半導体層構造と、
上記III族窒化物半導体層構造上に間隔をおいて配置されたゲート電極およびドレイン電極と、
上記III族窒化物半導体層構造上に、上記ドレイン電極および上記ゲート電極を被覆するように配置された第１の絶縁体層と、
上記ゲート電極の上記ドレイン電極側とは反対側に、上記ゲート電極に間隔をおいて位置するソース電極本体と、上記第１の絶縁体層上に位置すると共に、上記ソース電極本体から上記ドレイン電極に向けてひさし状に延びるフィールドプレートとを有するソース電極と
を有し、
上記第１のトランジスタ部の上記III族窒化物半導体層構造と、上記第２のトランジスタ部の上記III族窒化物半導体層構造とは、一体化されており、

上記第１のトランジスタ部の上記第１の絶縁体と、上記第２のトランジスタ部の上記第１の絶縁体とは、一体化されており、
上記第１のトランジスタ部の上記ドレイン電極と、上記第２のトランジスタ部の上記ドレイン電極とは、一体化されており、
上記第１のトランジスタ部と、第２のトランジスタ部とは、略面対称に配置され、
上記第１のトランジスタ部の上記フィールドプレートと、上記第２のトランジスタ部のフィールドプレートとは、電気的に接続されていることを特徴とする電界効果トランジスタ。
【請求項１１】
請求項１から１０までのいずれか一項に記載の電界効果トランジスタにおいて、
上記第１トランジスタ部の上記フィールドプレートおよび上記第２のトランジスタ部の上記フィールドプレートは、貫通穴を有し、上記第１のトランジスタ部の上記ドレイン電極および上記第２のトランジスタ部の上記ドレイン電極は、上記第１のトランジスタ部の上記ドレイン電極の上面の法線方向に、上記貫通穴に重なっていることを特徴とする電界効果トランジスタ。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、電界効果トランジスタに関する。
【背景技術】
【０００２】
III族窒化物半導体を用いた高耐圧ヘテロ接合型電界効果トランジスタ（ＨＦＥＴ）は、高い絶縁破壊電界強度、高い熱伝導率を有する高周波のパワースイッチング素子として広く研究されている（例えば、特許文献１参照）。図１２に、III族窒化物半導体を用いた代表的なｎチャネル型ＨＦＥＴの概略断面を示す（特許文献１参照）。
【０００３】
図１２のトランジスタでは、基板１２０１上に、III族窒化物半導体を含むバッファ層１２０２が形成され、その上部にIII族窒化物半導体からなるチャネル層１２０３が形成され、その上部にチャネル層１２０３よりも大きなバンドギャップを持ったIII族窒化物半導体からなるバリア層１２０４が形成されている。互いに異なるバンドギャップを有するチャネル層１２０３とバリア層１２０４との界面にはヘテロ接合が形成されている。自発分極とピエゾ分極によりヘテロ接合界面の近傍は、電子が高濃度で蓄積する二次元電子ガス１２２０が存在すると共に、ヘテロ接合を含むIII族窒化物半導体層構造になっている。また、二次元電子ガスのシート電子濃度は、チャネル層とバリア層の構成により異なるが、例えば、1×10^{12}～1×10^{13}／ｃｍ^{2}程度になっている。
【０００４】
ソース電極１２０５、ドレイン電極１２０７およびゲート電極１２０６がバリア層１２０４上部に形成され、絶縁体層１２０８がバリア層を覆うよう形成されている。
【０００５】
上記ゲート電極１２０６は、ドレイン電極１２０７側にひさし状に張り出し絶縁体層１２０８上に形成されたフィールドプレート部１２９１を有している。これにより、電界効果トランジスタに高電圧を印加した際に、バリア層１２０４と接するドレイン電極１２０７側のゲート電極１２０６の端角部（図１２のＡ部）に掛かる電界を緩和させる。この結果、前記のゲート電極１２０６の端角部に局所的に電界が集中することによるゲート電極１２０６の周囲での破壊を抑制し、トランジスタの破壊耐圧の低下を防ぐようになっている。
【０００６】
尚、図１２のようなトランジスタでは、ソース電極１２０５とドレイン電極１２０７との間の電流は、電子をキャリアとして、主に二次元電子ガス１２２０内を流れるようになっている。上記ゲート電極１２０６に印加する電圧を変化させることにより、オン／オフ

を切換えできるようになっている。

【０００７】

しかし、図１２に示すような構造の電界効果トランジスタにおいて、トランジスタがオフの状態で、ソース電極１２０５およびゲート電極１２０６と、ドレイン電極１２０７との間に高電圧を印加すると、素子内部にかかる電界によりキャリアが増大して、素子が壊れてしまう場合がある。

【０００８】

詳しくは、従来のフィールドプレート構造を有する電界効果トランジスタに、高電圧を印加すると、「バリア層と接触しているドレイン側のゲート電極端角部（図１２のＡ部）」だけでなく、「ドレイン電極との距離が最も短くなるフィールドプレート電極端角部（図１２のＢ部）」と、「前記フィールドプレート電極端角部直下の絶縁体層および半導体からなるバリア層（図１２のＣ部）」に局所的な電界集中が起こる。特に、ドレイン電極１２０７との距離が短くなった場合においては、フィールドプレート電極端角部（図１２のＢ部）で非常に電界が集中しやすいことが知られている（非特許文献１参照）。

【０００９】

このことにより、上記フィールドプレート電極端角部の周囲にある絶縁体層１２０８や半導体からなるバリア層１２０４（図１２のＢ部およびＣ部）において、局所的に非常に大きな電界がかかる部分が生じ、キャリアが増大し素子が壊れることがある。

【００１０】

このキャリアの増大は、高電圧を印加すると、素子内部に絶縁破壊強度を超える電界強度が局所的部分にかかり、その部分でなだれ降伏が起こることが一因であると考えられている。トランジスタを構成する絶縁体層１２０８や、バリア層１２０４などといった半導体部において、キャリアが急激に増加することにより、素子破壊が起こると考えられているのである。

【先行技術文献】

【特許文献】

【００１１】

【特許文献１】特開２００４－２００２４８号公報

【特許文献２】特開２００４－１７７１５１号公報

【非特許文献】

【００１２】

【非特許文献１】Wataru Saito, Masahiko Kuraguchi, Yoshiharu Takada, Kunio Tsuda, Ichiro Omura, and Tsuneo Ogura "Design Optimization of High Breakdown Voltage AlGaN-GaN Power HEMT on an Insulating Substrate for RONA-VB Tradeoff Characteristics" IEEE TRANSACTIONS ON ELECTRON DEVICES, vol.52, No.1, 2005

【発明の概要】

【発明が解決しようとする課題】

【００１３】

そこで、本発明の課題は、高電圧を印加しても壊れにくい電界効果トランジスタを提供することにある。

【課題を解決するための手段】

【００１４】

上記課題を解決するため、この発明の電界効果トランジスタは、

第１のトランジスタ部と、

上記第１のトランジスタ部と略同一の第２のトランジスタ部と

を備え、

上記第１のトランジスタ部および上記第２のトランジスタ部は、夫々

ヘテロ接合を含むIII族窒化物半導体層構造と、

上記III族窒化物半導体層構造上に間隔をおいて配置されたソース電極およびドレイン電極と、

上記III族窒化物半導体層構造上に上記ドレイン電極を被覆するように配置された第１の絶縁体層と、

上記ソース電極と上記ドレイン電極との間に、上記ソース電極および上記ドレイン電極に間隔をおいて位置するゲート電極本体と、上記第１の絶縁体層上に位置すると共に、上記ゲート電極本体から上記ドレイン電極に向けてひさし状に延びるフィールドプレートとを有するゲート電極と

を有し、

上記第１のトランジスタ部の上記III族窒化物半導体層構造と、上記第２のトランジスタ部の上記III族窒化物半導体層構造とは、一体化されており、

上記第１のトランジスタ部の上記第１の絶縁体と、上記第２のトランジスタ部の上記第１の絶縁体とは、一体化されており、

上記第１のトランジスタ部の上記ドレイン電極と、上記第２のトランジスタ部の上記ドレイン電極とは、一体化されており、

上記第１のトランジスタ部と、第２のトランジスタ部とは、略面対称に配置され、

上記第１のトランジスタ部の上記フィールドプレートと、上記第２のトランジスタ部のフィールドプレートとは、電気的に接続されていることを特徴としている。

【００１５】

また、一実施形態では、

上記第１のトランジスタ部の上記フィールドプレートと、上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面とのその上面の法線方向の最大の距離は、１ミクロン以上である。

【００１６】

また、一実施形態では、

上記第１のトランジスタ部の上記フィールドプレートは、上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面から上記第１のトランジスタ部の上記フィールドプレートまでの上記上面の法線方向の距離が、上記第１のトランジスタ部の上記ゲート電極から上記第１のトランジスタ部の上記ドレイン電極に行くにしたがって連続的に大きくなる部分を有している。

【００１７】

また、一実施形態では、

上記第１のトランジスタ部の上記フィールドプレートは、

上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面に略平行な状態で、その上面にその上面の法線方向に対向する第１の面を有する第１部分と、

上記法線方向において、上記第１部分の上記第１のトランジスタ部の上記III族窒化物半導体層構造側とは反対側に位置すると共に、上記上面に略平行な状態で上記上面に上記法線方向に対向する第２の面を有する第２部分と、

上記第１部分と上記第２部分とを連結する連結部と

を有し、

上記第１部分の延在方向の長さが、０．５μｍ以上かつ３μｍ以下であり、

上記第１の面と上記上面との上記法線方向の距離が、１０μｍ以上かつ５０μｍ以下である。

【００１８】

また、一実施形態では、

上記第１のトランジスタ部の上記第１の絶縁体層は、誘電率が互いに異なる複数の層を有している。

【００１９】

また、一実施形態では、

上記第１のトランジスタ部の上記ゲート電極と、上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面との間に第２の絶縁体層を備える。

【００２０】

また、一実施形態では、
上記第１のトランジスタ部の上記III族窒化物半導体層構造の上記上面は、凹部を有し、
上記第１のトランジスタ部の上記ゲート電極は、上記凹部に上記第１のトランジスタ部の上記III族窒化物半導体層構造の上面の法線方向に重なる位置に存在している。
【００２１】
また、一実施形態では、
上記第１のトランジスタ部の上記III族窒化物半導体層構造は、
下層チャネル層と、
上記下層チャネル層の上面に配置された上層チャネル層と、
上記上層チャネル層の上面に配置されたバリア層と
を有し、
上記上層チャネル層は、上記バリア層および上記下層チャネル層のいずれよりも小さいバンドギャップを有している。
【００２２】
また、一実施形態では、
上記第１のトランジスタ部および上記第２のトランジスタ部は、夫々導電性基板を備え
上記第１のトランジスタ部の上記導電性基板と、上記第２のトランジスタ部の上記導電性基板とは、一体化されており、
上記第１のトランジスタ部の上記III族窒化物半導体層構造は、上記第１のトランジスタ部の上記導電性基板上に配置されている。
【００２３】
また、本発明の電界効果トランジスタは、
第１のトランジスタ部と、
上記第１のトランジスタと略同一の第２のトランジスタ部と
を備え、
上記第１のトランジスタ部および上記第２のトランジスタ部は、夫々
ヘテロ接合を含むIII族窒化物半導体層構造と、
上記III族窒化物半導体層構造上に間隔をおいて配置されたゲート電極およびドレイン電極と、
上記III族窒化物半導体層構造上に、上記ドレイン電極および上記ゲート電極を被覆するように配置された第１の絶縁体層と、
上記ゲート電極の上記ドレイン電極側とは反対側に、上記ゲート電極に間隔をおいて位置するソース電極本体と、上記第１の絶縁体層上に位置すると共に、上記ソース電極本体から上記ドレイン電極に向けてひさし状に延びるフィールドプレートとを有するソース電極と
を有し、
上記第１のトランジスタ部の上記III族窒化物半導体層構造と、上記第２のトランジスタ部の上記III族窒化物半導体層構造とは、一体化されており、
上記第１のトランジスタ部の上記第１の絶縁体と、上記第２のトランジスタ部の上記第１の絶縁体とは、一体化されており、
上記第１のトランジスタ部の上記ドレイン電極と、上記第２のトランジスタ部の上記ドレイン電極とは、一体化されており、
上記第１のトランジスタ部と、第２のトランジスタ部とは、略面対称に配置され、
上記第１のトランジスタ部の上記フィールドプレートと、上記第２のトランジスタ部のフィールドプレートとは、電気的に接続されていることを特徴としている。
【００２４】
また、一実施形態では、
上記第１トランジスタ部の上記フィールドプレートおよび上記第２のトランジスタ部の上記フィールドプレートは、貫通穴を有し、

上記第１のトランジスタ部の上記ドレイン電極および上記第２のトランジスタ部の上記ドレイン電極は、上記第１のトランジスタ部の上記ドレイン電極の上面の法線方向に、上記貫通穴に重なっている。

【発明の効果】

【００２５】

従来のフィールドプレート構造を有する電界効果トランジスタに、高電圧を印加すると、「バリア層と接触しているドレイン側のゲート電極端角部（図１２のＡ部）」だけでなく、「ドレイン電極との距離が最も短くなるフィールドプレート電極端角部（図１２のＢ部）」と、「前記フィールドプレート電極端角部直下の絶縁体層および半導体からなるバリア層（図１２のＣ部）」に局所的な電界集中が起こる。特に、ドレイン電極１２０７との距離が短くなった場合においては、フィールドプレート電極端角部（図１２のＢ部）で非常に電界が集中しやすいことが知られている。

【００２６】

また、フィールドプレート電極が、ソース電極１２０５とゲート電極１２０７のいずれか、または、それら両方の電極に接続されて、フィールドプレートがそれら電極の一部をなしているか否かに係わらずフィールドプレート電極(角)端への電界集中は発生する。

【００２７】

このことにより、局所的に非常に大きな電界がかかる部分が生じ、周囲にある絶縁破壊が起こりやすい部分、例えば絶縁体層１２０８や半導体からなるバリア層１２０４で絶縁破壊が生じる。

【００２８】

この結果、素子の破壊が起こり易くなり、絶縁破壊耐圧および信頼性低下の原因の一つとなってしまう。

【００２９】

本発明によれば、局所的な電界集中の原因となるフィールドプレート電極端角部（図１２のＢ部）がないことから、これに伴う、絶縁破壊が起こりやすい部分への電界集中を緩和することができる。したがって、絶縁耐層やバリア層など半導体層の絶縁破壊を防止することができて、トランジスタの破壊電圧（耐圧）を向上でき、高電圧を印加しても壊れにくい電界効果トランジスタを得ることができる。

【図面の簡単な説明】

【００３０】

【図１】本発明の第１実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図２】本発明の第２実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図３】本発明の第３実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図４】本発明の第４実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図５】本発明の第５実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図６】本発明の第６実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図７】本発明の第７実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図８】本発明の第８実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図９】本発明の第９実施形態の電界効果トランジスタの構成を示す概略断面図である。

【図１０Ａ】従来の電界効果トランジスタについてのシミュレーションの結果を示す説明図であり、トランジスタ内部の電位の分布を示す図である。

【図１０Ｂ】従来の電界効果トランジスタについてのシミュレーションの結果を示す説明図であり、トランジスタ内部の電界強度分布を示す図である。

【図１１Ａ】本発明の第１実施形態の電界効果トランジスタについてのシミュレーションの結果を示す説明図であり、トンジスタ内部の電位の分布を示す図である。

【図１１Ｂ】本発明の第１実施形態の電界効果トランジスタについてのシミュレーションの結果を示す説明図であり、トランジスタ内部の電界強度分布を示す図である。

【図１２】従来の電界効果トランジスタの構成を示す概略断面図である。

【発明を実施するための形態】

【００３１】
以下、本発明の各実施形態を、図面を用いて説明する。尚、図面や以下の記述中で示す構成は、例示であって、本発明の範囲は、図面や以下の記述中で示すものに限定されるものではない。
【００３２】
本発明において、電界効果トランジスタとは、ゲート電極に加えた電圧（電荷）によりゲート電極下の半導体層のキャリアを制御し、ソース電極とドレイン電極との間の電流を増減させるトランジスタをいう。また、本発明の電界効果トランジスタは、ヘテロ接合型電界効果トランジスタであってもよい。
【００３３】
尚、以下に示す第１乃至第９実施形態の電界効果トランジスタでは、いずれも、第１のトランジスタ部１１，２１１，３１１，４１１，５１１，６１１，７１１，８１１，９１１と、第２のトランジスタ部１２，２１２，３１２，４１２，５１２，６１２，７１２，８１２，９１２とは、略同一であり、かつ、略面対称に位置している。
【００３４】
（第１実施形態）
図１は、本発明の第１実施形態の電界効果トランジスタの構造を示す概略断面図である。
【００３５】
この電界効果トランジスタは、第１のトランジスタ部１１と、第２のトランジスタ部１２とを備える。上記第１のトランジスタ部１１は、第２のトランジスタ部１２と略同一である。
【００３６】
上記第１のトランジスタ部１１は、導電性Ｓｉ基板１、バッファ層２、III族窒化物半導体からなるチャネル層３、III族窒化物半導体からなるバリア層４、ソース電極５、ゲート電極６、ドレイン電極７および第１の絶縁体層としての絶縁体層８を有する。上記バッファ層２、チャネル層３およびバリア層４は、ヘテロ接合を含むIII族窒化物半導体層構造を構成している。
【００３７】
上記III族窒化物半導体からなるバッファ層２、III族窒化物半導体からなるチャネル層３およびIII族窒化物半導体からなるバリア層４は、導電性Ｓｉ基板１上にこの順で設けられている。また、上記ソース電極５、ゲート電極６およびドレイン電極７は、バリア層４上にこの順で離間して設けられている。上記絶縁体層８は、ドレイン電極７を覆うように、III族窒化物半導体層構造上に配置されている。
【００３８】
上記ゲート電極６は、ゲート電極本体９０と、フィールドプレート９１とを有し、このフィールドプレート９１は、絶縁体層８上に位置すると共に、ゲート電極本体９０からドレイン電極７側にひさし状に張り出している。
【００３９】
言い換えると、上記フィールドプレート９１は、ヘテロ構造を含むIII族窒化物半導体層構造の上面１８の法線方向において、III族窒化物半導体層構造側とは反対側かつ上記法線方向に垂直な方向においてドレイン電極７側に延在している。
【００４０】
上記第２のトランジスタ部１２の導電性Ｓｉ基板５１は、導電性Ｓｉ基板１と一体化され、第２のトランジスタ部１２のIII族窒化物半導体層構造は、第１のトランジスタ部１１のIII族窒化物半導体層構造と一体化されている。また、上記第２のトランジスタ部１２の第１の絶縁体層としての絶縁体層５８は、絶縁体層８と一体化され、第２のトランジスタ部１２のドレイン電極５７は、ドレイン電極７と一体化されている。上記第１のトランジスタ部１１と第２のトランジスタ部１２とは、略面対称に配置されている。もっと詳しくは、上記第２のトランジスタ部１２は、図１の断面において、第１のトランジスタ部

１１に対して、ドレイン電極７を垂直に二等分する線（図１にＺで示す）に対して、線対称となるように配置されている。

【００４１】

上記第１のトランジスタ部１１と第２のトランジスタ部１２とは、互いに向かい合うように配置されている。上記第１のトランジスタ部１１のフィールドプレート９１と、第２のトランジスタ部１２のフィールドプレート９２とは、ドレイン電極７を被覆するように形成された絶縁体層８上で電気的に接続されている。

【００４２】

尚、図１において、５２は、第２のトランジスタ部１２のバッファ層を示し、５３は、第２のトランジスタ部１２のチャネル層を示し、５４は、第２のトランジスタ部１２のバリア層を示し、５６は、第２のトランジスタ部１２のゲート電極を示し、７０は、第２のトランジスタ部１２の二次元電子ガスを示し、９４は、第２のトランジスタ部１２のゲート電極５６のゲート電極本体を示している。

【００４３】

上記基板１は、上部にチャネル層３などの半導体層を形成できる基板であれば如何なる基板であっても良い。上記基板１は、導電性基板であってもよく、高抵抗基板であってもよい。上記基板１としては、例えば、ｎ型不純物をドープしたＳｉ（n^+－Ｓｉ基板）、Ｓｉ、ＧａＮ、ＳｉＣ、Ga_2O_3またはサファイア基板等を使用できる。

【００４４】

また、上記基板１は、導電性基板であってもよい。この場合、上記基板１と、ソース電極５とを、電気的に接続してもよい。このようにすると、上記基板１と、ドレイン電極５との間に電圧を印加できて、ゲート電極６と、ドレイン電極７との間にかかる電界を緩和することができる。そして、その結果、絶縁破壊の発生を抑制することができる。

【００４５】

また、上記基板１が導電性基板である場合、ソース電極５および基板１を接地することもできる。また、上記基板１が導電性基板である場合、基板１と、ソース電極５とを電気的に接続することにより、ダイボンドやワイヤーボンドなどの実装工程を簡略化することができて、電界効果トランジスタをパッケージングする場合に、デバイスを小型化することができる。

【００４６】

また、導電性基板は、ソース電極５と電気的に接続してもよい。このことにより、ソース電極５とドレイン電極７との間に電圧を印加した場合、基板１とドレイン電極７との間に縦方向の電界が生じドレイン電極７の下部のチャネル層３にかかる電界強度が大きくなる。その結果、ソース電極５およびゲート電極６とドレイン電極７との間の電界を緩和することができる。これらより、絶縁破壊が生じやすいドレイン電極７のゲート電極６側のチャネル層３にかかる電界強度を緩和することができ、絶縁破壊を抑制することができる。

【００４７】

上記バッファ層２は、基板１の上に設けられることができ、上部にチャネル層３等の半導体層を形成で出来るものであれば、如何なる材料で構成されても良い。上記バッファ層２は半導体であっても良く、半導体の複数の層で構成されても良い。上記バッファ層２としては、例えば、化合物半導体である、ＧａＮ、ＡｌＮ、ＩｎＮ、$Al_xGa_{1-x}N$、$In_xGa_{1-x}N$、ＳｉＣ、ＢＮなどの半導体を使用できる。

【００４８】

また、上記バッファ層２は複数の半導体の超格子でも良い。このようにすると、上記チャネル層３およびバリア層４の欠陥密度を減らし、結晶性を向上させることができるため、良好なスイッチング特性のトランジスタを得ることができる。

【００４９】

上記チャネル層３は、バッファ層２の上（もっと広くは基板１の上）に設けられることができ、かつ、ソース電極５とドレイン電極７との間の電流が流れうるものであれば如何

なる材料からなっていても良い。また、キャリアは、電子であってもよい。上記チャネル層３は、例えば、III族窒化物半導体で構成されても良く、例えば、ＧａＮ、$Al_xGa_{1-x}N$、$In_xGa_{1-x}N$等で構成されても良い。なお、例えばｘは０より大きく０．５以下でもよい。また、例えばｘは、０．００１以上０．１以下であってもよい。また、上記チャネル層３の厚さは、特に限定されないが、例えば、１～１０μｍであり、さらに好ましくは２μｍ～５μｍである。上記チャネル層３は、例えば、基板の上にＭＯＣＶＤやＭＢＥにより形成することができる。

【００５０】

上記バリア層４は、チャネル層３の上に設けられることができ、チャネル層３との界面にヘテロ接合を形成できるものであれば如何なる材料からなっていても良い。上記バリア層４は、例えば、III族窒化物半導体からなっていても良く、例えば、ＡｌＮ、$Al_xGa_{1-x}N$、$In_xGa_{1-x}N$などからなってもよい。ここで、例えば、ｘは０．０５以上０．５以下でもよい。また、例えば、ｘは、０．１以上０．３以下であってもよい。III族窒化物半導体は、絶縁破壊強度が高く熱伝導率が高いため、高周波のパワースイッチング素子とすることができる。また、例えば、チャネル層３がＧａＮまたは$Ga_xAl_{1-x}N$からなり、バリア層４が$Ga_yAl_{1-y}N$からなるとき、ｙはｘより大きくてもよく、０．０２≦（ｙ－ｘ）≦０．３であってもよい。このようにすると、上記バリア層４のバンドギャップは、チャネル層３のバンドギャップよりも大きくすることができる。

【００５１】

また、上記バリア層４は、チャネル層３よりも大きいバンドギャップを有していても良い。このようにすると、上記チャネル層３との界面に、二次元電子ガス２０を形成することができる。なお、ＡｌＧａＮ／ＧａＮヘテロ接合では、自発分極と、ピエゾ分極とにより1×10^{12}～1×10^{13}／cm^2程度のシート電子濃度が発生する。また、ソース電極５とドレイン電極７との間に流れる電流、つまりキャリアである電子の大部分を、チャネル層３内に流すことができる。また、バリア層４の厚さは、特に限定されないが、例えば、０．０１μｍ以上０．１μｍ以下とすることができる。また、例えば、０．０１５μｍ以上０．０５μｍ以下とすることができる。上記バリア層４は、例えば、チャネル層３の上にＭＯＣＶＤやＭＢＥにより形成することができる。

【００５２】

本発明において、ソース電極５、ゲート電極６、ドレイン電極７は、本発明の電界効果トランジスタを構成することができる電極であれば特に限定されない。上記ソース電極５は、バリア層４上に、ソース電極５、ゲート電極６およびドレイン電極７の順で離間して設けられる電極であれば、如何なる材料からなり、如何なる構造であっても良い。ソース電極５の材料としては、例えば、Ｔｉ、Ｚｒ、Ｈｆ、Ａｌ、ＡｌＳｉ、Ｗ、ＷＮ、Ａｕ、Ｐｔから選択された少なくとも一種の金属を用いることができる。また、上記ソース電極５は、例えば、Ｔｉ／Ｐｔ／Ａｕ、Ｈｆ／Ａｌ／Ａｕ、Ｔｉ／Ａｌからなる電極とすることができる。

【００５３】

上記ソース電極５は、真空蒸着法、スパッタ法などにより形成することができる。また、バリア層４上に絶縁体層８を形成している場合、ソース電極５を形成する部分の絶縁体層８をエッチングにより除去して、ソース電極５がバリア層４に接触するように、ソース電極を形成することができる。

【００５４】

また、上記ソース電極５は、真空蒸着法、スパッタ法などにより形成した後、熱処理を行うことで形成できる。熱処理は、時間、温度は、限定されない。熱処理としては、例えば、８００℃で１分間の熱処理を採用できる。このようにすると、ソース電極５とチャネル層３とを、オーミック接続させることができる。

【００５５】

上記ソース電極５は、ソース電極５直下に形成されたｎ型不純物拡散層を介してオーミ

ック接続する構成であっても良い。ｎ型不純物拡散層は、ソース電極５直下のバリア層４およびチャネル層３にｎ型不純物をイオン注入することにより、形成することができる。また、イオン注入後に熱処理を行うことにより、ｎ型不純物拡散領域を活性化することができる。このことによりソース電極５とチャネル層３との間の接触抵抗を低減することができる。また、ソース電極５は、真空蒸着法、スパッタ法などにより、上記ｎ型不純物拡散領域直上に形成した後、熱処理されることができる。熱処理は、時間、温度は、限定されない。熱処理としては、例えば、５５０℃で１分間の熱処理を採用できる。このことにより、ソース電極５とチャネル層３とを、ｎ型不純物拡散層を介したより良好なオーミック接続することができる。

【００５６】

上記ドレイン電極７は、バリア層４上に、ソース電極５、ゲート電極６およびドレイン電極７の順で離間して設けられる電極であれば、如何なる材料からなっていても良く、如何なる構造を有していても良い。ドレイン電極７の材料としては、例えば、Ｔｉ、Ｚｒ、Ｈｆ、Ａｌ、ＡｌＳｉ、Ｗ、ＷＮ、Ａｕ、Ｐｔから選択された少なくとも一種の金属を用いることができる。また、ドレイン電極７は、例えば、Ｔｉ／Ｐｔ／Ａｕ、Ｈｆ／Ａｌ／Ａｕ、Ｔｉ／Ａｌからなる電極とすることができる。上記ドレイン電極は７、真空蒸着法、スパッタ法などにより形成することができる。

【００５７】

上記バリア層４上に絶縁体層８を形成している場合、ドレイン電極７を形成する部分の絶縁体層８をエッチングにより除去し、ドレイン電極７がバリア層４に接触するように、ドレイン電極７を形成することができる。上記ドレイン電極７は、真空蒸着法、スパッタ法などにより形成した後、熱処理されることができる。熱処理は、時間、温度は、限定されない。熱処理としては、例えば、８００℃で１分間の熱処理を採用できる。このことにより、ドレイン電極７とチャネル層３とを、オーミック接続することができる。また、上記ドレイン電極７は、ドレイン電極７直下に形成されたｎ型不純物拡散層を介してオーミック接続されても良い。ここで、上記ｎ型不純物拡散層は、ドレイン電極７直下のバリア層４およびチャネル層３にｎ型不純物をイオン注入することにより、形成することができる。また、イオン注入後に熱処理を行うことにより、ｎ型不純物拡散領域を活性化することができる。このことによりドレイン電極７とチャネル層３との間の接触抵抗を低減することができる。また、上記ドレイン電極７は、真空蒸着法、スパッタ法などにより前記ｎ型不純物拡散領域直上に形成した後、熱処理されることができる。熱処理は、時間、温度は、限定されない。熱処理としては、例えば、５５０℃で１分間の熱処理を採用することができる。このことにより、ドレイン電極７とチャネル層３とを、ｎ型不純物拡散層を介するより良好なオーミック接続することができる。上記ｎ型不純物拡散領域に含まれるｎ型不純物は、特に限定されない。バリア層４およびチャネル層３がIII族窒化物である場合、上記ｎ型不純物拡散領域に含まれるｎ型不純物としては、例えば、Ｓｉ、Ｇｅ、Ｓｎを採用できる。

【００５８】

上記ゲート電極６は、バリア層４上に接触し、ソース電極５、ゲート電極６およびドレイン電極７の順で離間して設けられる電極である。上述のように、上記第１のトランジスタ部１１および第２のトランジスタ部１２のフィールドプレート９１，９２が、ドレイン電極７を被覆するように形成された絶縁体層８上で接触している。

【００５９】

上記ゲート電極６と、ドレイン電極７とは、一定の間隔を有するように設けられてもよい。また、ゲート電極６が有するチャネル層３に最も近い下面と、ドレイン電極７の下面は、一定の間隔を有するように設けられてもよい。上記ゲート電極６の材料としては、Ｔｉ、Ｚｒ、Ｈｆ、Ａｌ、ＡｌＳｉ、Ｗ、ＷＮ、Ａｕ、Ｐｔから選択された少なくとも一種の金属を用いることができる。上記ゲート電極６は、真空蒸着法、スパッタ法により形成することができる。上記バリア層４上に絶縁体層８を形成している場合、ゲート電極６を形成する部分の絶縁体層８をエッチングにより除去し、ゲート電極６がバリア層４に接触

するように、ゲート電極６を形成することができる。

【００６０】

図１に示すように、上記絶縁体層８は、バリア層４の上で、ソース電極５とゲート電極６の間およびゲート電極６とドレイン電極７との間に設けられることができる。上記絶縁体層８は、ドレイン電極７を覆うように形成され、絶縁体層８の上部に、フィールドプレート９１を設けることができる。

【００６１】

上記絶縁体層８は、絶縁体であれば如何なる材料からなっていても良い。上記絶縁体層８の材料としては、例えば、SiO_2、ＳｉＯＮ、ＳｉＮ、ポリイミド、TaO_x、HfO_x等を採用することができる。上記絶縁体層８は、例えばＣＶＤ法、スパッタ法、スピンオン塗布により形成することができる。

【００６２】

上記絶縁体層８の厚さは特に限定されないが、ドレイン電極７の直上部の厚さを１μｍ以上とすると良い。ドレイン電極７を接地し、トランジスタがオフの状態でドレイン電極７に高電圧を印加した場合、ドレイン電極７からドレイン電極７上部のフィールドプレート９１に向けてかかる縦方向電界の影響により、ドレイン電極７端角部に電界が集中する。そこで、上記ドレイン電極７と、フィールドプレート９１との距離を広く設計することにより、ドレイン電極７端に電界が集中することによる素子の破壊を防止することができる。

【００６３】

上記第１実施形態の電界効果トランジスタによれば、トランジスタ特性を保持したまま、フィールドプレート９１の端部周囲の絶縁破壊が起こりやすい絶縁体層８およびバリア層（半導体）４に大きな電界がかかることを抑制することができて、絶縁破壊の発生を抑制することができる。また、絶縁体層８を設けることにより、ソース電極５とゲート電極６との間の電界、およびゲート電極６とドレイン電極７との間の電界を緩和することができて、特に、チャネル層３などでの電界集中が生じるのを抑制することができる。この結果、高電圧を印加しても壊れにくい電界効果トランジスタを得ることができ、素子の破壊や信頼性の低下を抑制することができる。

【００６４】

簡潔にいうと、第１実施形態の電界効果トランジスタは、第１のトランジスタ部１１と、第２のトランジスタ部１２とを備え、その第１のトランジスタ部１１は、ヘテロ接合を含むIII族窒化物半導体層構造を有し、そのIII族窒化物半導体層構造上に、ソース電極５、ゲート電極６およびドレイン電極７がこの順で離間して設けられている。また、第１のトランジスタ部１１は、ゲート電極本体９０に接続されドレイン電極７側にひさし状に張り出し、絶縁体層８上に形成されたフィールドプレート９１を有する。

【００６５】

上記第２のトランジスタ部１２は、上記半導体層構造およびドレイン電極７が第１のトランジスタ部１１と共通で、ドレイン電極７における図１の線分Ｚを軸に鏡面対称となるように配置されている。また、互いに向かい合うように形成された第１のトランジスタ部１１および第２のトランジスタ部１２のフィールドプレート９１、９２が、ドレイン電極７を被覆するように形成された絶縁体層８上で接するように形成されている。

【００６６】

この構成によれば、トランジスタ特性を保持したまま、フィールドプレート９１，９２の端部周囲の絶縁破壊が起こりやすい絶縁体層８および半導体層に、大きな電界がかかることを抑制することができ、絶縁破壊の発生を抑制することができる。これにより、素子の破壊や信頼性の低下を抑制できる。

【００６７】

また、本発明のトランジスタにおいて、最大の絶縁体層８の厚み（図１の線分Ｘ）は１μｍ以上有しても良い。これによれば、ゲート電極６とドレイン電極７との間に電圧を印加したとき、ドレイン電極７およびゲート電極６にかかる電位差により、ドレイン電極７

の端に電界が集中することによる、絶縁破壊強度を超える電解集中を防止でき、素子の破壊を防止することができる。

【００６８】

（第２実施形態）

図２は、本発明の第２実施形態の電界効果トランジスタの構成を示す概略断面図である。

【００６９】

尚、第２実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および作用効果についても説明を省略する。

【００７０】

尚、図２において、２１２は、第２のトランジスタ部を示し、２５８は、第２のトランジスタ部２１２の第１の絶縁体層としての絶縁体層を示す。

【００７１】

図２に示すように、この電界効果トランジスタの第１トランジスタ部２１１は、ゲート電極２０６およびフィールドプレート２９１と、バリア層４の表面とのなす角度θが、鋭角、より詳しくは、略３０°に設定されている。これにより、バリア層４と接すると共にドレイン電極７側のゲート電極２０６端角部に掛かる電界の集中を緩和することができる。

【００７２】

この結果、ショットキー接合部のリーク電流や、ゲート電極２０６周囲の第１の絶縁体層としての絶縁体層２０８および半導体からなるバリア層４の絶縁破壊を防止することができる。

【００７３】

尚、上記ゲート電極２０６と、バリア層４表面とのなす角度θは、１５°～４５°に設定されると作用効果が顕著に現れて好ましい。上記絶縁体層２０８は、バリア層４およびドレイン電極７を覆うように形成されている。

【００７４】

上記絶縁体層２０８は、絶縁体層２０８の最大の厚み（図２の線分Ｘ）が１μｍ以上になるように形成されている。言い換えれば、III族窒化物半導体層構造の上面の法線方向において、第１のトランジスタ部２１１のフィールドプレート２９１と、上記III族窒化物半導体層構造との最大の距離は、１ミクロン以上になっている。

【００７５】

第２実施形態の電界効果トランジスタによれば、ゲート電極２０６と、半導体からなるバリア層４とのショットキー接合部のリーク電流や、ゲート電極２０６の周囲の絶縁体層２０８およびバリア層４の絶縁破壊を防止することができるため、高電圧を印加しても壊れにくい電界効果トランジスタを得ることができる。

【００７６】

尚、第２実施形態は、ゲート電極２０６およびフィールドプレート２９１が斜めの斜めゲートを示す実施形態である。

【００７７】

斜めゲートを有する本発明の電界効果トランジスタでは、バリア層からゲート電極またはゲート電極に接続されたフィールドプレートまでの高さは、ドレイン電極方向に向かうに従い、連続的に変化しても良い。これにより、バリア層と接しドレイン側のゲート電極端角部に掛かる電界の集中を緩和することができ、ショットキー接合部のリーク電流や、ゲート電極周囲の絶縁膜およびバリア層（半導体）の絶縁破壊を防止することができる。

【００７８】

（第３の実施形態）

図３は、本発明の第３実施形態の電界効果トランジスタの構成を示す概略断面図である。

【００７９】
尚、第３実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および作用効果についても説明を省略する。
【００８０】
尚、図３において、３１２は、第２のトランジスタ部を示し、３５８は、第２のトランジスタ部３１２の第１の絶縁体層としての絶縁体層を示し、３９２は、第２のトランジスタ部３１２のフィールドプレートを示す。
【００８１】
第３実施形態の電界効果トランジスタは、ゲート電極３０６の一部をなすフィールドプレート３９１が、二段フィールドプレート構造を有している。ゲート電極３０６側の一段目のフィールドプレートを直上部に形成する絶縁層（図３のＹ部）は、幅が０．５～３μｍ、高さが１０～５０ｎｍに設定されている。また、２段目のフィールドプレートを上部に形成する絶縁層３０８の最大の厚み（図３の線分Ｘ）は、１μｍ以上に設定されている。
【００８２】
より詳しくは、第１のトランジスタ部３１１のフィールドプレート３９１は、III族窒化物半導体層構造の上面３１８に略平行な状態で、その上面３１８にその上面３１８の法線方向に対向する第１の面３１９を有する第１部分３２０と、その法線方向において、第１部分３２０の上記III族窒化物半導体層構造側とは反対側に位置すると共に、上記上面３１８に略平行な状態で上記上面３１８に上記法線方向に対向する第２の面３２９を有する第２部分３３０と、第１部分３２０と第２部分３３０とを連結する連結部３３１とを有する。
【００８３】
上記第１部分３２０の上記法線方向に垂直な方向の長さは、０．５μｍ以上かつ３μｍ以下になっている。簡単に表現すると、第１部分３２０の延在方向の長さは、０．５μｍ以上かつ３μｍ以下になっている。また、上記第１の面３１９と上記上面３１８との上記法線方向の距離が、１０μｍ以上かつ５０μｍ以下になっている。
【００８４】
上記第３実施形態の電界効果トランジスタによれば、バリア層４と接するドレイン電極７側のゲート電極３０６の端角部にかかる電界の集中を、より効果的に抑制することができる。したがって、上記ゲート電極３０６と、半導体からなるバリア層４とにおけるショットキー接合部のリーク電流や、ゲート電極周囲の絶縁体層３０８および半導体層での絶縁破壊を、より効果的に防止することができる。この結果、高耐圧を印加しても壊れにくい電界効果トランジスタを得ることができる。
【００８５】
尚、第３実施形態は、薄いゲートＦＰを示す実施形態である。上述のように、第３実施形態の電界効果トランジスタにおいて、ゲート電極３０６の一部をなすフィールドプレート３９１、３９２は、二段構造を有する。また、ゲート電極側の一段目のフィールドプレートを直上部に形成する絶縁層（図３のＹ部）は幅が０．５～３μｍ、高さが１０～５０ｎｍを有し、２段目のフィールドプレートを上部に形成する絶縁層３０８の最大の厚み（図３の線分Ｘ）は１μｍ以上を有する。このことにより、バリア層４と接しドレイン電極７側のゲート電極３０６の端に掛かる電界の集中を、より効果的に抑制することができ、ゲート電極（金属）３０６とバリア層（半導体）４におけるショットキー接合部のリーク電流や、ゲート電極３０６の周囲の絶縁体層３０８および半導体層での絶縁破壊を、より効果的に防止することができる。
【００８６】
（第４の実施形態）
図４は、本発明の第４実施形態の電界効果トランジスタの構成を示す概略断面図である。

【００８７】
尚、第４実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および作用効果についても説明を省略する。
【００８８】
尚、図４において、４０６は、第１のトランジスタ部４１１のゲート電極を示し、４９１は、第１のトランジスタ部４１１のフィールドプレートを示し、４１２は、第２のトランジスタ部を示す。また、４５６は、第２のトランジスタ部４１２のゲート電極を示し、４５８は、第２のトランジスタ部４１２の第１の絶縁体層としての絶縁体層を示し、４８２は、第２のトランジスタ部４１２の上部絶縁体層を示す。また、４８３は、第２のトランジスタ部４１２の下部絶縁体層を示し、４９２は、第２のトランジスタ部４１２のフィールドプレートを示す。
【００８９】
第４実施形態の電界効果トランジスタの基本構造は、図１と同様であるが、バリア層４上の絶縁体膜）が、二層構造を有している。すなわち、第４実施形態では、第１のトランジスタ部４１１の第１の絶縁体層としての絶縁体層４０８は、誘電率が互いに異なる二つの層４８０，４８１を有している。
【００９０】
二層絶縁体構造は、例えば、SiN_x、SiO_2をこの順で設けてなる。二層絶縁体構造により、バリア層４と、上部絶縁体層４８０の下方に位置する下部絶縁体層４８１との界面における界面準位の低減と、絶縁体層４０８における絶縁破壊耐圧の向上とを、同時に実現することが可能になる。これにより、良好なスイッチング特性を持った高耐圧トランジスタを得ることができる。尚、この発明では、第１の絶縁体層は、誘電率の異なる複数の層を備えていてもよい。例えば、第１の絶縁体層は、Al_2O_3、Ga_2O_3、HfO_x、SiN_x、SiO_2、SiON、TaO_x、ZrO_2などを有し、誘電率の異なる多層構造であっても良い。
【００９１】
上記第４実施形態の電界効果トランジスタによれば、良好な絶縁特性を得ることができると共に、トランジスタを高耐圧なものにすることができ、スイッチング特性を良好なものにすることができる。
【００９２】
（第５の実施形態）
図５は、本発明の第５実施形態の電界効果トランジスタの構成を示す概略断面図である。
【００９３】
尚、第５実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および作用効果についても説明を省略する。
【００９４】
第５実施形態は、ＭＩＳを示す実施形態である。尚、図５において、５１２は、第２のトランジスタ部を示している。
【００９５】
第５実施形態の電界効果トランジスタは、第１のトランジスタ部５１１が、上側絶縁体層５８１の他に、ゲート電極５０６とバリア層４との間に下側絶縁体層５８２を備えている。これにより、トランジスタオフの状態でソース電極５を接地し、ドレイン電極７に高電圧を印加した際に、ゲート電極５０６と二次元電子ガス２０との間で、バリア層４を介して流れるリーク電流を抑制することができるため、良好なゲート絶縁特性を得ることができる。
【００９６】
上記下側絶縁体層５８２において、ゲート電極５０６と、第１のトランジスタ部５１１

のIII族窒化物半導体層構造の上面との間に位置する部分、すなわち、下側絶縁体層５８２において、ゲート電極５０６と、第１のトランジスタ部５１１のIII族窒化物半導体層構造の上面とで挟まれている部分は、第２の絶縁体層を構成する。また、上記下側絶縁体層５８２のその部分以外の部分と、上側絶縁体層５８１とは、第１の絶縁体層を構成している。

【００９７】

尚、上記下側絶縁体層５８２は、絶縁体であれば特に限定されない。上記下側絶縁体層５８２は、例えば、Al_2O_3、Ga_2O_3、HfO_x、SiN_x、SiO_2、SiON、TaO_x、ZrO_2膜で構成されることができる。また、上記下側絶縁体層５８２は、チャネル層３またはバリア層４の酸化膜を用いてもよい。また、上記下側絶縁体層５８２は、上側絶縁体層５８１と同一であってもよい。

【００９８】

また、上記下側絶縁体層５８２の厚さは、特に限定されない。上記下側絶縁体層５８２の膜厚は、例えば、０．０１μｍ～０．１μｍとすることができる。上記下側絶縁体層５８２は、例えば、ＣＶＤ法、スパッタ法により形成することができる。第５実施形態の電界効果トランジスタによれば、良好なゲート絶縁特性を獲得することができる。

【００９９】

（第６実施形態）

図６は、本発明の第６実施形態の電界効果トランジスタの構成を示す概略断面図である。

【０１００】

尚、第６実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および作用効果についても説明を省略する。尚、図６において、６２０は、二次元電子ガスを示し、６８１は、第１のトランジスタ部６１１の上側絶縁体層を示し、６１２は、第２のトランジスタ部を示す。

【０１０１】

第６実施形態のトランジスタは、第１のトランジスタ部６１１が、上層チャネル層６３１と下層チャネル層６３２から構成されたチャネル層６０３を有する。

【０１０２】

上記上層チャネル層６３１は、バリア層６０４および下層チャネル層６３２のいずれよりも小さいバンドギャップを有している。また、バリア層６０４および上層チャネル層６３１の一部をエッチングすることによるリセス構造を有し、ゲート電極６０６は、リセス構造の凹部６９９上に下側絶縁体層６８２を介して設けられている。

【０１０３】

上記第６実施形態の電界効果トランジスタによれば、ゲート電極６０６直下の上層チャネル層６３１には二次元電子ガス６２０を形成できないから、ゲート電極６０６に電圧を印加しない場合、ソース電極５とドレイン電極７の間にはほとんど電流が流れない。また、上記ゲート電極６０６にプラスの電圧を印加することにより、ゲート電極６０６の直下の上層チャネル層６３１に電子層を形成することができ、トランジスタをオンとすることができる。これにより、ゲート絶縁特性の優れたノーマリーオフ型のトランジスタを作成することができる。

【０１０４】

また、上記第６実施形態の電界効果トランジスタによれば、キャリアである電子の大部分が上層チャネル層６３１に閉じ込められるようなバンド構造となるので、電子が下層チャネル層６３２、バッファ層２、および基板１を介して移動することによるリーク電流を低減できる。この結果、ソース電極５とドレイン電極７の間を流れる電流を上層チャネル層６３１に集中して流すことができる。

【０１０５】

尚、上層チャネル層６３１の材料は、特に限定されないが、上層チャネル層６３１の材

料としては、例えば、III族窒化物半導体である、ＧａＮ、$Al_xGa_{1-x}N$、$In_xGa_{1-x}N$等を用いることができる。尚、ここで、例えば、ｘは、０より大きく０．５より小さくてもよい。また、例えば、ｘは、０．００１以上０．１以下であってもよい。

【０１０６】

また、上記上層チャネル層６３１の厚さは特に限定されないが、例えば、０．０１μｍ以上０．１μｍ以下である。また、例えば、０．０１μｍ以上０．０５μｍ以下である。また、上記上層チャネル層６３１の厚さは、下層チャネル層６３２の厚さより小さくてもよい。このことにより、キャリアである電子を、より狭い範囲に閉じ込めることができる。

【０１０７】

上記下層チャネル層６３２の材料は、特に限定されない。上記下層チャネル層６３２の材料は、例えば、III族窒化物半導体である、$Al_xGa_{1-x}N$、$In_xGa_{1-x}N$などからなってもよい。尚、ここで、例えば、ｘは、０．０１以上０．５以下でもよい。また、例えば、ｘは、０．０２以上０．２以下であってもよい。また、例えば、上記上層チャネル層６３１がＧａＮからなるとき、下層チャネル層６３２は、$Al_xGa_{1-x}N$（$0.01 \leqq x \leqq 0.2$）からなっていてもよい。また、例えば、上記上層チャネル層６３１が、ＧａＮ又は$Al_xGa_{1-x}N$からなり、下層チャネル層６３２が$Al_yGa_{1-y}N$ならなるとき、ｙはｘより大きくてもよい。この場合、上記上層チャネル層６３１のバンドギャップは、下層チャネル層６３２のバンドギャップより大きくなるからである。また$0.01 \leqq (y-x) \leqq 0.2$であってもよい。

【０１０８】

上記下層チャネル層６３２の厚さは、特に限定されないが、例えば、１～１０μｍであり、さらに好ましくは、２μｍ～５μｍである。

なお、ゲート電極６０６は、リセス構造を有するバリア層６０４の凹部６９９の上に設けることもできる。上記下側絶縁体層６８２は、基板の法線方向において、バリア層６０４とゲート電極６０６との間に設けることもできる。

【０１０９】

上記第６実施形態の電界効果トランジスタによれば、良好なピンチオフ特性をもったノーマリオフ型のトランジスタを実現することができる。

【０１１０】

上述のように、第６実施形態は、ゲートリセス構造を示す実施形態である。すなわち、上記バリア層６０４またはチャネル層６０３は、リセス構造を有し、ゲート電極６０６は、リセス構造の凹部６９９上に設けられてもよい。この構成により、本発明のトランジスタは、良好なスイッチング特性を得ることができる。また、ゲート電極６０６とバリア層６０４またはチャネル層６０３との間に第２の絶縁体層６８８をさらに備え、かつチャネル層３をリセス構造とすることにより、ゲート絶縁特性の優れたノーマリオフ型のトランジスタとすることができる。

【０１１１】

（第７実施形態）

図７は、本発明の第７実施形態の電界効果トランジスタの構成を示す概略断面図である。第７実施形態は、ソースＦＰを有する実施形態である。

【０１１２】

尚、第７実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および作用効果についても説明を省略する。

【０１１３】

第７実施形態の電界効果トランジスタの第１のトランジスタ部７１１は、ヘテロ接合を含むIII族窒化物半導体層構造を備え、その半導体層構造上に、ソース電極７０５のソース電極本体７９０、ゲート電極７０６およびドレイン電極７０７がその順で離間して設けられている。

【０１１４】
この電界トランジスタは、第１のトランジスタ部７１１と、第２のトタンジスタ部７１２とを備える。上記第１のトランジスタ７１１部のソース電極７０５は、ソース電極本体７９０と、フィールドプレート７９１とを有し、フィールドプレート７９１は、ソース電極本体７９０につながると共に、ドレイン電極７０７側にひさし状に張り出している。
【０１１５】
上記第２トランジスタ７１２部のIII族窒化物半導体層構造は、第１のトランジスタ７１１部のIII族窒化物半導体層構造と一体化され、第２トランジスタ７１２部のドレイン電極５７は、第１のトランジスタ部７１１のドレイン電極７と一体化されている。また、上記第２のトランジスタ部７１２の第１の絶縁体層としての絶縁体層７５８は、第１のトランジスタ部７１１の第１の絶縁体層としての絶縁体層７０８と一体化されている。上記第１のトランジスタ部７１１と第２のトランジスタ部７１２とは、図７において、一体化されたドレイン電７，５７の垂直二等分線（図７にＺで示す）に対して線対称な形状をしており、二等分線Ｚに対して、鏡面対称となるように配置されている。
【０１１６】
互いに向かい合うように形成された第１のトランジスタ部７１１および第２のトランジスタ部７１２のフィールドプレート７９１、７９２は、一体化されたゲート電極７０６，７５６および一体化されたドレイン電極７，５７を被覆するように形成された一体化された絶縁体層７０８，７５８上で接触している。
【０１１７】
上記第１のトランジスタ部７１１は、ヘテロ接合を含むIII族窒化物半導体層構造と、上記III族窒化物半導体層構造上に間隔をおいて配置されたソース電極本体７９０およびドレイン電極７と、ソース電極本体７９０とドレイン電極７との間に、ソース電極本体７９０およびドレイン電極７に間隔をおいて位置するゲート電極７０６とを有する。
【０１１８】
また、上記第１のトランジスタ部７１１は、上記III族窒化物半導体層構造の上面の法線方向において上記III族窒化物半導体層構造側とは反対側かつ上記法線方向に垂直な方向においてドレイン電極７側に延在するフィールドプレート７９１と、上記III族窒化物半導体層構造上に、ドレイン電極７およびゲート電極７０６を被覆するように配置された第１の絶縁体層としての絶縁体層７０８とを有する。
【０１１９】
上記第２のトランジスタ部７１２は、一体化されたドレイン電極７，５７の垂直二等分面に対して第１トランジスタ部７１２と略面対称に位置する。上記第１のトランジスタ部７１１のフィールドプレート７９１と、第２のトランジスタ７１２部のフィールドプレート７９２とは、一体化された絶縁体層７０８，７５８上で接触している。
【０１２０】
上記第７実施形態の電界効果トランジスタは、第１実施形態の電界効果トランジスタとの比較において、ゲートフィールドプレート７９１，７９２の端角部で電界集中が起こってしまう。しかし、図１２に示す従来の電界効果トランジスタと比較すると、上記ゲートフィールドプレート７９１，７９２の端角部周囲での電界集中を緩和することができる。また、素子の最表面がソース電極７０５，７５５になるため、ダイボンド、ワイヤーボンドまたはパッケージング等のトランジスタの後半の実装工程を格段に容易に行うことが可能になる。
【０１２１】
（第８実施形態）
図８は、本発明の第８実施形態の電界効果トランジスタの構成を示す概略断面図である。
【０１２２】
尚、第８実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および

作用効果についても説明を省略する。尚、図８において、８１２は、第２のトランジスタ部を示し、８８１は、第１のトランジスタ部８１２の第１の絶縁体層の上部絶縁体層を示し、８８２は、第１のトランジスタ部８１２の第１の絶縁体層の下部絶縁体層を示す。

【０１２３】

第８実施形態の電界効果トランジスタは、第１のトランジスタ部８１１のゲート電極８０６の一部をなすフィールドプレート８９１が、ドレイン電極７の直上部を覆わないように形成されている。

【０１２４】

第８実施形態の電界効果トランジスタは、第１実施形態の電界効果トランジスタと比較した場合、第１のトランジスタ部８１１のゲート電極８０６のフィールドプレート８９１の端角部が存在するため電界集中が起こってしまう。

【０１２５】

しかし、図１２に示すような従来の電界効果トランジスタと比較した場合、のトランジスタ部８１１のゲート電極８０６の端角部への電界集中を緩和することができ、周囲部での素子の破壊を抑制することができる。

【０１２６】

また、トランジスタが環状に形成されている場合、穴の存在によって、ドレイン電極をトランジスタの上部から引き出すことができるため、ワイヤーボンドやダイボンドといった実装工程を容易に行うことができる。

【０１２７】

尚、第８実施形態は、ダブルヘテロ構造と、穴開きゲートを示す実施形態である。

【０１２８】

すなわち、第８実施形態では、第１のトランジスタ部８１１のチャネル層８０３は、上層チャネル層８３１と下層チャネル層８３２からなり、上層チャネル層８３１は、バリア層８０４および下層チャネル層８３２のいずれよりも小さいバンドギャップを有してもよい。このことにより、第１のトランジスタ部８１１のソース電極８０５と、第１のトランジスタ部８１１のドレイン電極８０７との間を流れる電流を、上層チャネル層８３１に集中して流すことができ、リーク電流を低減することができる。

【０１２９】

また、第８実施形態では、第１のトランジスタ部８１１のゲート電極８０６の一部をなすフィールドプレート８９１は、ドレイン電極８０７の直上部に形成されていない。このことにより、ワイヤーボンドやダイボンドといった実装工程を格段に容易に行うことができる。

【０１３０】

（第９の実施形態）

図９は、本発明の第９実施形態の電界効果トランジスタの構成を示す概略断面図である。

【０１３１】

尚、第９実施形態においては、第１実施形態と同一の構成については、第１実施形態と同一の参照番号を付して詳細な説明を省略する。また、第１実施形態と同一の構成および作用効果についても説明を省略する。尚、図９において、９１２は、第２のトランジスタ部を示し、９９２は、第２のトランジスタ部９１２のフィールドプレートを示し、９８１は、第１のトランジスタ部９１２の第１の絶縁体層の上部絶縁体層を示し、９８２は、第１のトランジスタ部９１２の第１の絶縁体層の下部絶縁体層を示す。

【０１３２】

第９実施形態の電界効果トランジスタは、第１のトランジスタ部９１１のゲート電極９０６の一部をなすフィールドプレート９９１が、第１のトランジスタ部９１１のドレイン電極７の直上部を覆わないように形成されている。

【０１３３】

第９実施形態の電界効果トランジスタは、第１実施形態の電界効果トランジスタと比較

した場合、ゲートフィールドプレート９９１の端角部が存在することに起因する電界集中が起こってしまう。

【０１３４】

しかし、図１２に示すような従来の電界効果トランジスタと比較した場合、ゲート電極９９１の端角部への電界集中を緩和することができ、周囲部での素子の破壊を抑制することができる。

【０１３５】

また、トランジスタが環状に形成されている場合、第１のトランジスタ部９１１のドレイン電極７をトランジスタの上部から引き出すことができるため、ワイヤーボンドやダイボンドといった実装工程を容易に行うことができる。

【０１３６】

尚、第９実施形態は、穴開きゲートを示す実施形態である。第９実施形態のように、ゲート電極９０６の一部をなすフィールドプレート９９１は、ドレイン電極７の直上部に形成しなくても良い。このことにより、ワイヤーボンドやダイボンドといった実装工程を容易にすることができる。

【０１３７】

以下、従来例の電界効果トランジスタと、本発明の電界効果トランジスタとの物理量のシミュミレーション結果を示し、本発明の電界効果トランジスタの優位性について説明する。

【０１３８】

先ず、従来の電界効果トランジスタについてのシミュレーション結果について説明する。

【０１３９】

図１２に示す従来の電界効果トランジスタについて、トランジスタ内部の電界強度分布を調べるシミュレーションを行った。

【０１４０】

シミュレーションの条件としては、バッファ層１２０２およびチャネル層１２０３を厚さ５μｍのＧａＮ層、バリア層１２０４を厚さ０．０２５μｍの$Al_{1-x}Ga_xN$（ｘ＝０．２０）層とした。

【０１４１】

また、ソース電極１２０５とゲート電極１２０６との間、および、ゲート電極１２０６とドレイン電極１２０７との間にSiN_xからなる絶縁体層１２０８を設けた。上記ゲート電極１２０６の基部から１μｍのフィールドプレートを延在させ、そのフィールドプレートは、絶縁体層１２０８上に位置するようにした。また、ソース電極１２０５とゲート電極１２０６との間隔を１μｍとし、ゲート電極１２０６とドレイン電極１２０７との間隔を６μｍとした。

【０１４２】

また、チャネル層１２０３とバリア層１２０４との界面に生じる二次元電子ガス１２２０のシートキャリア濃度を$1\times10^{13}\ cm^{-2}$とした。

【０１４３】

また、基板１２０１を導電性基板とし、基板１２０１とソース電極１２０５とを電気的に接続し、接地した。また、ゲート電極１２０６には－１０Ｖの電圧印加し、ドレイン電極１２０７には＋６００Ｖの電圧を印加したこととした。

【０１４４】

図１０Ａは、従来の電界効果トランジスタについて行ったシミュレーション結果であり、トランジスタ内部のポテンシャル（電位）分布を示す図である。また、図１０Ｂは、従来の電界効果トランジスタについて行ったシミュレーション結果であり、トランジスタ内部の電界強度分布である。尚、図１０Ａのポテンシャル分布の間隔が密な場所ほど、図１０Ｂの電界強度は大きくなる。

【０１４５】

従来例では、図１０Ａに示すように、バリア層１２０４と接触しているドレイン電極１２０７側のゲート電極端角部（図１２のＡ部）だけでなく、ドレイン電極１２０７との距離が最も短くなるフィールドプレート１２９１，１２９２の端角部（図１２のＢ部）でも、電界集中が生じていることがわかる。

【０１４６】

図１０の最も電界の集中しているＢ部における絶縁破壊強度を計算すると、Ｂ部の下側の絶縁膜において１５．９ＭＶ／ｃｍの電界集中が起こることがわかった。シミュレーションに用いた絶縁膜である一般的なSiN_xの絶縁破壊電界強度は、およそ９ＭＶ／ｃｍであることから、図１０のＢ部付近で、絶縁破壊が起こってしまうことがわかる。

【０１４７】

次に、本発明の電界効果トランジスタについてのシミュレーション結果について説明する。

【０１４８】

図１に示す第１実施形態の電界効果トランジスタについて、トランジスタ内部の電界強度分布を調べるシミュレーションを行った。

【０１４９】

シミュレーションの条件としては、バッファ層２およびチャネル層３を厚さ５μｍのＧａＮ層、バリア層４を厚さ０．０２５μｍの$Al_{1-x}Ga_xN$（ｘ＝０．２０）層とした。また、バリア層４およびドレイン電極７上部にSiN_xからなる第１の絶縁体層としての絶縁体層８を設けたこととした。また、絶縁体層８の厚みをドレイン電極７の直上部において１μｍとした。また、ソース電極５とゲート電極６との間隔を１μｍとし、ゲート電極７とドレイン電極７との間隔を６μｍとした。

【０１５０】

また、チャネル層３とバリア層４との界面に生じる二次元電子ガス２０のシートキャリア濃度を$2\times10^{12}cm^{-2}$とした。

【０１５１】

また、基板１を導電性基板とし、基板１とソース電極６とを電気的に接続し、接地した。また、ゲート電極６には－１０Ｖの電圧印加し、ドレイン電極７には＋６００Ｖの電圧を印加した。

【０１５２】

図１１Ａは、本発明の電界効果トランジスタについて行ったシミュレーション結果であり、電界効果トランジスタを構成する第１のトランジスタ部７１１に関するシミュレーション結果である。図１１Ａは、トランジスタ内部のポテンシャル（電位）分布である。

【０１５３】

また、図１１Ｂは、本発明の電界効果トランジスタについて行ったシミュレーション結果であり、電界効果トランジスタを構成する第１のトランジスタ部７１１に関するシミュレーション結果である。図１１Ｂは、トランジスタ内部の電界強度分布である。

【０１５４】

尚、図１１Ａのポテンシャル分布の間隔が密な場所ほど、図１１Ｂの電界強度は大きくなる。

【０１５５】

第１実施形態では、図１１Ｂに示すように、バリア層４と接触しているドレイン電極７側のゲート電極６の端角部（図１１ＡのＡ部）と、ドレイン電極７のゲート電極６側のチャネル層３およびバリア層４付近（図１１ＡのＤ部）で電界集中が起きているのがわかる。図１１Ｂに示すように、この角部のドレイン電極７側において７．１ＭＶ／ｃｍの電界集中が起こる。しかし、角部の周囲を構成するSiN_x層の絶縁破壊電界強度は、およそ９ＭＶ／ｃｍであることから、この付近では、この条件においては絶縁破壊が起こらない。

【０１５６】

また、図１１Ｂに示すように、ドレイン電極７のゲート電極６側のチャネル層３および

バリア層４付近（図１１ＡのＤ部）において、４．９ＭＶ／ｃｍの電界集中が起こることがわかった。チャネル層３であるＧａＮおよびバリア層４であるＡｌＧａＮの絶縁破壊電界強度は、およそ５ＭＶ／ｃｍであることから、この付近では、この条件においては絶縁破壊が起こらない。

【０１５７】

以上の結果から、従来の電界効果トランジスタではフィールドプレートの端角部で絶縁破壊が生じ素子の破壊を起こしてしまう条件において、本発明の電界効果トランジスタでは絶縁破壊が起こることはなく、素子の破壊を防止することができることがわかる。

【０１５８】

尚、第１実施形態のシミュレーション結果と、略同様のシミュレーション結果を、第２実施形態乃至第９実施形態でも得ている。

【０１５９】

また、この発明が、第１乃至第９実施形態のうちの２以上の構成を有していても良いことは、言うまでもない。また、その場合に、その発明が、対応する２以上の作用効果を奏することができることも言うまでもない。

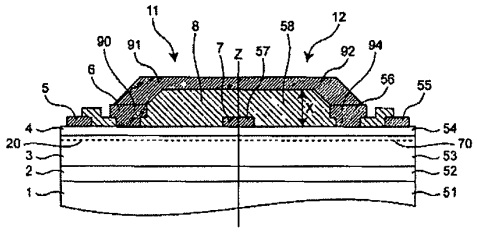
【符号の説明】

【０１６０】

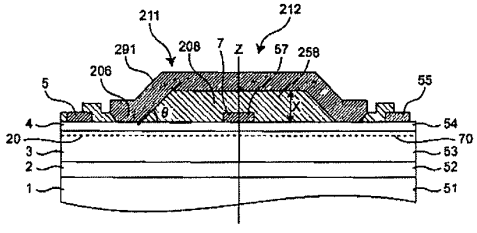
１　第１のトランジスタ部の基板
２　第１のトランジスタ部のバッファ層
３，６０３　第１のトランジスタ部のチャネル層
４，６０４，８０４　第１のトランジスタ部のバリア層
５，７０５，８０５　第１のトランジスタ部のソース電極
６，２０６，３０６，４０６，５０６，６０６，７０６，８０６，９０６　第１のトランジスタ部のゲート電極
７，８０７　第１のトランジスタ部のドレイン電極
８，２０８，３０８，４０８，７０８　第１のトランジスタ部の第１の絶縁体層に相当する絶縁体層
１１，２１１，３１１，４１１，５１１，６１１，７１１，８１１，９１１　第１のトランジスタ部
１２，２１２，３１２，４１２，５１２，６１２，７１２，８１２，９１２　第２のトランジスタ部
２０，６２０，８２０　第１のトランジスタ部の二次元電子ガス
５１　第２のトランジスタ部の基板
５２　第２のトランジスタ部のバッファ層
５３　第２のトランジスタ部のチャネル層
５４　第２のトランジスタ部のバリア層
５５，７５５　第２のトランジスタ部のソース電極
５６，４５６，７５６　第２のトランジスタ部のゲート電極
５７　第２のトランジスタ部のドレイン電極
５８，２５８，３５８，４５８，７５８　第２のトランジスタ部の第１の絶縁体層に相当する絶縁体層
７０　第２のトランジスタ部の二次元電子ガス
９０　第１のトランジスタ部のゲート電極本体
９１，２９１，３９１，４９１，７９１，８９１，９９１　第１のトランジスタ部のフィールドプレート
９２，３９２，４９２，７９２，８９２，９９２　第２のトランジスタ部のフィールドプレート
９４　第２のトランジスタ部のゲート電極本体
３１８　III族窒化物半導体層構造の上面
３１９　第１のトランジスタ部のフィールドプレートの第１部分の第１の面

３２０　第１のトランジスタ部のフィールドプレートの第１部分
３２９　第１のトランジスタ部のフィールドプレートの第２部分の第２の面
３３０　第１のトランジスタ部のフィールドプレートの第２部分
３３１　第１のトランジスタ部のフィールドプレートの連結部
４８０，８８１，９８１　第１のトランジスタ部の第１の絶縁体層の上部絶縁体層
４８１，８８２，９８２　第１のトランジスタ部の第１の絶縁体層の下部絶縁体層
４８２　第２のトランジスタ部の第１の絶縁体層の上部絶縁体層
４８３　第２のトランジスタ部の第１の絶縁体層の下部絶縁体層
５８１，６８１　第１のトランジスタ部の上側絶縁体層
５８２，６８２　第１のトランジスタ部の下側絶縁体層
６３１，８３１　第１のトランジスタ部の上層チャネル層
６３２，８３２　第１のトランジスタ部の下側チャネル層
６９９　第１のトランジスタ部の凹部
７９０　第１のトランジスタ部のソース電極本体

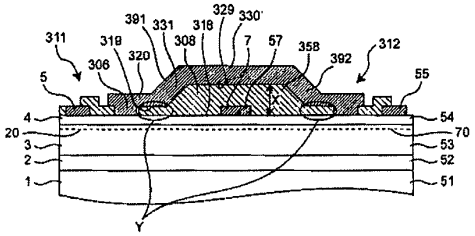
【図１】



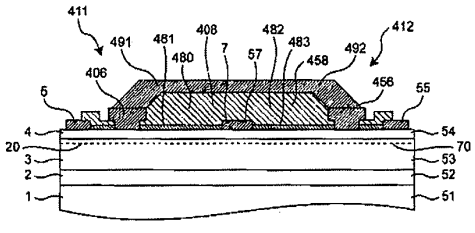
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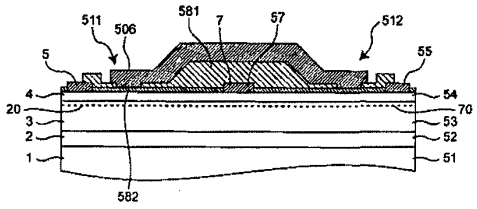
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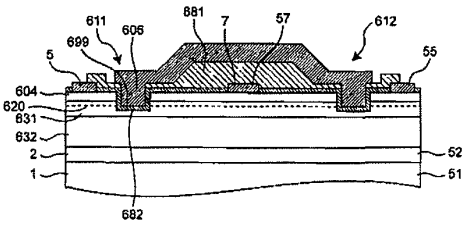
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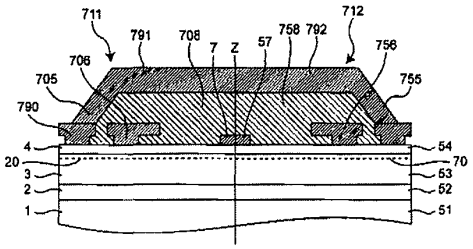
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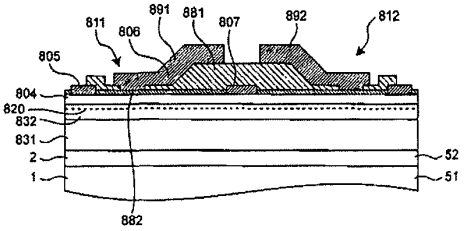
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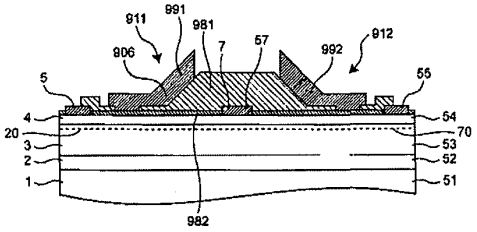
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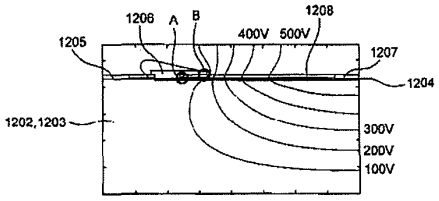
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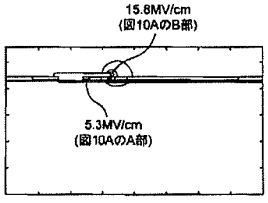
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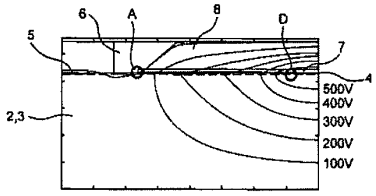
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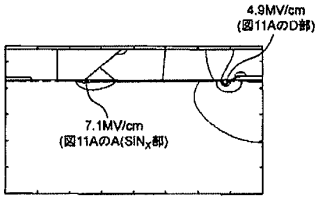
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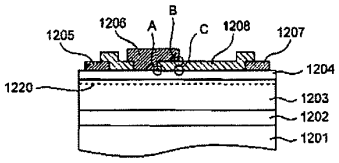
【図１１Ａ】



【図１１Ｂ】



【図１２】



フロントページの続き

(51)Int.Cl.		F I	テーマコード（参考）
H01L	*21/28*	*(2006.01)*	
H01L	*29/41*	*(2006.01)*	

Fターム(参考) 4M104 AA04 BB02 BB03 BB06 BB09 BB13 BB14 BB18 BB33 DD15
DD16 DD17 DD18 DD20 DD34 DD37 DD79 FF01 FF06 FF10
FF13 GG12 GG18
5F102 FA01 GA01 GB01 GC01 GD01 GD10 GJ02 GJ03 GJ04 GJ10
GK04 GK08 GL04 GL08 GL16 GM04 GN04 GQ01 GR04 GR06
GR12 GS03 GS04 GS06 GT02 GT03 GT05 GT06 GV06 GV07
GV08 GV09 HC01 HC11 HC15

Docket No.: E0101.0032
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit:

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: N/A

REQUEST FOR CORRECTED FILING RECEIPT

Office of Initial Patent Examination
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants hereby request that a corrected Filing Receipt be issued in connection with the above-identified patent application. The Domestic Application was omitted from the official Filing Receipt received by Applicants. The Domestic Application should read as the following:

This appln claims benefit of 61/860,976 08/01/2013

The official Filing Receipt received by Applicant has an incorrect title. The title should read as the following:

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

A marked-up copy of the official Filing Receipt showing the error and necessary correction is attached.

Applicant additionally requests that all pertinent U.S. Patent and Trademark Office records relating to the subject application be changed to reflect this correction.

Dated: January 23, 2015

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
1825 Eye Street NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/447,069	07/30/2014	2811	730	E0101.0032.US	16	3

CONFIRMATION NO. 7150

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

FILING RECEIPT

OC000000070079080

Date Mailed: 08/07/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jianjun Cao, Torrance, CA;
Alexander Lidow, Marina Del Rey, CA;
Alana Nakata, Redondo Beach, CA;

Applicant(s)

Efficient Power Conversion Corporation, ElSegundo, CA

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Applications for which benefit is claimed - ~~**None.**~~ This appln claims benefit of 61/860,976 08/01/2013
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/07/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/447,069**

Projected Publication Date: 02/04/2016

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

Title

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Electronic Acknowledgement Receipt	
EFS ID:	21298362
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Deborah Proctor
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	23-JAN-2015
Filing Date:	30-JUL-2014
Time Stamp:	18:02:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		E01010032.pdf	2205240 829312d606bdc7e636a20967821d95d74250915c	yes	39

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	3
	Other Reference-Patent/App/Search documents	4	5
	Foreign Reference	6	34
	Request for Corrected Filing Receipt	35	39
Warnings:			
Information:			
	Total Files Size (in bytes):	2205240	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: E0101.0032
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jianjun Cao et al.

Application No.: 14/447,069 Confirmation No.: 7150

Filed: July 30, 2014 Art Unit: N/A

For: GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

Pursuant to 37 C.F.R. § 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 C.F.R. § 1.97(b)(3)).

The references listed on the attached PTO/SB/08 form were cited in the enclosed International Search Report, issued in connection with corresponding International Application No. PCT/US2014/048826.

A summary/abstract translation of the non-English language references is enclosed.

In accordance with 37 C.F.R. § 1.98(a)(2)(ii), Applicant has not submitted copies of U.S. patents and U.S. patent applications. Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. E0101.0032.

Dated: January 23, 2015

Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/447,069

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	16 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/447,069	07/30/2014	2811	730	E0101.0032.US	16	3

CONFIRMATION NO. 7150

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

FILING RECEIPT



Date Mailed: 08/07/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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Applicant(s)

Efficient Power Conversion Corporation, ElSegundo, CA

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/07/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/447,069**

Projected Publication Date: 02/04/2016

Non-Publication Request: No

Early Publication Request: No
** **SMALL ENTITY** **

Title

GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PTO/AIA/15 (03-13)
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UTILITY PATENT APPLICATION TRANSMITTAL

(ONLY FOR NEW NONPROVISIONAL APPLICATIONS UNDER 37 CFR 1.53(B))

Attorney Docket No.	E0101.0032.US
First Named Inventor	Jianjun Cao
Title	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS
Express Mail Label No.	

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. [ ] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [X] **Specification** [*Total Pages* 15]
   Both the claims and abstract must start on a new page.
   (See MPEP § 608.01(a) for information on the preferred arrangement)
5. [ ] **Drawing(s)** *(35 U.S.C. 113)* [*Total Sheets* 6]
6. **Inventor's Oath or Declaration** [*Total Pages* 3]
   (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))
   a. [X] Newly executed (original or copy)
   b. [ ] A copy from a prior application (37 CFR 1.63(d))
7. [X] **Application Data Sheet** **See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. [ ] **CD-ROM or CD-R** In duplicate, large table, or Computer Program *(Appendix)*
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, items a. – c. are required)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

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ACCOMPANYING APPLICATION PARTS

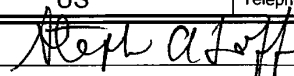
10. [ ] **Assignment Papers** (cover sheet & document(s))
    Name of Assignee
11. [ ] **37 CFR 3.73(c) Statement** *(when there is an assignee)* [X] **Power of Attorney**
12. [ ] **English Translation Document** *(if applicable)*
13. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** *(MPEP § 503) (Should be specifically itemized)*
16. [ ] **Certified Copy of Priority Document(s)** *(if foreign priority is claimed)*
17. [ ] **Nonpublication Request** Under 35 U.S.C.122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [ ] Other:

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

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Signature		Date	July 30, 2014
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DSMDB-3274268 v1

Application Data Sheet

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Correspondence Information

Correspondence Customer Number::	24998

Application Information

Application Type::	Regular
Subject Matter::	Utility
CD-ROM or CD-R?::	None
Sequence submission?::	None
Computer Readable Form (CRF)?::	No
Title::	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

Attorney Docket Number::	E0101.0032.US
Request for Early Publication?::	No
Request for Non-Publication?::	No
Total Drawing Sheets:	6
Small Entity?::	Yes
Petition included?::	No
Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2::	No
Authorization to Permit Access to the Instant Application by the Participating Offices::	No
This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013::	No

Representative Information

Representative Customer Number::	24998

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This application	An application claiming the benefit under 35 USC 119(e)	61/860,976	08/01/13

Applicant Information

Applicant Type::	Assignee
Organization Name::	Efficient Power Conversion Corporation
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State or Province of mailing address::	CA
Postal or Zip Code of mailing address::	90245

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.			
Signature		Date	July 30, 2014
Name (Print/Type)	Stephen A. Soffen	Registration No. (Attorney/Agent)	31,063

Docket No.: E0101.0032/P032

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

NON-PROVISIONAL APPLICATION FOR U.S. LETTERS PATENT

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

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DOCSNY-571445

GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GAN TRANSISTORS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/860,976, filed on August 1, 2013, the entire disclosure of which is hereby incorporated by reference

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0002] The present invention relates generally to transistors and, more particularly, to an enhancement mode GaN transistor with reduced gate leakage current between the gate and the 2DEG region.

2. Description of the Related Art:

[0003] GaN semiconductor devices are increasingly desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages. Development of these devices has generally been aimed at high power/high frequency applications. Devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFET), high electron mobility transistors (HEMT), or modulation doped field effect transistors (MODFET). These types of

devices can typically withstand high voltages, e.g., 30V-to-2000 Volts, while operating at high frequencies, e.g., 100 kHZ-100 GHz.

[0004] A GaN HEMT device includes a nitride semiconductor with at least two nitride layers. Different materials formed on the semiconductor or on a buffer layer cause the layers to have different band gaps. The different material in the adjacent nitride layers also causes polarization, which contributes to a conductive two dimensional electron gas (2DEG) region near the junction of the two layers, specifically in the layer with the narrower band gap.

[0005] The nitride layers that cause polarization typically include a barrier layer of AlGaN adjacent to a layer of GaN to include the 2DEG, which allows charge to flow through the device. This barrier layer may be doped or undoped. Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted (*i.e.*, removed) below the gate at zero applied gate bias, the device can be an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

[0006] Fig. 1 illustrates a conventional schematic enhancement-mode GaN transistor. As shown, a p-type material 101 is used as the gate 103. At 0V bias, the p-type material 101 depletes the 2DEG 102 under the gate 103, and the device is in an OFF state. The transistor is turned ON by applying a positive voltage to the gate 103. Fig. 2 illustrates a schematic diagram of two gate leakage current paths 201, 202 of a conventional enhancement-mode GaN transistor. The first gate

leakage current path 201 flows along the sidewall of the p-type gate material 101 and the second gate leakage current path 202 flows through the bulk of the p-type gate material 101.

[0007] Figs. 3A and 3B illustrate schematic diagrams of two test structures 300A, 300B designed to determine the types of structures for an enhancement-mode GaN transistor that may result in lower gate leakage current. In particular, the transistor structure 300A illustrated in Fig. 3A is designed with a larger gate surface area and fewer gate edges when compared to the transistor structure 300B illustrated in Fig. 3B. In this example, the transistor structure 300A has a gate surface area of 140,000 μm^2 and 2,500 μm edges, while the transistor structure 300B has a gate surface area of 84,000 μm^2 and 247,000 μm edges.

[0008] Fig. 4 illustrates a graphical comparison of the gate leakage currents of the transistor structures 300A and 300B illustrated in Fig. 3A and 3B, respectively. As shown, structure 300B has a higher gate leakage current than structure 300A, suggesting that the gate leakage current is predominately along the gate edge, *i.e.*, path 201 illustrated in Fig. 2.

[0009] Accordingly, it is an object of the present invention is to provide an enhancement-mode GaN transistor with reduced gate leakage current between the gate 103 and the 2DEG 102.

SUMMARY OF THE INVENTION

[0010] An enhancement-mode GaN transistor and method for manufacturing the same is disclosed herein with the enhancement-mode GaN transistor having reduced gate leakage current between a gate contact and a 2DEG region and a method for manufacturing the same. The

enhancement-mode GaN transistor including a GaN layer, a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer, and source contact and drain contacts disposed on the barrier layer. The GaN transistor further includes a p-type gate material formed above the barrier layer and between the source and drain contacts and a gate metal disposed on the p-type gate material, with wherein the p-type gate material including comprises a pair of self-aligned ledges that extend toward the source contact and drain contact, respectively.

[0011] A method for manufacturing the enhancement-mode GaN transistor disclosed herein includes the steps of forming a GaN layer; forming a barrier layer on the GaN layer; depositing a p-type gate material on the barrier layer; depositing a gate metal on the p-type gate material; forming a photoresist over the gate metal; etching the gate metal and the p-type gate material; and isotropically etching the gate metal to form pair of ledges on the p-type gate material below the gate metal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The features, objects, and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

[0013] Fig. 1 illustrates a schematic of a conventional enhancement-mode GaN transistor.

[0014] Fig. 2 illustrates a schematic diagram of two gate leakage current paths of a conventional enhancement-mode GaN transistor.

[0015] Fig. 3A illustrates a schematic diagram of test structure of an enhancement-mode GaN transistor.

[0016] Fig. 3B illustrates a schematic diagram of test structure of another enhancement-mode GaN transistor.

[0017] Fig. 4 illustrate a graphical comparison of the gate leakage currents of structures shown in Figs. 3A and 3B.

[0018] Fig. 5 illustrates a schematic diagram of a transistor device according to an exemplary embodiment of the present invention.

[0019] Figs. 6A-6C illustrates a fabrication process to manufacture a gate of a transistor device with self-aligned ledges according to an exemplary embodiment.

[0020] Fig. 7A illustrates a cross-sectional image of a conventional gate structure without a ledge.

[0021] Fig. 7B illustrates a cross-sectional image of a gate structure with a self-aligned ledge according to an exemplary embodiment.

[0022] Fig. 8 illustrates a graphical comparison of gate leakage current of the gate structures illustrated in Figs. 7A and 7B.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0023] In the following detailed description, reference is made to certain embodiments. These embodiments are described with sufficient detail to enable those skilled in the art to practice them.

It is to be understood that other embodiments may be employed and that various structural, logical, and electrical changes may be made. The combinations of features disclosed in the following detailed description may not be necessary to practice the teachings in the broadest sense, and are instead taught merely to describe particularly representative examples of the present teachings.

[0024] Fig. 5 illustrates a schematic diagram of a transistor device according to an exemplary embodiment of the present invention. As shown, the transistor includes a source metal 510 (i.e., source contact) and a drain metal 512 (i.e., drain contact) with a gate contact disposed between the source and drain metals. In particular, a GaN base layer 501 is provided with a barrier layer 502 formed over the GaN base layer 501 and a two dimensional electron gas (2DEG) region formed at the interface between the GaN base layer and the barrier layer 502. In the exemplary embodiment, the barrier layer 502 is formed from aluminum gallium nitride (AlGaN).

[0025] As further shown, the gate contact includes a p-type gate material 503 formed on the barrier layer 502 and includes ledges 506 that are created by a self-aligned process at the top corners of the p-type gate material 503 as will be discussed in detail below. A gate metal 504 is disposed over the p-type gate material 503. As shown, the gate metal 504 has a smaller width (i.e., the width between sidewalls of the gate metal 504) than the width of the p-type gate material 503 (i.e., the width between side surfaces of the p-type gate material 503), effectively forming the pair of horizontal ledges 506 on each side of the gate metal 504. The pair of ledges 506 that extend past sidewalls of the gate metal 504 have equal or substantially equal widths, *i.e.*, the respective ledges

are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material, which is due to the self-aligned manufacturing process.

[0026] The primary benefits of using a self-aligned manufacturing process is to: (1) enable the creation of a p-type gate with a minimum critical dimension ("CD"), (2) lower processing cost because a second mask is not required, and (3) create ledges 506 that are symmetric to the gate metal 504 disposed on the p-type gate material. As indicated by the arrows (denoted by reference numbers 505) shown on ledges 506 and the side surfaces of the p-type gate material 503, when a positive voltage V_g is applied to the gate metal 504, the gate current path 505 first travels horizontally along the upper edge of the p-type gate material 503 and, once it reaches the ledges 506, the current path 505 follows the diagonal path along the edge of the p-type gate material 503. This structure results in reduced gate leakage current as discussed below with respect to Fig. 8.

[0027] Figs. 6A-6C illustrate a manufacturing process for fabricating a gate with self-aligned ledges in accordance with an exemplary embodiment of the present invention. As shown in Fig. 6A, the base structure of the device is first formed with a base layer 601 of gallium nitride (GaN), a barrier layer 602 of aluminum gallium nitride (AlGaN) formed on the GaN layer 601, and a layer of p-type gate material 603 formed on the barrier layer 502, over which the gate metal 604 is deposited.

[0028] Next, as shown in Fig. 6B, a photoresist 605 is deposited and the gate metal 604 is then etched. The p-type gate material 603 is also etched in a manner that results in the gate structure depicted in Fig. 6B. As shown in Fig. 6C, the gate metal 604 is then etched isotropically, which

results in the gate metal have a width less than the planar upper surface of the p-type gate material 603. This second etching step results in the formation of the ledges 506 of the p-type gate material 603.

[0029] Finally, the manufacturing process includes a step of removing the photoresist 605, which is not shown, and results in the gate with self-aligned ledge shown in Fig. 5. It should also be appreciated that contact metals for the drain and source contacts can be separately deposited using conventional fabrication techniques, but their formation will not be described herein so as to not unnecessarily obscure the aspects of the invention.

[0030] Figs. 7A-7B illustrate a transmission electron microscopy ("TEM") image of a cross-sectional view of a conventional transistor gate and an x-ray of a cross-sectional view of a gate with a self-aligned ledge according to the exemplary embodiment disclosed herein. Fig. 8 illustrates a graph comparing the gate leakage current of the present invention (shown in Fig. 7B) with the gate leakage current of a conventional transistor (shown in Fig. 7A). As can be clearly seen in Fig. 8, the gate with self-aligned ledges has significantly lower gate leakage current than conventional gates without ledges when the transistor device is in the ON state.

[0031] Finally, it is noted that the self-aligned process illustrated in Figs. 6A-6C is vastly superior to forming gate ledges using separate masks. In the process of using separate masks, a photoresist mask is applied to the unetched structure after the p-type gate material is deposited on the barrier layer of the device. In this instance, the first mask is used to pattern and etch the gate metal to a minimum CD. A second mask is then used to pattern and etch the p-type material with a wider CD

than the gate metal. One significant disadvantage of this two mask process is the possibility of misalignment between the gate metal and the p-type gate material.

[0032] The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described herein. Modifications and substitutions to specific process conditions can be made. Accordingly, the embodiments of the invention are not considered as being limited by the foregoing description and drawings.

CLAIMS

What is claimed:

1. An enhancement-mode GaN transistor, comprising:

a GaN layer;

a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending towards the barrier layer; and

a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal, the pair of horizontal edges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

2. The enhancement-mode GaN transistor according to claim 1, further comprising a source contact and a drain contact disposed on the barrier layer.

3. The enhancement-mode GaN transistor according to claim 2, wherein the pair of horizontal ledges of the p-type gate material extend toward the source contact and drain contact, respectively.

4. The enhancement-mode GaN transistor according to claim 3, wherein the side surfaces of the p-type gate material extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

5. The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

6. The enhancement-mode GaN transistor according to claim 1, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

7. The enhancement-mode GaN transistor according to claim 1, wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width.

8. An enhancement-mode GaN transistor, comprising:

a GaN layer;

a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

a source contact and a drain contact disposed on the barrier layer;

a p-type gate material formed above the barrier layer and between the source and drain contacts;

and a gate metal disposed on the p-type gate material,

wherein the p-type gate material comprises a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively.

9. The enhancement-mode GaN transistor according to claim 8, wherein the p-type gate material further comprises side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer.

10. The enhancement-mode GaN transistor according to claim 8, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

11. The enhancement-mode GaN transistor according to claim 8, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

12. A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

forming a GaN layer;

forming a barrier layer on the GaN layer;

depositing a p-type gate material on the barrier layer;

depositing a gate metal on the p-type gate material;

forming a photoresist over the gate metal;

etching the gate metal and the p-type gate material; and

isotropically etching the gate metal to form pair of ledges on the p-type gate material below the gate metal.

13. The method according to claim 12, wherein the step of isotropically etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.

14. The method according to claim 12, further comprising depositing source and drain contacts on the barrier layer.

15. The method according to claim 12, wherein the step of etching the p-type material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

16. The method according to claim 12, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

ABSTRACT

An enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a 2DEG region and a method for manufacturing the same. The enhancement-mode GaN transistor including a GaN layer, a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer, and source contact and drain contacts disposed on the barrier layer. The GaN transistor further includes a p-type gate material formed above the barrier layer and between the source and drain contacts and a gate metal disposed on the p-type gate material, with wherein the p-type gate material including comprises a pair of self-aligned ledges that extend toward the source contact and drain contact, respectively.

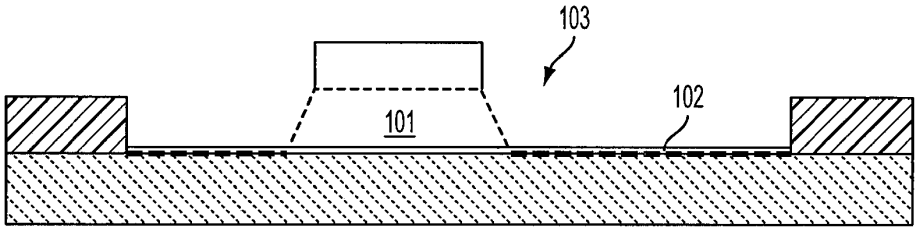


FIG. 1
PRIOR ART

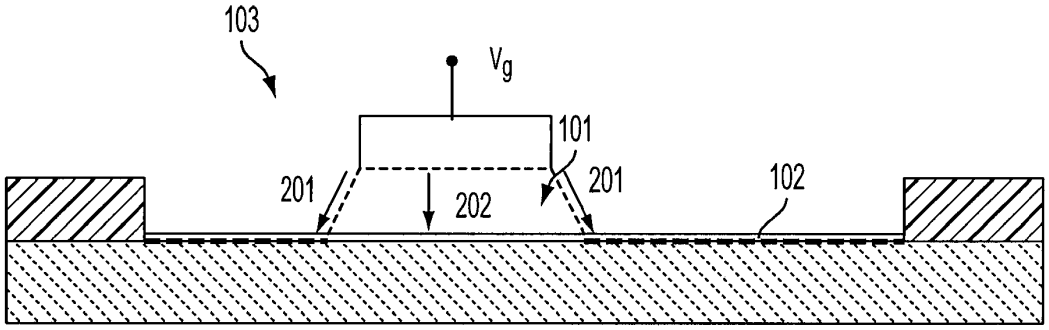


FIG. 2
PRIOR ART

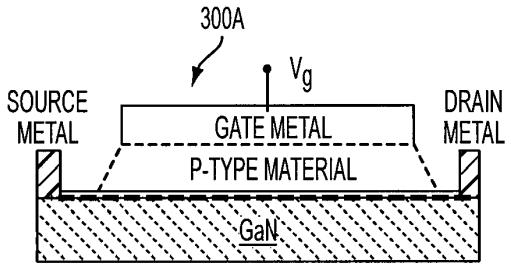


FIG. 3A
PRIOR ART

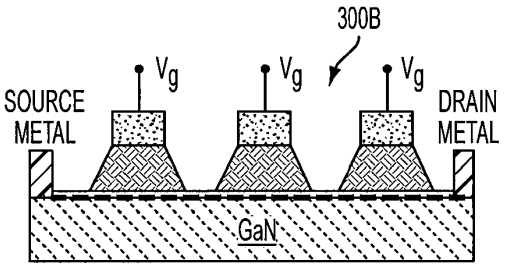


FIG. 3B
PRIOR ART

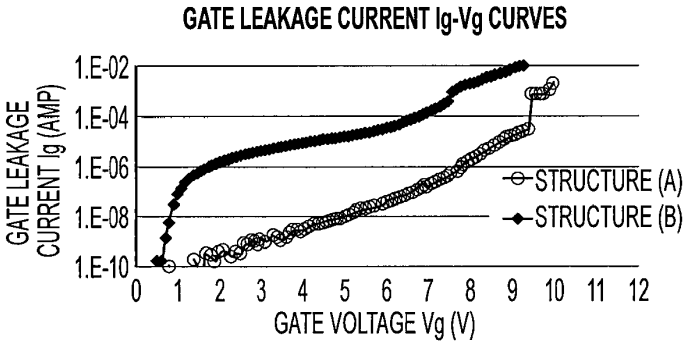


FIG. 4
PRIOR ART

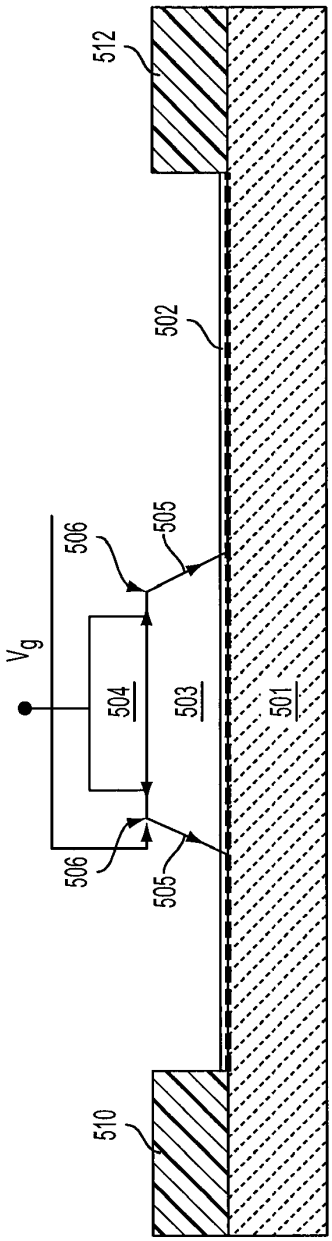


FIG. 5

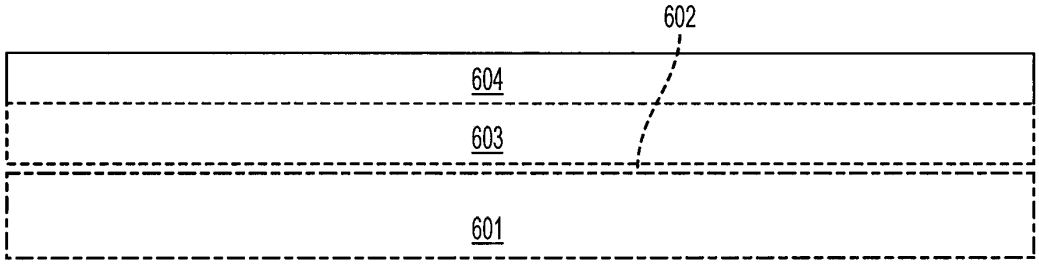


FIG. 6A

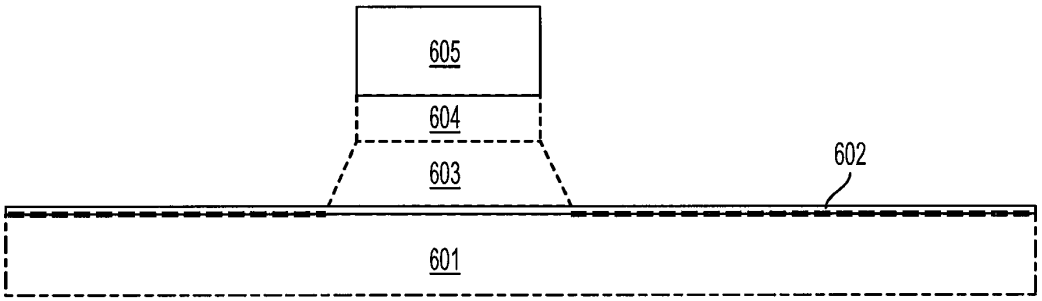


FIG. 6B

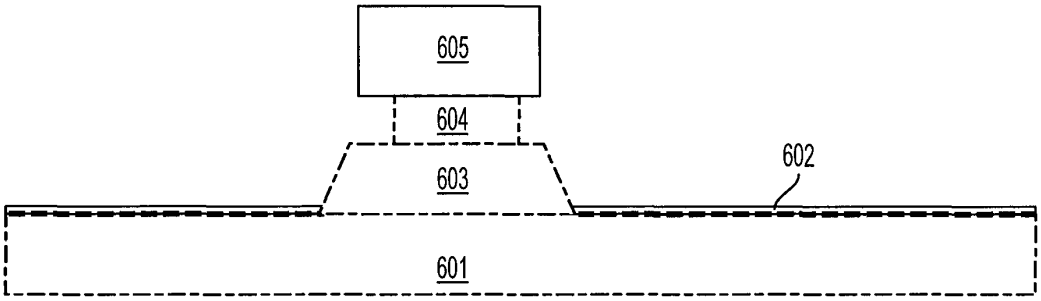


FIG. 6C

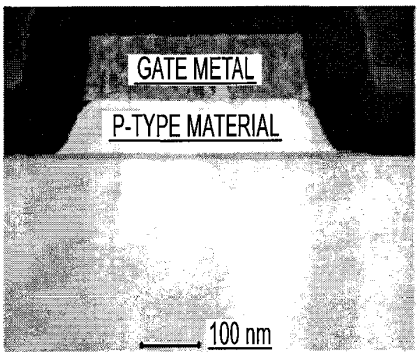


FIG. 7A
PRIOR ART

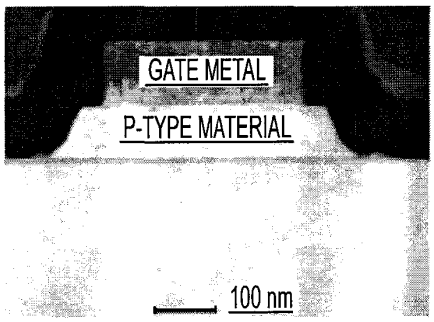


FIG. 7B

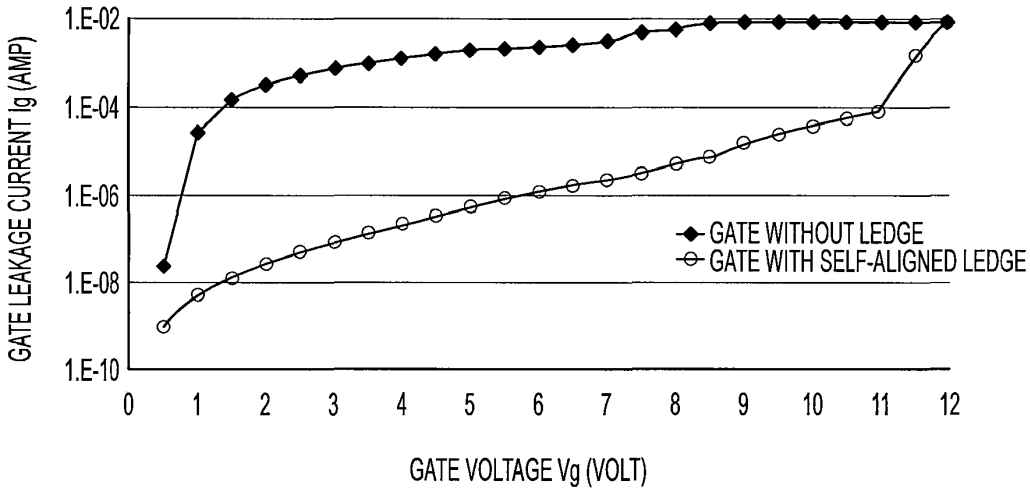

1.E-02
1.E-04
1.E-06
1.E-08
1.E-10
GATE LEAKAGE CURRENT Ig (AMP)
0
1
2
3
4
5
6
7
8
9
10
11
12
GATE VOLTAGE Vg (VOLT)
GATE WITHOUT LEDGE
GATE WITH SELF-ALIGNED LEDGE

FIG. 8

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Jianjun Cao Date (Optional): _____

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

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LEGAL NAME OF INVENTOR

Inventor: Alexander Lidow Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS

As the below named inventor, I hereby declare that:

This declaration is directed to:
- [x] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Alana Nakata Date (Optional): July 25, 2014

Signature: Alana Nakata

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

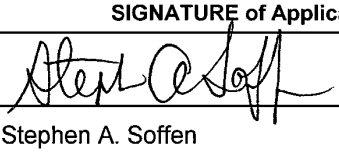
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Application Number	Not Yet Assigned
Filing Date	Concurrently Herewith
First Named Inventor	Jianjun Cao
Title	GATE WITH SELF-ALIGNED LEDGE FOR ENHANCEMENT MODE GaN TRANSISTORS
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	E0101.0032.US

SIGNATURE of Applicant or Patent Practitioner

Signature		Date	July 30, 2014
Name	Stephen A. Soffen	Telephone	(202) 420-4879
Registration Number	31,063		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

[X] *Total of 1 forms are submitted.

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Doc Code: PA..
Document Description: Power of Attorney

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I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
Not Yet Assigned	Concurrently Herewith

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OR

[ ] I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Efficient Power Conversion Corporation

[ ] Inventor or Joint Inventor (title not required below)

[ ] Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

[X] Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

[ ] Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	David Reusch	Date (Optional)	12-26-13
Name	David Reusch		
Title			

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Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Filer:	Stephen A. Soffen/Kanessa Howard
Attorney Docket Number:	E0101.0032.US
Filed as Small Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**730**

Electronic Acknowledgement Receipt	
EFS ID:	19730694
Application Number:	14447069
International Application Number:	
Confirmation Number:	7150
Title of Invention:	GATE WITH SELF-ALIGNED LEDGED FOR ENHANCEMENT MODE GaN TRANSISTORS
First Named Inventor/Applicant Name:	Jianjun Cao
Customer Number:	24998
Filer:	Stephen A. Soffen/Kanessa Howard
Filer Authorized By:	Stephen A. Soffen
Attorney Docket Number:	E0101.0032.US
Receipt Date:	30-JUL-2014
Filing Date:	
Time Stamp:	16:22:22
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	yes
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Payment was successfully received in RAM	$730
RAM confirmation Number	2587
Deposit Account	041073
Authorized User	SOFFEN, STEPHEN A.
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1		E0101_0032_NonProvApp.pdf	1261088 b0605b6d476c414df2e09d630a2aad582b6131a8	yes	31

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal of New Application	1	1
Application Data Sheet	2	5
Specification	6	15
Claims	16	19
Abstract	20	20
Drawings-only black and white line drawings	21	26
Oath or Declaration filed	27	29
Power of Attorney	30	31

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2	Fee Worksheet (SB06)	fee-info.pdf	33053 c07c867411dc17802f451048cab8e5d9199641e0	no	2

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