

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY AND

INNOSCIENCE AMERICA, INC.,

Petitioner

v.

EFFICIENT POWER

CONVERSION CORPORATION,

Patent Owner

Case No. IPR2023-01382

U.S. Patent No. 9,748,347

DECLARATION OF JAMES RICHARD SHEALY, PH.D.

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	SUMMARY OF OPINIONS.....	2
III.	QUALIFICATIONS AND BACKGROUND	2
IV.	MATERIALS CONSIDERED	6
V.	LEGAL STANDARDS	8
A.	Level of Ordinary Skill in the Art	10
B.	Anticipation	10
C.	Obviousness.....	11
VI.	OVERVIEW OF THE '347 PATENT	16
A.	The Claims and Specification	16
B.	Prosecution History	21
VII.	LEVEL OF ORDINARY SKILL IN THE ART	24
VIII.	TECHNOLOGY BACKGROUND AND THE STATE OF THE PRIOR ART.....	25
IX.	CLAIM CONSTRUCTION	31
A.	forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer” [claim 1], [1f].....	33
B.	“etching the gate metal and the p-type gate material” [claim 1], [1g]	37
C.	“etching the gate metal to form a pair of ledges” [claim 1], [1i]	38

X.	Ground 1: <i>Saxler</i> in View of <i>Beach</i> and <i>Shenoy</i> Renders Obvious	
	Claims 1-3.....	39
A.	Overview of Ground 1.....	39
1.	<i>Saxler</i>	39
2.	<i>Beach</i>	44
3.	<i>Shenoy</i>	45
4.	Combination of <i>Saxler</i> , <i>Beach</i> , and <i>Shenoy</i>	46
5.	Motivation to Combine	47
B.	Independent Claim 1	53
1.	[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:	53
2.	[1a] forming a GaN layer;.....	54
3.	[1b] forming a barrier layer on the GaN layer;.....	54
4.	[1c]: depositing source and drain contacts on the barrier layer;.....	55
5.	[1d]: depositing a p-type gate material on the barrier layer;.....	56
6.	[1e]: depositing a gate metal on the p-type gate material;.....	57
7.	[1f]: forming a photoresist over the gate metal;	59
8.	[1g]: etching the gate metal and the p-type gate material,.....	60
9.	[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and.....	61

10.	[1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.	65
C.	[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.	67
D.	[Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.	68
XI.	Ground 2: <i>Saxler</i> in view of <i>Yoshida</i> , <i>Beach</i> , and <i>Shenoy</i>	69
A.	Overview of Ground 2	69
1.	<i>Yoshida</i>	69
2.	The Combination of <i>Saxler</i> in View of <i>Yoshida</i>	71
3.	Motivation to Combine	71
B.	Independent Claim 1	78
1.	[1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:	78
2.	[1a]: forming a GaN layer;	79
3.	[1b]: forming a barrier layer on the GaN layer;	79
4.	[1c]: depositing source and drain contacts on the barrier layer;	79
5.	[1d]: depositing a p-type gate material on the barrier layer;	79
6.	[1e]: depositing a gate metal on the p-type gate material;	79
7.	[1f]: forming a photoresist over the gate metal;	79
8.	[1g]: etching the gate metal and the p-type gate material, ...	80

9.	[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and	81
10.	[1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.	81
C.	[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.	82
D.	[Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.	83
XII.	Ground 3: <i>Saxler</i> in view of <i>Ahn</i>	83
A.	Overview of Ground 3	83
1.	<i>Ahn</i>	83
2.	Combination of <i>Saxler</i> and <i>Ahn</i>	86
3.	Motivation to Combine	86
B.	Independent Claim 1	89
1.	[1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:	89
2.	[1a]: forming a GaN layer;	89
3.	[1b]: forming a barrier layer on the GaN layer;	89
4.	[1c]: depositing source and drain contacts on the barrier layer;	90
5.	[1d]: depositing a p-type gate material on the barrier layer;	90

6.	[1e]: depositing a gate metal on the p-type gate material;.....	90
7.	[1f]: forming a photoresist over the gate metal;	90
8.	[1g]: etching the gate metal and the p-type gate material,.....	91
9.	[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and	92
10.	[1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.	94
C.	[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.	96
D.	[Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.	97
XIII.	Ground 4: <i>Yoshida</i> in view of <i>Saxler</i> , <i>Beach</i> , and <i>Shenoy</i> Renders Obvious Claims 1-2	98
A.	Overview of Ground 4.....	98
1.	Ground 4: <i>Yoshida</i> in view of <i>Saxler</i> , <i>Beach</i> , and <i>Shenoy</i>	99
2.	Ground 4: Motivation to Combine.....	100
B.	Independent Claim 1	107
1.	[1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:	107
2.	[1a]: forming a GaN layer;.....	108
3.	[1b]: forming a barrier layer on the GaN layer;.....	108

4.	[1c]: depositing source and drain contacts on the barrier layer;.....	109
5.	[1d]: depositing a p-type gate material on the barrier layer;.....	110
6.	[1e]: depositing a gate metal on the p-type gate material;.....	112
7.	[1f]: forming a photoresist over the gate metal;	114
8.	[1g]: etching the gate metal and the p-type gate material;.....	115
9.	[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and.....	116
10.	[1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.	121
C.	[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.	122
D.	[Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.	123
XIV.	Ground 5: <i>Yoshida</i> in view of <i>Ahn</i>	124
A.	Overview of Ground 5.....	124
1.	Ground 5: The Combination of <i>Yoshida</i> and <i>Ahn</i>	124
2.	Ground 5: Motivation to Combine.....	126
B.	Independent Claim 1	128
1.	[1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:	128

2.	[1a]: forming a GaN layer;.....	128
3.	[1b]: forming a barrier layer on the GaN layer;.....	128
4.	[1c]: depositing source and drain contacts on the barrier layer;.....	129
5.	[1d]: depositing a p-type gate material on the barrier layer;.....	129
6.	[1e]: depositing a gate metal on the p-type gate material;.....	129
7.	[1f]: forming a photoresist over the gate metal;	129
8.	[1g]: etching the gate metal and the p-type gate material,.....	130
9.	[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and	131
10.	[1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.	132
C.	[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.	135
D.	[Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.	135
XV.	CONCLUSION.....	137

I. INTRODUCTION

[001] I have been retained by Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively “Innoscience”), as an independent expert for the above-identified inter partes review proceeding involving U.S. Patent No. 9,748,347 (“the ’347 patent”).

[002] I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

[003] Although I am being compensated for my time in connection with this proceeding at my standard hourly consulting rate and reimbursed for reasonable out-of-pocket expenses, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

[004] I have been asked to provide my opinion whether the claims of the ’347 patent would have been obvious to a person of ordinary skill in the art at the time of the earliest claimed priority date of the ’347 patent. In performing my analysis, I have been asked to assume that the priority date is April 8, 2009. My opinions are set forth below.

[005] Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not

intended to suggest that they are the only support for the propositions for which they are cited.

II. SUMMARY OF OPINIONS

[006] This declaration analyses claims 1-3 of the '347 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for my opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

[007] Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of April 8, 2009), it is my opinion that claims 1-3 of the '347 patent would have been obvious based on the asserted grounds discussed below.

III. QUALIFICATIONS AND BACKGROUND

[008] I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A.

[009] I am competent to write this Declaration.

[010] I have been involved in the science and engineering of high-power compound semiconductor transistors for over 40 years. I have been deeply involved in the research and design of III-V compound semiconductor devices over

the course of my career. I have been a Professor at Cornell University, School of Electrical and Computer Engineering, and have been teaching and conducting research at Cornell since 1987. In 2022, I was granted emeritus status.

[011] I received a B.S. degree from North Carolina State University in 1978, a M.S. from Rensselaer Polytechnic Institute in 1980, and a Ph.D. from Cornell University in 1983. I joined the Cornell faculty in 1987. And I am currently a Full Professor at Cornell's School of Electrical and Computer Engineering.

[012] In 1978, I joined the technical staff of General Electric's Corporate Research and Development Center under an Edison Fellowship. While there, among other work, I developed GaAs epitaxial materials for high voltage electronics. I was the inventor of two patents on Vertical Field Effect Transistors.

[013] In 1980, I transferred to General Electric's Advanced Electronics Laboratory where I developed materials and processes for the fabrication of AlGaAs LEDs as well as developing an OMVPE reactor and related processes for the fabrication of AlGaAs quantum well laser diodes. In 1985, I was designated Principal Staff Scientist at General Electric in recognition of my research contributions.

[014] While at General Electric, I was also concurrently working at Cornell. In 1984, my group at Cornell developed the first single quantum well red laser by

Organometallic Vapor-Phase Epitaxy (“OMVPE”), a technique used for growing semiconductor crystals. The fabrication of these devices involved multi-level metallization and dielectric passivation.

[015] I joined the Cornell faculty in 1987 as a Professor of Electrical and Computer Engineering (ECE) and Materials Science and Engineering (MSE). While at Cornell I have continued my research in OMVPE, particularly as it relates to high frequency transistors, LEDs, and laser diodes. I have also researched GaN and related materials for both high-power transistors and LEDs.

[016] In 1997, I was named the Director of Cornell's Optoelectronics Technology Center. In 1998, I was promoted to full professor at Cornell. I have published over 120 articles and am the inventor of over 19 patents, many of which deal with GaN-based materials and devices. Over the years, I have received numerous teaching awards for delivering quality instruction to undergraduates in Materials Science and Electrical Engineering.

[017] In 1998-99, the research group that I led invented and patented a single temperature method for nucleation and growth of GaN materials on sapphire, SiC, and Si substrates. This technique has become the preferred method for growing GaN-based transistors and LED today. This nucleation method was used to grow AlN/GaN layers on silicon. By mid-1999, my research group had

produced a gallium nitride-on-silicon (GaN-Si) RF transistor, a technology currently used by several GaN companies for high efficiency power convertors and RF amplifiers.

[018] By the early 2000s, my research group produced the first RF integrated circuits with gallium nitride-on-silicon carbide (GaN on SiC) transistors including X Band VCOs, TR switches, frequency doublers, and internally matched power amplifiers. By 2008, my group discovered a new passivation technology (LPCVD of AlSiN, patented) for GaN-based FETs which, when applied to GaNSiC HEMTs, produced the largest power density operation (over 18 Watts/mm at 10 GHz) ever observed on submicron gated devices. These devices also delivered record power-added-efficiencies and linear gain during 10 GHz operation (PAE > 65 %, Gain > 36 dB at 60 V bias). These benchmarks remain unchallenged today.

[019] In 2015, I cofounded Akoustis Technology (AKTS on the NASDAQ), a company which manufactures AlN bulk acoustic wave filters which are required for 5G communications. In 2019, I cofounded Odyssey Semiconductor, a company which is developing GaN Vertical field effect transistors for the emerging power convertor market. Odyssey Semiconductor also recently developed the fabrication techniques and built micro-LED Arrays in both AlGaInP and AlGaInN materials.

[020] I have remained current in the field, as evidenced by my publications listed in my curriculum vitae.

[021] I have also served as an expert in certain legal proceedings relating to GaN transistors, including materials growth, device fabrication, and packaging. A list of cases in which I have testified at trial, hearing, or by deposition is provided in my curriculum vitae.

IV. MATERIALS CONSIDERED

[022] In forming my opinions, I read and considered the '347 patent and its prosecution history, the exhibits listed in the Exhibit List filed with the petition for *inter partes* review of the '347 patent, as well as any other materials referenced herein. I have reviewed the following at least the following documents:

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,748,347 B2 to Cao et al. (“the '347 patent”)
Ex. 1002	Prosecution History of the '347 patent
Ex. 1005	Japanese Patent Publication No. JP H11-261053 to Yoshida
Ex. 1006	Certified Translation of Japanese Patent Publication No. JP H11-261053 to Yoshida (“ <i>Yoshida</i> ”)

Exhibit	Description
Ex. 1007	U.S. Patent Application Publication No. US 2006/0108606 A1 to Saxler et al. (“ <i>Saxler</i> ”)
Ex. 1008	U.S. Patent Application Publication No. US 2007/0007547 A1 to Beach (“ <i>Beach</i> ”)
Ex. 1009	R.V. Shenoy and M. Datta, <i>Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining</i> , 143 J. Electrochemical Soc’y, pp. 544-549 (1996) (“ <i>Shenoy</i> ”)
Ex. 1010	U.S. Patent No. 5,905,274 to Ahn et al. (“ <i>Ahn</i> ”)
Ex. 1011	U.S. Patent Application Publication No. US 2010/0258843 A1 to Lidow et al. (“ <i>Lidow</i> ”)
Ex. 1014	Chuan Xu et al., <i>The Leakage Current of the Schottky Contact on the Mesa Edge of AlGa_N/Ga_N Heterostructure</i> , 28 IEEE Electron Device Letters, pp. 942-944 (2007) (“ <i>Xu</i> ”)
Ex. 1015	U.S. Patent Application Publication No. US 2002/0066908 A1 to Smith (“ <i>Smith</i> ”)
Ex. 1016	U.S. Patent Application Publication No. US 2006/0273347 A1 to Hikita et al. (“ <i>Hikita</i> ”)
Ex. 1017	U.S. Patent Application Publication No. US 2009/0072272 A1 to Suh et al. (“ <i>Suh</i> ”)
Ex. 1018	X. Hu et al., <i>Enhancement mode AlGa_N/Ga_N HFET with selectively grown pn junction gate</i> , 36 Electronics Letters, pp. 753-754 (2000) (“ <i>Hu</i> ”)
Ex. 1019	U.S. Patent Application Publication No. US 2005/0087763 A1 to Kanda et al. (“ <i>Kanda</i> ”)

Exhibit	Description
Ex. 1020	Yasushiro Uemoto et al., <i>A Normally-off AlGaIn/GaN Transistor with $R_{on}A=2.6\Omega\text{cm}^2$ and $BV_{ds}=640\text{V}$ Using Conductivity Modulation</i> , 2006 International Electron Devices Meeting, IEEE (2006) (“Uemoto”)
Ex. 1021	U.S. Patent Application Publication No. US 2006/0019435 A1 to Sheppard et al. (“Sheppard”)
Ex. 1023	Dietrich W. Widmann, <i>Metallization for Integrated Circuits Using a Lift-Off Technique</i> , 11 IEEE Journal of Solid-State Circuits, pp. 466-471 (1976) (“Widmann”)
Ex. 1027	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 (“Beach-IP”)
Ex. 1028	Petitioner and Complainant’s Proposed Claim Construction, ITC 337-TA-1366
Ex. 1029	C. S. Suh et al., “p-GaN/AlGaIn/GaN Enhancement-Mode HEMTs, 2006 64th Device Research Conference, June 2006, pp. 163-164 (“Suh 2006”)

[023] I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

V. LEGAL STANDARDS

[024] I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related

matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

[025] I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

[026] I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

[027] I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-3 of the '347 patent from the perspective of a person of ordinary skill in the art at the '347 patent's earliest claimed priority date in 2009, as described in more detail below.

[028] I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving

unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

[029] For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill in the Art

[030] I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

[031] I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Anticipation

[032] I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by

anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

C. Obviousness

[033] I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

[034] I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

[035] I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of

invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the challenged claims is April 8, 2009. My opinions would not change if I assumed a later date of invention.

[036] I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

[037] I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory

statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

[038] In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

[039] I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

[040] I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

[041] I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

[042] I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '347 patent.

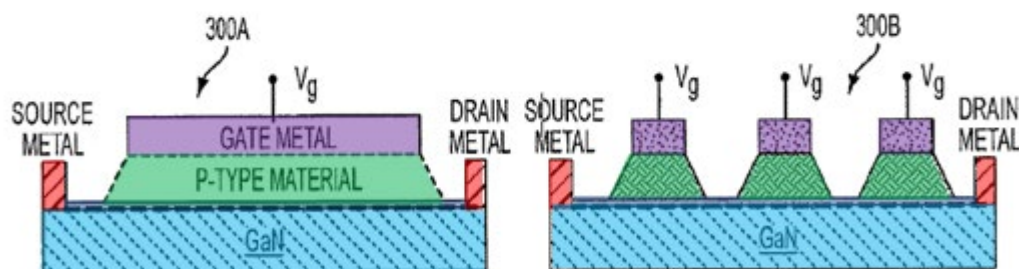
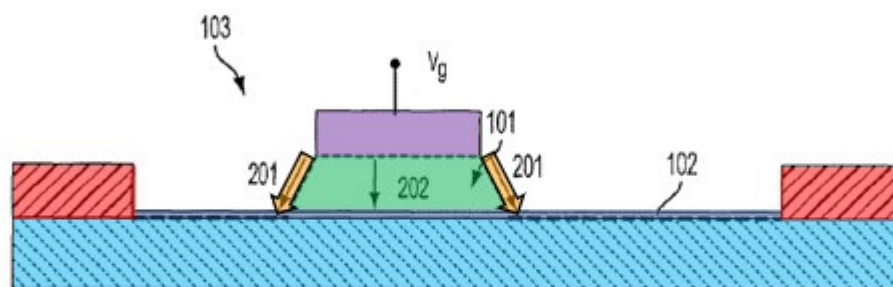
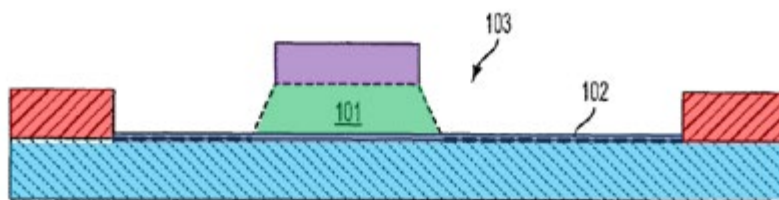
[043] I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. OVERVIEW OF THE '347 PATENT

A. The Claims and Specification

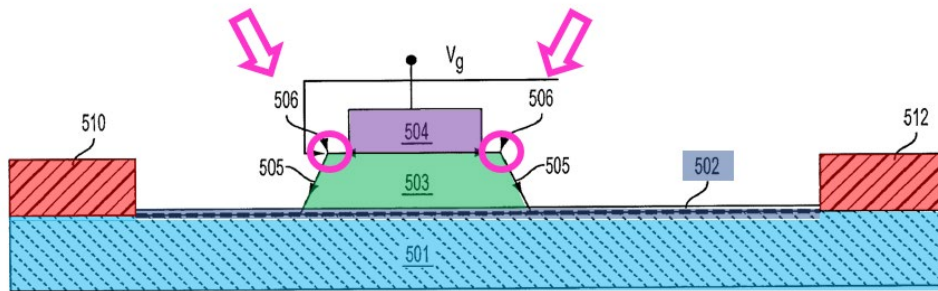
[044] The '347 patent relates to enhancement-mode GaN power transistors and methods of making these transistors. Ex. 1001, 1:19-23, 2:29-53, Fig. 5, claims 1-3. Consistent with my own understanding of the state of the art prior to April 2009, the patent describes that conventional prior art GaN HEMT devices suffered from high gate leakage current between the gate and 2DEG region. Ex. 1001, 1:17-2:25. The '347 patent admits that conventional GaN enhancement mode devices included **a GaN channel layer, an AlGaN barrier layer, source**

and **drain electrodes**, and a gate structure consisting of a **p-type GaN layer with sloped sidewalls** to address gate leakage (identifying **leakage path 201**) and an overlying **gate metal**—all features in the claims of the '347 patent. Ex. 1001, 1:17-2:25, Figs. 1-2, 3A-3B, claims 1-3.



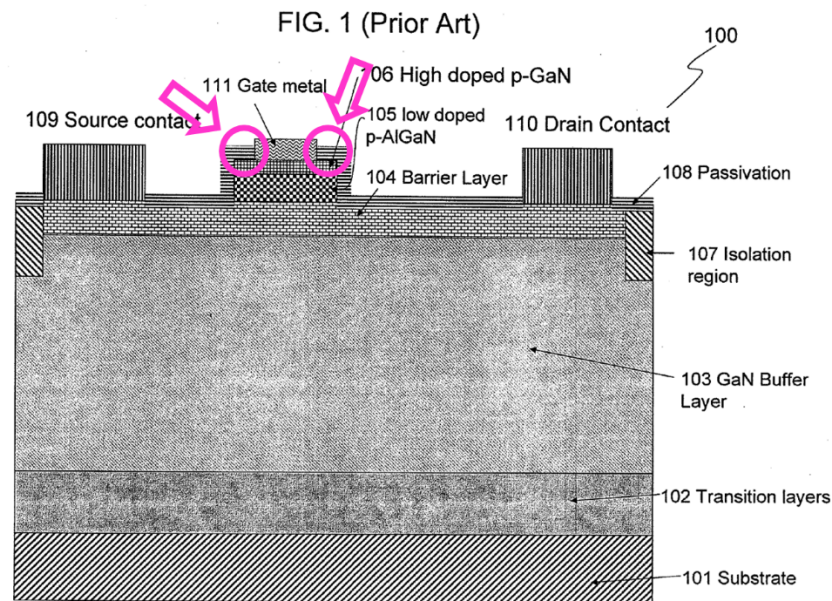
Ex. 1001, Figs. 1-2, 3A-3B.

[045] To solve the leakage problem, the '347 patent purports to invent *just one feature*: a pair of **ledges** on the p-type gate material, on either side of the gate metal. Ex. 1001, 2:29-53, 3:60-4:7, 4:40-51, Figs. 1-2, 3A-3B, 4-5, 7A-7B, 8, claims 1-3. It also asserts advantages to making these ledges using a particular method of making these ledges—a “self-aligned” technique employing a single photomask, which as I will show herein was known in the prior art. EX. 1001, 3:60-4:12, 4:46-57.



Ex. 1001, Fig. 5.

[046] Indeed, the '347 patent's priority application *Lidow* notes such ledges were conventional. *Lidow*, Fig. 1; §VI.B (Prosecution History).



Lidow, Fig. 1.

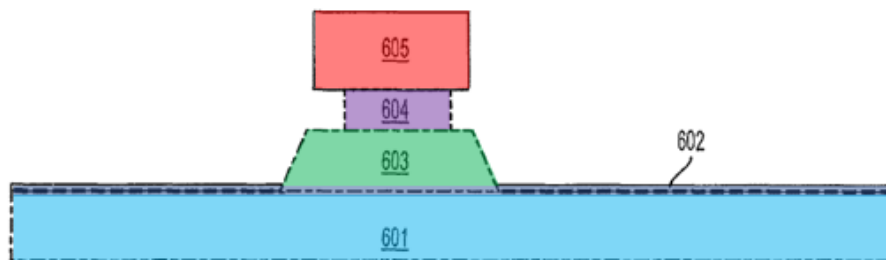
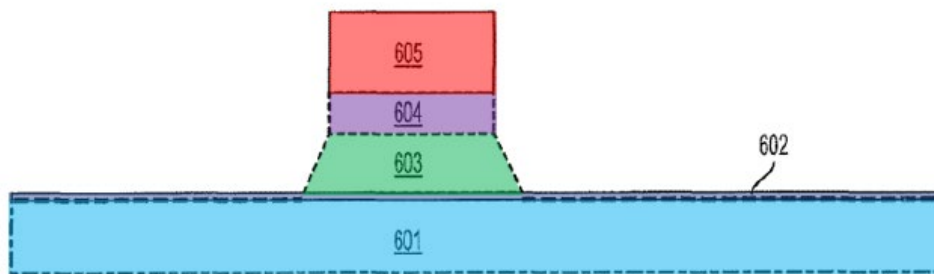
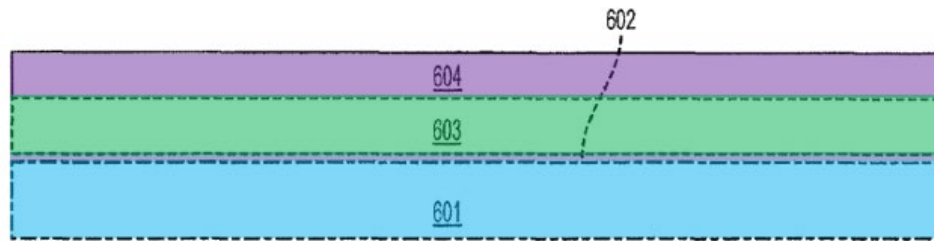
a. Self-aligned ledges

[047] As I explained above, the '347 patent uses a “self-aligned” process to make its **ledges**. Ex. 1001, 4:8-33, claim 3, Figures 6A-6C. The self-aligned process creates **ledges** by:

1. Forming **GaN layer 601**, **AlGaN layer 602**, and **p-type gate material 603**.
2. Depositing the **gate metal 604**.
3. Applying **photoresist 605**.
4. Etching the **gate metal**.

5. Etching the **p-type gate material**.
6. Etching the **gate metal** again, undercutting the same **photomask**.

Ex. 1001, 4:8-33.



Ex. 1001, Figs. 6A-6C.

B. Prosecution History

[048] From the cover of the patent, I understand that the '347 patent claims priority to U.S. Provisional Patent Application No. 61/860,976, filed August 1, 2013. Ex. 1001, cover & p. 2. It also claims priority as a continuation-in-part to U.S. Application No. 13/838,792 which was a division of U.S. Application No. 12/756,960, filed April 8, 2010, and claimed priority to U.S. Provisional Patent Application No. 61,167,777, filed April 8, 2009.'347 patent, cover & p. 2.

[049] During examination, I understand that the applicant initially received a rejection over prior art reference *Lidow*, then subsequently claimed priority to *Lidow* a continuation-in-part. Ex. 1002, 95-128, 250. But even after claiming priority to *Lidow*, the applicant nevertheless next received a rejection over *Lidow* because the pending claims included the term "isotropically etching," which was not disclosed by *Lidow*. Ex. 1002, 84-86. The applicant broadened the claim to remove the term "isotropically" from the claim in response, and the Examiner then found that *Lidow* supported the claims of what became the '347 patent. Ex. 1002, 52, 75-76, 85-86. Thus, to the extent the priority claim is valid (which I assume without offering an opinion), *Lidow* supports the claims of the '347 patent.

[050] Considering the specification, priority applications, and prosecution history, the '347 patent was allowed without disclosing *any* specific methods to

etch the gate metal to obtain the claimed ledges because such methods were well within the skill level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99. When challenged, the applicant argued that *Lidow* at [0044]-[0045] and Fig. 10 supports “etching” the gate metal to form ledges. Ex. 1002, 76. But *Lidow* only states that “[f]ollowing the step shown in FIG. 3C, the wafer is placed back in an etching machine that only etches the gate metal layer 17, without etching any other part of the device,” resulting in the structure of Figures 9-10. *Lidow*, [0043]-[0045]. Importantly, this passage does not explain *how* the metal is etched to create the claimed **ledges**, it simply states that the metal is etched. *Lidow*, [0043]-[0044].

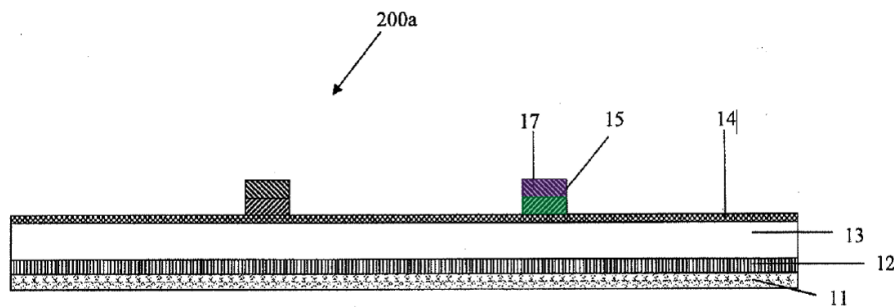


FIG. 3C

Lidow, Fig. 3C.

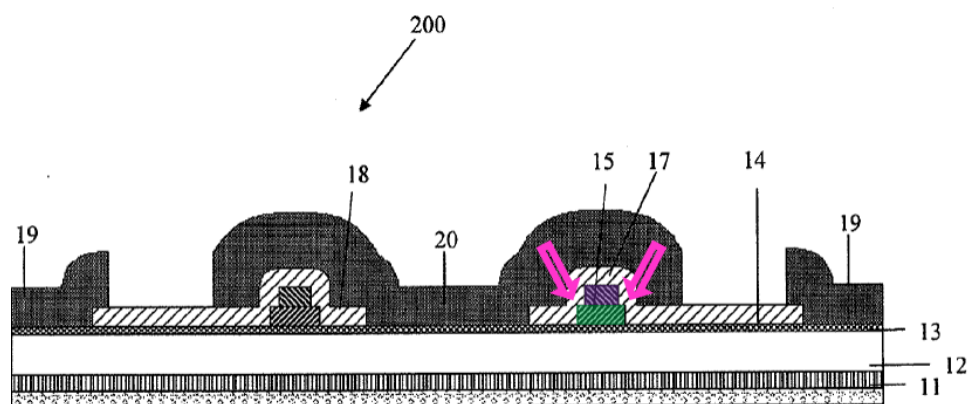
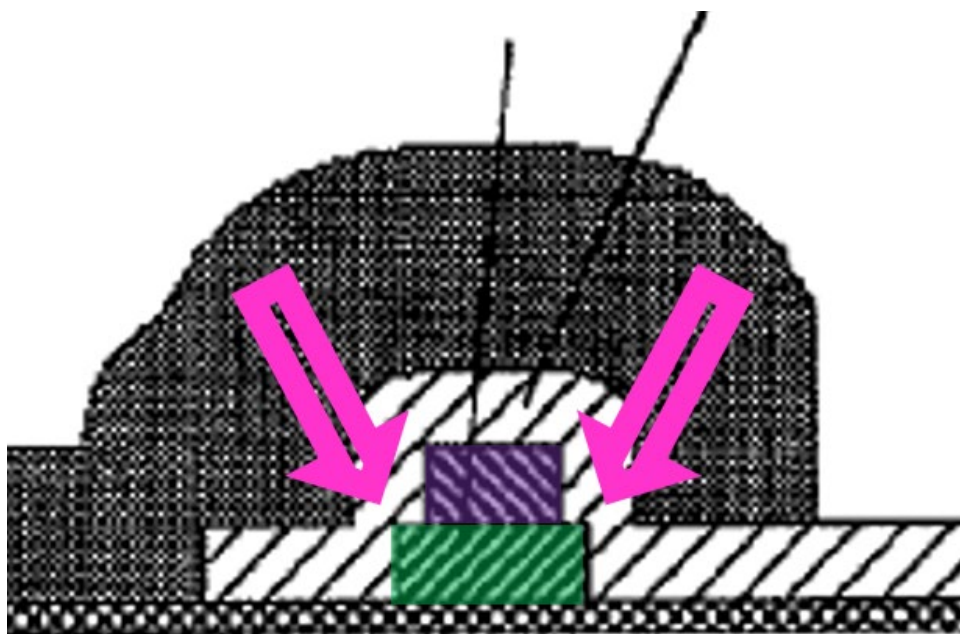


FIG. 9

Lidow, Fig. 9.



Id. (excerpted).

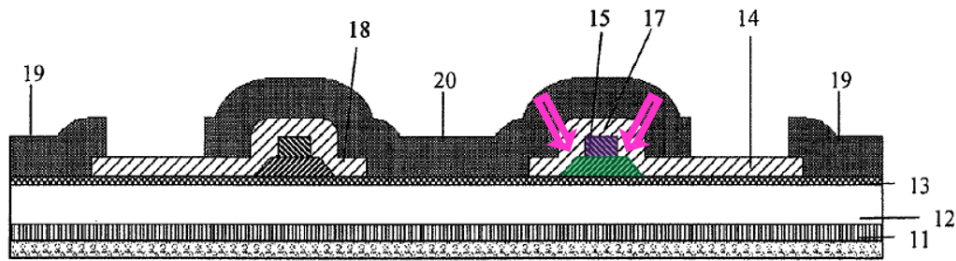


FIG. 10

Lidow, Fig. 10.

[051] Subsequently, the Examiner allowed the claims on the next action, and the Examiner identified the combination of the sloped sidewalls and ledges in the reason for allowance. Ex. 1002, 23-30.

VII. LEVEL OF ORDINARY SKILL IN THE ART

[052] In rendering the opinions set forth in this declaration, I have been asked to consider the '347 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the art," "skilled artisan," "POSITA," "POSA" or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

[053] Taking the factors described in the Legal Standards – Level of Ordinary Skill in the Art section into consideration, it is my opinion that a person of ordinary skill in the art for the '347 patent would have had at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa.

[054] Based on my educational background and experience, I was at least a person of ordinary skill in the art at the earliest priority date of the '347 patent.

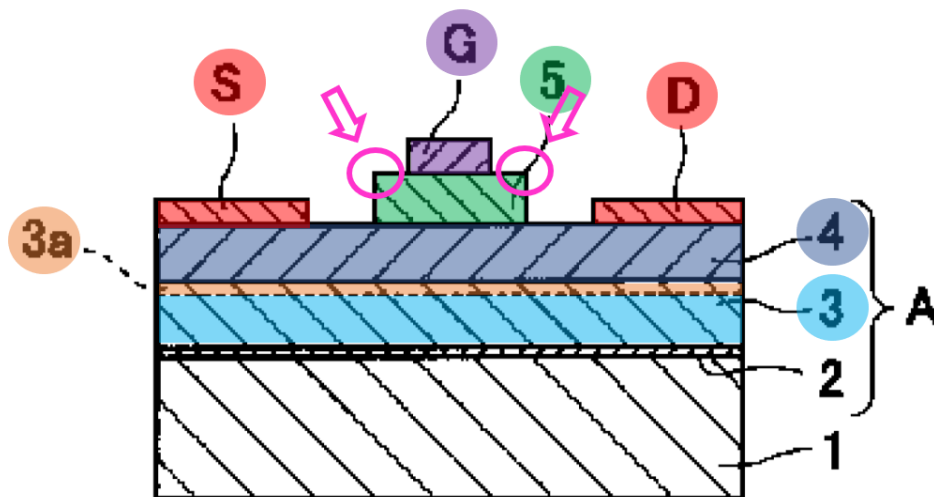
VIII. TECHNOLOGY BACKGROUND AND THE STATE OF THE PRIOR ART

[055] Power transistors fabricated with GaN have a large band gap which increases the maximum electric field strength, resulting in a large breakdown voltage making them attractive for high power applications. Ex. 1001, 1:25-44. GaN transistors were well known long before the '347 patent. *E.g.*, *Smith*, [0004]-[0010] (discussing “well known” features of GaN HEMT devices). Conventional features of such transistors include a **GaN channel** and **AlGaN barrier** layers, at the heterojunction of which a **two-dimensional electron gas (2DEG) region** forms, as well as **source** and **drain electrodes**, and a gate structure including **GaN**

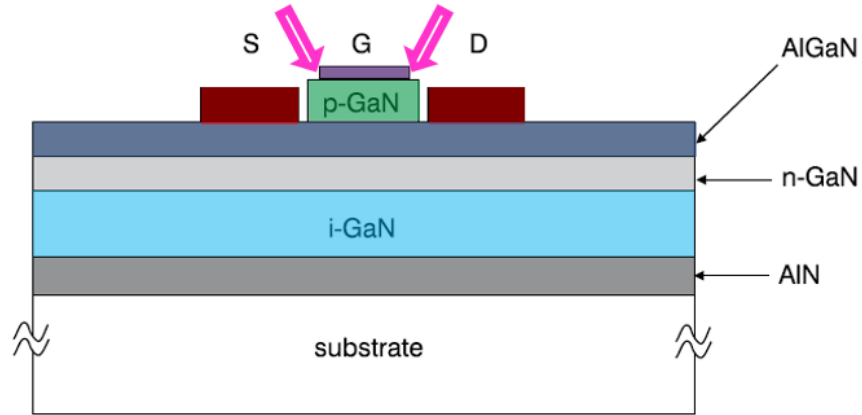
gate materials under a **gate metal**. Ex. 1001, 1:24-2:21 *Yoshida*, Abstract; *Suh*, [0002]-[0005], [0015], Figs. 1, 6-7.

[056] Enhancement mode GaN transistors are normally off, meaning no drain current flows through the 2DEG without applying positive voltage to the gate. Ex. 1001, 1:45-48, 1:59-64; *Hu*, 1. These devices achieve the normally-off state in part with a **GaN layer**, often doped p-type, in the gate structure under a **gate metal**, which increases the gate voltage (to a positive value) where the gate has a strong influence on the electron concentration in the 2DEG. Ex. 1001, 1:45-48, 1:59-64; *Hu*, 1.

[057] Below, I show example GaN HEMT arrangements in publications ranging from 1999 through 2009, the earliest claimed priority date of the '347 patent. I have marked **horizontal ledges** at the surface of the **p-type GaN gate materials**:



Yoshida, Fig. 1 (1999).



365/1

Fig. 1 Schematic diagram of structure of pn junction regrown gate HFET

Hu, Fig. 1 (2000).

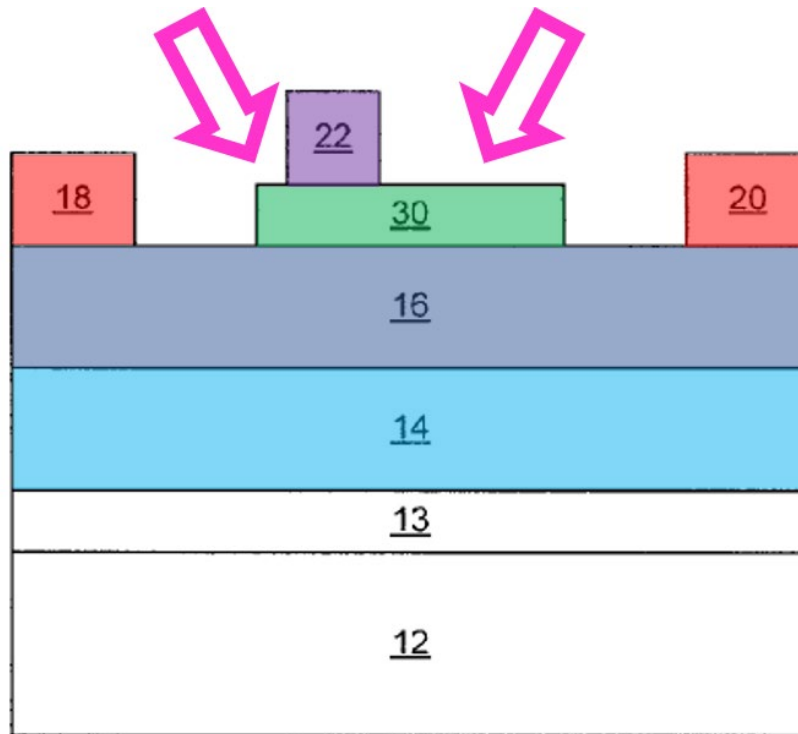
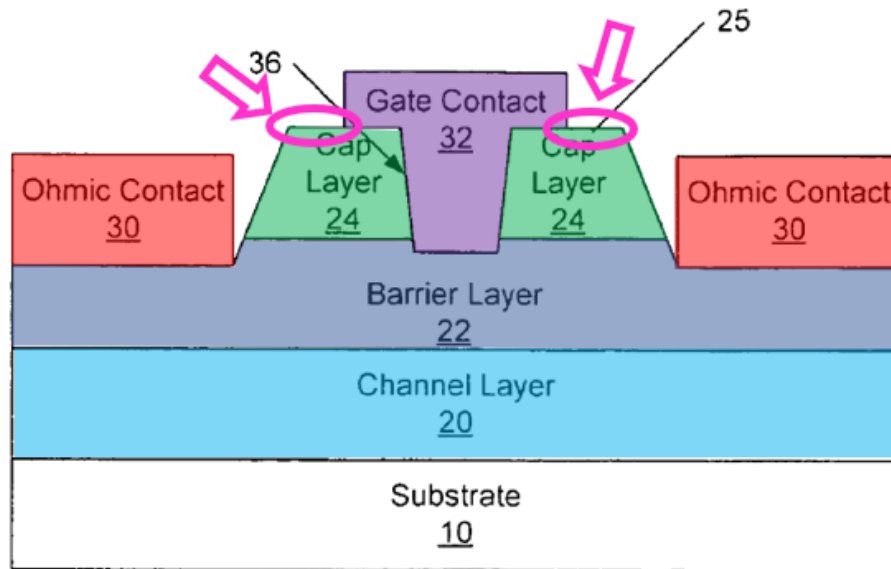
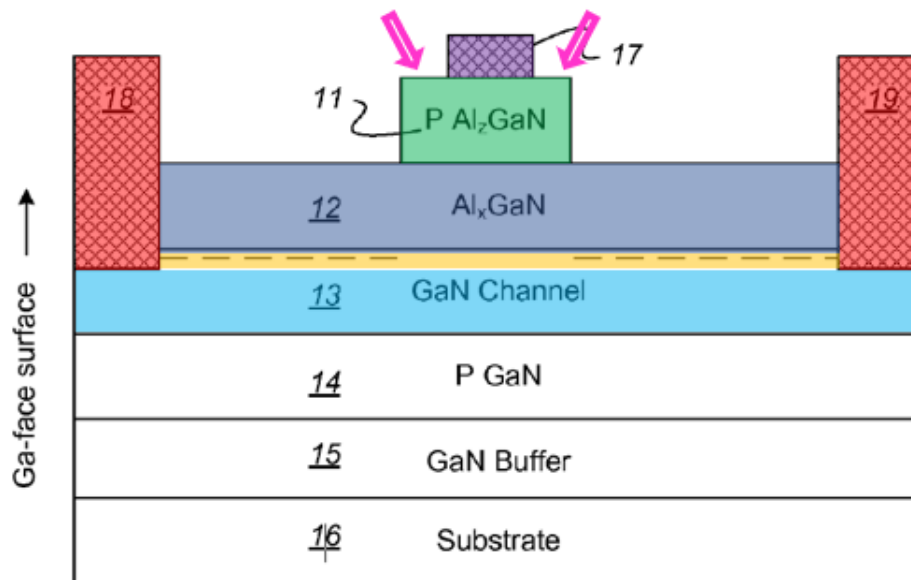


Figure 5B

Smith, Fig. 5B (2002).*Saxler, Fig. 1A (2006).**Suh, Fig. 6 (2009).*

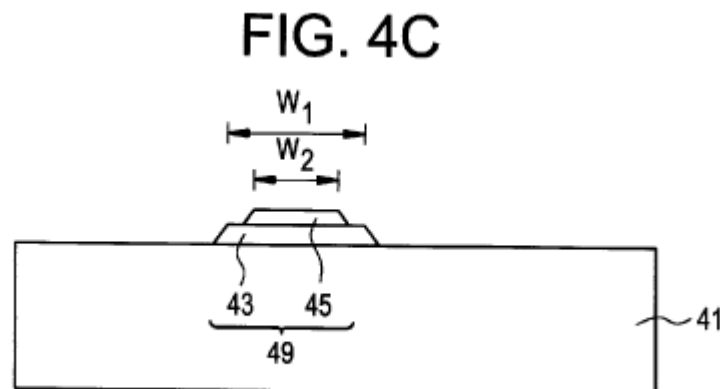
[058] As these examples illustrate, the sole point of alleged novelty of the '347 patent, making **ledges** at the surface of **p-type GaN gate materials**, was common, just as were the other features of the claims.

[059] The prior art also included many different methods of manufacturing these devices. For example, single-mask techniques to self-align stacked gate structures were long known. *Beach*, [0040]. Conventional etching techniques achieved sloped sidewalls, which were known to increase leakage paths. Ex. 1001, 1:49-2:3, Fig. 2; *Saxler*, [0064], Figs. 1A-1B; *Ahn; Xu; Sheppard*, [0044]. And it was long-known and conventional to undercut under photomasks to isotropically etch metals, as evidenced by the fact that this technique was used over a decade before the '347 patent. *Shenoy*, 1.

[060] In my opinion, a POSITA would have been familiar with many methods for making stepped gate structures with **ledges**, including (i) sequential masking and etching techniques, (ii) lift off techniques, and (iii) self-aligned techniques. For example, *Yoshida* discloses masking and etching the p-type GaN **layer 5**, then depositing the **gate electrode**. *Yoshida*, [0022]-[0023] (sequential masking and etching). *Kanda* forms stepped gate structures using lift-off. *Kanda*, [0091], [0110], [0123], [0137], [0151], Figs. 2C, 5C, 7C, 9D, 11D. *Hu* grows gate layers in “selective areas defined by opening in an SiO₂ mask.” *Hu*, 1 (sequential

masking and etching). *Smith* fabricates its gate structure by patterning the **GaN cap layer**, using conventional etching to remove portions of it, then forming a **gate electrode** on the GaN segment. *Smith*, [0040]-[0041] (sequential masking and etching). *Smith* also uses **self-aligned** techniques. *Smith*, [0041]-[0044], Figs. 6A-6C. *Saxler* discloses sequential masking, etching, and deposition steps to form its stacked gate structure. *Saxler*, [0064]-[0066]. *Suh* likewise etches “to define a gate region where the p-type AlGaN cap 11 is located,” and depositing the gate on top. *Suh*, [0056] (sequential masking and etching).

[061] *Beach* makes a self-aligned two-layer gate structure using a single photomask. *Beach*, [0040], [0045], [0054]. *Ahn*, published in 1999, likewise uses a single mask and further discloses isotropic and anisotropic etching techniques to create stacked gate structures having stepped features and sloped sidewalls, as shown below. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C.



Ahn, Fig. 4C.

[062] In addition, long before the '347 patent, *Shenoy* discloses techniques to isotropically etch and undercut metal layers below masks, which a POSITA would understand would be one method of forming stepped gate structures. *Shenoy*, 2-3. Lift-off had similarly been known for decades to undercut photoresists for creating stepped structures. Ex. 1023.

[063] Typical GaN HEMT devices thus included every feature and method of making the enhancement mode transistor claimed in the '347 patent.

IX. CLAIM CONSTRUCTION

[064] I am not an attorney. However, I have been informed by counsel of certain legal standards that apply with respect to claim construction and indefiniteness, and have used those standards, described below in formulating my opinions.

[065] I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent (Ex. 1002). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his

patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term's plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent's written description, the patent's prosecution history, or both.

[066] I understand that claim interpretation may also be informed by “extrinsic evidence” (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the relevant time period.

[067] I am also informed by counsel that the applicant of the '347 patent can act as their own lexicographer, to set forth a definition of a claim term in the specification. The definition provided by the applicant can differ from the claim term's plain and ordinary meaning. I have also been informed by counsel that when a patent claim uses the term “comprises” as a transitional statement after the preamble, there is a presumption that the claim is open-ended and not limited to the recited elements.

[068] I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '347 patent, other than as identified below.

[069] Based on my review of these materials and my personal knowledge and experience, I have considered the plain and ordinary meaning of each term of the '347 patent as it would have been understood by one skilled in the art at the earliest claimed priority date of the '347 patent of April 8, 2009. I apply the plain and ordinary meaning of each claim term throughout this declaration, other than as identified below.

- A. forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer” [claim 1], [1f]**

[070] In a related matter, the parties proposed:

Petitioners'	Patent Owner's
“forming side surfaces of the p-type gate material <i>such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces that contact the barrier layer</i>”	“forming side surfaces of the p-type gate semiconductor material <i>such that the bottom of the material, which contacts the barrier layer, is wider than the top of the material</i>”

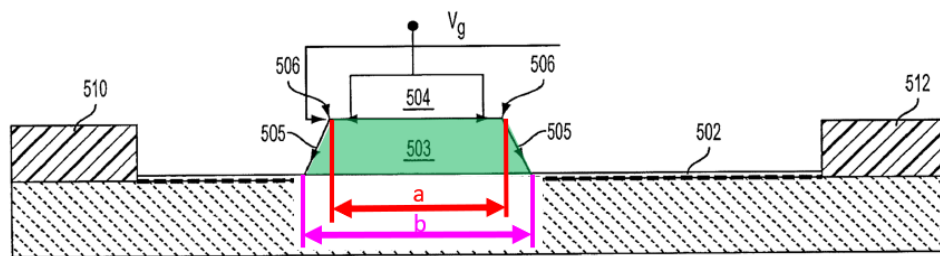
Ex. 1028.

[071] As I will explain below, the challenged claims are unpatentable under both constructions because a 10% slope will also be wider on the bottom than the top, so this term need not be construed. In my view, the construction agrees with the disclosure of the prior application, *Lidow*, which provides support for the present claims (§VI.B (Prosecution History)). *Lidow* discusses the advantage of using sloped sidewalls in a p-type GaN gate layer to reduce gate leakage. *Lidow*, [0041]-[0042], Fig. 8. The only way *Lidow* distinguishes its sidewalls is by indicating that a “base that is more than 10% wider than the top” advantageously “causes a longer path for electrons to travel between the gate metal 17 and the

2DEG along the pGaN side wall,” thereby “result[ing] in lower gate leakage.” *Id.*, [0042]. *Lidow*’s depicts and describes the same p-type layer and gate structure that the ’347 patent discloses. *Id.*, Fig. 8; Ex. 1001, 3:49-64, Fig. 5. The construction thus enables the purpose of the element—reducing gate leakage, including through the conventional method of sloping the sidewalls to increase the length of sidewall leakage path 201. Ex. 1001, Abstract, 1:19-23, 2:15-43, 3:60-4:7, 4:34-45, Figs. 2, 4, 7A-7B, 8.

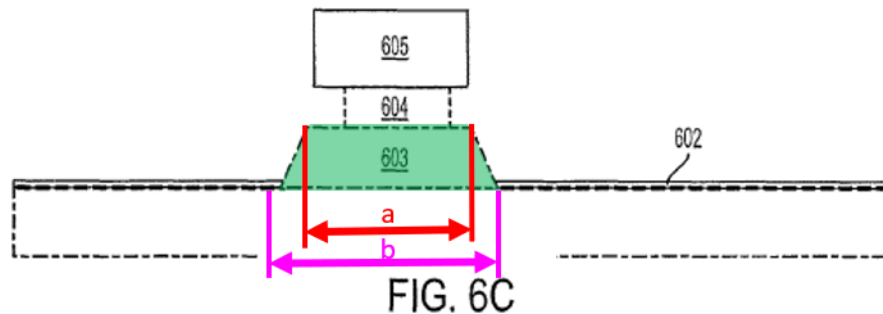
[072] Aside from the 10% guidance, *Lidow* provides no other explanation of how much slope would be necessary to achieve the alleged improvement of the ’347 patent, reduced gate leakage. Explicit guidance on the amount of slope would be needed to distinguish the claim from the prior art because nearly all layers have at least slightly sloped sidewalls. Few structures, if any, have perfectly vertical sidewalls in practice, even if depicted as vertical in functional diagrams, a point that which *Saxler* notes. *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5; *infra* §XIII.B.5 (Ground 4, Limitation [1d]). *Lidow* controls the shape of the p-type GaN material during etching to achieve a base 10% wider than the top and gain the alleged benefits of lower gate leakage due to a longer leakage path as compared to leakage rates in the prior art. *Lidow*, [0041]-[0042]. Petitioners’ construction makes this distinction clear, unlike Patent Owner’s construction.

[073] Petitioner's construction likewise agrees with the '347 patent specification. For example, the '347 patent shows a **p-type gate material** with sloped side surfaces whose bottom surface is more than 10% wider than the top. Ex. 1001, Figs. 5, 6C, 7B.



Ex. 1001, Fig. 5.

Width “b” above is approximately 1.32 times the width of “a” (~30% wider), and the same holds true for Figures 6C and 7B (“b” is 1.36 times wider than “a” in 6C and 1.34 times wider in 7B). If the Patent Owner argues that Fig. 5 and 6C are schematic diagrams not intended to be drawn to scale, Fig. 7B is an actual image of the etched gate structure, and my measurements confirm it has similar dimensions to Fig. 5 and Fig 6C.



Ex. 1001, Fig. 6C.

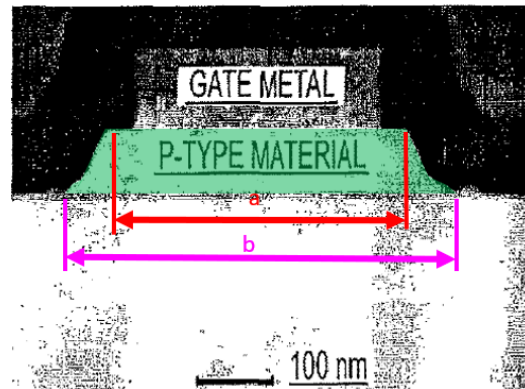


FIG. 7B

Ex. 1001, Fig. 7B

[074] All combinations meet Petitioner’s construction. If Patent Owner’s broader construction is accepted, the patent is also unpatentable under all grounds.

B. “etching the gate metal and the p-type gate material” [claim 1], [1g]

[075] In a related matter, parties proposed:

Petitioners'	Patent Owner's
<i>"using the photoresist to etch the gate metal and the p-type gate material"</i>	<i>"Etching the gate metal and etching the p-type gate material."</i>

[076] The challenged claims are unpatentable under both constructions as both materials will be etched under either construction. The Board need not construe this term to resolve a dispute.

C. "etching the gate metal to form a pair of ledges" [claim 1], [1i]

[077] In a related matter, the parties proposed:

Petitioners'	Patent Owner's
<i>"after the etching of the gate metal and the p-type gate material, etching the gate metal to form a pair of ledges"</i>	<i>"Performing a process during which gate metal is removed and two ledges are created."</i>

[078] The challenged claims are unpatentable under both constructions, as the process of etching the metal a second time to form ledges will remove gate metal.

X. Ground 1: *Saxler* in View of *Beach* and *Shenoy* Renders Obvious Claims 1-3

A. Overview of Ground 1

[079] *Saxler* makes a GaN HEMT using a sequence of forming, masking, and etching steps. In my opinion, *Saxler*'s device includes every feature of devices made according to the method of the '347 patent's claims. For example, *Saxler* masks and etches the p-type gate material and gate metal to form the stepped, stacked gate structure. And although not explicitly disclosed, it is my opinion that a POSITA would have understood that *Saxler* uses a photomask to etch the gate material because *Saxler* requires precise position of its gate that is achievable using a conventional masking approach. Further, in my view, a POSITA would have found it obvious modify *Saxler*'s methods with *Beach*'s and *Shenoy*'s techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal using a single mask to obtain self-aligned ledges, resulting in the same gate structure that *Saxler* discloses.

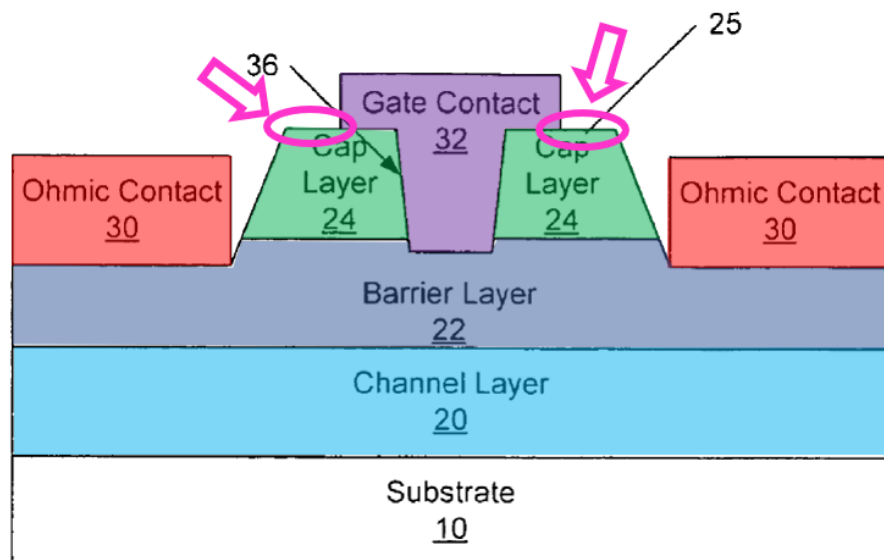
1. *Saxler*

[080] *Saxler* discloses a GaN transistor with high breakdown voltage. *Saxler*, [0006], [0007]-[0030], Figs. 1A, 2B. Below, I will explain how *Saxler*'s device discloses all features of the device made according the claimed method of

the '347 patent. As I illustrate below with color-coded highlighting, *Saxler* discloses making a GaN transistor with high breakdown voltage by:

1. Forming the **channel layer**, **barrier layer**, and **cap layer**.
2. Masking and etching the **cap layer** to expose the **barrier layer**, creating sloped sidewalls.
3. Depositing the **source and drain contacts**.
4. Forming a **gate contact**.

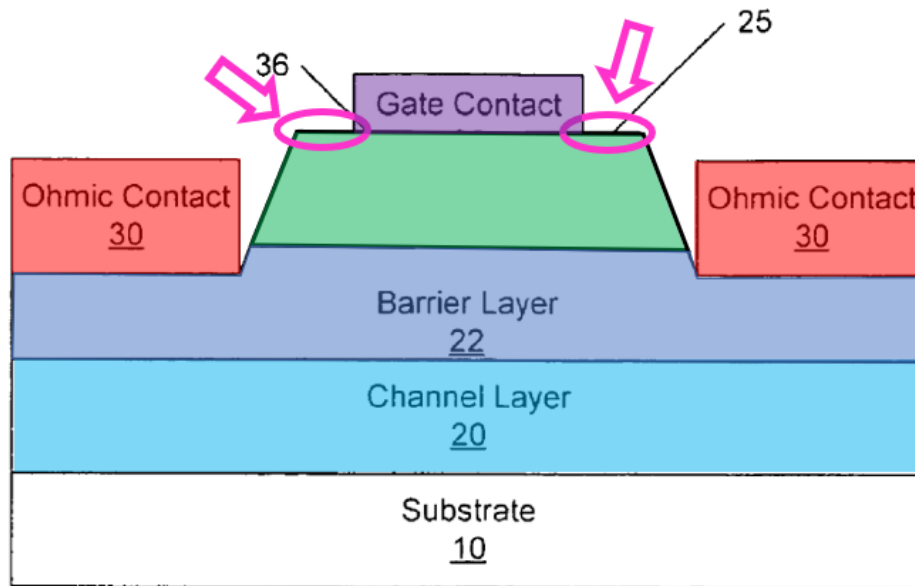
Saxler, [0057]-[0066].



Saxler, Fig. 1A.

[081] *Saxler*'s gate contact may be recessed or non-recessed (i.e., flat).

Saxler, [0052], [0066]. Where the gate recess is not utilized, *Saxler* would result in the following structure:



Saxler, Fig. 1A (modified).

[082] *Saxler*'s **channel layer 20** is a GaN layer grown on a GaN buffer layer, and *Saxler*'s **barrier layer 22** is a Group III-nitride that may be AlGaN. *Saxler*, [0057]-[0060]. The stacked gate structure above the **barrier layer 22** consists of a **cap layer** and **gate contact** that is metal. *Saxler*, [0061]-[0063], [0066], [0071]-[0073], [0076], [0087]. *Saxler*'s **cap layer** is a p-type gate material that may include a "p-type dopant" in a subregion or doped throughout the layer. *Saxler*, [0013], [0069], [0071], [0073].

[083] *Sheppard*, incorporated by *Saxler* to provide methods of fabricating *Saxler*'s GaN HEMTs (*Saxler*, [0046], [0068]), describes a similar process. *Sheppard*, [0044]-[0051], Figs. 1A-1F.

[084] *Saxler* also incorporates *Smith* by reference (*Saxler*, [0087]), to disclose methods of making gate structures which explicitly discloses using “conventional photolithographic techniques and mask alignment tools” to precisely position the gate contact close to or flush with the cap layer using one or two masks, including a “self-aligned” technique. *Smith*, [0041]-[0044], Fig. 4A-4C, 5A-5B, 6A-6C, claim 25.

[085] *Saxler* expressly recognizes that various other HEMT structures would be compatible with its embodiments, and explicitly includes *Smith*'s devices among such options. *Saxler*, [0087]. *Smith* discloses non-recessed gate electrodes in stacked structures that are similar to *Saxler*'s recessed stacked gate structure. *Smith*, [0033], [0041], Figs. 3, 5B. *Smith* states that “there is no benefit to recessing the gate down to the barrier layer” in GaN HEMT devices “because the top surface of GaN is generally not conductive.” *Id.*, [0010]. And although *Smith* briefly discloses using T-shaped gate electrodes for “microwave and RF” applications (*Smith*, [0017], [0034], claim 20), *Smith* otherwise only discloses stacked gate structures having a **GaN cap layer** with a non-recessed **gate electrode** (*id.*,

[0033]-[0037], [0039]-[0043], claim 1, Figs. 3, 4A-4C, 5A-5B). Just like *Saxler*, *Smith*'s GaN HEMT also includes a **GaN channel layer** and **AlGaN barrier layer** (inducing a **2DEG region**), and **source** and **drain electrodes**. *Smith*, [0030]-[0037], [0041]. A POSITA would thus have understood non-recessed electrodes were a suitable option for *Saxler*'s GaN, which bears substantially the same layers and structure.

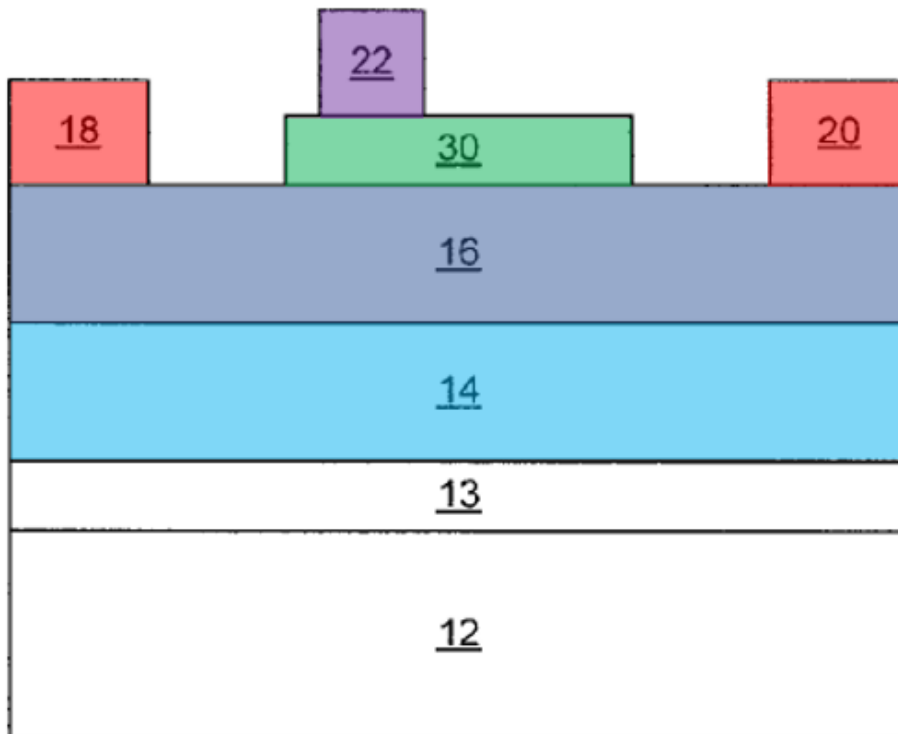
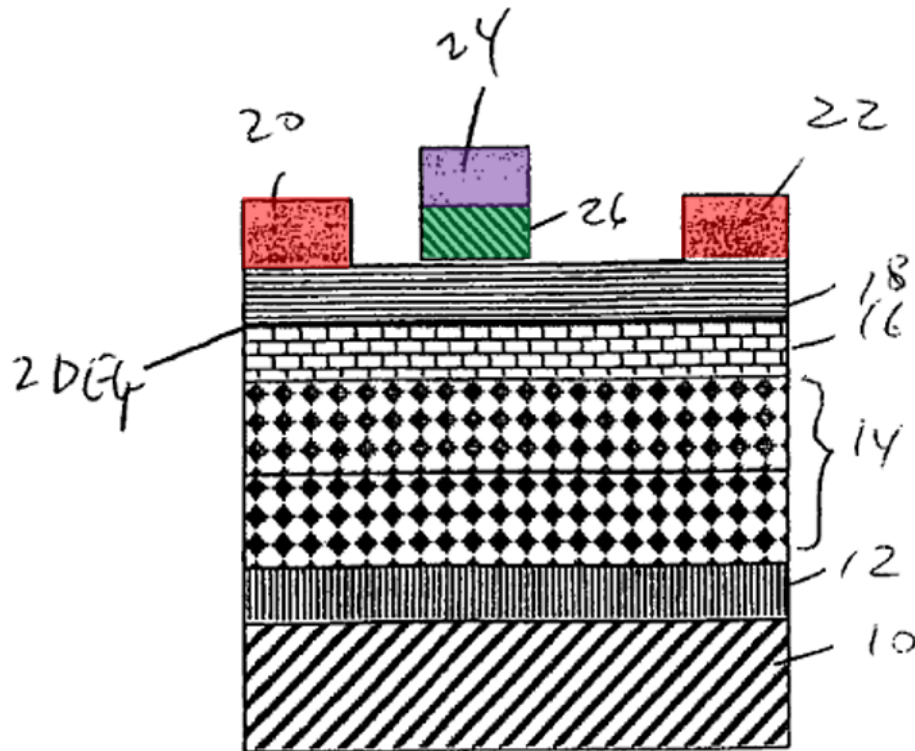


Figure 5B

Smith, Fig. 5B.

2. Beach

[086] *Beach* describes GaN enhancement-mode devices. *Beach*, Abstract, [0003]-[0018]. *Beach* uses a self-aligned method to make stacked gate structures in GaN HEMT devices that relies on using just one mask, a well known approach at the time. *Id.*, [0040], [0045], [0054]. *Beach* provides steps to deposit and pattern these layers with a single mask to make a **gate barrier 26** and **gate arrangement 24** above a p-n junction and between **power electrodes**, as I have illustrated below in color coded shading. *Beach*, [0040]. These self-aligned techniques were common in the field as of relevant date for the '347 patent. *Beach*'s "gate arrangement 24" includes a **gate electrode**, which is a metal, and **gate barrier 26**, which is a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F.



Beach, Fig. 1.

3. *Shenoy*

[087] *Shenoy*, which published February 22, 1996, well over a decade before the '347 patent's asserted priority date of April 8, 2009, describes well known techniques of using isotropic etching to undercut the metal below photoresist masks. *Shenoy*, 2-3. *Shenoy* provides method to control the “**undercut U**,” illustrated in Figure 1, which evolves symmetrically on both sides of a symmetric photomask such that the width of the etched metal structure is less than the photomask. *Shenoy*, 2-3. *Shenoy*'s methods were conventional for etching metals in semi-conductors as of the relevant date of the '347 patent.

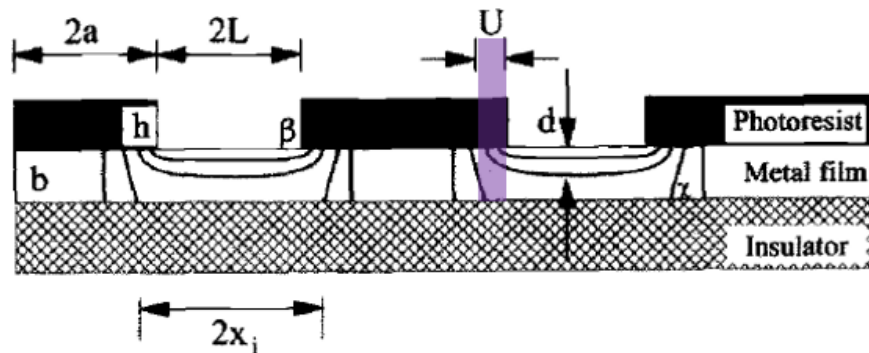


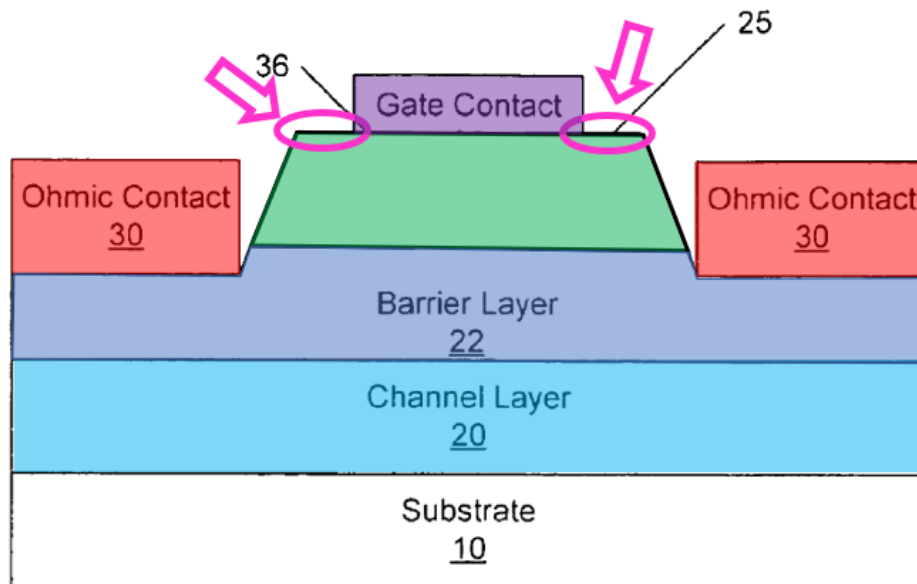
Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

Shenoy, Fig. 1.

[088] At least as of April 8, 2009, and as early as its publication date of February 22, 1996, I understand that *Shenoy* was publicly available and disseminated. *See Shenoy*, 1; Ex. 1025 (Declaration of Kelley Hazel). In my opinion, a POSITA designing GaN transistors routinely would have accessed similar scholarly articles and would have looked to *Shenoy* for its techniques of etching metals.

4. Combination of *Saxler*, *Beach*, and *Shenoy*

[089] The combination would yield the same structure as the non-recessed *Saxler* embodiment:



Saxler, Fig. 1A (modified).

5. Motivation to Combine

[090] In my opinion, a POSITA would have found it obvious to make *Saxler*'s stacked gate structure consisting of a cap layer and the gate contact of *Saxler*'s non-recessed embodiments using the methods of *Beach* and *Shenoy*.

[091] As I explained above, *Saxler* uses a sequence of steps to arrive at its stacked gate structure, include masking and etching the cap layer, removing the mask, then depositing the gate contact. *Saxler*, [0064]-[0066], Figs. 1A-1B; §X.A.1 (Ground 1, *Saxler*). In my opinion, a POSITA would have understood a second mask would be used to deposit the gate contact in its non-recessed embodiments, then removed, because *Saxler* uses this approach for its recessed embodiments as

does *Smith* in its non “self-aligned” embodiments. §§VIII (Technology Background, X.B.8 (Ground 1, Limitation [1g]), X.B.8 (Ground 1, Limitation [1g]), X.B.10 (Ground 1, Limitation [1i]); *Smith*, [0041], Figs. 4A-4C; *Saxler*, [0065]-[0066]. *Smith* is incorporated by reference to disclose methods of making gate structures. *Saxler* [0046], [0087]. In its non “self-aligned” embodiments, *Smith* discloses using “using conventional photolithographic techniques and mask alignment tools” to position the gate, i.e. it uses two masks, one for the cap layer and one for the gate contact, in contrast to its “self-aligned” embodiments, which use one mask for the cap layer and gate. *Smith*, [0041]-[0044], Figs. 4A-4C, 6A-6C.

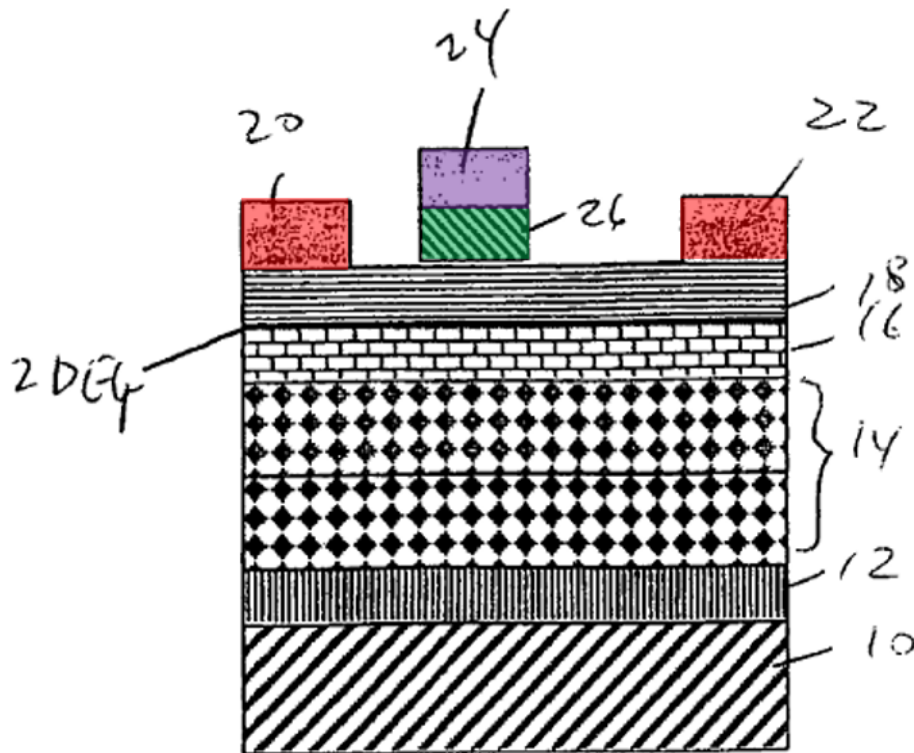
[092] In my view, there were numerous techniques available and known to a POSITA to make *Saxler*’s gate structure, and a POSITA would have been motivated to simplify this process and reduce costs by using fewer masking steps. *Smith*, for example, teaches a “self-aligned” approach that does not include a pair of horizontal ledges, and a POSITA would have been motivated to look for methods of using that self-aligned approach to more precisely make symmetric ledges. *Smith*, [0042].

[093] Manufacturing methods were used interchangeably at the time, and a POSITA would have been familiar with many ways to create *Saxler*’s stepped gate

structure in its non-recessed embodiments and would have swapped them interchangeably. §VIII (Technology Background). In my opinion, a POSITA would have found it obvious to modify *Saxler* by using *Beach*'s self-aligned technique and *Shenoy*'s isotropic etching to arrive at *Saxler*'s same non-recessed gate structure, which would reduce steps and costs while improving reproducibility and symmetry of the gate contact with respect to the cap layer. A POSITA would have recognized this as a simple and predictable combination in light of *Smith*'s use of self-alignment techniques to create its stacked gate structure, which has flush sidewalls between cap layer and gate contact. *Smith*, [0041]-[0044], Figs. 4A-4C, 5A-5C, 6A-6C. In fact, *Ahn* discloses this same approach for making a stepped gate in a thin-film transistor. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C.

[094] As I explained above, *Beach* provides a method of making stacked gate structures in GaN HEMT devices that uses a single mask, which helps ensure alignment of layers. *Beach*, [0040], [0045], [0054];]; *Beach-II*, [0047]-[0048]. *Beach*'s gate structure includes the "gate arrangement 24," which comprises a gate electrode, and an underlying "gate barrier 26," which is a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F. *Beach*'s process (i) deposits "gate barrier 26" and "gate arrangement 24" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits power electrodes. *Beach*, [0040].

A POSITA would have understood *Beach*'s "self-aligned" techniques would have used a single photomask, as described in greater detail another *Beach* publication. *Beach-II*, [0047]-[0048]. Such self-aligned techniques were common in the field as of relevant date.



Beach, Fig. 1.

[095] In my opinion, a POSITA would have found it obvious to use *Beach*'s approach to create *Saxler*'s gate structure, which would have improved alignment between layers, reduced steps, and reduced costs. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3. It would have been obvious to look to *Beach* for its simple methods of making stacked gate structures. Indeed, *Sheppard*, expressly incorporated by *Saxler* to

disclose methods of fabricating GaN HEMTs (*Saxler*, [0046], [0068]), describes a flexible approach to masking and etching. It notes that “operations described as multiple steps could be combined into a single step” (and vice versa), making the choice of *Beach*’s manufacturing steps no more than simple substitutions.

Sheppard, [0058].

[096] While *Beach* does not disclose steps to create the **horizontal ledges** of *Saxler*’s stacked gate structure following its self-aligned process, *Shenoy* does. As previously explained, *Shenoy* discloses simple isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks. *Shenoy*, 2-3; §X.A.3 (Ground 1, *Shenoy*).

[097] Thus, in my opinion, an ordinary artisan would have found it straightforward and obvious to use *Beach*’s self-aligned method of making *Saxler*’s stacked gate structure in a GaN HEMT and *Shenoy*’s methods to undercut the **gate electrode** to create *Saxler*’s **horizontal ledges**. Indeed, such a combination of steps was already known in the art for creating stepped, stacked transistor gates. *Ahn*. It is my opinion that a POSITA would have found the combination a simple substitution of *Beach*’s and *Shenoy*’s known methods that could be predictably implemented in *Saxler*’s flexible method of manufacturing to

improve alignment and symmetry between layers and reduce steps and costs.

Saxler, [0046], [0068]; *Sheppard*, [0058].

[098] It would have been simple and predictable to use the known techniques of *Beach* and *Shenoy*, which were among the many ways to obtain the *Yoshida-Saxler* gate structure. The '347 patent was allowed without disclosing any particular method to etch the gate metal and obtain the claimed ledges because such methods were well within the skill level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§VIII (Technology Background), VI.B (Prosecution History). Appropriate methods such as lift-off when removing the photomask or isotropic etching were well within the level of ordinary skill. §VIII (Technology Background); Ex. 1023. As a reason for the allowance, the Examiner identified that the cited art did not disclose forming sloped sidewalls of its p-type gate material in structures that also had ledges. Ex. 1002, 29, 55. But *Saxler* discloses such sloped sidewalls with the claimed ledges, and *Beach* and *Shenoy* would have provided a known, obvious way to create that structure. §§X.A.1 (Ground 1, *Saxler*), X.A.4-X.A.5(Ground 1, Combination and Motivation).

B. Independent Claim 1**1. [1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:**

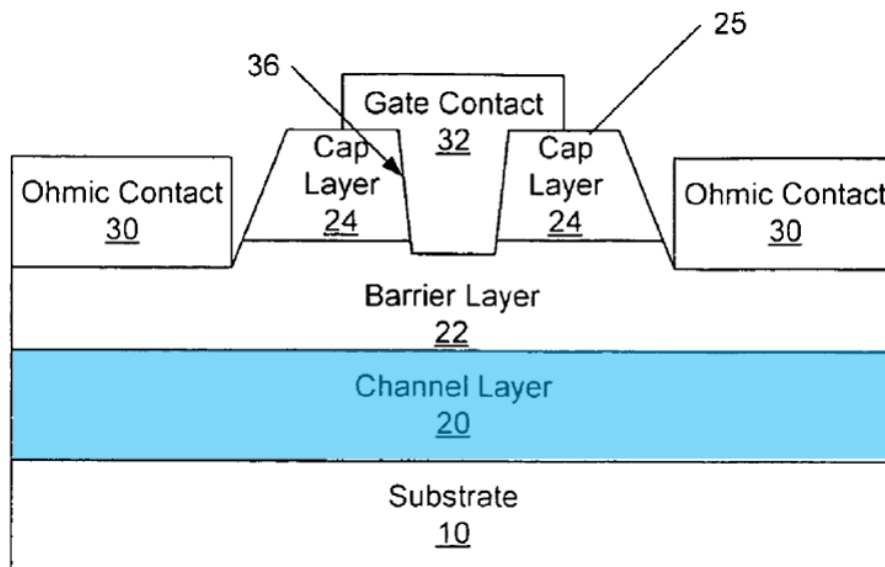
[099] *Saxler* discloses or at least renders obvious the preamble. *Saxler* discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer. *Saxler*, [0007]-[0010], [0046], [0059]-[0064], Figs. 1A, 1B. Although *Saxler* does not use the phrase “enhancement mode,” this transistor indeed constitutes a normally-off enhancement-mode GaN transistor when these p-type dopants are placed in the cap layer, as *Saxler* discloses.

[100] A POSITA would have understood *Saxler*’s transistors were enhancement-mode GaN transistors at least because of their gate structure, which is one of the defining features of enhancement-mode transistors. For example, *Sheppard*, which *Saxler* expressly incorporates (*Saxler*, [0046], [0068], (referencing Ser. No. 10/897,726)), likewise discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer, where the cap layer “moves the top surface of the device physically away from the channel, which may reduce the effects of the surface,” and when the cap layer is doped p-type this will constitute a normally-off enhancement-mode GaN transistor. *Sheppard*, [0014], [0040], [0042], Fig. 1F.

2. [1a] forming a GaN layer;

[101] As an initial matter, the '347 patent admits Limitation [1a] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B. I agree.

[102] *Saxler* discloses a **GaN channel layer**. *Saxler*, [0007], [0010], [0016], [0057]-[0058], [0069], Figs. 1A-1F. It describes methods to form the GaN channel layer. *Saxler*, [0057].

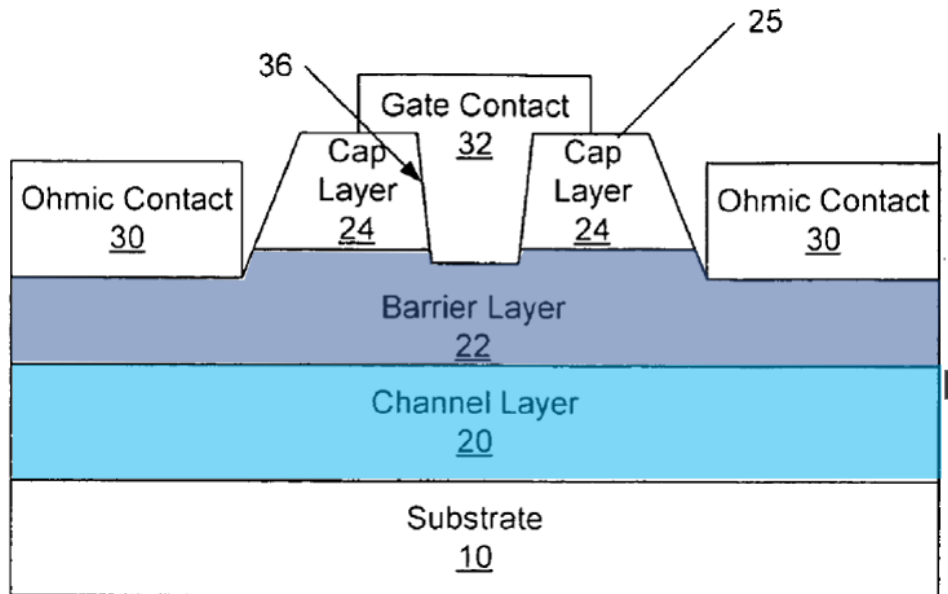


Saxler, Fig. 1A.

3. [1b] forming a barrier layer on the GaN layer;

[103] The '347 patent admits Limitation [1b] was conventional. Ex. 1001, 1:27-2:21, Figs. 1-2, 3A-3B.

[104] *Saxler* discloses Limitation [1b]. *Saxler*'s **barrier layer 22** is formed on its GaN **channel layer**. *Saxler*, Abstract, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B.



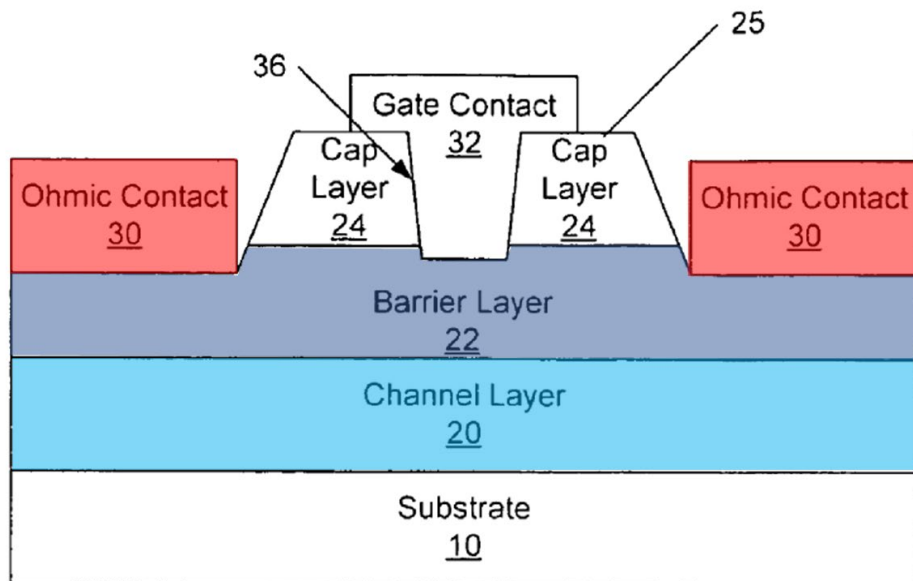
Saxler, Fig. 1A.

[105] *Saxler*'s barrier layer may be an AlGaIn layer. *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B. The '347 patent likewise discloses that the claimed barrier layer may be an AlGaIn layer. Ex. 1001, 1:37-58, 3:32-43, 4:10-16.

4. [1c]: depositing source and drain contacts on the barrier layer;

[106] Again, the '347 patent admits Limitation [1c] was conventional, and I agree. Ex. 1001, 1:64-2:19, Figs. 1-2, 3A-3B.

[107] Such source and drain contacts were wholly conventional in GaN transistors, and *Saxler* discloses “ohmic contacts 30” that may “provide **source** and **drain contacts**” formed on barrier layer 22. *Saxler*, [0065], Figs. 1A, 2B.



Saxler, Fig. 1A.

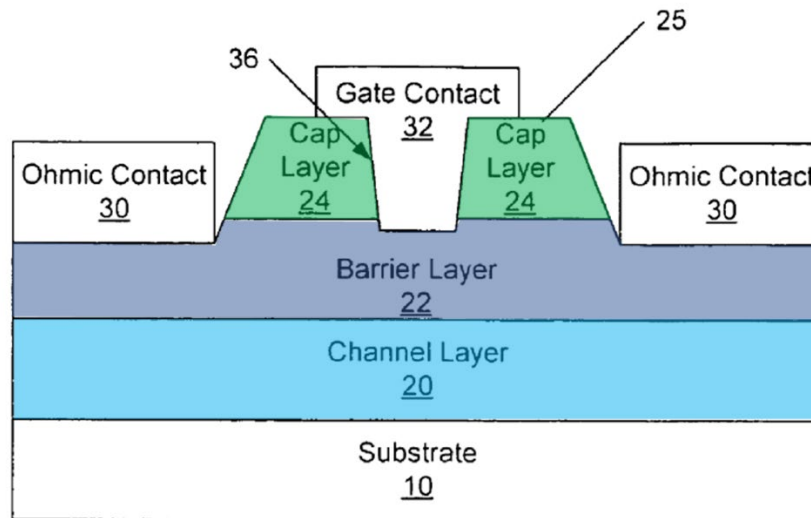
5. [1d]: depositing a p-type gate material on the barrier layer,

[108] As with the other limitations, the patent also admits Limitation [1d] was conventional. Ex. 1001, 1:37-2:21, Figs. 1-4, 7A. I agree.

[109] *Saxler* discloses Limitation [1d]. *Saxler*’s **cap layer** is a p-type gate material on the AlGaN **barrier layer**. *Saxler*, [0010], [0013], [0059]-[0063], [0069], [0071], [0073], Figs. 1A, 2B. The **cap layer** “may be blanket formed on

the barrier layer 22 and may be epitaxially grown and/or formed by *deposition*.”

Saxler, [0061].



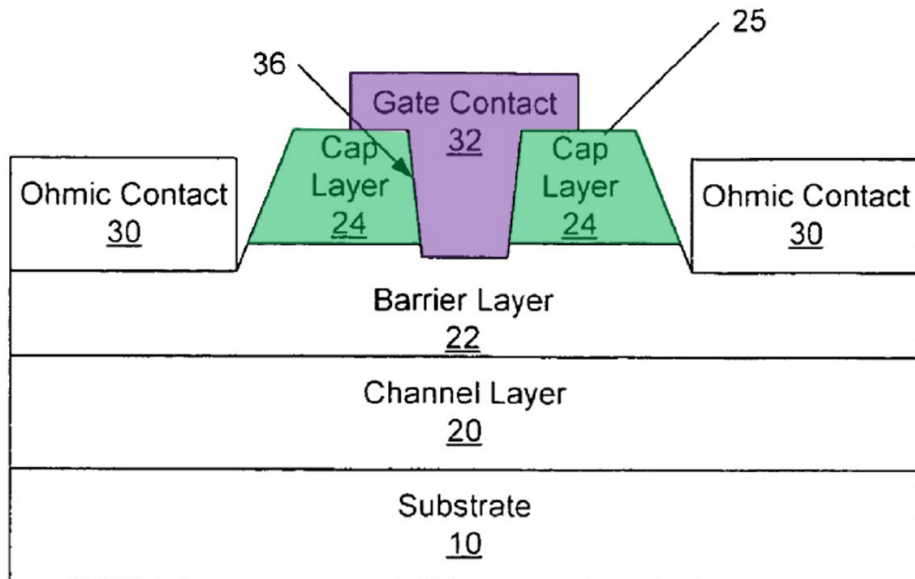
Saxler, Fig. 1A.

6. [1e]: depositing a gate metal on the p-type gate material;

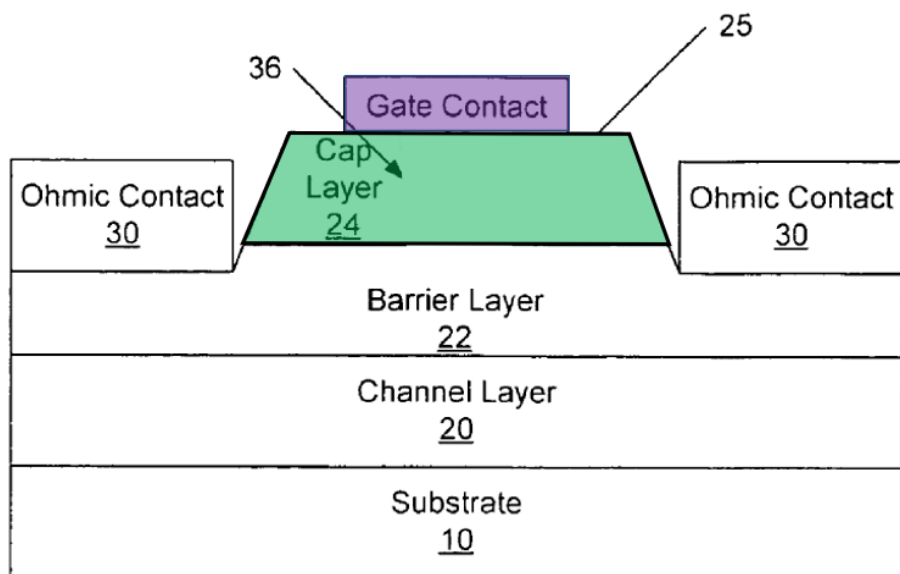
[110] The patent admits [1e] was conventional, and I agree. Ex. 1001, 1:24-2:21, Figs. 1-4, 7A.

[111] In my opinion, *Saxler* renders obvious [1e]. *Saxler*’s **gate contact** is a gate metal (e.g., “Ni, Pt, NiSi_x, Cu, Pd, Cr, W and/or WSiN”) formed on its **cap layer**. *Saxler*, [0066], Figs. 1A, 2B. As I explained, in some embodiments *Saxler* lacks a gate recess and does not separate the **cap layer** into distinct portions, and in such embodiments (as well as the recessed embodiments), *Saxler* deposits its gate contact on the cap layer. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064],

[0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; §X.B.9 (Ground 1, Limitation [1h]).



Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

7. [1f]: forming a photoresist over the gate metal;

[112] *Lidow*, the prior application, admits Limitation [1f] was conventional because ledges in a “conventional enhancement mode transistor” are made using separate masks for the p-type gate material and gate metal. *Lidow*, [0006], Fig. 1. I agree this step was conventional.

[113] In my opinion, a POSITA would have found it obvious to form a photoresist over the gate metal in view of *Saxler*, as claimed. §X.A.1 (Ground 1, *Saxler*). *Saxler* precisely positions its gate contact in the center of its cap layer or precisely position the gate contact off-center. *Saxler*, [0065] (gate recess contact closer to source than drain in “particular embodiments”), Figs. 1A-1B, 2A-2B (centered). A POSITA would have understood such precession when placing the gate contact would have been achievable using conventional masking and etching techniques, which would have involved forming a photoresist over the gate metal. §X.A.1 (Ground 1, *Saxler*). This was just one of many methods for forming stacked, stepped gate structures that a POSITA would have known. §VIII (Technology Background).

[114] Further, in my opinion, *Saxler*, *Beach* and *Shenoy* also render obvious Limitation [1f]. *Beach*, for example, forms a photoresist over the gate metal, specifying that “the stack is patterned and etched to obtain gate arrangement 24

over gate barrier 26.” *Beach*, [0040]; *Beach-II*, [0047]-[0048]. *Shenoy* similarly describes using a photoresist over a metal electrode. *Shenoy*, 1.

[115] In view of the above, in my opinion it would have been obvious to combine *Saxler* with *Beach* and *Shenoy*’s techniques of using a single photomask over *Saxler*’s gate metal and cap layer when making *Saxler*’s non-recessed GaN HEMT device. §X.A.5 (Ground 1, Motivation to Combine).

8. [1g]: etching the gate metal and the p-type gate material,

[116] *Lidow*, the prior application, admits Limitation [1g] was conventional under Patent Owner’s construction because ledges in a “conventional enhancement mode transistor” are made using separate masks for the p-type gate material and gate metal, thereby admitting it was known to “etch[] the gate metal and etch[] the p-type gate material” (Patent Owner’s construction). *Lidow*, [0006], Fig. 1; §IX.B (Claim Construction). I agree.

[117] In my opinion, *Saxler* discloses or at least renders obvious this limitation under the proper construction, which is “*using the photoresist to etch the gate metal and the p-type gate material.*” §IX.B (Claim Construction). *Saxler* etches the cap layer “to expose the underlying barrier layer” and place the source and drain contacts. *Saxler*, [0064], Figs. 1A-1B. *Saxler* also discloses or at least renders obvious etching the gate metal using the same photoresist. As explained, a

POSITA would have understood depositing *Saxler*'s gate contact would have involved masking and etching the gate metal to precisely place the gate. §§X.A.1 (Ground 1, *Saxler*), X.B.7 (Ground 1, Limitation [1f]).

[118] *Saxler*, *Beach* and *Shenoy* also renders obvious Limitation [1g] in my opinion. *Beach* uses just one mask when etching the gate metal and p-type gate material, specifying that both layers of “the stack [are] patterned and etched to obtain gate arrangement 24 over gate barrier 26.” *Beach*, [0040]; *Beach-II*, [0047]-[0048], *Shenoy* employs the same approach. *Shenoy*, 1.

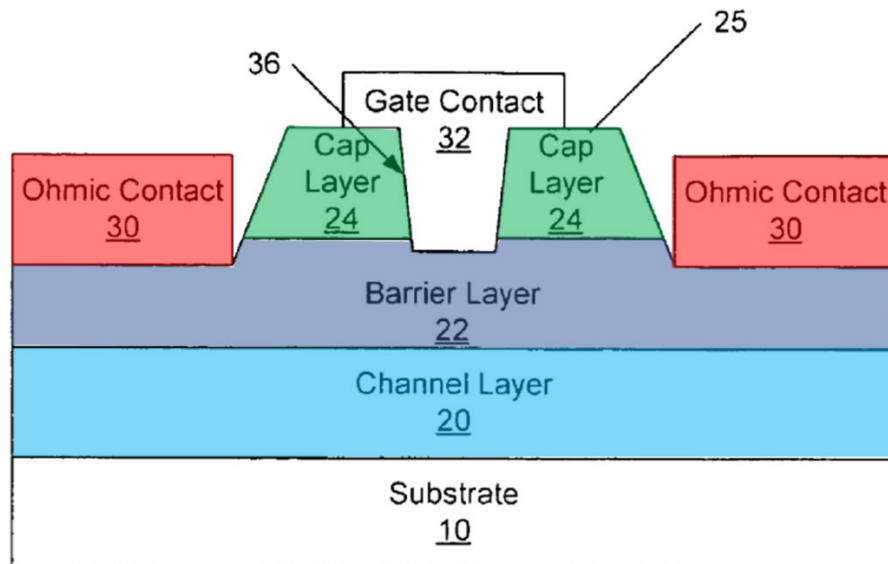
[119] In my opinion, it would have been obvious to combine *Saxler* with *Beach* and *Shenoy*'s techniques of masking and etching the gate metal and p-type gate material using a single photomask when making *Saxler*'s non-recessed GaN HEMT device. §X.A.5 (Ground 1, Motivation to Combine). This satisfies both parties' construction. §IX.B (Claim Construction).

9. **[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and**

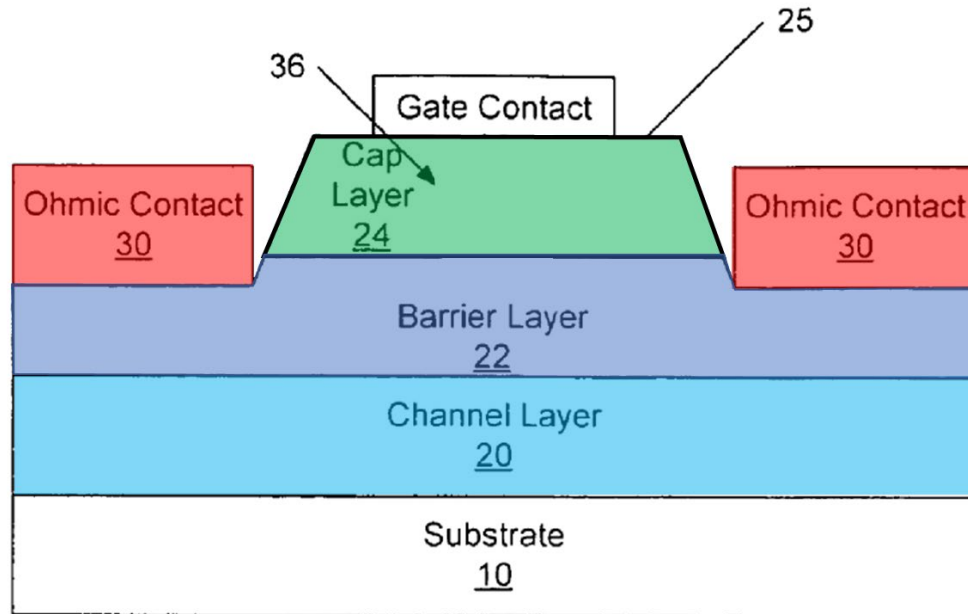
[120] The '347 patent admits Limitation [1h] was conventional, a point with which I agree. Ex. 1001, 1:37-2:21, Figs. 1-2, 3A-3B.

[121] *Saxler* discloses Limitation [1h]. *Saxler* etches the **cap layer** “to expose the underlying **barrier layer**” and place the source and drain contacts.

Saxler, [0064], Figs. 1A-1B. The sidewalls of the **cap layer** extend horizontally towards **source** and **drain contacts** and contact the **barrier layer** in both recessed and non-recessed embodiments.



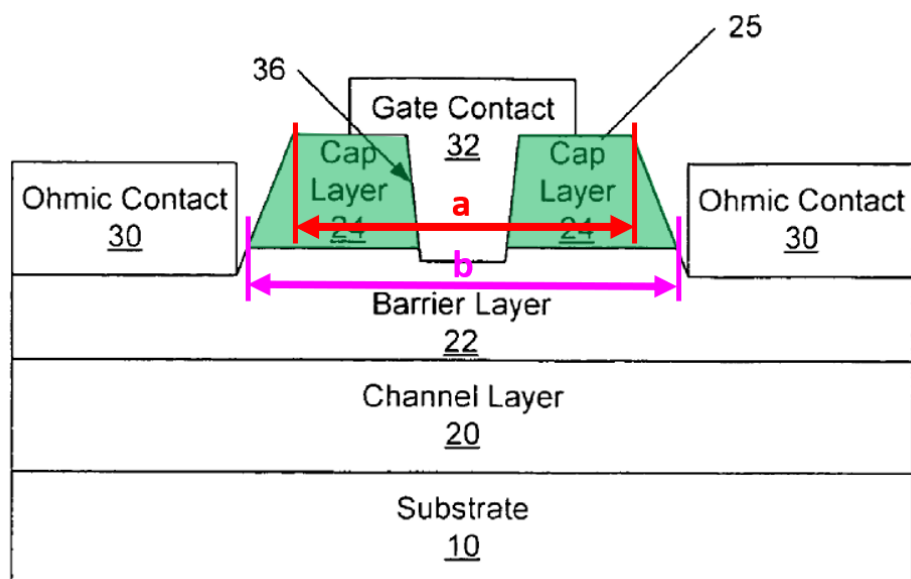
Saxler, Fig. 1A.



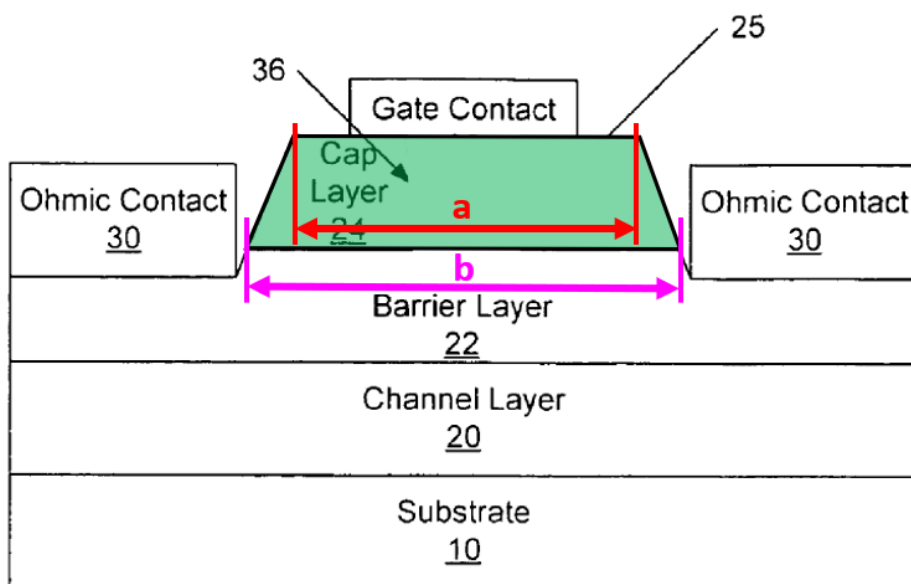
Saxler, Fig. 1A (modified).

[122] *Saxler* discloses “side surfaces of the p-type gate material.” The recess in *Saxler*’s cap layer 24 is optional, and where not employed the cap is a continuous material with sloped sidewalls. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88.

[123] In my opinion, *Saxler* also discloses both parties’ construction of the side surfaces limitation. *Saxler*, [0064], Figs. 1A, 2B; §X.A.1 (Ground 1, *Saxler*). In either the recess or non-recess *Saxler* embodiments, the bottom of the **cap layer** (length “**b**,” below) is about 1.25 times wider than the top (length “**a**”), i.e. more than 10% wider (Ground 1).



Saxler, Fig. 1A.

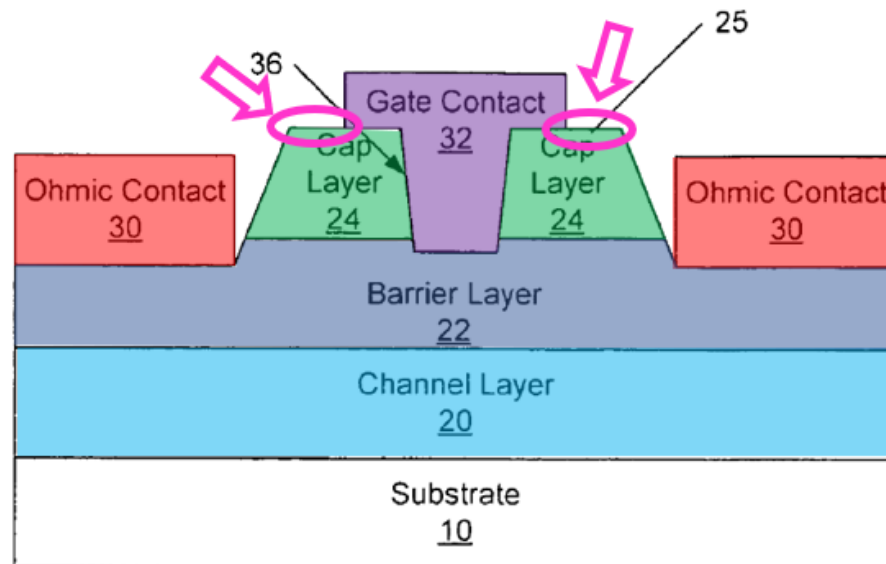
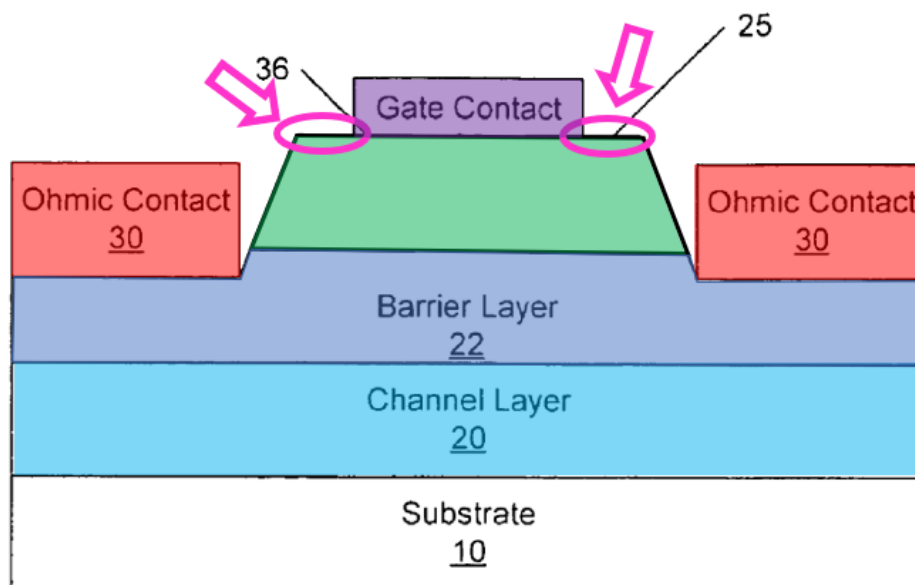


Saxler, Fig. 1A (modified).

10. [1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

[124] Limitation [1i] is the only feature of independent claim 1 that the '347 patent does not acknowledge is found in the prior art. Ex. 1001, 1:19-2:21, Figs. 1-4, 7A. Yet under Patent Owner's construction (§IX.B (Claim Construction)), *Lidow*, the prior application, notes this approach was conventional, stating that ledges in a "conventional enhancement mode transistor" are made using separate masks for the p-type gate material and gate metal. *Lidow*, [0006], Fig. 1.

[125] In my opinion, *Saxler*, *Beach* and *Shenoy* render Limitation [1i] obvious under either construction. *Saxler* depicts its **gate contact** is narrower than its **cap layer**, thereby exposing **horizontal ledges** on the **cap layer**. *Saxler*, Fig. 1F. *Saxler*'s non-recessed embodiments would have included these same features, as I show below. §X.A.1 (Ground 1, *Saxler*).

*Saxler, Fig. 1A.**Saxler, Fig. 1A (modified).*

[126] *Saxler* renders obvious making these **ledges** by etching the gate metal.

As I explained, a POSITA would have found it obvious use a single mask to etch

the gate metal and cap layer which would have allowed greater precision when placing the gate and would also have reduced manufacturing steps by reducing the number of masks employed. §§X.A.1 (Ground 1, *Saxler*), X.B.7-X.B.8 (Ground 1, [1f]-[1g]).

[127] Further, *Saxler*, *Beach* and *Shenoy* render obvious Limitation [1f]. *Shenoy* discloses methods of isotropically etching the gate metal to form symmetric undercuts of a photomask. *Shenoy*, 1-2; §X.A.3 (Ground 1, *Shenoy*). This long-known technique, applied to the mask of *Beach*, would have straightforwardly generated the pair of **ledges** on *Saxler*'s cap layer. In light of the many known ways to generate *Saxler*'s ledges, it is my opinion that a POSITA would have found it obvious to use *Beach* and *Shenoy*'s methods to build the structure of *Saxler*. §§VIII (Technology Background), X.A.5 (Ground 1, Motivation to Combine). This satisfies both parties' construction. §IX.C (Claim Construction).

- C. **[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.**

[128] Claim 2 recites nothing more than that the gate metal is narrower than the p-type gate material, but this is already required to form the **ledges** of Limitation [1i]. *Saxler*, [0014], [0046], claims 1, 18, 20, 29, Fig. 1F. As I explained

for Limitation [1i], *Saxler*, *Beach* and *Shenoy* render obvious the features of claim 2. §X.B.10 (Ground 1, Limitation [1i]).

D. [Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.

[129] In my opinion, the combination of *Saxler*, *Beach*, and *Shenoy* renders obvious Claim 3.

[130] *Beach* discloses a stacked “*self-aligned*” gate arrangement” using a single photo mask to etch both the “gate arrangement 24” (gate electrode) and the underlying “gate barrier 26” (GaN semiconductor), and this process is the same “self-aligned” process depicted in the ’347 patent at Figures 6A-6B. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Ex. 1001, 4:8-20; §§VI.1 (’347 Claims and Specification Overview), X.A.2 (Ground 1, *Beach*), X.A.5 (Ground 1, Motivation to Combine).

[131] As I have also explained, *Shenoy* etches a photomask to isotropically undercut the metal layer below the photomask, and this process is the same one shown in Figures 6B-6C of the ’347 patent. *Shenoy*, 2-3; Ex. 1001, 4:17-33; §§VI.1 (’347 Claims and Specification Overview), X.A.3 (Ground 1, *Shenoy*), X.A.5 (Ground 1, Motivation to Combine).

[132] In my opinion, it would have been obvious to use *Beach*’s self-alignment method and *Shenoy*’s undercutting techniques to predictably make

Saxler's gate structure, improving alignment, as I have previously explained.

§X.A.5 (Ground 1, Motivation to Combine).

XI. Ground 2: *Saxler* in view of *Yoshida*, *Beach*, and *Shenoy*

A. Overview of Ground 2

[133] As I have explained, *Saxler* discloses that its recessed gate is optional—in some embodiments there is no recess, and the gate contact sits flush on the cap layer. However, *Yoshida* also discloses and depicts a similar device having a p-type gate material without a gate recess, which further renders this modification obvious, in my opinion.

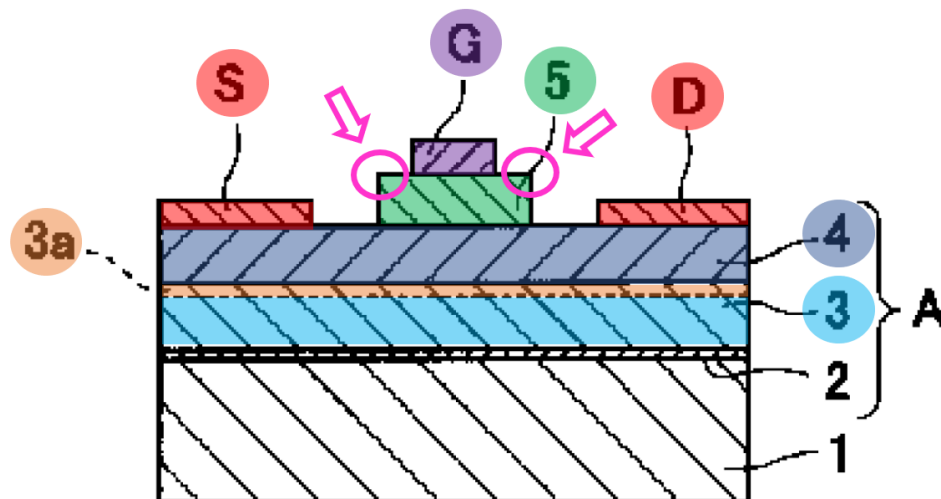
1. *Yoshida*

[134] *Yoshida* published ten years before the earliest possible priority of the '347 patent. *Yoshida* also discloses a normally-off enhancement mode GaN transistor having a p-type GaN layer below the gate that “enables voltage control with a small amount of carrier injection,” an arrangement that was entirely conventional by the time of the '347 patent. *Yoshida*, [0017], [0015], Fig. 1. *Yoshida* declares it improves breakdown voltages over prior art GaN transistors. *Yoshida*, [0008]-[0009].

[135] Just like *Saxler*'s channel and barrier layers, *Yoshida*'s **layer 3** is a GaN layer grown on a GaN buffer layer (layer 1) on a silicon substrate and **layer 4**

is an n-type semiconductor, and a **2DEG 3a** forms at their interface. *Yoshida*, Abstract, [0010], [0013], [0019]. The device includes a **source** and **drain** contact, as was conventional. *Yoshida*, Abstract, [0009].

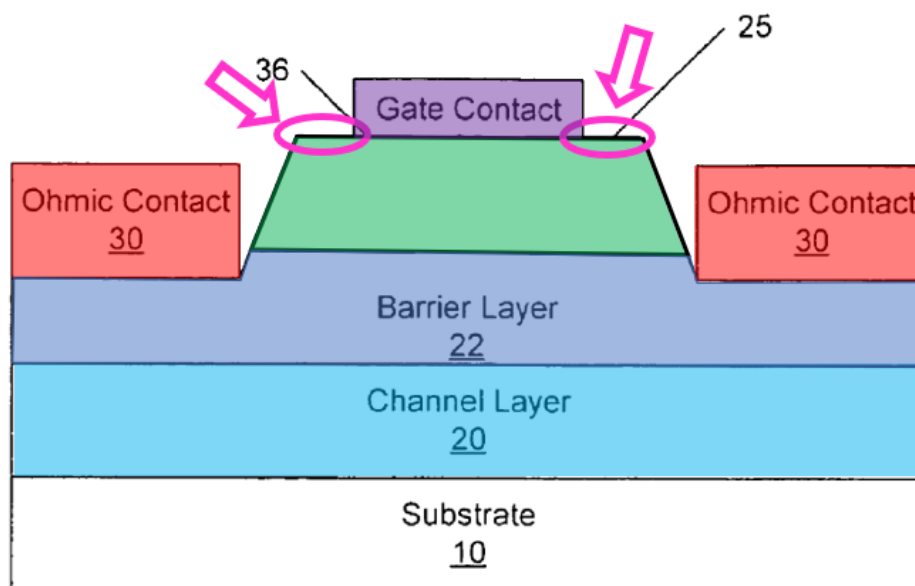
[136] *Yoshida* also discloses a stacked gate structure consisting of a **doped GaN layer** above the **semiconductor layer 4** and an overlying **gate metal**, with a pair of **horizontal ledges** on either side of the gate metal, like the ledges of *Saxler* and the '347 patent. *Yoshida*, Abstract, [0015], Fig. 1.



Yoshida, Fig. 1.

2. The Combination of *Saxler* in View of *Yoshida*

[137] Implementing *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure results in the following combined structure. The resulting structure has the same arrangement of components as *Saxler*'s non-recessed embodiment:



Saxler, Fig. 1A (modified).

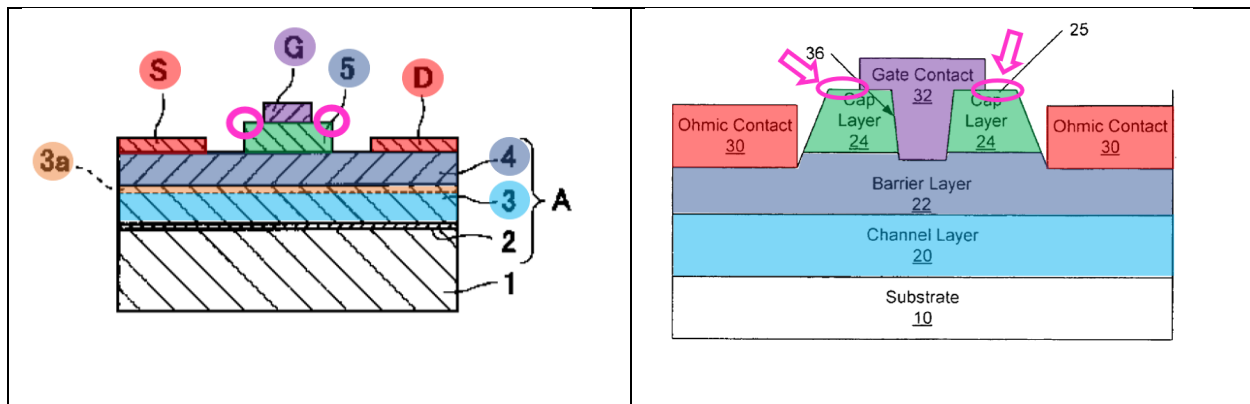
[138] In the combination, *Beach* and *Shenoy* would be used to form this gate structure of *Saxler-Yoshida*.

3. Motivation to Combine

a. *Saxler* and *Yoshida*

[139] In my opinion, it would have been obvious to implement *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure.

[140] The devices of these references are compatible. *Saxler* and *Yoshida* disclose compatible enhancement-mode GaN HEMT devices comprising the same layers performing the same functions, including stacked gate structures having a cap layer and gate metal. Both references describe gallium nitride HEMTs that they claim will improve breakdown voltages over the prior art. *Yoshida*, [0008]-[0009]; *Saxler*, [0006], [0007]-[0030]. Unsurprisingly, *Yoshida* and *Saxler*'s transistors share numerous overlapping features. As I illustrate below, they use the same arrangement of layers.



Yoshida, Fig. 1, *Saxler*, Fig. 1A

[141] As I explained above, *Yoshida*'s **layer 3** is GaN over a silicon substrate, as is *Saxler*'s **channel layer 20**. *Yoshida*, [0012], [0019]; *Saxler*, [0057]-[0058]. *Yoshida*'s **layer 4** is an n-type semiconductor, just like embodiments of *Saxler*'s **barrier layer 22**. *Yoshida*, Abstract, [0010], [0013];

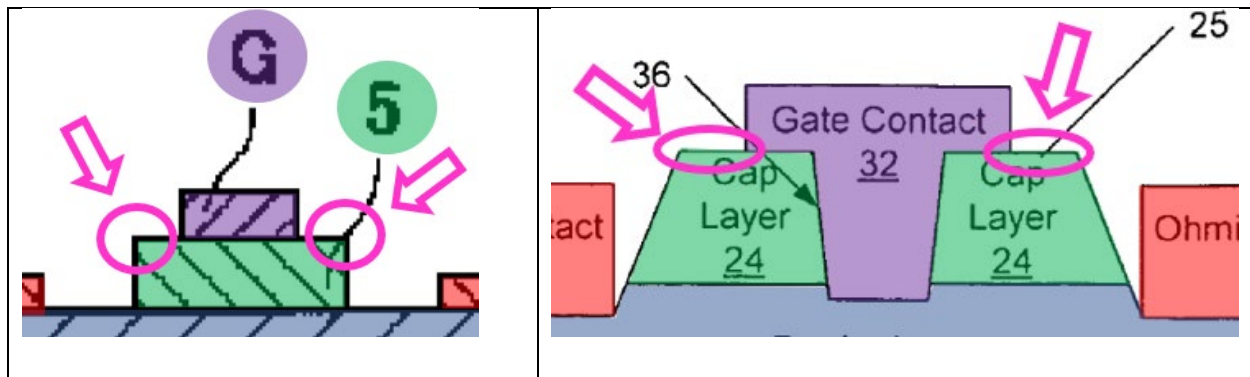
Saxler, [0059]-[0060]. Both have **2DEG regions** formed at the junction of these two layers, as was typical. *Yoshida*, [0016]; *Saxler*, [0004], [0006], [0008]. Both references have **source**, **drain**, and **gate metal** contacts, which was common.

Yoshida, Abstract, [0009]; *Saxler*, [0065]-[0066]. And both disclose a **doped layer** above the **barrier** and in contact with the **gate metal**, which also was common.

Yoshida, Abstract, [0015]; *Saxler*, [0069], Figs. 1A, 2B.

[142] While *Yoshida* and *Saxler* disclose slightly different topologies for their stacked gate structures, these structures perform identical functions in both references, which is, as *Yoshida* puts it, to control voltage “with a small amount of carrier injection” and “enable[] control of current flowing between channels” at high voltage. *Yoshida*, [0017]; *Saxler*, [0065].

[143] In the embodiments shown in *Saxler*’s figures, the gate metal occupies a recess in the cap layer extending into the barrier layer, and *Saxler* describes that this recess that may reach to touch the barrier layer in some embodiments but may not touch the barrier layer in others. *Saxler*, Abstract, [0007]-[0008], Figs. 1A, 2B. *Yoshida*’s gate metal, in contrast, sits flush on top of layer 5. *Yoshida*, Fig. 1. I have illustrated those structures below.



Yoshida, Fig. 1, *Saxler*, Fig 1A.

[144] *Saxler* states many times that this gate recess is optional. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88. And while its figures do not explicitly show a stacked gate structure without a gate recess, *Saxler*'s many statements that the recess is optional in view of the rest of *Saxler*'s description and figures disclose or at least render obvious the structure claimed by the '347 patent. To the extent Patent Owner disagrees that *Saxler*'s optional recess renders the claims of the '347 patent obvious (Ground 1), *Yoshida* further renders the claimed device obvious (Ground 2).

[145] In my opinion, a POSITA would have been motivated to combine *Saxler*'s and *Yoshida*'s gate structures and accompanying fabrication techniques and found it obvious to do so. A POSITA would have been familiar with many methods of making such stacked, stepped structures, as I explained above (§ VIII

(Technology Background)). Given the many interchangeable ways to fabricate such structures, it would have been obvious to combine *Saxler* and *Yoshida* to simplify manufacturing and decrease costs.

[146] For example, *Saxler* references and incorporates *Sheppard* (Ex. 1021) as disclosing “[s]uitable structures and techniques for fabricating GaN-based HEMTs” of *Saxler*’s embodiments. *Saxler*, [0046] (referencing Ser. No. 10/897,726), [0068] (same). To create the same gate recess as *Saxler* and deposit the gate metal, *Sheppard* discloses complicated and exacting manufacturing processes. *Id.*, [0043], [0046]-[0051], [0053]-[0056], Figs. 1C-1F, 2A-2B, Fig. 3. *Sheppard*’s GaN cap layer may be “about 2 nm to 500 nm thick,” for example, and its thin AlGaN underlying barrier layer is between “0.1 nm and about 40 nm.” GaN. *Id.*, [0040], [0042]. As a POSITA would have understood, manufacturing tolerances were accordingly extremely small, which raises complexity and costs of manufacturing to avoid costly out-of-tolerance defects. Further, with the recess, *Saxler*’s device is not enhancement mode (always off), and a POSITA would have been motivated to remove the recess to create an enhancement mode device and realize the benefits of a normally off device which renders it suitable for high power applications. *Suh*, 1.

[147] To avoid these problems, a POSITA would have been motivated to use *Saxler*'s non-recessed gate contact in its stacked gate structure in combination with *Yoshida*'s gate structure and accompanying fabrication techniques. That approach would have eliminated the exacting gate-recess manufacturing steps. In my opinion, a POSITA would have recognized *Yoshida*'s approach as a suitable option for solving such problems. And, as I explained above, a POSITA would have been familiar with a wide variety of stacked gate structures in GaN HEMT devices, including many without recessed gates, and thus found *Yoshida*'s and *Saxler*'s structures readily combinable and interchangeable.

[148] Indeed, *Saxler* expressly recognizes that various other HEMT structures would be compatible with its embodiments, and explicitly includes *Smith*'s devices among such options. *Saxler*, [0087]. *Smith* discloses non-recessed gate electrodes in stacked structures that are similar to *Saxler*'s recessed stacked gate structure. *Smith*, [0033], [0041], Figs. 3, 5B. *Smith* states that "there is no benefit to recessing the gate down to the barrier layer" in GaN HEMT devices "because the top surface of GaN is generally not conductive." *Id.*, [0010]. And although *Smith* briefly discloses using T-shaped gate electrodes for "microwave and RF" applications (*Smith*, [0017], [0034], claim 20), *Smith* otherwise only discloses stacked gate structures having a **GaN cap layer** with a non-recessed **gate**

electrode (*id.*, [0033]-[0037], [0039]-[0043], claim 1, Figs. 3, 4A-4C, 5A-5B). Just like *Saxler*, *Smith*'s GaN HEMT also includes a **GaN channel layer** and **AlGaN barrier layer** (inducing a **2DEG region**), and **source** and **drain electrodes**. *Smith*, [0030]-[0037], [0041]. A POSITA would thus have understood non-recessed electrodes were a suitable option for *Saxler*'s GaN, which bears substantially the same layers and structure.

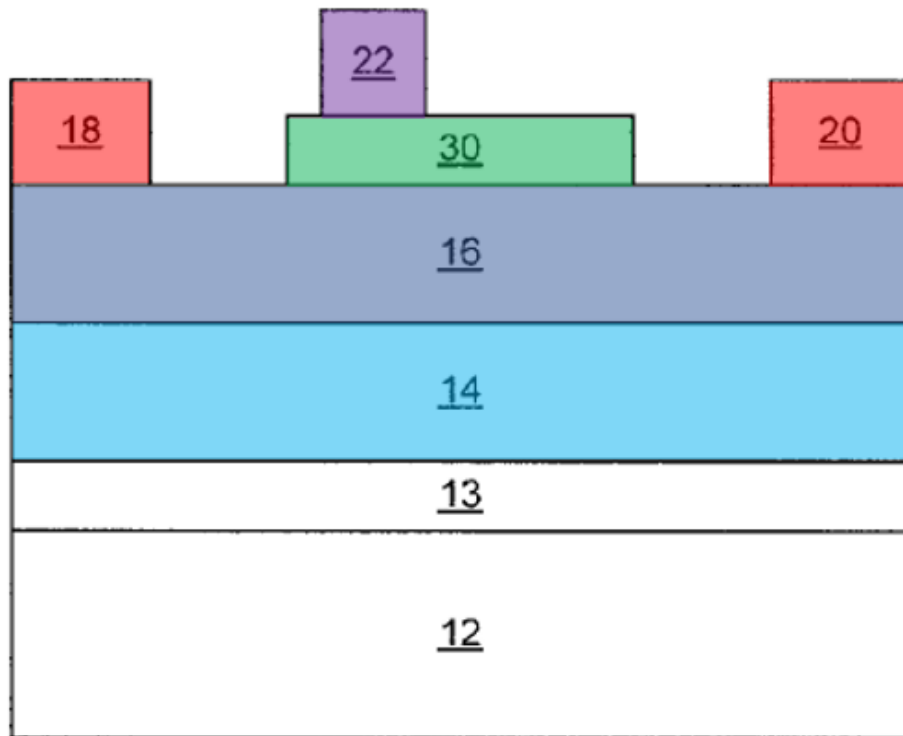


Figure 5B

Smith, Fig. 5B.

[149] In view of the many interchangeable options for stacked gate structures in GaN HEMT, a POSITA would have found the combination of *Yoshida*'s non-recessed gate arrangement in *Saxler*'s gate arrangement a simple substitution of known elements to predictably yield an enhancement mode GaN HEMT device.

b. Saxler-Yoshida, Beach, and Shenoy

[150] In my opinion, a POSITA would have found it obvious to use the methods of *Beach* and *Shenoy* to fabricate the *Saxler-Yoshida* gate structure for the same reasons I explained with respect to using *Beach* and *Shenoy* to make the non-recessed *Saxler* structure. §X.A.5 (Ground 1, Motivation to Combine). As I noted, the *Saxler-Yoshida* gate structure is the same as the non-recessed *Saxler* structure. §XI.A.2 (Ground 2, Combination). The combination of *Saxler-Yoshida* with *Beach* and *Shenoy* would have been obvious to predictably improve gate alignment and symmetry while reducing manufacturing steps and costs. §X.A.5 (Ground 1, Motivation to Combine).

B. Independent Claim 1

1. **[1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:**

[151] *Saxler* discloses Limitation [1p], as I explained above. §X.B.1 (Ground 1, Limitation [1p]).

2. [1a]: forming a GaN layer;

[152] *Saxler* discloses Limitation [1a], as I explained above. §X.B.2
(Ground 1, Limitation [1a]).

3. [1b]: forming a barrier layer on the GaN layer;

[153] *Saxler* discloses Limitation [1b], as I explained above. §X.B.3
(Ground 1, Limitation [1b]).

4. [1c]: depositing source and drain contacts on the barrier layer;

[154] *Saxler* discloses Limitation [1c], as I explained above. §X.B.4
(Ground 1, Limitation [1c]).

5. [1d]: depositing a p-type gate material on the barrier layer,

[155] *Saxler* discloses Limitation [1d], as I explained above. §X.B.5
(Ground 1, Limitation [1d]).

6. [1e]: depositing a gate metal on the p-type gate material;

[156] *Saxler* discloses Limitation [1e], as I explained above. §X.B.6
(Ground 1, Limitation [1e]).

7. [1f]: forming a photoresist over the gate metal;

[157] *Saxler, Beach* and *Shenoy* renders obvious Limitation [1f], as I
explained above. §X.B.7 (Ground 1, Limitation [1f]).

[158] In my opinion, *Saxler-Yoshida*, *Beach* and *Shenoy* likewise renders obvious [1f]. As I have noted, the *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §XI.A.2 (Ground 2, Combination). In my opinion, it would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy*, disclosing Limitation [1f] for the same reasons I explained for *Saxler*, *Beach*, and *Shenoy*. §§XI.A.3 (Ground 2, Motivation to Combine), X.B.7 (Ground 1, Limitation [1f]).

8. [1g]: etching the gate metal and the p-type gate material,

[159] *Saxler*, *Beach* and *Shenoy* renders obvious Limitation [1g], as I explained above. §X.B.8 (Ground 1, Limitation [1g]).

[160] In my opinion, *Saxler-Yoshida*, *Beach* and *Shenoy* also renders obvious Limitation [1g]. As I have noted, the *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §XI.A.2 (Ground 2, Combination). In my opinion, it would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy*, disclosing Limitation [1g] for the same reasons I explained as for *Saxler*, *Beach*, and *Shenoy*. §§XI.A.3 (Ground 2, Motivation to Combine), X.B.8 (Ground 1, Limitation [1g]). This satisfies both parties' construction. §IX.B (Claim Construction).

9. **[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and**

[161] *Saxler* and *Beach* renders obvious Limitation [1h], as I have explained. §X.B.9 (Ground 1, Limitation [1h]).

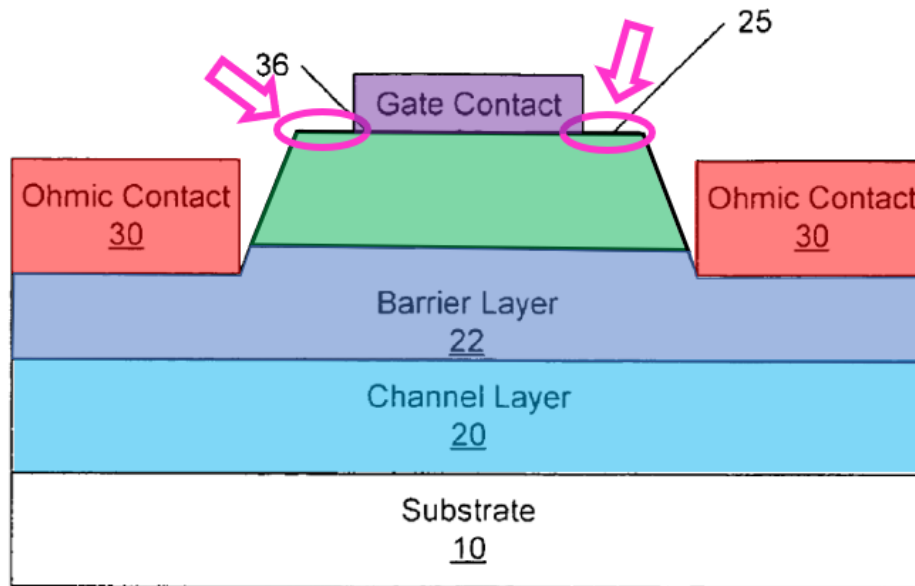
[162] In my opinion, *Saxler-Yoshida* also renders obvious this limitation. As I have noted, the *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §XI.A.2 (Ground 2, Combination). In my opinion, it would have been obvious to combine *Saxler-Yoshida*, disclosing Limitation [1g] for the same reasons I explained as for *Saxler*, *Beach*, and *Shenoy*. §§XI.A.3 (Ground 2, Motivation), X.B.9.

10. **[1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.**

[163] *Saxler*, *Beach* and *Shenoy* renders obvious Limitation [1i], as I explained above. §X.B.10 (Ground 1, Limitation [1i]).

[164] In my opinion, *Saxler-Yoshida*, *Beach* and *Shenoy* also renders obvious this limitation. As I have noted, the *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §XI.A.2 (Ground 2, Combination). In my opinion, it would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy*, disclosing Limitation [1i] for the

same reasons I explained as for *Saxler*, *Beach*, and *Shenoy*. §§XI.A.3 (Ground 2, Motivation), X.B.10 (Ground 1, Limitation [1i]). This satisfies both parties' construction. §IX.C (Claim Construction).



Saxler, Fig. 1A (modified).

- C. **[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.**

[165] As I explained, claim 2 does not further limit claim 1 because its requirements are included in Limitation [1i]. §X.C (Ground 2, Claim 2). Thus, *Saxler-Yoshida*, *Beach* and *Shenoy* render obvious claim 2 for the same reasons I explained for Limitation [1i]. §XI.B.10 (Ground 2, Limitation [1i]).

D. [Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.

[166] *Saxler, Beach* and *Shenoy* renders obvious claim 3, as I explained above. §X.D (Ground 1, Claim 3).

[167] In my opinion, *Saxler-Yoshida, Beach* and *Shenoy* also renders obvious this limitation. As I have noted, the *Saxler-Yoshida* combination discloses the same stacked, stepped gate structure as the non-recessed *Saxler* embodiments. §XI.A.2 (Ground 2, Combination). In my opinion, it would have been obvious to combine *Saxler-Yoshida* with *Beach* and *Shenoy*, disclosing claim 3 for the same reasons I explained as for *Saxler, Beach*, and *Shenoy*. §§XI.A.3 (Ground 2, Motivation), X.D (Ground 1, Claim 3).

XII. Ground 3: *Saxler* in view of *Ahn*

A. Overview of Ground 3

[168] To the extent *Saxler* alone does not explicitly disclose masking and etching the gate contact or self-aligned etching, it is my opinion that *Ahn* renders this method obvious.

1. Ahn

[169] *Ahn* uses a single mask and employs steps to isotropically and anisotropically etch to create stacked gate structures having stepped features and sloped sidewalls, as I have shown below in annotated figures. *Ahn*, Abstract, 3:41-

58, 6:15-26, 7:7-14, Fig. 4A-4C. In particular, Ahn's **top layer gate metal** and **underlying layer** are etched using a single **photomask** and results in sloped sidewalls and a pair of horizontal **ledges** on either side of the **top gate metal**. *Id.* Ahn explain that it etches **top layer gate metal** and **underlying layer** to different thicknesses W_1 and W_2 to create those ledges, and Ahn notes many times that this structure improves performance and prevents deterioration. Ahn, 4:39-59, 5:21-27, 5:63-6:26, 7:24-31. The layers of Ahn's gate structure are symmetric, and Ahn state that their side surfaces preferably have an "inclined shape." Ahn, 6:12-37, Fig. 4C.

FIG. 4A

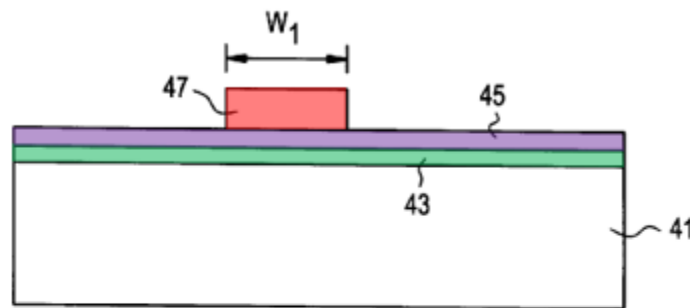
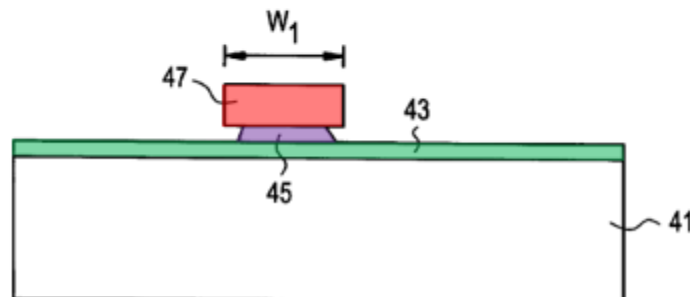
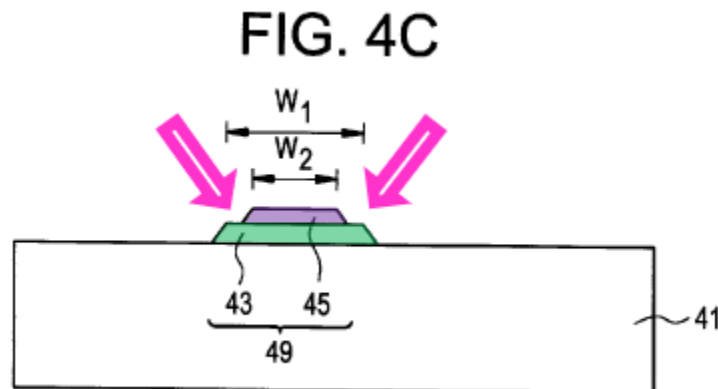


FIG. 4B



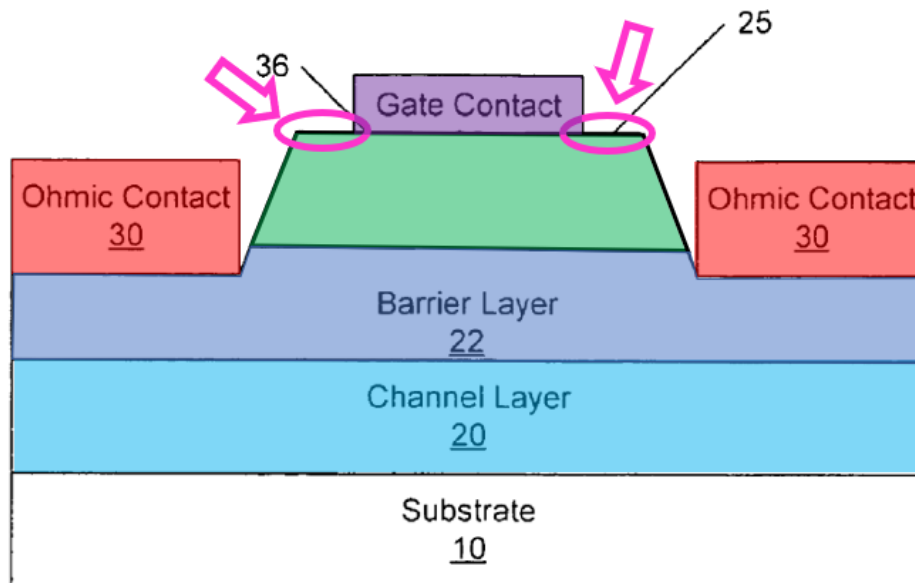


Ahn, Figs. 4A-4C.

[170] *Ahn* teaches that a **single mask** can be used to obtain this same structure in a variety of ways, and in my experience a POSITA at the time of the '347 patent would have been familiar with *Ahn*'s techniques. *Ahn*'s methods include: (i) using a single mask, perform an anisotropic dry etch to obtain sloped sidewalls then etch the gate metal isotropically (*Ahn*, 7:7-14); (ii) using a single mask, etch both layers simultaneously with a solution that etches the top layer more quickly (*Ahn*, 7:15-30); and (iii) using a single mask, dry etch the first layer and wet etch the second layer (*Ahn*, 7:31-46). Although *Ahn* is directed to semiconductor transistors in liquid crystal displays, the transistor gate structure is analogous to those in GaN HEMT devices and in my opinion a POSITA would have readily understood the *Ahn*'s approach to masking etching to form the gate structure, which was typical at the time of the '347 patent, would have been used to make gate structures in GaN HEMT transistors.

2. Combination of *Saxler* and *Ahn*

[171] As I show below, the combination of *Saxler* and *Ahn* would have straightforwardly yielded the same structure as the non-recessed *Saxler* embodiment:



Saxler, Fig. 1A (modified).

3. Motivation to Combine

[172] In my opinion, a POSITA would have found it obvious to use *Ahn*'s techniques to form a transistor gate to make *Saxler*'s non-recessed, stacked gate structure consisting of a cap layer and gate contact.

[173] This would have been an efficient combination. For example, *Saxler* produces its stacked gate structure by (i) masking and etching the cap layer, (ii) removing the mask, then (iii) depositing the gate contact. *Saxler*, [0064]-[0066],

Figs. 1A-1B; §X.A.1 (Ground 1, *Saxler*). A POSITA would have understood a second mask would be used to deposit the gate metal, then removed, which was an approach disclosed in many GaN transistors at the time because *Saxler* uses this approach for its recessed embodiments as does *Smith* in its non “self-aligned” embodiments. §§VIII (Technology Background, X.B.8 (Ground 1, Limitation [1g]), X.A.5, X.B.10 (Ground 1, Limitation [1i]); *Smith*, [0041], Figs. 4A-4C; *Saxler*, [0065]-[0066]). For example, *Smith* (incorporated by reference into *Saxler*) uses “conventional photolithographic techniques and mask alignment tools” to precisely place the gate contact. *Smith*, [0041]. In my opinion, a POSITA would have been motivated to simplify *Saxler*’s process and reduce costs by using fewer masking steps.

[174] A POSITA would have been familiar with many ways to create *Saxler*’s stepped gate structure in its non-recessed embodiments and would have used these methods interchangeably, as I explained above. §VIII (Technology Background). The ’347 patent was allowed without disclosing any particular method to etch the gate metal and obtain the claimed ledges because such methods were well within the skill level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§VIII (Technology Background), VI.B (Prosecution History). Appropriate methods such as lift-off when removing the photomask or isotropic etching were

well within the level of ordinary skill. §VIII (Technology Background). In my opinion, a POSITA would have found it obvious to modify *Saxler* by using *Ahn*'s approach for making a stepped gate in a thin-film transistor to improve alignment in *Saxler*'s structure. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C.

[175] *Ahn* provides a flexible approach, recognizing the interchangeability of methods of making the gate structure—it teaches many ways that would be used to obtain the non-recessed *Saxler* gate structure, including etching both layers simultaneously, or etching the layers sequentially using combinations of conventional wet and dry etching techniques. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C. For example, *Ahn* exploits differences between rates of dissolution of its layers to make the top gate layer narrower than the bottom. *Ahn*, 7:7-14-46. In my experience, a POSITA would have understood that *Saxler*'s cap layer, which was a p-type doped semiconductor, would have had a slower rate of dissolution than its metallic gate contact and found it obvious to use *Ahn*'s approach to arrive at the stepped gate structure of *Saxler*'s non-recessed embodiments. As shown in its figures, *Ahn*'s methods result in symmetrically aligned layers. *Ahn*, 6:15-37, Fig. 4C. *Ahn* also explicitly teaches that its single-mask approach is “preferred,” and that it leads to symmetrically aligned layers with

ledges of “substantially the same width” for “best results.” *Ahn*, 4:52-49, 5:55-62, 6:27-37, 7:15-46.

[176] In my opinion, a POSITA would have found the *Saxler-Ahn* combination a simple substitution of *Ahn*’s known methods that would be predictably implemented in *Saxler*’s flexible method of manufacturing to improve alignment and symmetry between layers while reducing manufacturing steps and costs.

B. Independent Claim 1

1. **[1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:**

[177] *Saxler* discloses Limitation [1p], as I explained above. §X.B.1
(Ground 1, Limitation [1p]).

2. **[1a]: forming a GaN layer;**

[178] *Saxler* discloses Limitation [1a], as I explained above. §X.B.2
(Ground 1, Limitation [1a]).

3. **[1b]: forming a barrier layer on the GaN layer;**

[179] *Saxler* discloses Limitation [1b], as I explained above. §X.B.3
(Ground 1, Limitation [1b]).

4. [1c]: depositing source and drain contacts on the barrier layer;

[180] *Saxler* discloses Limitation [1c], as I explained above. §X.B.4

(Ground 1, Limitation [1c]).

5. [1d]: depositing a p-type gate material on the barrier layer,

[181] *Saxler* discloses Limitation [1d], as I explained above. §X.B.5

(Ground 1, Limitation [1d]).

6. [1e]: depositing a gate metal on the p-type gate material;

[182] *Saxler* discloses Limitation [1e], as I explained above. §X.B.6

(Ground 1, Limitation [1e]).

7. [1f]: forming a photoresist over the gate metal;

[183] *Saxler* and *Ahn* renders obvious Limitation [1f], as I explained above.

Ahn forms “**photoresist 47**” over the **top gate metal** layer before etching, and it would have been obvious to implement this approach to make *Saxler*’s gate structure for reasons I previously explained. *Ahn*, 5:55-6:36, 7:7-46; §XII.A.3 (Ground 3, Motivation to Combine).

FIG. 4A

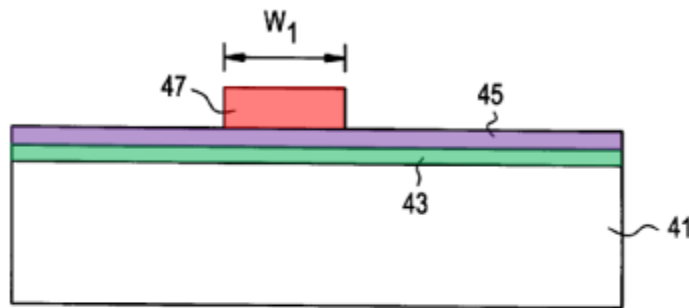
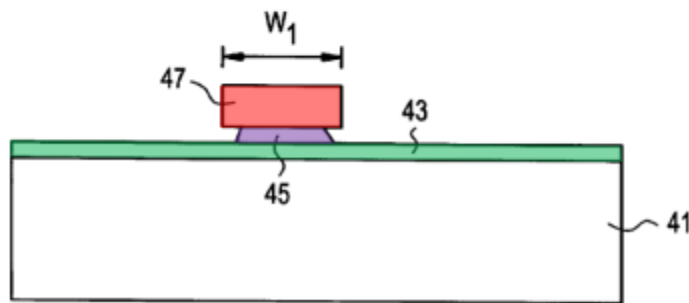


FIG. 4B



Ahn, Figs. 4A-4B.

8. [1g]: etching the gate metal and the p-type gate material,

[184] In my opinion, *Saxler* and *Ahn* renders obvious Limitation [1g]. As I explained previously, *Ahn* etches both layers of its gate structure. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C. And *Ahn* provides several interchangeable ways to do so, including (i) using a single mask, perform an anisotropic dry etch to obtain sloped sidewalls then etch the gate metal isotropically (*Ahn*, 7:7-14); (ii) using a single mask, etch both layers simultaneously with a solution that etches the top layer

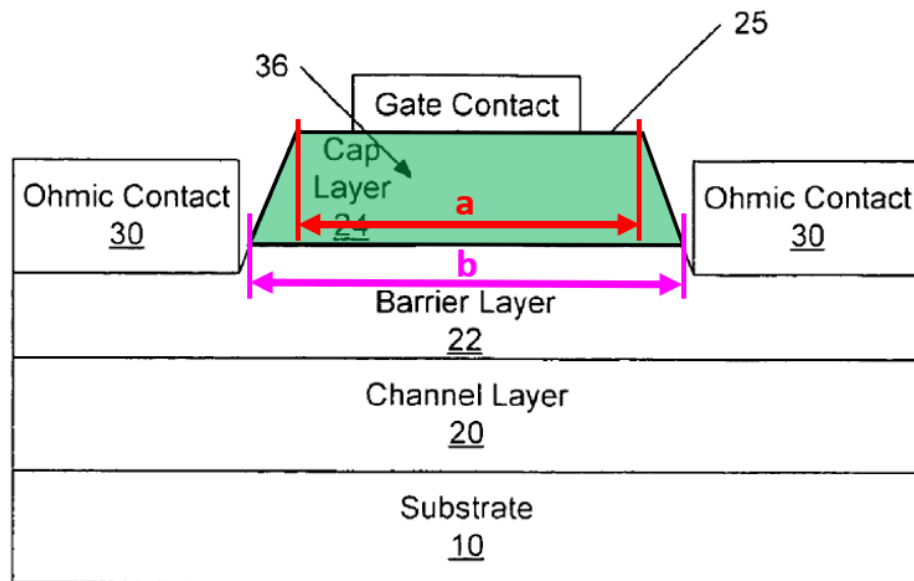
more quickly (*Ahn*, 7:15-30); and (iii) using a single mask, dry etch the first layer and wet etch the second layer (*Ahn*, 7:31-46). Further, *Ahn* teaches that its single-mask approach is “preferred,” and that this approach leads to symmetrically aligned layers with ledges of “substantially the same width” for “best results.” *Ahn*, 4:52-49, 5:55-62, 6:27-37, 7:15-46.

[185] In my opinion, it would have been obvious to make *Saxler*’s gate structure with *Ahn*’s approach of using a single a photomask over the gate metal and etching both *Saxler*’s gate metal and its cap layer for reasons I previously explained. §XII.A.3 (Ground 3, Motivation to Combine). This satisfies both parties’ construction. §IX.B (Claim Construction).

9. **[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and**

[186] In my opinion, *Saxler* and *Ahn* render obvious Limitation [1h]. In the combination, *Saxler*’s **cap layer** would be etched using conventional techniques to obtain its sloped sidewalls extending towards **source** and **drain contacts** and contacting the **barrier layer**. *Saxler* and *Sheppard*, incorporated by reference to disclose methods of forming gate structures (*Saxler* [0046] (referencing Ser. No. 10/897,726), [0068] (same))), each describe using several conventional techniques to etch the cap layer and generate the slope sidewalls shown in their

figures. *Saxler*, [0064], Figs. 1A-1B; *Sheppard*, [0044], Figs. 1B-1C. Further, the layers of *Ahn*'s gate structure also have sloped sidewalls just as *Saxler*'s **cap layer** sidewalls are sloped. *Ahn*, Fig. 4C. In my opinion, it would have been obvious to combine *Saxler*'s techniques with *Ahn*'s single mask processes to differentially etch multiple metal layers to obtain the **cap layer**'s sloped sidewalls in a stacked structure. *Ahn*, 5:55-6:36, 7:7-46; §XII.A.3 (Ground 3, Motivation). In the combination, the bottom of the **cap layer** (length "**b**," below) is about 1.25 times wider than the top (length "**a**"), i.e. more than 10% wider, thus satisfying either parties' construction.



Saxler, Fig. 1A (modified).

10. [1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

[187] In my opinion, *Saxler* and *Ahn* renders obvious this limitation. As I previously explained, *Ahn* etches its **top layer gate metal** under a **photoresist** such that is narrower than the **underlying layer** to form a pair of **ledges** on either side of the **top gate metal**. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C. Although not depicted as separate steps in the figures, *Ahn* explains that, in some embodiments, it etches the top layer as a second step to narrow the top layer *after* first etching both layers of its gate structure. *Ahn*, 7:7-14. Further, *Ahn* teaches that its single-mask approach is “preferred,” and that it leads to symmetrically aligned layers with ledges of “substantially the same width” for “best results.” *Ahn*, 4:52-49, 5:55-62, 6:27-37, 7:15-46.

FIG. 4A

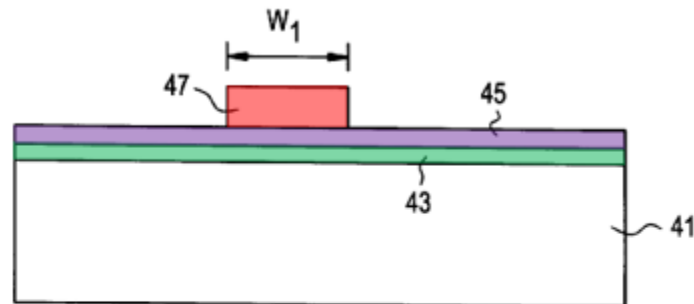


FIG. 4B

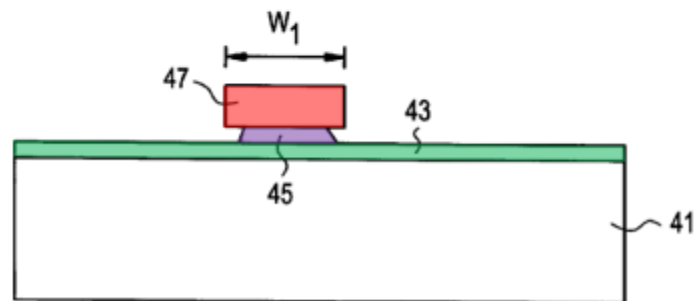
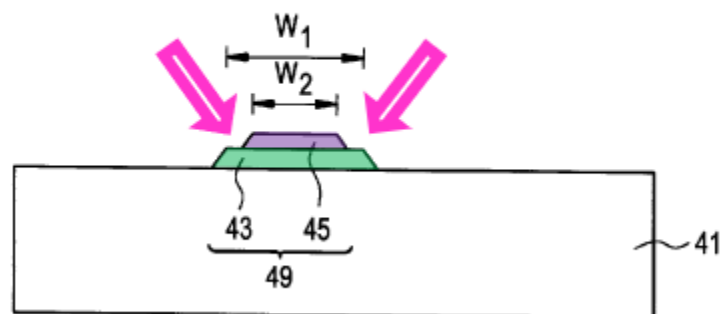


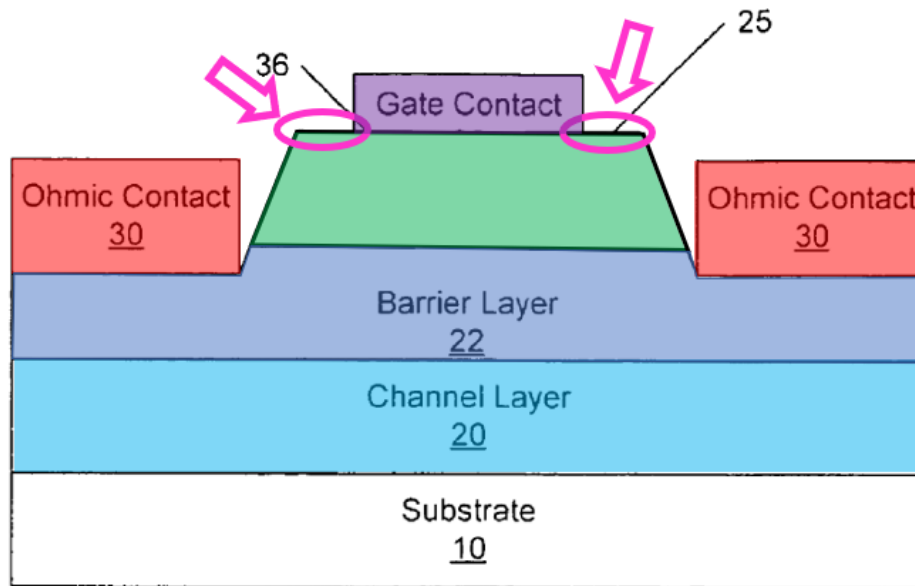
FIG. 4C



Ahn, Figs. 4A-4C.

[188] In my opinion, it would have been obvious to combine *Saxler*'s techniques with *Ahn*'s single mask processes to differentially etch multiple metal

layers to obtain a narrower gate contact and ledges on an underlying in a stacked structure. *Ahn*, 5:55-6:36, 7:7-46; §XII.A.3 (Ground 3, Motivation). This satisfies both parties' construction. §IX.C (Claim Construction).



Saxler, Fig. 1A (modified).

- C. **[Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.**

[189] As I explained, claim 2 does not further limit claim 1 because its requirements are included in Limitation [1i]. §X.C (Ground 1, Claim 2). Thus, *Saxler* and *Ahn* renders obvious claim 2 for the same reasons I explained for Limitation [1i]. §XII.B.10 (Ground 3, Limitation [1i]).

D. [Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.

[190] In my opinion, the combination of *Saxler* and *Ahn* renders obvious Claim 3.

[191] As I explained, *Ahn* uses a **single mask** to etch a gate having a **top metal layer** and **underlying layer** with horizontal **ledges**, which is a “self-aligned” process. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C. And *Ahn* describes several ways to etch two layers under a single photomask to create this stacked, stepped gate structure. *Ahn*, 7:7-46.

FIG. 4A

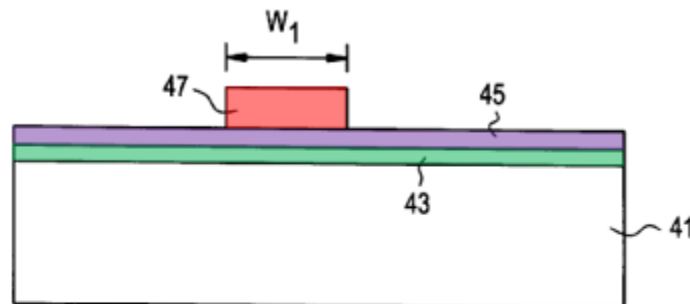
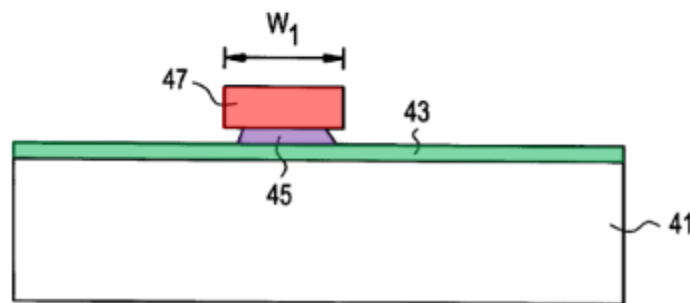
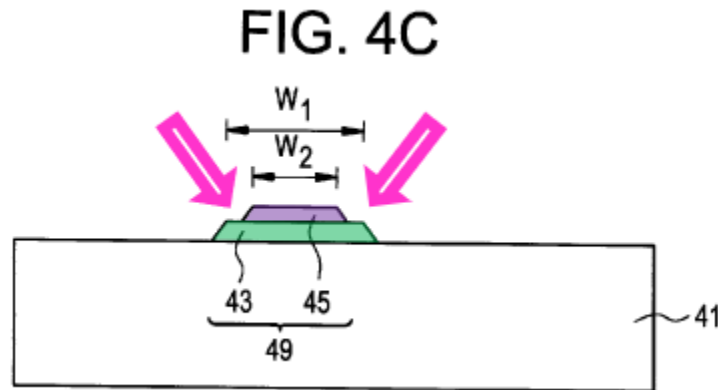


FIG. 4B





Ahn, Figs. 4A-4C.

[192] In my opinion, it would have been obvious and predictable to combine *Saxler*'s flexible manufacturing techniques with *Ahn*'s simple approach of using a single mask to make *Saxler*'s gate structure. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C; §XII.A.3 (Ground 3, Motivation to Combine).

XIII. Ground 4: *Yoshida* in view of *Saxler*, *Beach*, and *Shenoy* Renders Obvious Claims 1-2

A. Overview of Ground 4

[193] In my opinion, the combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious claims 1-3.

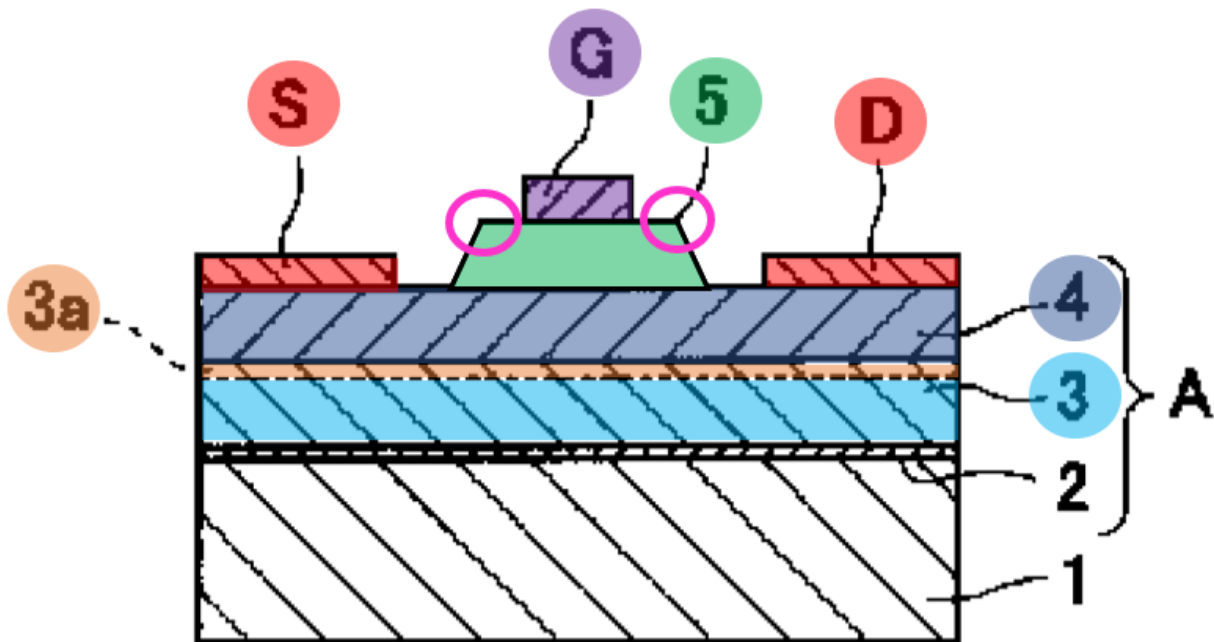
[194] As I explain above and below, *Yoshida* discloses the arrangement of semiconductor layers and structures produced by the method of claim 1, including the claimed ledges, but its figures show that its p-type gate material have vertical sidewalls. *Saxler* also disclose the structure made according to the method of

claim 1, including the ledges and sloped sidewalls on its cap layer (e.g., Ground 1). As I previously explained, the references are compatible, and their combination would have been a simple substitution to predictably make *Yoshida*'s same GaN HEMT device but with *Saxler*'s sloped sidewalls.

[195] Further, it is my opinion that a POSITA would have found it obvious to use *Beach* and *Shenoy*'s techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal—this approach would use a single mask to obtain self-aligned ledges, resulting in the same gate structure that *Yoshida-Saxler* discloses.

1. Ground 4: *Yoshida* in view of *Saxler*, *Beach*, and *Shenoy*

[196] Implementing *Saxler*'s **sloped sidewalls** in *Yoshida*'s **layer 5** results in the following combined structure. In the combination, the gate structure would have been made using *Beach* and *Shenoy*'s techniques.



Yoshida, Fig. 1 (modified).

2. Ground 4: Motivation to Combine

a. Yoshida-Saxler

[197] In my opinion, it would have been obvious to modify *Yoshida*'s transistor with the sloped sidewalls of *Saxler*'s capping layer to reduce gate leakage. The combination calls for nothing more than the simple substitution of *Saxler*'s sidewalls to predictably make an enhancement mode GaN HEMT. And a POSITA would have recognized *Saxler*'s sidewalls would have reliably reduced *Yoshida*'s gate leakage, making the combination obvious.

[198] The references are compatible for reasons I explained in Ground 2. §XI.A.3 (Ground 2, Motivation to Combine). In view of these many similarities, a

POSITA would have found it obvious to incorporate *Saxler*'s known sloped **cap layer** sidewalls into *Yoshida* p-type **layer 5**. Sloped sidewalls were conventional, as the '347 patent admits. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A. The '347 patent provides "conventional schematic[s] [of an] enhancement mode GaN transistor" depicting just such sloped sidewalls. Ex. 1001, 1:17-2:21, Figs. 1-4, 7A. The angle of *Saxler*'s sloped sidewall is typical for known mesa structures. *See, e.g., Xu* (Figs. 1-3); *Kanda* (Fig. 1); *Widman* (Fig. 4). It would have been a simple substitution of *Yoshida*'s vertical sidewalls with *Saxler*'s sloped sidewalls to predictably yield an enhancement mode GaN HEMT.

[199] In my opinion, a POSITA would have readily understood how to implement the combination. *Saxler* discloses conventional etching techniques for straightforwardly forming its sloped sidewalls. *Saxler*, [0064]. *Yoshida* also forms its p-type **layer 5** through etching. *Yoshida*, [0021]-[0023]. It would have been a simple substitution to employ *Saxler*'s etching approach to predictably shape *Yoshida*'s sidewalls.

[200] Accordingly, a POSITA would have recognized that *Saxler* provided a known option for shaping the sidewalls of *Yoshida*'s p-type **layer 5**, and the combination would have been obvious.

[201] It is my further opinion that a POSITA would have additionally recognized that *Saxler*'s sloped sidewalls would have beneficially reduced *Yoshida*'s leakage losses and found the combination obvious. It was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage. *Xu*, 1; *Kanda*, [0013], [0027], [0144], [0157], Fig. 12A. The '347 patent itself recognizes this basic fact, pointing out that capping structures in prior art enhancement-mode GaN transistors with sloped sidewalls had a known "gate leakage current path 201 [that] flows along the sidewall of the p-type gate material 101." Ex. 1001, 1:64-2:8, Fig. 2. A POSITA would have accordingly understood that the geometry of *Saxler*'s sloped sidewalls provided longer leakage paths than *Yoshida*'s vertical sidewalls, thereby lowering gate leakage. *E.g.*, *Xu*, 1; *Kanda*, [0013], [0027], [0144], [0157], Fig. 12A.

[202] In my opinion, a POSITA would also have found it obvious to form a photoresist over the gate metal to etch the gate metal and achieve the gate structure of the *Yoshida-Saxler* device. *Yoshida* and *Saxler* teach interchangeable methods of forming stacked, stepped gate structure, which were among numerous techniques a POSITA would have known. §VIII (Technology Background). *Yoshida* deposits its **gate electrode** in an opening etched into a SiO₂ mask but does not explicitly

disclose forming a photoresist on the gate and etching the gate metal. *Yoshida*, [0022]-[0023]). Yet as I explained for Ground 1, a POSITA would have found it obvious to form a single photoresist over the gate metal to etch the gate metal and the underlying layer in view of *Saxler*, which advantageously would have allowed greater precision and reliability when positioning the gate metal. §§X.A.1 (Ground 1, *Saxler*), X.B.7 (Ground 1, Limitation [1f]). And for the same reasons, it would have been obvious to use a photoresist over the gate metal in the combination of *Yoshida-Saxler*.

b. Yoshida-Saxler in view of Beach and Shenoy

[203] In my opinion, a POSITA would have found it obvious to make the stacked gate structure of the *Yoshida-Saxler*'s GaN HEMT device using the methods of *Beach* and *Shenoy* for the same reasons I explained for *Saxler* alone or the *Saxler-Yoshida* device. §§X.A.5 (Ground 1, Motivation to Combine), XI.A.3 (Ground 2, Motivation to Combine).

[204] The *Yoshida-Saxler* combination uses a sequence of steps to arrive at a stacked gate structure with p-type GaN layer and a gate electrode. *Yoshida*, [0021]-[0022]. Specifically, *Yoshida* discloses: (i) depositing a p-type GaN layer 5 onto AlGaIn layer 4 (*Yoshida*, [0021]); (ii) dry etching the "p-type layer except where the gate electrode was to be loaded" (*Yoshida*, [0022]); (iii) depositing an

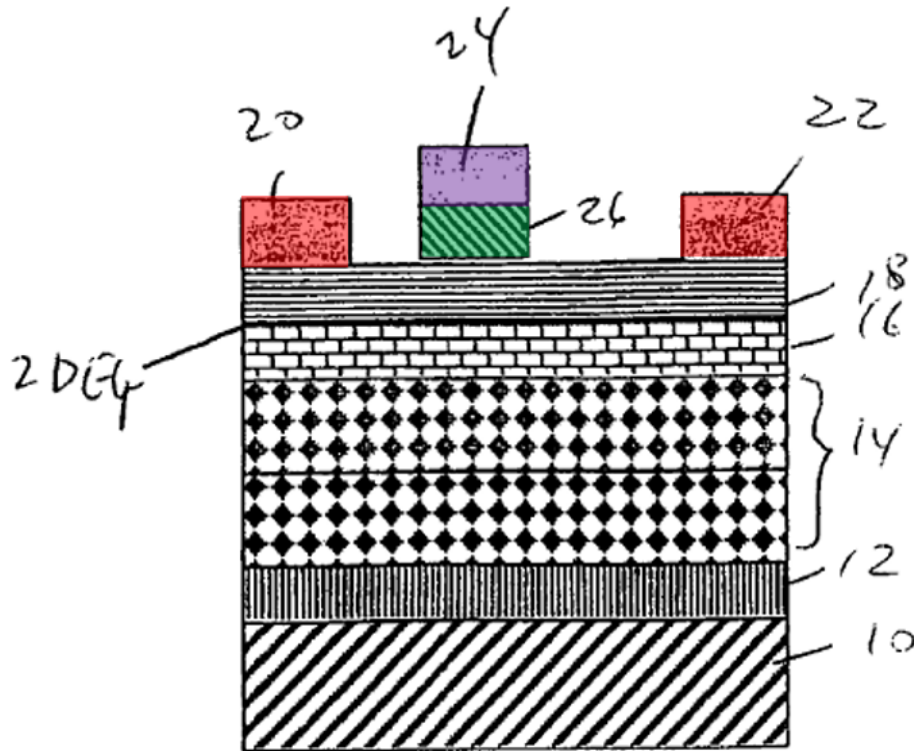
SiO₂ film over the entire surface (*id.*); (iv) patterning with a photoresist, and masking where the gate electrode was to be loaded (*id.*); (v) depositing source and drain electrodes (*id.*); (vi) “etching away the masking and opening the SiO₂ film (*Yoshida*, [0023]); (vii) masking the source and drain electrodes; and (viii) depositing Au to form the gate electrode (*id.*). That process thus requires at least two masks. In the *Yoshida-Saxler* combination, etching step (ii) would simply employ *Saxler*’s conventional etching techniques to create sloped sidewalls and would employ *Saxler*’s techniques to position the gate metal, which are similar to *Beach*’s techniques. *Saxler*, [0064]; §XIII.A.2.a (Ground 4, *Yoshida-Saxler*)).

[205] In my opinion, a POSITA would have been familiar with many ways to create *Yoshida-Saxler*’s stepped gate structure and would have used these methods interchangeably. §VIII (Technology Background). The ’347 patent was allowed without disclosing any particular method to obtain the claimed ledges because their manufacture was well within the skill level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§VI.B (Prosecution History), VIII (Technology Background). A POSITA would have found it obvious to modify *Yoshida-Saxler* by using *Beach*’s self-aligned technique and *Shenoy*’s isotropic etching to arrive at that same gate structure, which would have improved efficiency by eliminating masking and etching steps and would have ensured symmetry of the gate metal

with respect to the p-gate material. In my opinion, a POSITA would have understood *Beach*'s "self-aligned" techniques would have used a single photomask, as described in greater detail in another *Beach* publication. *Beach-II*, [0047]-[0048], Figs. 1D-1E. This approach was known—*Ahn* discloses this same approach for making a stepped gate in a thin-film transistor with symmetrically aligned layers. *Ahn*, Abstract, 3:41-58, 6:15-37, 7:7-14, Fig. 4C. And a POSITA would have found *Beach* and *Shenoy*'s methods obvious and predictable in light of *Smith*, incorporated into *Saxler* by reference to disclose methods of making gate structures (*Saxler*, [0087]), which also uses a "self-aligned" technique. *Smith*, [0041]-[0044], claim 25; §X.A.1 (Ground 1, *Saxler*).

[206] *Beach* teaches a method of making stacked gate structures in GaN HEMT devices that is more efficient and has fewer steps than *Saxler*'s multiple masking approach because *Beach* uses a single mask. *Beach*, [0040], [0045], [0054]. *Beach*'s gate structure includes the "gate arrangement 24," which comprises a gate electrode, and an underlying "gate barrier 26," a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F. *Beach*'s process (i) deposits "gate barrier 26" and "gate arrangement 24" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits power electrodes. *Beach*, [0040]. In my experience, such self-aligned techniques were

common in the field as of relevant date (e.g., *Beach*, *Beach-II*, and *Smith* all describe such self-aligned techniques).



Beach, Fig. 1.

[207] In my opinion, a POSITA would have found it obvious to use *Beach*'s approach to create and symmetrically align *Yoshida-Saxler* gate structure for improved performance. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3.

[208] *Beach* does not describe steps to create the **horizontal ledges** of *Yoshida-Saxler*'s stacked gate structure following its self-aligned process. But as I previously explained, *Shenoy*, which published over a decade before the '347 patent, describes long-used, simple isotropic etching techniques for

symmetrically undercutting metal layers below photoresist masks. *Shenoy*, 2-3; §X.A.3 (Ground 1, *Shenoy*).

[209] Thus, in my opinion, an ordinary artisan would have found it obvious to use *Beach*'s self-aligned method of making *Yoshida-Saxler*'s stacked gate structure in a GaN HEMT and to use *Shenoy*'s methods to undercut the **gate electrode** and create *Yoshida-Saxler*'s **horizontal ledges**. A POSITA would have found the combination a simple substitution of *Beach*'s and *Shenoy*'s known methods to predictably create *Yoshida-Saxler*'s stacked gate structure more efficiently and symmetrically.

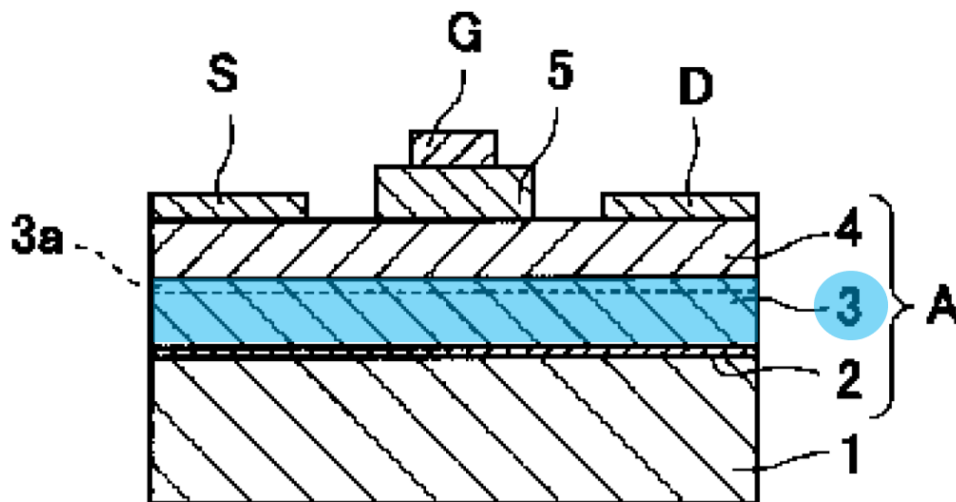
B. Independent Claim 1

1. [1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[210] *Yoshida* discloses Limitation [1p]. For example, *Yoshida* discloses manufacturing a GaN high-mobility transistor that includes a p-type GaN layer below the gate, which “enables voltage control with a small amount of carrier injection,” constituting a normally off enhancement mode GaN transistor. *Yoshida*, Abstract, [0015], [0017], Fig. 1. Although *Yoshida* does not use the phrase “enhancement mode,” such a transistor indeed constitutes a normally-off enhancement-mode GaN transistor.

2. [1a]: forming a GaN layer;

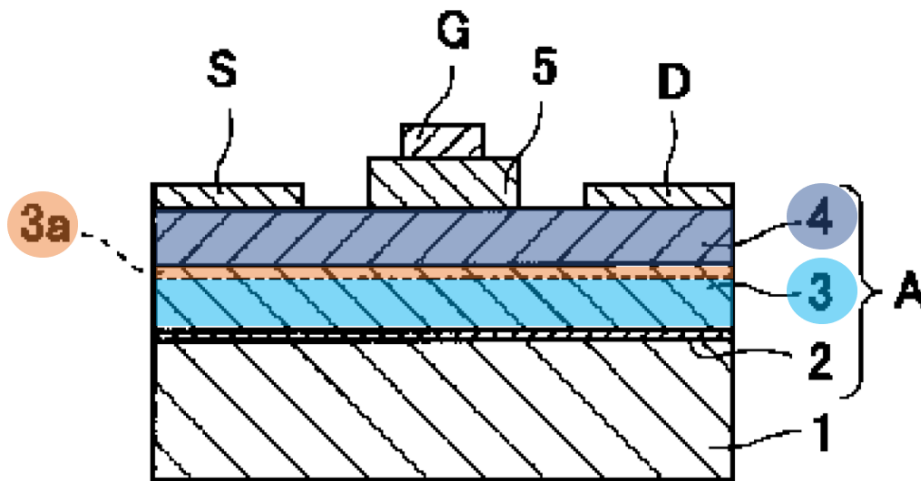
[211] Limitation [1a] was conventional (§X.B.2 (Ground 1, Limitation [1a])), and *Yoshida* discloses it. *Yoshida* forms “**layer 3**,” which is a GaN layer. *Yoshida*, Abstract, [0010]-[0012], [0019]-[0020]. *Yoshida* teaches that “i-type GaN is [a] particularly preferable” embodiment of “**layer 3**,” which is an intrinsic or undoped GaN. *Yoshida*, Abstract, [0012], Fig. 1.



Yoshida, Fig. 1.

3. [1b]: forming a barrier layer on the GaN layer;

[212] Limitation [1b] was conventional (§X.B.3 (Ground 1, Limitation [1b])), and *Yoshida* discloses it. *Yoshida*’s “**layer 4**” is a barrier layer formed on GaN “**layer 3**.” *Yoshida*, Abstract, [0010], [0013], [0019]-[0021], Fig. 1. A “**two-dimensional electron gas layer 3a** is formed at the heterojunction interface” of **layer 4** and **layer 3**, as was typical of such devices *Yoshida*, [0016].

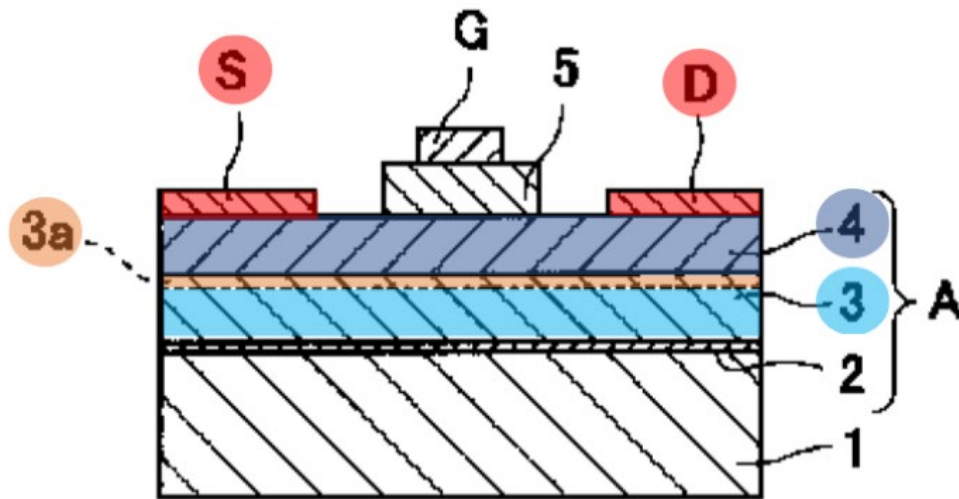


Yoshida, Fig. 1.

[213] More specifically, *Yoshida* identifies that “n-type AlGaN is [a] favorable” choice for **layer 4**. *Yoshida*, Abstract, [0010], [0013], Fig. 1. The ’347 patent likewise discloses that the claimed barrier layer may be an AlGaN layer, which is covered in dependent claims, and was a typical arrangement at the time. Ex. 1001, 1:37-58, 3:32-43, 4:8-16, claims 3, 6.

4. [1c]: depositing source and drain contacts on the barrier layer;

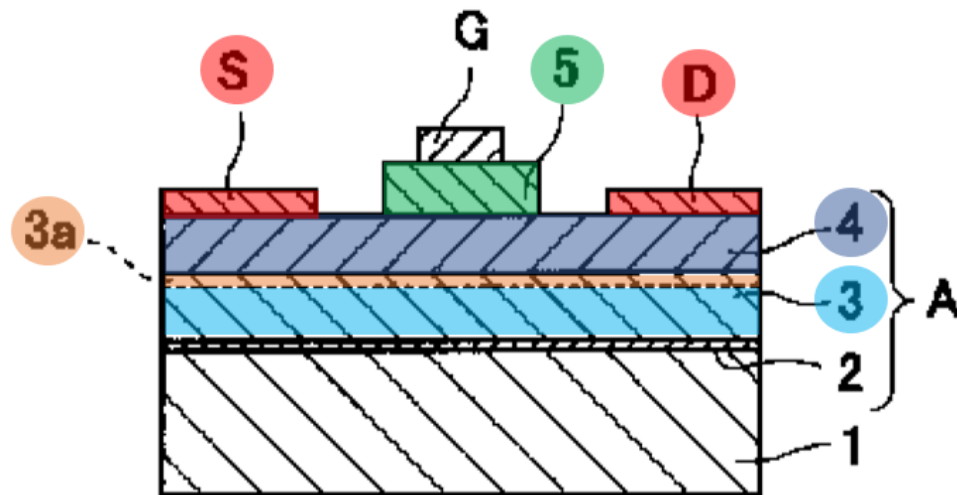
[214] Limitation [1c] was conventional (§X.B.4 (Ground 1, Limitation [1c])), and *Yoshida* discloses **source** and **drain electrodes** (contacts) that are “directly loaded” (deposited) on barrier **layer 4**, which was wholly conventional. *Yoshida*, Abstract, [0014], [0022], Figs. 1-2, 3A-3B.



Yoshida, Fig. 1.

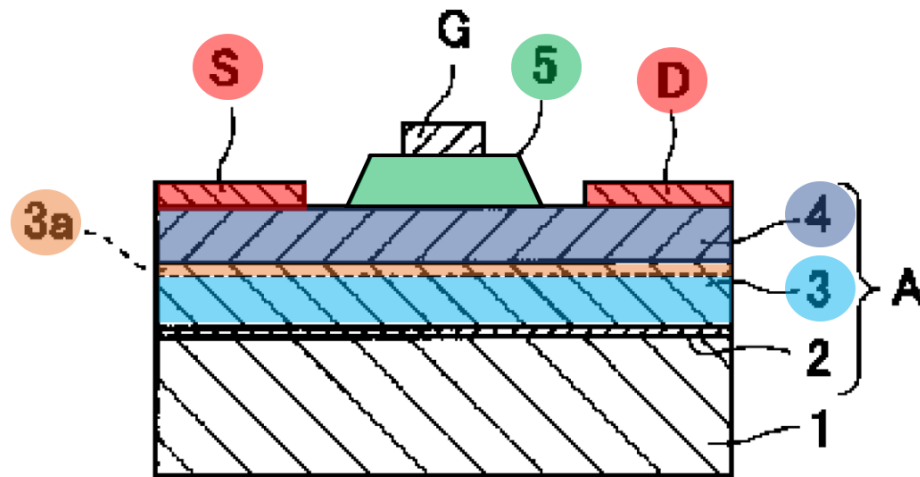
5. [1d]: depositing a p-type gate material on the barrier layer,

[215] Limitation [1d] was conventional (§X.B.5 (Ground 1, Limitation [1d])), and *Yoshida* discloses it. *Yoshida*'s **layer 5** is “a p-type gate material” that is deposited on the **barrier layer**. *Yoshida* explains that **layer 5** may be a single- or double-layer comprising a “p-type GaN.” *Yoshida*, Abstract, [0009], [0015], [0018], claim 2.



Yoshida, Fig. 1.

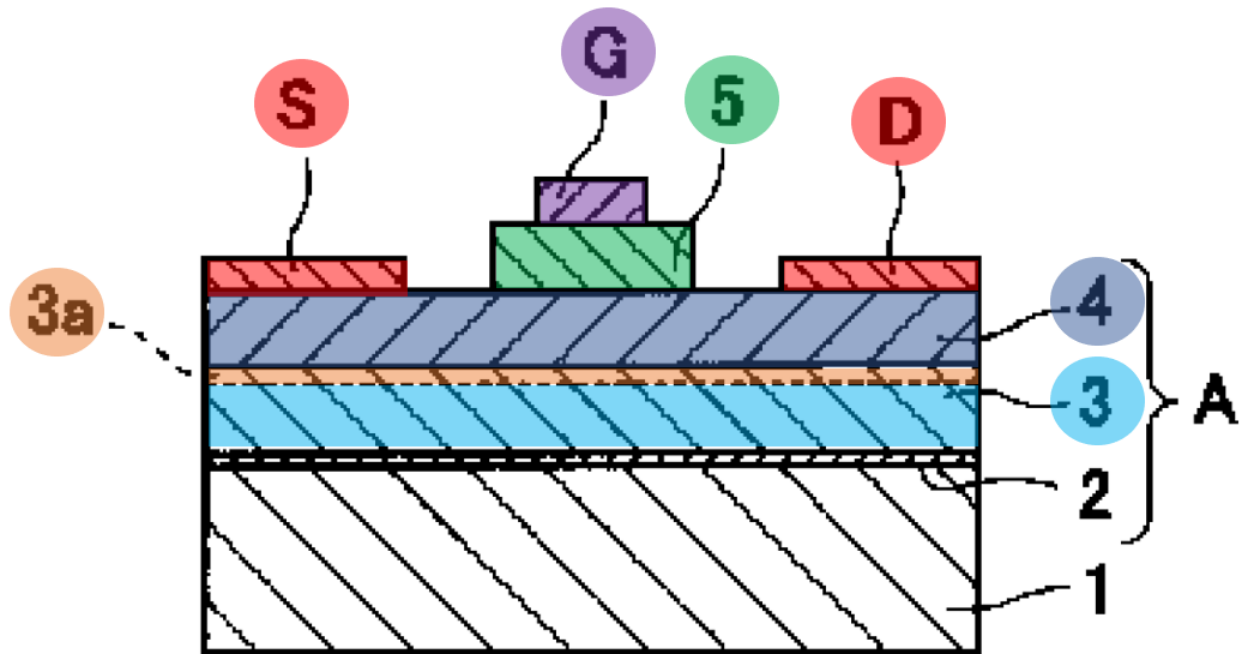
[216] In my opinion, *Yoshida-Saxler* also renders obvious this limitation. *Saxler* discloses depositing a **cap layer** on the **barrier layer**. *Saxler*, [0010], [0013], [0059]-[0063], [0069], [0071], [0073], Figs. 1A, 2B; §X.B.5 (Ground 1, Limitation [1d]). In my opinion, it would have been obvious to combine these references to deposit a **layer 5** with sloped sidewalls on the **barrier layer**. §XIII.A.2 (Ground 4, Motivation to Combine).



Yoshida, Fig. 1 (modified).

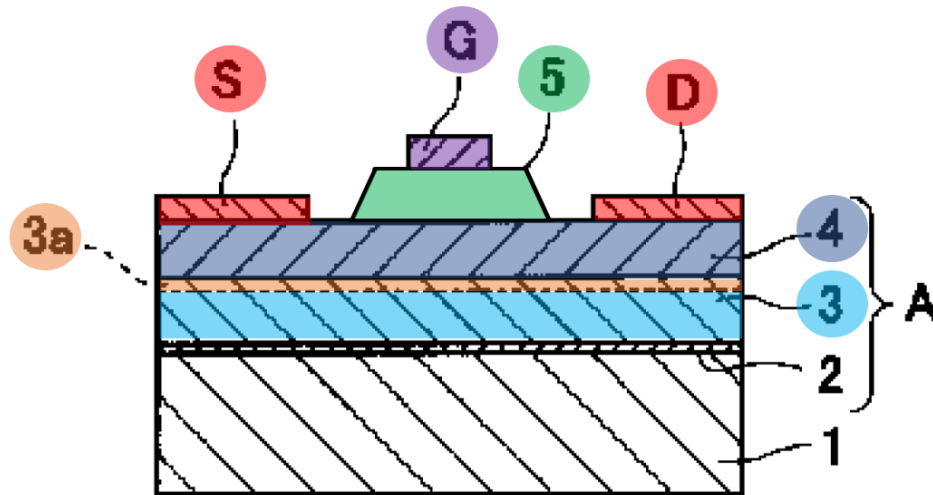
6. [1e]: depositing a gate metal on the p-type gate material;

[217] Limitation [1e] was conventional (§X.B.6 (Ground 1, Limitation [1e])), and *Yoshida* discloses it. *Yoshida*’s “**gate electrode**” is a metal (e.g., “Au/Pt, Al”) deposited on p-type **layer 5**. *Yoshida*, Abstract, [0006], [0009]-[0010], [0016], [0022]-[0023], claim 1, Fig. 1.



Yoshida, Fig. 1.

[218] In my opinion, *Yoshida-Saxler* also renders obvious this limitation. *Saxler*'s **gate contact** is a gate metal (e.g., "Ni, Pt, NiSix, Cu, Pd, Cr, W and/or WsiN") formed on its **cap layer** in non-recessed embodiments. *E.g.*, *Saxler*, Abstract, [0052], [0066], Figs. 1A, 2B; §X.B.6 (Ground 1, Limitation [1e]). It would have been obvious to combine these references to deposit a **gate electrode**, which is a metal (e.g., "Au/Pt, Al") deposited on a p-type **layer 5** with sloped sidewalls. §XIII.A.2 (Ground 4, Motivation to Combine).



Yoshida, Fig. 1 (Modified).

7. [1f]: forming a photoresist over the gate metal;

[219] Limitation [1f] was conventional (§X.B.7 (Ground 1, Limitation [1f])) and *Yoshida-Saxler* renders obvious it obvious. The references teach interchangeable methods to achieve their stacked, stepped gate structures that render obvious forming a photoresist over the gate metal. §§VIII (Technology Background); XIII.A.2. *Yoshida* deposits its **gate electrode** in an opening etched into a SiO₂ mask but does not explicitly disclose forming a photoresist on the gate and etching the gate metal. *Yoshida*, [0022]-[0023]). Yet as I explained for Ground 1, a POSITA would have found it obvious to mask and etch the gate metal in view of *Saxler* to precisely and reliably position the gate metal. §§X.A.1 (Ground 1, *Saxler*), X.B.7 (Ground 1, Limitation [1f]). And for the same reasons, it is my opinion that a POSITA would have found it obvious to form a photomask

over the gate metal in the *Yoshida-Saxler* combination. §XIII.A.2 (Ground 4, Motivation to Combine).

[220] Further, in my opinion, *Yoshida-Saxler* in view of *Beach* and *Shenoy* also renders obvious Limitation [1f]. *Beach* discloses forming a photoresist over the gate metal, specifying that “the stack is patterned and etched to obtain gate arrangement 24 over gate barrier 26.” *Beach*, [0040]. *Shenoy* likewise discloses a photoresist over a metal electrode. *Shenoy*, 1.

[221] In my opinion, it would have been obvious to make *Yoshida-Saxler*’s gate structure with *Beach*’s and *Shenoy*’s approach to using a single a photomask over the gate metal with isotropic etching for reasons I previously explained. §XIII.A.2 (Ground 4, Motivation to Combine).

8. [1g]: etching the gate metal and the p-type gate material,

[222] Limitation [1g] was conventional (§X.B.8 (Ground 1, Limitation [1g])), and *Yoshida-Saxler* renders it obvious. *Yoshida* explains it deposits then etches **layer 5**. *Yoshida*, [0021]-[0022]. And as I explained for Limitation [1f], in the *Yoshida-Saxler* combination it would have been obvious to subsequently mask and etch the gate metal to position the gate metal precisely and reliably. §XIII.B.7 (Ground 4, Limitation [1f]).

[223] *Yoshida-Saxler, Beach* and *Shenoy* also renders obvious Limitation [1g]. *Beach* discloses using a single mask when etching the gate metal and p-type gate material, specifying that both layers of “the stack [are] patterned and etched to obtain gate arrangement 24 over gate barrier 26.” *Beach*, [0040]. *Shenoy* describes the same. *Shenoy*, 1.

[224] In my opinion, as POSITA would have been familiar with many interchangeable manufacturing techniques and it would have been obvious and predictable to make *Yoshida-Saxler*’s gate structure with *Beach*’s and *Shenoy*’s approach to using a single a photomask over the gate metal with isotropic etching. §XIII.A.2 (Ground 4, Motivation to Combine). This satisfies both parties’ construction. §IX.B (Claim Construction).

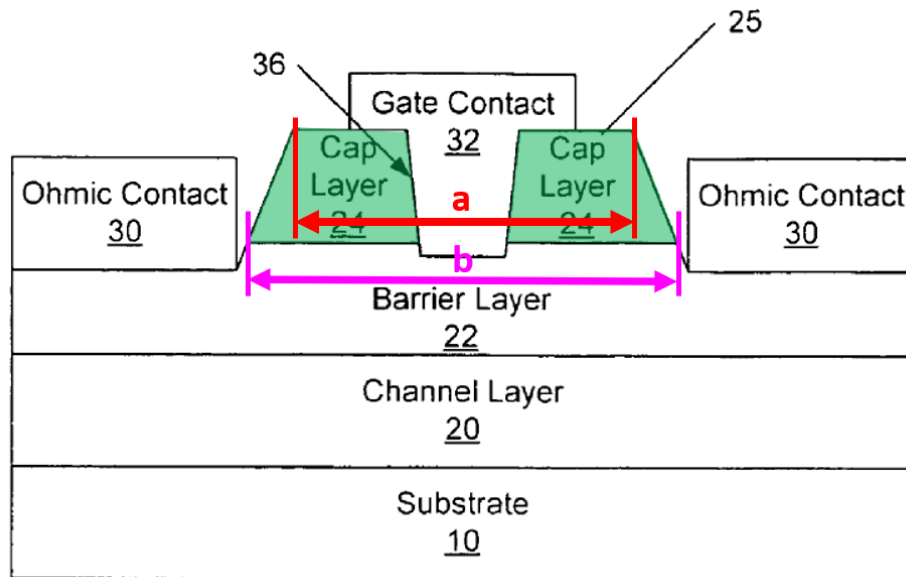
9. **[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and**

[225] Limitation [1h] was conventional (§X.B.9 (Ground 1, Limitation [1h])), and *Yoshida-Saxler* renders it obvious. Both *Yoshida*’s **layer 5** and *Saxler*’s **cap layer** are p-type gate materials that may be doped p-type in a subregion or throughout the layer. *Saxler*, [0013], [0069], [0071], [0073]. The **cap layer** resides above an AlGaN **barrier layer**, just like *Yoshida*’s **layer 5** and as claim 1 of the ’347 patent requires. *Saxler*, [0010], [0059]-[0063], Figs. 1A, 2B.

Saxler explains its **cap layer** may take several forms, including “p-type dopant,” which may be doped in a region of the cap layer or incorporated throughout.

Saxler, [0069].

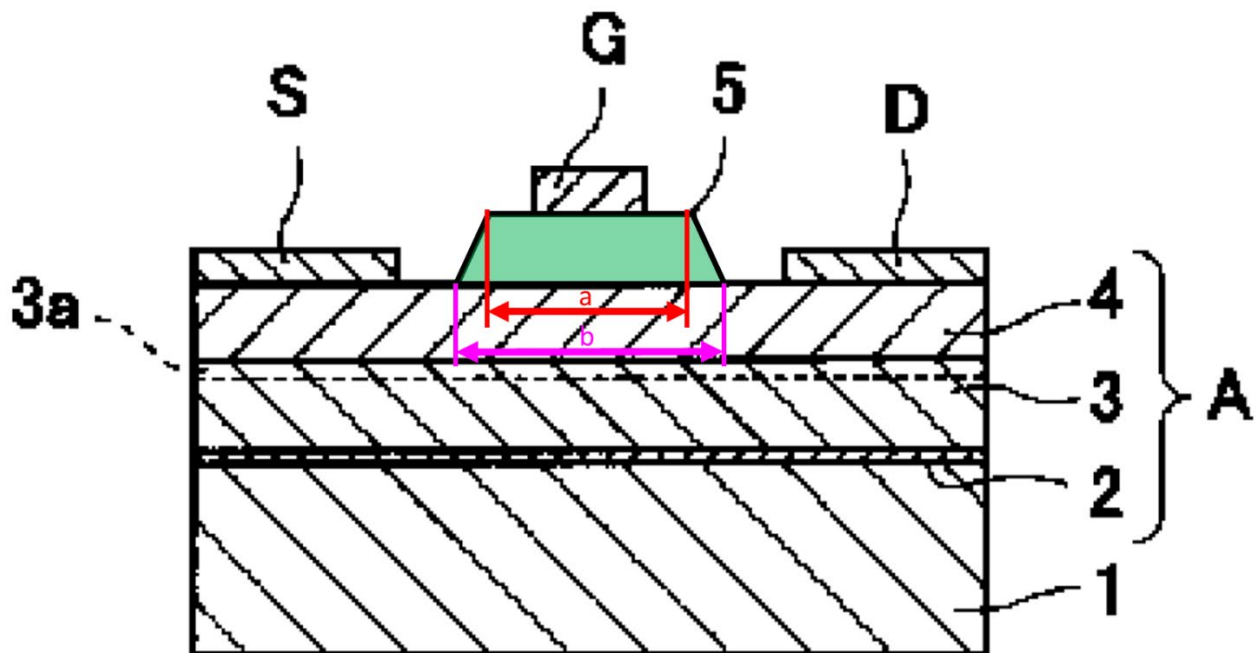
[226] Further, *Saxler*’s **cap layer** has side surfaces extending horizontally towards the **source** and **drain contact** under either parties’ construction. §X.B.9 (Ground 1, Limitation [1h]); *Saxler*, [0064], Figs. 1A, 2B.



Saxler, Fig. 1A.

[227] As I explained above, it would have been obvious to combine the sloped sidewalls of *Saxler*’s doped **cap layer** into *Yoshida*’s p-type **layer 5** such that they horizontally extended towards the **source** and **drain contacts** in the *Yoshida-Saxler* device, resulting in the sloped structure under either construction,

where the bottom of the **p-type gate material** (length “**b**,” below) is more than 10% wider than the top (length “**a**”). §XIII.A.2 (Ground 4, Motivation to Combine). Here, I measured these distances and found that **b** is approximately 1.24 times the length of **a**.

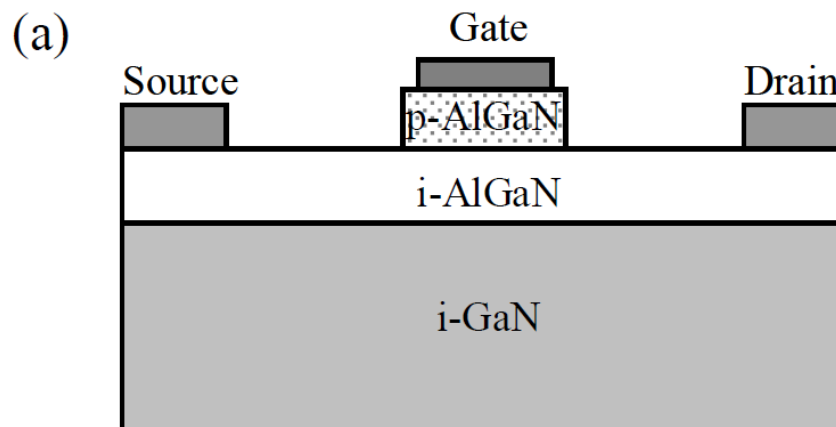


Yoshida, Fig. 1 (modified).

[228] In addition, it is my opinion that *Yoshida-Saxler* in view of *Beach* and *Shenoy* renders obvious Limitation [1h]. It would have been obvious to make *Yoshida-Saxler*'s gate structure with *Beach*'s approach to using a single a photomask over the gate metal. §XIII.A.2 (Ground 4, Motivation to Combine).

[229] Further, *Yoshida* alone renders obvious sloped sidewalls that extend horizontally towards source and drain contacts under Patent Owner's construction. Although *Yoshida* draws substantially vertical sidewalls of p-type **layer 5**, a POSITA would have known a sidewall drawn vertically would have a slight slope when built in a practical device.

[230] In my opinion, a POSITA would have been familiar with this principle. For example, *Saxler* states that, in practice, "an etched region illustrated as a rectangle will, typically, have *tapered*, rounded or curved features." *Saxler*, [0042]. As another example, a 2006 IEEE paper on a GaN HEMT with a similar gate structure to *Yoshida* depicts its p-AlGaN gate layer having vertical sidewalls in its drawings (Fig. 1) but shows sloped sidewalls extending horizontally towards source and drain contacts in a microscope image of a device built according to the drawings. *Uemoto*, Figs. 1-2, 5.



Uemoto, Fig. 1(a) (drawing).

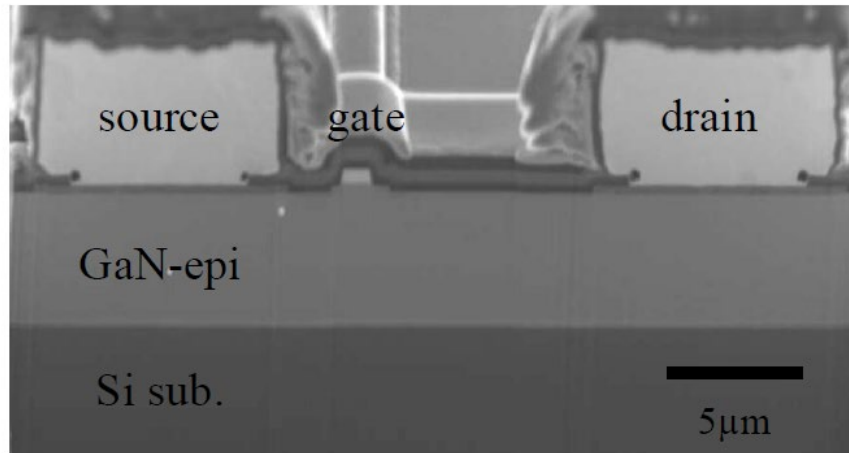
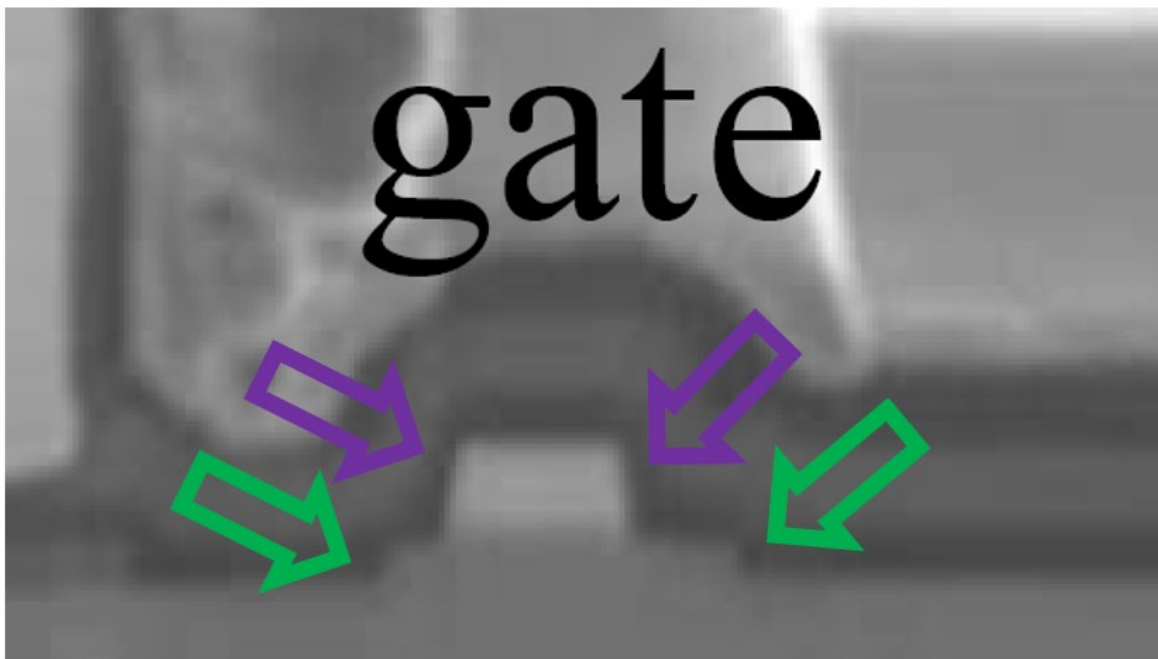


Fig.5 Cross sectional SEM image of GIT on a Si substrate.

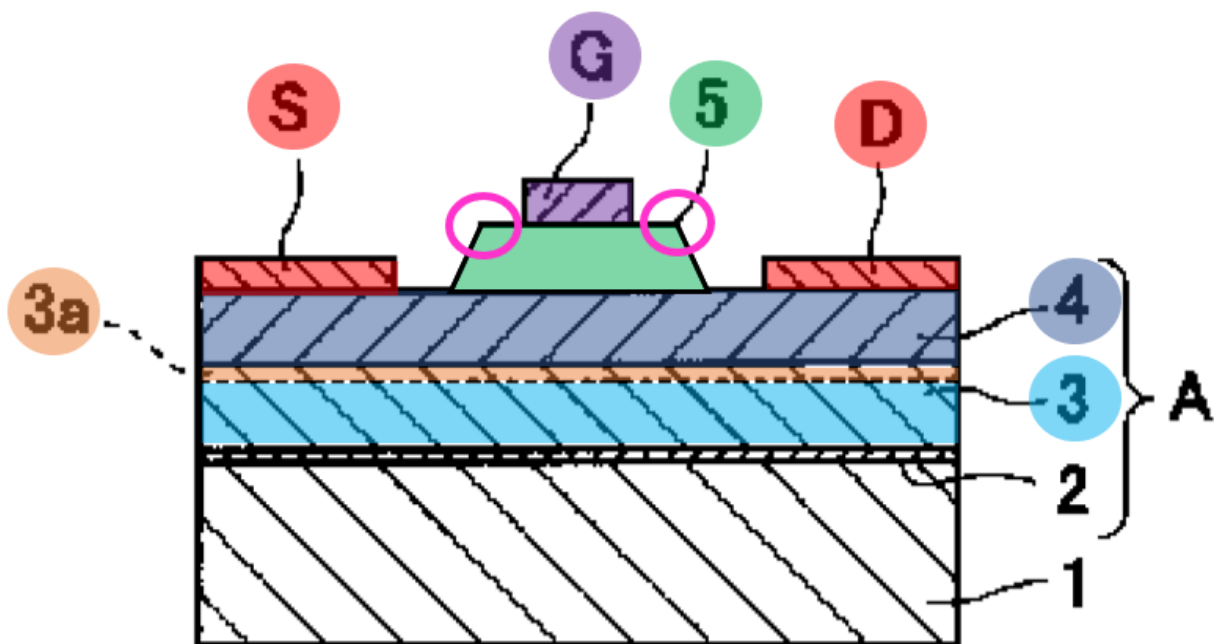
Uemoto, Fig. 5 (microscope image).



Uemoto, Fig. 5 (showing sloped sidewalls of the p-AlGaN layer and gate metal).

10. [1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

[231] Limitation [1i] was conventional (§X.B.10 (Ground 1, Limitation [1i])), and *Yoshida-Saxler* renders it obvious. As I explained, the combination yields the stacked, stepped gate structure having a pair of **ledges**, as shown below, and it would have been obvious over *Yoshida-Saxler* to form those ledges by masking and etching the gate metal using a single mask. §§XIII.A.1-XIII.A.2 (Ground 4, Combination and Motivation), XIII.B.7-XIII.B.9 (Ground 4, Limitation [1f]-[1h]).



Yoshida, Fig. 1(modified).

[232] In addition, *Yoshida-Saxler*, *Beach* and *Shenoy* renders obvious etching the gate metal to form the **ledges** of Limitation [1i]. As I have explained, POSITA would have been familiar with numerous common techniques to form the ledges of *Yoshida-Saxler* after etching the gate metal and cap layer using a single photomask, including lift-off, and would have found implementing *Beach*'s and *Shenoy*'s techniques obvious. *E.g.*, Ex. 1023; §VIII (Technology Background). As I explained, *Shenoy* discloses long-used, simple methods of isotropically etching the gate metal to form symmetric undercuts of a photomask. *Shenoy*, 1-2. This technique would have generated the pair of **ledges** on *Yoshida-Saxler*'s **layer 5**. In my opinion, it would thus have been obvious and predictable to combine *Yoshida-Saxler*'s techniques with *Beach*'s single mask process and *Shenoy*'s isotropic etching to arrive at the *Yoshida-Saxler* structure, as I previously explained. §XIII.A.2 (Ground 4, Motivation). This satisfies both parties' construction. §IX.C (Claim Construction).

C. [Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.

[233] As I explained, claim 2 does not further limit claim 1 because its requirements are included in Limitation [1i]. §X.C (Ground 1, Claim 2).

Accordingly, *Yoshida-Saxler*, *Beach*, and *Shenoy* renders obvious claim 2 for the

same reasons I explained for Limitation [1i]. §XIII.B.10 (Ground 4, Limitation [1i]).

D. [Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.

[234] In my opinion, the combination of *Yoshida-Saxler*, *Beach*, and *Shenoy* renders obvious Claim 3.

[235] *Beach* discloses a stacked “*self-aligned*” gate arrangement” using a single photo mask to etch both the “gate arrangement 24” (gate electrode) and the underlying “gate barrier 26” (GaN semiconductor), and this process is the same “self-aligned” process depicted in the ’347 patent at Figures 6A-6B. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Ex. 1001, 4:8-20; §§VI.1 (’347 Claims and Specification Overview), X.A.2 (Ground 1, *Beach*), X.A.5 (Ground 1, Motivation), XIII.A.2 (Ground 4, Motivation).

[236] As I have also explained, *Shenoy* etches a photomask to isotropically undercut the metal layer below the photomask, and this process is the same one shown in Figures 6B-6C of the ’347 patent. *Shenoy*, 2-3; Ex. 1001, 4:17-33; §§VI.1 (’347 Claims and Specification Overview), X.A.3 (Ground 1, *Shenoy*), X.A.5 (Ground 1, Motivation), XIII.A.2(Ground 4, Motivation).

[237] In my opinion, it would have been obvious to use *Beach*’s self-alignment method and *Shenoy*’s undercutting techniques to predictably make

Yoshida-Saxler's gate structure, improving alignment, as I previously explained.

§XIII.A.2 (Ground 2, Motivation).

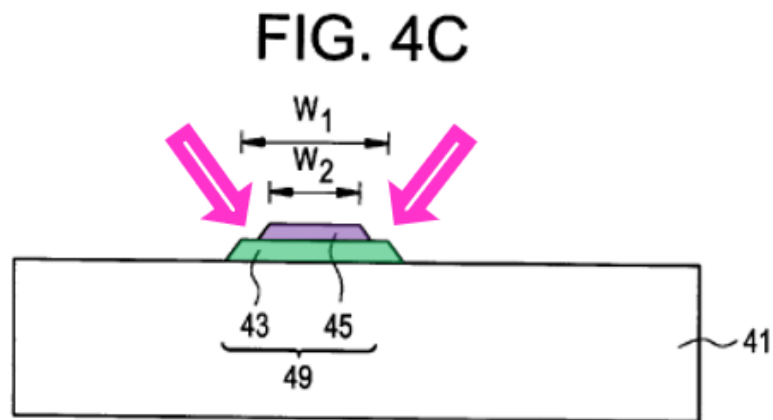
XIV. Ground 5: *Yoshida* in view of *Ahn*

A. Overview of Ground 5

[238] In my opinion, *Yoshida* and *Ahn* render claims 1-3 obvious. A POSITA would have found it obvious to use *Ahn's* techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal using a single mask to obtain the gate structure of *Yoshida*.

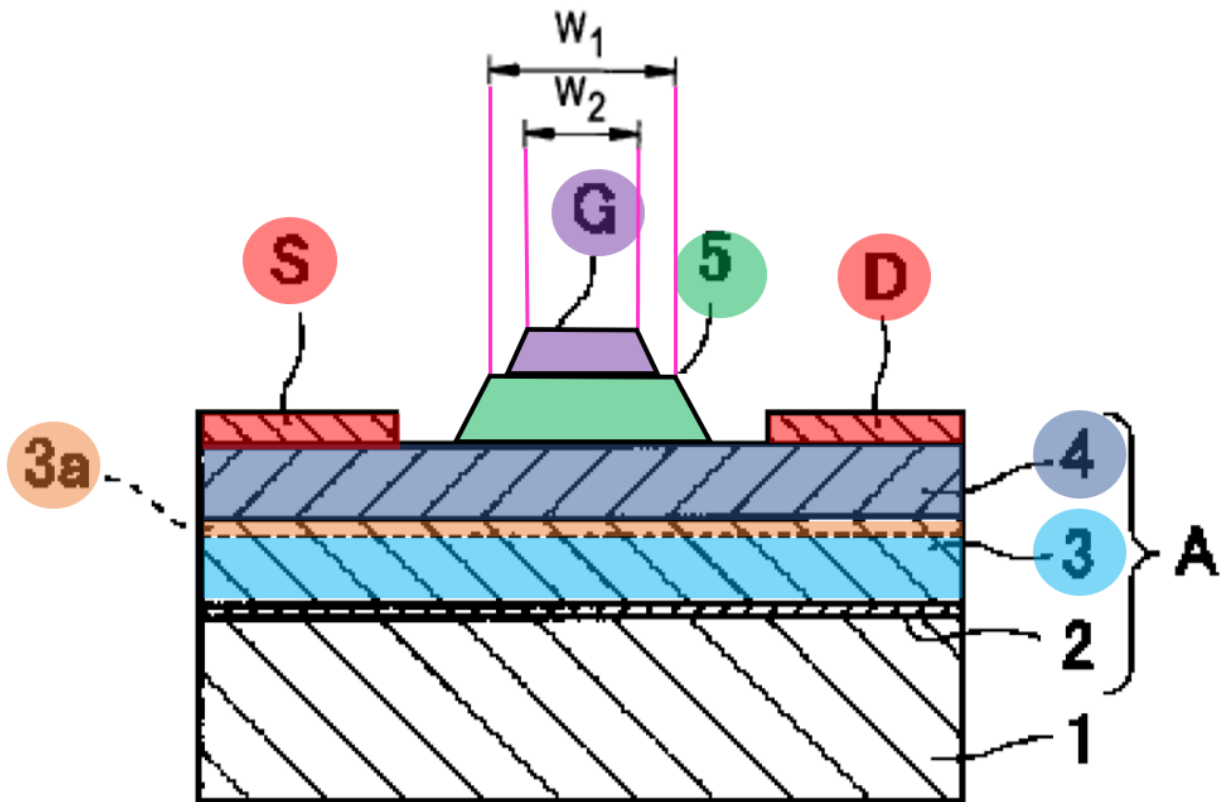
1. Ground 5: The Combination of *Yoshida* and *Ahn*

[239] *Ahn* describes a thin film transistor and depicts sloped sidewalls of an **underlying layer** and **top gate layer** in a stacked gate structure having a pair of **ledges** on either side of the **top gate layer**. *Ahn*, Figs. 4A-4C. *Ahn* explains it etches layers to different thicknesses W_1 and W_2 to create those ledges because this structure improves performance and prevents deterioration. *Ahn*, 4:39-59, 5:21-27, 5:63-6:26, 7:24-31. *Ahn's* layers are symmetric, and *Ahn* states its side surfaces preferably have an “inclined shape.” *Ahn*, 6:12-37, Fig. 4C.



Ahn, Fig. 4C.

[240] Using *Ahn*'s techniques to create *Yoshida*'s gate structure would lead to the following device, which is substantially the same as *Yoshida*'s original device but with the widths W_1 and W_2 and inclined sidewalls of *Ahn*'s device.



Yoshida, Fig. 1 (modified).

2. Ground 5: Motivation to Combine

[241] In my opinion, a POSITA would have found it obvious to make the stacked gate structure of *Yoshida*'s gate electrode and layer 5 with sloped sidewalls using *Ahn*'s methods of forming a transistor gate.

[242] As I have explained, a POSITA would have been familiar with many ways to create *Yoshida*'s stepped gate structure and would have used these methods interchangeably. §VIII (Technology Background). The '347 patent was allowed without disclosing any particular method to etch the gate metal and obtain

the claimed ledges because such methods were well within the skill level of a POSITA. Ex. 1002, 25-30, 44-55, 74-76, 80-99; §§VI.B (Prosecution History), VIII (Technology Background). Appropriate methods such as lift-off when removing the photomask or isotropic etching were well within the level of ordinary skill. §VIII (Technology Background). As a reason for the allowance, the Examiner identified that the cited art did not disclose forming sloped sidewalls of its p-type gate material in structures that also had ledges. Ex. 1002, 29, 55.

[243] In my opinion, *Ahn* would have provided a known and obvious way to create that same structure for *Yoshida*'s device. A POSITA would have found it obvious to modify *Yoshida* by using *Ahn*'s approach for making a stepped gate in a thin-film transistor to improve alignment and precision, which would result in a stacked-stepped gate structure with sloped sidewalls. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C.

[244] *Ahn* provides a flexible approach, recognizing the interchangeability of methods of making the gate structure—it teaches many ways to obtain the *Yoshida* gate structure, including etching both simultaneously or etching them sequentially using combinations of conventional wet and dry etching techniques. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C. For example, *Ahn* exploits differences between rates of dissolution of its layers to make the top gate

layer narrower than the bottom. *Ahn*, 7:7-14-46. A POSITA would have understood that *Yoshida*'s layer 5, which was a p-type doped semiconductor, would have had a slower rate of dissolution than its metallic gate contact and found it obvious to use *Ahn*'s approach. *Ahn*'s methods result in symmetrically aligned layers. *Ahn*, 6:15-37, Fig. 4C. A POSITA would have found the combination a simple substitution of *Ahn*'s known methods that could be predictably implemented when making *Yoshida*'s device to improve alignment and symmetry between layers.

B. Independent Claim 1

1. [1p]: A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[245] *Yoshida* discloses Limitation [1p], as I previously explained.

§XIII.B.1 (Ground 4, Limitation [1p]).

2. [1a]: forming a GaN layer;

[246] *Yoshida* discloses Limitation [1a], as I previously explained.

§XIII.B.2 (Ground 4, Limitation [1a]).

3. [1b]: forming a barrier layer on the GaN layer;

[247] *Yoshida* discloses Limitation [1b], as I previously explained.

§XIII.B.3 (Ground 4, Limitation [1b]).

4. **[1c]: depositing source and drain contacts on the barrier layer;**

[248] *Yoshida* discloses Limitation [1c], as I previously explained.

§XIII.B.4 (Ground 4, Limitation [1c]).

5. **[1d]: depositing a p-type gate material on the barrier layer,**

[249] *Yoshida* discloses Limitation [1d], as I previously explained.

§XIII.B.5 (Ground 4, Limitation [1d]).

6. **[1e]: depositing a gate metal on the p-type gate material;**

[250] *Yoshida* discloses Limitation [1e], as I previously explained.

§XIII.B.6 (Ground 4, Limitation [1e]).

7. **[1f]: forming a photoresist over the gate metal;**

[251] In my opinion, *Yoshida* and *Ahn* renders obvious Limitation [1f].

[252] As I have explained, *Ahn* forms “**photoresist 47**” over the **top gate metal** layer before etching. *Ahn*, 5:55-6:36, 7:7-46. *Ahn* emphasizes that this single-mask approach improves symmetry and reduces masking steps. *Ahn*, 5:55-62, 6:27-37, 7:16-46, Figs. 4A-4C. In my opinion, it would have been obvious and predictable to make *Yoshida*’s gate structure with *Ahn*’s approach to using a single photomask over the gate metal, as I explained above. §XIV.A.2 (Ground 5, Motivation).

FIG. 4A

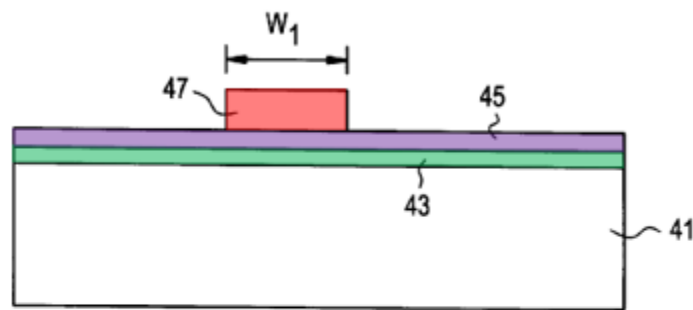
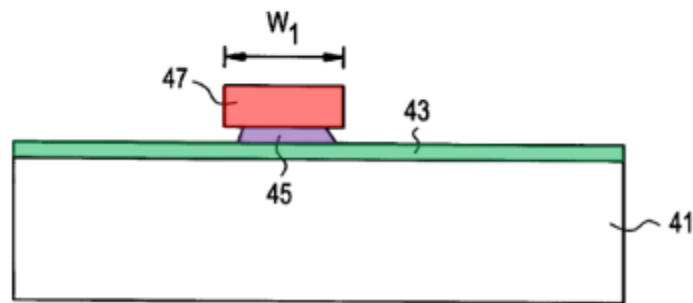


FIG. 4B



Ahn, Figs. 4A-4B.

8. [1g]: etching the gate metal and the p-type gate material,

[253] In my opinion, *Yoshida* in view of *Ahn* renders obvious

Limitation [1g].

[254] As I explained, *Ahn* etches its top layer gate metal and its underlying layer. *Ahn*, 5:55-6:36, 7:7-46. It would have been obvious and predictable to make *Yoshida*'s gate structure with *Ahn*'s approach of using a single a photomask over

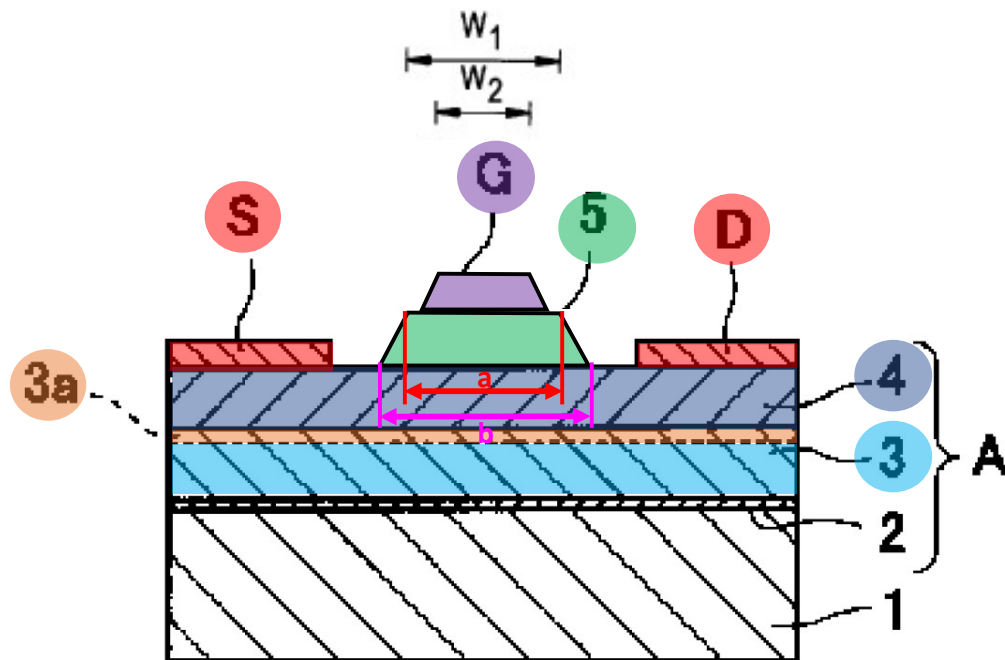
the gate metal, as I explained above. §XIV.A.2 (Ground 5, Motivation). This satisfies both parties' construction. §IX.B (Claim Construction).

9. **[1h]: wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer; and**

[255] In my opinion, *Yoshida* and *Ahn* renders obvious Limitation [1h].

[256] First, *Yoshida* alone renders this limitation obvious at least under Patent Owner's construction because at least slightly sloped sidewalls are common—few structures, if any, have perfectly vertical sidewalls in practice, even if depicted as vertical in functional diagrams, which I explain above. *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5; §XIII.B.9 (Ground 4, [1h]).

[257] Second, it would have been obvious and predictable to combine *Yoshida* techniques with *Ahn*'s single mask processes to differentially etch multiple metal layers to obtain a narrower gate contact and ledges on an underlying in a stacked structure, with improved reproducibility, precision, and symmetry. *Ahn*, 5:55-6:36, 7:7-46; §XIV.A.2 (Ground 5, Motivation). *Yoshida-Ahn* renders the sidewalls of Limitation [1h] obvious under either parties' construction. §§IX.A (Claim Construction), XIV.A (Ground 5, Motivation and Combination). I measured the bottom of the **layer 5** below (width “**b**”) and found it is approximately 1.34 times the width of the top (width “**a**”), i.e. more than 10%.



Yoshida, Fig. 1 (modified).

10. [1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

[258] In my opinion, *Yoshida* and *Ahn* also renders obvious Limitation [1i].

As I have explained, *Ahn* etches its **top layer gate metal** under a **photoresist** such that is narrower than the **underlying layer** to form a pair of **ledges** on either side of the **top gate metal**. *Ahn*, 5:55-6:36, 7:7-46.

FIG. 4A

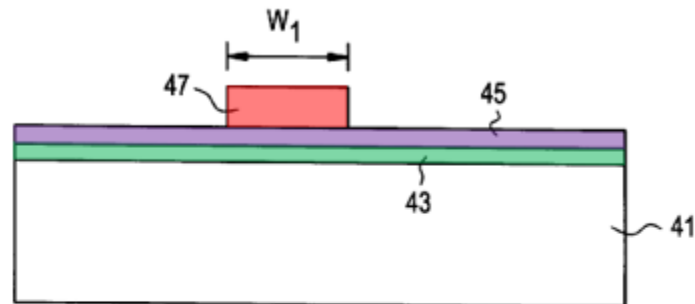


FIG. 4B

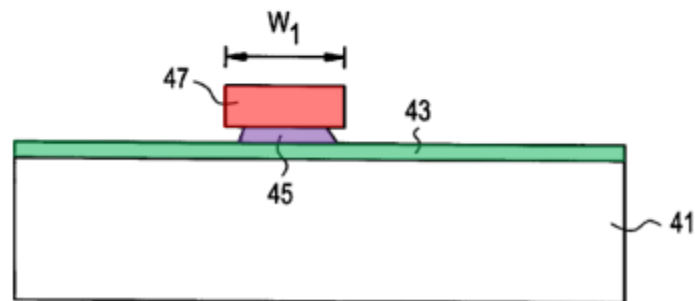
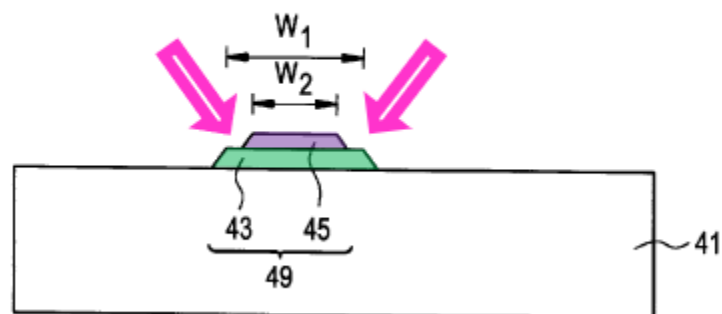


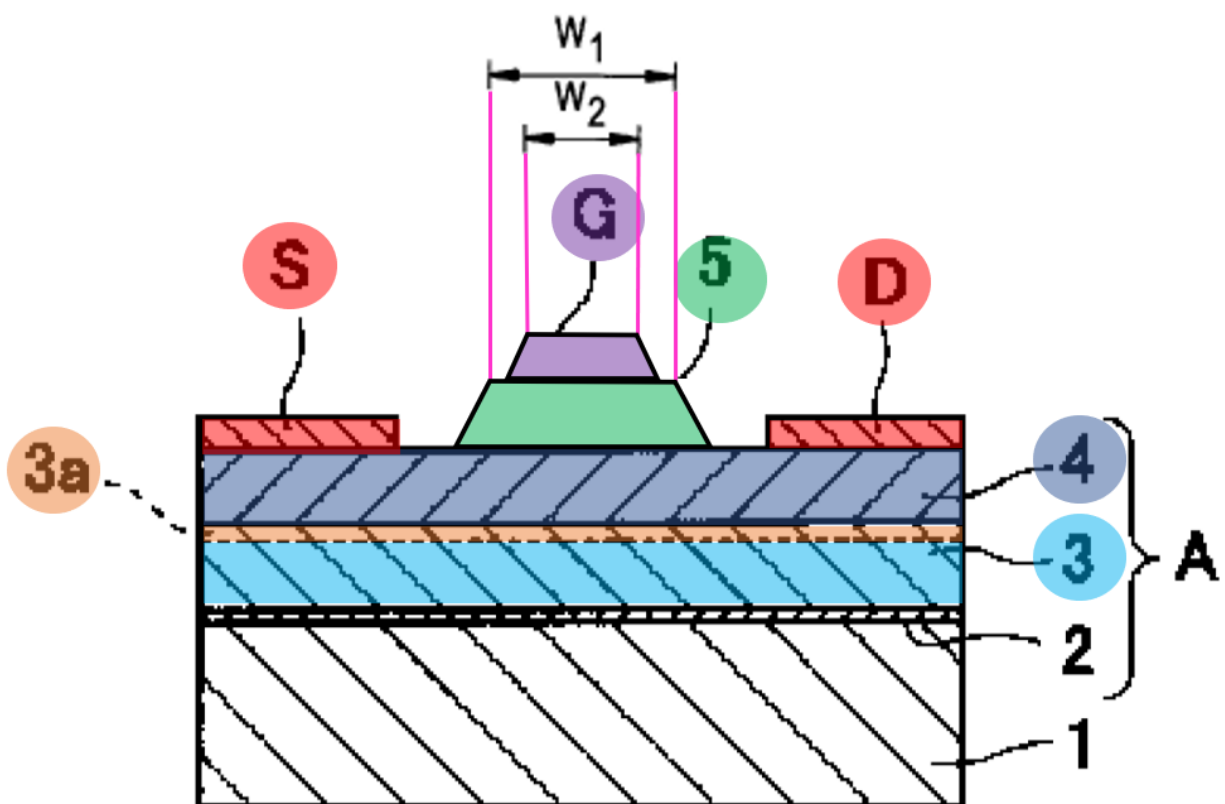
FIG. 4C



Ahn, Figs. 4A-4C.

[259] In my opinion, it would have been obvious to combine *Yoshida's* techniques with *Ahn's* single mask processes to differentially etch multiple metal

layers and obtain a narrower gate contact and ledges on an underlying in a stacked structure, for reasons I previously explained. *Ahn*, 5:55-6:36, 7:7-46; §XIV.A.2 (Ground 5, Motivation to Combine). This satisfies both parties' construction. §IX.C (Claim Construction).



Yoshida, Fig. 1 (modified).

- C. [Claim 2]: The method according to claim 1, wherein the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal, such that the width of the gate metal is less than a width of the p-type gate material.**

[260] As I explained, claim 2 does not further limit claim 1 because its requirements are included in Limitation [1i]. §X.C (Ground 1, Claim 2). Thus, *Yoshida* and *Ahn* render obvious claim 2 for the reasons I explained for Limitation [1i]. §XIV.B.10 (Ground 5, Limitation [1i]).

- D. [Claim 3]: The method according to claim 1, wherein the pair of ledges of the p-type gate material are self-aligned.**

[261] In my opinion, *Yoshida* and *Ahn* renders obvious Claim 3.

[262] As I have explained, *Ahn* uses a **single mask** to etch a gate having a **top metal layer** and **underlying layer** with horizontal **ledges**, which is a “self-aligned” process. *Ahn*, 5:55-6:36, 7:7-46, Figs. 4A-4C. *Ahn* describes multiple ways to etch two layers under a single photomask and arrive at this same stacked, stepped gate structure. *Ahn*, 7:7-46.

FIG. 4A

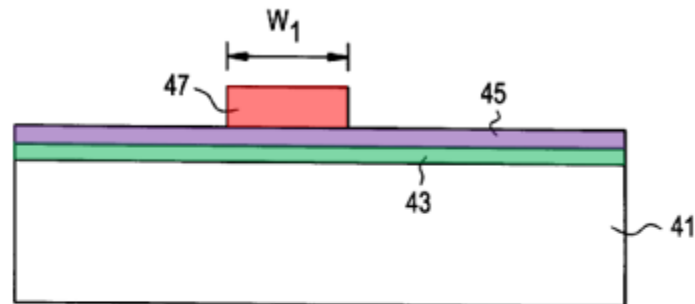


FIG. 4B

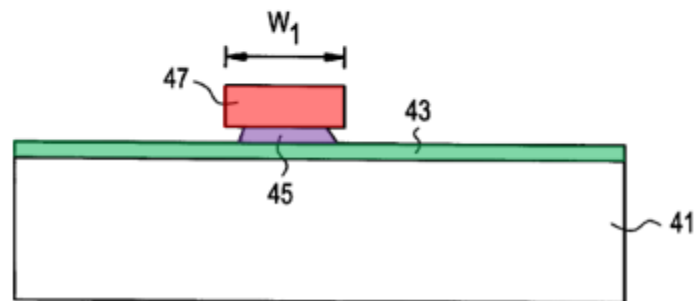
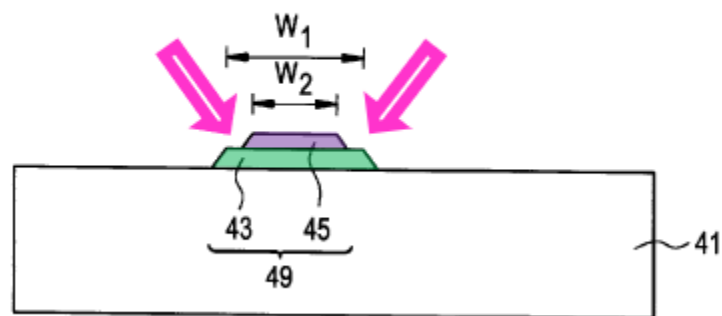


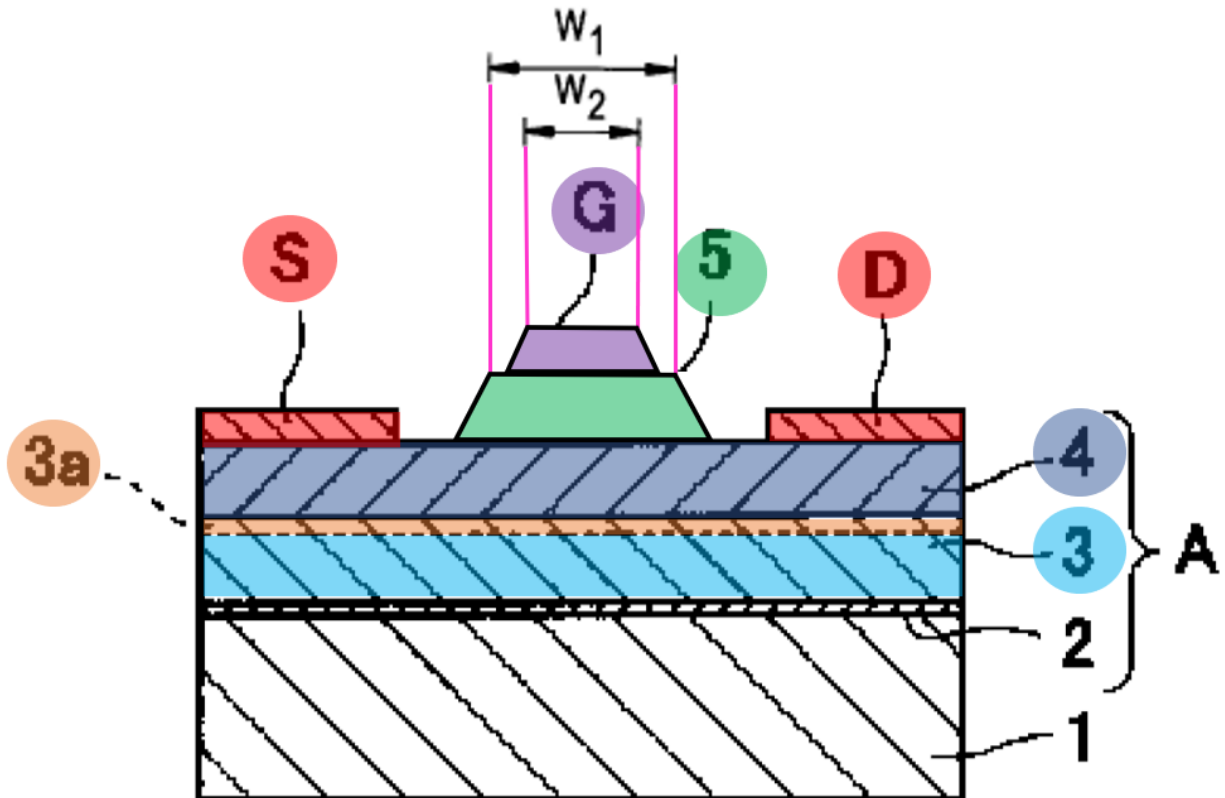
FIG. 4C



Ahn, Figs. 4A-4C.

[263] In my opinion, it would have been obvious and predictable to combine *Yoshida*'s techniques with *Ahn*'s single-mask, self-aligned processes to

differentially etch multiple metal layers to obtain sloped edges in a stacked structure, as I have previously explained. *Ahn*, 5:55-6:36, 7:7-46; §XIV.A.2 (Ground 5, Motivation to Combine).



Yoshida, Fig. 1 (modified).

XV. CONCLUSION

[264] For the reasons set forth above, in my opinion, a person of ordinary skill in the art would have found claims 1-3 of the '347 patent obvious.

[265] In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

[266] I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 20, 2023

By: _____

A handwritten signature in cursive script, appearing to read "James R. Shealy", written over a horizontal line.

James Richard Shealy, Ph.D.