US 20060019435A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2006/0019435 A1

Sheppard et al. (43) Pub. Date: Jan. 26, 2006

(54) METHODS OF FABRICATING NITRIDE-BASED TRANSISTORS WITH A CAP LAYER AND A RECESSED GATE

(76) Inventors: **Scott Sheppard**, Chapel Hill, NC (US); **Richard Peter Smith**, Carrboro, NC (US)

Correspondence Address:
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627 (US)

(21) Appl. No.: 10/897,726

(22) Filed: Jul. 23, 2004

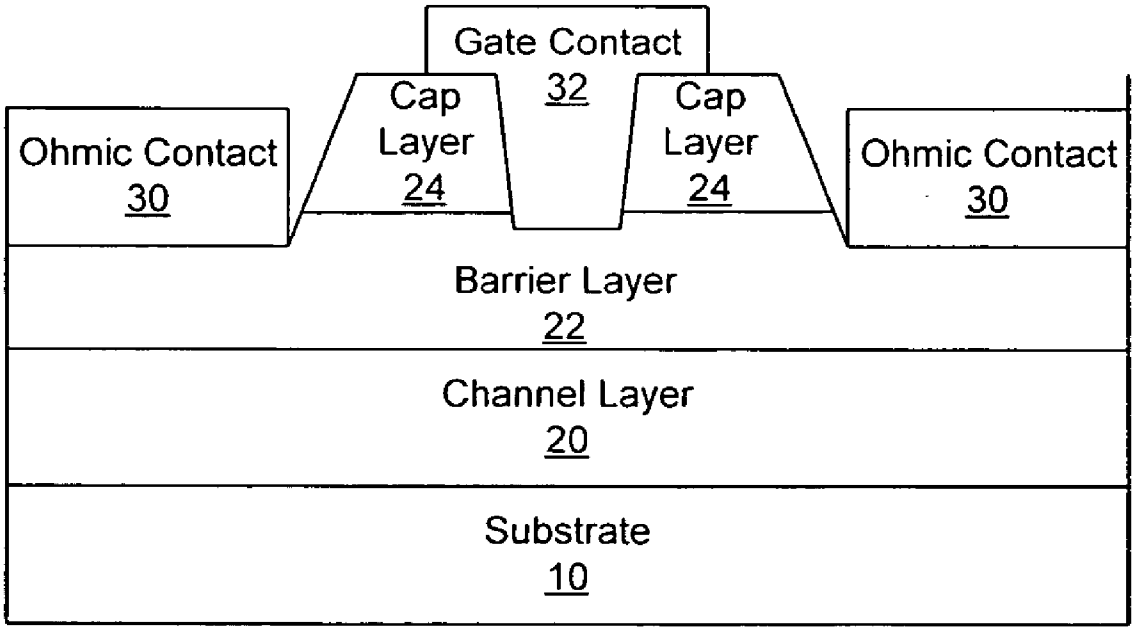
Publication Classification

(51) Int. Cl.
H01L 21/338 (2006.01)

(52) U.S. Cl. **438/167**; 438/172

(57) ABSTRACT

An anneal of a gate recess prior to formation of a gate contact, such as a Schottky contact, may reduce gate leakage and/or provide a high quality gate contact in a semiconductor device, such as a transistor. The use of an encapsulation layer during the anneal may further reduce damage to the semiconductor in the gate recess of the transistor. The anneal may be provided, for example, by an anneal of ohmic contacts of the device. Thus, high quality gate and ohmic contacts may be provided with reduced degradation of the gate region that may result from providing a recessed gate structure as a result of etch damage in forming the recess.



 INNOSCIENCE EXHIBIT 1021

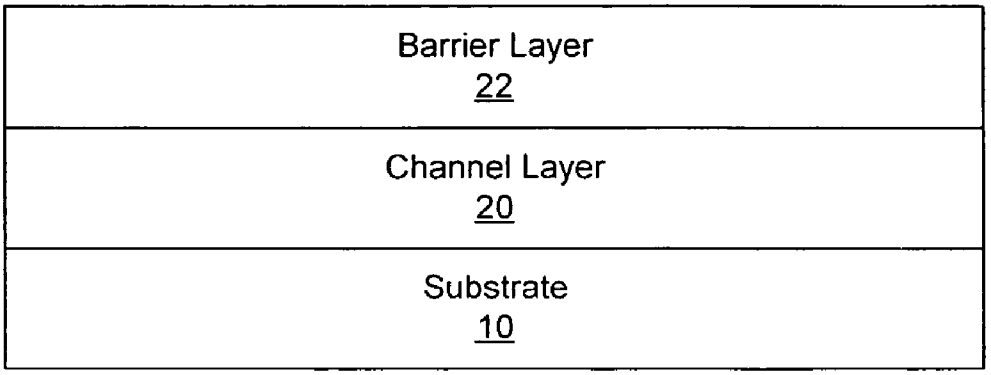


Figure 1A

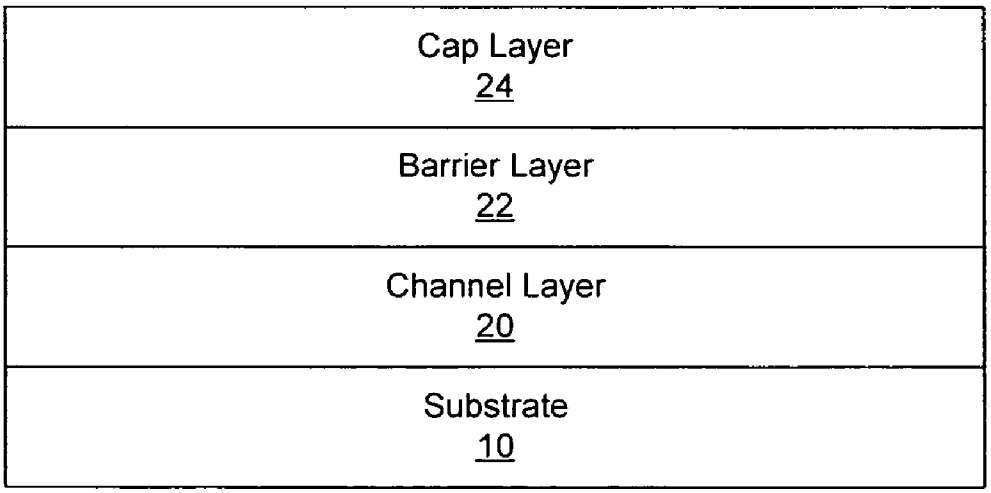


Figure 1B

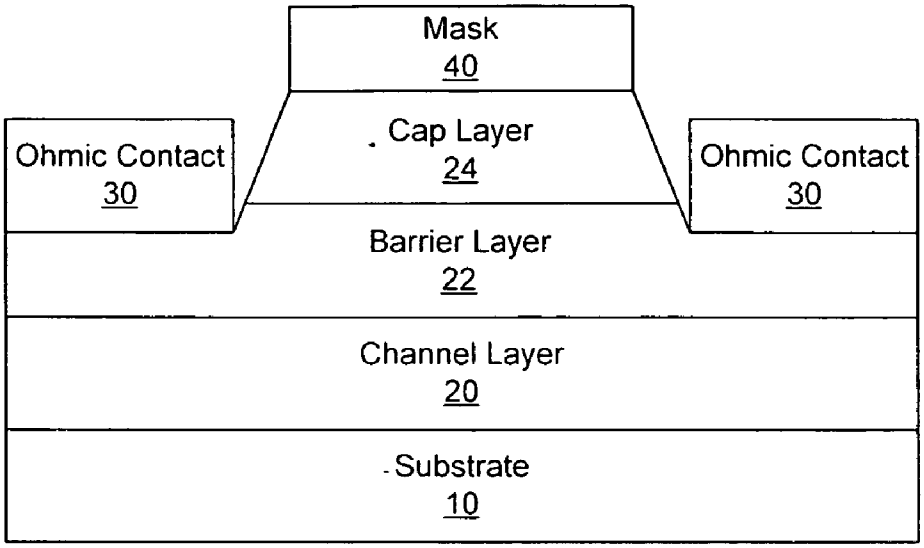


Figure 1C

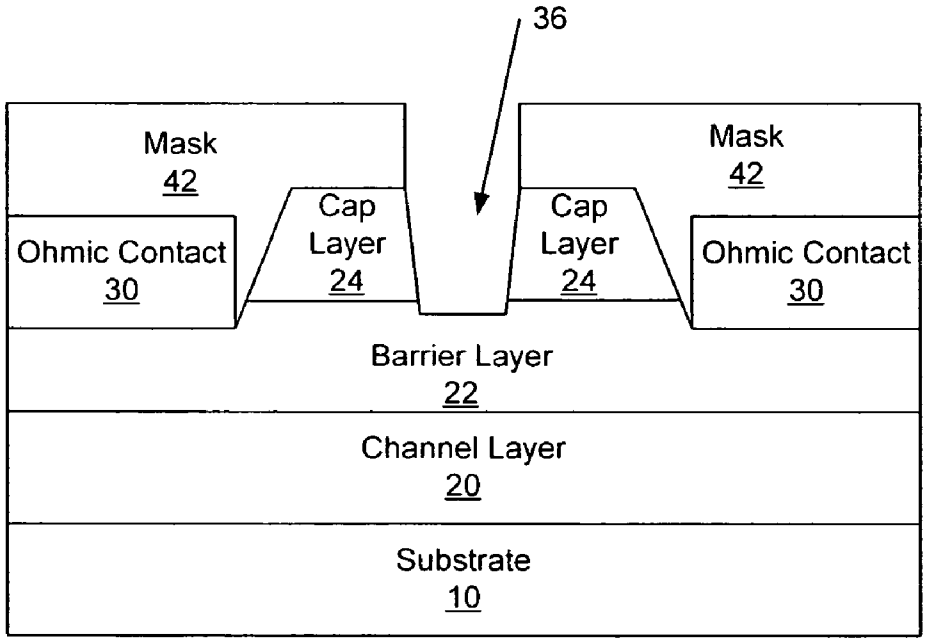


Figure 1D

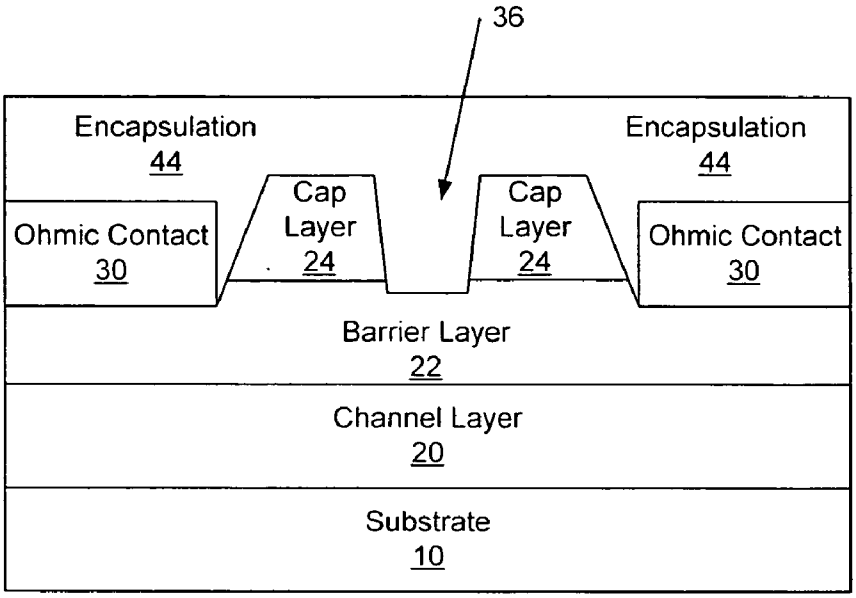


Figure 1E

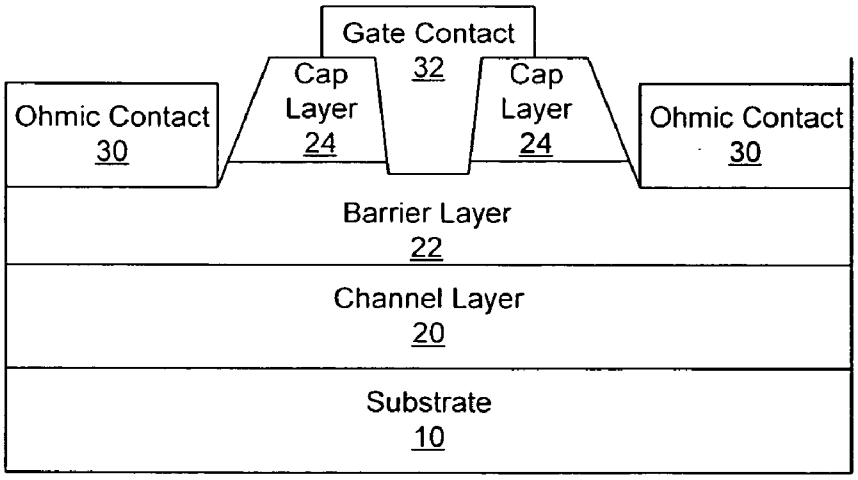


Figure 1F

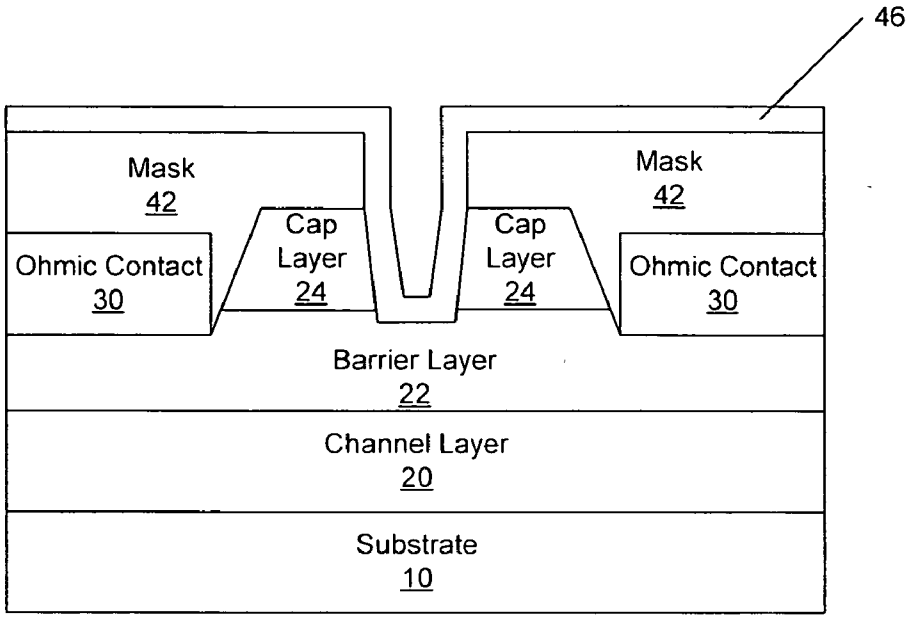


Figure 2A

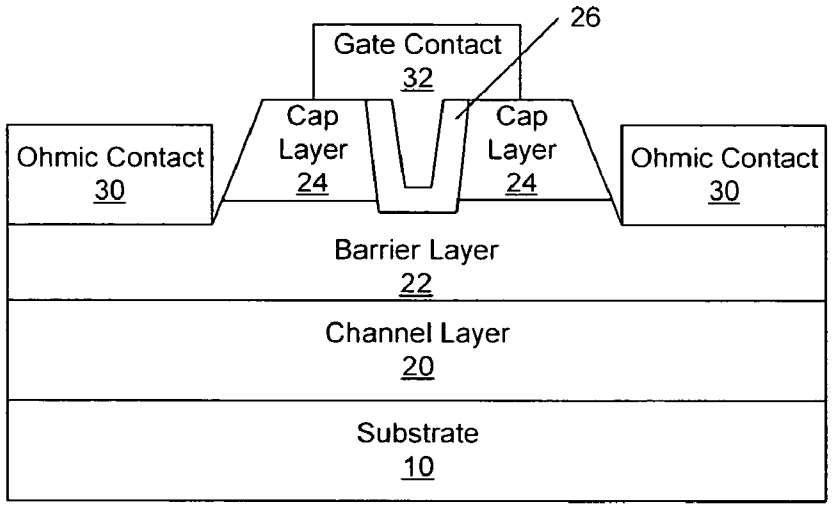


Figure 2B

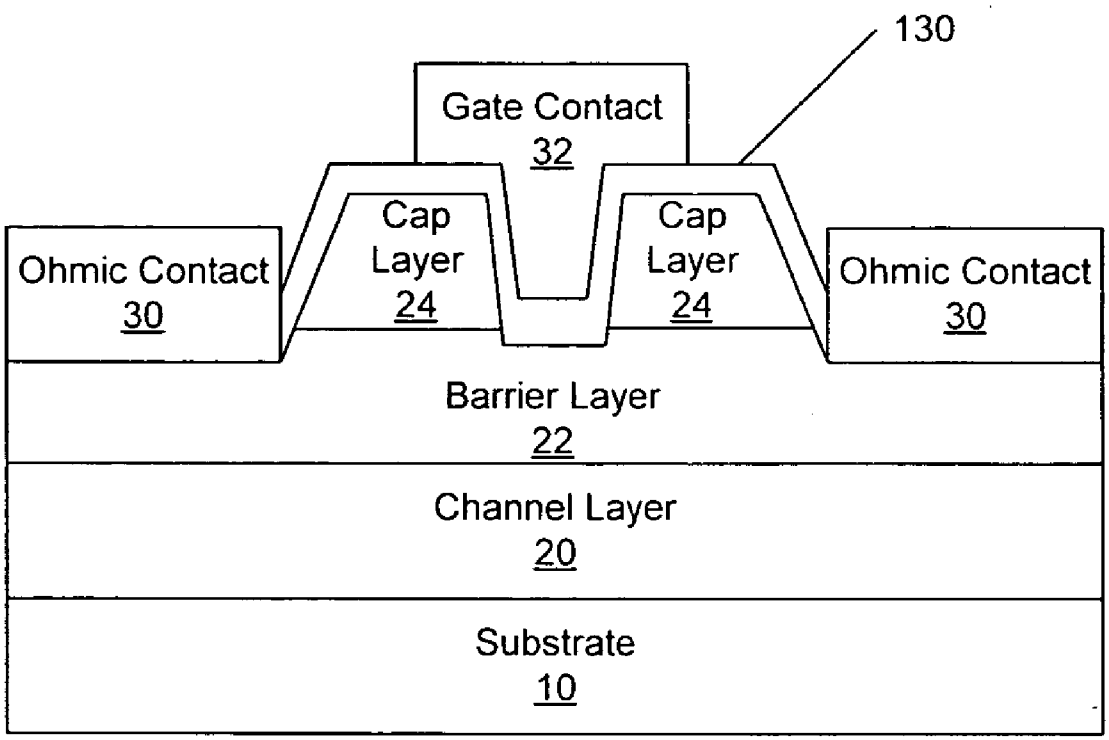

130
Gate Contact
32
Cap
Layer
24
Cap
Layer
24
Ohmic Contact
30
Ohmic Contact
30
Barrier Layer
22
Channel Layer
20
Substrate
10

Figure 3

METHODS OF FABRICATING NITRIDE-BASED TRANSISTORS WITH A CAP LAYER AND A RECESSED GATE

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor devices and, more particularly, to transistors that incorporate nitride-based active layers.

BACKGROUND

[0002] Materials such as silicon (Si) and gallium arsenide (GaAs) have found wide application in semiconductor devices for lower power and (in the case of Si) lower frequency applications. These, more familiar, semiconductor materials may not be well suited for higher power and/or high frequency applications, however, because of their relatively small bandgaps (e.g., 1.12 eV for Si and 1.42 for GaAs at room temperature) and/or relatively small breakdown voltages.

[0003] In light of the difficulties presented by Si and GaAs, interest in high power, high temperature and/or high frequency applications and devices has turned to wide bandgap semiconductor materials such as silicon carbide (2.996 eV for alpha SiC at room temperature) and the Group III nitrides (e.g., 3.36 eV for GaN at room temperature). These materials, typically, have higher electric field breakdown strengths and higher electron saturation velocities as compared to gallium arsenide and silicon.

[0004] A device of particular interest for high power and/or high frequency applications is the High Electron Mobility Transistor (HEMT), which, in certain cases, is also known as a modulation doped field effect transistor (MODFET). These devices may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity. The 2DEG is an accumulation layer in the undoped ("unintentionally doped"), smaller bandgap material and can contain a very high sheet electron concentration in excess of, for example, 10^{13} carriers/cm^2. Additionally, electrons that originate in the wider-bandgap semiconductor transfer to the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering.

[0005] This combination of high carrier concentration and high carrier mobility can give the HEMT a very large transconductance and may provide a strong performance advantage over metal-semiconductor field effect transistors (MESFETs) for high-frequency applications.

[0006] High electron mobility transistors fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material system have the potential to generate large amounts of RF power because of the combination of material characteristics that includes the aforementioned high breakdown fields, their wide bandgaps, large conduction band offset, and/or high saturated electron drift velocity. A major portion of the electrons in the 2DEG is attributed to polarization in the AlGaN. HEMTs in the GaN/AlGaN system have already been demonstrated. U.S. Pat. Nos. 5,192,987 and 5,296,395 describe AlGaN/GaN HEMT structures and methods of manufacture. U.S. Pat. No. 6,316,793, to Sheppard et al., which is commonly assigned and is incorporated herein by reference, describes a HEMT device having a semi-insulating silicon carbide substrate, an aluminum nitride buffer layer on the substrate, an insulating gallium nitride layer on the buffer layer, an aluminum gallium nitride barrier layer on the gallium nitride layer, and a passivation layer on the aluminum gallium nitride active structure.

[0007] One step in the fabrication of some nitride-based transistors is the formation of a gate contact in a recess. A thick cap structure of the transistor may be desirable in achieving high current capability and low dispersion. However, a gate recess through the cap layer may be desirable to achieve high breakdown voltage, low RF dispersion and/or high transconductance with concomitant high-frequency performance. On the other hand, an etching process used to form a recessed gate structure may damage the underlying barrier layer(s) from which electrons originate. U.S. patent application Ser. No. 10/758,871, filed Jan. 16, 2004 and entitled "NITRIDE-BASED TRANSISTORS WITH A CAP LAYER AND A LOW-DAMAGE RECESS AND METHODS OF FABRICATION THEREOF", the disclosure of which is incorporated herein as if set forth fully herein, describes devices and techniques to provide a low-damage recess through SiN passivation.

[0008] Other attempts to mitigate high leakage on etched GaN and AlGaN surfaces have included using a high temperature anneal after a Schottky metal is deposited. Such attempts have used anneal temperatures of 400-600° C. Post-Schottky high-temperature annealing appears to improve a high leakage Schottky/AlGaN contact to a moderately leaky Schottky/AlGaN contact.

SUMMARY OF THE INVENTION

[0009] Some embodiments of the present invention provide methods of fabricating high electron mobility transistors (HEMTs), including forming a channel layer, forming a barrier layer on the channel layer, forming a cap layer on the barrier layer and forming a gate recess in the cap layer that extends to the barrier layer. The barrier layer, channel layer and cap layer with the gate recess are annealed and then a gate contact is formed in the annealed gate recess. The gate contact may be a Schottky contact.

[0010] In further embodiments of the present invention, annealing the barrier layer, channel layer and cap layer with the gate recess includes annealing the barrier layer, channel layer and cap layer with the gate recess at a temperature of at least about 700° C. The annealing may be preceded by forming an encapsulation layer on the cap layer and in the gate recess. The annealing may be followed by removing the encapsulation layer and forming a Schottky gate contact may be preceded by removing the encapsulation layer. The encapsulation layer may include AlN.

[0011] In additional embodiments of the present invention, the methods further include forming ohmic contact recesses in the cap layer on opposite sides of the gate recess and forming ohmic contact material patterns in the ohmic contact recesses. In some embodiments, annealing the barrier layer, channel layer and cap layer with the gate recess includes annealing the barrier layer, channel layer, ohmic contact material patterns and cap layer with the gate recess. Furthermore, forming ohmic contact material patterns may be followed by, and annealing may be preceded by, forming

an encapsulation layer on the cap layer, the ohmic contact material patterns and in the gate recess. The annealing may be followed by, and forming a gate contact may be preceded by removing the encapsulation layer. The encapsulation layer may include AlN.

[0012] In still further embodiments of the present invention, forming a gate recess includes patterning a mask layer on the cap layer to have an opening corresponding to the gate recess and etching the cap layer using the patterned mask layer as an etch mask to provide the gate recess. The annealing may be preceded by forming an encapsulation layer on the patterned mask layer and the gate recess. The encapsulation layer may include AlN. The annealing may be followed by removing the mask layer and the encapsulation layer utilizing a self-aligned lift-off technique so as to provide a portion of the encapsulation layer that remains in the gate recess. The portion of the encapsulation layer in the gate recess may be removed prior to forming the gate contact.

[0013] In some embodiments of the present invention, an insulating layer is formed on the cap layer and in the gate recess. The gate contact may be formed on the insulating layer in the gate recess. The gate contact may also extend onto the insulating layer on the cap layer.

[0014] In some embodiments of the present invention, forming a cap layer includes forming a GaN layer on the barrier layer. For example, the GaN layer may be an undoped GaN layer, an AlGaN layer graded to GaN, an AlGaN layer graded to GaN and a doped GaN layer and/or a doped GaN layer. Forming a cap layer may also include forming a GaN layer on the barrier layer and forming a SiN layer on the GaN layer. Furthermore, forming a gate recess may include forming a gate recess that extends through the cap layer and into but not through the barrier layer. In particular embodiments of the present invention, the cap layer includes a GaN based semiconductor material.

[0015] In additional embodiments of the present invention, methods of fabricating high electron mobility transistors include forming a first layer of GaN based semiconductor material on a substrate, forming a second layer of AlGaN based semiconductor material on the first layer, the second layer being configured to induce a two-dimensional electron gas in a region proximate an interface between the first layer and the second layer and forming a third layer of GaN based semiconductor material on the second layer of GaN based semiconductor material. The methods further include forming a gate recess in the third layer that extends to the second layer, annealing the first layer, second layer and third layer with the gate recess and then forming a gate contact in the annealed gate recess. The gate contact may be a Schottky gate contact.

[0016] In further embodiments of the present invention, the annealing is preceded by forming an encapsulation layer on the third layer of GaN based semiconductor material and in the gate recess. The anneal may be followed by removing the encapsulation layer. Forming a gate contact may be preceded by removing the encapsulation layer.

[0017] In still further embodiments of the present invention, the methods further include forming ohmic contact recesses in the third layer of GaN based semiconductor material on opposite sides of the gate recess and forming ohmic contact material patterns in the ohmic contact recesses. In such a case, annealing the first layer, second layer and third layer with the gate recess includes annealing the first layer, second layer, ohmic contact material patterns and third layer with the gate recess.

[0018] In additional embodiments of the present invention, forming a gate recess includes patterning a mask layer on the third layer of GaN based semiconductor material to have an opening corresponding to the gate recess and etching the third layer of GaN based semiconductor material using the patterned mask layer as an etch mask to provide the gate recess. In such a case, the annealing is preceded by forming an encapsulation layer on the patterned mask layer and the gate recess and is followed by removing the mask layer and the encapsulation layer utilizing a self-aligned lift-off technique so as to provide a portion of the encapsulation layer that remains in the gate recess. The encapsulation layer may include AlN, SiO_2, and oxynitride, an ONO structure and/or SiN.

[0019] In some embodiments of the present invention, the portion of the encapsulation layer that remains in the gate recess is removed prior to forming the gate contact. Furthermore, an insulating layer may be formed on the third layer of GaN-based material and in the recess and the gate contact formed on the insulating layer in the gate recess. The gate contact may also be formed on the insulating layer on the third layer of GaN-based material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] **FIGS. 1A-1F** are schematic drawings illustrating fabrication of transistors according to some embodiments of the present invention.

[0021] **FIGS. 2A and 2B** are schematic drawings illustrating fabrication of transistors according to further embodiments of the present invention.

[0022] **FIG. 3** is a schematic drawing illustrating fabrication of transistors according to further embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0023] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. However, this invention should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. As used herein the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0024] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations,

elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0025] It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Like numbers refer to like elements throughout the specification.

[0026] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0027] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another elements as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in the Figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower", can therefore, encompasses both an orientation of "lower" and "upper," depending of the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

[0028] Embodiments of the present invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments of the present invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the present invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the present invention.

[0029] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0030] It will also be appreciated by those of skill in the art that references to a structure or feature that is disposed "adjacent" another feature may have portions that overlap or underlie the adjacent feature.

[0031] Some embodiments of the present invention utilize an anneal of a recess prior to formation of a Schottky contact to reduce gate leakage and/or provide a high quality Schottky contact in a semiconductor device, such as a transistor. In some embodiments of the present invention an anneal of a recess may also restore conductivity to the 2DEG channel under the etched recess area. The use of an encapsulation layer during the anneal may prevent further damage to the semiconductor in the gate recess of the transistor. The anneal may be provided, for example, by an anneal of ohmic contacts of the device. Thus, high quality gate and ohmic contacts may be provided with reduced degradation of the gate region that may result from providing a recessed gate structure as a result of etch damage in forming the recess.

[0032] Embodiments of the present invention may be particularly well suited for use in nitride-based HEMTs such as Group III-nitride based devices. As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). The term also refers to ternary and quaternary compounds such as AlGaN and AlInGaN. As is well understood by those in this art, the Group III elements can combine with nitrogen to form binary (e.g., GaN), ternary (e.g., AlGaN, AlInN), and quaternary (e.g., AlInGaN) compounds. These compounds all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the Group III elements. Accordingly, formulas such as $Al_xGa_{1-x}N$ where $0 \leqq x \leqq 1$ are often used to describe them.

[0033] Suitable structures for GaN-based HEMTs that may utilize embodiments of the present invention are described, for example, in commonly assigned U.S. Pat. No. 6,316,793 and U.S. Patent Publication No. 2002/0066908A1 filed Jul. 12, 2001 and published Jun 6, 2002, for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," U.S. Provisional Patent Application Ser. No. 60/290,195 filed May 11, 2001 for "GROUP III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER," U.S. Patent Publication No. 2002/0167023A1 to Smorchkova et al., published Nov. 14, 2002, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER", U.S. patent application Ser. No. 10/617,843 filed Jul. 11, 2003 for "NITRIDE-BASED TRANSISTORS AND METHODS OF

FABRICATION THEREOF USING NON-ETCHED CONTACT RECESSES," and U.S. Patent Publication No. 2003/0020092 filed Jul. 23, 2002 and published Jan. 30, 2003 for "INSULATING GATE ALGAN/GAN HEMT", the disclosures of which are hereby incorporated herein by reference in their entirety.

[**0034**] Methods of fabrication according to some embodiments of the present invention are schematically illustrated in **FIGS. 1A-1F**. As seen in **FIG. 1A**, a substrate **10** is provided on which nitride based devices may be formed. In particular embodiments of the present invention, the substrate **10** may be a semi-insulating silicon carbide (SiC) substrate that may be, for example, 4H polytype of silicon carbide. Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes. The term "semi-insulating" is used descriptively rather than in an absolute sense. In particular embodiments of the present invention, the silicon carbide bulk crystal has a resistivity equal to or higher than about 1×10^5 Ω-cm at room temperature.

[**0035**] Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate **10**. For example, an AlN buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Additionally, strain balancing transition layer(s) may also be provided as described, for example, in commonly assigned U.S. Patent Publication No. 2003/0102482A1, filed Jul. 19, 2002 and published Jun. 5, 2003, and entitled "STRAIN BALANCED NITRIDE HETROJUNCTION TRANSISTORS AND METHODS OF FABRICATING STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTORS, and U.S. Provisional Patent Application Ser. No. 60/337,687, filed Dec. 3, 2001 and entitled "STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTOR," the disclosures of which are incorporated herein by reference as if set forth fully herein.

[**0036**] Appropriate SiC substrates are manufactured by, for example, Cree, Inc., of Durham, N.C., the assignee of the present invention, and methods for producing are described, for example, in U.S. Pat. Nos. Re. 34,861; 4,946,547; 5,200,022; and 6,218,680, the contents of which are incorporated herein by reference in their entirety. Similarly, techniques for epitaxial growth of Group III nitrides have been described in, for example, U.S. Pat. Nos. 5,210,051; 5,393,993; 5,523,589; and 5,292,501, the contents of which are also incorporated herein by reference in their entirety.

[**0037**] Although silicon carbide may be used as a substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like. In some embodiments, an appropriate buffer layer also may be formed.

[**0038**] Returning to **FIG. 1A**, a channel layer **20** is provided on the substrate **10**. The channel layer **20** may be deposited on the substrate **10** using buffer layers, transition layers, and/or nucleation layers as described above. The channel layer **20** may be under compressive strain. Furthermore, the channel layer and/or buffer nucleation and/or transition layers may be deposited by MOCVD or by other techniques known to those of skill in the art, such as MBE or HVPE.

[**0039**] In some embodiments of the present invention, the channel layer **20** is a Group III-nitride, such as $Al_xGa_{1-x}N$ where $0\leqq x<1$, provided that the energy of the conduction band edge of the channel layer **20** is less than the energy of the conduction band edge of the barrier layer **22** at the interface between the channel and barrier layers. In certain embodiments of the present invention, x=0, indicating that the channel layer **20** is GaN. The channel layer **20** may also be other Group III-nitrides such as InGaN, AlInGaN or the like. The channel layer **20** may be undoped ("unintentionally doped") and may be grown to a thickness of greater than about 20 Å. The channel layer **20** may also be a multi-layer structure, such as a superlattice or combinations of GaN, AlGaN or the like.

[**0040**] A barrier layer **22** is provided on the channel layer **20**. The channel layer **20** may have a bandgap that is less than the bandgap of the barrier layer **22** and the channel layer **20** may also have a larger electron affinity than the barrier layer **22**. The barrier layer **22** may be deposited on the channel layer **20**. In certain embodiments of the present invention, the barrier layer **22** is AlN, AlInN, AlGaN or AlInGaN with a thickness of between about 0.1 nm and about 40 nm. Examples of layers according to certain embodiments of the present invention are described in U.S. Patent Publication No. 2002/0167023A1, to Smorchkova et al., entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosure of which is incorporated herein by reference as if set forth fully herein. In particular embodiments of the present invention, the barrier layer **22** is thick enough and has a high enough Al composition and doping to induce a significant carrier concentration at the interface between the channel layer **20** and the barrier layer **22** through polarization effects. Also, the barrier layer **22** should be thick enough to reduce or minimize scattering of electrons in the channel due to ionized impurities or imperfections deposited at the interface between the barrier layer **22** and the cap layer **24** (**FIG. 1B**).

[**0041**] The barrier layer **22** may be a Group III-nitride and has a bandgap larger than that of the channel layer **20** and a smaller electron affinity than the channel layer **20**. Accordingly, in certain embodiments of the present invention, the barrier layer **22** is AlGaN, AlInGaN and/or AlN or combinations of layers thereof. The barrier layer **22** may, for example, be from about 0.1 nm to about 40 nm thick, but is not so thick as to cause cracking or substantial defect formation therein. In certain embodiments of the present invention, the barrier layer **22** is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}. In some embodiments of the present invention, the barrier layer **22** is $Al_xGa_{1-x}N$ where $0<x<1$. In particular embodiments, the aluminum concentration is about 25%. However, in other embodiments of the present invention, the barrier layer **22** comprises AlGaN with an aluminum concentration of between about 5% and about 100%. In specific embodiments of the present invention, the aluminum concentration is greater than about 10%.

[**0042**] **FIG. 1B** illustrates formation of a relatively thick cap layer **24** on the barrier layer **22**. The cap layer **24** may be a Group III-nitride, and, in some embodiments, a GaN based semiconductor material, such as GaN, AlGAN and/or InGaN. In particular embodiments of the present invention, the cap layer is GaN. Furthermore, the cap layer **24** may be a single layer or multiple layers of uniform and/or non-uniform composition and/or thickness. In some embodi-

ments of the present invention, the cap layer **24** may be a graded AlGaN layer and a GaN layer as described in Shen et al., "High-Power Polarization-Engineered GaN/AlGaN/GaN HEMTs Without Surface Passivation," IEEE Electron Device Letters, Vol. 25, No. 1, pp. 7-9, January 2004, the disclosure of which is incorporated herein by reference as if set forth in its entirety. For example, in some embodiments of the present invention, the cap layer **24** may be a GaN layer with a SiN layer on the GaN layer. The cap layer **24** moves the top surface of the device physically away from the channel, which may reduce the effect of the surface.

[**0043**] The cap layer **24** may be blanket formed on the barrier layer **22** and may be epitaxially grown and/or formed by deposition. For example, the cap layer may be formed by in-situ growth of SiN on a GaN cap layer or ex-situ PECVD of SiN or SiO_2 on top of the GaN cap layer. Typically, the cap layer **24** may have a thickness of from about 2 nm to about 500 nm. For example, a cap layer **24** of SiN and GaN may have a thickness of about 300 nm. Examples of cap layers according to some embodiments of the present invention are described in U.S. Patent Publication No. 2002/0167023A1, to Smorchkova et al., entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER."

[**0044**] As illustrated in **FIG. 1C**, windows are opened in a mask layer to provide a first mask pattern **40** for formation of ohmic contacts **30**. In some embodiments of the present invention, the first mask layer may be a conventional photolithography mask material. In some embodiments of the present invention, the mask material may be SiN, SiO_2 or the like. The windows may be formed utilizing a patterned mask and an etch process to expose the underlying barrier layer **22**. In some embodiments of the present invention, the etch may be a low damage etch. In some embodiments of the present invention the etch is a wet etch with a strong base, such as KOH with UV illumination. In other embodiments, the etch is a dry etch. Examples of low damage etch techniques for Group III-nitrides include etching techniques other than reactive ion etching, such as inductively coupled plasma using Cl_2, BCl_3, CCl_2F_2 and/or other chlorinated species or electron cyclotron resonance (ECR) and/or downstream plasma etching with no DC component to the plasma. Examples of low damage etch techniques for SiN include etching techniques other than reactive ion etching, such as inductively coupled plasma using CF_4/O_2, NF_3/O_2 and/or other fluorinated species or electron cyclotron resonance (ECR) and/or downstream plasma etching with no DC component to the plasma.

[**0045**] As is further illustrated in **FIG. 1C**, for example, with a subsequent photolithography step and evaporation, ohmic metal is patterned to provide ohmic contact material patterns that when annealed provide the ohmic contacts **30**. In some embodiments of the present invention utilizing SiN and/or SiO_2 in the cap layer **24**, the ohmic contacts **30** are spaced apart from the SiN and/or SiO_2 portions of the cap layer **24** a distance sufficiently large to allow for misalignment tolerances in the formation and patterning of the ohmic contact metal. If the ohmic contact metal contacts the SIN and/or SiO_2 portions of cap layer **24**, the metal may diffuse into the cap layer **24** during subsequent heating steps that may result in a short between a gate contact and the ohmic contact(s) **30**.

[**0046**] **FIG. 1D** illustrates the formation of a gate recess. As seen in **FIG. 1D**, a second mask pattern **42** is formed on the ohmic contacts and the cap layer **24** and patterned to form a window that exposes a portion of the cap layer **24**. In some embodiments of the present invention, the second mask pattern **42** may be a conventional photolithography mask material. In some embodiments of the present invention, the mask material may be silicon nitride, silicon dioxide or the like. A recess **36** is then formed through the cap layer **24** to expose a portion of the barrier layer **22**. In some embodiments of the present invention, the recess **36** is formed to extend into the barrier layer **22**. The recess **36** may extend into the barrier layer **22** to, for example, adjust performance characteristics of the device such as threshold voltage, frequency performance, etc. The recess may be formed using the mask **42** and an etch process as described above. In particular embodiments where the ohmic contacts **30** provide source and drain contacts, the recess may be offset between the source and drain contacts such that the recess, and subsequently the gate contact **32**, is closer to the source contact than the drain contact.

[**0047**] **FIG. 1E** illustrates the formation of an optional encapsulation layer **44** after removal of the second mask pattern **42**. The encapsulation layer **44** may be formed on the cap layer **24** and in the recess **36**. The encapsulation layer **44** may be silicon nitride (Si_xN_y), aluminum nitride (AlN), an ONO structure and/or other suitable protective material, such as silicon dioxide (SiO_2) and/or an oxynitride. Other materials may also be utilized for the encapsulation layer **44** as long as the material may be removed without significantly damaging the underlying barrier layer **22**. For example, the encapsulation layer **44** could also include magnesium oxide, scandium oxide, aluminum oxide and/or aluminum oxynitride. Furthermore, the encapsulation layer **44** may be a single layer or multiple layers of uniform and/or non-uniform composition.

[**0048**] In particular embodiments of the present invention, the encapsulation layer **44** may be SiN, AlN, an ONO structure and/or SiO_2. The SiN, AlN and/or SiO_2 may be formed by PVD and/or CVD and may be non-stoichiometric. Suitable encapsulation materials are described in further detail with reference to the protective layer in U.S. patent application Ser. No. 10/758,871, filed Jan. 16, 2004 and entitled "NITRIDE-BASED TRANSISTORS WITH A CAP LAYER AND A LOW-DAMAGE RECESS AND METHODS OF FABRICATION THEREOF", the disclosure of which is incorporated herein as if set forth fully herein.

[**0049**] The encapsulation layer **44** may be blanket formed on the cap layer **24** and into the recess **36** so as to be positioned on the barrier layer **22** in the recess **36** and may be formed by deposition. For example, a silicon nitride layer may be formed by high quality sputtering and/or PECVD. Typically, the encapsulation layer **44** may have a thickness of about 30 nm, however, other thickness layers may also be utilized. For example, the encapsulation layer should be sufficiently thick so as to protect the underlying layers during a subsequent anneal of ohmic contacts. Layers as thin as two or three monolayers may be sufficient for such purposes. However, in general, the encapsulation layer **44** may have a thickness of from about 10 nm to about 500 nm. Also, a high quality SiN protective layer may be grown in-situ with the MOCVD growth of the group III nitride layers.

[0050] After formation of the gate recess **36** and the encapsulation layer **44** if present, but prior to formation of a gate contact, the ohmic contact material is annealed to provide the ohmic contacts **30**. The anneal may be a high temperature anneal. For example, the anneal may be at a temperature of from about 700° C. to about 900° C. and in some embodiments, greater than about 900° C. For example, an anneal may be carried out for from about 30 seconds to about five minutes in an environmental temperature of from about 700° C. to about 900° C. as measured using conventional measuring techniques in rapid thermal anneal systems, such as using a thermocouple embedded in a susceptor holding the wafer and/or optically by pyrometry. Through the use of an ohmic contact anneal, the resistance of the ohmic contacts may be reduced from a high resistance to less than about 1 Ω-mm. Thus, as used herein, the term "ohmic contact" refers to a non-rectifying contact that has a contact resistance of less than about 1 Ω-mm. The anneal of the etched gate recess **36** may remove damage to the barrier layer **22** that may result from fabrication of the gate recess **36**. Thus, for example, the sheet resistance of the region of the barrier layer **22** proximate the gate recess **36** after the high temperature ohmic contact anneal may be substantially the same as the sheet resistance of the region as if the remaining un-etched barrier layer were grown in the reactor.

[0051] As seen in **FIG. 1F**, the encapsulation layer **44** is removed if present and a gate contact **32** is formed in the recess and contacts the exposed portion of the barrier layer **22**. The gate contact may be a "T" gate as illustrated in **FIG. 1F** and may be fabricated using conventional fabrication techniques. Suitable gate materials may depend on the composition of the barrier layer, however, in certain embodiments, conventional materials capable of making a Schottky contact to a nitride based semiconductor material may be used, such as Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WSiN. It is possible that a small gap between the cap layer **24** and the gate contact **32** may arise as a result of, for example, anisotropy of the gate recess etch, resulting in an exposed surface of the barrier layer **22** between the protective layer **24** and the gate contact **32**. This gap may be formed intentionally.

[0052] A passivation layer may also be provided on the structure of **FIG. 1F**. The passivation layer may be blanket deposited on the structure of **FIG. 1F**. In particular embodiments, the passivation layer may be deposited so as to substantially fill the gap between the cap layer **24** and the ohmic contacts **30**, if present, and also the gap between the cap layer **24** and the gate contact **32**, if such gap exists. In certain embodiments of the present invention, the passivation layer may be silicon nitride, aluminum nitride, silicon dioxide, an ONO structure and/or an oxynitride. Furthermore, the passivation layer may be a single or multiple layers of uniform and/or non-uniform composition.

[0053] **FIGS. 2A and 2B** illustrate fabrication of transistors according to further embodiments of the present invention. Fabrication of the transistors of **FIGS. 2A and 2B** may be provided in the same manner as described above with reference to **FIGS. 1A-1D**. However, as seen in **FIG. 2A**, rather than removing the second mask pattern **42**, an encapsulation layer **46** is provided on the mask **42** and in the recess **36**. The encapsulation layer **46** may, for example, be formed of the same materials as described above with reference to the encapsulation layer **44**. In particular embodiments of the present invention, the encapsulation layer **46** is AlN. In further embodiments of the present invention, the encapsulation layer **46** may be any inert ceramic material. Furthermore, the second mask **42** may be SiN.

[0054] In embodiments of the present invention where the second mask **42** is a photo-resist or other material that may be substantially damaged by a subsequent anneal, the second mask **42** and portions of the encapsulation layer **46** are removed, for example, using a self-aligned lift-off technique, to provide a portion **26** of the encapsulation layer **46** in the gate recess. The structure of **FIG. 2A** is then annealed as described above. The encapsulation layer **46** may, in some embodiments of the present invention, have a thickness of from about 1 nm to about 500 nm.

[0055] As is seen in **FIG. 2B**, the second mask **42** and portions of the encapsulation layer **46** are removed, for example, using a self-aligned lift-off technique, to provide a portion **26** of the encapsulation layer **46** in the gate recess. The gate contact **32** is then formed on the portion **26** remaining in the gate recess. In some embodiments, the portion **26** is removed prior to formation of the gate contact **32**. In the embodiments illustrated in **FIG. 2B**, the gate contact may be formed of materials as described above.

[0056] **FIG. 3** illustrates formation of transistors according to further embodiments of the present invention. As seen in **FIG. 3**, the structure of **FIG. 2B** may have the portion **26** removed and an insulating layer **130** formed on the resulting structure including in the gate recess. The gate contact **32** may then be formed on the insulating layer **130**. The insulating layer **130** may be one or more layers and may include, for example, SiN, AlN, SiO_2, and/or an ONO structure. Thus, in some embodiments of the present invention, an insulating gate HEMT may be provided, for example, as described in U.S. Patent Publication No. 2003/0020092 entitled "INSULATING GATE ALGAN/GAN HEMT", to Parikh et al., the disclosure of which is incorporated herein by reference as if set forth fully herein.

[0057] While embodiments of the present invention have been described with reference to a particular sequence of operations, some modification in the sequence may be made or other operations may be included while still benefiting from the teachings of the present invention. For example, the formation of the cap layer **24** prior to ohmic metal deposition may be omitted and the ohmic metal may be deposited and patterned on the barrier layer **22** to provide ohmic contact material regions **30** on the barrier layer **22**. A cap layer could then be formed after deposition and patterning of the ohmic contact material. The cap layer may then be etched to provide the gate recess and the ohmic contact anneal carried out prior to formation of the gate contact.

[0058] Operations described above as being provided in a single step may be provided in multiple steps and, likewise, operations described as multiple steps could be combined into a single step. For example, while the anneal to remove damage from the gate recess etch has been described as provided by the ohmic contact anneal, a separate anneal could also be provided. If the anneal is provided as a separate anneal, the anneal may be carried out, for example, at a temperature of from about 600° C. to about 900° C. for from about 20 minutes to about thirty seconds. Additionally, the etch of the ohmic contact recess and the gate recess may be carried out using a single mask rather than two separate masks as described above.

[0059] While embodiments of the present invention have been described herein with reference to particular HEMT structures, the present invention should not be construed as limited to such structures. For example, additional layers may be included in the HEMT device while still benefiting from the teachings of the present invention. Such additional layers may include GaN cap layers, as for example, described in Yu et al., "Schottky barrier engineering in III-V nitrides via the piezoelectric effect," Applied Physics Letters, Vol. 73, No. 13, 1998, or in U.S. Patent Publication No. 2002/0066908A1 filed Jul. 12, 2001 and published Jun. 6, 2002, for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," the disclosures of which are incorporated herein by reference as if set forth fully herein. In some embodiments, insulating layers such as SiN, an ONO structure or relatively high quality AlN may be deposited for making a MISHEMT and/or passivating the surface. The additional layers may also include a compositionally graded transition layer or layers.

[0060] Furthermore, the barrier layer **22** may also be provided with multiple layers as described in U.S. Patent Publication No. 2002/0167023A1, to Smorchkova et al., entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosure of which is incorporated herein by reference as if set forth fully herein. Thus, embodiments of the present invention should not be construed as limiting the barrier layer to a single layer but may include, for example, barrier layers having combinations of GaN, AlGaN and/or AlN layers. For example, a GaN, AlN structure may be utilized to reduce or prevent alloy scattering. Thus, embodiments of the present invention may include nitride based barrier layers, such nitride based barrier layers may include AlGaN based barrier layers, AlN based barrier layers and combinations thereof.

[0061] In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation.

That which is claimed is:

1. A method of fabricating a high electron mobility transistor (HEMT), comprising:

forming a channel layer;

forming a barrier layer on the channel layer;

forming a cap layer on the barrier layer;

forming a gate recess in the cap layer that extends to the barrier layer;

annealing the barrier layer, channel layer and cap layer with the gate recess; and then

forming a gate contact in the annealed gate recess.

2. The method of claim 1, wherein annealing the barrier layer, channel layer and cap layer with the gate recess comprises annealing the barrier layer, channel layer and cap layer with the gate recess at a temperature of at least about 700° C.

3. The method of claim 1, wherein the step of annealing is preceded by forming an encapsulation layer on the cap layer and in the gate recess and wherein the step of annealing is followed by and the step of forming a gate contact is preceded by removing the encapsulation layer.

4. The method of claim 3, wherein the encapsulation layer comprises AlN.

5. The method of claim 1, further comprising:

forming ohmic contact recesses in the cap layer on opposite sides of the gate recess;

forming ohmic contact material patterns in the ohmic contact recesses; and

wherein annealing the barrier layer, channel layer and cap layer with the gate recess comprises annealing the barrier layer, channel layer, ohmic contact material patterns and cap layer with the gate recess.

6. The method of claim 5, wherein the step of forming ohmic contacts is followed by and the step of annealing is preceded by forming an encapsulation layer on the cap layer, the ohmic contact material patterns and in the gate recess and wherein the step of annealing is followed by and the step of forming a gate contact is preceded by removing the encapsulation layer.

7. The method of claim 6, wherein the encapsulation layer comprises AlN.

8. The method of claim 1, wherein forming a gate recess comprises:

patterning a mask layer on the cap layer to have an opening corresponding to the gate recess; and

etching the cap layer using the patterned mask layer as an etch mask to provide the gate recess.

9. The method of claim 8, wherein annealing is preceded by forming an encapsulation layer on the patterned mask layer and the gate recess and wherein annealing is followed by removing the mask layer and the encapsulation layer utilizing a self-aligned lift-off technique so as to provide a portion of the encapsulation layer that remains in the gate recess.

10. The method of claim 9, wherein the encapsulation layer comprises AlN, SiN, SiO_2, an oxynitride and/or an ONO structure.

11. The method of claim 9, further comprising removing the portion of the encapsulation layer in the gate recess prior to forming the gate contact.

12. The method of claim 11, further comprising:

forming an insulating layer on the cap layer and in the gate recess; and

wherein forming the gate contact comprises forming the gate contact on the insulating layer in the gate recess.

13. The method of claim 12, wherein the gate contact also extends on the insulating layer on the cap layer.

14. The method of claim 1, wherein the gate contact comprises a Schottky contact.

15. The method of claim 1, wherein forming a cap layer comprises forming a GaN layer on the barrier layer.

16. The method of claim 1, wherein forming a cap layer comprises:

forming a GaN layer on the barrier layer; and

forming a SiN layer on the GaN layer.

17. The method of claim 16, wherein the SiN layer is formed in-situ.

18. The method of claim 1, wherein forming a gate recess comprises forming a gate recess that extends through the cap layer and into but not through the barrier layer.

19. The method of claim 1, wherein the cap layer comprises a GaN based semiconductor material.

20. A method of fabricating a high electron mobility transistor, comprising:

forming a first layer of GaN based semiconductor material on a substrate;

forming a second layer of GaN based semiconductor material on the first layer, the second layer being configured to induce a two-dimensional electron gas in a region proximate an interface between the first layer and the second layer;

forming a third layer of GaN based semiconductor material on the second layer of GaN based semiconductor material;

forming a gate recess in the third layer that extends to the second layer;

annealing the first layer, second layer and third layer with the gate recess; and then

forming a gate contact in the annealed gate recess.

21. The method of claim 20, wherein the step of annealing is preceded by forming an encapsulation layer on the third layer of GaN based semiconductor material and in the gate recess and wherein the step of annealing is followed by and the step of forming a gate contact is preceded by removing the encapsulation layer.

22. The method of claim 20, further comprising:

forming ohmic contact recesses in the third layer of GaN based semiconductor material on opposite sides of the gate recess;

forming ohmic contact material patterns in the ohmic contact recesses; and

wherein annealing the first layer, second layer and third layer with the gate recess comprises annealing the first layer, second layer, ohmic contact material patterns and third layer with the gate recess.

23. The method of claim 20, wherein forming a gate recess comprises:

patterning a mask layer on the third layer of GaN based semiconductor material to have an opening corresponding to the gate recess;

etching the third layer of GaN based semiconductor material using the patterned mask layer as an etch mask to provide the gate recess;

wherein annealing is preceded by forming an encapsulation layer on the patterned mask layer and the gate recess; and

wherein annealing is followed by removing the mask layer and the encapsulation layer utilizing a self-aligned lift-off technique so as to provide a portion of the encapsulation layer that remains in the gate recess.

24. The method of claim 23, wherein the encapsulation layer comprises AlN.

25. The method of claim 23, further comprising removing the portion of the encapsulation layer that remains in the gate recess prior to forming the gate contact.

26. The method of claim 25, further comprising:

forming an insulating layer on the third layer of GaN-based material and in the recess; and

wherein forming the gate contact comprises forming the gate contact on the insulating layer in the gate recess.

27. The method of claim 26, wherein the gate contact is also formed on the insulating layer on the third layer of GaN-based material.

28. The method of claim 20, wherein the gate contact comprises a T gate structure.

29. The method of claim 20, wherein forming a gate recess comprises forming a gate recess that extends through the third layer and into but not through the second layer.

30. The method of claim 20, wherein the gate contact is a Schottky contact.

31. The method of claim 22, wherein forming ohmic contact recesses is preceded by forming a passivation layer on the third layer of GaN-based material in-situ.

* * * * *