Metallization for Integrated Circuits Using a Lift-Off Technique

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Abstract—A special lift-off technique for realizing small metal interconnection geometries for integrated circuits is described. 0.6-μm gaps between metal conductors can be obtained even at 0.8-μm metal layer thickness. The slopes of the conductors are tapered. Etching problems inherent in alloy films or sandwiched layers such as Al/Si or Al/Cu/Si are avoided by the technique proposed. SEM micrographs of Al/Si conductor patterns are presented.

Introduction

THE increasing packing density of integrated circuits requires small conductor linewidths and small spaces between conductors.

The interconnection pattern can be formed by conventional chemical etching techniques. However, chemical etching has several drawbacks. First, after delineation of alloy films such as Al/Si or Al/Si/Cu, silicon residues may remain in the field between the conductors [1]. Second, the cross section of the conductors may be considerably reduced by etchant penetration at steep oxide steps [1]. Third, due to the lateral etch attack, the widths of the conductors are reduced, and the spaces between adjacent conductors are increased (Fig. 1). The undercutting Δx per edge (see Fig. 1) might be in the order of the conductor thickness. As long as the desired spacing between adjacent conductors is large enough, i.e., larger than about 3 μm for 1-μm conductor thickness and 1-μm minimum photoresist dimension, the undercutting effect can be compensated by proper dimensioning the corresponding geometries on the photomask. However, if spaces of about 1 μm are required between 1-μm thick metal conductors, the compensation procedure fails.

The edge contours of conductors delineated by wet chemical etching are nearly conical [2], the upper portion of the edges being steep or even overhanging. Edge contours of this kind may lead to poor coverage of such edges by subsequently deposited layers such as passivation and metal layers.

Alternative methods which might be used instead of chemical etching are sputter or ion beam etching, plasma etching, selective plating, selective anodization, and lift-off techniques. This paper reports on results obtained with a lift-off technique, which is suitable for the metallization of integrated circuits with high packing density.

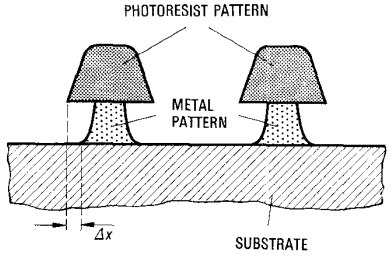

Fig. 1. Schematic illustration of a typical cross section of metal conductors after chemical etching. The undercutting at the bottom of the conductors is Δx.

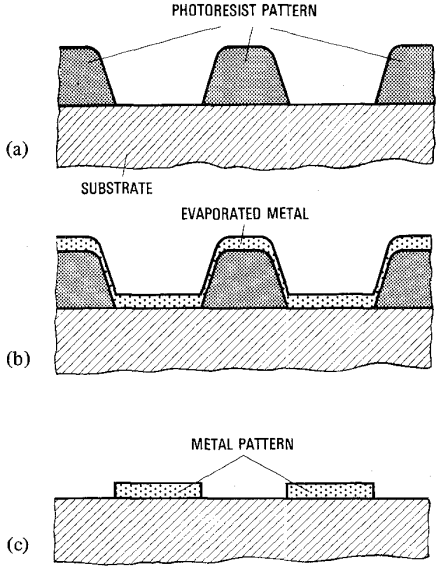

Fig. 2. Schematic illustration of metal pattern definition using the original lift-off technique. (a) Photoresist pattern definition. (b) Metal evaporation. (c) Photoresist stripping, thereby lifting off the overlying metal. The spaces between the metal features are equal to the corresponding photoresist linewidths, as measured at the bottom of the photoresist bars.

Lift-Off Techniques

The lift-off technique for metal pattern formation is shown schematically in Fig. 2. This technique has been known for many years. For instance, it was used in 1966 by Stelter [3] for the fabrication of chromium masks.

The process in Fig. 2 looks very simple. However, there are severe limitations concerning the thickness and the brittleness of the metal layer. The lifting mechanism works reliably only if the metal thickness at the bottom of the photoresist bars is thin enough, i.e., some 100 Å, and if the metal is brittle so that it cracks readily at the photoresist edges [4]. For ductile

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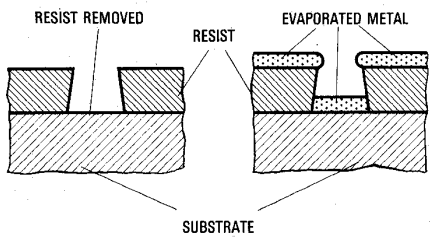


Fig. 3. Metal patterning by a lift-off technique using slightly overhanging sidewalls of electron resist (after Hatzakis [7]).

metals, such as aluminum, the metal layer deposited on the photoresist should be completely separated from the other portions of the metal layer deposited on the substrate. This could be accomplished, for instance, by realizing vertical or slightly overhanging photoresist side walls, and by directing the evaporated metal atoms normal to the substrate surface [5]. The metal layer thickness should not exceed about 2/3 of the resist thickness [6], in order to assure complete separation of the two portions of the metal layer. Hatzakis [7] has demonstrated that properly exposed and developed electron resist layers exhibit overhanging edges suitable for lift-off patterning (Fig. 3). Yu *et al.* [8] used this technique for the fabrication of an 8 kbit memory of high density. Photoresist edges might also be realized with overhanging portions, for instance, due to interference effects during exposure of the photoresist [9] or due to poor adherence of the photoresist to the substrate. However, it is not very attractive to utilize these effects for lift-off metallization because they are difficult to reproduce.

The use of auxiliary layers is another possibility to realize overhanging edges. Hu [10] used an electrolytically plated copper pattern, and Grebe *et al.* [11] have proposed a lift-off process in which overhanging edges are realized by two photoresist layers and an auxiliary metal layer between the photoresist layers. We studied another approach which is described in the following sections. The principle of this technique is similar to the process demonstrated by Browne and Perkins [12]. The technique uses the effect of an undercut auxiliary layer. There are no limitations concerning the shape of the sidewall contours of the resist, and metal atoms are allowed to impinge on the substrate surface at various angles of incidence, as is the case for instance in vacuum systems with planetary rotation of the substrates. Fine metal lines and spaces can be achieved with tapered sidewalls of the conductors, even if the metal layer thickness is on the order of 1 μm, which is the currently used thickness for integrated circuits.

Lift-Off Technique Using an Auxiliary Layer

The lift-off process which we have studied is shown schematically in Fig. 4. First, a thin auxiliary layer is deposited on the substrate. With the aid of conventional photolithography those regions which shall be free of metallization are masked with photoresist [Fig. 4(a)]. The auxiliary layer is etched [Fig. 4(b)]. Due to undercutting the photoresist bars are overhanging over the remaining portions of the auxiliary layer. The desired metallization layer is evaporated [Fig. 4(c)] by

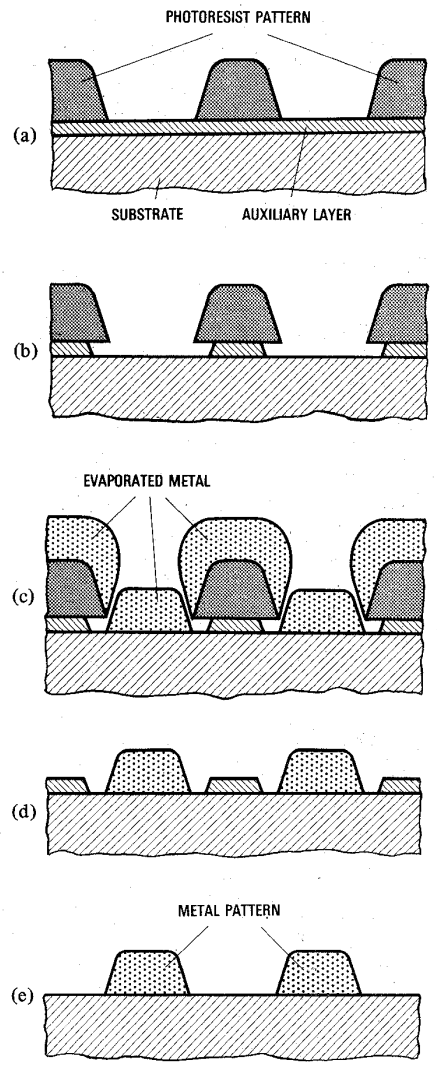


Fig. 4. Schematic illustration of the investigated lift-off process using an auxiliary layer. (a) Deposition of a thin auxiliary layer followed by photoresist patterning. (b) Etching of the free portions of the auxiliary layer. (c) Metal evaporation. (d) Metal lift-off. (e) Removal of the auxiliary layer.

moving the substrates in the vacuum chamber such that the evaporated metal atoms are impinging on the substrate surface at varying angles. The metal regions deposited on the photoresist pattern are lifted off by dissolving the photoresist in a suitable stripper [Fig. 4(d)]. It is important to note that in the undercut regions the bottom of the photoresist bars is always completely free of metal coverage even if the metal atoms arrive at angles near 90°. The stripper can thus reach the photoresist after having penetrated the microcracks. Finally, the auxiliary layer must be removed selectively [Fig. 4(e)]. The resulting metallization pattern is inverse compared to the original photoresist pattern.

Evaporation Model

As previously pointed out, the lift-off mechanism works reliably only as long as there is no continuity between the ma-

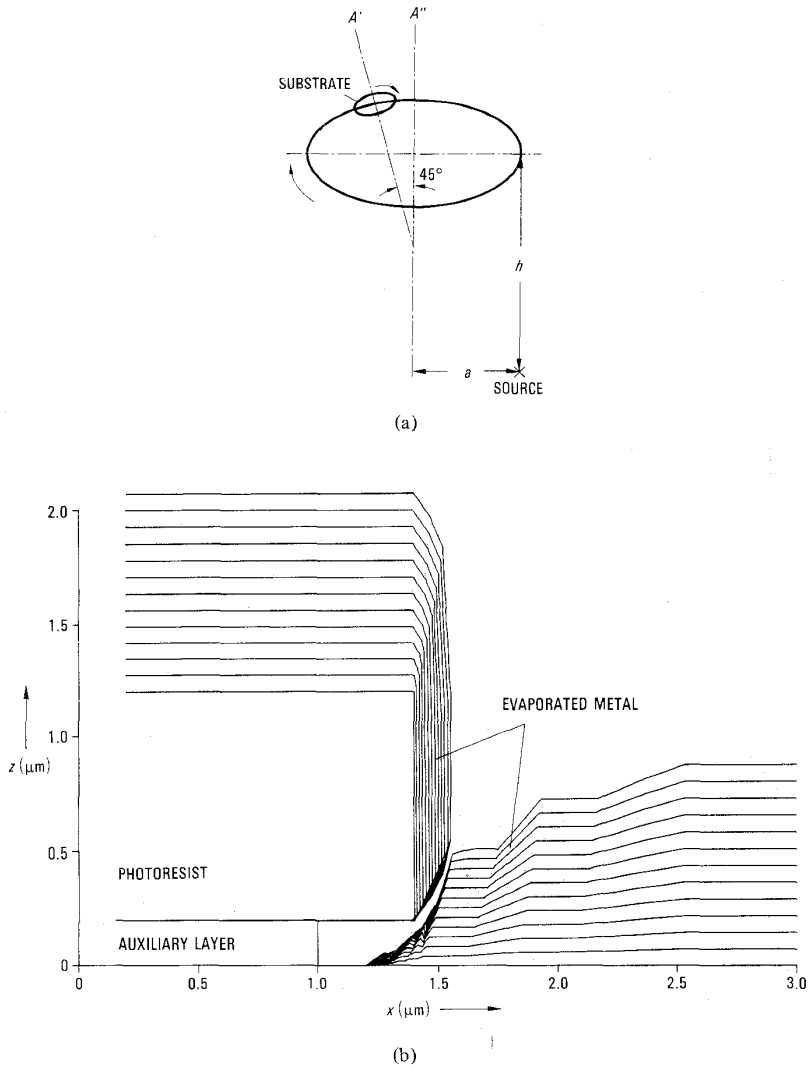
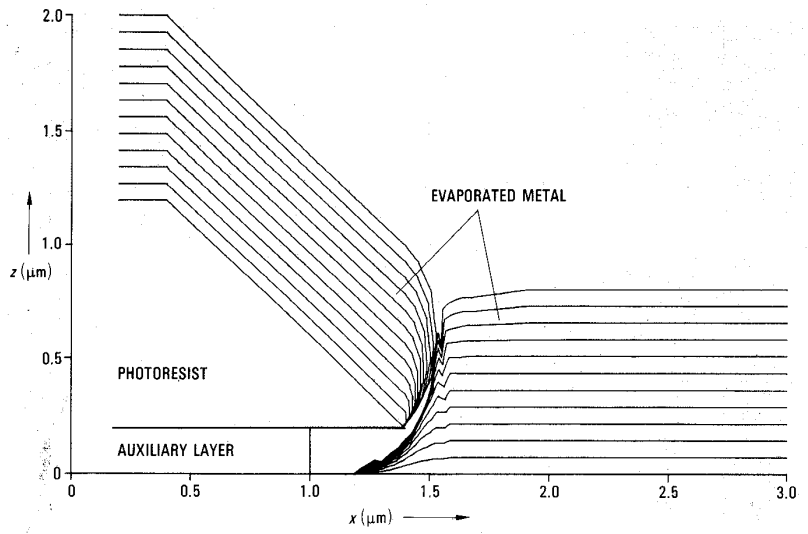


Fig. 5. Computer simulation of the metal layer buildup in the vicinity of undercut photoresist edges assuming no diffusion of the metal atoms after deposition. (a) Assumed geometry and substrate motion in the evaporation apparatus. The substrates are rotating around their own axis A' and simultaneously around the axis A''. The number of rotations during the evaporation cycle is assumed to be large. For the angular characteristic of the evaporation rate of the source, a cosine law is assumed. (b) Calculated metal configuration in the center of the substrate with the following assumptions: Auxiliary layer thickness 0.2 μm; photoresist thickness 1.0 μm; vertical photoresist sidewall; undercutting under the photoresist edge 0.4 μm; evaporated metal film thickness 0.8 μm.

terial deposited on the substrate and that deposited on top of the photoresist. In order to study the film profiles at the photoresist edges during evaporation, the metal film growth was simulated using a step-by-step construction similar to that proposed by Blech *et al.* [13]. It is assumed that the metal atoms have zero diffusivity after deposition, an assumption which is approximately valid for substrate temperatures near room temperature.

Fig. 5(b) and (c) show the calculated metal film profiles for a distinct evaporation geometry given in Fig. 5(a). Due to the assumed planetary rotation of the substrates, the angular distribution of the incident atoms in the center of the substrates is symmetrical with respect to the substrate axis. The evaporated film profiles are thus the same for any orientation of the photoresist geometries. If the substrate diameter is small compared to the substrate-to-source distance, the same is approximately valid for the photoresist geometries at the periphery of the substrate.

In Fig. 5(b) vertical photoresist sidewalls are assumed. The main result of the calculation is that a microcrack of about 200 Å in width remains between the two portions of the metal film, although the metal layer thickness is four times the auxiliary layer thickness. The maximum slope angle of the profile of the remaining metal pattern is about 70°. The position of the bottom edge of the metal film on the substrate is not exactly identical with the position of the photoresist edge. As



(c)

Fig. 5 (continued). (c) Calculation for a 45° slope angle of the photoresist sidewall.

the maximum angle of incidence of the evaporated atoms is 45°, the bottom edge of the metal film is apart from the photoresist edge by an amount which corresponds to the thickness of the auxiliary layer. It should be noted that the calculation shown in Fig. 5(b) must be modified if the width of the conductor is comparable to or smaller than the thickness of the photoresist.

Fig. 5(c) shows the calculation for a photoresist sidewall exhibiting an angle of 45° with respect to the substrate surface. In this case the metal film on the substrate is separated from that deposited on top of the photoresist only if the metal layer thickness is smaller than about twice the auxiliary layer thickness. Our calculations have shown that the photoresist sidewalls should have slope angles of more than about 60° in order to realize complete separation of the two portions of the metal film if the thickness of the metal film is four times the auxiliary layer thickness.

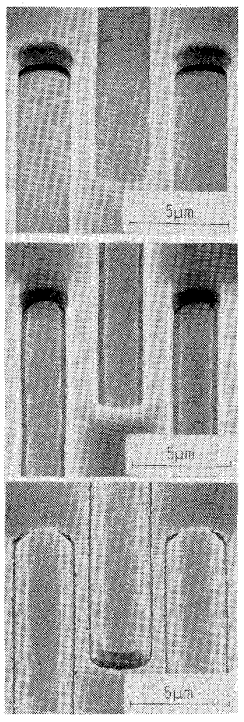
Wafer Preparation

The silicon wafers, 2 in in diameter, were prepared according to the processing sequence of the conventional n-channel metal-gate metal-oxide-semiconductor (MOS) technology. The thicknesses of the gate oxide and the field oxide are 0.06 μm and 0.6 μm, respectively. The field oxide is covered by a 0.1-μm thick phosphorus silicate glass (PSG) layer. The doping of the source and drain regions was performed either by phosphorus diffusion using a $POCl_3$ source, or by ion implantation of arsenic.

The metal interconnection pattern was defined according to the schematical illustration in Fig. 4 . A 0.2-μm thick chromium layer was evaporated as the auxiliary layer. The wafers were coated with a 1-μm thick Shipley AZ 1350 H photoresist layer. Photoresist drying was performed at 65°C for 30 min followed by alignment and exposure in a contact printing machine. After development of the resist, the chromium pattern was etched at room temperature in a cerium sulfate solution. Typically, the undercutting under the photoresist edges is 0.3 μm. After a dip etch in diluted hydrofluoric acid followed by rinsing in deionized water, a 0.8-μm thick aluminum layer containing 1.7 percent of silicon was evaporated on the wafers at room temperature using an electron beam gun as the evaporation source. During evaporation the wafers were rotated in a similar manner as that illustrated in Fig. 5(a). The only difference was that the wafer shown in Fig. 5(a) was replaced by a rotating plate loaded by five wafers. Three such rotating plates were mounted in the vacuum chamber. After metal deposition, the wafers were dipped in an ultrasonic bath containing a photoresist stripper. The remaining auxiliary chromium pattern was removed selectively by plasma etching in an oxygen ambient. Annealing was performed in forming gas at 450°-500°C for 30 min.

Experimental Results

The SEM micrographs in Fig. 6 show three intermediate stages of the lift-off process. Fig. 6(a) corresponds to the stage illustrated schematically in Fig. 4(b), i.e., after etching of the chromium pattern. The overhang of the photoresist edges is clearly visible. The sidewalls of the photoresist pattern exhibit a slope angle of about 75° with respect to the wafer surface. This indicates that in this area of the wafer there was no intimate contact between mask and wafer during exposure of the photoresist. Fig. 6(b) shows the same detail after metal evaporation, and Fig. 6(c) after the lift-off process, corresponding to Fig. 4(c) and (d), respectively. A small gap of about 0.1 μm is left between the auxiliary metal pattern and the desired Al/Si pattern. The spaces between adjacent Al/Si bars are 0.85 μm, i.e., 0.4 μm smaller than the corresponding photoresist stripes in Fig. 6(a) which are 1.25-μm wide, in accordance with the estimation in the previous section. The average slope angle of the Al/Si sidewalls is about 50°.



(a)

(b)

(c)

Fig. 6. SEM micrographs showing the same detail after three intermediate stages of the lift-off process. (a) After etching of the chromium pattern. (b) After evaporation of Al + 1.7 percent Si. (c) After the lift-off process. In the spaces between the Al/Si stripes the auxiliary chromium pattern is visible. Thicknesses: 0.2 μm Cr, 1.0 μm AZ 1350 H photoresist, 0.8 μm Al/Si.

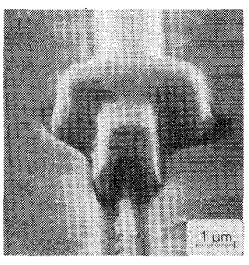


Fig. 7. SEM micrograph of a small area of a wafer surface after incomplete lift-off. A portion of the metal deposited on top of the photoresist is left on the sample while the photoresist is already removed. The discontinuities in the metal film at the bottom points of the metal bridge are clearly visible.

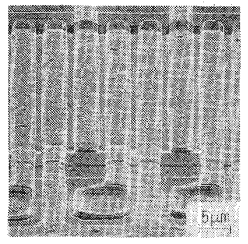


Fig. 8. SEM micrograph showing some of the electrodes of a linear CCD sensor. The average width of the gaps between the electrodes is 1 μm. The thickness of the Al/Si electrodes is 0.8 μm.

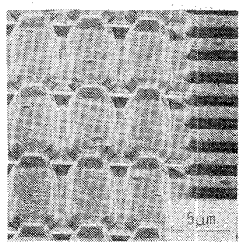


Fig. 9. SEM micrograph showing some of the electrodes of a two-dimensional CCD sensor. The gaps between the electrodes are 0.6-μm wide. The thickness of the Al/Si electrodes which are running over 0.5-μm high oxide steps is 0.8 μm.

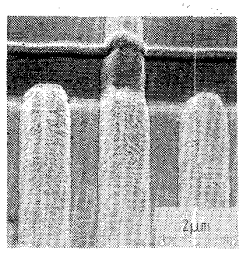


Fig. 10. SEM micrograph showing three electrodes of a linear CCD sensor. The widths of the electrodes and the spaces between the electrodes are 1.7 μm and 0.8 μm, respectively. The electrode in the center of the picture is running over a PSG step which is too steep so that the step coverage is poor. The thickness of the Al/Si electrodes is 0.8 μm.

The smooth edge contour of the Al/Si bars confirms that no continuity had existed between the remaining metal pattern and the metal film deposited on top of the photoresist. With the SEM micrograph of Fig. 7 we have tried to make the microcrack at the photoresist edges visible. The lift-off process was performed such that lift-off was incomplete so that portions of the metal deposited on top of the photoresist were remaining on the sample while the photoresist was already dissolved.

Figs. 8–10 are SEM micrographs showing details of charge-coupled devices (CCD's) whose Al/Si electrodes and interconnections were formed by the lift-off technique described. CCD sensors organized by the frame transfer principle with a total electrode length of 1.35 meters and an electrode spacing of 1.2 μm could be fabricated without defects in the metallization. It should be noted that the contours of the Al/Si sidewalls pointing to the right side of the micrographs in Figs. 8–10 are not symmetrical to those pointing to the left side. This is due to the fact that the rotation of the wafers during evaporation was not an ideal planetary rotation.

For semiconductor devices, it is very important that the metallization process has no detrimental effect on the electrical characteristics of the devices. We have performed capacitance-voltage measurements of MOS structures before and after a bias temperature treatment (10 min at 200°C and $2 \cdot 10^6$ V $\cdot$ cm^{-1}). The density of surface states and mobile charges can be kept below $5 \cdot 10^{10}$ cm^{-2}.

Conclusions

The lift-off technique described is compatible with MOS technology. Spaces of 1-μm width and even smaller between metal conductors can be fabricated with a metal film thickness of about 1 μm. The sidewalls of the conductors are smoother than those fabricated by conventional etching. Tapering of the sidewalls is achieved by evaporating the metal film such that the metal atoms are directed on the substrates at various angles of incidence. Co-evaporation from different sources as well as subsequent evaporation of different materials is possible without the need for etching the resulting multicomponent layers. The slope angle of the photoresist sidewalls is not very critical. We have successfully used contact printing and projection printing for photoresist exposure. Due to the nonnormal incidence of the metal atoms during evaporation, the linewidths of the conductors, as measured at the bottom of the conductors, are larger than the widths of the correspondent spaces of the photoresist pattern. The linewidth difference is about double the auxiliary layer thickness, i.e., about 0.4 μm. This effect is opposite to the undercutting effect inherent in chemical etching which tends to reduce the conductor linewidths.

Two important drawbacks of the lift-off technique described must be mentioned. Compared to conventional etching more process steps are required and the substrate temperature must be kept below about 100°C during evaporation. This means that the steps over which the conductors are running must not be too steep in order to obtain sufficient step coverage [13]. Also, adhesion of the metal film and electromigration resistance [14] may be reduced compared to metal films evaporated on substrates kept at 200°-400°C during evaporation.

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