

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Innoscence (Zhuhai) Technology Company, Ltd.,
and
Innoscence America, Inc.,
Petitioner,

v.

Efficient Power Conversion Corporation,
Patent Owner.

Case No. IPR2023-01382
U.S. Patent No. 9,748,347

Declaration of Shauna L. Wiest Regarding *Widmann and Uemoto*

I. Introduction

1. I have prepared this Declaration in connection with the Innoscience (Petitioner) Petition for *Inter Partes* Review of U.S. Patent No. 9,748,347 which I understand will be filed concurrently with this Declaration.

2. I am currently a senior research analyst with the Research & Information Services team at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP located at 3300 Hillview Avenue, Palo Alto, CA 94304.

3. I am over eighteen years of age, and I am competent to make this Declaration. I make this Declaration based on my own personal knowledge, and my knowledge of library science practices.

4. I earned a Master of Science in Library Science degree from the University of North Carolina at Chapel Hill in 1999, and a Bachelor of Arts in Political Science degree from the University of California at San Diego in 1989. I have worked as a law librarian for over eighteen years. I have been employed in the Research & Information Services Department at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP since 2021. Before that, from 2000-2015, I was employed as a Law Librarian at Stoel Rives LLP, and from 2015-2016, I was employed as a Competitive Intelligence Specialist for Nossaman LLP. I am also an active member of the American Association of Law Libraries.

II. Standard Library Practices for Receiving, Cataloging, and Making Materials Publicly Available

5. I have knowledge of and experience with standard library practices regarding the receipt, cataloging, shelving, and making materials, including serial publications, available to the public. I have knowledge of and experience with the Machine-Readable Cataloging (MARC) system, an industry-wide standard that libraries use to catalog materials.

6. The MARC record system was developed during the 1960s to standardize bibliographic catalog records so they could be read by computers and shared among libraries. By the mid-1970s, MARC had become the international standard for cataloging bibliographic materials and is still used today. Many libraries provide public access to their MARC records via the Internet and/or their electronic cataloging systems at the library. In a MARC record, each field provides specific information about the cataloged item, including how materials are held and when they were catalogued and made available to the public.

III. MARC Record Field Tags

7. The MARC record system uses specific three-digit numeric codes (“field tags”) from 001-999 to identify each field in a catalog record. For example, field tag 008 provides the six-digit date the item was received and catalogued (Date entered on file). The first six characters of field tag 008 are always in the

“YYMMDD” format. Descriptions for all of the character positions of field tag 008 are outlined here: <https://www.loc.gov/marc/bibliographic/bd008a.html>

8. MARC field tag 022 provides the International Standard Serial Number (ISSN), a unique identification number assigned to a serial publication. MARC field tag 260 sets forth the place of publication, name of publisher, and copyright/publication date of the publication. Finally, MARC field tags 9XX provide local holdings information to assist the public in identifying the location of the desired resource.

9. Based on standard library practice, when a library receives an item, it stamps (and/or labels) the item with the library name, barcode, often with a date that is within a few days or weeks of receipt. Next, the library will catalog the item within a matter of a few days or weeks of receiving it.

10. Generally, after an item is cataloged, the public may access the item by searching the library catalog, browsing the library shelves, and either requesting or electronically accessing the item from the library. Standard library practice is to make the item available to the public within a few days or weeks of cataloging it.

IV. Serial Publications

11. A serial publication, often known as a “journal” or “periodical,” is a resource that is issued in successive parts and has no predetermined conclusion. These successive parts are commonly referred to as “issues,” and each issue is

usually chronologically numbered and dated. The presence of enumeration, years of coverage, frequency, and/or other chronological information also indicates a serial publication.

12. There are significant differences between cataloging finite resources (books/monographs) and continuing resources (serials). For serials, the catalog record provides information about the serial as a whole, including the first or earliest available issue. It also provides information as to holdings – the volumes and issues, with dates, received by the library and made available to the public. In serials cataloging, there are identifying characteristics unique to serials that are slightly different from monographs (books). The issue date for a print serial publication, for example, generally appears on the cover (front or back), the masthead page, the title page (if any), the table of contents page(s), or on the pages of the individual articles contained in the issue. More information regarding the unique aspects of cataloguing serials can be found at this link:

<https://www.loc.gov/aba/pcc/conser/scctppt/Basic-2014/Basic-Trainee-Mannual.pdf>

V. Public Availability of *Widmann* (EX 1023)

13. Section five of this Declaration relates to the date of public availability for the following reference: D. W. Widmann, "*Metallization for integrated circuits using a lift-off technique*," in IEEE Journal of Solid-State

Circuits, vol. SC-11, no. 4, pp. 466-471, August 1976. (“*Widmann*”). I understand that *Widmann* has been submitted as **Exhibit 1023** in this proceeding.

14. As detailed below, I have reviewed the print reference, public holdings information, and Library of Congress MARC record for *Widmann* to determine the date of public availability for this reference.

15. **Appendix A** to this declaration is a true and accurate copy of the print journal cover (including volume binding), title page, table of contents, call number, and Library of Congress Date Stamp for the print issue of IEEE Journal of Solid-State Circuits containing *Widmann* held by the Library of Congress. The date stamp on this issue indicates that *Widmann* was received by the Library of Congress on September 17, 1976.

16. **Appendix B** to this declaration is a true and correct copy of the public catalog record for IEEE Journal of Solid-State Circuits containing *Widmann* held by the Library of Congress, which was downloaded from <https://lccn.loc.gov/89657065> on August 31, 2023. The Library of Congress’s public catalog record for its copy of IEEE Journal of Solid-State Circuits containing *Widmann* sets forth the publication history and item availability including holdings, call number, and onsite location information for members of the public seeking the print issue of IEEE Journal of Solid-State Circuits containing *Widmann*. The public catalog record (**Appendix B**) indicates that the

print issue of IEEE Journal of Solid-State Circuits containing *Widmann* should be requested in the Newspaper & Current Periodical Reading Room (Madison LM133) within holdings v.1:no.1-v.40:no.6 (1966:Sept.-2005:June) at Call Number TK7871.85 .I23.

17. **Appendix C** to this declaration is a true and accurate copy of the Library of Congress MARC record for its holdings of the serial publication IEEE Journal of Solid-State Circuits containing *Widmann*, which was downloaded from <https://catalog.loc.gov/vwebv/staffView?searchId=22826&recPointer=0&recCount=25&bibId=11362790> on August 31, 2023.

18. The Library of Congress MARC record (**Appendix C**) for the serial publication IEEE Journal of Solid-State Circuits confirms the fixed data elements of MARC field tag 008 as 750901c19669999nyumrp0a0engc. As discussed above, the first six characters “750901” are in typical “**YYMMDD**” format and indicate that the serial publication IEEE Journal of Solid-State Circuits was initially catalogued by the Library of Congress on September 1, 1975. The publication status code “c1966” refers to “continuing resource currently published” indicating that the serial publication IEEE Journal of Solid-State Circuits began publication in 1966 and is a continuing resource currently published.

19. MARC record field tag 022 (**Appendix C**) denotes the unique International Standard Serial Number (ISSN) for IEEE Journal of Solid-State

Circuits as 0018-9200. MARC Field tag 260 sets forth the place of publication, publisher, and copyright date as: |a New York, N.Y. : |b Institute of Electrical and Electronics Engineers, |c ©1966-

20. Finally, MARC record field tags 991 set forth the local holdings, location, and call number information for the serial publication IEEE Journal of Solid-State Circuits containing *Widmann*. The MARC record (**Appendix C**) sets forth that the serial publication IEEE Journal of Solid-State Circuits containing *Widmann* is held in the Library of Congress General Collection or in the Newspaper & Current Periodical Reading Room (Madison LM133) at Call Number TK7871.85 .I23 beginning with the issue v 1-2:Sept-Dec * 1966.

21. Based on the information in **Appendices A, B and C** it is clear that the issue of Solid-State Circuits containing *Widmann* was received by the Library of Congress on September 17, 1976. Based on standard library practices, *Widmann* would have been processed and catalogued by the Library of Congress within a matter of a few days or weeks of September 17, 1976.

22. Accordingly, *Widmann* would have been made available to the public within a few days or weeks of being checked-in and catalogued. The public could have accessed *Widmann* by searching the Library of Congress catalog, requesting the item from a library staff member, or by visiting the Newspaper & Current

Periodical Reading Room (Madison LM133) within a few weeks of September 17, 1976.

VI. Public Availability of *Uemoto* (EX 1020)

23. Section six of this Declaration relates to the date of public availability for the following reference: Y. Uemoto et al., "*A Normally-off AlGaIn/GaN Transistor with $R_{onA}=2.6m\Omega cm^2$ and $BV_{ds}=640V$ Using Conductivity Modulation*," 2006 International Electron Devices Meeting, December 11-13, 2006, San Francisco, CA, Volume 2, pp. 654-657. ("*Uemoto*"). I understand that *Uemoto* has been submitted as **Exhibit 1020** in this proceeding.

24. As detailed below, I have reviewed the print reference, public holdings information, and Library of Congress MARC record for *Uemoto* to determine the date of public availability for this reference.

25. **Appendix D** to this declaration is a true and accurate copy of the print journal cover (including volume binding), title page, table of contents, call number, and barcode for the print volume of the 2006 International Electron Devices Meeting containing *Uemoto* received and held by the Library of Congress. The call number on the binding spine and title page indicates that *Uemoto* is publicly held at the Library of Congress at TK 7801 .I53 2006 Vol. 2 Set 1.

26. **Appendix E** to this declaration is a true and correct copy of the public catalog record for the print volume of the 2006 International Electron

Devices Meeting containing *Uemoto* held by the Library of Congress, which was downloaded from <https://lccn.loc.gov/81642284> on September 1, 2023. The Library of Congress’s public catalog record for its copy of the 2006 International Electron Devices Meeting containing *Uemoto* sets forth the publication history, description, and item availability including holdings, call number, and onsite location information for members of the public seeking the print volume of the 2006 International Electron Devices Meeting containing *Uemoto*. The public catalog record (**Appendix E**) indicates that the Library of Congress maintains holdings for the International Electron Devices Meeting for 1973-1975, 1977-2000, 2002-2003, 2005-2006 (both 2006 volumes), 2009-2010 and 2012. The public catalog record (**Appendix E**) also shows that the print volume of the 2006 International Electron Devices Meeting containing *Uemoto* should be requested in the Jefferson or Adams Building Reading Rooms within holdings 2006, v. 2 at Call Number TK7801 .I53.

27. **Appendix F** to this declaration is a true and accurate copy of the Library of Congress MARC record for its holdings of the serial publication “International Electron Devices Meeting” containing *Uemoto*, which was downloaded from <https://catalog.loc.gov/vwebv/staffView?searchId=20290&recPointer=0&recCount=25&bibId=11248470> on September 1, 2023.

28. The Library of Congress MARC record (**Appendix F**) for the serial publication “International Electron Devices Meeting” confirms the fixed data elements of MARC field tag 008 as 780413c19739999nyuar1a0eng. As discussed above, the first six characters “780413” are in typical “YYMMDD” format and indicate that the serial publication “International Electron Devices Meeting” was first catalogued by the Library of Congress on April 13, 1978. The publication status code “c1973” refers to “continuing resource currently published” showing that the serial publication “International Electron Devices Meeting” began publication in 1973 and is a continuing resource currently published.

29. MARC record field tag 022 (**Appendix F**) denotes the unique International Standard Serial Number (ISSN) for International Electron Devices Meeting as 0163-1918. MARC Field tag 260 sets forth the place of publication, publisher, and copyright date as: |a New York, N.Y. : |b Institute of Electrical and Electronics Engineers, |c 1973-

30. Finally, MARC record field tags 9XX set forth the holdings policies, location, and call number information for the serial publication “International Electron Devices Meeting” containing *Uemoto*. The MARC record (**Appendix F**) states that one copy of all issues received for International Electron Devices Meeting are to be kept permanently. **Appendix F** also sets forth the public holdings for “International Electron Devices Meeting” as held in the Library of

Congress General Collection in the Jefferson or Adams Building Reading Rooms at Call Number TK7801 .I53 beginning with receipts beginning in 1973.

31. Based on the information in **Appendices D, E and F** it is clear that the volume of “International Electron Devices Meeting” containing *Uemoto* would have been received by the Library of Congress during December 2006. Based on standard library practices, *Uemoto* would have been processed and catalogued by the Library of Congress within a matter of a few days or weeks of December 2006.

32. Accordingly, *Uemoto* would have been made available to the public within a few days or weeks of being checked-in and catalogued. The public could have accessed *Uemoto* by searching the Library of Congress catalog and/or requesting the item from a library staff member, or by visiting the Library of Congress Jefferson or Adams Building Reading Rooms during January 2007.

VII. Conclusion

33. In signing this Declaration, I understand it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I understand I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

34. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on September 5, 2023.

Shauna L. Wiest

Shauna L. Wiest

APPENDIX A

IEEE
JOURNAL OF
SOLID-STATE
CIRCUITS

11

1976

TK 7871

.85

.123

SOLID-STATE
CIRCUITS

100407

AUGUST 1976

VOLUME SC-11

NUMBER 4

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS COUNCIL

SPECIAL ISSUE ON TECHNOLOGY AND PROCESSING FOR INTEGRATED CIRCUITS

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The following are upcoming Special Issues of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. Prospective authors should contact the appropriate Guest Editor or the Editor of the JOURNAL for details. In general, the deadline for submission of manuscripts is six to seven months in advance of the publication date.

October 1976

Semiconductor Memory and Logic

B. T. Murphy, *Guest Editor for Logic*
Bell Labs.
600 Mountain Ave.
Murray Hill, NJ 07974

L. L. Vadasz, *Guest Editor for Memory*
Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051

December 1976

Linear and Analog Circuits

G. L. Baldwin, *Co-Guest Editor*
Bell Labs.
Room 4D-625
Holmdel, NJ 07733

R. G. Meyer, *Co-Guest Editor*
Elec. Eng. and Comput. Sci., Cory Hall
Univ. of California
Berkeley, CA 94720

April 1977

Integrated Injection Logic (I²L/MTL)

C. G. Thornton, *Co-Guest Editor*
U.S. Army Electronics Command
Fort Monmouth, NJ 07703

N. C. de Troye, *Co-Guest Editor*
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Eindhoven, The Netherlands



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AUGUST 1976

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Metallization for Integrated Circuits Using a Lift-Off Technique

DIETRICH W. WIDMANN

Abstract—A special lift-off technique for realizing small metal interconnection geometries for integrated circuits is described. $0.6\text{-}\mu\text{m}$ gaps between metal conductors can be obtained even at $0.8\text{-}\mu\text{m}$ metal layer thickness. The slopes of the conductors are tapered. Etching problems inherent in alloy films or sandwiched layers such as Al/Si or Al/Cu/Si are avoided by the technique proposed. SEM micrographs of Al/Si conductor patterns are presented.

INTRODUCTION

THE increasing packing density of integrated circuits requires small conductor linewidths and small spaces between conductors.

The interconnection pattern can be formed by conventional chemical etching techniques. However, chemical etching has several drawbacks. First, after delineation of alloy films such as Al/Si or Al/Si/Cu, silicon residues may remain in the field between the conductors [1]. Second, the cross section of the conductors may be considerably reduced by etchant penetration at steep oxide steps [1]. Third, due to the lateral etch attack, the widths of the conductors are reduced, and the spaces between adjacent conductors are increased (Fig. 1). The undercutting Δx per edge (see Fig. 1) might be in the order of the conductor thickness. As long as the desired spacing between adjacent conductors is large enough, i.e., larger than about $3\text{ }\mu\text{m}$ for $1\text{-}\mu\text{m}$ conductor thickness and $1\text{-}\mu\text{m}$ minimum photoresist dimension, the undercutting effect can be compensated by proper dimensioning the corresponding geometries on the photomask. However, if spaces of about $1\text{ }\mu\text{m}$ are required between $1\text{-}\mu\text{m}$ thick metal conductors, the compensation procedure fails.

The edge contours of conductors delineated by wet chemical etching are nearly conical [2], the upper portion of the edges being steep or even overhanging. Edge contours of this kind may lead to poor coverage of such edges by subsequently deposited layers such as passivation and metal layers.

Alternative methods which might be used instead of chemical etching are sputter or ion beam etching, plasma etching, selective plating, selective anodization, and lift-off techniques. This paper reports on results obtained with a lift-off technique, which is suitable for the metallization of integrated circuits with high packing density.

LIFT-OFF TECHNIQUES

The lift-off technique for metal pattern formation is shown schematically in Fig. 2. This technique has been known for

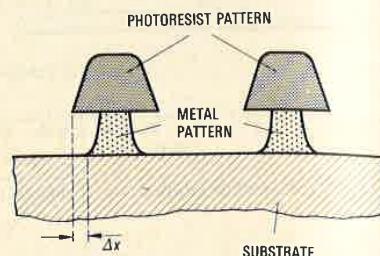


Fig. 1. Schematic illustration of a typical cross section of metal conductors after chemical etching. The undercutting at the bottom of the conductors is Δx .

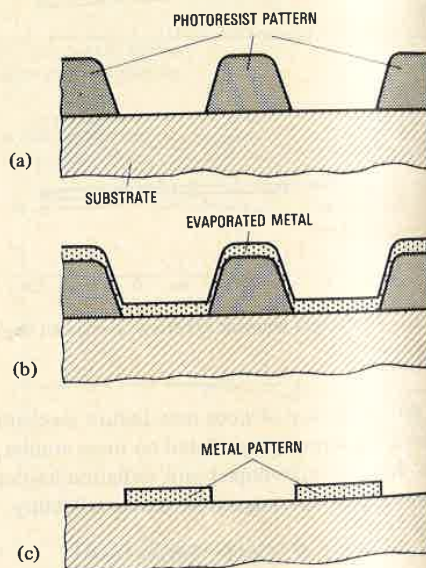


Fig. 2. Schematic illustration of metal pattern definition using the original lift-off technique. (a) Photoresist pattern definition. (b) Metal evaporation. (c) Photoresist stripping, thereby lifting off the overlying metal. The spaces between the metal features are equal to the corresponding photoresist linewidths, as measured at the bottom of the photoresist bars.

many years. For instance, it was used in 1966 by Stelter [3] for the fabrication of chromium masks.

The process in Fig. 2 looks very simple. However, there are severe limitations concerning the thickness and the brittleness of the metal layer. The lifting mechanism works reliably only if the metal thickness at the bottom of the photoresist bars is thin enough, i.e., some $100\text{ }\text{\AA}$, and if the metal is brittle so that it cracks readily at the photoresist edges [4]. For ductile

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The author is with the Research Laboratories, Siemens AG, Munich, Germany.

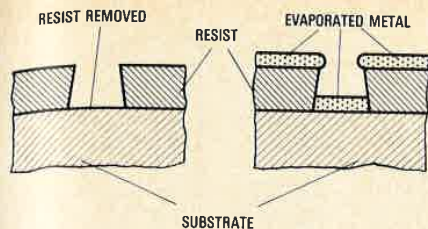


Fig. 3. Metal patterning by a lift-off technique using slightly overhanging sidewalls of electron resist (after Hatzakis [7]).

metals, such as aluminum, the metal layer deposited on the photoresist should be completely separated from the other portions of the metal layer deposited on the substrate. This could be accomplished, for instance, by realizing vertical or slightly overhanging photoresist side walls, and by directing the evaporated metal atoms normal to the substrate surface [5]. The metal layer thickness should not exceed about 2/3 of the resist thickness [6], in order to assure complete separation of the two portions of the metal layer. Hatzakis [7] has demonstrated that properly exposed and developed electron resist layers exhibit overhanging edges suitable for lift-off patterning (Fig. 3). Yu *et al.* [8] used this technique for the fabrication of an 8 kbit memory of high density. Photoresist edges might also be realized with overhanging portions, for instance, due to interference effects during exposure of the photoresist [9] or due to poor adherence of the photoresist to the substrate. However, it is not very attractive to utilize these effects for lift-off metallization because they are difficult to reproduce.

The use of auxiliary layers is another possibility to realize overhanging edges. Hu [10] used an electrolytically plated copper pattern, and Grebe *et al.* [11] have proposed a lift-off process in which overhanging edges are realized by two photoresist layers and an auxiliary metal layer between the photoresist layers. We studied another approach which is described in the following sections. The principle of this technique is similar to the process demonstrated by Browne and Perkins [12]. The technique uses the effect of an undercut auxiliary layer. There are no limitations concerning the shape of the sidewall contours of the resist, and metal atoms are allowed to impinge on the substrate surface at various angles of incidence, as is the case for instance in vacuum systems with planetary rotation of the substrates. Fine metal lines and spaces can be achieved with tapered sidewalls of the conductors, even if the metal layer thickness is on the order of 1 μm , which is the currently used thickness for integrated circuits.

LIFT-OFF TECHNIQUE USING AN AUXILIARY LAYER

The lift-off process which we have studied is shown schematically in Fig. 4. First, a thin auxiliary layer is deposited on the substrate. With the aid of conventional photolithography those regions which shall be free of metallization are masked with photoresist [Fig. 4(a)]. The auxiliary layer is etched [Fig. 4(b)]. Due to undercutting the photoresist bars are overhanging over the remaining portions of the auxiliary layer. The desired metallization layer is evaporated [Fig. 4(c)] by

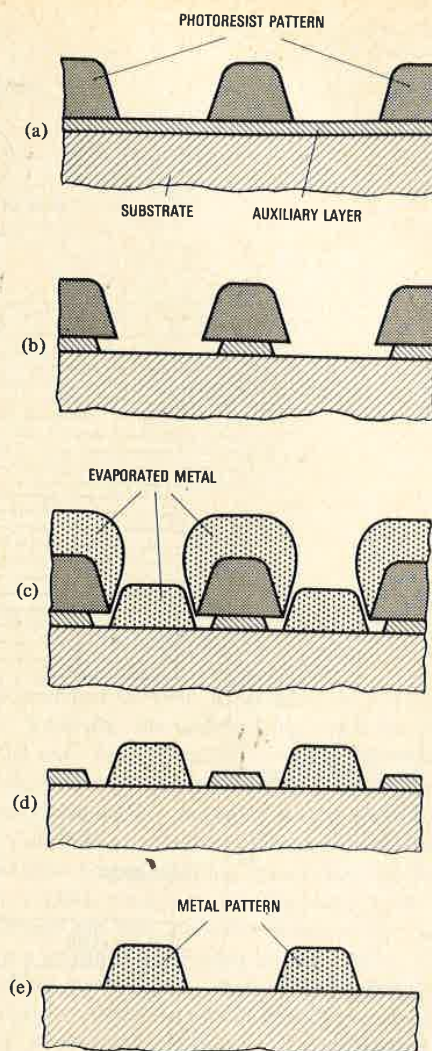


Fig. 4. Schematic illustration of the investigated lift-off process using an auxiliary layer. (a) Deposition of a thin auxiliary layer followed by photoresist patterning. (b) Etching of the free portions of the auxiliary layer. (c) Metal evaporation. (d) Metal lift-off. (e) Removal of the auxiliary layer.

moving the substrates in the vacuum chamber such that the evaporated metal atoms are impinging on the substrate surface at varying angles. The metal regions deposited on the photoresist pattern are lifted off by dissolving the photoresist in a suitable stripper [Fig. 4(d)]. It is important to note that in the undercut regions the bottom of the photoresist bars is always completely free of metal coverage even if the metal atoms arrive at angles near 90° . The stripper can thus reach the photoresist after having penetrated the microcracks. Finally, the auxiliary layer must be removed selectively [Fig. 4(e)]. The resulting metallization pattern is inverse compared to the original photoresist pattern.

EVAPORATION MODEL

As previously pointed out, the lift-off mechanism works reliably only as long as there is no continuity between the ma-

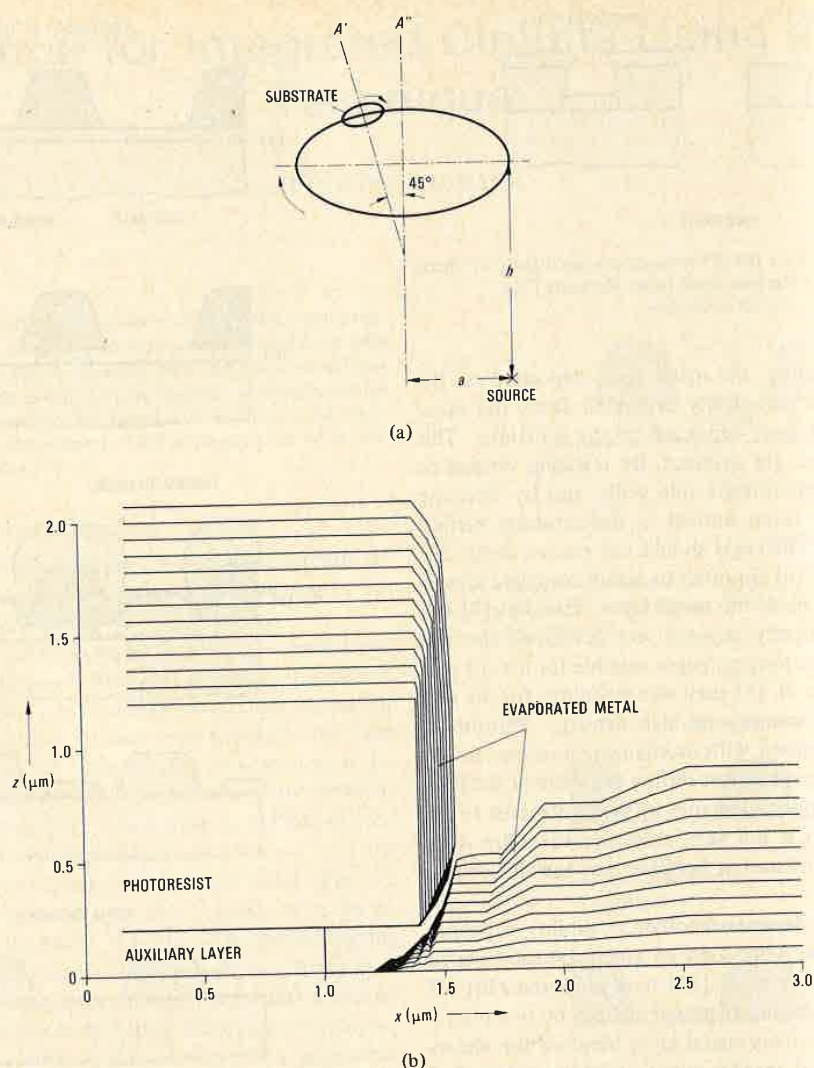


Fig. 5. Computer simulation of the metal layer buildup in the vicinity of undercut photoresist edges assuming no diffusion of the metal atoms after deposition. (a) Assumed geometry and substrate motion in the evaporation apparatus. The substrates are rotating around their own axis A' and simultaneously around the axis A'' . The number of rotations during the evaporation cycle is assumed to be large. For the angular characteristic of the evaporation rate of the source, a cosine law is assumed. (b) Calculated metal configuration in the center of the substrate with the following assumptions: Auxiliary layer thickness $0.2 \mu\text{m}$; photoresist thickness $1.0 \mu\text{m}$; vertical photoresist sidewall; undercutting under the photoresist edge $0.4 \mu\text{m}$; evaporated metal film thickness $0.8 \mu\text{m}$.

terial deposited on the substrate and that deposited on top of the photoresist. In order to study the film profiles at the photoresist edges during evaporation, the metal film growth was simulated using a step-by-step construction similar to that proposed by Blech *et al.* [13]. It is assumed that the metal atoms have zero diffusivity after deposition, an assumption which is approximately valid for substrate temperatures near room temperature.

Fig. 5(b) and (c) show the calculated metal film profiles for a distinct evaporation geometry given in Fig. 5(a). Due to the assumed planetary rotation of the substrates, the angular distribution of the incident atoms in the center of the substrates is symmetrical with respect to the substrate axis. The evap-

orated film profiles are thus the same for any orientation of the photoresist geometries. If the substrate diameter is small compared to the substrate-to-source distance, the same is approximately valid for the photoresist geometries at the periphery of the substrate.

In Fig. 5(b) vertical photoresist sidewalls are assumed. The main result of the calculation is that a microcrack of about $200 \text{ \AA}$ in width remains between the two portions of the metal film, although the metal layer thickness is four times the auxiliary layer thickness. The maximum slope angle of the profile of the remaining metal pattern is about 70° . The position of the bottom edge of the metal film on the substrate is not exactly identical with the position of the photoresist edge. As

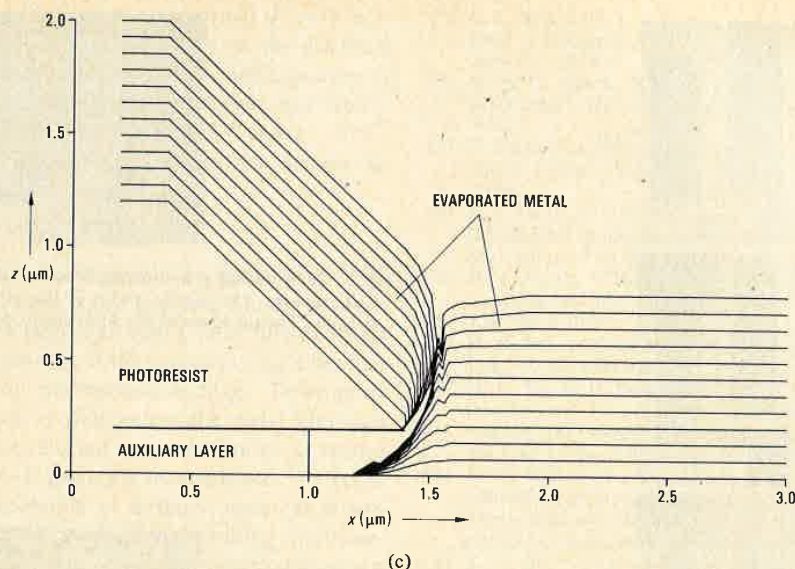


Fig. 5 (continued). (c) Calculation for a 45° slope angle of the photoresist sidewall.

the maximum angle of incidence of the evaporated atoms is 45°, the bottom edge of the metal film is apart from the photoresist edge by an amount which corresponds to the thickness of the auxiliary layer. It should be noted that the calculation shown in Fig. 5(b) must be modified if the width of the conductor is comparable to or smaller than the thickness of the photoresist.

Fig. 5(c) shows the calculation for a photoresist sidewall exhibiting an angle of 45° with respect to the substrate surface. In this case the metal film on the substrate is separated from that deposited on top of the photoresist only if the metal layer thickness is smaller than about twice the auxiliary layer thickness. Our calculations have shown that the photoresist sidewalls should have slope angles of more than about 60° in order to realize complete separation of the two portions of the metal film if the thickness of the metal film is four times the auxiliary layer thickness.

WAFER PREPARATION

The silicon wafers, 2 in in diameter, were prepared according to the processing sequence of the conventional n-channel metal-gate metal-oxide-semiconductor (MOS) technology. The thicknesses of the gate oxide and the field oxide are 0.06 μm and 0.6 μm, respectively. The field oxide is covered by a 0.1-μm thick phosphorus silicate glass (PSG) layer. The doping of the source and drain regions was performed either by phosphorus diffusion using a POCl_3 source, or by ion implantation of arsenic.

The metal interconnection pattern was defined according to the schematical illustration in Fig. 4. A 0.2-μm thick chromium layer was evaporated as the auxiliary layer. The wafers were coated with a 1-μm thick Shipley AZ 1350 H photoresist layer. Photoresist drying was performed at 65°C for 30 min followed by alignment and exposure in a contact printing machine. After development of the resist, the chromium

pattern was etched at room temperature in a cerium sulfate solution. Typically, the undercutting under the photoresist edges is 0.3 μm. After a dip etch in diluted hydrofluoric acid followed by rinsing in deionized water, a 0.8-μm thick aluminum layer containing 1.7 percent of silicon was evaporated on the wafers at room temperature using an electron beam gun as the evaporation source. During evaporation the wafers were rotated in a similar manner as that illustrated in Fig. 5(a). The only difference was that the wafer shown in Fig. 5(a) was replaced by a rotating plate loaded by five wafers. Three such rotating plates were mounted in the vacuum chamber. After metal deposition, the wafers were dipped in an ultrasonic bath containing a photoresist stripper. The remaining auxiliary chromium pattern was removed selectively by plasma etching in an oxygen ambient. Annealing was performed in forming gas at 450°–500°C for 30 min.

EXPERIMENTAL RESULTS

The SEM micrographs in Fig. 6 show three intermediate stages of the lift-off process. Fig. 6(a) corresponds to the stage illustrated schematically in Fig. 4(b), i.e., after etching of the chromium pattern. The overhang of the photoresist edges is clearly visible. The sidewalls of the photoresist pattern exhibit a slope angle of about 75° with respect to the wafer surface. This indicates that in this area of the wafer there was no intimate contact between mask and wafer during exposure of the photoresist. Fig. 6(b) shows the same detail after metal evaporation, and Fig. 6(c) after the lift-off process, corresponding to Fig. 4(c) and (d), respectively. A small gap of about 0.1 μm is left between the auxiliary metal pattern and the desired Al/Si pattern. The spaces between adjacent Al/Si bars are 0.85 μm, i.e., 0.4 μm smaller than the corresponding photoresist stripes in Fig. 6(a) which are 1.25-μm wide, in accordance with the estimation in the previous section. The average slope angle of the Al/Si sidewalls is about 50°.

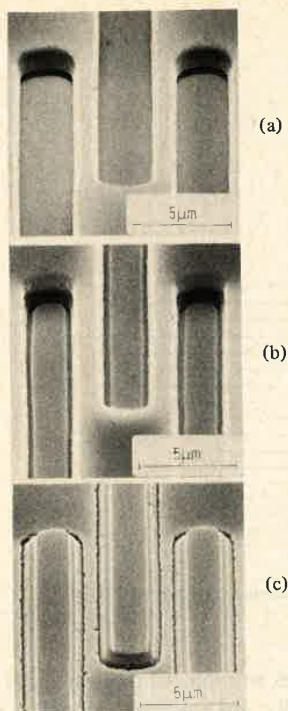


Fig. 6. SEM micrographs showing the same detail after three intermediate stages of the lift-off process. (a) After etching of the chromium pattern. (b) After evaporation of Al + 1.7 percent Si. (c) After the lift-off process. In the spaces between the Al/Si stripes the auxiliary chromium pattern is visible. Thicknesses: $0.2\text{ }\mu\text{m}$ Cr, $1.0\text{ }\mu\text{m}$ AZ 1350 H photoresist, $0.8\text{ }\mu\text{m}$ Al/Si.

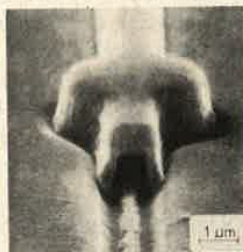


Fig. 7. SEM micrograph of a small area of a wafer surface after incomplete lift-off. A portion of the metal deposited on top of the photoresist is left on the sample while the photoresist is already removed. The discontinuities in the metal film at the bottom points of the metal bridge are clearly visible.

The smooth edge contour of the Al/Si bars confirms that no continuity had existed between the remaining metal pattern and the metal film deposited on top of the photoresist. With the SEM micrograph of Fig. 7 we have tried to make the microcrack at the photoresist edges visible. The lift-off process was performed such that lift-off was incomplete so that portions of the metal deposited on top of the photoresist were remaining on the sample while the photoresist was already dissolved.

Figs. 8-10 are SEM micrographs showing details of charge-



Fig. 8. SEM micrograph showing some of the electrodes of a linear CCD sensor. The average width of the gaps between the electrodes is $1\text{ }\mu\text{m}$. The thickness of the Al/Si electrodes is $0.8\text{ }\mu\text{m}$.

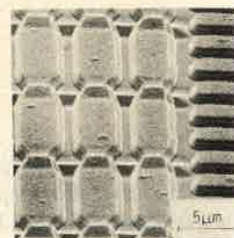


Fig. 9. SEM micrograph showing some of the electrodes of a two-dimensional CCD sensor. The gaps between the electrodes are $0.6\text{-}\mu\text{m}$ wide. The thickness of the Al/Si electrodes which are running over $0.5\text{-}\mu\text{m}$ high oxide steps is $0.8\text{ }\mu\text{m}$.

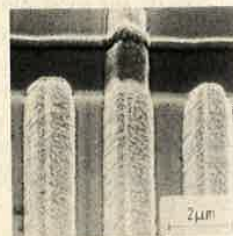


Fig. 10. SEM micrograph showing three electrodes of a linear CCD sensor. The widths of the electrodes and the spaces between the electrodes are $1.7\text{ }\mu\text{m}$ and $0.8\text{ }\mu\text{m}$, respectively. The electrode in the center of the picture is running over a PSG step which is too steep so that the step coverage is poor. The thickness of the Al/Si electrodes is $0.8\text{ }\mu\text{m}$.

coupled devices (CCD's) whose Al/Si electrodes and interconnections were formed by the lift-off technique described. CCD sensors organized by the frame transfer principle with a total electrode length of 1.35 meters and an electrode spacing of $1.2\text{ }\mu\text{m}$ could be fabricated without defects in the metallization. It should be noted that the contours of the Al/Si sidewalls pointing to the right side of the micrographs in Figs. 8-10 are not symmetrical to those pointing to the left side. This is due to the fact that the rotation of the wafers during evaporation was not an ideal planetary rotation.

For semiconductor devices, it is very important that the metallization process has no detrimental effect on the electrical characteristics of the devices. We have performed capacitance-voltage measurements of MOS structures before and after a bias temperature treatment (10 min at 200°C and $2 \cdot 10^6 \text{ V} \cdot \text{cm}^{-1}$). The density of surface states and mobile charges can be kept below $5 \cdot 10^{10} \text{ cm}^{-2}$.

CONCLUSIONS

The lift-off technique described is compatible with MOS technology. Spaces of 1- μm width and even smaller between metal conductors can be fabricated with a metal film thickness of about 1 μm . The sidewalls of the conductors are smoother than those fabricated by conventional etching. Tapering of the sidewalls is achieved by evaporating the metal film such that the metal atoms are directed on the substrates at various angles of incidence. Co-evaporation from different sources as well as subsequent evaporation of different materials is possible without the need for etching the resulting multicomponent layers. The slope angle of the photoresist sidewalls is not very critical. We have successfully used contact printing and projection printing for photoresist exposure. Due to the nonnormal incidence of the metal atoms during evaporation, the linewidths of the conductors, as measured at the bottom of the conductors, are larger than the widths of the correspondent spaces of the photoresist pattern. The linewidth difference is about double the auxiliary layer thickness, i.e., about 0.4 μm . This effect is opposite to the undercutting effect inherent in chemical etching which tends to reduce the conductor linewidths.

Two important drawbacks of the lift-off technique described must be mentioned. Compared to conventional etching more process steps are required and the substrate temperature must be kept below about 100°C during evaporation. This means that the steps over which the conductors are running must not be too steep in order to obtain sufficient step coverage [13]. Also, adhesion of the metal film and electromigration resistance [14] may be reduced compared to metal films evaporated on substrates kept at 200°–400°C during evaporation.

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Dietrich W. Widmann received the Dipl. Phys. and Dr. Ing. degrees from the Technical University of Stuttgart, Stuttgart, Germany, in 1962 and 1965, respectively.

In 1965 he joined the Siemens AG, Munich, Germany, where he has been engaged in development of bipolar integrated circuit technology. Since 1971 he has been working on the technology of LSI MOS integrated circuits. His research activities are in the areas of photolithography, metallization, and passivation for

integrated circuits with micron and submicron features. Dr. Widmann is a member of the German Physical Society.

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A Normally-off AlGaN/GaN Transistor with $R_{on}A=2.6m\Omega cm^2$ and $BV_{ds}=640V$ Using Conductivity Modulation

Yasuhiro Uemoto, Masahiro Hikita, Hiroaki Ueno, Hisayoshi Matsuo, Hidetoshi Ishida,
Manabu Yanagihara, Tetsuzo Ueda, Tsuyoshi Tanaka and Daisuke Ueda

Semiconductor Device Research Center, Semiconductor Company, Matsushita Electric - Panasonic
1 Kotari-yakemachi, Nagaokakyo-shi, Kyoto 617-8520, JAPAN
Phone: +81-75-956-9083, FAX: +81-75-956-9110, e-mail: uemoto.yasuhiro@jp.panasonic.com

Abstract

We report a normally-off GaN-based transistor using conductivity modulation, which we call GIT (Gate Injection Transistor). This new device principle utilizes hole-injection from p-AlGaN to AlGaN/GaN heterojunction, which increases electron density in the depleted channel resulting in dramatic increase of the drain current owing to the conductivity modulation. The fabricated GIT exhibits the threshold voltage of 1.0V with high maximum drain current of 200mA/mm. The obtained on-state resistance ($R_{on}A$) and off-state breakdown voltage (BV_{ds}) are $2.6m\Omega \cdot cm^2$ and 640V, respectively. These values are the best ones ever reported for GaN-based normally-off transistors.

Introduction

AlGaN/GaN heterojunction field effect transistors (HFETs) are widely investigated for high power switching applications. Most of the reported AlGaN/GaN HFETs are normally-on type taking advantage of the inherent high sheet carrier density caused by built-in polarization electric field [1-2]. Aiming at practical applications, normally-off operation is strongly desired for AlGaN/GaN HFETs in order to make the GaN devices compatible with currently used Si-based power MOSFETs / IGBTs for safety operation. Since the interfacial carriers are caused by the difference of the inherent fixed charges between GaN and AlGaN, reduction of the Al mole fraction and the thickness of AlGaN is effective to reduce those carriers and thereby to shift the threshold voltage. This approach results in reduced drain current as well as lower potential barrier to the gate. So far, high enough drain current with normally-off operation for AlGaN/GaN HFETs has never been reported [3-10].

In this paper, we demonstrate a new concept of GaN-based normally-off transistor called GIT (Gate Injection Transistor). The GIT utilizes hole injection from p-type gate to 2DEG region bringing out the conductivity modulation as is observed in IGBTs[11]. This new concept realizes high current driving capability even with normally-off operation.

Principle of GIT operation

The most notable feature of the GIT is p-AlGaN gate formed over undoped AlGaN/GaN hetero-structure as shown in Fig.1(a). The p-AlGaN lifts up the potential at the channel, which ends up with normally-off operation as shown in the band diagram of Fig.1(b). Fig.2 illustrates the basic operation of the GIT. At the gate voltages up to the forward built-in voltage V_f of the pn junction at the gate, the GIT is operated as a field effect transistor. Further increase of the gate voltage exceeding the V_f results in the hole injection to the channel from the p-AlGaN. The injection of the electrons from the channel to the gate is well suppressed by the hetero-barrier at AlGaN/GaN. The injected holes generate the equal numbers of electrons to keep charge neutrality at the channel. The generated electrons are moved by the drain bias with high mobility, while the injected holes

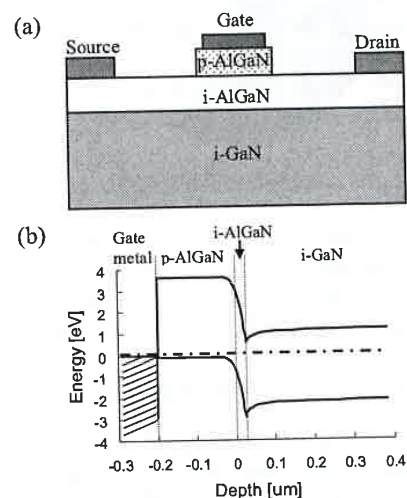


Fig.1 A schematic illustration of (a) GIT structure and (b) calculated band diagram of GIT at the gate bias of 0V. The epitaxial structure is designed to serve normally-off operations.

stay around the gate because the hole mobility is two order of magnitude lower than that of the electron. This results in significant increase of the drain current keeping the low gate current. Fig.3 shows distribution of holes and electrons in the

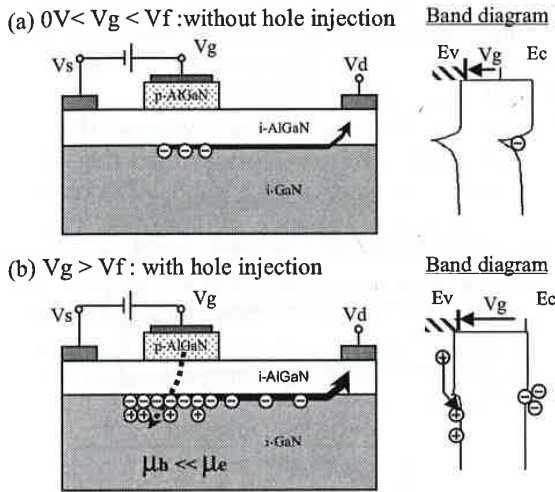


Fig.2 A schematic illustration of GIT operation varying gate voltages : (a) without hole injection at $V_g < V_f$, (b) with hole injection at $V_g > V_f$.

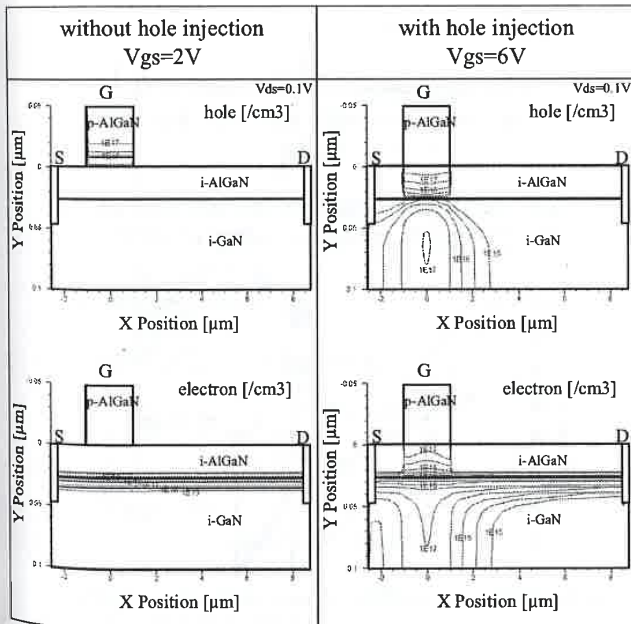


Fig.3 Distribution of holes and electrons in GITs varying gate voltages by 2D simulation : (a) $V_{gs}=2V$: without hole injection, (b) $V_{gs}=6V$: with hole injection.

GIT obtained by 2D-simulation at two gate voltages. At V_{gs} of 6V, hole injection into i-GaN as well as the increase of electron concentration is confirmed, while no hole is injected at V_{gs} of 2V. Fig.4 is the simulated sheet density of electrons and holes at the channel as a function of gate voltages, which indicates dramatic increase of carrier density at the gate voltages over the V_f .

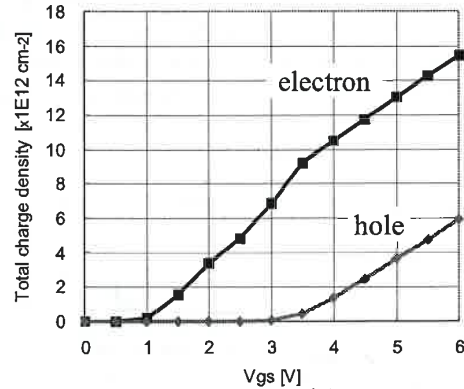


Fig.4 Calculated total charge density of holes and electrons integrated at entire depth in GIT varying gate voltages. The increased number of electrons are generated by the hole injection at higher gate voltage.

Device structure and fabrication

Fig. 5 shows the cross sectional SEM image of the fabricated GIT. A p-AlGaIn/AlGaIn/GaN hetero-epitaxial structure is grown on a cost-effective silicon substrate. In order to realize the normally-off operation, the Al mole fraction and the thickness of i-AlGaIn are optimized to be 15% and 25nm, respectively. The p-type gate is formed by inductively coupled plasma (ICP) dry etching. The used gate

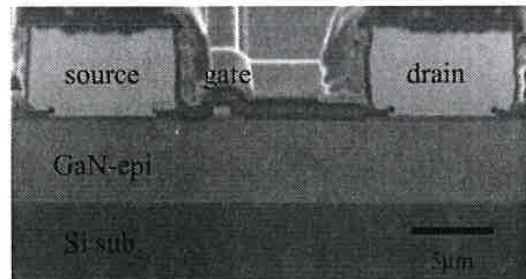


Fig.5 Cross sectional SEM image of GIT on a Si substrate.

and source/drain metals are Pd and Ti/Al, respectively. The gate length defined by the p-AlGaIn width is $2.0\mu\text{m}$ and a gate-drain spacing is $7.5\mu\text{m}$. The device is isolated by ion implantation of Boron.

Device Performance

Fig.6 and 7 summarize the DC characteristics of the fabricated GIT comparing with those of the conventional Schottky-gate FET. As shown in the figures, the forward gate voltage of 6V can be applied while the forward gate voltage is limited up to 2V in the conventional FET. No current-offset is observed at zero drain-bias as seen in Fig.6,

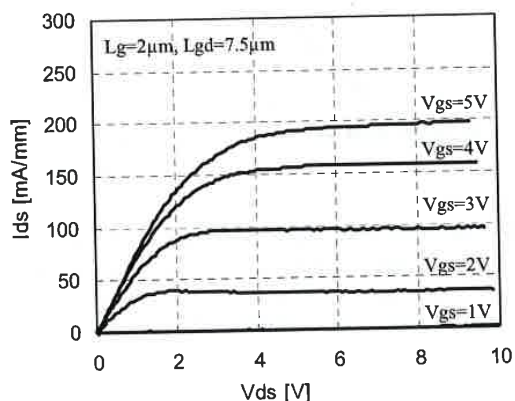


Fig.6 I_{ds} - V_{ds} characteristics of fabricated GIT ($R_{on}\cdot A=2.6\text{m}\Omega\cdot\text{cm}^2$, $I_{max}=200\text{mA/mm}$).

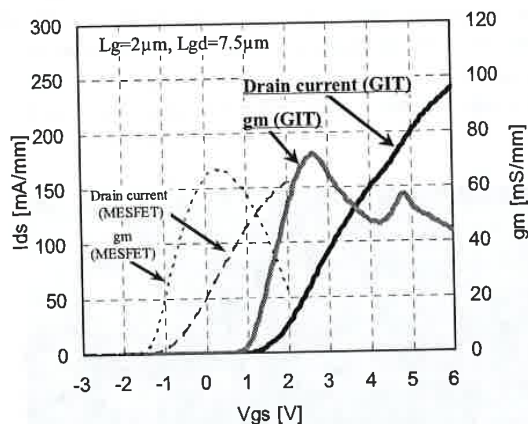


Fig.7 I_{ds} - V_{gs} and g_m - V_{gs} characteristics of fabricated (a) GIT and (b) MESFET.

implying the complete suppression of the gate current. The GIT exhibits peculiar transconductance characteristics with two peaks as seen in Fig.7. The device is operated as an FET up to the V_{gs} of 3V. Further increase of the V_{gs} super-linearly increases the I_{ds} corresponding to the second g_m peak, which is the direct evidence of the hole injection. Thus, this operation principle enables low on-state resistance with high drain current. The fabricated GIT exhibits the threshold voltage of 1.0V with high maximum drain current of 200mA/mm. The obtained on-state resistance ($R_{on}\cdot A$) and off-state breakdown voltage (BV_{ds}) are $2.6\text{m}\Omega\cdot\text{cm}^2$ and 640 V, respectively as shown in Fig.6 and 8. The cut-off (f_t) and the maximum frequency of oscillation (f_{max}) are extracted to be 4.2GHz and 10.7GHz, respectively as shown in Fig.9, which are as comparably high as the reported values of Schottky-gate normally-on AlGaIn/GaN power FETs [1].

In addition to the normally-off operation, suppression of the current collapse has been strongly desired for the GaN-

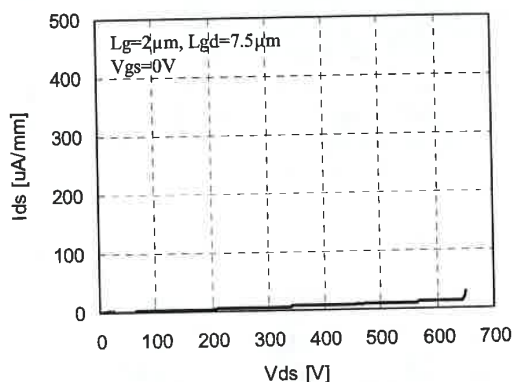


Fig.8 The off-state breakdown characteristics of GIT exhibiting the breakdown voltage of 640V.

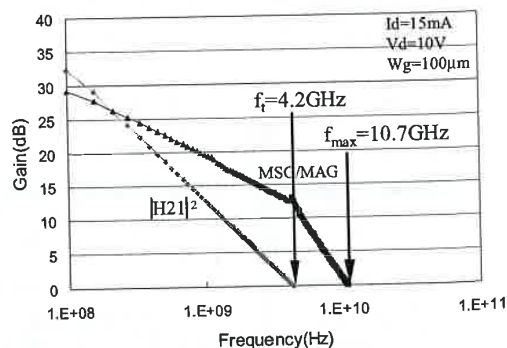


Fig.9 Frequency response of GIT. The cut-off and maximum oscillation frequency are extracted to be 4.2GHz and 10.7GHz, respectively.

based power switching devices. Fig.10 shows the results of the pulsed I-V measurements for the GIT with different initial bias conditions. The almost identical I-V characteristics imply that the GIT is operated free from the current collapse phenomena. The GIT is a conductivity modulated device so that it is not affected by the fixed charges trapped either at the surface or in the bulk GaN.

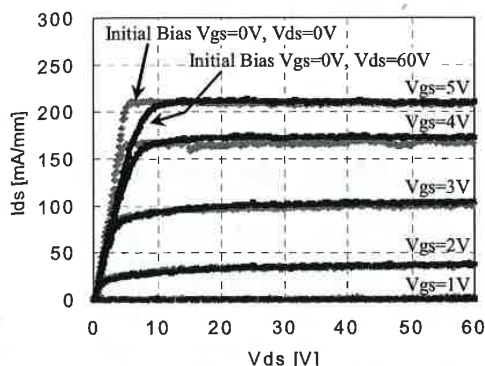


Fig.10 Pulsed I_{ds} - V_{ds} characteristics of fabricated GIT. Two sets of initial bias are used ($V_{gs}=0V$, $V_{ds}=0V$ and $V_{gs}=0V$, $V_{ds}=60V$). The used pulse width and period are $0.5\mu s$ and $1ms$, respectively.

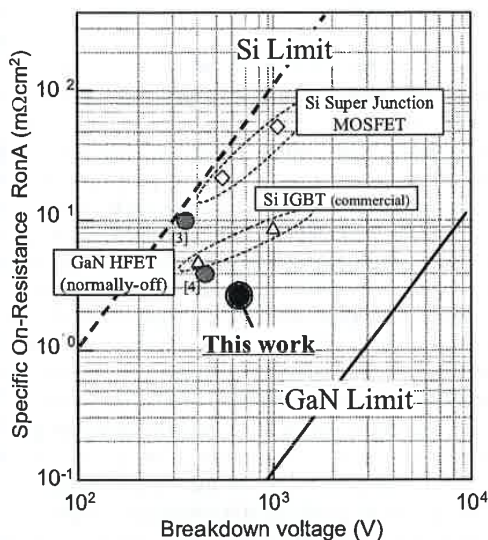


Fig.11 State-of-the-art $R_{on}A$ and breakdown voltage of normally-off GaN-based devices comparing with those of Si-based devices. The obtained results for the GIT is the best value among the reported values.

Conclusion

We have successfully developed a new normally-off AlGaIn/GaN transistor with high drain current. The transistor called GIT effectively utilizes hole-injection from the p-AlGaIn resulting in dramatic increase of the drain current at high gate voltages owing to the conductivity modulation. The resultant $R_{on}A$ and breakdown voltage are the best values among those of the reported GaN-based normally-off devices as summarized in Fig.11. The presented GIT is advantageous for power switching application replacing with currently used Si-based power MOSFETs and IGBTs.

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APPENDIX E



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