

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01382
Patent 9,748,347 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Innoscience (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc., (collectively “Petitioner”) filed a petition for an *inter partes* review (Paper 1 (“Pet.”)) challenging claims 1–3 of U.S. Patent No. 9,748,347 B2 (Ex. 1001 (“the ’347 Patent”)). Efficient Power Conversion Corporation (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). After receiving authorization from the Board, Petitioner filed a Reply to the Preliminary Response (Paper 8, “Reply”) and Patent Owner filed a Sur-reply (Paper 10, “Sur-reply”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, we determine the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review of all challenged claims of the ’347 patent on all grounds asserted in the Petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (stating that a decision to institute is “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

B. Related Matters

The parties identify two matters involving the '347 patent: *Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd*, 2:23-cv-04026-AB-AS (C.D. Cal. May 24, 2023) and *Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same*, Inv. No. 337-TA-1366 (ITC May 26, 2023). Pet. 108; Paper 5 (Patent Owner's Mandatory Notices), 2.

C. The '347 Patent (Ex. 1001)

The '347 patent, titled "Gate with Self-aligned Ledge for Enhancement Mode GaN Transistors," filed July 30, 2014 and issued August 29, 2017, is directed to "[a]n enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a [two-dimensional electron gas (2DEG)] region and a method for manufacturing the same." Ex. 1001, codes (45), (54), (57). The '347 patent claims priority to a number of applications, including US Patent Application 12/756,960, which published as Publication No. 2010/0258843 A1 (Ex. 1011, "Lidow").

The '347 patent explains that "GaN semiconductor devices are increasingly desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages." Ex. 1001, 1:25–27. Devices developed for high power/high frequency applications are based on structures that exhibit high electron mobility, and are referred to as, *inter alia*, high electron mobility transistors (HEMT). Ex. 1001, 1:29–33. A GaN HEMT device includes a nitride semiconductor with at least two nitride layers. Ex. 1001, 1:37–38. Different materials (e.g., AlGaN and GaN) on the semiconductor or on a buffer layer cause the layers to have different band gaps and also causes polarization, which contributes to a conductive

two dimensional electron gas (2DEG) region near the junction of the two layers, and allows charge to flow through the device. Ex. 1001, 1:40–44.

The '347 patent further explains that:

Because the 2DEG region exists under the gate at zero gate bias, most nitride devices are normally on, or depletion mode devices. If the 2DEG region is depleted (i. e., removed) below the gate at zero applied gate bias, the device can be an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide and because they are easier to control with simple, low cost drive circuits. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

Ex. 1001, 1:49–58.

Figure 2 of the '347 patent, reproduced below, depicts a prior art enhancement-mode GaN transistor.

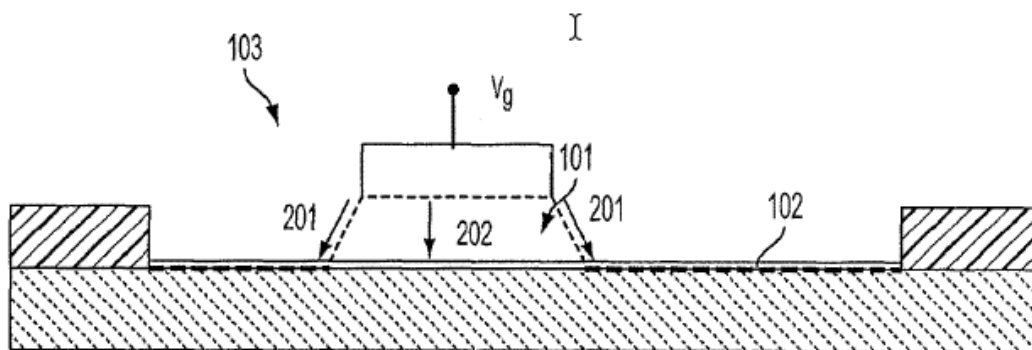


FIG. 2
PRIOR ART

Figure 2 depicts a conventional enhancement-mode GaN transistor having gate 103 comprising p-type material 101, and a 2DEG region 102 under gate 103, with two gate leakage current paths 201 and 202. Ex. 1001, 1:64–2:3, 2:63–65. According to the '347 patent, the first gate leakage current path 201 flows along the sidewall of the p-type gate material 101 and the second

gate leakage current path 202 flows through the bulk of the p-type gate material 101. Ex. 1001, 1:67–2:3.

The '347 patent depicts an embodiment of the claimed invention in Figure 5, reproduced below.

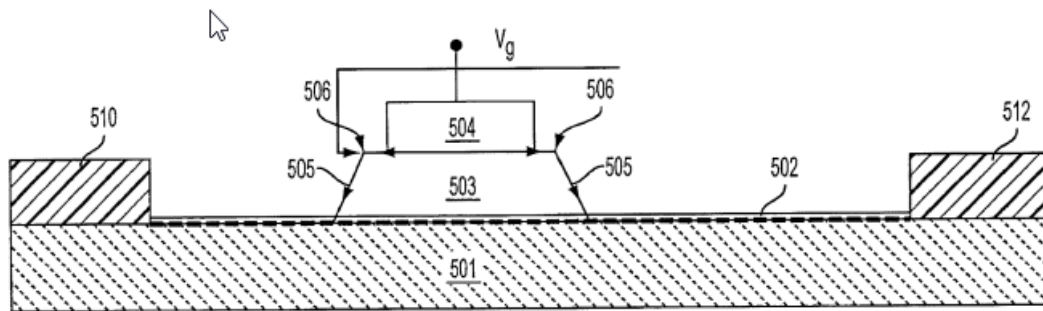


FIG. 5

Figure 5 shows a schematic diagram of a transistor device including GaN base layer 501, barrier layer 502, source metal 510 (i.e., source contact), drain metal 512 (i.e., drain contact), p-type gate material 503, gate metal 504, and horizontal ledges 506 on each side of gate metal 504. Ex. 1001, 3:5–7, 3:32–49. The '347 patent states that pair of ledges 506 that extend past sidewalls of gate metal 504 “have equal or substantially equal widths, i.e., the respective ledges are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material, which is due to the self-aligned manufacturing process.” Ex. 1001, 3:54–59.

Figure 5 also includes arrows showing gate current path 505 that travels horizontally along the ledges 506 and then follows the diagonal path along the edge of p-type gate material 503. Ex. 1001, 4:1–5. According to the '357 patent, this structure results in reduced gate leakage current compared to conventional gates without ledges. Ex. 1001, 4:6–7.

The '357 patent also describes an exemplary manufacturing process for forming a gate with self-aligned ledges, and depicts the steps in Figures 6A–6C, reproduced below. Ex. 1001, 4:8–33, Figs. 6A–6C.

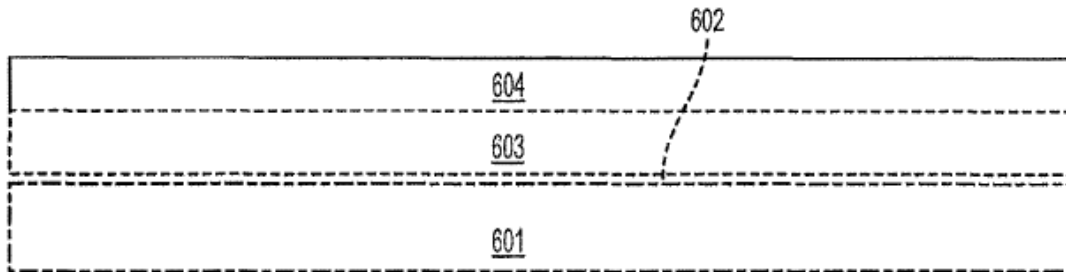


FIG. 6A

Figure 6A shows forming AlGaN barrier layer 602 on GaN base layer 601, forming a layer of p-type gate material 603 on barrier layer 602, and depositing gate metal 604 on p-type gate material 603. Ex. 1001, 4:10–16.

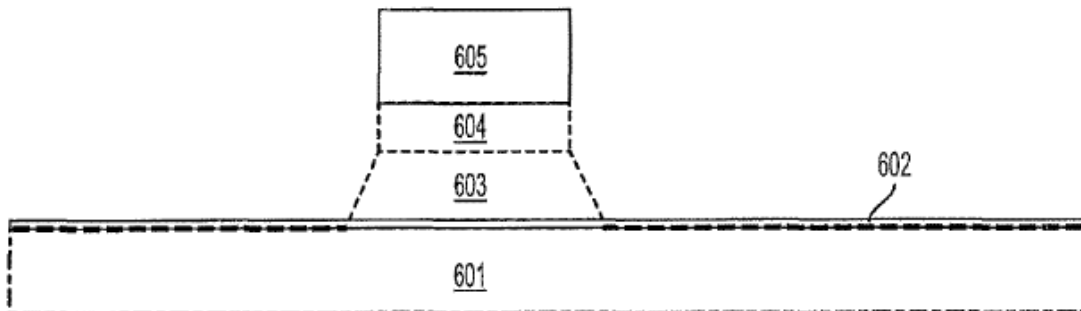


FIG. 6B

Figure 6B shows photoresist layer 605 deposited on gate metal 604, and the resulting structure after gate metal 604 and p-type gate material are etched. Ex. 1001, 4:17–20.

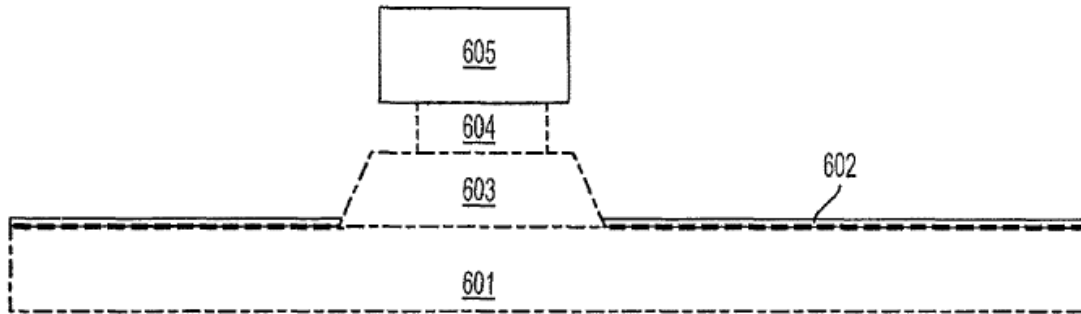


FIG. 6C

Figure 6C shows the resulting structure after gate metal 604 is etched isotropically such that gate metal 604 has a width less than the planar upper surface of p-type gate material 603. Ex. 1001, 4:20–23. According to the '347 patent, “[t]his second etching step results in the formation of the ledges 506 of the p-type gate material 603.” Ex. 1001, 4:23–25.

The '347 patent states that the self-aligned process illustrated in figures 6A–6C is “vastly superior to forming gate ledges using separate masks” due to the possibility of misalignment between the gate metal and p-type gate material when using a two-mask process. Ex. 1001, 4:46–57.

D. Illustrative Claims

Petitioner challenges claims 1–3 of the '347 patent. Independent claim 1 is reproduced below.

Claim 1:

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

- [1d] depositing a p-type gate material on the barrier layer;
- [1e] depositing a gate metal on the p-type gate material;
- [1f] forming a photoresist over the gate metal;
- [1g] etching the gate metal and the p-type gate material,
- [1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and
- [1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

Ex. 1001, 4:66–5:14 (labels and formatting added to correspond with Petitioner’s designation of claim limitations (Pet. Claim Appendix)).

E. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–3 are unpatentable based on the following challenges:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3	103	Saxler, ¹ Beach, ² Shenoy ³
1–3	103	Saxler, Yoshida, ⁴ Beach, Shenoy
1–3	103	Saxler, Ahn ⁵
1–3	103	Yoshida, Saxler, Beach, Shenoy

¹ US 2006/0108606 A1, published May 25, 2006 (Ex. 1007, “Saxler”).

² US 2007/0007547 A1, published Jan. 11, 2007 (Ex. 1008, “Beach”).

³ R.V. Shenoy, et. al, *Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*, J. ELECTROCHEM. SOC., Vol. 143, No. 2, 544, Feb. 1996 (Ex. 1009, “Shenoy”).

⁴ JP H11-261053, published Sept. 24, 1999 (Ex. 1005 (original language); Ex. 1006 (certified English translation), “Yoshida”).

⁵ US 5,905,247, issued May 18, 1999 (Ex. 1010, “Ahn”).

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3	103	Yoshida, Ahn

Pet. 17. Petitioner relies on the declaration of James Richard Shealy, Ph.D. (Ex. 1003).

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner asserts that a person of ordinary skill in the art would have had a “at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field, and at least two years of experience in semiconductor device design and/or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies.” Pet. 19 (citing Ex. 1003 ¶¶ 52–53). Petitioner also contends that “[a]dditional education could substitute for professional experience and vice versa.”

Pet. 19. Patent Owner does not challenge Petitioner’s definition or offer its own. *See generally* Prelim. Resp.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner’s proposal regarding the level of ordinary skill in the art. Based on our review of the ’347 patent and the prior art of record, we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the ’347 patent and the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown”)

(quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

B. Claim Construction

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). In this context, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (citations omitted) (en banc). The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

Both parties state that no claim construction is required at this stage of the proceeding. *See* Pet. 23; Prelim. Resp. 6. Petitioner, however, identifies three terms recited in claim 1 whose construction was disputed in a related proceeding, namely: (1) “forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer” (“forming the side surfaces” limitation), (2) “etching the gate metal and the p-type gate material”, and (3) “etching the gate metal to form a pair of ledges,” and proposes constructions for each of these terms. Pet. 19–24 (citing, *inter alia*, Ex. 1028 (Petitioner and Complainant’s Proposed Claim Construction, ITC 337–TA-1366)). Patent

Owner disputes Petitioner's proposed construction for "forming the side surfaces." Prelim. Resp. 6–9.

1. *"forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer"*

Petitioner contends that we should construe the "forming the side surfaces" limitation to mean "forming side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces that contact the barrier layer,*" which is the same construction that it proposed during the related ITC proceeding. Pet. 20 (citing Ex. 1028). According to Petitioner, its proposed construction should apply because an earlier application in the priority chain of the '347 patent (i.e., "Lidow," Ex. 1011), teaches that a "base that is more than 10% wider than the top" advantageously causes a longer path for electrons to travel between gate metal 17 and the 2DEG along the pGaN sidewall, thereby resulting lower gate leakage. Pet. 20 (citing Ex. 1011 ¶ 42). Petitioner explains that this construction enables the purpose of the element, namely reducing gate leakage, through the "conventional method of sloping the sidewalls to increase the length of sidewall leakage path 201." Pet. 21 (citing Ex. 1001, code (57), 1:19–23, 2:15–43, 3:60–4:7, 4:34–45, Figs. 2, 4, 7A–7B, 8; Ex. 1003 ¶ 73). Petitioner also asserts that this construction "accords" with the '347 Specification, which only shows sloped side surfaces whose bottom surfaces are approximately 30% wider (thus more than 10% wider) than the top. Pet. 21 (citing Ex. 1001, Figs. 5, 6C, 7B; Ex. 1003 ¶ 73).

Petitioner also asserts that the challenged claims are unpatentable under the construction proposed by Patent Owner during the related ITC

proceeding, i.e., “forming side surfaces of the p-type gate semiconductor material such that the bottom of the material, which contacts the barrier layer, is wider than the top of the material.” Pet. 20 (quoting Ex. 1028) (emphasis omitted).

Patent Owner responds by arguing Petitioner’s construction improperly imports three restrictions into claim 1. Patent Owner asserts that claim 1 should not be construed to require (1) that the claimed surfaces be *sloped*, (2) that the bottom of the top gate be *more than 10% wider* than the top of the material, or (3) that the sloped portion of the claimed side surfaces must *contact the barrier layer*. Prelim. Resp. 6–9. Patent Owner asserts that the claims do not recite any numerical degree of horizontal extension for the side surfaces or threshold values for the p-type gate material compared to the top, and Patent Owner’s only support for its proposed restriction comes from a single embodiment in the ’347 patent’s priority document, Lidow. Prelim. Resp. 6–7 (citing US 8,404,508,⁶ 5:23–28). Accordingly, Patent Owner argues that

there is no intrinsic evidence *defining* the horizontal extension of the side surfaces to have a minimum threshold value or unequivocally disavowing from the scope of the claims p-type gate materials where the side surfaces extend horizontally towards the source and drain contacts but where the bottom of those materials is less than 10% wider than the top.

⁶ The ’347 patent claims priority to US Patent App. 12/756,960, which published as US Pub. No. 2010/0258843 A1 (Ex. 1011), and which issued as US Patent 8,404,508.

Prelim. Resp. 7 (citing *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015)).

Patent Owner also contends that there is no support for Petitioner's proposed restriction that the claimed side surfaces must be "sloped." Prelim. Resp. 8–9. According to Patent Owner, a sloped side surface is only one example of the type of side surface encompassed by the plain and ordinary meaning of the claim language. Prelim. Resp. 8. Patent Owner contends that limiting the claim to sloped side surfaces would read out embodiments disclosed in Lidow, such as stepped side surfaces, wherein the bottom is wider than the top. Prelim. Resp. 8–9.

We first address Petitioner's argument that "side surfaces" of the p-type gate material of independent claim 1 requires that the "bottom of the p-type gate material is more than 10% wider than the top of the material." Pet. 19. We begin our analysis with the language of the claims themselves. *See Phillips*, 415 F.3d at 1312. Here, the claims do not recite any numerical degree of horizontal extension, let alone a requirement that the bottom of the p-type gate material must be more than 10% wider than the top of the material. Thus, the plain language of the claims themselves do not support Petitioner's proposed construction.

Of course, the claims do not stand alone, but rather, must be read in view of the specification, of which they are part. *Phillips*, 415 F.3d at 1313. Petitioner relies on a numerical value for horizontal extension disclosed in Lidow, which is incorporated by reference in the '347 patent. Pet. 20 (citing Ex. 1011 ¶¶ 41–42, Fig. 8; Ex. 1003 ¶¶ 70–74). But Lidow's disclosure of a numerical value (10%) is made in the context of discussing a single

embodiment. Ex. 1011 ¶ 41. Lidow does not include a numerical value in its disclosure of other embodiments. *See, e.g.*, Ex. 1011 ¶¶ 43–51.

Petitioner’s argument that its proposed construction “accords with the ’347 patent’s disclosure” of figures depicting a p-type gate material that has a bottom base that is approximately 30% wider than the top is similarly unavailing. Pet. 21–22. Petitioner’s argument is based on its numerical size measurements made on Figures 5, 6C, and 7B of the ’347 patent. Pet. 21–22. Figures 5 and 6C, however, are schematic diagrams that contain no numerical values and may not be relied upon to show particular sizes in this context. *See Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (stating “it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue”); *see also In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977) (“Absent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value.”). Dr. Shealy contends that Figure 7B is an actual image of an etched gate structure (Ex. 1003 ¶ 73), but the ’347 patent makes clear that this is only a single, exemplary embodiment. Ex. 1001, 3:22–23. The ’347 patent also states, with regard to the embodiments disclosed in the Specification, that “[i]t is to be understood that other embodiments may be employed and that various structural, logical, and electrical changes may be made.” Ex. 1001, 3:25–27. Thus, to the extent Petitioner’s size measurements are even accurate, we are not persuaded, based on the present record, that the “side surfaces” of the p-gate material recited in the independent claims should be construed to

require that the bottom of the p-type gate material is more than 10% wider than the top of the material.

We reach a similar determination regarding Petitioner's argument that we should construe the claims to require formation of sloped sidewalls. Pet. 19–21. The claims do not expressly require a sloped side surface or a sloped surface, and Petitioner does not direct us to any limiting language regarding sloped side surfaces in the Specification of the '347 patent. Further, as Patent Owner points out (Prelim. Resp. 8–9), Lidow discloses embodiments wherein the gate material has stepped sidewalls, such that the bottom of the gate material is wider than the top. *E.g.*, Ex. 1011, Figs. 9–12, ¶¶ 43–44. Thus, Petitioner's argument is not supported by Lidow's disclosure. Therefore, on this record, Petitioner fails to demonstrate sufficiently that the claims should be limited by requiring the side surfaces to be sloped.

In view of the foregoing, for purposes of this Decision, we decline to adopt Petitioner's proposed construction of the "side surfaces" limitation. After considering the arguments and information presented in the Petition and Preliminary Response, we determine that it is not necessary to further construe this term for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

2. *“etching the gate metal and the p-type gate material”*

Claim 1 requires the step of “etching the gate metal and the p-type material.” Petitioner asserts that “in a related matter,⁷” Petitioner proposed that this term should be construed as “*using the photoresist to etch the gate metal and the p-type gate metal and the p-type gate material*” and that Patent Owner proposed the term be construed as “etching the gate metal *and etching* the p-type gate material.” Pet. 23 (emphasis added by Petitioner). Petitioner, however asserts that the challenged claims are unpatentable under both constructions. Pet. 23. Patent Owner does not address the claim construction of this term. We determine that no claim construction of this term is required to resolve the issues in dispute for purposes of this Decision.

3. *“etching the gate metal to form a pair of ledges.”*

Claim 1 recites the step of “after the etching of the gate metal and the p-type gate material, etching the gate metal to form a pair of ledges.” Petitioner asserts that in a related matter, Petitioner proposed that this term should be construed as “after the etching of the gate meal and the p-type gate material, etching the gate metal to form a pair of ledges” and that Patent Owner proposed that this term should be construed as “[p]erforming a process during which gate metal is removed and two ledges are created.” Pet. 23 (emphasis omitted). Petitioner, however asserts that the challenged claims are unpatentable under both constructions because the process of etching the metal a second time to form ledges removes the gate metal. Pet.

⁷ Although not cited in the Petition, it appears that Petitioner is referring to the parties’ proposed constructions during the ITC proceeding. *See* Ex. 1028, 3 ([Petitioner’s] Proposed Constructions), 8 ([Patent Owner’s] Proposed Constructions).

23. Patent Owner does not address the claim construction of this term. We determine that no claim construction of this term is required to resolve the issues in dispute for purposes of this Decision.

C. Overview of Asserted Prior Art

1. Saxler (Ex. 1007)

Saxler, titled “Cap Layers and/or Passivation Layers for Nitride-Based Transistors, Transistor Structures and Methods of Fabricating Same” discloses Group III-nitride high electron mobility transistors and methods for forming those transistors. Ex. 1007, code (54), ¶¶ 1, 7. In particular, Saxler is directed to HEMTs that include “a non-uniform aluminum concentration AlGa_N based cap layer having a high aluminum concentration adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided.” Ex. 1007, code (57). Saxler explains that having such a cap layer “may improve robustness of the device during processing and/or device operation” over conventional devices. Ex. 1007 ¶ 47. Saxler also explains that HEMTs “may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies.” Ex. 1007 ¶ 4.

Saxler discloses several embodiments of its claimed invention, including the transistors depicted in Figures 1A and 1B, reproduced below.

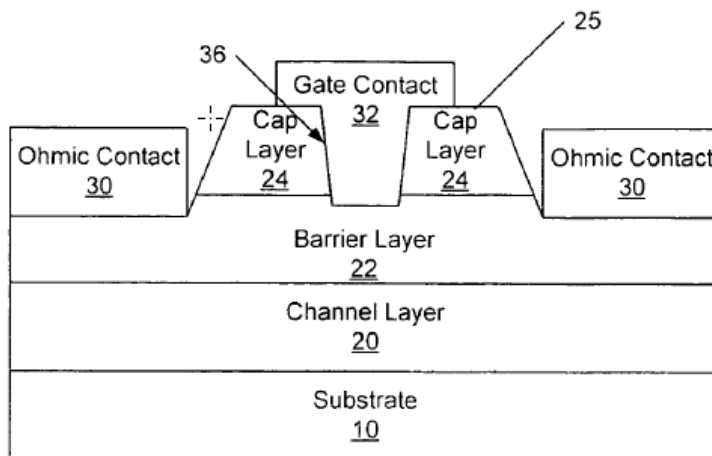


Figure 1A

Figure 1A of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66. In this embodiment, gate contact 32 occupies recess 36 in cap layer 24. Ex. 1007 ¶¶ 61, 66.

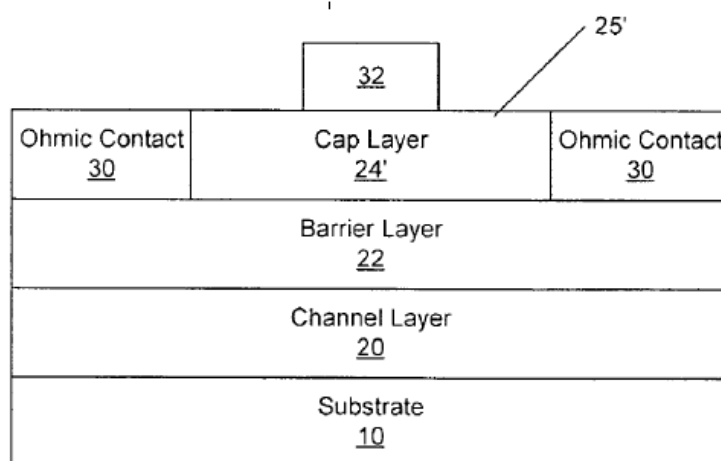


Figure 1B

Figure 1B of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66. In this embodiment, cap layer 24 does not have a recess, such that gate 32 is on cap layer 24. Ex. 1007 ¶¶ 61, 66.

Saxler describes the features of its various embodiments, including those with a gate recess and those without a gate recess. *E.g.*, Ex. 1007 ¶¶ 66 (describing suitable gate materials), 70 (describing suitable n-type dopants), 71 (describing suitable p-type dopants). Saxler also discloses methods for making transistors according to the embodiments described in the specification. Ex. 1007 ¶¶ 6, 68.

2. Yoshida (Ex. 1006)

Yoshida is a Japanese Patent Publication titled “High Mobility Transistor” that discloses novel GaN-based HEMT structures that can operate under the application of high voltages and at higher speeds. Ex. 1006 ¶¶ 1, 8. Yoshida depicts the basic structure of its claimed invention in Figure 1, reproduced below.

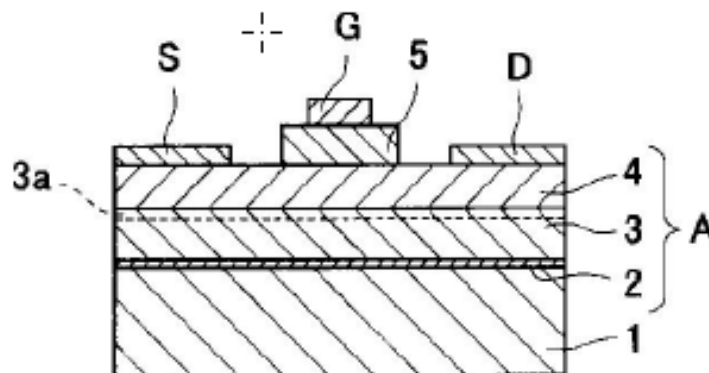


Figure 1 of Yoshida shows a cross-sectional view of a transistor having a stacked structure comprising buffer layer 2, i-type semiconductor layer 3, and n-type semiconductor layer 4 formed on semi-insulating substrate 1. Ex. 1006 ¶ 10. Figure 1 also shows gate electrode G on p-type semiconductor layer 5, as well as source electrode S and drain electrode D, all formed on n-type semiconductor layer 4. Ex. 1006 ¶ 10.

Yoshida discloses methods for fabricating the structure shown in Figure 1, including deposition and etching conditions. Ex. 1006 ¶¶ 19–23.

3. Beach (Ex. 1008)

Beach is a US Patent Publication titled “III-Nitride Enhancement Mode Devices” that discloses a “normally OFF III-nitride power semiconductor device and a method for the fabrication thereof.” Ex. 1008 code (12), ¶ 9. Beach depicts an embodiment of its invention in Figure 1, reproduced below.

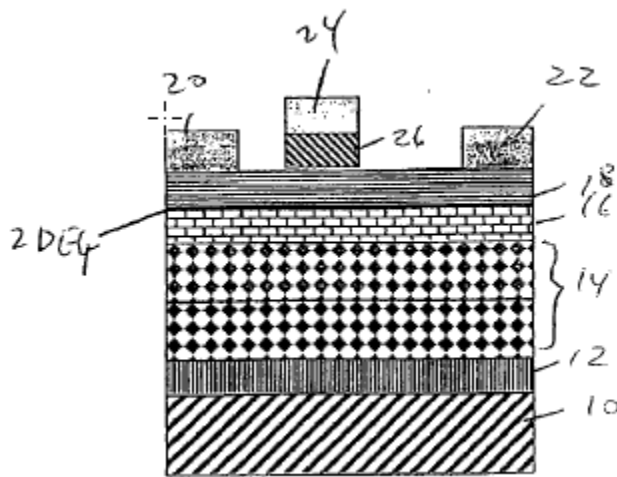


Figure 1 of Beach shows substrate 10, bonding layer 12, first III-nitride buffer body 14, first III-nitride semiconductor body 16, second III-nitride semiconductor body 18, first power electrode 20 and second power electrode 22, and gate arrangement 24, with gate barrier 26 disposed under gate

arrangement 24 and over second III-nitride semiconductor body 18.

Ex. 1008 ¶¶ 31–32.

Beach describes a method for making the embodiment shown in Figure 1, wherein “[m]aterials for the gate arrangement are then deposited on gate barrier material 42 and the stack is patterned and etched to obtain gate arrangement 24 over gate barrier 26.” Ex. 1008 ¶ 40. Beach states that “the method as described results in a self-aligned gate arrangement.” Ex. 1008 ¶ 40. Beach further explains that a device made according to the first embodiment is advantageous because, *inter alia*, it is an enhancement-mode device and it includes “self-aligned gates.” Ex. 1008 ¶¶ 43–45.

4. Shenoy (Ex. 1009)

Shenoy is an article titled “Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Machining.” Ex. 1009, 1. Shenoy pertains to the development of a “mathematical model to predict shape evolution during through-mask electrochemical micromachining (EMM).” Ex. 1009, 2.⁸ Shenoy explains that EMM is “receiving increasing attention in microfabrication for patterning, shaping, and finishing.” Ex. 1009, 2. Shenoy further explains that in through-mask EMM, an exposed metal surface is removed by high-rate anodic metal dissolution, and etching can occur from a single side or both sides simultaneously. Ex. 1009, 2. According to Shenoy, “[t]he isotropic nature of the metal removal process leads to undercutting of the [photoresist] mask,” and “knowledge of the metal removal rates and undercutting of the photoresist is, therefore, essential in designing the photoresist mask.” Ex. 1009, 2.

⁸ Citations to Shenoy are to page numbers added by Petitioner.

Shenoy states that EMM provides cost and environmental advantages over other fabrication techniques, and therefore “the predictability and control of metal wall profile and undercut are of particular interest.”

Ex. 1009, 2. In view of this, Shenoy investigates “the influence of the mask wall angle on the current distribution, the shape of the evolving cavity, and the etch factor.” Ex. 1009, 2.

5. *Ahn (Ex. 1010)*

Ahn is a US Patent titled “Thin-Film Transistor and Method of Making the Same” that issued on May 18, 1999. Ex. 1010, codes (45), (54). Ahn is directed to a thin-film transistor having a substrate, a gate having a double layered structure, and method of making same. Ex. 1010 at code (57). Figure 4C of Ahn is shown below.

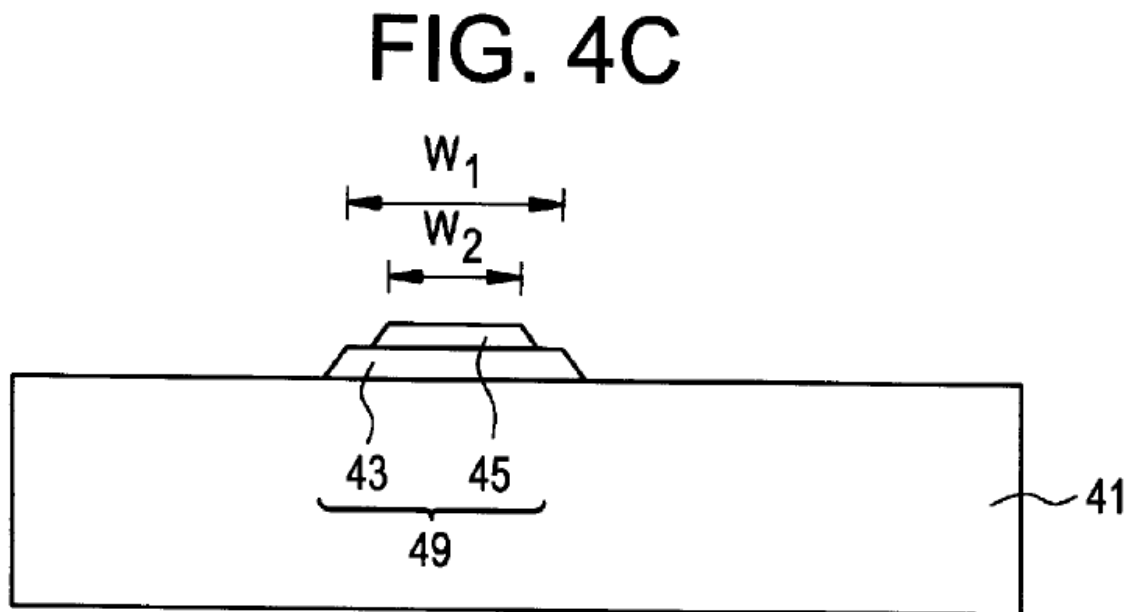


Figure 4C is a diagram depicting a step in the process for fabricating thin-film transistor. Ex. 1010, 5:38–40.

Ahn states that first metal layer 43 and second metal layer 45 result from a single photoresist step and form gate 49 having a double-layered

metal structure. Ex. 1010, 6:27–30. Gate 49 has second metal layer 45 positioned substantially in the middle of first metal layer 43. Ex. 1010, 6:30–34.

D. Claims 1–3 – Alleged Obviousness over Saxler, Beach, and Shenoy (Ground 1)

Petitioner contends claims 1–3 of the '347 patent are unpatentable as obvious over Saxler, Beach, and Shenoy. Pet. 24–50; Reply 2–8. Patent Owner opposes. Prelim. Resp. 18–28; Sur-reply 1–4.

1. Claim 1

Petitioner asserts that Saxler, or Saxler in combination with Beach and Shenoy, teaches the preamble and claim elements [1a]–[1d].

Petitioner states that Saxler discloses GaN transistors, such as the one shown below in Saxler Figure 1A, with Petitioner's color annotations added.

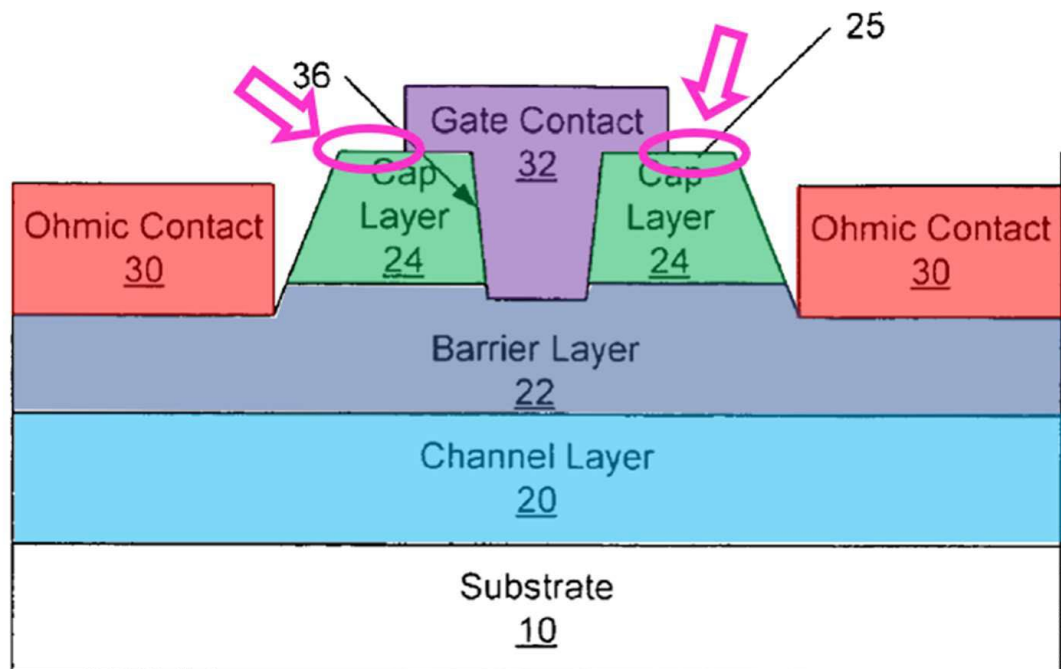
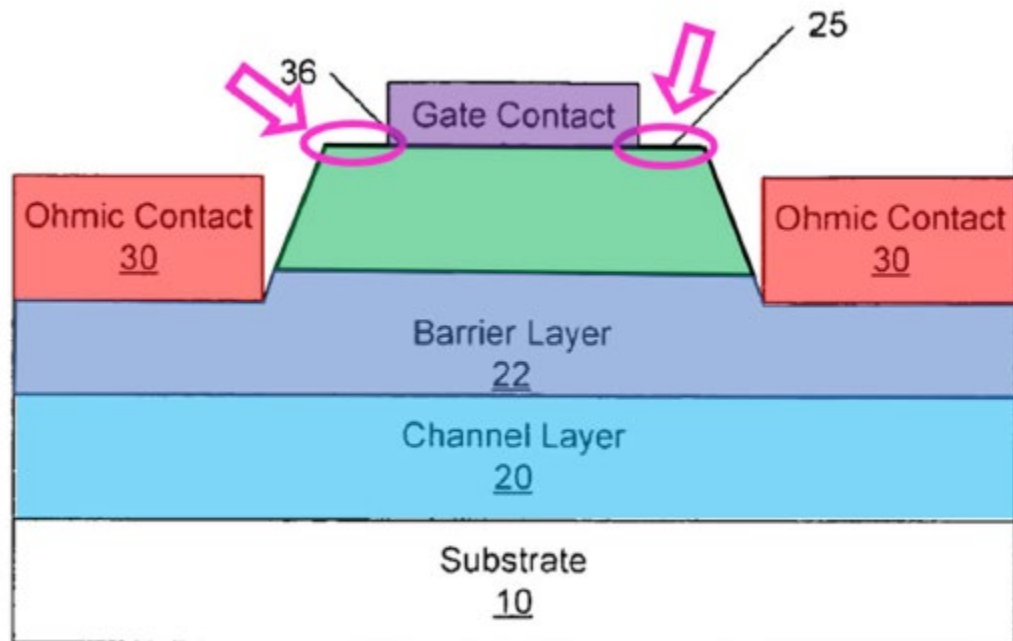


Figure 1A of Saxler shows a cross-sectional schematic view of a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30,

cap layer 24, and gate contact 32. Petitioner has annotated Figure 1A to show channel layer 20 in light blue, barrier layer 22 in dark blue, cap layer 24 in green, gate contact 32 in purple, and source and drain contacts 30 in red. Pet. 5, 25.

Petitioner recognizes that Figure 1A of Saxler shows an embodiment where gate contact 32 is recessed so that it extends through cap layer 24 into barrier layer 22. Pet. 25. Petitioner, however, contends that Saxler also teaches that its gate contact may be non-recessed (i.e., flat). Pet. 25 (citing, *inter alia*, Ex. 1007 ¶¶ 66, 81), 31 (citing Ex. 1007 ¶¶ 12–13, 27, 52, 64, 70–71, 73, claims 3, 14, 21, 27, 31, 88, Abstract). Petitioner asserts that where the gate recess is not utilized, Saxler would result in the following modified Figure 1A structure.



Petitioner's modified version of Saxler Figure 1A shows gate contact 36 (in purple), without a recess, stacked on cap layer 32 (in green), formed on barrier layer 22 (in dark blue), which is on top of channel layer 20 (light

blue) and substrate 10. Pet. 25–26. It also depicts source and drain contacts 30 (in red). Pet. 24–26.

Petitioner contends Saxler discloses making its GaN HEMT device (e.g., the device of modified Figure 1A) using a series of steps and that the device includes every feature according to the method of the '347 patent claims. Pet. 24–27, 35–49.

For example, Petitioner asserts Saxler discloses or suggest the preamble⁹ and steps [1a]–[1d] by teaching forming GaN channel layer 20, (light blue) and barrier layer 22 (dark blue) and depositing Ohmic source and drain contacts 30 (red) and a p-gate material (cap layer 24 – green) on barrier layer 22. Pet. 35–40 (citing Ex. 1007, code (57), ¶¶ 7–10, 13–14, 40, 42 46, 53–66, 69, 71–73 Figs. 1A, 1B, 1F; Ex. 1003 ¶¶ 99–108).

Petitioner asserts that Saxler, or Saxler in combination with Beach and Shenoy, render obvious steps [1e]–[1h], and that Saxler, in combination with Beach and Shenoy, renders obvious step [1i]. Pet. 40–49. Petitioner asserts Saxler renders obvious step [1e] (i.e., depositing a gate metal on the p-type gate material) because Saxler's gate contact is a metal, and in some embodiments—such as that of Saxler's modified Figure 1A—Saxler lacks a gate recess and does not separate the cap layer into distinct portions. Pet. 40–41 (citing, *inter alia*, Ex. 1003 ¶¶ 110–111; Ex. 1007 ¶¶ 12–13, 27, 52, 64, 66, 77–71, 73).

Petitioner asserts that it would have been obvious to form a photoresist over Saxler's gate metal as required by step [1f] because Saxler precisely positions its gate contact on the cap layer and a POSITA would

⁹ Neither Petitioner nor Patent Owner directly address whether the preamble is limiting. The parties are invited to address this issue during trial.

have understood that using a photoresist over gate metal is a conventional and precise masking technique. Pet. 42 (citing Ex. 1003 ¶¶ 60–62).

Petitioner also asserts that, under both parties’ proposed claim constructions, Saxler discloses or suggest “etching the gate metal and p-type gate material” to form “side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer” and “etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal” as recited in steps [1g]–[1i].

Pet. 43–49. In particular, Petitioner asserts Saxler etches its cap layer “to expose the underlying barrier” and place the source and drain contacts.

Pet. 44 (citing Ex. 1007 ¶ 64, Figs. 1A–1B; Ex. 1003 ¶ 120). According to Petitioner, the “sidewalls of the cap layer extend horizontally towards the source and drain contacts and contact the barrier layer in both recessed and [modified] non-recessed embodiments” and the bottom of the cap layer is more than 10% wider than the top. Pet. 44–45 (emphasis omitted) (citing Ex. 1003 ¶¶ 120, 123).

With respect to step [1i] (i.e., “etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal”), Petitioner asserts that Patent Owner admitted that, in a conventional enhancement mode transistor, ledges are made using separate masks for the p-type gate material and gate metal. Pet. 47 (citing Ex. 1011 ¶ 6, Fig. 1; Ex. 1003 ¶ 124). Petitioner further states that it would have been obvious in view of Saxler to make the ledges by etching the gate material and that it would have been obvious to use one mask to etch both the gate metal and cap layer to precisely place the gate and reduce manufacturing steps and costs. Pet. 47–48 (citing *inter alia*, Ex. 1003 ¶ 126).

Petitioner also relies on the combination of Saxler, Beach, and Shenoy for teaching the limitations of steps [1f]–[1i]. *See* Pet. 28–35, 48–49. In particular, Petitioner contends that Beach discloses a self-aligned method of making stacked gate structures in GaN HEMT devices using a single mask, and Shenoy discloses isotropic etching techniques for undercutting metal below photoresist masks. Pet. 28–29 (citing Ex. 1008 ¶¶ 40, 45, 54; Ex. 1009, 2–3). Petitioner contends it would have been obvious to make the stacked gate structure of Saxler’s non-recessed embodiments using the methods of Beach and Shenoy to, *inter alia*, reduce steps and costs, improve reproducibility and symmetry of the gate structure layers, and that doing so would have been simple and predictable. Pet. 31–35 (citing, *inter alia*, Ex. 1011 (“Smith”) and Ex. 1010 (“Ahn”) as teaching self-alignment techniques; Ex. 1003 ¶ 93). Petitioner also notes that the ’347 patent was allowed without disclosing any particular method to obtain the claimed ledges because their manufacture was within the skill level of a POSITA. Pet. 34 (citing Ex. 1002, 25–30, 44–45, 74–76, 80–99; Ex. 1003 ¶¶ 57–63, 98).

According to Petitioner, self-aligned techniques were common in the field as of the priority date of the ’347 patent, and Sheppard (Ex. 1021), incorporated by reference in Saxler to disclose methods of fabricating GaN transistors, describes a flexible approach to masking and etching. Pet. 33–34 (citing Ex. 1007 ¶¶ 46, 68; Ex. 1021 ¶ 58; Ex. 1003 ¶ 95). Petitioner further contends that a person of ordinary skill in the art would have created the stepped gate structure by using Beach’s self-aligned technique and Shenoy’s isotropic undercutting to improve reproducibility and symmetry of the gate contact with respect to the gate layer. Pet. 34–35 (citing Ex. 1003 ¶¶ 57–63,

96–98). Petitioner also asserts Beach and Shenoy’s techniques reduce masking steps and costs. Pet. 34–35 (citing Ex. 1003 ¶ 159). Petitioner contends that using Beach’s manufacturing steps and Shenoy’s isotropic techniques would have involved simple substitutions that could be predictably implemented in Saxler’s flexible method of manufacturing. Pet. 35 (citing Ex. 1003 ¶ 98). Finally, Petitioner asserts that the ’347 patent was allowed without disclosing any particular methods to obtain the claimed ledges because such methods were within a POSITA’s ability. Pet. 35 (citing Ex. 1003 ¶¶ 57–63, 98; Ex. 1002, 29, 55).

Patent Owner responds that Petitioner’s hypothetical structure of modified Figure 1A of Saxler, which combines the non-recessed gate of Figure 1B with ledges and sloping sidewalls of Figure 1A, does not appear anywhere in Saxler, and is designed solely based on hindsight. Prelim. Resp. 18–23. According to Patent Owner, Saxler discloses two embodiments of its cap layer: a bifurcated recessed cap layer with slanted sidewalls shown in Figure 1A and a non-recessed cap layer depicted as a rectangular layer between the source and drain contacts, as shown in Figure 1B. *E.g.*, Prelim. Resp. 18, 21. Patent Owner contends that Saxler does not teach, nor would a POSITA have been motivated, to combine or modify these embodiments to arrive at the “hypothetical” modified Figure 1A. Prelim. Resp. 18, 22. Thus, Patent Owner asserts Saxler does not teach or suggest “forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier” as recited in claim 1. Prelim. Resp. 22.

Patent Owner further asserts that forming sloped sidewalls together with top surface ledges was not known and Petitioner has not cited to any

evidence teaching benefits of elongated surface ledges for enhancement mode GaN transistors. Prelim. Resp. 22. Patent Owner contends that Saxler chose to depict its non-recessed embodiments without sloped sidewalls, and a POSITA may have understood that forming the opening for the recessed gate, if anything, also formed the sloped sidewalls on the gate structure. Prelim. Resp. 22–23.

Although the structure depicted in modified Figure 1A of Saxler does not itself appear in Saxler, Petitioner has provided sufficient argument and evidence at this stage of the proceeding that a person of ordinary skill in the art would have understood that Saxler suggests a stacked gate structure having a gate contact, a cap layer without a recess, and sloped sidewalls, as depicted in modified Figure 1A. E.g., Pet. 25–26, 39–41. First, as Petitioner and Dr. Sealy note, the '347 patent itself recognizes that sloped sidewalls were known and conventional in the prior art. Pet. 74; Ex. 1003 ¶ 199; Ex. 1001, 1:28–2:26, Figs. 1, 2, 3A, 3B (all labeled as “PRIOR ART” and showing sloped sidewalls).

Next, Saxler describes embodiments of its claimed invention without a gate recess. *See* Ex. 1007 ¶¶ 12, 13, 27, 70, 73, claims 3, 14, 21, 27, 31, 88. For example, in paragraph 27, Saxler states that “[t]he transistor may further include a gate contact recessed into the AlN cap layer,” and also that “[t]he transistor may *also* include a gate contact on the AlN cap layer and not recessed into the AlN cap layer.” Ex. 1007 ¶ 27 (emphasis added). Additionally, in its figures, Saxler discloses cap layer 24 with and without a recess. Ex. 1007, Figs. 1A, 1B. Saxler’s figures also depict gate contact 32 being formed in a gate recess of cap layer 24 (having a T shape as shown in Figure 1A) or on top of cap layer 24 (i.e., flat, as shown in Figure 1B).

Moreover, Saxler states that the embodiments shown in the figures are exemplary, and its claimed invention should not be limited to those examples. Ex. 1007 ¶ 52.

Dr. Shealy states that in embodiments where a gate recess is not utilized, Saxler has the structure shown in modified Figure 1A of Saxler. Ex. 1003 ¶ 81. Dr. Shealy's testimony appears to be consistent with the disclosure of Saxler, and Patent Owner does not offer conflicting testimony from a declarant.

For all of the foregoing reasons, based on the present record, Petitioner sufficiently shows that Saxler at least suggests a stacked gate structure having a gate contact and cap layer without a recess, as depicted in modified Figure 1A of Saxler.

Patent Owner also argues that Saxler does not disclose or suggest a method for manufacturing an enhancement-mode device. Prelim. Resp. 11, 18–21. Patent Owner contends that Saxler explains the purpose of doping the cap layer is to reduce gate leakage along dislocations and that a person of ordinary skill in the art would have understood this “is unrelated and distinct from creating an enhancement mode transistor.” Prelim. Resp. 11. Patent Owner also asserts that the transistor depicted in modified Figure 1A would not function as an enhancement-mode device, stating that “it would be non-operational due to its inability to induce a 2DEG between the ohmic contacts.” Prelim. Resp. 19.

According to Patent Owner, the cap layer in modified Figure 1A of Saxler reaches “all the way from source to drain,” depleting the access regions between the gate contact and each of the ohmic contacts, which results in the absence of 2DEG all the way from source to drain. Prelim.

Resp. 20. Patent Owner thus asserts that the hypothetical transistor would always lack a 2DEG in the access regions and the 2DEG could not be induced in those regions. Prelim. Resp. 20. Patent Owner concludes that “[w]ithout a 2DEG, such a transistor will not work properly and could not be switched to its ON state, thereby rendering the hypothetical device non-functional as an enhancement-mode device.” Prelim. Resp. 21.

Petitioner, however, contends that a person of ordinary skill in the art would have understood Saxler’s transistors lacking a gate recess are enhancement-mode GaN when the cap is doped p-type. Pet. 35–36 (citing Ex. 1003 ¶ 99; Ex. 1021 ¶¶ 14, 40, 42, Fig. 1F). Additionally, Petitioner presents declarant testimony supporting its argument that the structure depicted in modified Figure 1A is an enhancement-mode device when p-type dopants are placed in the cap layer below the gate and above an AlGa_N barrier layer, as disclosed in Saxler. Ex. 1003 ¶ 99 (citing Ex. 1007 ¶¶ 7–10, 46, 59–64, Figs. 1A, 1B). Dr. Shealy also relies on disclosures in Sheppard, which is incorporated by reference in Saxler, to support his position that a person of ordinary skill in the art would have understood a transistor having the gate structure shown in modified Figure 1A to constitute a normally-off enhancement-mode GaN transistor. Ex. 1003 ¶ 100 (citing Ex. 1021 ¶¶ 14, 40, 42; Ex. 1007 ¶¶ 46, 68, Fig. 1F).

Patent Owner’s argument that a person of ordinary skill in the art would have recognized the purpose of doping in Saxler is unrelated to and distinct from creating an enhancement mode device is unavailing at this stage of the proceeding as it raises issues best resolved on a full record at trial. Prelim. Resp. 11. At this stage of the proceeding, Patent Owner relies on unsupported attorney argument for this contention, which does not

constitute evidence. *See Laitram Corp. v. Cambridge Wire Cloth Co.*, 919 F.2d 1579, 1583 (Fed. Cir. 1990). Additionally, even if Patent Owner is correct about the purpose of doping—to reduce gate leakage along dislocations—its argument does not address the relevant question of whether or not doping the cap layer in Saxler actually creates an enhancement mode transistor. At this stage of the proceeding, Petitioner has provided sufficient evidence, supported by declaration testimony, that Saxler discloses an enhancement mode GaN transistor. *E.g.*, Pet. 35–36.

Patent Owner also argues that a POSITA would not have found it obvious to combine the teachings of Saxler, Beach, and Shenoy because Beach discloses a “gate-first” fabrication process, which is incompatible with Saxler, which discloses a gate-last fabrication process. Prelim. Resp. 23–26. Patent Owner further asserts that Beach describes a substantially different layer sequence and device structure, and Beach’s teachings would not, and could not, have been adapted into Saxler. Prelim. Resp. 24–25 (stating Beach describes N-polar orientation, which is different from Saxler). Patent Owner also contends that Petitioner fails to provide any motivation to use Shenoy’s isotropic etching technique to obtain ledges after Beach’s self-aligned process. Prelim. Resp. 26. Patent Owner further contends that Petitioner fails to address how a POSITA would have manufactured ledges *after* Beach’s self-aligned etching process has already occurred and does not explain whether or not an additional photomask would be required. Prelim. Resp. 26–27.

Again, Patent Owner’s arguments raise issues that are best resolved on a full record. While we do have some concern’s regarding Petitioner’s asserted reasons to combine all of the prior art references, Petitioner has

provided sufficient argument and evidence for purposes of institution that a POSITA would have had reason to manufacture the modified Figure 1A of Saxler by using Beach's self-aligned technique with Shenoy's isotropic etching process, and would have had a reasonable expectation of success. Pet. 32 (citing Ex. 1003 ¶¶ 60–62, 93; Ex. 1014 (Xu); Ex. 1021 (Sheppard); Ex. 1015 (Smith); Ex. 1018 (Hu); Ex. 1009 (Shenoy); Widmann (Ex. 1023); Ahn (Ex. 1010); *see also* Pet. 31–35. For example, Dr. Shealy testifies that a POSITA would have recognized that using Beach's self-aligned techniques and Shenoy's isotropic etching process to arrive at Saxler's non-recessed gate structure would have been a simple and predictable combination in view of Smith's use of self-alignment techniques to create its stacked gate structure and would have done so to reduce steps and costs while improving reproducibility. Ex. 1003 ¶ 93.

We also note that we understand Petitioner's proposed combination uses a single photomask when etching both the gate metal and the p-type gate material layer, including when etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal. *See, e.g.*, Pet. 48 (stating that it would have been obvious to use one mask to etch the gate metal and cap layer and further stating that using Shenoy's method of isotropically etching the gate metal would form symmetric undercuts of the photomask). To the extent, the Board's understanding of Petitioner's argument is not correct, the parties are urged to address this issue.

Finally, Patent Owner asserts that Shenoy is non-analogous art and may not be combined with Saxler or Beach because Shenoy involves *electrochemical* etching, a highly specialized etching method with little

relevance to the process described in the '347 patent or Saxler. Prelim. Resp. 27.

A reference is analogous art to the claimed invention if: (1) the reference is from the same field of endeavor as the claimed invention (even if it addresses a different problem) or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it is not in the same field of endeavor as the claimed invention). *See In re Clay*, 966 F.2d 656, 658 (Fed. Cir. 1992).

Based on the present record, Petitioner's evidence and arguments, sufficiently show that Shenoy and the '347 patent are analogous art under both of the above recited tests. First, Petitioner asserts that Shenoy, which discloses conventional methods for etching metals in semiconductors, is from the same field of endeavor as the '347 patent. Pet. 29–30 (citing Ex. 1003 ¶¶ 87–88); Sur-reply 5. Petitioner states that the '347 patent generally relates to transistors and broadly defines the pertinent field as “layered semiconductors that include various field effect transistors.” Reply 4–5 (citing, *inter alia*, Ex. 1001, 1:20–58). Petitioner also asserts that Shenoy discloses etching methods that can improve gate metal positioning relative to the underlying layer while reducing costs and is thus reasonably pertinent to the particular problem of gate leakage addressed by the '347 patent. Sur-reply 6 (citing Ex. 1003 ¶¶ 87, 150 203–209). Patent Owner's arguments to the contrary raise issues best resolved on a full record.

We have reviewed Petitioner's arguments and evidence and determine, based on the present record, that Petitioner has sufficiently shown for purposes of institution that Saxler, Beach, and Shenoy teach or suggest all of the limitations of claim 1 and that a person of ordinary skill in the art

would have had reason to combine the teachings of the asserted art, notwithstanding Patent Owner's arguments to the contrary. Patent Owner's arguments to the contrary raise issues best resolved on a full record. Accordingly, we determine that Petitioner has demonstrated a reasonable likelihood of showing that claim 1 would have been obvious over Saxler, Beach, and Shenoy.

Because we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one of the claims challenged in the Petition, we institute *inter partes* review of all claims and all challenges raised in the petition. Nevertheless, in order to further guide the parties after institution, we provide the following observations.

2. *Claim 2*

Claim 2 depends from claim 1 and further requires that the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal such that the width of the gate metal is less than a width of the p-type gate material. Ex. 1001, 5:15–18. Petitioner asserts that claim 2 would have been obvious for the same reasons set forth in connection with step [1i]. Pet. 49 (citing Ex. 1007 ¶¶ 14, 46, Fig. 1F; Ex. 1003 ¶ 128).

Patent Owner does not address Petitioner's arguments with respect to claim 2, apart from its arguments related to independent claim 1, addressed above. We have reviewed Petitioner's arguments and evidence and determine Petitioner has shown sufficiently, at this stage of the proceeding, that Saxler, Beach, and Shenoy teach or suggest all of the limitations of claim 2 and that a person of ordinary skill in the art would have had reason to combine the teachings of the asserted art. Accordingly, we determine that

Petitioner has demonstrated a reasonable likelihood of showing that claim 2 would have been obvious over Saxler, Beach, and Shenoy.

3. *Claim 3*

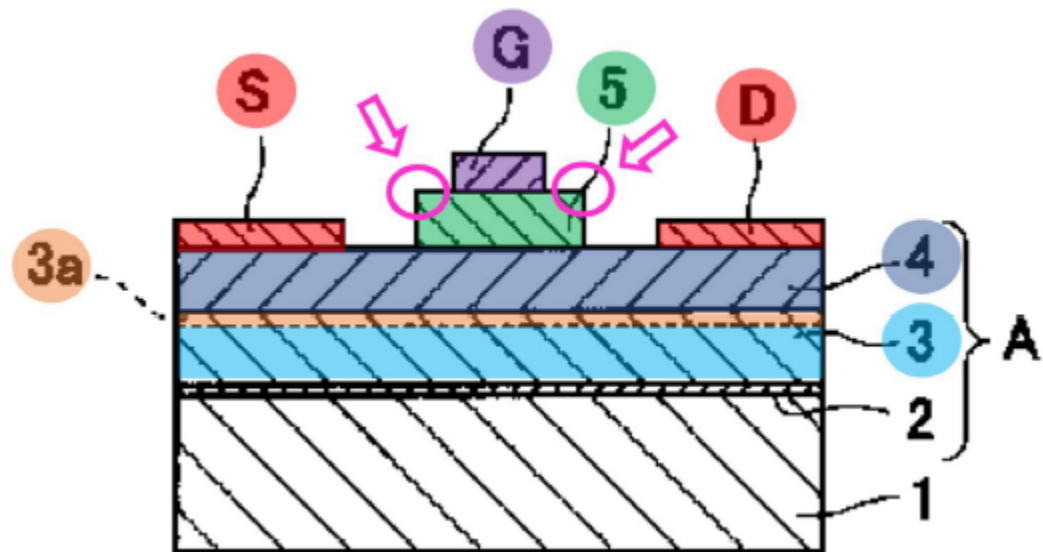
Claim 3 depends from claim 1 and further requires that the pair of ledges are self-aligned. Ex. 1001, 5:19–20. Petitioner asserts that claim 3 would have been obvious over Saxler, Beach, and Shenoy. Pet. 49–50. Petitioner asserts that Beach performs the same self-aligned process taught in the '347 patent. Pet. 49–50 (citing Ex. 1009 ¶¶ 32–33, 40, Figs. 1, 2E–2F; Ex. 1003 ¶ 130; Ex. 1009, 2–3; Ex. 1001, 4:8–33). Petitioner further asserts Shenoy's method of etching a photomask to isotropically undercut the metal layer below the photomask is the same process depicted in Figures 6B–6C of the '347 patent. Pet. 49–50 (citing Ex. 1009, 2–3; Ex. 1001, 4:17–33; Ex. 1003 ¶ 130; Pet. 29–35). Petitioner asserts that it would have been obvious to use Beach's self-alignment method and Shenoy's undercutting techniques to predictably make Saxler's gate structure, which would improve alignment. Pet. 50 (citing Ex. 1003 ¶ 131; Pet. 31–35).

Patent Owner does not address Petitioner's arguments with respect to claim 3, apart from its arguments related to independent claim 1, addressed above. We have reviewed Petitioner's arguments and evidence and determine Petitioner has shown sufficiently, at this stage of the proceeding, that Saxler, Beach, and Shenoy teach or suggest all of the limitations of claim 3 and that a person of ordinary skill in the art would have had reason to combine the teachings of the asserted art. Accordingly, we determine that Petitioner has demonstrated a reasonable likelihood of showing that claim 3 would have been obvious over Saxler, Beach, and Shenoy.

E. Claims 1–3 – Alleged Obviousness over Saxler, Yoshida, Beach, Shenoy (Ground 2)

Petitioner contends that claims 1–3 of the '347 patent are unpatentable as obvious over Saxler in view of Yoshida, Beach, and Shenoy. Pet. 50–59; Reply 1–8. Patent Owner opposes. Prelim. Resp. 28–32; Sur-reply 1–4.

Petitioner states that Yoshida discloses stacked gate structures such as the one shown below in Yoshida Figure 1A, with Petitioner's color annotations added.



Petitioner's color annotated version of Yoshida Figure 1 shows a cross-sectional view of a transistor having GaN layer 3 (highlighted in light blue) and n-type semiconductor layer 4 (highlighted in dark blue) formed over barrier layer 2 and substrate 1, with 2DEG 3a (highlighted in orange) forming at the interface of layers 3 and 4. Pet. 50–51; Ex. 1006 ¶ 10, 13, 15, 19. Petitioner also states Figure 1 depicts source contact S and drain contact D (both highlighted in red) and a stacked gate structure above semiconductor layer 4 consisting of gate metal G (highlighted in purple) overlaying doped

GaN layer 5 (highlighted in green). Pet. 50–51 (citing Ex. 1006, code (57), ¶ 9).

Petitioner contends that implementing Yoshida’s non-recessed gate structure in Saxler’s stacked gate structure would result in the same arrangement as Saxler’s non-recessed embodiment shown in modified Figure 1A of Saxler. Pet. 51–52.

Petitioner contends that it would have been obvious to combine Saxler’s stacked gate structure with Yoshida’s non-recessed gate structure because, (1) a person of ordinary skill in the art would have been familiar with a wide variety of stacked gate structures in GaN HEMT devices, including many without recessed gates, (2) Saxler repeatedly teaches that its gate recess is optional, and (3) a person of ordinary skill in the art would have removed Saxler’s gate recess to “turn Saxler’s device into an enhancement mode device, thus realizing the benefits of reduced power consumption and suitability for high power applications.” Pet. 52–55.

Petitioner also contends a person of ordinary skill in the art would have been motivated to use Yoshida’s non-recessed gate fabrication techniques to simplify manufacturing and decrease costs. Pet. 54. In particular, Petitioner contends that creating a gate recess requires complicated and exacting manufacturing processes which raises costs. Pet. 55. Petitioner asserts that a person of ordinary skill in the art would have been familiar with methods for making stacked, stepped gate structures, and would have understood that these techniques are less complicated and cost less than methods for making recessed gate structures. Pet. 55.

Accordingly, Petitioner argues that a person of ordinary skill in the art would have “found the combination of *Yoshida*’s non-recessed gate arrangement in Saxler’s gate arrangement nothing more than the simple substitution of known elements to predictably yield an enhancement mode GaN HEMT device.” Pet. 56.

Petitioner asserts that it would have been obvious to use the methods of Beach and Shenoy to fabricate the Saxler-Yoshida gate structure for the same reasons set forth in ground 1 for making the non-recessed Saxler structure of modified Figure 1A. *See, e.g.*, Pet. 56 (staging the combination of Saxler-Yoshida with Beach and Shenoy would have been obvious to predictably improve gate alignment and symmetry while reducing manufacturing steps and costs); Ex. 1003 ¶¶ 90–98, 150.

Patent Owner responds that the side surfaces of Yoshida’s p-type GaN layer are vertical, and therefore cannot teach or disclose the formation of side surfaces that extend horizontally towards the source and drain contact as claim 1 requires. Prelim. Resp. 28–31. This argument, however, does not address the full scope of Petitioner’s arguments as Petitioner does not rely on Yoshida’s structure alone to satisfy this limitation. Rather, Patent Owner is relying on the combination of Yoshida and Saxler, which Petitioner asserts discloses the formation of side surfaces that extend horizontally towards the source and drain contacts.

Patent Owner also contends that a person of ordinary skill in the art would not have been motivated to combine the teachings of Saxler and Yoshida. Prelim. Resp. 31–32. Patent Owner contends that Saxler and Yoshida are substantially different, as Saxler is directed to a device that is inoperable in enhancement mode, whereas Yoshida is directed to forming an

enhancement mode device and Petitioner provides no motivation as to why a POSITA would have incorporated features from Saxler's device, which cannot operate in enhancement mode, into Yoshida's preexisting operable enhancement mode device. Prelim. Resp. 31–32.

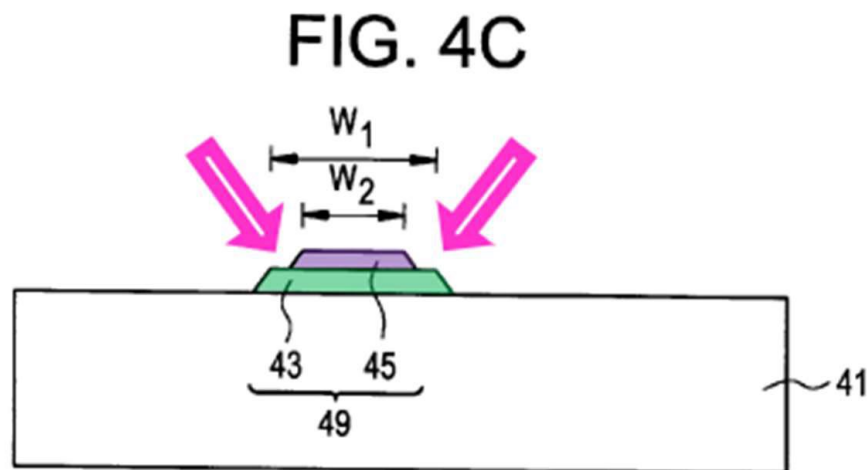
As discussed above, Petitioner provides sufficient argument and evidence that Saxler teaches or suggests an operable enhancement mode device. *See* § II.D.1 *supra*. Additionally, Patent Owner's argument regarding modifications that “could be detrimental” to certain devices is not only speculation, but also comprised entirely of attorney argument. *See* Prelim. Resp. 32. Finally, Patent Owner does not directly address Petitioner's arguments and accompanying evidence that a person of ordinary skill in the art would have had reason to combine the teachings of Saxler and Yoshida to take advantage of simplified manufacturing steps and reduced costs.

Based on the present record, Petitioner has sufficiently shown that Saxler, Yoshida, Beach, and Shenoy disclose or suggest all of the limitations in independent claim 1 and dependent claims 2–3 and that a person of ordinary skill in the art would have had a reason to combine the teachings of the asserted art with a reasonable expectation of success. Pet. 50–60 (citing, *inter alia*, Ex. 1003 ¶¶ 134–150, 167). Patent Owner's arguments to the contrary raise issues best resolved on a full record. Accordingly, we determine Petitioner has established a reasonable likelihood of prevailing on its challenge that claims 1–3 are unpatentable as obvious in view of Saxler, Yoshida, Beach, and Shenoy.

*F. Claims 1–3 – Alleged Obviousness over Saxler and Ahn
(Ground 3)*

Petitioner contends claims 1–3 of the '347 patent are unpatentable as obvious over Saxler and Ahn. Pet. 60–72; Reply 1–8. Patent Owner opposes. Prelim. Resp. 32–36; Sur-reply 1–4.

Petitioner asserts that the combination of Saxler and Ahn would yield the same structure as that shown in Saxler's modified Figure 1A. Pet. 62. Petitioner asserts that Saxler discloses steps [1a]–[1e] for the same reasons set forth with respect to ground 1 and that Saxler and Ahn render obvious steps [1f]–[1i]. Pet. 64–72. Petitioner asserts that Ahn teaches using a single mask with isotropic and anisotropic etching to create stacked gate structures having stepped features and sloped sidewalls. Pet. 60 (citing Ex. 1010, code (57), 3:41–58, 6:15–26, 7:7–14, Figs. 4A–4C; Ex.1003 ¶169). Ahn's Figures 4A–4C, with Petitioner's annotations added, are reproduced below.



Ahn Figure 4C is a diagram illustrating part of a process for fabricating a thin-film transistor, with color annotations added by Petitioner. Ex. 1010, 4:14–16.

Petitioner asserts that Ahn teaches using a single photomask to etch Ahn's top gate metal layer (purple) and underlying layer (green) to have sloped sidewalls and a pair of horizontal ledges (pink arrows) on either side of the top gate material (purple). Pet. 60 (citing Ex. 1010, code (57), 3:41–58, 6:15–26, 7:7–14, Figs. 4A–4C; Ex. 1003 ¶ 169). Petitioner asserts that its layers are symmetric and their side surfaces preferably have an inclined shape. Pet. 60 (citing Ex. 1010, 6:12–37, Fig. 4C; Ex. 1003 ¶ 169).

Petitioner asserts that it would have been obvious to make Saxler's non-recessed stacked gate structure using Ahn's method of forming a transistor gate. Pet. 62–64. Petitioner contends that a POSITA would have been motivated to use a single mask as taught by Ahn, in place of Saxler's two mask process, to simplify the process and reduce costs. Pet. 63 (citing, *inter alia*, Ex. 1003 ¶ 91; Ex. 1007 ¶¶ 65–66).

Petitioner further asserts that there were many known ways to create Saxler's stepped gate structure in its non-recessed embodiments and a POSITA would have used these methods interchangeably. Pet. 63 (citing Ex. 1003 ¶¶ 173–174). Petitioner again asserts that the '347 patent was allowed without disclosing any particular method to obtain the claimed ledges because their manufacture was within the skill level of a POSITA. Pet. 63 (citing Ex. 1002, 25–30, 44–45, 74–76, 80–99; Ex. 1003 ¶¶ 57–63).

Petitioner asserts that Ahn teaches a number of ways to obtain the non-recessed Saxler gate, including use of multiple and single masks, but teaches that its single-mask method, which etches both layers simultaneously with a solution that etches the top layer more quickly, is preferred because it leads to symmetrically-aligned layers with ledges of substantially the same width for best results. Pet. 64 (citing Ex. 1010, 4:52–

49, 5:55–62, 6:27–37, 7:15–46, Fig. 4C; Ex. 1003 ¶ 175). Petitioner asserts that it would have been a simple substation of Ahn’s known methods that would be predictably implemented in Saxler’s flexible method of manufacturing to improve alignment and symmetry between layers while reducing manufacturing steps and costs. Pet. 64 (citing Ex. 1003 ¶ 176).

We have reviewed Petitioner’s arguments and evidence and determine that, at this stage of the proceeding, Petitioner has sufficiently shown that claim 1 would have been unpatentable over Saxler and Ahn, notwithstanding Patent Owner’s arguments to the contrary, which we now address.

Patent Owner asserts that neither Saxler nor Ahn teach forming side surfaces extending horizontally towards the source and drain contacts, respectively, and contacting the barrier layer as required by claim 1.

Prelim. Resp. 32–33. Patent Owner relies on its arguments made regarding Saxler for ground 1 and further asserts that Ahn’s gate material is formed from *a double undoped metal layer* that is covered by a later-formed gate oxide layer, and therefore does not disclose any p-type gate material.

Prelim. Resp. 33–34 (citing Ex. 1010, 5:41–47, Fig. C).

Patent Owner’s argument, however, attacks each reference individually and does not address the full scope of Petitioner’s arguments, which rely on the combined teachings of Saxler—teaching depositing a gate metal on top of a p-type gate material—with Ahn’s method of etching a top gate metal layer and its underlying layer using a single photomask. Pet. 60–70. Petitioner asserts that Ahn’s method etches both layers such that each layer has sloped sidewalls and the underlying layer has ledges as recited in steps [1g]–[1i]. Pet. 60–70.

Patent Owner also asserts that Ahn is non-analogous art and may not be combined with Saxler because Ahn is directed to thin film transistors (a different technology) in liquid crystal displays (a different application), which is substantially different from the gate material of the '347 patent. Prelim. Resp. 35.

This argument is not persuasive on the present record. Petitioner states that the '347 patent generally relates to transistors and broadly defines the pertinent field as “layered semiconductors that include various field effect transistors.” Reply 4–5 (citing, *inter alia*, Ex. 1001, 1:20–58). Petitioner asserts that Ahn also involves etching metals in semiconductors, which is from the same field of endeavor as the '347 patent. Reply 6. Petitioner also asserts that Ahn discloses etching methods that can improve gate metal positioning relative to the underlying layer while reducing costs and is thus reasonably pertinent to the particular problem of gate leakage addressed by the '347 patent. Reply 6 (citing Ex. 1003 ¶¶ 169–176, 238–244). Thus, based on the present record, Petitioner’s evidence and arguments sufficiently show that Ahn and the '347 patent are analogous art. Patent Owner’s arguments to the contrary raise issues best resolved on a full record.

Patent Owner also asserts that Petitioner has not established a sufficient reason why a POSITA would have applied Ahn’s metal etching technique to a gate structure comprised of a metal and *p-type material*, absent impermissible hindsight. Prelim. Resp. 36. While we do have concerns regarding Petitioner’s asserted reasons to combine Saxler and Ahn, Petitioner has presented arguments and evidence that (1) a POSITA would have understood that Saxler’s cap layer, which is a p-type doped

semiconductor, would have a slower rate of dissolution than its metallic gate contact, (2) a POSITA would have found it obvious to use Ahn's approach to arrive at a non-recessed, stepped gate structure, and (3) that the simple substitution of Ahn's known methods could be predictably implemented in Saxler's flexible method of manufacturing to improve alignment and symmetry between layers while reducing manufacturing steps. Pet. 64 (citing Ex. 1003 ¶ 175). Patent Owner's arguments to the contrary raise issues best resolved on a full record.

Based on the present record, Petitioner has provided sufficient evidence and argument for purposes of institution that Saxler and Ahn disclose or suggest all of the limitations of claim 1 and that a POSITA would have had a reason to combine the teachings of Saxler and Ahn with a reasonable expectation of success. Accordingly, based on the present record, Petitioner has demonstrated a reasonable likelihood of showing that claim 1, as well as claims 2–3, which Patent Owner does not separately dispute, are unpatentable over Saxler and Ahn.

G. Claims 1–3 – Alleged Obviousness over Yoshida, Saxler, Beach, and Shenoy (Ground 4)

Petitioner asserts that claims 1–3 would have been obvious over the combination of Yoshida, Saxler, Beach, and Shenoy. Pet. 72–95; Reply 1–8. Patent Owner opposes. Prelim. Resp. 36–38; Sur-reply 1–4.

Petitioner provides arguments and evidence as to how the art teaches or suggests each limitation of claim 1. For example, Petitioner asserts that Yoshida or Yoshida and Saxler teach forming a GaN layer and a barrier layer, depositing source and drain contacts on the barrier layer, and depositing a p-type gate material and a gate metal as recited in steps [1a]–

[1e]. Pet. 80–84. Petitioner further asserts that although Yoshida does not expressly disclose forming a photo resist on the gate layer and etching the gate metal that, as explained for ground 1, a POSITA would have found it obvious to mask and etch the gate metal in view of Saxler to precisely and reliably position the gate metal. Pet. 86–87 (citing Ex. 1003 ¶ 219).

Petitioner further asserts that it would have been obvious to make the Yoshida-Saxler gate structure with Beach’s and Shenoy’s approach to use a single photomask over the gate metal with isotropic etching for the same reasons asserted with respect to ground 1. Pet. 87–88. With respect to step [1h], which requires etching the gate metal to form a pair of ledges on the p-type gate material below, Petitioner asserts that it would have been obvious to combine Saxler’s sloped sidewalls of the cap layer into Yoshida’s p-type layer so that they horizontally extend toward the source and drain contacts in the Yoshida-Saxler device such that the bottom of the p-type gate material is more than 10% wider than the top. Pet. 88–89. Petitioner also asserts that it would have been obvious to make the Yoshida-Saxler gate structure with Beach’s approach of using a single photomask over the gate metal to reduce gate leakage. Pet. 73–76, 90–92.

Petitioner also asserts that Yoshida alone teaches sloped sidewalls that extend horizontally towards the source and drain under Patent Owner’s claim construction because a POSITA would have known that sidewalls drawn vertically would have a slight slope when built in a practical device. Pet. 90–91 (citing Ex. 1007 ¶ 42; Ex. 1020 (“Uemoto¹⁰”), Figs. 1–2, 5;

¹⁰ Uemoto et al., *A Normally-off AlGaIn/GaN Transistor with $R_{on}A=2.6\Omega\text{cm}^2$ and $BV_{ds}=640\text{V}$ Using Conductivity Modulation*, IEEE Paper, 2006 (Ex. 1020).

Ex. 1003 ¶ 230). As an example, Petitioner asserts that Uemoto depicts its p-AlGa_N gate layer having vertical sidewalls in its drawings (e.g., Figure 1), but shows sloped sidewalls in an image of a device built according to the drawings. Pet. 90–92 (citing Ex. 1020, Figs. 1, 2, 5; Ex. 1003 ¶ 230).

Patent Owner responds that, for the reasons set forth in ground 1, Saxler, Beach and Shenoy do not teach forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts and contact the barrier layer as required by claim 1 and Yoshida does not remedy this deficiency. Prelim. Resp. 28–31. Patent Owner also asserts that Yoshida’s side surfaces do not extend horizontally and that there is no motivation to combine Saxler with Yoshida, Beach, or Shenoy. Prelim. Resp. 30–32.

Patent Owner’s arguments raise issues best resolved on a full trial. While we do have some concern’s regarding Petitioner’s asserted reasons to combine all of the prior art references, we have reviewed Petitioner’s arguments and evidence and determine that Petitioner has sufficiently shown, at this stage of the proceeding, that Yoshida, Saxler, Beach, and Shenoy teach or suggest the limitations of claim 1 and that a POSITA would have had a reason to combine the teachings of the asserted art to take advantage of Saxler’s sloped sidewalls and for the asserted benefits of using a single photoresist. With respect to Patent Owner’s contention that Yoshida’s side surfaces are vertical and cannot extend horizontally, Petitioner has directed us to at least some evidence in Saxler and Uemoto, as well testimony from Dr. Shealy, to support its position. *E.g.*, Pet. 90–91 (citing Ex. 1007 ¶ 42; Ex. 1020, Figs. 1–2, 5; Ex. 1003 ¶ 230). Accordingly, we determine that Petitioner has demonstrated a reasonable likelihood of

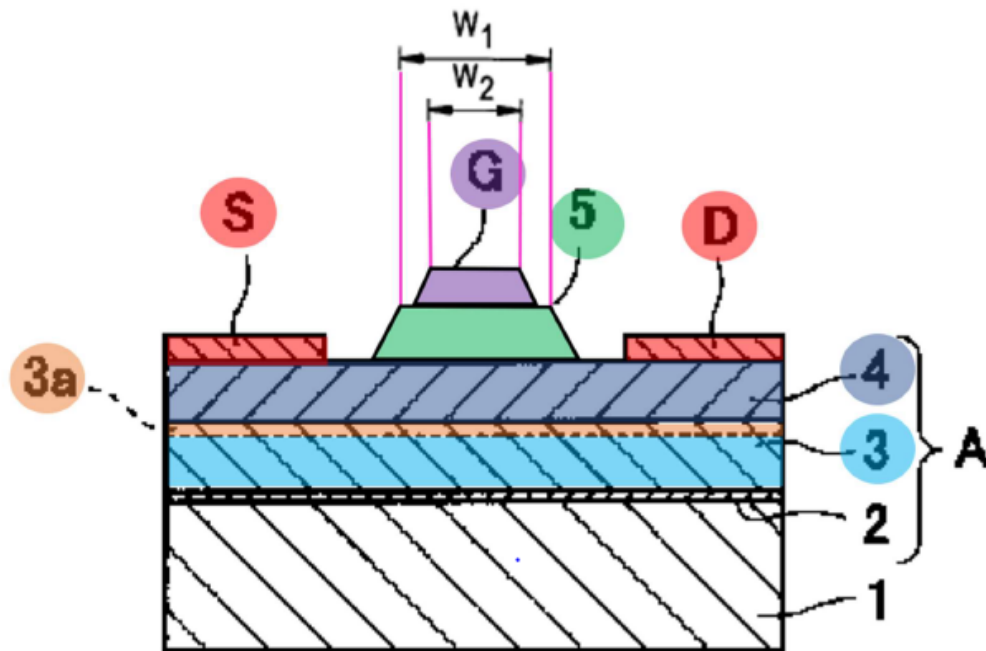
showing that claim 1, as well as claims 2–3 which Patent Owner does not separately dispute, are unpatentable over Yoshida, Saxler, Beach, and Shenoy.

*H. Claims 1–3 – Alleged Obviousness over Yoshida and Ahn
(Ground 5)*

Petitioner asserts that claim 1 would have been obvious over Yoshida and Ahn. Pet. 95–104. Patent Owner opposes. Prelim. Resp. 38–39.

Petitioner asserts that Yoshida teaches the preamble and steps [1a]–[1e] and that Yoshida and Ahn render obvious steps [1f]–[1i]. Petitioner asserts that a POSITA would have found it obvious to use Ahn’s techniques to self-align Yoshida’s p-type material and gate metal and to isotropically etch the gate metal using a single mask to obtain the gate structure of Yoshida. Pet. 95 (citing Ex. 1003 ¶¶ 238–262). Petitioner asserts that Ahn teaches either simultaneously etching the layers or etching them sequentially using combinations of wet and dry etching techniques, as well as exploiting differences between rates of dissolution of its layers to make the top gate layer narrower than the bottom. Pet. 98 (citing Ex. 1010, code (57), 3:41–58, 6:15–26, 7:7–46, 4A–4C; Ex. 1003 ¶¶ 244, 239); *see also* Pet. 98–99 (stating a POSITA would have understood that Yoshida’s p-type doped layer 5 would have a slower rate of dissolution than its metallic gate contact). Petitioner asserts that it would have been obvious to use Ahn’s approach as a simple substitution of Ahn’s known methods that would be predictably implemented when making Yoshida’s device to improve alignment and symmetry between layers. Pet. 98–99 (citing Ex. 1003 ¶ 244). Petitioner also asserts that Ahn’s etching processes create ledges that improve performance and prevent deterioration and that it would have been obvious

to use Ahn's technique to make Yoshida's stacked gate structure to improve alignment and precision. *E.g.*, Pet. 95, 99 (citing, *inter alia*, Ex. 1003 ¶¶ 243, 244). Petitioner contends that using Ahn's method to create Yoshida's gate structure would result in the device, illustrated below, which is substantially the same as Yoshida's original device, but has widths W_1 and W_2 and inclined sidewalls. Pet. 96–97.



Yoshida, Fig. 1 (modified).

The figure above is Petitioner's representation of Yoshida's Figure 1, modified so that gate electrode G (purple) and p-type GaN layer 5 (green) each have inclined sidewalls and to provide color annotations. Compare Pet. 96 with Ex. 1004, Fig. 1.

Patent Owner presents arguments that are similar to those presented for grounds 2 and 3. Prelim. Resp. 38–39. Patent Owner asserts that neither Yoshida nor Ahn teach the “forming the side surfaces” as required by claim element 1, which requires “forming side surfaces of the p-type gate material

that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer.” Prelim. Resp. 38–39. Patent Owner’s argument, however, attacks the references individually, while Petitioner relies on the combination of Yoshida and Ahn. For example, Petitioner provides argument and evidence that a POSITA would have used Ahn’s self-alignment etching technique to etch Yoshida’s gate metal layer and a p-type material and presents reasons why a POSITA would have combined the two references. Pet. 95 (citing, *inter alia*, Ex. 1003 ¶¶ 238–262); *see also* Pet. 97–98 (stating a POSITA would have found Ahn’s known methods could be predictably implemented when making Yoshida’s device to improve alignment and symmetry between the layers).

Patent Owner further contends that Ahn is directed to non-analogous art, namely thin film transistors for liquid crystal displays, and may not be combined with Yoshida, which is directed to enhancement mode transistors. Prelim. Resp. 39. As discussed above in connection with ground 3, Petitioner has sufficiently shown that Ahn is analogous art to the ’347 patent. Also, while we do have concerns regarding Petitioner’s asserted reasons to combine Yoshida and Ahn, based on the present record, Petitioner has provided sufficient evidence and argument that (1) a POSITA would have understood that Yoshida’s p-type doped layer 5 would have had a slower rate of dissolution than its metallic gate contact, (2) a POSITA would have found it obvious to use Ahn’s approach to arrive at a non-recessed, stepped gate structure, and (3) that the simple substitution of Ahn’s known methods could be predictably implemented in Yoshida’s flexible method of manufacturing to improve alignment and symmetry between layers while reducing manufacturing steps. Pet. 97–99 (citing, *inter alia*, Ex. 1003

¶¶ 241–244). Patent Owner’s arguments to the contrary raise issues best resolved on a full record.

Based on the present record, Petitioner has provided sufficient evidence and argument for purposes of institution that Yoshida and Ahn disclose or suggest all of the limitations of claim 1 and that a POSITA would have had a reason to combine the teachings of Yoshida and Ahn with a reasonable expectation of success. Accordingly, based on the present record, Petitioner has demonstrated a reasonable likelihood of showing that claim 1, as well as claims 2–3, which Patent Owner does not separately dispute, are unpatentable over of Yoshida and Ahn.

III. CONCLUSION

Because Petitioner has demonstrated a reasonable likelihood that at least one challenged claim of the ’347 patent is unpatentable over the prior art of record, we institute an *inter partes* review of all challenged claims on all asserted grounds.

At this stage of the proceeding, we have not made a final determination with respect to the patentability of any challenged claim or any underlying factual or legal issue, including claim construction.

IV. ORDER

For the reasons given, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–3 of the ’347 patent is instituted with respect to all grounds of unpatentability asserted in the Petition, commencing on the entry date of this Decision; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial.

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Patent 9,748,347 B2

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