

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01382
U.S. Patent No. 9,748,347

PATENT OWNER'S RESPONSE

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TABLE OF PETITIONER’S EXHIBIT LIST

<u>Exhibit</u>	<u>Description of Exhibit</u>
1001	U.S. Patent No. 9,748,347 B2 to Cao et al. (“the ’347 patent”)
1002	Prosecution History of the ’347 patent
1003	Declaration of Dr. James Richard Shealy
1004	Curriculum Vitae of Dr. James Richard Shealy
1005	Japanese Patent Publication No. JP H11-261053 to Yoshida
1006	Certified Translation of Japanese Patent Publication No. JP H11 261053 to Yoshida (“Yoshida”)
1007	U.S. Patent Application Publication No. US 2006/0108606 A1 to Saxler et al. (“Saxler”)
1008	U.S. Patent Application Publication No. US 2007/0007547 A1 to Beach (“Beach”)
1009	R.V. Shenoy and M. Datta, Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining, 143 J. Electrochemical Soc’y, pp. 544-549 (1996) (“Shenoy”)
1010	U.S. Patent No. 5,905,274 to Ahn et al. (“Ahn”)
1011	U.S. Patent Application Publication No. US 2010/0258843 A1 to Lidow et al. (“Lidow”)
1012	RESERVED
1013	RESERVED
1014	Chua Xu et al., <i>The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure</i> , 28 IEEE Electron Device Letters, pp. 942-944 (2007) (“Xu”)

1015	U.S. Patent Application Publication No. US 2002/0066908 A1 to Smith (“Smith”)
1016	U.S. Patent Application Publication No. US 2006/0273347 A1 to Hikita et al. (“Hikita”)
1017	U.S. Patent Application Publication No. US 2009/0072272 A1 to Suh et al. (“Suh”)
1018	X. Hu et al., Enhancement mode AlGaIn/GaN HFET with selectively grown pn junction gate, 36 Electronics Letters, pp. 753-754 (2000) (“Hu”)
1019	U.S. Patent Application Publication No. US 2005/0087763 A1 to Kanda et al. (“Kanda”)
1020	Yasushiro Uemoto et al., <i>A Normally-off AlGaIn/GaN Transistor with $R_{onA}=2.6\Omega\text{cm}^2$ and $BV_{ds}=640\text{V}$ Using Conductivity Modulation</i> , 2006 International Electron Devices Meeting, IEEE (2006) (“Uemoto”)
1021	U.S. Patent Application Publication No. US 2006/0019435 A1 to Sheppard et al. (“Sheppard”)
1022	Order Granting Defendants’ Unopposed Motion for Stay Pending ITC Proceeding, Case No. 2:23-cv-04026-AB-AS, Central District of California (July 27, 2023)
1023	Dietrich W. Widmann, Metallization for Integrated Circuits Using a Lift-Off Technique, 11 IEEE Journal of Solid-State Circuits, pp. 466 471 (1976) (“Widmann”)
1024	RESERVED
1025	Declaration of Kelley Hayes Greenhill
1026	Declaration of Shauna Wiest
1027	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 (“Beach-II”)

1028	Petitioner and Complainant's Proposed Claim Construction, ITC 337 TA-1366
1029	C. S. Suh et al., "p-GaN/AlGaIn/GaN Enhancement mode HEMTs, 2006 64th Device Research Conference, June 2006, pp. 163-164 ("Suh 2006")
1030	Excerpt of the Declaration of Dr. Eric Fred Schubert in Support of Complainant's Opening Claim Construction Brief
1031	Excerpt of Complainant's Supplemental Responses to Respondent's Supplemental Invalidity Contentions

TABLE OF PATENT OWNER'S EXHIBIT LIST

<u>Exhibit</u>	<u>Description of Exhibit</u>
2001	Patent Owner's Notice of Deposition of Dr. James Shealy
2002	Diagram produced by Dr. James Shealy during Deposition on May 16, 2024
2003	Diagram produced by Dr. James Shealy during Deposition on May 16, 2024
2004	Certified Transcript of Oral Deposition of Dr. James Shealy
2005	Declaration of Dr. E. Fred Schubert
2006	Curriculum Vitae of Dr. E. Fred Schubert
2007	Petition for Inter Partes Review of U.S. Patent. No. 10,312,335
2008	Evidentiary Hearing Transcript, pages 741-984 (Inv. No. 337-TA-1366) (Public)
2009	Respondents' Post-Hearing Initial Brief (Inv. No. 337-TA-1366)

I. INTRODUCTION

On March 26, 2024, the Board issued a Decision (Paper 11) granting *inter partes* review of claims 1-3 of U.S. Patent No. 9,748,347 (“the ’347 patent”) on each of five grounds raised by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (“Petitioner”).

All grounds raised in the Petition (Paper 1) allege obviousness of the challenged claims. Each of the grounds (as summarized below) rely on at least one of two primary references – either U.S. Patent Application Publication 2006/0108606 (“Saxler”)¹ and/or Japanese Publication 2290799 (“Yoshida”)² – in addition to a combination of U.S. Patent Application Publication 2007/0007547 (“Beach”)³ and non-patent literature entitled “*Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*” (“Shenoy”)⁴ or U.S. Patent 5,905,274 (“Ahn”)⁵. Each of the grounds is fatally flawed and must be rejected, as discussed herein.

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	Saxler, Beach, and Shenoy
2	1-3	§ 103	Saxler, Yoshida, Beach, and Shenoy
3	1-3	§ 103	Saxler and Ahn
4	1-3	§ 103	Yoshida, Saxler, Beach, and Shenoy

¹ Ex. 1007.

² Ex. 1006.

³ Ex. 1008.

⁴ Ex. 1009.

⁵ Ex. 1010.

5	1-3	§ 103	Yoshida and Ahn
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The Petition is tainted by obvious hindsight to combine disparate prior art references to allegedly achieve the claimed methods, without *ever presenting a description of the actual proposed modified prior art process*. Rather, Petitioner simply picks and chooses different *elements* of the prior art and abstractly asserts that the combination renders the claims obvious, without explaining how the proposed combination would fit into an overall process to arrive at the claimed invention.

Using the claim as a roadmap, Petitioner attempts to “mix and match” disparate references dealing with different devices having different materials and serving different purposes to allegedly render claim 1 obvious. Petitioner fails to provide sufficient motivation to combine, modify, and rearrange these references other than to allege that the references could be combined to reverse engineer the claimed invention; nowhere, however, does Petitioner explain why a POSA *would* have combined, modified, or rearranged the teachings of the references. “[O]bviousness concerns whether a skilled artisan not *only could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis in original). Moreover, “[c]ombining prior art references without evidence of such a suggestion, teaching, or motivation simply

takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight.” *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999).

In *InTouch*, the Federal Circuit vacated a finding of invalidity because the defendant’s expert opined that the elements of the claim existed in the prior art but failed to explain how to combine the elements:

Dr. Yanco’s testimony was nothing more than impermissible hindsight; she opined that all the elements of the claims disparately existed in the prior art, but failed to provide the glue to combine these references. While she opined that the references were like separate pieces of a simple jigsaw puzzle, she did not explain what reason or motivation one of ordinary skill in the art at the time of the invention would have had to place those pieces together.

Id. at 1348-49.

In this case, Petitioner does not explain how the pieces of the puzzle fit together, much less why a POSA would have been motivated to combine the pieces. Petitioner goes from one limitation to the next, picking and choosing the reference it is relying on to meet that limitation without tying any motivation to the particular references and their processes or explaining how the “pieces of the jigsaw” actually even fit together to allegedly achieve the elements of the claim. EX2001 ¶135. Simply put, even if one were to have been motivated to combine the references identified by Petitioner, because Petitioner failed to particularly explain the

combination, it is impossible to determine whether a POSA would have expected to successfully combine the references, and whether that unidentified process flow would yield an operable device. This is exactly why the Board should sustain the patentability of the claims.

II. BACKGROUND

A. The '347 Patent

The '347 Patent issued on August 29, 2017, from an application filed on July 30, 2014. The '347 Patent claims priority to a United States Provisional Application No. 61/860,976 and is a continuation-in-part of U.S. Patent No. 8,890,168 that is a divisional of U.S. Pat. No. 8,404,508 that claims priority to U.S. Provisional Application No. 61/167,777, which was filed on April 8, 2009.

The '347 Patent describes and claims a *method* for forming an *enhancement-mode* GaN (Gallium Nitride) MISFET (Metal Insulator Semiconductor Field Effect Transistor) with self-aligned ledges. The claims are distinguishable from, and do not read on, methods for manufacturing depletion-mode transistors. *See* EX1001 1:45-58. As Dr. Schubert explains, the two devices operate differently. EX2005 ¶35. While enhancement-mode devices are turned on with the application of a positive bias, depletion-mode devices are turned off with the application of a negative bias. *Id.* As such, the material layers are different and serve different purposes. *Id.*

The '347 Patent is specifically directed to reducing the gate current between the gate and the 2DEG region of an enhancement-mode GaN transistor. EX1001 1:20-22. The '347 patent explains that prior art enhancement-mode GaN high electron mobility transistors (HEMT) have unacceptably high gate leakage current. Referring to Figure 2 (prior art), the '347 patent explains that gate leakage occurs between the gate contact above gate material 101 and the 2DEG region 102 below and adjacent to the gate material along gate leakage current paths 201 (along the sidewalls of gate material 101) and 202 (through the bulk of gate material 101). *Id.* at FIG. 2 (reproduced below), 1:64-2:3.

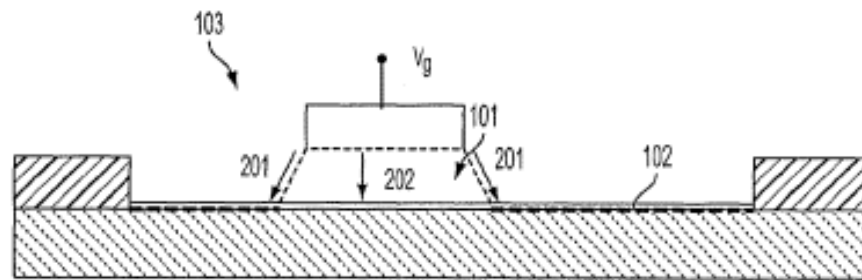


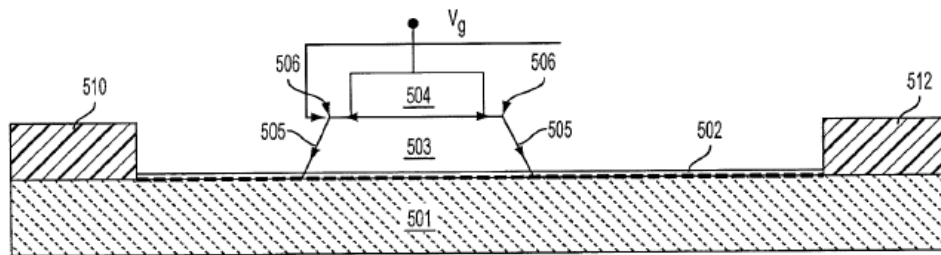
FIG. 2
PRIOR ART

EX1001, Fig. 2

The gate leakage current of the prior art structure occurs predominantly along gate leakage current path 201, e.g., along the edge of the gate material. *Id.* FIGs. 3A, 3B, and 4 (demonstrating that an increased number of gate p-type semiconductor sidewall edges increases the gate leakage current).

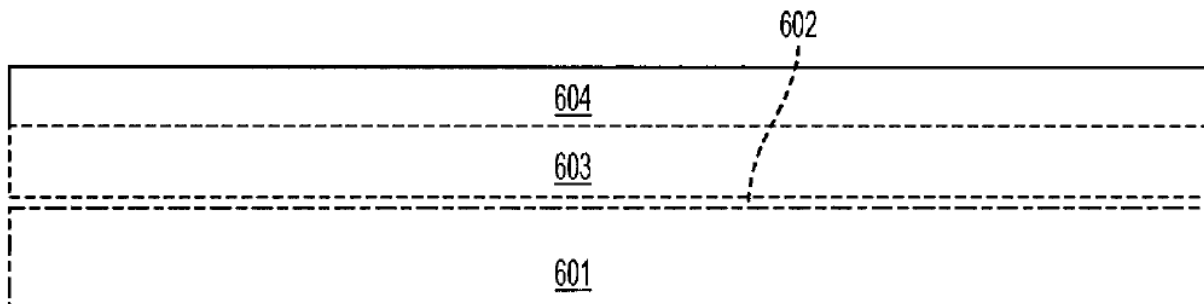
GaN FETs are known for their ability to carry greater current and withstand

higher voltages than their silicon counterparts. EX2005 ¶28, 39. In particular, the '347 Patent claims a method of making a device having a gate structure with an elongated surface length that reduces the gate leakage from the device. *Id.* ¶¶39, 41-46. Due to the enhanced surface length of the elongated ledges and sidewalls of the device, gate leakage is reduced during operation. *Id.* ¶39, 47. In accordance with the '347 Patent, gate leakage current is reduced by lengthening the gate leakage current path at the edges of the gate p-type semiconductor material by including a pair of ledges that extend horizontally towards the source and drain contacts, as shown in Fig. 5 (reproduced below). *Id.* ¶39. The '347 Patent describes a self-aligned process for forming the ledges. EX1001 at 2:41-43.



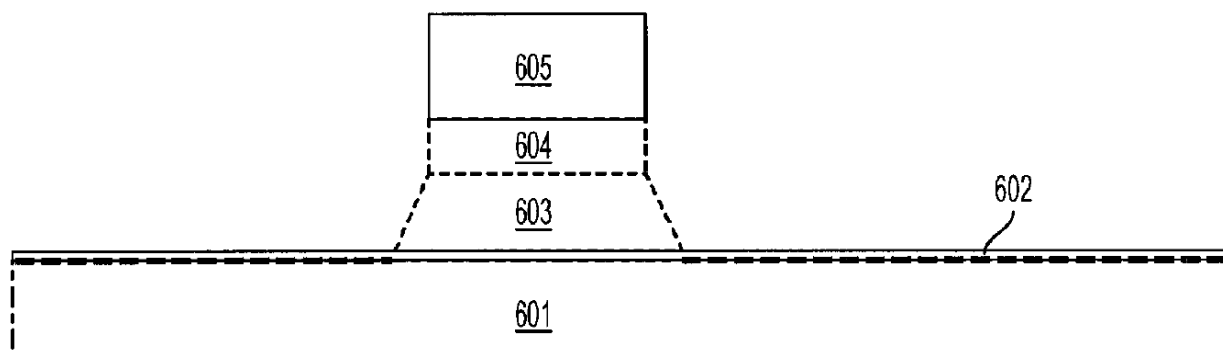
EX1001, Fig. 5

As shown in FIG. 6A (below), the base structure of the device is first formed with a base layer 601 of gallium nitride (GaN), a barrier layer 602 of aluminum gallium nitride (AlGaN) formed on the GaN layer 601, and a layer of p-type gate material 603 formed on the barrier layer 502, over which the gate metal 604 is deposited. *Id.* at 4:10-16.



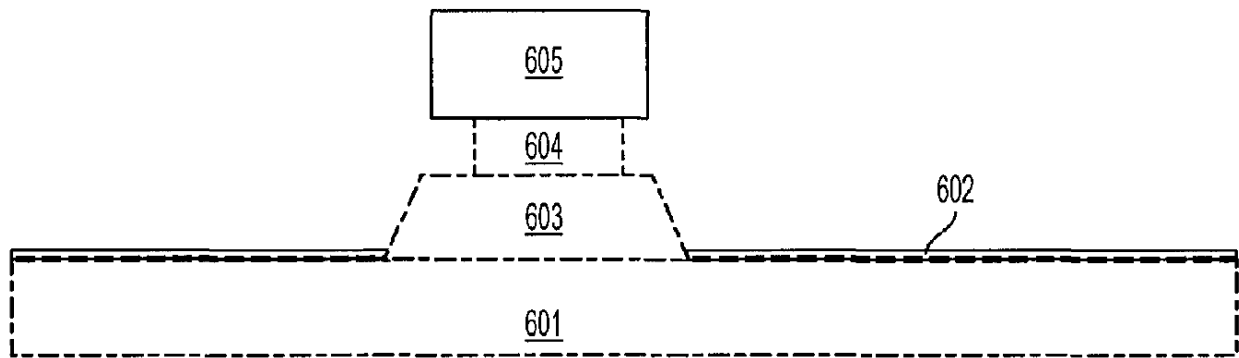
EX1001, Fig. 6A

Next, as shown in FIG. 6B (below), a photoresist 605 is deposited and the gate metal 604 is then etched. The p-type gate material 603 is also etched in a manner that results in the gate structure depicted in FIG. 6B. *Id.* at 4:17-20.



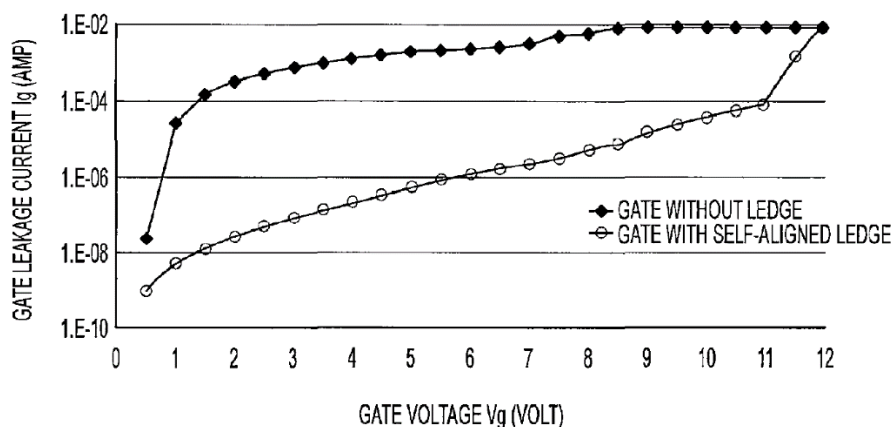
EX1001, Fig. 6B

As shown in FIG. 6C (below), the gate metal 604 is then etched, resulting in the gate metal having a cross-sectional width less than the cross-sectional width of the p-type gate material 603. This second etching step results in the formation of the ledges 506 (FIG. 5) of the p-type gate material 603. *Id.* at 4:20-25.



EX1001, Fig. 6C

Fig. 8 of the '347 patent provides data showing that the gate with self-aligned ledges has significantly lower gate leakage current than conventional gates without ledges when the transistor device is in the ON state. *Id.* at 4:41-45.



EX1001, Fig. 8

The described method is vastly superior to forming gate ledges using separate masks. In the process of using separate masks, a photoresist mask is applied to the unetched structure after the p-type gate material is deposited on the barrier layer of the device. EX2005 ¶48. In this instance, the first mask is used to pattern and etch the gate metal to a minimum CD. *Id.* A second mask is then used to pattern and

etch the p-type material with a wider CD than the gate metal. *Id.*

In a self-aligned process, such as in the '347 patent, a single photomask is used to pattern and etch more than one feature thereby resulting in a self-aligned structure in which two features are aligned with one another. EX2005 ¶49_. The self-aligned structure is achieved because the single photo-mask pattern is used to pattern the photoresist which is then used to pattern (by etching) the first layer as the etching process proceeds downward from the top of the wafer towards the substrate. *Id.* After the first layer has been etched, the photoresist can either remain or be removed because the first etched layer has now been etched to accord with the pattern transferred from the photomask. *Id.* ¶¶49-50 Then, using either the photoresist or the top layer, the second layer/feature can be etched with either the photoresist and/or the top layer/feature serving to protect the portion of the second layer/feature from being etched. *Id.* Through these steps, the top layer/feature and the second layer/feature share the same pattern from the photomask and are automatically aligned (“self-aligned”) with each other. *Id.*

The self-aligned process of the '347 patent provides multiple benefits to the transistor due to the lack of overlay errors. Due to such a process, the minimal critical dimension, e.g., the smallest dimension possible, as limited by photolithography, can be achieved for the gate contact. *Id.* at 50. Without such a process, the gate semiconductor material (or other layers) below the gate metal had

to be wider than the gate metal to accommodate for misalignment that unavoidably occurs when more than one photo-mask is used. *Id.* ¶¶48, 50.

III. CLAIM CONSTRUCTION

The preamble of claim 1 of the ‘347 patent recites “A method for manufacturing an enhancement-mode GaN transistor, comprising . . .” The body of claim 1 recites a step of “depositing a p-type gate material on the barrier layer.”

In an ITC proceeding on a related patent, Petitioner took the position that HEMT devices with a p-type gate material are enhancement mode. EX2008 at 936:17-937:2 (Lebby) (“If you design a device with p-type material as we’ve heard in this litigation, it’s enhancement-mode.”). Patent Owner agrees that this is generally true.

Accordingly, there is no dispute that claim 1 of the ‘347 patent covers “an enhancement-mode GaN transistor,” as explicitly recited in the preamble.

IV. REBUTTAL TO STATEMENT OF FACTS

Petitioner’s alleged Statement of Material Facts (Pet. 18) is materially deficient and should be ignored. Petitioner failed to include any citations to the record supporting any of its alleged facts (*see* 37 C.F.R. § 42.22(c)), and therefore, the alleged facts should not be assumed into evidence, nor is it Patent Owner’s responsibility to presuppose and rebut the unsupported allegations.

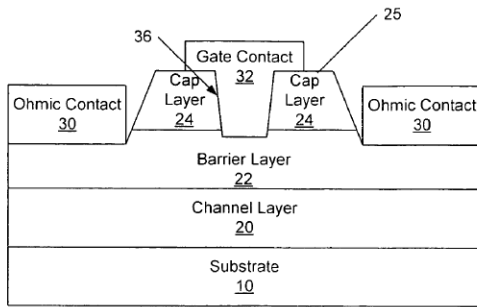
V. LEVEL OF ORDINARY SKILL IN THE ART

Based on the description in the '347 patent (and the '508 patent from which it claims priority) and the relevant art discussed during the prosecution history and cited on the patent, EPC submits that a person of ordinary skill in the art in the context of the '347 patent would have possessed at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN. EX2005 ¶20. Relevant graduate education could substitute for the professional work experience. *Id.* Dr. Schubert opines, however, that the difference between Innoscience's proposed POSA and EPC's proposed POSA would not affect the outcome of this proceeding or change his opinion in any material manner. *Id.*

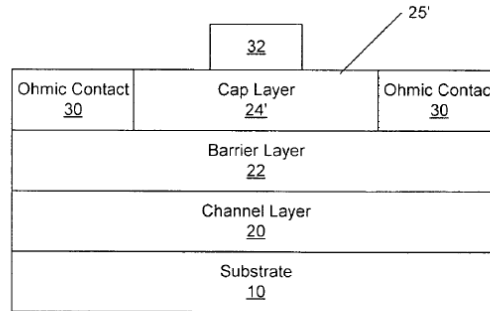
VI. OVERVIEW OF THE REFERENCES RELIED UPON BY PETITIONER

A. Saxler

Saxler describes two different high electron mobility transistors (HEMTs) – a recessed embodiment and a non-recessed embodiment. Both embodiments are depletion mode devices. EX2005 ¶54. The two embodiments are shown in Figures 1A and 1B (reproduced below).



EX1007, Fig. 1A



EX1007, Fig. 1B

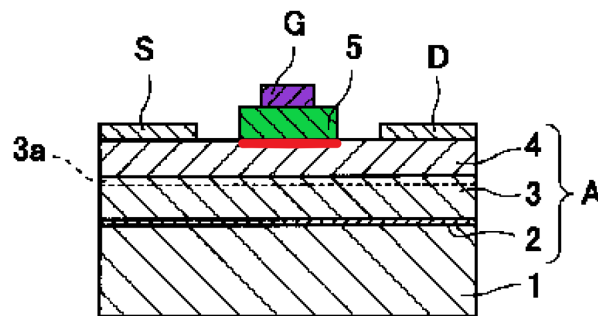
As can be seen in Fig. 1A, the cap layer 24 of the recessed embodiment has two distinct regions on either side of the gate with slanted sidewalls. In Saxler's non-recessed embodiment (Fig. 1B), the cap layer 24' is a rectangle extending from ohmic contact 30 to ohmic contact 30. Saxler describes a number of structural and functional distinctions between the recessed embodiment and the non-recessed embodiment, including the shape, thickness, doping, and function of the cap layers. EX1007, Figs. 1A, 1B, 2A, 2B, ¶¶[0007], [0012], [0014], [0027], [0062], [0070], [0071], [0073], [0074], [0076], [0081]; EX2005 ¶55. Significantly, Saxler discloses that "the regions illustrated in the figures are schematic in nature and *their shapes are not intended to illustrate the precise shape of a region of a device.*" EX1007 ¶42 (emphasis added).

Saxler describes the general knowledge of a "gate-last" fabrication process in which the cap layer is layered and etched to form the source and drain contacts, followed by the gate contact being deposited. EX1007 ¶¶[0063]-[0066]; EX2005 ¶57 (illustrating the steps of Saxler's process).

B. Yoshida

Yoshida discloses an enhancement-mode GaN HEMT having a semi-insulating substrate (1), a buffer (GaN) layer (2), an i-type semiconductor (GaN) layer (3), an n-type semiconductor (InGaN) layer (4), and a p-type GaN layer (5).

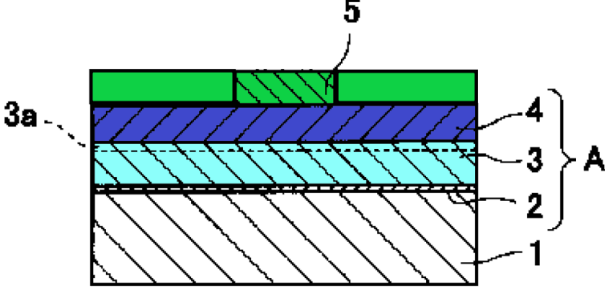
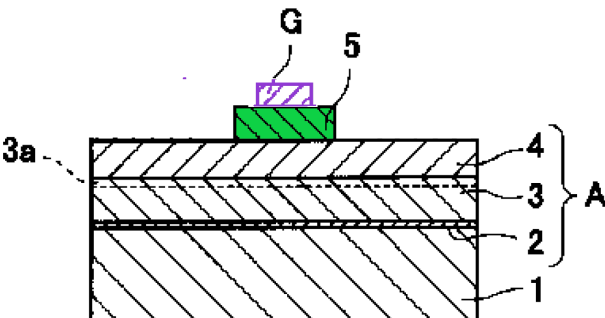
The layers are deposited to form a **pn junction** “immediately under the **gate electrode G**” to “enable[] voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility.” EX1006 ¶[0017].

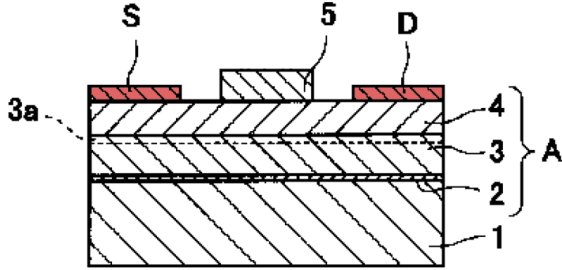
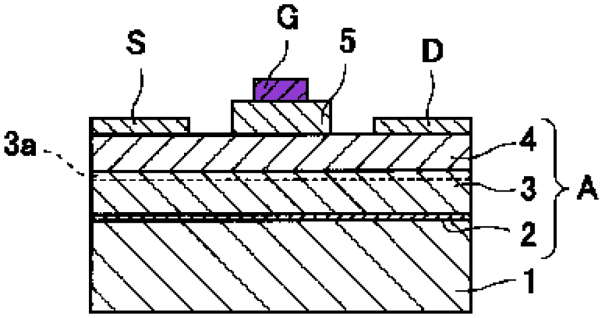


EX1007, Fig. 1(annotated)

Like Saxler, Yoshida is formed by a “gate-last” process where the **p-type GaN layer 5** is deposited and etched to form the source and drain contacts S, D before the **gate electrode G** is deposited. EX2005 ¶61. More specifically Yoshida discloses “an etchant to etch away the **p-type GaN layer** except where the **gate electrode** was to be loaded.” EX1006 ¶[0022]. As Dr. Schubert explains (EX2005 ¶61), Yoshida’s

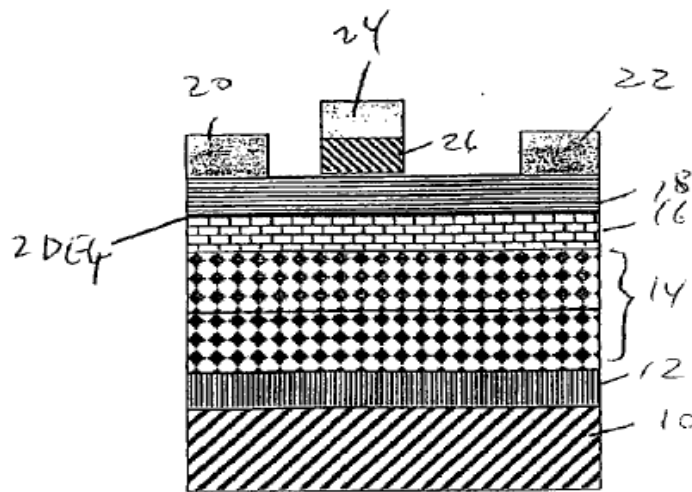
process occurs in the following specific order:

Step	Process
1	A GaN buffer layer 2, an i-type GaN layer 3, an ntype AlGaIn layer 4, a p-type GaN layer 6 are deposited through epitaxial growth. EX1006 ¶¶[0019]-[0021].  EX1006, Fig. 1 (modified)
2	Dry etching was performed to etch away the p-type GaN layer “except where the gate electrode was to be loaded and exposing the n-type InGaIn layer 4”. Ex1006 ¶[0022].  EX1006, Fig. 1 (modified)
3	An SiO₂ film is deposited to cover the entire surface, and after patterning with photoresist, the area including the part where

	the gate electrode was to be loaded was masked, leaving the portion where source and drain electrodes were to be loaded open.” EX1006 ¶[0022].
4	Al is deposited on the exposed n-type InGaN layer 4 to load source electrode S and drain electrode D. EX1006 ¶[0022].  EX1006, Fig. 1 (modified)
5	After etching away the masking and opening the SiO₂ film beneath it, the source electrode S and drain electrode G locations were masked with SiO₂ film, Au was deposited in the opening portions, and gate electrodes G were loaded above the p-type GaN layer 5. EX1006 ¶[0023].  EX1006, Fig. 1 (annotated)

C. Beach

Beach describes a III-Nitride enhancement mode semiconductor device, including a gate barrier layer under the gate. EX1008, Abs., Title. Beach describes a transistor (as shown below) including substrate 10, bonding layer 12, first III-N buffer body 14, first III-N semiconductor body 16, second III-N semiconductor body 18, first and second power electrodes 20, 22, gate barrier 26, and gate arrangement 24. *Id.* ¶¶[0031]-[0032]; EX2005 ¶62.



EX1008, Fig. 1

Beach discloses that the gate structure of gate arrangement 24 and gate barrier 26 is patterned and etched to form a self-aligned gate arrangement. EX1008, Fig 2F, ¶[0040]. Beach discloses that the gate structure is fabricated before the ohmic contacts 20, 22 are formed on the device (i.e., a “gate-first” process). *See, e.g., id.*; EX2005 ¶65.

D. Shenoy

Shenoy is an article exploring the theoretical shape evolution that occurs in through-mask electrochemical micromachining (EMM) through mathematical modeling. EX1009, Abstract. Shenoy is not directed to the formation of GaN based semiconductors and/or HEMTs. EX2005 ¶66. Shenoy further does not disclose nor suggest methods of manufacturing an enhancement-mode GaN transistor. *Id.* Shenoy further does not address self-aligned structures. *Id.*

Instead, Shenoy theoretically explores how deviations in photoresist mask wall angle affect the directionality of the subsequent etching process. *Id.* ¶67. Further, because Shenoy is based on a mathematical model, its disclosure relies upon theoretical assumptions that would not necessarily be applicable in practice, or true with respect to enhancement-mode GaN transistors and their applicable materials. *Id.* Particularly, Shenoy describes the shape of an ideal evolving EMM etching cavity but does not explicitly or implicitly instruct a POSA how to etch a GaN-based layer, any particular desired patterning designs, or methods or desires to achieve particular sidewall designs. *Id.* Instead, Shenoy is entirely ambivalent to any desired design. *Id.*

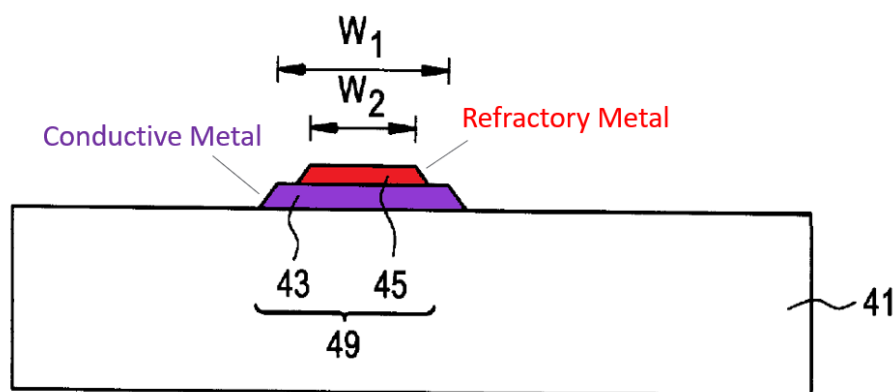
E. Ahn

Ahn is directed to thin film transistors for liquid crystal displays and discloses etching of a double-layered metal gate. EX1010, 1:5-10; 3:27-29. A thin film transistor is a special type of FET where the transistor is made by a specific thin film

deposition, diverging from GaN HEMTs. EX2005 ¶68. Because the layers are thin and they are grown on inert substrates, rather than on wafers, the semiconductor must be deposited in a dedicated process, distinct from GaN HEMTs. *Id.* The most common application for thin film transistors is in a liquid crystal display (LCD) where the transistor is embedded within the panel itself due to its low profile. *Id.*

Ahn establishes that prior art gates in LCD transistors are made of a single layer of aluminum to reduce its wiring resistance, but the single layer metal gate has an issue of causing defects such as hillock. *Id.* ¶69 (citing EX1010, 1:17-19). Thus, Ahn is specifically directed to the development of a double-layered metal gate as a substitute for a single-layered metal gate for a thin film transistor. *Id.* (citing EX1010 at 1:20-23, 3:21-26).

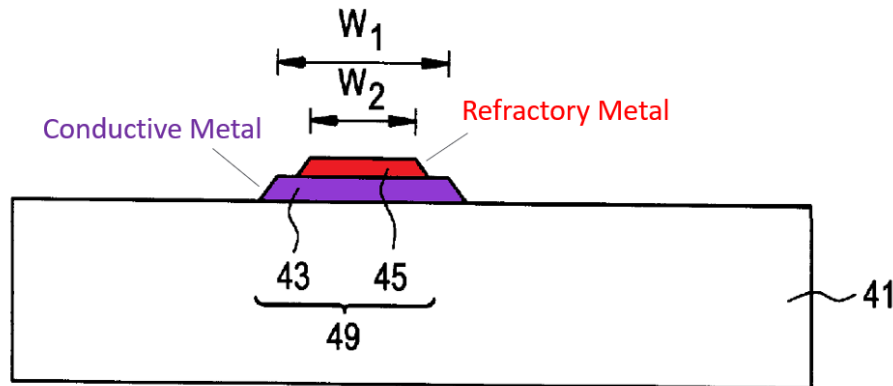
The double-layered metal is specifically made up of a bottom conductive metal layer 43 (Al, Cu, or Au) and a top refractory metal layer 45 (Mo, Ta, or Co). *Id.* ¶69 (citing EX1010 at 4:33-38).



EX1010, Fig. 4C (annotated)

As further illustrated below, the thin film transistor in Ahn has a layering structure of the double-layered gate 21 deposited on a substrate 11. EX2005 ¶71. Thin film transistors are named for the very reason that thin film transistors are constituted by thin films to enable the overlap of the gate and electrode components. *Id.* A first insulating layer 23 (“gate oxide layer”) is deposited on the double-layered gate 21. *Id.* (citing EX1010, 2:22-26). Semiconductor and ohmic contact layers 25 and 27 are formed by sequentially depositing undoped polycrystalline silicon and heavily doped silicon on the gate oxide layer 23. *Id.* (citing EX1010 at 2:26-31). Source and drain electrodes 29, 31 are layered on the semiconductor and ohmic contact layers 25 and 27, and a second insulator 33 is deposited on the entire surface of the structure. *Id.* (citing EX1010 at 2:32-36). The semiconductor contact layer 25 provides a connection between the source and drain electrodes 29, 31 that is controlled by the gate 21. *Id.* (citing EX1010 at 2:36-38; Fig. 1F). The thin film transistor is still a FET, thus the overlying gate oxide layer 23 has to be thin (on the order of 10 nm) to be sure that double-layer metal gate structure can apply a magnetic field to the semiconductor contact layer 25. *Id.*

¶73 (citing EX1010, 4:46-52).



EX1010, Fig. 4C (annotated)

The vertical arrangement, the double-layered metal gate, and the gate oxide layer of Ahn are not even remotely applicable to an enhancement mode transistor. *Id.* ¶74. Ahn does not teach or disclose the use of any p-doping in its gate material. *Id.* ¶74. Ahn’s lack of relevance to GaN transistors is further apparent from its discussion of the formation of a pixel electrode 65, “which is electrically connected to the drain electrode 59 through the contact hole 63.” *Id.* (citing EX1010, 7:4-6). That pixel electrode – not a feature of GaN transistors – is present because Ahn is directed to transistors that are used in vastly different applications, relating to liquid crystal displays. *Id.* (citing EX1010. at 1:5-10.

VII. GROUND 1 (SAXLER IN VIEW OF BEACH AND SHENOY)

A. Overview

In Ground 1, Petitioner asserts that Saxler in view of Beach and Shenoy renders obvious claims 1-3 of the ’347 Patent. Pet. 24.

Petitioner misrepresents the teachings of Saxler by “mix[ing] and match[ing]” features and parameters of two distinct embodiments (recessed and non-recessed) of Saxler to arrive at the gate structure of the ’347 patent. EX2005 ¶76.

But the hypothetical transistor proposed by Petitioner would not operate as an enhancement-mode transistor, because Saxler describes depletion-mode transistors, not enhancement-mode transistors. *Id.* ¶76.

Petitioner recognizes that Saxler does not disclose a self-aligned technique for forming its gate structure, and therefore disregards Saxler’s gate formation method and instead attempts to shoehorn the self-aligned technique of Beach, an enhancement mode transistor. Pet. 24; EX2005 ¶77. But, as explained below, using the Beach gate formation process to form Saxler’s gate would remove the portions of the cap layer 24 that Petitioner relies on for claim 1’s side surfaces. EX2005 ¶142-45. Moreover, the subsequent gate semiconductor etching process of Beach will remove the barrier layer in the source and drain regions and etch through the 2DEG and into the channel layer, resulting in a non-working device. *Id.* at ¶77.

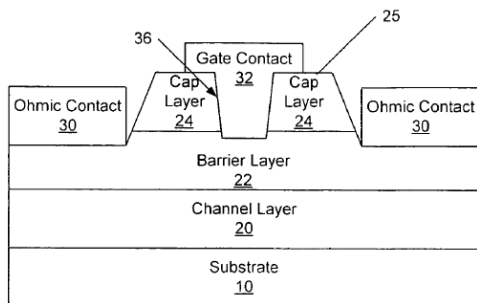
Recognizing that the Beach etching process will result in an inoperative device, Petitioner substitutes a mathematical model of EMM etching from Shenoy. Pet. 30-31; EX2005 ¶77. But Shenoy’s process is not applicable and would not work to form a transistor because it requires an insulating layer underlying the metal layer. EX2005 ¶77 Even if a POSA were to apply the EMM etching of Shenoy, it would

etch at least the claimed ledges (underlying the gate metal). *Id.* This meandering path of reengineering would not be obvious to POSA and, in any event, would not result in the claimed method. *Id.*

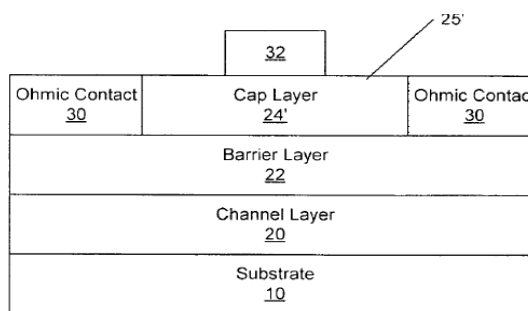
B. A POSA would not consider the gate recess of Saxler as “optional” based on Saxler’s two distinct embodiments

Petitioner alleges that “although [Fig. 1A] depicts its gate recess may separate its cap layer into two portions in some embodiments, **the recess in Saxler’s cap layer 24 is optional**, and where not employed the cap is a continuous material.” Pet. 45. The interpretation is incorrect .

Saxler discloses two distinct embodiments. A first recessed embodiment is illustrated in FIGS. 1A, 2B having a bifurcated recessed cap layer where the gate contact intersects and divides the cap layer. EX2005 ¶81. A second non-recessed embodiment is illustrated in FIGS. 1B, 2A with a non-recessed gate contact positioned on top of the cap layer. *Id.* ¶81.

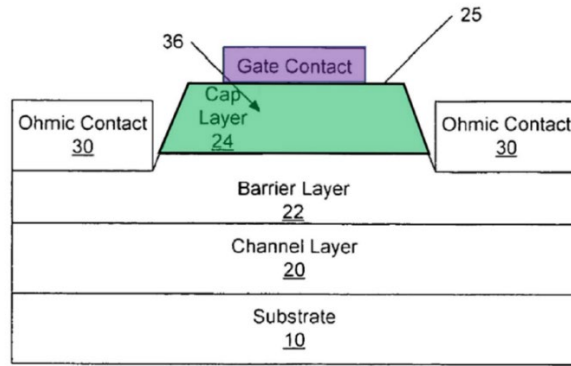


EX1007, Fig. 1A



EX1007, Fig. 1B

Petitioner’s “modified” rendition (shown below) is clearly not illustrated or supported by or suggested by Saxler. *Id.* ¶82

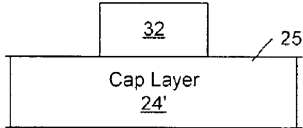
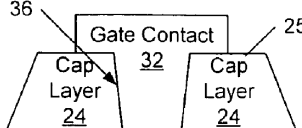


Pet. 41

Indeed, Petitioner’s cited passages of Saxler actually contradict Petitioner’s premise by highlighting the structural and functional distinction of the cap layer 24 in the recessed embodiment and the cap layer 24’ in the non-recessed embodiment. *Id.* ¶83.

For example, as relied on by Petitioner, ¶[0012] discloses “in particular embodiments of the present invention without a gate recess, the doped region extends into the cap layer from about 2.5 Å to about 50 Å” and “in particular embodiments of the present invention with a gate recess, the doped region extends into the cap layer from about 20 Å to about 5000 Å.” EX1007 ¶[0012]; EX2005 ¶84. Petitioner alleges that, because the recessed embodiment and the non-recessed embodiment are described in the same paragraph, they are structurally equivalent except for the presence of the gate recess. EX2005 ¶84. However, ¶[0012] explicitly describes the embodiments as “particular embodiments of the present invention without a gate recess” and “particular embodiments of the present invention with a

gate recess,” while distinguishing the depth of the doped regions between the non-recessed embodiment (about 2.5 Å to about 50 Å) and the recessed embodiment (20 Å to about 5000 Å). EX1007 ¶[0012]; EX2005 ¶84. Additional exemplary distinctions are summarized below.

Saxler Feature(s)	Non-Recessed Embodiment	Recessed Embodiment
Shape of cap layer and gate contact Fig. 1B, 1A, <i>see also</i> Fig. 2A, 2B		
Thickness of cap layer ¶[0027], <i>see also</i> ¶[0081]	“from about 2 Å to about 20 Å”	“from about 5 to about 5000 Å”
Level of doping of cap layer ¶[0071], <i>see also</i> ¶[0073]	“should be sufficiently high so as to reduce leakage current... and be the dominant ‘surface’ state but not so high as to [] introduce traps or leakage paths by becoming a conductive layer”	“a high level of p-type dopants may be provided such that the cap layer 34’ may be provided as a conductive layer”
Dopant concentration of cap layer ¶[0012]	“from about 10^{18} to about 10^{21} cm^{-3} ”	“more heavily doped than 10^{21} cm^{-3} ”
Thickness of doped region ¶[0012], <i>see also</i> ¶[0014],	“into the cap layer from about 2.5 Å to about 50 Å”	“into the cap layer from about 20 Å to about 5000 Å”

[0070], [0071], [0073]		
Increased concentration of Al ¶[0007], <i>see also</i> ¶[0062]	“extends into the cap layer from about 2.5 Å to about 100 Å”	“extends into the cap layer from about 30 Å to about 1000 Å”

The cap layer of the recessed embodiment is thicker with a higher concentration of doping and a doping layer that extends further into the cap layer than the non-recessed embodiment. EX1007 Figs. 1A-B, ¶¶[0012], [0013], [0014], [0070], [0071], [0027], [0081]; EX2005 ¶85. A POSA would understand that the non-recessed embodiment disclosed by Saxler is consistent with surface doping, and the maximum thickness of the doped region of the non-recessed embodiments is 250 times thinner than that of the recessed embodiments, with very limited overlap with respect to the range of the recessed embodiment. EX1007 ¶[0027]; EX2005 ¶87. Furthermore, the dopant concentration is further divergent between the two embodiments. EX1007 ¶¶[0012], [0073]. Thus, Saxler does not provide any suggestion to a POSA of the dopant concentration or the thickness of the dopant for Petitioner’s hypothetical transistor. EX2005 ¶87. Simply put, Saxler provides absolutely no disclosure or suggestion of removing the recess from the recessed embodiment.

When asked about these structural and functional distinctions in Saxler, Dr.

Shealy could not support his position that these passages disclose an “optional” gate recess. EX2004, 38:12-19. (“It was pretty clear what was stated in those paragraphs”). Dr. Shealy further revealed that Petitioner’s position relies solely on paragraph [0052] of Saxler. *Id.* at 38:12-39:5. Dr. Shealy is of the opinion that paragraph [0052] of Saxler allows you to “take all the embodiments and bring in which ones you want, depending on what you’re trying to accomplish.” *Id.* at 39:3-5. This testimony reveals Petitioner’s intention and hindsight -- Petitioner is trying to reengineer the recessed embodiment of Saxler to “accomplish” the claimed invention. EX2005 ¶104.

Petitioner’s reliance on paragraph [0052] as a substitute for motivation to modify (and its attendant expectation of success) is misplaced. Paragraph [0052] does NOT state that the disclosed embodiments of the recessed gate structure (FIGS. 1A, 2B) and non-recessed gate structure (FIGS. 1B, 2A) can be freely modified to include or exclude a recessed gate. EX1007 ¶[0052] Rather, the paragraph only states that “**other** embodiments of the present invention may include or not include a gate recess.” EX2005 ¶97. Indeed, as noted above and as explained by Dr. Schubert, the features and parameters of the recessed and non-recessed embodiments are vastly different and, absent hindsight of claim 1, a POSA having read paragraph [0052] would have understood the “other embodiment” not having a gate recess to be the non-recessed structure depicted in Figure 1B. *Id.* ¶98. A POSA would not

have understood it to mean the modified figure created by Petitioner because a POSA would have understood that additional process steps would be required to get from Figure 1B to the modified figure – none of which are provided by Petitioner. *Id.*

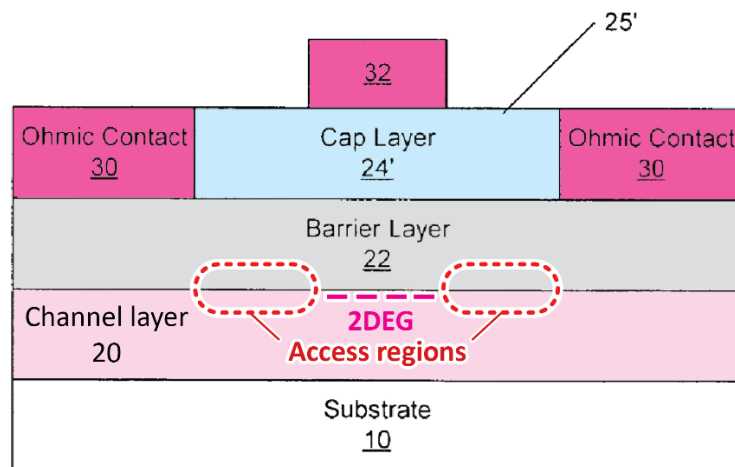
C. Petitioner’s proposed modification of Saxler does not produce an operable method for manufacturing an enhancement mode transistor

Saxler discloses depletion-mode transistors, not enhancement-mode transistors. EX2005 ¶114; EX1003 ¶099 (“Saxler does not use the phrase ‘enhancement-mode’”).

Indeed, Petitioner acknowledges that the recessed embodiment disclosed by Saxler is not enhancement-mode due to the recessed gate structure. Pet. 55-56; EX1003 ¶146 (“with the recess, Saxler’s device is not enhancement-mode (always off)”; EX2004, 59:5-10 (“as it's drawn, it would be a depletion-mode device”).

Petitioner concedes that the non-recessed transistor of FIG. 1B would not be a functional enhancement-mode transistor because the cap layer 24’ extends from ohmic contact 30 to ohmic contact 30. EX2004, 53:13-19 (“1B is a strange cartoon... I've never seen a device built that way, where the sides of the Ohmics are able to butt up against the cap layer -- you're not going to be able to fabricate that.”); 65:16-18 (“[T]hat structure, as shown, would have these shunt problems I was talking about.”). Dr. Shealy later contradicts himself, stating that it can be enhancement-mode. EX2004 66:19-68:11.

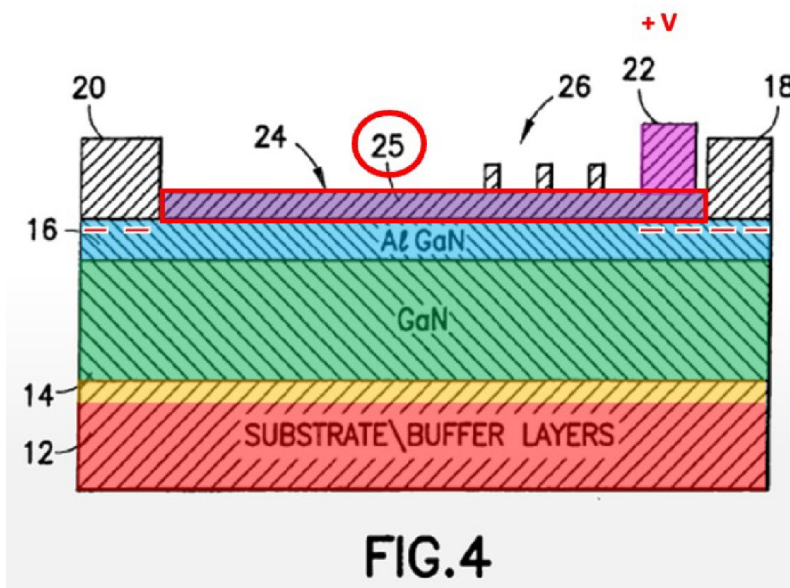
As acknowledged by Dr. Shealy, Saxler's cap layer 34 in Fig. 1B extends completely from Source to Drain (ohmic contacts 30), including the access regions that are located between the S&G (source and gate) electrodes, as well as between the G&D (gate & drain) electrodes. EX2005, 117.



When a voltage is applied to the gate electrode, a 2DEG is induced substantially below the gate electrode but, importantly, not under the entirety of the cap layer 24' of Saxler (that is, not all the way from Source to Drain). As a result, the transistor, if enhancement mode, could never be switched ON. *Id.* at 118.

Petitioner confirmed this operation in the related ITC proceeding between the parties. There, for a transistor that has a GaN layer that extends from source to drain, Petitioner agreed that the 2DEG is not reconstituted between the source and the drain when a positive voltage—necessary for enhancement-mode operation—is applied to the gate. Ex. 2008 at 938:1-10. When such a positive voltage (+v) is applied, as shown below, the 2DEG (represented as red dash “—”) is *only* reconstituted under

the gate, which is insufficient to turn the device ON because the 2DEG is not continuous between the source and drain contacts. *Id.* Petitioner’s expert in the ITC proceeding, Dr. Lebby, admitted as much during his redirect examination at trial, referring to the image below, noting that “...you can establish a 2DEG with a positive voltage on an enhancement-mode, and the question here is, is that the 2DEG doesn’t – **it’s not continuous all the way from the source to the drain...**” *Id.* at 938:5-10 (emphasis added); *see also*, EX2009 at 41; EX2005 ¶123.

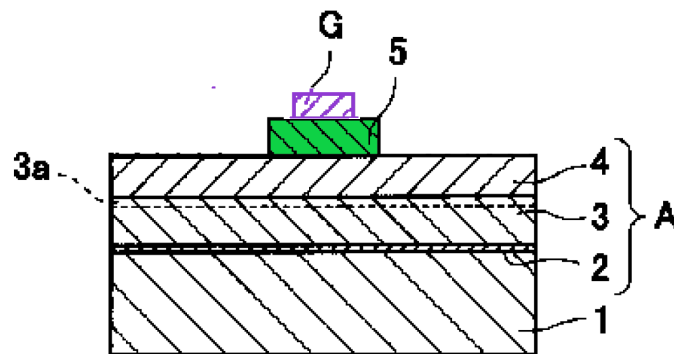


EX2009, 41

Even assuming that Dr. Shealy is correct in that it would be possible to apply a sufficiently high voltage to replenish the electrons in the access regions, a POSA would not produce an enhancement-mode circuit in this manner. EX2005 ¶124.

Conversely, cap layers in depletion mode transistors can extend substantially the entire length between the ohmic contacts because the transistor is normally ON

and the cap layer only needs to pinch off the current by depleting the 2DEG under the gate to turn the transistor OFF. EX2005 ¶125. On the other hand, enhancement mode transistors are normally OFF, and the situation is reversed, and the 2DEG must be replenished under the p-type gate material. EX2005 ¶125. As disclosed, for example, in Yoshida, enhancement mode transistors are designed to provide voltage control with a small amount of carrier injection. EX1006 ¶[0017]. This is produced in Yoshida by “etch[ing] away the p-type GaN layer except where the gate electrode was to be loaded and exposing the n-type InGaN layer 4.” *Id.* ¶[0022]. Thus, a POSA would understand that the gate material is designed in an enhancement-mode transistors such that only a small portion of the 2DEG needs to be replenished to turn it ON. EX2005 ¶126.



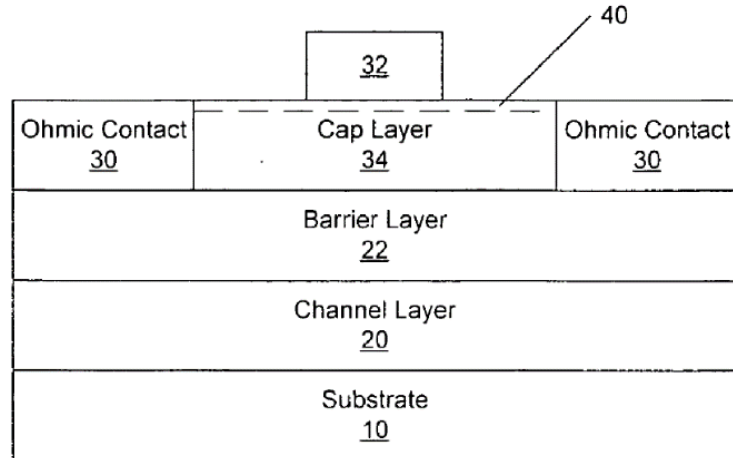
EX1005, Fig. 1

Moreover, Petitioner’s expert from the ITC proceeding, Dr. Lebby, admitted that he has no quantitative basis for his theory that a sufficiently high voltage could replenish electrons in the 2DEG; he conceded that he has neither modeled nor simulated any part of this theory. EX2008 at 938:19-939:8. Dr. Lebby’s vague

instructions to a POSA are to “play with” various aspects, with the admitted caveat that even if such a device were to exist (and it does not), it would have “lots of leakage” due to the massive amount of voltage passing through the gate. *Id.* at 939:5-8. That is precisely why a POSA would not have been motivated to apply such a high voltage. EX2005 ¶127.

Thus, a POSA would have no reason to convert the depletion mode transistor of Saxler, having the cap layer 24 extending entire or substantially entirely between the ohmic contacts, to an enhancement mode transistor. The modification proposed by Petitioner, even if possible, would knowingly require excessive voltage to be applied to turn the transistor ON (assuming that it would even turn ON), which a POSA would know is undesirable for transistors. EX1006 ¶[0017].

Indeed, all of the embodiments disclosed in Saxler are depletion mode transistors. For example, Saxler discloses with reference to Figure 2A, “the doped region 40 may be doped with p-type dopants so as to provide a p-n junction between the doped region and the cap layer 34 and the gate contact 32 is provided directly on the doped region 40 so as to provide a Junction HEMT (JHEMT).” EX1007 ¶[0072]. As acknowledged by Dr. Shealy, the disclosed JHEMT is depletion mode and not enhancement mode. EX2004, 72:1-15. ([I]t would be in depletion mode – and it’s a bad idea.”).



EX1007, Fig. 2A

Paragraph [0049] explains the purpose of p-type doping of region 40 at the top of the cap layer: “the dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations.” EX1007 ¶[0049] Indeed, Saxler points out that the dopants “segregate to dislocations” rather than depleting the 2DEG. *Id.* Paragraph [0049] further explains that “a shallow dopant in the bulk crystal may have characteristics of a deep level when at a dislocation” which is “especially true in the case of p-type [...] dopants.” *Id.* Thus, the shallow acceptors of Saxler do not even act as acceptors once they “segregate to dislocations.” EX2005 ¶128. If the shallow dopants do not act as acceptors, the cap layer cannot function in enhancement mode. *Id.* That is, the dopants that Dr. Shealy envisions as regular, shallow p-type dopants, are in fact characteristics of “deep level” dopants. *Id.* This fact would be perceived as problematic and de-motivating by a POSA, because, contrary to Dr. Shealy’s

assertions, “deep levels” are generally not suitable to deplete a 2DEG. *Id.* As a result, a POSA would lack motivation, and actually be discouraged, to take the path Dr. Shealy envisions.

D. Contrary to Petitioner’s assumption, Saxler does not disclose “precise” central alignment of the gate electrode on the cap layer

Petitioner bases Ground 1 on reverse engineering the schematic of Fig. 1A of Saxler in proposing “a known, obvious way to create that structure.” Pet. 35; EX2005 ¶130.

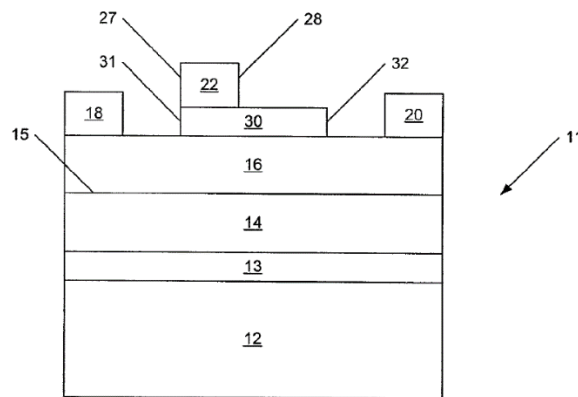
Petitioner further alleges that “[a]lthough not explicitly disclosed, a POSITA would have understood that Saxler uses a photomask to etch the gate because Saxler requires precise positioning achievable using this conventional approach.” Pet. 24.

However, Petitioner does not provide any support for the statement that “Saxler requires precise positioning,” nor that Saxler discloses a precisely centrally aligned gate structure. Petitioner appears to rely solely on FIGS. 1A and 1B to support its assertion that “precise positioning” is required. Pet. 42. But Petitioner’s reliance on the drawings for “precise positioning” is improper. *See Hockerson-Halberstadt, Inc. v. Avia Group Int’l*; 222 F.3d 951, 956 (Fed. Cir. 2000); *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977); *Go Med. Indus. Pty, Ltd. v. Inmed Corp.*, 471 F.3d 1264, 1271 (Fed. Cir. 2006).

Indeed, Saxler explicitly discloses that “the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise

shape of a region of a device and are not intended to limit the scope of the present invention.” EX1007 ¶[0042]. Thus, Saxler explicitly states that the drawings cannot be relied on for exact dimensions or direct alignment in that “the precise shape of a region” (positioning) is not required. EX2005 ¶133. Petitioner and Dr. Shealy’s agreement is shown by their discrediting the accuracy of the drawings of Saxler, citing ¶[0042] of Saxler to argue that “an etched region illustrated as a rectangle will, typically have tapered, rounded or curved features.” Pet. 90.

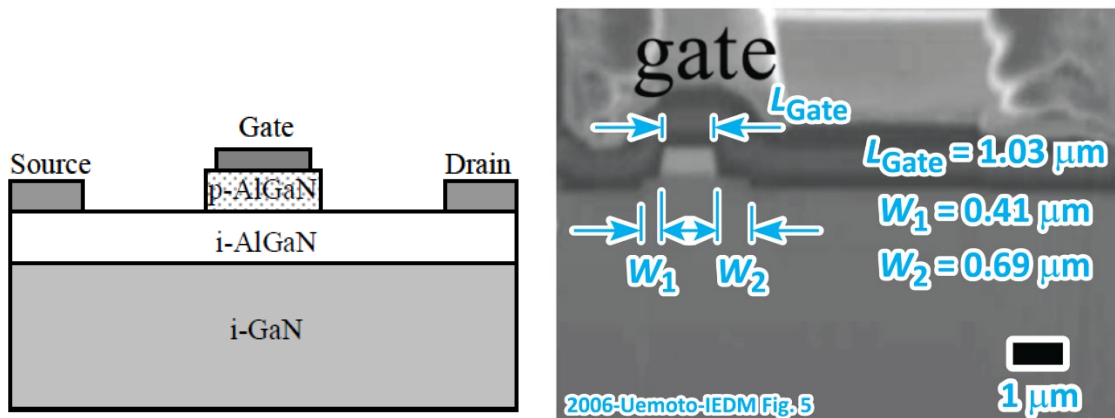
The only disclosure of the relative position of the gate electrode on the cap layer is that “in particular embodiments where the ohmic contacts 30 provide source and drain contacts, the recess may be offset... closer to the source contact than the drain contact” (EX1007 ¶[0065]) which is consistent with the disclosure of Smith as incorporated (EX1007 ¶[0042], EX1015 ¶¶[0041]-[0042]). EX2005 ¶134.



EX1015, Fig. 3

This offset position is echoed by Petitioner’s later reliance on *Uemoto*. Notably, Uemoto shows a diagram of what appears to be a centrally aligned gate.

But the actual SEM image that corresponds to that diagram shows the gate with an “offset” gate electrode “closer to the source contact than the drain contact.” Pet. 90-92; EX1020, Figs. 1, 5; EX2004, 94:21-22 (Dr. Shealy acknowledging that the structure of Uemoto does not have substantially equal ledges); EX2005 ¶135.



EX1020, Fig. 1

Pet. 92 (EX1020, Fig. 5 annotated)

For the foregoing reasons, Petitioner does not provide any support that “Saxler requires precise positioning” with a “precisely” centrally aligned gate structure. EX2005 ¶136.

E. Saxler provides no disclosure or suggestion of etching the gate electrode and cap layer with a single photoresist

In addressing [1g], Petitioner alleges that “Saxler also discloses or at least renders obvious etching the gate metal using the same photoresist.” Pet. 43. This assertion was directly negated by Dr. Shealy at his deposition, where Dr. Shealy admitted that Saxler does not disclose “using the same mask.” EX2004, 55:1-7 (“[W]e bring in the self-aligned with other references: Beach and Ahn”). EX2005

¶138.

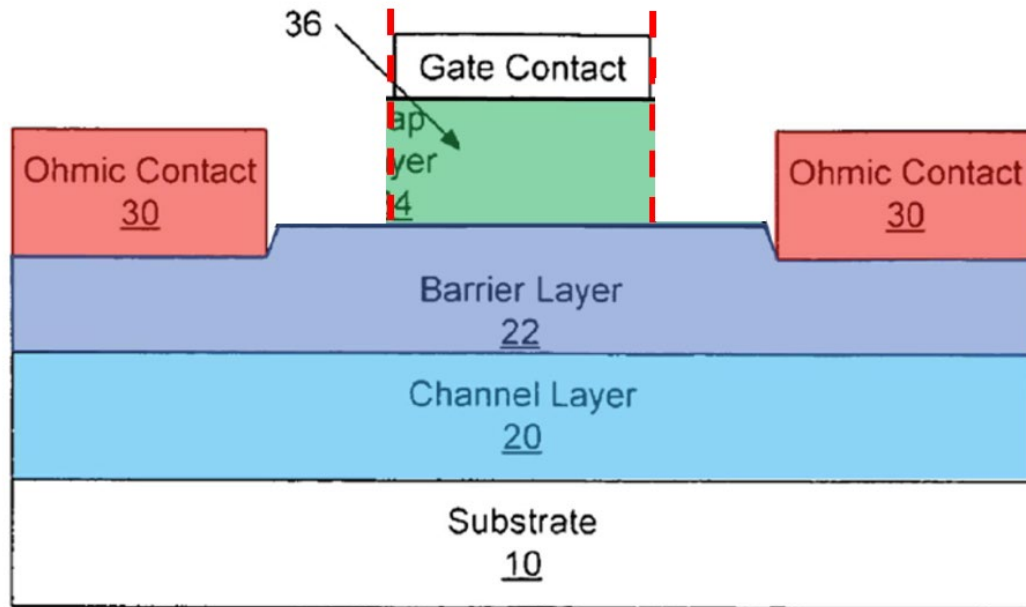
Moreover, Petitioner's assertion that Saxler renders obvious etching the gate metal using the same photoresist is based on the false premise that that "a POSITA would have understood depositing Saxler's gate contact would have involved masking and etching the gate metal *to precisely position it*," (Pet. 43 (emphasis added)), as noted above.

F. A POSA would not modify Saxler with the "self-aligned" technique of Beach

The "self-aligned" technique of Beach would not produce the sloped sidewalls of Saxler, as relied on by Petitioner. Petitioner alleges that "it would have been obvious to modify Saxler with Beach's self-aligned technique." Pet. 32. Petitioner further alleges "Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet. 35.

Petitioner's premise for the combination of Saxler and Beach is that Saxler requires "precise" and direct alignment of the gate electrode on the center axis of the cap layer, solely based on Figs. 1A, 1B. Pet. 24. However, Petitioner's premise is false, as it is based solely on Saxler's schematic figures. Indeed, Saxler does not disclose any "precisely" centrally aligned structures, but rather discloses, to the contrary, the gate contact being "offset... closer to the source contact than the drain contact." EX1007 ¶¶[0042], [0065].

Furthermore, as acknowledged by Dr. Shealy, applying Beach's self-aligned technique would either cut off, or not form, the horizontally extending "sloped" side surfaces that Petitioner relies on from Fig. 1A of Saxler and in the hypothetical transistor, as illustrated below. EX2005 ¶145.



Pet. 45 (showing etching from Beach)

Indeed, Dr. Shealy explained "what Beach figure shows is a -- you know, it's drawn as a vertical wall. It's an idealized drawing, of course. Well, one would expect it to have some curvature." EX2004, 87:15-19. Thus, Shealy directly undercuts Petitioner's assertion that "Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet. 35. Applying the Beach self-aligned technique to Saxler would not produce the sloped sidewalls as illustrated in Saxler but would

rather produce intentionally vertical sidewalls with potentially “some curvature.” EX2005 ¶146.

Petitioner relies on the sloped walls as exactly illustrated in Fig. 1A because it is “a fair representation of what Saxler is trying to achieve” except for the vertical scale showing detail of the epitaxial layer. EX2004, 56:21-25. Furthermore, Petitioner specifically relies on those sloped walls for dimensions. Pet. 46, 67. Thus, modifying Saxler with the self-aligned technique of Beach would not result in the “sloped sidewalls” of Saxler as illustrated in Fig. 1A and relied on by Petitioner. EX2005 ¶143-154 (discussing *Beach*, *Beach-II*, and *Smith* as mentioned by Petitioner). Neither reference discloses or suggests a sloped sidewall of the lower layer together with a self-aligned process.

Moreover, the etching in Beach is incompatible with Saxler. Beach discloses N-polar (nitrogen-polar) technology (¶10), while Saxler discloses Ga-polar (gallium-polar) technology. EX2005 ¶155. The two polarities cannot be combined, mixed, or synthesized, because they are mutually exclusive opposites. *Id.* Due to the N-polar orientation of Beach, a POSA would not have used Beach as guidance to modify the teachings of Saxler. *Id.*

Therefore, as explained above, the devices described in each reference are substantially different, and the teachings of Beach would not have been incorporated by a POSA into the structure and method of manufacture described in Saxler.

EX2005 ¶143-155.

G. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner’s reasoning

Petitioner alleges that “it would have been obvious to combine Saxler with Beach and Shenoy’s techniques of masking and etching the gate metal and p-type gate material using a single photomask when making Saxler’s non-recessed GaN HEMT device.” Pet. 43-44.

Shenoy involves electrochemical etching – etching with an applied voltage, an applied electric field, and an electrical current flowing. EX2005 ¶157. However, because the method of Shenoy is performed under very controlled conditions, a POSA would not have considered Shenoy to modify the teachings of Saxler as modified by Beach. *Id.* Indeed, electrochemical etching can only be used in conjunction with conductive materials and insulator materials. *Id.*

More specifically, the process of Shenoy in forming the undercut “U” on the metal film is explicitly dependent on the positioning of the metal film on an underlying insulator and in isolation of other components that could be etched. *Id.* ¶155. As further discussed in the “Model Development”, Shenoy discloses “the metal film thickness ratio determines **the extent to which EMM must proceed before the underlying insulator is exposed... Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal**

“wall angle, γ .” EX1009 at 2 (emphasis added); EX2005 ¶¶155-159.

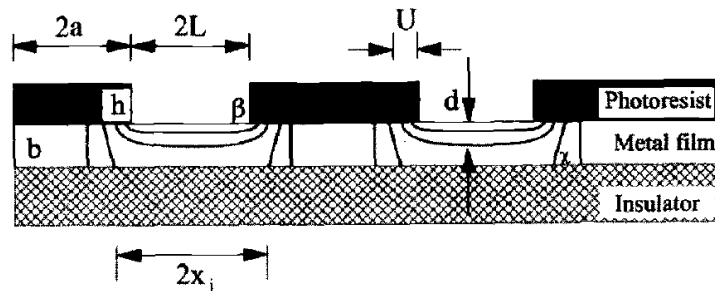
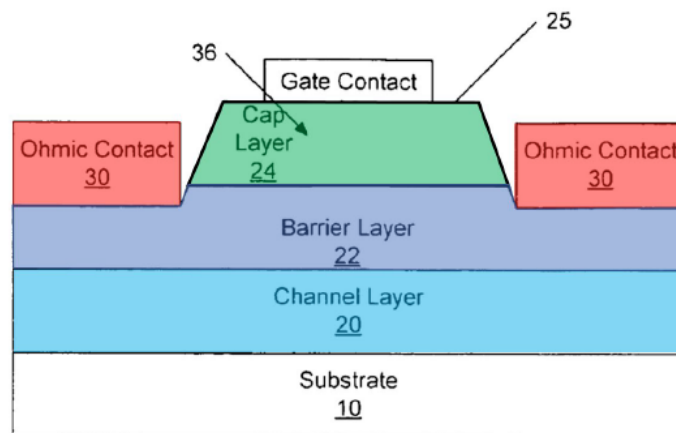


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

A POSA would not have modified the method of Saxler as proposed with Beach and Shenoy, because the cap layer 24 and gate contact 32 of Saxler would already be in place on the transistor and etched by the technique of Beach to expose the side layers of the gate contact 32. EX2005 ¶161.



Pet. 45

In an attempt to support Petitioner’s position, Dr. Shealy asserts that “gallium nitride is a pretty tough material to etch, and a lot of these etches will not etch it. So that – that’s again like Shenoy: The insulator is not being etched in Shenoy.”

EX2004, 99:18-21.

However, as Dr. Shealy apparently recognizes, GaN is not an insulator. EX2005 ¶164. Shenoy specifically models the etching based on current distribution, not “tough[ness].” *Id.* Furthermore, Shealy is referring to “liquid metal etches” (EX2004, 97:11-13, 9:14-17), which are not cited in the petition and thus have no bearing to the present claims. *Id.*

Shenoy specifically relies on “Faraday’s law” and “Laplace's equation” (EX1009 at 3) that equally apply to metals as well as semiconductors, thereby elucidating that the metal as well as the semiconductor is being etched away when Shenoy is applied to the transistor of Saxler. *Id.* ¶165.

Shenoy specifically models the etching based on equation 5, as reproduced below.

The current distribution at the anode has been combined with Faraday’s law to determine the evolution of the metal surface. The rate, r , at which the anodic surface recedes is

$$r = \frac{M\theta}{nF\rho} i \quad [5]$$

where M is the molecular weight of the metal, n is the metal dissolution valence, ρ is the density of the metal film, F is Faraday’s constant, and θ is the current efficiency of metal dissolution which is assumed to be constant at 100%.

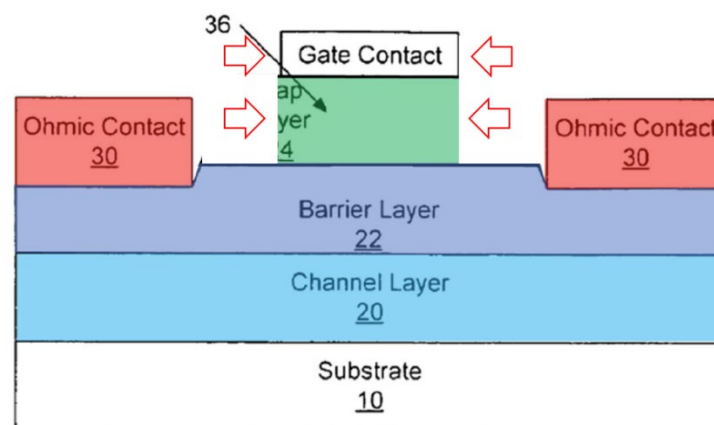
EX1009, 3

In applying equation 5, the current distribution i would be zero for insulators (such as SiO_2), thereby showing that no etching would occur in the insulator (SiO_2)

underlying Shenoy's metal layer, consistent with Shenoy's proposed results. EX2005 ¶167. However, a current distribution would occur in the GaN because it is not an insulator, thus etching would occur contrary to Petitioner's proposed modification. *Id.*

In further addressing GaN, Dr. Shealy alleges that "this is a p-type semiconductor doped of magnesium, and it would normally have holes. But because of these side surfaces, the holes are depleted away from the surface where the etching is occurring. And what that means is, is that the semiconductor layer behaves as an insulator just like Shenoy's structure, because there are no mobile charges near the etching region in the semiconductor." EX2004, 99:4-13.

However, neither Saxler nor Beach teach any passivating of the GaN material. EX2005 ¶169. According to Dr. Schubert, the cap layer of Saxler would still be conductive and thus be etched. *Id.*



Pet. 45 (showing etching of Shenoy)

However, even assuming that Dr. Shealy is correct, the side surfaces that would have been etched by Beach in the proposed modification are not relevant to the method of Shenoy. *Id.* ¶169. Rather, the spread or undercutting is induced by an underlying insulator. EX1009 at 1; EX2005 ¶169.

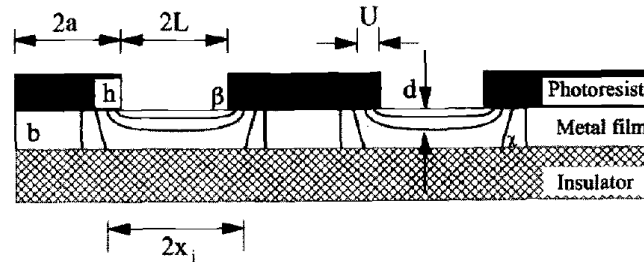
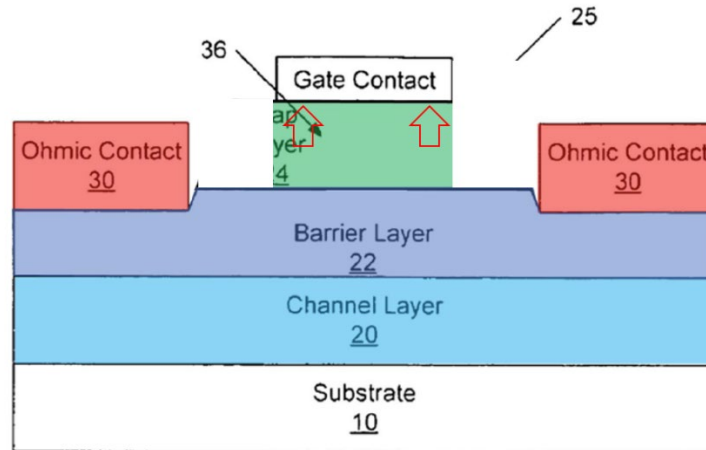


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

The etched side walls that Dr. Shealy is referring to would not underlie the gate contact. EX2005 ¶170. Rather, when comparing the mathematic setup of Shenoy to the transistor of Saxler, the portion of the cap layer 34 underlying the gate contact 32 in Saxler would actually be the surfaces pointed out in **red arrows** below. *Id.* These surfaces would not have been etched by the self-aligned process of Beach. *Id.* Those same surfaces of the cap layer 34 are also relied on by Petitioner for the claimed ledges. *Id.*



Pet. 45 (etched by Beach's self-alignment)

Even assuming Dr. Sheely's reasoning (which is incorrect), the surface of the cap layer 34 underlying the gate contact would still "have holes," because it would not have been etched (EX2004, 99:4-13) by the Beach process and thus not act as an insulator. EX2005 ¶171. Therefore, the underlying surfaces of the cap layer 34 would be etched along with the gate contact in the etching process of Shenoy, and thus would not be retained as ledges. *Id.*

Therefore, in addition to Beach, Shenoy undercuts Petitioner's assertion that "Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet. 35. Applying the EMM etching of Shenoy would etch at least the alleged ledges of the cap layer 34 in Saxler that would underlie the gate contact in Petitioner's proposed method. EX2005 ¶172. Thus, applying the method of Shenoy would not produce the hypothetical structure of Saxler, as alleged by Petitioner. *Id.* ¶¶172-73. What would happen is unpredictable at best. Shenoy's etching process is not a

selective etching with the exclusion of perfect insulators. *Id.* ¶173.

H. A POSA would not have found it obvious to combine Saxler, Beach, and Shenoy

Petitioner fails to articulate a reason for POSA to combine Saxler, Beach, and Shenoy, and has left it to Patent Owner and the Board to fill in the gaps between the proposed combinations of Saxler with Beach and Shenoy. EX2005 ¶176. Petitioner's failure to explain a reason to combine all three references undermines Patent Owner's ability to respond to the obviousness contentions. *Id.* It is well established that an "obviousness ground, in particular, cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with rational underpinning to support the legal conclusion of obviousness." *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (*quoting KSR Int'l. Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)). As discussed at the outset and pervading each of Petitioner's grounds, Petitioner fails to provide sufficient specifics on how the combined/modified/rearranged process would actually be performed. EX2005 ¶177. Importantly, Petitioner has not provided a fabrication process sequence, neither in a narrative nor pictorial manner. *Id.* Petitioner repeatedly relies on reasoning such as "no more than simple substitution" and "known methods that would be predictably implemented" (Pet. 34), **but never provides a specific process sequence** for the proposed combination. EX2005 ¶177. Petitioner thereby avoids having to reconcile the conflicts and incompatibilities associated with the

proposed combinations . *Id.*

Dr. Shealy's testimony on obviousness is nothing more than a conclusory statement that a POSA would have known, based on an alleged "simple substitution" of various claimed steps, how to combine any of a number of references to arrive at the claimed **process**. This is insufficient for a **method** patent and is "fraught with hindsight bias." *ActiveVideo Networks, Inc. v. Verizon Commc'n, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012); EX2005 ¶177

Petitioner mischaracterizes the method of Saxler as being "flexible" in alleging complete freedom to modify Saxler. Petitioner alleges that "Sheppard, incorporated to disclose methods of fabricating GaN HEMTs (Saxler, [0046], [0068]), describes a flexible approach to masking and etching. It notes that 'operations described as multiple steps could be combined into a single step' (and vice versa), making the choice of Beach's manufacturing steps no more than simple substitutions." Pet. 34.

Furthermore, splitting a single described step into multiple steps or combining multiple described steps into a single step as described by Sheppard does not support Petitioner's proposed modification of Saxler's process. EX2005 ¶180.

Recreating the process of Saxler by piecing together 1) some steps of Saxler, 2) some steps of Beach, and 3) some steps of Shenoy (in no specified order) to arrive at the claimed invention goes far beyond any alleged "flexible" approach as

suggested by Sheppard. *Id.* ¶¶180-81. It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant’s structure as a template and selecting features from the references to fill the gaps. *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991).

For at least those reasons, *Saxler* in view of *Beach* and *Shenoy* does not render obvious claims 1-3 of the ’347 Patent. EX2005 ¶183.

VIII. GROUND 2 (SAXLER IN VIEW OF YOSHIDA, BEACH, AND SHENOY)

Ground 2 is substantially duplicative of Ground 1, thus has similar deficiencies as discussed in §VII. EX2005 ¶¶184-185. Petitioner attempts to form the same modified Fig. 1A representation of *Saxler* but rely upon the non-recessed structure of *Yoshida* instead of the non-recessed embodiment of *Saxler*. Pet. 50, 59 Indeed, Ground 2 is asserted “to the extent Patent Owner disagrees *Saxler*’s disclosure that the use of the recess is optional alone renders this structure obvious (Ground 1)” (Pet. 54), which is a tacit admission that a POSA would not have immediately come to the conclusion that the modified figure 1A is disclosed by *Saxler*.

A. A POSA would not modify the recessed embodiment of *Saxler* by removing the recess based on *Yoshida*

Contrary to Petitioner’s allegations, “*Saxler* and *Yoshida*” *do not* “disclose compatible enhancement-mode GaN HEMT devices comprising the same layers

performing the same functions, including stacked gate structures having a cap layer and gate metal. ” Pet. 52. For all of the reasons discussed above, *Saxler* is *not* an enhancement mode device. EX2005 ¶193.

Dr. Shealy explicitly opines that the recessed embodiment of Saxler would not be functionally equivalent with the enhancement-mode transistor of Yoshida in stating that “with the recess, Saxler’s device is not enhancement-mode (always off).” EX1003 ¶146. Indeed, the cap layer of Saxler extends entirely or substantially the entire length between ohmic contacts, consistent with depletion-mode and not enhancement-mode (§VII.C), while Yoshida discloses an enhancement-mode transistor (§VI.B). There are a number of additional divergent parameters provided in relation the recessed embodiment of Saxler. §VII.B. Thus, at least according to Dr. Shealy, Saxler and Yoshida would not have “the same layers performing the same functions” as alleged by Petitioner. EX2005 ¶193.

For this same reason, a POSA would have to change *Saxler*’s principal of operation (i.e., enhancement mode) (*see* EX2004, 59:5-10) for it to be combinable with *Yoshida* (i.e., enhancement mode).

Thus, Petitioner’s motivation of “remov[ing] the gate recess to turn Saxler’s device into an enhancement-mode device” (Pet. 55-56) would be improper as it would change the principle operation of Saxler and destroy Saxler’s depletion-mode transistor. MPEP § 2143.01; *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959); *see also*

EX2005 ¶¶35, 193.

Petitioner’s arguments are also inconsistent with the disclosure of Saxler. As further discussed in §VI.A, Saxler describes two embodiments having a number of distinguishing structural and functional aspects including differences in the cap layer thicknesses, dopant concentrations, and doping depth. EX1007, Figs. 1A, B, 2A, 2B, and ¶¶[0007], [0012], [0014], [0027], [0062], [0070], [0071], [0073], [0074], [0076], [0081]. Thus, Saxler would not remove the recess from the recessed embodiment in view of Yoshida for the same reasons that Saxler does not disclose a non-recessed embodiment with the parameters of the recessed embodiment. Saxler’s embodiments are distinct without any reason to “mix and match”. EX2005 ¶194.

B. Petitioner’s apparent modification of Saxler does not produce a method for manufacturing an operational enhancement mode transistor

Petitioner cites Ground 1 in addressing [1p]. Pet. 57. Thus, the arguments fail for the reasons provided in §VI.C; EX2005 ¶¶197-203.

C. A POSA would not modify Saxler with the “self-aligned” technique of Beach

Petitioner cites Ground 1 in addressing [1f], [1g], [1h]. Pet. 57-58. Thus, the argument fails for the reasons provided in §VI.F; EX2005 ¶¶205-208.

D. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges, based on Petitioner’s reasoning

Petitioner cites Ground 1 in addressing [1i]. Pet. 58-59. Thus, the argument fails for the reasons provided in §VI.G; EX2005 ¶¶209-214.

E. A POSA would not have found it obvious to combine Saxler, Yoshida, Beach, and Shenoy

In again relying on Saxler, Beach, and Shenoy in addition to Yoshida, Petitioner’s argument has the same deficiencies in motivation as discussed in §VII.H; EX2005 ¶¶215-218.

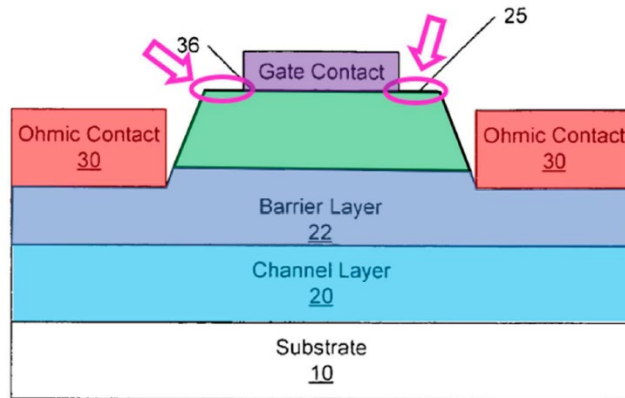
For at least those reasons, *Saxler* in view of *Yoshida*, *Beach*, and *Shenoy* does not render obvious claims 1-3 of the ’347 Patent.

IX. GROUND 3 (SAXLER IN VIEW OF AHN)

At the outset, Ground 3 suffers from the same fatal flaws as the other grounds without *ever presenting a description of the actual proposed modified prior art process*. EX2005 ¶219. Rather, Petitioner simply picks and chooses different *features* of the prior art and abstractly asserts that the combination renders the claims obvious, without explaining how the proposed combination would fit into an overall process to arrive at the claimed invention or even which process Petitioner is relying on. *Id.*

In Ground 3, Petitioner largely relies on the same reasoning as Ground 1 by – again – starting with the hypothetical “non-recessed Saxler embodiment.” *Id.* ¶219.

Petitioner alleges “to the extent Saxler alone does not explicitly disclose masking and etching the gate contact or self-aligned etching, Ahn renders this obvious.” Pet. 60. Petitioner further alleges “the combination would yield the same structure as the non-recessed Saxler embodiment” as follows:



Pet. 62

- A. A POSA would not consider the gate recess of Saxler as “optional” and Dr. Shealy’s “mix and match” actually implies substantial modifications**

Since Petitioner is relying on the same structure based on the same rational as Ground 1, Ground 3 is improper for at least the reasons provided in §VII.B.

- B. Petitioner’s apparent modification of Saxler does not produce a method for manufacturing an operational enhance mode transistor**

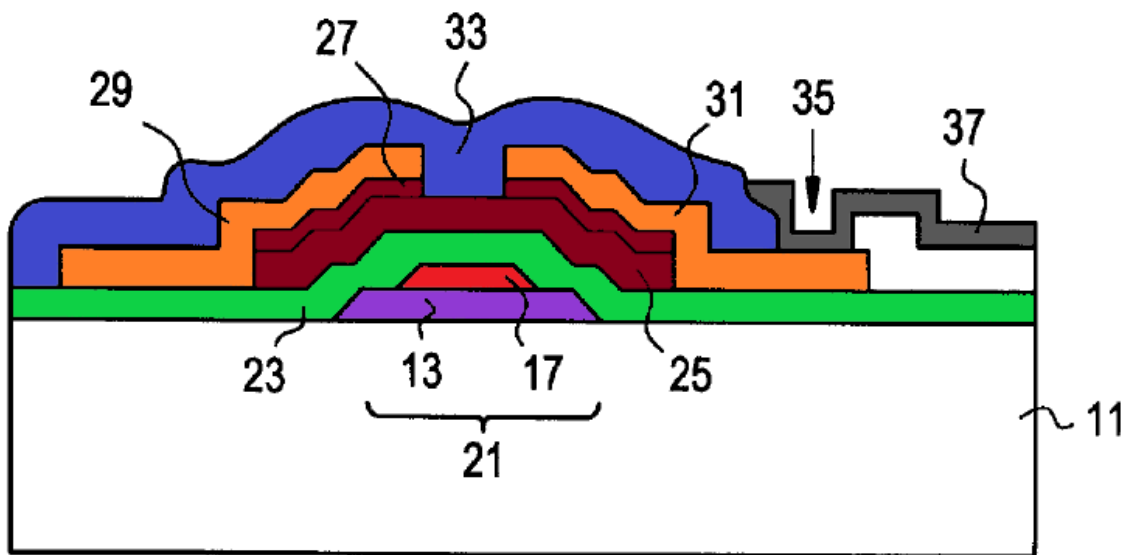
Petitioner refers back to Ground 1 to address [1p]. Pet. 64. Thus, the interpretation is improper for at least the reasons provided in §VII.C.

- C. A POSA would have no motivation to modify the method of Saxler based on Ahn**

Petitioner begins the analysis based on a faulty premise that Saxler intends for

a centrally aligned gate electrode. Petitioner further alleges that “a POSITA would have found it obvious to modify Saxler with Ahn’s approach for making a stepped gate in a thin-film transistor to improve alignment.” Pet. 63. As further discussed in §VII.D, Petitioner’s presumption that Saxler requires “alignment”, specifically central alignment (as taught by Ahn), is incorrect. *See* EX2005 ¶¶234-237.

Ahn teaches a substantially different gate structure from Saxler and intends to solve an unrelated problem with different etching methods. EX2005 ¶¶238-248. As discussed in §VI.E, Ahn is directed to a thin film transistor, which is a special type of FET where the transistor is made by a specific thin film deposition, diverging from GaN HEMTs. EX2005 ¶¶239-241.

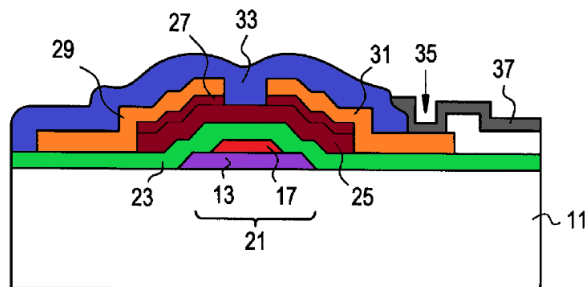
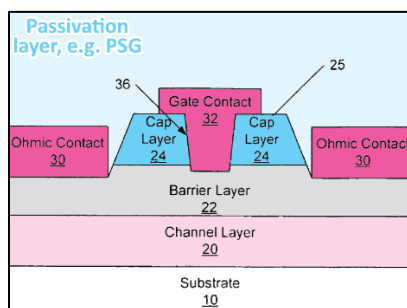


EX1010, Fig. 1F (annotated)

Saxler is not a thin film transistor, nor does Saxler have a relevant analogous structure. EX2005 ¶242. Saxler does not have a thin **gate oxide layer** 23 separating

the gate and the source and drain electrodes 29, 31. *Id.* Furthermore, Saxler does not disclose a gate structure of a double-layer metal structure. *Id.*

The functioning and layering of GaN HEMTs such as Saxler is completely different than that of thin film transistors such as Ahn. *Id.* ¶241. For example, the ohmic contacts 30 of Saxler (and other GaN HEMTs) do not overlap with the gate contact 32 nor is the gate contact 32 separated from a semi-conductive layer by a thin gate oxide layer. *Id.* Rather, as Dr. Shealy states, each of the components in Saxler are laterally spaced apart by a significant distance to avoid a short circuit. EX2004, 65:15-18. The 2DEG in Saxler is formed underneath the gate structure. Furthermore, any passivation layer above the GaN HEMTs such as Saxler is substantially thick (e.g., 500 nm to 1,000 nm) compared to the thin gate oxide layer 23 of Ahn that is on the order of 10 nm. EX2005 ¶242. Additionally, the passivation layers of bulk GaN HEMTs (like Saxler) are made of a different material than thin film transistors, such as PSG (phospho silicate glass) or BPSG (boro phospho silicate glass), where Boron and/or Phosphorus are added to make the glass tend to flow (rather than being rigid) so that pin-holes are rare or absent. *Id.*



EX1007, Fig. 1A (modified)

EX1020, Fig. 1F (annotated)

Thus, the deterioration of the thin **gate oxide layer** 23 of Ahn would not be relevant to Saxler. EX2005 ¶246. Therefore, a POSA would not modify the gate structure of Saxler based on that of the thin film transistor of Ahn. *Id.* Furthermore, the combination of Saxler with Ahn fails to produce an enhancement mode device.

X. GROUND 4 (YOSHIDA IN VIEW OF SAXLER, BEACH, AND SHENOY)

Ground 4 is similar to that of Grounds 1 and 2 in that Petitioner relies on Yoshida, Saxler, Beach and Shenoy. Pet. 72. However, Petitioner starts with Yoshida in Ground 4. *Id.* At the outset, and as discussed above, the drawings of Saxler cannot be relied on to show the shape of Saxler’s device, including the alleged sloped sidewalls that Petitioner alleges can simply substitute Yoshida’s vertical sidewalls. EX2005 ¶250-255.

A. Neither Petitioner nor Yoshida characterizes Yoshida’s method as being “flexible” as relied on by the Board

Patent Owner notes the Decision’s characterization of “Yoshida’s flexible method.” Institution 50. Yoshida does not describe its method as being flexible, nor does Petitioner characterize it as such. EX2005 ¶256.

Yoshida describes its process in ¶¶[0019]-[0023] with transitional terms including “first... then... then... then... lastly...” This is acknowledged by Dr. Shealy in describing Yoshida’s process in a specific order, “(i)... (ii)... (iii)... (iv)...

(v)... (vi)... (vii).” EX1003 ¶204. At his deposition, Dr. Shealy stated that “it’s not clear what the order of the process is” (EX2004, 78:14-15) in direct contradiction of the statement in his Declaration. EX1003 ¶204; EX2005 ¶257.

Furthermore, Yoshida describes its process with specificity, including exact growth temperatures, deposition conditions, and timing of transitions in metal supplies. EX1006 ¶¶[0017]-[0023]; EX2005 ¶258.

Due to this specificity in order, processes and explicitly expressed desire to achieve enhancement mode GaN transistors with sufficient electron mobility, a POSA would recognize that Yoshida’s method is *not* flexible. EX2005 ¶259.

B. Yoshida teaches away from using other methods of manufacturing its gate

Yoshida distinguishes its process from forming the gate structure with “conventional photolithography and etching” in that the transistors produced by those “conventional” methods “cannot be said to have sufficient electron mobility to meet recent demands for still higher speed operations.” EX1006 ¶¶[0006], [0008]. EX2005 ¶260.

Thus, Yoshida directly contradicts Petitioner’s statement that “a POSITA would have known many ways to create Yoshida-Saxler’s . . . structure and would have used these methods interchangeable” (Pet. 77), where Yoshida expressly distinguishes its method from “conventional photolithography and etching.” EX1006 ¶¶[0006], [0008]. EX2005 ¶261.

As explained above, the process of Yoshida is directed to forming a transistor with a pn junction of a p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility.” EX1006 ¶¶0017]. EX2005 ¶262.

This configuration and functionality are not produced by prior art relied on by Petitioner, specifically Saxler, Shenoy, and Ahn, that are directed to producing completely different transistors or even theoretical mathematical models as discussed herein. EX2005 ¶263.

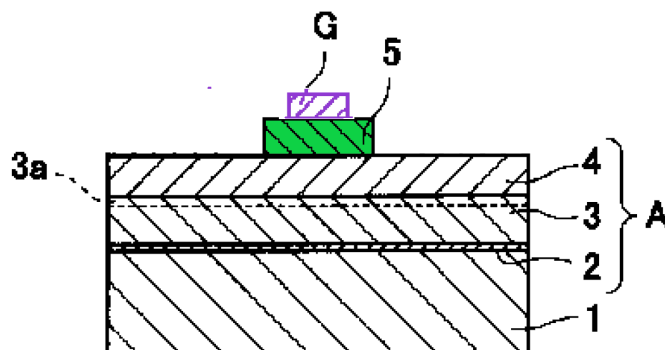
For at least these reasons, Petitioner’s reverse engineering of Yoshida’s method in ground 4 in “trying to accomplish” (EX2004, 38:3-5) the claimed invention is again improper. EX2005 ¶264.

C. A POSA would not have any reason to form ledges after the self-aligned process of Beach

Petitioner alleges “a POSITA would have found it obvious to use Beach and Shenoy’s techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal using a single mask to obtain self-aligned ledges, resulting in the same gate structure that Yoshida-Saxler discloses.” Pet. 72.

As discussed in §§VI.B, X.C, the transistor of Yoshida is formed by a process

where the p-type GaN layer 5 is layered and “etch[ed] away... except where the gate electrode was to be loaded” (prior to loading the gate electrode G). EX1006 ¶[0022]; EX2005 ¶266.



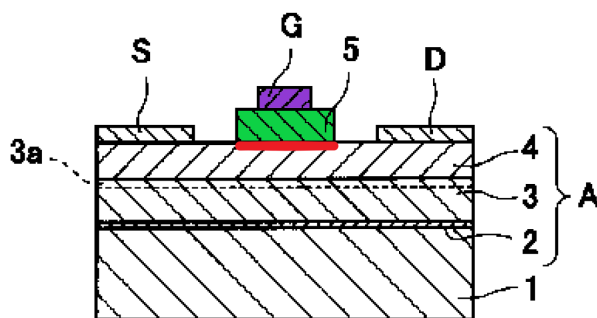
EX1005, Fig. 1 (annotated)

Although the p-type GaN layer 5 is illustrated as being formed wider than the gate G, that structure is typical for processes where the p-type GaN layer 5 is patterned before the gate electrode G is loaded to provide a wider platform to be sure that the gate electrode is received on the p-type GaN layer 5 without overhang. EX1001 at 4:52-54; EX2005 ¶259.

This is consistent with the references that Petitioner cites to show a pair of ledges, where the ledges are common when the base is patterned before the electrode metal is deposited. EX2005 ¶268; EX1011 Fig. 1, ¶[0006] (“processed with two different photomasks”); EX1018 at Fig. 1, Page 1 (“Transistors were then fabricated with... source-drain contacts... Ni/Au contacts were then deposited over the selective area grown *p*-GaN regions.”); EX1017, Figs. 5-6; ¶[0056] (“Referring to FIG. 5, the p-type Al_z GaN cap layer 11 is etched to define a gate region where

the p-type Al₂GaN cap 11 is located. Referring to FIG. 6, a gate 17 with a schottky contact... are formed on the Ga-face to form an assembly.”); EX1007 Fig. 1A, 1B, ¶¶[0061]-[0065].

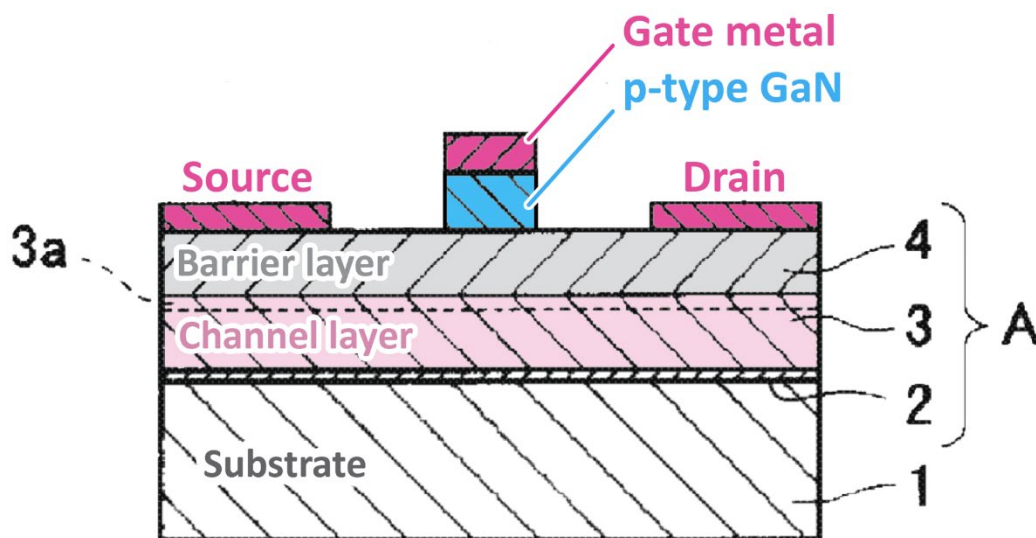
Yoshida does not describe any operational function of the illustrated ledges after the gate electrode is loaded. Rather, as previously discussed, the transistor of Yoshida is assembled to locate the **pn junction** of a p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility.” EX1006 ¶[0017]. This is obtained in the gate-last approach of Yoshida by “etch[ing] away the p-type GaN layer except for where the gate electrode was to be loaded.” EX1006 ¶[0022]; EX2005 ¶¶269-270.



EX1005, Fig. 1 (annotated)

If a POSA were to modify the process of Yoshida to incorporate the “self-

aligned” technique of Beach, this “self-aligned” technique would achieve what Yoshida intends. The p-type GaN layer 5 would be “etch[ed] away... except for where the gate electrode was [] loaded” because the gate electrode G would be self-aligned with the p-type GaN layer 5. EX1006 ¶[0022]. Thus, the pn junction of a p-type GaN layer 5 would be “immediately under” the gate electrode G. EX1006 ¶[0017]. The direct alignment of the gate electrode G with the pn junction would optimize “voltage control with a small amount of carrier injection” as is the intended result of Yoshida. EX1006 ¶[0017]; EX2005 ¶271.



EX1006, Fig. 1 (modified with self-aligned etch of Beach)

Thus, a POSA would not have any reason or motivation to perform additional etching steps to form the claimed ledges that have no disclosed operational function after the gate metal G is loaded on the p-type GaN layer 5. Indeed, Petitioner provides no motivation or reasoning for a POSA to perform additional etching steps

to form ledges that have no disclosed operational function after the gate electrode G is loaded on the p-type GaN layer 5. EX2005 ¶272.

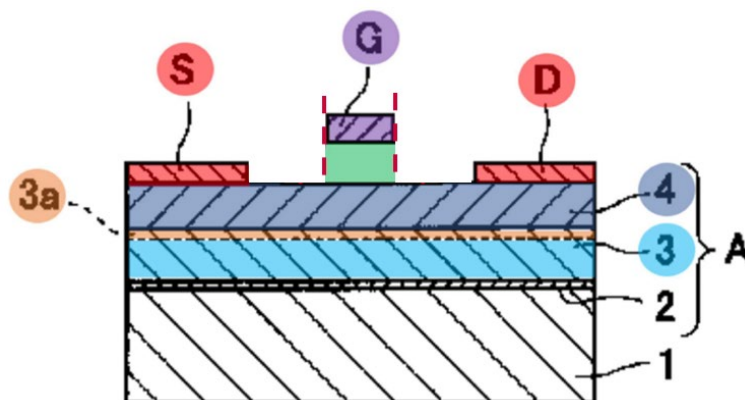
Indeed, the unnecessary etching would add manufacturing cost and steps, producing a less efficient method, contrary to motivations relied on by Petitioner. Pet. 32, 35, 48, 54-56, 64, 77; EX1003 ¶¶93, 205 (“eliminating masking and etching steps,” “reduc[ing] steps and costs” and predictably creating the “stacked gate structure more efficiently”). Petitioner merely relies on the depiction of Yoshida in Fig. 1, which is a schematic of a transistor formed by the p-type GaN layer 5 being etched before deposition of the gate electrode G. EX2005 ¶273. Petitioner is advocating for modifying Yoshida’s process, which results in ledges, with a process in which ledges are not formed, but removed (using *Beach*), and forming ledges by etching the gate electrode G.

Furthermore, selectively etching the gate electrode G after being loaded on the p-type material 5 would be contrary to the intention of Yoshida because it would intentionally reduce the width of the gate electrode G relative to the pn junction creating non-overlapping segments of the pn junction, thus reducing “voltage control” by increasing the required amount of carrier injection. *Id.* ¶274

D. The “self-aligned” technique of *Beach* would not produce the sloped sidewalls of Saxler

Petitioner alleges that “a POSITA would have found it obvious to use Beach’s approach to create and symmetrically align Yoshida-Saxler gate structure for

improved performance.” Pet. 79. However, as discussed above in §VII.F and as acknowledged by Dr. Shealy, applying Beach’s self-aligned technique would either cut off or not form the horizontally extending “sloped” side surfaces that Petitioner relies on from Fig. 1A of Saxler. EX2005 ¶¶301-03.



Pet. 88 (Annotated)

E. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges

Petitioner cites and reiterates Ground 1 in addressing [1i]. Pet. 92-94. This argument fails for the reasons provided in §VII.G. EX2005 ¶¶304-310.

F. A POSA would not have found it obvious to combine Yoshida, Saxler, Beach, and Shenoy

Ground 4 is based again on reverse engineering the schematic of Fig. 1 of Yoshida. Pet. 72 (“resulting in the same gate structure that Yoshida-Saxler discloses”). However, that premise is improper as further discussed with reference to the related transistor schematic as discussed in §VII.C. *Hockerson*, 222 F.3d at 956 (Fed. Cir. 2000).

In again relying on Saxler, Beach and Shenoy in addition to Yoshida, Petitioner's argument has similar deficiencies in motivation and articulating specific steps as further discussed in §VII.H. EX2005 ¶¶311.

For at least those reasons, *Saxler* in view of *Yoshida*, *Beach*, and *Shenoy* does not render obvious claims 1-3 of the '347 Patent.

XI. GROUND 5 (YOSHIDA IN VIEW OF AHN)

At the outset, Ground 5 suffers from the same fatal flaws as the other grounds without *ever presenting a description of the actual proposed modified prior art process*. Rather, Petitioner simply picks and chooses different *features* of the prior art and abstractly asserts that the combination renders the claims obvious, without explaining how the proposed combination would fit into an overall process to arrive at the claimed invention. The Board's "concern regarding Petitioner's asserted reasons to combine Saxler and Ahn" (*see* Paper 11 at 50) is justified because there would be no motivation to combine the two references. First, as discussed above in §X.A, Yoshida discloses specific steps to its process and is not "flexible." EX2005 ¶¶256-259. Indeed, Yoshida teaches away from using other methods of manufacturing its gate because it expressly distinguishes its method from "conventional photolithography and etching" EX1006 ¶¶[0006], [0008,] as further discussed in above in §X.B. EX2005 ¶¶260-264. Second, a POSA would not include additional steps that would add costs to Yoshida's process. EX2005 ¶¶265-

274. Yoshida is a “gate-last” process, Ahn is a “gate-first” process. A POSA would not have looked to a “gate-last” process to modify a gate first process. *See* EX2005 ¶316.

Moreover, Petitioner’s “simple substitution” cannot excuse the proper analysis for obviousness. *MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015) (“[T]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . . [r]ather the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.”).

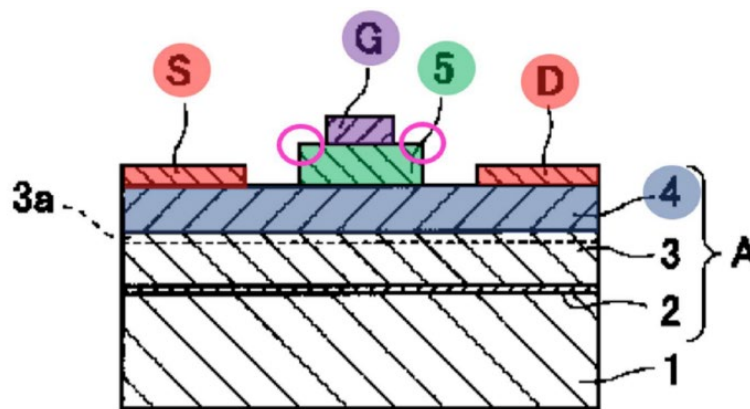
A. A POSA would have no reason to form ledges on Yoshida after aligning the gate metal on the p-type GaN material

As discussed in §X.C, a POSA would not perform any additional etching steps to address [1i] as proposed by Petitioner because the ledges do not have any disclosed function in the operation of the transistor. This unnecessary etching would undesirably add manufacturing cost and steps, producing a less efficient method. *See, e.g.*, Pet. 32, 35, 48, 54-56, 64, 77.

B. A POSA would have no motivation to modify the method of Yoshida based on Ahn

Ground 5 is based on reverse engineering the schematic of Fig. 1 of Yoshida, relying on specific dimensions (w_1 , w_2). Pet. 95-97 (“to obtain the gate structure of Yoshida”).

symmetric with respect to the gate metal” of claim 7 in U.S. Pat. 10,312,335, Petitioner alleges that “Yoshida’s gate electrode is narrower than layer 5, thereby exposing horizontal ledges that extend past the respective sidewalls of the gate electrode and toward the source and drain. Yoshida, [0022]-[0023], Fig. 1; Shealy, [214]. These ledges are symmetric on either side of the gate metal (i.e., having substantially equal widths). Yoshida, Fig. 1; Shealy, [214]. Yoshida thus discloses this element (Ground 4).” EX2007 83.

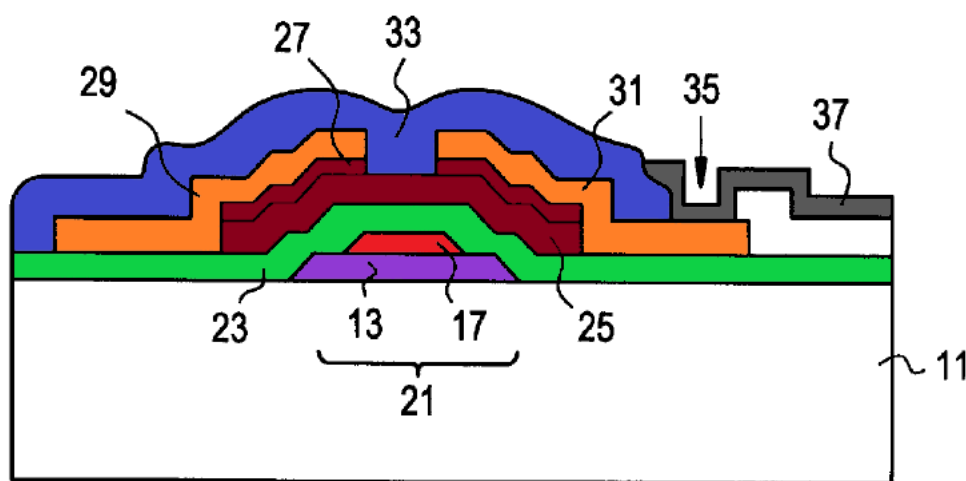


EX2007 83 (annotating EX1006, Fig. 1)

A POSA would not look to another method “to improve alignment and precision” and “to improve alignment and symmetry between layers” of the gate electrode on the p-type GaN material when, according to Petitioner, the gate structure of Yoshida is already aligned with ledges of the p-type GaN being “symmetric on either side of the gate metal.” EX2007 83; EX2005 ¶328. Thus, there is no motivation to combine.

This provides further evidence of Petitioner relying on hindsight in “trying to

Ahn teaches a substantially different gate structure from Yoshida solving an unrelated problem and with different etching methods. As further discussed in §§VI.E, IX.C, Ahn is directed to a thin film transistor having a double-layer metal gate structure to prevent deterioration of a thin overlying gate oxide layer 23 to avoid a short circuit with vertically aligned source and drain electrodes 29, 31. EX1010 1:6-9. A thin film transistor is a special type of FET where the transistor is made by a specific thin film deposition, diverging from GaN HEMTs. EX2005 ¶347.

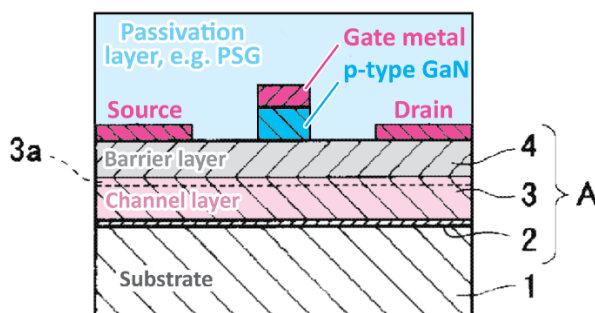


Petitioner vaguely alleges that the structure of Ahn “improves performance and prevents deterioration.” Pet. 95. However, those improvements are not applicable to GaN HEMTs Yoshida, especially to the detriment of the voltage control. §§VI.B, VI.E, IX.C, X.C; EX2005 ¶348. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away

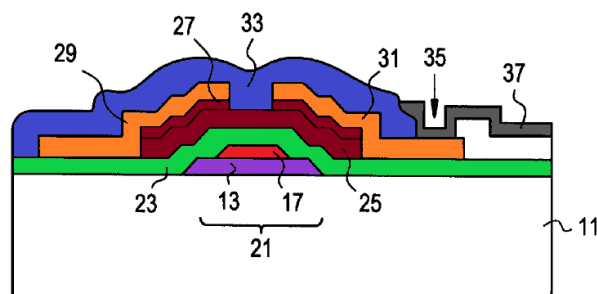
from the claimed invention. MPEP 2141.02-IV (*citing W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552 (Fed. Cir. 1983)).

Yoshida is not a thin film transistor and does not have relevant analogous structure. EX2005 ¶349. Yoshida does not have a thin **gate oxide layer** 23 separating the gate and the **source and drain electrodes** 29, 31. *Id.* Furthermore, Yoshida does not disclose a gate structure of a double-layer metal structure. *Id.*

For example, as similarly discussed in §IX.C, the source and drain of Yoshida are not overlapping with the gate contact nor is the semi-conductive layer separated by a thin gate oxide layer from the gate contact, thus there is no concern in Yoshida for a short circuit as in Ahn (EX1010, 1:35-38). EX2005 ¶331. Rather, as Dr. Shealy states, each of the components are laterally spaced apart by a sufficient distance to avoid a short circuit. EX2004, 65:15-18 (referencing another GaN transistor in Saxler). The 2DEG is formed underneath the gate structure, and not above as in Ahn. EX2005 ¶350. Any passivation layer above the gate is much thicker (e.g., 500 nm to 1,000 nm) than the **gate oxide layer** 23 of Ahn, and would also likely be a different material deposited in a different manner than the thin **gate oxide layer** 23 of Ahn. *Id.*



EX1005, Fig. 1 (modified)



EX1010, Fig. 1F (annotated)

Thus, the deterioration of the thin **gate oxide layer** 23 of Ahn would not be of concern to Yoshida, because Yoshida's structure is substantially divergent from thin film transistors. Therefore, a POSA would not modify the gate structure of Yoshida based on that of the thin film transistor of Ahn to the detriment of the voltage control of Yoshida. §§VI.E, VII.C, X.C; EX2005 ¶352; MPEP 2141.02-IV (*citing W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552 (Fed. Cir. 1983)) ("prior art must be considered in its entirety, including disclosures that teach away from the claims").

C. Petitioner provides no evidence that the slower rate of etching of the cap layer relative to the metal contact has the exact proportionality as that in Ahn to similarly etch such small dimensions precisely

In referencing the different etching rates, Ahn specifically discloses that the etching is successful in forming the double step structure "because of the etching material and metals used for the first and second metal layers of the gate" (EX1010, 7:23-24), where the first metal layer 43 is a conductive metal (Al, Cu, or Au), the second metal layer 45 is a refractory metal (Mo, Ta, or Co) (*Id.* at 5:42-47), and the

etching material is a mixture of phosphoric acid H_3PO_4 , acetic acid CH_3COOH and nitric acid HNO_3 (*Id.* at 7:21-23). EX2005 ¶353.

Merely stating “a POSITA would have understood that Yoshida’s layer 5, which was a p-type doped semiconductor, would have had a slower rate of dissolution than its metallic gate contact and found it obvious to use Ahn’s approach” (Pet. 98) does not provide sufficient “articulated reasoning with some rational underpinning” as required. EX2005 ¶354 Petitioner provides no “articulated reasoning” on the complex interactions of any known etching material with each of the specific p-type doped semiconductor of the gate material and the specific metals of the gate contact of Yoshida and Saxler, as required in the specific relative etching rates of the proposed modification in view of Ahn. *Id.*

XII. RESERVATION OF RIGHTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein. Similarly, Patent Owner does not concede any underlying contentions in the Petition and reserves the right to rebut any such contention later. Further, Patent Owner is not limited to the arguments presented in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented herein.

XIII. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and claim 1 of the '347 patent should be held patentable.

Dated: June 18, 2024

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 13,223 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

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