

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

IPR2023-01382

CERTIFIED COPY

U.S. Patent No. 9,748,347

**INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD. and
INNOSCIENCE AMERICA, INC.,
Petitioners,
v.
EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.**

ORAL DEPOSITION OF JAMES RICHARD SHEALY, PH.D.

Thursday, May 16, 2024

Reported by:

SUSAN ASHE, Certified Electronic Reporter

Job No.: 137277

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1 **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
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4 **IPR2023-01384**

5 **U.S. Patent No. 10,312,335**

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7 -----
8 **INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD. and**
9 **INNOSCIENCE AMERICA, INC.,**

10 **Petitioners,**

11 **v.**

12 **EFFICIENT POWER CONVERSION CORPORATION,**

13 **Patent Owner.**
14 -----

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17 **Oral deposition of JAMES RICHARD SHEALY,**
18 **PH.D., taken on behalf of the Petitioners, beginning**
19 **at 9:03 a.m., on Thursday, May 16, 2024, at the law**
20 **offices of Finnegan, Henderson, Farabow, Garrett &**
21 **Dunner, LLP, 1875 Explorer~Street, Reston, Virginia,**
22 **before Susan Ashe, Certified Electronic Reporter,**
23 **and Notary Public of the Commonwealth of Virginia.**
24
25

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21 **Caitlin Coverstone, Patent Agent**

22 **Finnegan, Henderson, Farabow, Garrett &**

23 **Dunner, LLP**

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EXHIBITS

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Exhibit 2001	Patent Owner's Notice of Deposition of Dr. James Shealy U.S. Patent No. 10,312,335	11
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PREVIOUSLY MARKED EXHIBITS

Exhibit No.		Introduced
Exhibit 1003	Declaration of	
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09:03

09:04

09:04

THURSDAY, MAY 16, 2024;
9:03 A.M. EASTERN DAYLIGHT TIME
--o0o--
Whereupon,
JAMES RICHARD SHEALY, PH.D.
having been first duly sworn, was examined
and testified as follows:
MR. DOSHI: Dipu Doshi, for
Efficient Power Conversion Corporation,
from Blank Rome.
Also with me are Mark Mashack
and Ameya Paradkar.
MS. SPECHT: And Kara Specht,
from Finnegan, for Innoscience, the
petitioner.
And with me is Dr. Luke
MacDonald, Lionel Lavenue, Caitlin
Coverstone -- also from Finnegan.
EXAMINATION
BY MR. DOSHI:
Q. Good morning, Dr. Shealy.
A. Good morning.
Q. How are you?
A. Fine, thanks.
Q. Okay. You've been deposed before?

09:04

1 A. Yes.

2 Q. And so, I'll just give you the short
3 version of the ground rules, which are that the
4 court reporter, or something, is taking all of the
5 words that we're saying today down. So it's

09:04

6 important that we not talk over one another. Okay?

7 And I'm going to try to break every 45 to
8 60 minutes. If you need a break before that time,
9 just let me know and we'll break. But I just ask
10 that if there's a pending question, that you answer
11 the question before.

09:04

12 And then I think....

13 That's the short version --

14 A. Okay.

09:04

15 Q. -- of the ground rules.

16 If anything else comes up, let me know.

17 A. Okay.

18 Q. All right. So what did you do to prepare
19 for today's deposition?

09:05

20 A. Okay. I got these binders in the mail
21 about two weeks ago -- maybe two and a half weeks
22 ago, I think.

23 And then about a week ago, we had two
24 Zoom, like, prep sessions with these three lawyers
25 here.

09:05

09:05 1 And then we had, the day before yesterday
2 and yesterday, in-office prep session.

3 Q. Great. And did you speak with anyone
4 other than the Finnegan lawyers in preparing for
09:06 5 today's deposition?

6 A. No.

7 Q. Did you review documents, other than those
8 that you said were shipped to you?

9 A. There's two binders for each patent -- one
09:06 10 exhibits, one pleadings.

11 So, I've looked at those.

12 Q. Okay.

13 A. And that's all I've looked at.

14 Q. Okay. And just to be clear, you said "the
09:06 15 two patents."

16 So it's your understanding that we're
17 talking about the '347 and '335 patents today?

18 A. Yes.

19 Q. Okay. And so for the record, I'll say
09:06 20 that the '347 patent is 9,748,347.

21 Is that your understanding?

22 A. That's correct.

23 Q. And that is for IPR2023-01382.
24 Is that correct?

09:06 25 A. That's correct.

09:06 1 Q. All right. And the '335 patent, the full
2 number for that is 10,312,335.
3 Do you agree?
4 A. Yes.

09:07 5 Q. All right. And that is for IPR2023-01384.
6 Correct?
7 A. Yes.

8 Q. Okay, great.
9 All right. So you have authored a total
09:07 10 of four declarations for four patents that are
11 assigned to EPC. Correct?
12 A. Yes. But I've only reviewed these two for
13 today.
14 Q. Understood. That's great.

09:07 15 MR. DOSHI: Okay. So I'm going
16 to hand you -- this is more of a formality
17 than anything else and just for the
18 record -- a notice of deposition of
19 Dr. James Shealy.

09:07 20 So we'll mark this as....
21 (Pause.)
22 MR. DOSHI: Bear with us.
23 THE WITNESS: Sure.
24 (Pause.)

09:07 25 MR. DOSHI: So we'll go with

09:07 1 2001.
2 (Whereupon, Exhibit 2001 was marked for
3 identification.)
4 MR. DOSHI: And that's 1382,
09:09 5 2001 -- so, it's complicated.
6 And I'm handing you what's going
7 to be also 2001 for 1384, a notice of
8 deposition.
9 COURT REPORTER: It's 2001
09:09 10 again?
11 MR. DOSHI: Yeah -- I know, it's
12 complicated.
13 (Whereupon, Exhibit 2001 was marked for
14 identification.)
10:25 15 BY MR. DOSHI:
16 Q. And again, this is more for formalities
17 than anything else.
18 A. Okay.
19 Q. And have you seen these documents before,
09:10 20 the ones I just handed you -- 2001, 1382?
21 A. I don't -- I don't recall. I might have
22 received them in an email or something. But....
23 MR. DOSHI: Okay. Let me hand
24 you what has previously been marked as
09:10 25 1003, Exhibit 1003 in the 1382 proceeding.

09:10 1 (Whereupon, Exhibit 1003, previously
2 marked, was presented to the witness.)
3 BY MR. DOSHI:
4 Q. Do you recognize that document?
09:11 5 A. Yes.
6 Q. Okay. And that is -- what?
7 A. That's my declaration for the '347 patent.
8 Q. And I'm handing you 1384, what's been
9 marked as 1003.
09:11 10 It's been previously marked, so you don't
11 have to mark it.
12 Do you recognize that document?
13 A. Yes.
14 Q. And what do you recognize that to be?
09:11 15 A. That's my declaration for the '335 patent.
16 Q. Okay. So those two declarations are
17 documents that you reviewed in preparation for
18 today's deposition?
19 A. Yes.
09:12 20 Q. Okay. And do you have your own -- you
21 have your own copy?
22 A. Yes.
23 Q. Okay. That has notes and stuff in there?
24 A. No; no notes.
09:12 25 Q. Okay. And you can use your own copy if it

09:12 1 has no notes in it.

2 A. No; there's no notes.

3 Q. Okay. If you're comfortable with that.

4 So the declarations that I've handed you

09:12 5 have your opinions on the validity of the two

6 patents. Correct?

7 A. Correct.

8 Q. In formulating your opinions, did you

9 speak with anyone outside of the Finnegan attorneys?

09:12 10 A. No.

11 Q. Okay. Other than the documents that you

12 cite in your reports for your declarations, did you

13 review any other documents?

14 A. Yes.

09:13 15 Q. Okay. And do you recall what those

16 documents were?

17 A. The patent owner response, the Board

18 decisions and, you know, all the references.

19 I'm trying to think if I'm forgetting

09:13 20 anything. Let me look....

21 We have all the pleadings for each case.

22 And so, there's -- so I've looked at all

23 of these: the petition, the patent owner response,

24 the petitioner preliminary reply, the patent owner

09:14 25 sur reply, and then the institution decision.

09:14 1 So I looked at all of those -- for each
2 patent.

3 Q. Have you spoken with anyone about the
4 ongoing litigation between EPC and Innoscience?

09:14 5 A. No -- well, other than this case.

6 I mean, I don't know if this is considered
7 a litigation, but....

8 It is, isn't it?

9 Q. Sure.

09:14 10 A. Yeah.

11 Q. How did you come about being an expert for
12 Innoscience?

13 A. I think I was contacted. I don't remember
14 by who, but one of the attorneys.

09:14 15 And I had done work for Finnegan before.
16 I don't know if that had any bearing on it.

17 But they contacted me and we discussed it.
18 And then we decided I would be the expert in these.

19 Q. Okay. And do you recall when you were
09:15 20 contacted by Finnegan?

21 A. It's been a while. So I can't really give
22 you an accurate date. But....

23 Q. 2023?

24 A. I would say something on the order of a
09:15 25 year ago, maybe -- is my guess.

09:15 1 Q. Spring 2023?

2 A. Something like that, yeah.

3 Q. Okay. In Paragraph 3 of your declaration

4 for the '347, you say that you're being compensated

09:15 5 for your time at your standard hourly consulting

6 rate.

7 What is your consulting rate?

8 A. Yes, I see that. 750 an hour.

9 Q. Okay. And you state that you have no

09:15 10 other interest in this proceeding.

11 Is that correct?

12 A. No -- I mean, what do you mean? "No

13 interest"?

14 Q. It's on Paragraph 3 -- so, if you can look

09:16 15 at Paragraph 3, the last part of that sentence, the

16 last sentence.

17 A. No. I have no other interest in this

18 proceeding.

19 Q. Okay. Other than publicly available prior

09:16 20 art and the documents you discussed, did counsel

21 provide you with any material -- any other material

22 from the --

23 Well, let me back up.

24 Do you understand that there is a pending

09:16 25 ITC investigation between EPC and Innoscience?

09:16 1 A. Yes.

2 Q. Okay. Did counsel provide you with any of

3 the documents from that investigation?

4 A. No.

09:16 5 Q. Okay. Have you had discussions with

6 Dr. Levy?

7 A. No.

8 Q. Okay. Do you know who Dr. Levy is?

9 A. Not really.

09:17 10 Q. Okay. Dr. Levy --

11 A. Georgia Tech, was it? Or....

12 Q. That's a good question. I don't know.

13 Do you know if Innoscience has another

14 expert that opined on invalidity in connection with

09:17 15 the ITC investigation?

16 A. I don't know who it is, and I have no

17 information on that. So....

18 Q. Okay. Were you provided with any

19 deposition transcripts to review in --

09:17 20 A. No.

21 Q. Any emails from Dr. Levy?

22 A. No.

23 Q. Any hearing transcripts?

24 A. No.

09:17 25 Q. Did you discuss your -- I think I asked

09:18 1 this, but I'm going to phrase it a little
2 differently.

3 Did you discuss your involvement in
4 this -- in these proceedings with anyone outside of
09:18 5 your lawyers?

6 A. No.

7 Q. Did you speak with some of your colleagues
8 at work about this?

9 A. No.

09:18 10 Q. Did you inform them of your involvement in
11 this case?

12 And let me clear that up.

13 Have you informed your colleagues of your
14 involvement in this case?

09:18 15 A. No. They know I'm out of town for a week.
16 But other than that, no.

17 Q. All right. Let's turn to Paragraph 19
18 of --

19 A. Where, the '347?

09:18 20 Q. '347.

21 In 2019, you co-founded Odyssey
22 Semiconductor. Correct?

23 A. Where did you say?

24 Q. I'm sorry. Paragraph 19. Page 5.

09:19 25 A. Oh, Paragraph 19. Okay.

09:19

1

(Pause.)

2

A. Okay.

3

Q. In Paragraph 19, you quote -- you say,

4

quote:

09:19

5

I co-founded Odyssey

6

Semiconductor, end quote.

7

Do you see that?

8

A. Yes.

9

Q. What is the business of Odyssey

09:19

10

Semiconductor?

11

A. Odyssey Semiconductor is engaged in

12

designing and building prototypes of vertical

13

high-power gallium nitride transistors.

14

Q. Okay. Can you elaborate on what the

09:20

15

day-to-day operations of Odyssey Semiconductor are?

16

A. We have a semiconductor fab. So we

17

take -- we do not produce gallium nitride epitaxy.

18

So we procure that.

19

And we conduct semiconductor processes to

09:20

20

create vertical FETs in that host material.

21

And so, those devices involve plasma

22

etching, several types of plasma etching, metal

23

deposition, dielectric deposition -- you know, all

24

of the photolithography -- everything you associate

09:21

25

with building a gallium nitride device.

09:21 1 It's not the same device, as these are
2 lateral conduction devices.

3 So vertical conduction is a totally
4 different animal, but it uses a lot of the same
09:21 5 fabrication techniques.

6 Q. Understood.

7 And when you say it's not the same as
8 these, you're pointing to the patents?

9 A. Yes. These are -- these two patents --
09:21 10 and all of the prior art references all describe --
11 well, not all the prior art, but much -- much of the
12 prior art describes lateral conduction Field Effect
13 Transistors. And they're often referred to as
14 "HEMTs."

09:22 15 I used to build HEMTs at Cornell back in
16 the late '90s.

17 We built the first gallium nitride HEMT on
18 silicon, which is the basis for all of this
19 technology.

09:22 20 We were also the first to build an
21 insulated gate transistor on gallium nitride. And
22 we developed nucleation methods, which are -- appear
23 to be dominating the -- you have to nucleate these
24 materials when you grow them on silicon or sapphire,
09:22 25 a different semiconductor substrate.

09:22 1 And so, we've -- we were the first --
2 well, "first" -- we -- Nakamura came up with a
3 nucleation method. That's what the world used.
4 We came up with one in the mid '90s which
09:23 5 replaced that and works better, and now that's
6 heavily in use. And that's also patented.
7 Q. Okay. Thank you.
8 Going back to Odyssey, you say that the --
9 you don't do -- Odyssey doesn't have its own epi.
09:23 10 A. That's correct.
11 Q. Okay. So when we say "epi," we're talking
12 about the growth of the layers up to what level?
13 A. Well, the epitaxial structure for a
14 vertical device is obviously different than a HEMT.
09:23 15 But -- so the vertical device would
16 typically have three to five layers in it, and
17 they're all gallium nitride, and they're all doped
18 n-type.
19 Q. Okay. And where does Odyssey
09:23 20 Semiconductor source that material from?
21 A. We've sourced it from a lot of places.
22 But, currently, we're collaborating with
23 Sandia Labs, and they're providing us all the
24 epitaxial material there.
09:24 25 They're actually experts. They've been at

09:24 1 it a long time -- as have I. I mean, when I was at
2 Cornell, we -- my group designed and built MOCVD
3 reactors to grow gallium nitride.

4 So I've been involved in the -- heavily
09:24 5 involved in the epitaxy end of things.

6 Q. Has Odyssey Semiconductors sourced any
7 material from Innoscience?

8 A. No.

9 (Pause.)

09:24 10 A. Maybe I should have said: The vertical
11 transistors are grown on a gallium nitride
12 substrate.

13 And as far as I know, neither one of these
14 parties involved here work with gallium nitride
09:25 15 substrates.

16 So it's a single crystal, low-defect
17 density sort of arrangement.

18 Q. And that would be the substrate?

19 A. The substrate is low-defect density. We
09:25 20 source those from Japan.

21 But the -- it's also a conducting
22 substrate. And when you're doing HEMTs, you're
23 looking for an insulating substrate, generally.

24 So there's a lot of differences, right
09:25 25 from the substrate all the way up.

09:25 1 Q. And you say in Paragraph 19 on Page 5
2 that:
3 Odyssey Semiconductor also
4 recently developed the
09:25 5 fabrication techniques.
6 How recently did Odyssey Semiconductor
7 develop the fabrication techniques?
8 A. This is referring to micro-LED arrays.
9 To help pay the bills, we do foundry work
09:26 10 because we have a fab.
11 So there's two or three companies that
12 have approached us, and we've done micro-LED work
13 for two companies.
14 So that also involved a lot of the same
09:26 15 core sets of gallium nitride-based Light Emitting
16 Diode. And a lot of the same fabrication techniques
17 that were used there are also used kind of generally
18 to process gallium nitride and related materials.
19 Q. Where are Odyssey Semiconductor's fabs
09:26 20 located?
21 A. There's only one fab. It's in Ithaca, New
22 York -- at the airport.
23 Q. Let's go back to your....
24 How many times have you been deposed?
09:27 25 A. I don't know. Somewhere between, I'd say,

09:27 1 ten and twenty times.

2 Q. Have you testified at trial?

3 A. Do you consider ITC trials?

4 Q. Sure.

09:27 5 A. I've done, I think, three ITC trials.

6 I've only done one district court trial in

7 front of a live jury.

8 Q. Okay.

9 A. But...I think that covers it.

09:27 10 Q. Okay. Do you know Dr. Schubert?

11 A. Yes.

12 Q. How do you know him?

13 A. I've known him a long time.

14 Back when he was at Bell Labs is when I

09:27 15 first met him. He used to come up and visit us at

16 Cornell.

17 But I was his expert when he was going

18 around litigating his patent. So I know him from

19 that as well.

09:28 20 Q. You said you've testified at a jury trial.

21 What did that trial involve?

22 A. That involved Light Emitting Diodes used

23 for, you know, commercial lighting lamps.

24 Q. Okay. And then the three ITC trials, what

09:28 25 did those involve?

09:28 1 A. The first one involved...the....
2 All right. Now you're taking me back a
3 decade or so.
4 Q. To the best of your recollection.
09:29 5 A. The first one involved a patent that -- I
6 can't even remember the....
7 The patent involved gallium nitride
8 materials, in general.
9 And the other ITC trial was a -- involved
09:29 10 Light Emitting Diodes again.
11 And that, I think....
12 And then, the last ITC trial I did was
13 involving the electronic circuits to drive LEDs.
14 Q. Have you worked with EPC at all?
09:30 15 A. No. I discussed working with them, but I
16 never have worked for them.
17 Q. Do you know Alex Lidow?
18 A. No.
19 Q. Do you know any of the inventors on the
09:30 20 '347 patent?
21 A. No.
22 Q. Okay. Earlier, you said that you do
23 foundry work because you have a fab.
24 Is that right?
09:31 25 A. Yes.

09:31 1 Q. And there are two or three companies that
2 approached you.

3 Is that right?

4 A. There's been a lot of companies that have
09:31 5 approached us.

6 We've done a lot of fab work for a lot of
7 different companies I just mentioned.

8 I was responding to your question about
9 the micro-LED arrays.

09:31 10 Q. Okay. What other companies have you done
11 work for?

12 A. There's a company called "Innovation." I
13 don't know if there's anything beyond "Innovation."
14 That's what I call them.

09:31 15 They -- they're in -- I think they're
16 based in Rochester. And we've built micro-LED
17 arrays for them.

18 There was another Canadian company we did
19 that for, and I -- VueReal, I think -- or VueReal,
09:32 20 or something, was their name.

21 And then we've done a lot of odd jobs
22 for -- you know, I'm not really involved in the
23 foundry part of that. So....

24 But the...there's a company in Buffalo
09:32 25 we're currently building some nuclear batteries,

09:32 1 using GaN.
2 And then there's many others I just can't
3 remember.
4 Q. Do any of the companies design gallium
09:32 5 nitride transistors?
6 A. I think we've done one job involving HEMTs
7 and gallium nitride, yeah.
8 Q. Can you tell me any details about that
9 job?
09:33 10 A. We just -- there was a company interested
11 in integrating HEMTs with another device.
12 And so, we -- they provided us with some
13 substrates. And HEMTs are, by comparison, much
14 easier to fabricate than a vertical GaN transistor.
09:33 15 And so, we just built some standard HEMTs
16 for them, using, more or less, the techniques
17 that -- we kind of imported the technology from
18 Cornell, obviously, into this company. So we have
19 certain ways of building HEMTs.
09:33 20 And so, we've carried that -- those out.
21 Q. Okay. And which company was that?
22 A. I can't tell you off the top of my head.
23 It wasn't a big HEMT company like the two
24 players here.
09:34 25 It was a small company. I just don't

09:34 1 remember the name.

2 Q. Have you had discussions with any
3 Innoscience employees in formulating your opinions?

4 A. No.

09:35 5 Q. So it was just the one company that you
6 were focused on making HEMTs for?

7 A. Yeah, it was....

8 Like, you know, we built them, tested
9 them, shipped them out. And that was the end of it.

09:35 10 Q. And that was in your fab in New York?

11 A. That's correct.

12 Q. And the way that works is that epitaxial
13 layers are sourced from somewhere and then shipped
14 to your fab?

09:35 15 A. Yes.

16 Q. Do you know where those epitaxial layers
17 were shipped from?

18 A. No. I don't remember the details of the
19 job. I just know that the job did happen, because I
09:36 20 was consulted on some of the fabrication issues on
21 it.

22 MR. DOSHI: Why don't we take a
23 short break --

24 THE WITNESS: Okay.

09:37 25 MR. DOSHI: -- because I'm about

09:37 1 to switch topics.
2 Can we go off the record.
3 (Whereupon, a recess was taken
4 from 9:37 a.m. until 9:49 a.m.)
09:49 5 BY MR. DOSHI:
6 Q. Dr. Shealy, welcome back.
7 A. Thank you.
8 Q. Before the break, we were talking about
9 HEMTs. And I just want to clarify for the record,
09:49 10 it's H-E-M-T. Correct?
11 A. High Electron Mobility Transistor, yeah.
12 Q. Thank you.
13 MR. DOSHI: All right. I'm
14 handing you what has previously been
09:49 15 marked as 1007.
16 So this is 1007 in both 1382 and
17 1384.
18 THE WITNESS: These aren't being
19 marked now?
09:49 20 COURT REPORTER: They're
21 premarked.
22 THE WITNESS: Oh.
23 MR. DOSHI: They've been marked.
24 (Whereupon, Exhibit 1007, previously
09:49 25 marked, was presented to the witness.)

09:49 1 THE WITNESS: Okay -- oh, yeah.

2 BY MR. DOSHI:

3 Q. And do you recognize this document?

4 A. Yes.

09:50 5 Q. What do you recognize it to be?

6 A. Excuse me?

7 Q. What do you recognize it to be?

8 A. This is a prior art reference authored by
9 Saxler.

09:50 10 Q. Okay. And you rely on this document in
11 your opinions. Correct?

12 A. Yes.

13 Q. Okay. Looking at Figure 1A of Saxler, it
14 shows a transistor having a recessed gate structure.
09:50 15 Correct?

16 A. Yes.

17 Q. Okay. And then 1B shows a nonrecessed
18 transistor.

19 Is that right?

09:50 20 A. 1B is some sort of idealized....

21 Yes, it's....could you repeat that
22 question? Sorry.

23 Q. Sure. 1B shows a -- let me try it again.

24 1B of Saxler shows a nonrecessed

09:50 25 transistor. Right?

09:51 1 A. It shows a transistor where the gate isn't
2 recessed.

3 Q. Okay. And then, you said -- turning to
4 Figures 2 and A -- 2A and 2B on the next page.

09:51 5 Do you see that?

6 A. Yes.

7 Q. Yeah. It seems like they reversed it.
8 Right?

9 A and B is now reversed. And it looks
09:51 10 like 2A is the nonrecessed transistor. Right?

11 A. In that depiction, yes, the gate is not
12 recessed.

13 Q. And 2B is the recessed transistor?

14 A. The gate is recessed into the barrier
09:51 15 layer in 2B.

16 Q. Into the barrier layer in 2B, yes -- okay.
17 Thank you.

18 And on Page 41 of your declaration -- so,
19 let's go to your report here.

09:51 20 Sorry. I'm using things interchangeably.

21 Do you want to refer to your declaration
22 as a particular noun? Is there something --

23 A. Sure. Let's refer to the declaration,
24 yeah.

09:52 25 Q. Okay, declaration.

09:52 1 Page 41 of your declaration, you have an
2 illustration.

3 Do you see that?

4 A. Yes.

09:52 5 Q. And what is that illustration?

6 A. That is an illustration of a nonrecessed
7 gate.

8 So you start with Figure 1A and you remove
9 the gate recess. And that's what you get when you
09:52 10 remove the gate recess and change nothing else.

11 Q. Okay. And the modified structure is
12 something you put together?

13 A. Yeah, it was my opinion to -- that's what
14 it means to recess the gate -- or to remove the
09:53 15 recess, leave everything else the same. Let's just
16 remove the recess.

17 Q. And this illustration is not in Saxler.
18 Correct?

19 A. It's described in Paragraph 52, I think,
09:53 20 pretty effectively, if you want to look at that.

21 Q. We'll get there.

22 A. Okay.

23 Q. What I'm asking is: This depiction is not
24 from Saxler. Correct?

09:53 25 A. It's a modified version of a figure from

09:53 1 Saxler.

2 Q. And you modified it. Right?

3 A. Yes.

4 Q. And then, did you use Photoshop -- or how

09:53 5 did you come about this?

6 A. I think I probably told somebody to modify

7 it. Somebody else did it on the computer.

8 Q. Okay. So we'll call....

9 Okay. You say that -- in your

09:53 10 declaration, you say that the recess is optional.

11 Right?

12 A. Saxler says that again and again.

13 Q. Okay. And you cite to a couple of

14 paragraphs that you say support your conclusion that

09:54 15 it's optional. Right?

16 A. Yes.

17 Q. And then one of them is the abstract.

18 Right?

19 (Witness reading.)

09:54 20 A. I don't see any discussion of a gate

21 recess in the abstract.

22 Q. Okay.

23 A. There's an Ohmic contact without a

24 recess --

09:54 25 Q. That's right.

09:54 1 A. -- mentioned in the abstract.
2 Q. Okay. And then, another Paragraph is 13.
3 You're looking at Paragraph 13.
4 A. Yes.

09:55 5 Q. And then, the first sentence says:
6 In particular embodiments
7 of the present invention
8 without a gate recess....
9 A. Wait a minute, where are we reading?

09:55 10 Q. Paragraph 13 of Saxler.
11 A. Saxler?
12 In other embodiments?
13 Q. In particular embodiments.
14 A. My version of this says "in other
09:55 15 embodiments."
16 Q. Oh, I'm sorry. It's line....
17 Well, there are no lines.
18 It's the fifth line from the top:
19 In particular
09:55 20 embodiments....
21 A. In that paragraph? Or the....
22 Q. Yeah, in Paragraph 13.
23 (Witness reading.)
24 A. Okay.

09:55 25 Q. Okay. It says:

09:55 1 In particular embodiments
2 of the present invention with a
3 gate recess, the doped region
4 extends into the cap layer from
09:56 5 about 30 angstroms to about
6 5000 angstroms.
7 Is that right?
8 A. Yes.
9 Q. Okay. And then, the sentence that
09:56 10 follows -- well, actually, if you go up from there,
11 the second line from the top, it says:
12 In particular embodiments
13 of the present invention
14 without a gate recess, the
09:56 15 doped region extends into the
16 cap layer from about 2.5
17 angstroms to about
18 15 angstroms.
19 Do you see that?
09:56 20 A. Yes.
21 Q. So there are differences between the two
22 embodiments. Correct?
23 A. There are many other embodiments where I
24 don't think those differences show up.
09:56 25 But in Paragraph 13, what you said is

09:56 1 correct.

2 Q. And you cite to Paragraph 13. Right?

3 A. I cite many others as well.

4 Q. Okay. So let's go to Paragraph 27.

09:56 5 That's another one that you cite to. Correct?

6 A. From Page 41 of the declaration? I don't

7 see 27 mentioned there.

8 Q. All right. Paragraph....

9 So if you flip to Page 63 of your

09:57 10 declaration, Paragraph 122. You say:

11 The recess in Saxler's cap

12 layer 24 is optional.

13 And you cite to Paragraph 27.

14 A. Okay.

09:58 15 Q. Yeah. So if we go back to Saxler at

16 Paragraph 27.

17 Here again, it says:

18 And the transistor may

19 further include a gate contact

09:58 20 recessed into the aluminum

21 nitride cap layer --

22 I'm on -- one, two, three, four, five --

23 six from the top.

24 A. Yes.

09:58 25 Q. (Continued reading:)

09:58 1 In such embodiments, the
2 aluminum layer has a thickness
3 of -- from about 5 to about
4 5000 angstroms.

09:58 5 Do you see that?

6 A. Yes.

7 Q. Okay. And -- one, two, three, four,
8 five -- six from the bottom:

9 The transistor may also

09:59 10 include a gate contact on the
11 aluminum nitride cap layer and
12 not recessed into the aluminum
13 nitride cap layer. In such
14 embodiments, the aluminum

09:59 15 nitride cap layer has the
16 thickness of about -- or from
17 about 2 angstroms to about
18 20-angstroms.

19 Do you see that?

09:59 20 A. Yes.

21 Q. Okay. So there are, again, differences in
22 the thickness of the cap layer. Correct?

23 A. In the embodiments described in
24 Paragraph 27, yes.

09:59 25 Q. Okay. And so, there are differences

09:59 1 between the recessed and nonrecessed embodiments.
2 Correct?
3 MS. SPECHT: Objection; form.
4 A. I wouldn't agree with that.
09:59 5 If you go to Paragraph 52, we could -- I
6 could explain that a little better.
7 Q. Okay. Let's go to 52.
8 (Pause.)
9 Q. I'm there.
10:00 10 A. Okay. 52 -- in Paragraph 52, they're
11 referring to Figures 1A through 6. And they --
12 (Reading:)
13 Thus, while embodiments of
14 the present invention are
10:00 15 described herein with reference
16 to a recessed gate structure or
17 a nonrecessed gate structure,
18 other embodiments of the
19 present invention may include
10:00 20 or not include a gate recess.
21 So I interpret that to apply to Figure 1A.
22 Q. Okay. Despite the differences between the
23 recessed and nonrecessed embodiments that are
24 specifically recited in Saxler?
10:00 25 A. Yes. Because a p-doping can be doped

10:00 1 throughout, and it can be on the surface.
2 You know, I think you can -- they
3 basically say you can....
4 It further says:

10:01 5 Embodiments of the present
6 invention not be -- should not
7 be construed as limited to the
8 particular exemplary
9 embodiments.

10:01 10 So I read that to mean it could be doped
11 throughout if you want to.

12 Q. Okay. But the Saxler paragraphs that we
13 went through describe differences between the
14 recessed and nonrecessed embodiments in terms of
10:01 15 thicknesses and in terms of dope in regions.
16 Correct?

17 MS. SPECHT: Objection; form.

18 A. It was pretty clear what was stated in
19 those paragraphs. So....

10:02 20 Q. Okay. But it's your opinion that 52
21 allows for the -- allows for what, exactly?

22 A. Well, allows for just what it says:

23 The embodiments of the
24 present invention should not be
10:02 25 as -- construed as limiting to

10:02 1 the particular exemplary
2 embodiment.
3 So I think you can take all the
4 embodiments, and mix and match. That's kind of what
10:02 5 that means to me.
6 Q. So it's your opinion that Saxler provides
7 support for any gallium nitride transistor?
8 MS. SPECHT: Objection;
9 mischaracterization.
10:02 10 Q. Based on Paragraph 52?
11 A. No.
12 Q. Okay. So what are the parameters that are
13 limited in Paragraph 52?
14 A. What they describe in this patent.
10:02 15 So, Figures 1A through 6, I read that as
16 it's fair game to pull the recess out of any of
17 those figures. And they give a variety of
18 discussion of dopants, different types of dopants,
19 different distributions.
10:03 20 So I think all those embodiments could be
21 brought into 1A, modified.
22 Q. That also talks about different
23 thicknesses in the recessed and nonrecessed. Right?
24 A. It -- in those paragraphs, it did say the
10:03 25 cap layer was a different thickness.

10:03 1 Q. So in your opinion, you can mix and match
2 all of that?

3 MS. SPECHT: Objection;
4 mischaracterizes prior testimony.

10:03 5 A. It means that you can -- within -- you can
6 take what's in the embodiments and mix and match.
7 That's what I mean, because -- because of the
8 language that appears in 52.

9 They're not -- these -- none of these
10:04 10 embodiments are limiting.

11 Q. Okay. So in your opinion, does Saxler,
12 based on Paragraph 52, allow for multiple recesses
13 in the cap layer?

14 A. That's not in Saxler. I don't really have
10:04 15 an opinion on that. I haven't....

16 So I'm not sure where -- you know, what
17 you're getting at, but I don't have an opinion on
18 it.

19 Q. You don't have an opinion on that?

10:04 20 A. Multiple recesses? No.

21 Q. Okay. Could it have vertical sidewalls?

22 A. Could what have vertical sidewalls?

23 Could a recess? Or....

24 Q. Could the recess have vertical sidewalls,
10:04 25 yes.

10:04 1 MS. SPECHT: Objection;
2 foundation.
3 A. Not generally, no.
4 Q. Does. Does Saxler....
10:04 5 Let's go back to Paragraph 27.
6 There it's talking about the cap layer
7 thickness. Right?
8 A. Yes.
9 Q. And there is a wide range from about 5 to
10:05 10 about 5000 angstroms for the thickness of the cap
11 layer. Right?
12 A. Correct.
13 Q. And that's in connection with the recessed
14 embodiment. Correct?
10:05 15 A. Yes.
16 Q. And then if we go down below, we're
17 talking about a thickness of 2 to 20 angstroms for
18 the nonrecessed embodiment. Correct?
19 A. That's what it says.
10:06 20 Q. Okay. In your opinion, does Paragraph 52
21 allow for a nonrecessed cap layer to have
22 5000 angstroms thickness?
23 MS. SPECHT: Objection; form.
24 A. As I said before, I think you could take
10:06 25 all the embodiments and bring in which ones you

10:06 1 want, depending on what you're trying to accomplish.

2 Q. So in your opinion, are there any
3 transistor -- are there any gate structures that are
4 outside the scope of Saxler?

10:07 5 A. You mean, in general --

6 Q. Yes.

7 A. -- out there in the world?

8 Of course, there are.

9 Q. Which ones?

10:07 10 A. How about a T gate for a microwave
11 transistor? That's not described in Saxler.

12 Q. I'm not talking about application. I'm
13 talking about the gate structure shape.

14 A. There are T gates. There are W gates.

10:07 15 There's V gates used in microwave devices. There
16 are many types of gate structures.

17 Q. So there are certain....

18 But in your opinion, aren't Saxler just --
19 isn't Saxler just providing some examples?

10:07 20 A. Of gate structures?

21 Q. Yes.

22 A. Yeah, there's examples of gate structures
23 in Saxler.

24 Q. So are you saying that T gate structures
10:07 25 are not disclosed by Saxler?

10:08 1 A. Well, Figure 1A has a gate contact that
2 kind of looks like a T, but those aren't the same
3 kind of gates used in microwave devices.

4 So you asked: Are there any other types
10:08 5 of gates? And there are a lot. And they -- a lot
6 of the differences appear in microwave devices,
7 which these are not, generally.

8 Q. Okay. So are there any gate structures
9 that fall outside the scope of Saxler, in your
10:08 10 opinion, that would be specific for HEMTs?

11 A. As I said, there's a lot of other gate
12 structures used in HEMTs that aren't described in
13 Saxler.

14 Q. All right. You mentioned "T gate," but I
10:08 15 think Saxler talks about T gates. Right?

16 A. Yeah, he does have a gate that looks like
17 a T gate, but that's not the way you would do it in
18 a microwave device. So the entire gate structure is
19 different, even though it kind of is -- 1A kind of
10:09 20 looks like a T metalization.

21 Q. What's different about a microwave gate?

22 A. You're not going to load a microwave gate
23 with this cap layer. It will introduce too many
24 parasitics.

10:09 25 Q. In your opinion, does Saxler provide

10:09 1 support for a gate structure having step sidewalls?

2 MS. SPECHT: Objection;

3 foundation.

4 A. Which -- could you tell me exactly what
10:10 5 you mean by a "step sidewall."

6 Q. Are you familiar with "step sidewalls"?

7 A. I think I know what it means. I want to
8 make sure.

9 Q. Okay. What's your understanding of that?

10:10 10 A. Well, it means the sidewall would be
11 basically looking like maybe a staircase or
12 something.

13 Q. Okay. So with that understanding, does
14 Saxler provide support for a gate structure having
10:10 15 step sidewalls?

16 A. I don't believe so.

17 I could read Saxler and answer that with a
18 better certainty, but I don't believe it's in there.

19 Q. Does Saxler provide any support for a
10:11 20 vertical sidewall in its cap layer?

21 A. Let's see...if you look at Paragraph 42 of
22 Saxler.

23 Q. I'm there.

24 A. So they're talking about etching these
10:11 25 walls. And they say typically they have tapered,

10:11 1 rounded, or curved features -- which is true.
2 The etching processes that are used to
3 etch that material do not produce the vertical
4 sidewalls.

10:13 5 Q. You discuss vertical sidewalls in your
6 declaration. Right?

7 A. I believe there's a discussion
8 of...describing walls.

9 Q. Um-hum. And in your opinion --

10:13 10 A. Do you want to point me to where in the
11 declaration you're talking about?

12 Q. Let me try to find it.
13 Paragraph 72, on Page 35.

14 A. Okay.

10:14 15 Q. I'm sorry, 43, 43.

16 A. You said "Paragraph 72"?

17 Q. "35" -- wait, I'm sorry.
18 You say, "Few structures, if any...."
19 I'm on -- one, two, three, four, five --
10:14 20 five from the top, "Few structures...."
21 Do you see that?

22 A. Yes.

23 Q. You say:
24 Few structures, if any,
10:14 25 have perfectly vertical

10:14

1 sidewalls in practice.

2 That's your opinion. Right?

3 A. It takes extra processing steps to get a
4 vertical sidewall, and none of those steps are
10:14 5 described in any of these references. So....

6 So, really, there's no vertical walls in
7 an actual "cell-G" (phonetic) device.

8 Q. What extra processing steps would be
9 required to get vertical sidewalls?

10:15

10 A. I'd like to make a drawing to illustrate
11 that. Is that okay?

12 It will answer your question.

13 Q. Sure.

14 A. Okay. So I'll make a diagram and try to
10:15 15 describe it as I make it.

16 We start with a semiconductor surface of
17 gallium nitride or aluminum gallium nitride. We
18 pattern photoresist on it.

19 So this is photoresist (indicating).

10:16

20 So, so far, we just have a planar gallium
21 nitride surface with photoresist on it. Okay?

22 And then what we do is: We subject this
23 sample to a plasma etch.

24 Now, the reason it's a plasma etch is
10:16 25 because this is c-plane gallium phase gallium

10:16 1 nitride. That's what's that top surface on these
2 structures, except for the structure in Beach.
3 The c-plane is impervious to wet chemical
4 etching. So there are no known wet chemical etches
10:16 5 to etch that. So we use a plasma etch to etch it.
6 And the plasma edge has, depending on the
7 type of plasma etch -- but the two most common,
8 there's very little undercut that occurs under the
9 mask. And so, I'll schematically illustrate what
10:17 10 these walls generally look like.
11 So the first part of the figure I'll call
12 "A." And then what we do is: We subject this to a
13 plasma etch, and that arrives on the diagram labeled
14 "B."
10:17 15 Do you see the rounded -- that's supposed
16 to be symmetric, but....
17 So you see the rounded shapes that occur.
18 And then what you have to do, if you want
19 vertical walls -- you have to subject this sample to
10:17 20 what's called a "crystallographic etch."
21 The only known crystallographic etches are
22 wet etches.
23 So the next step is: We subject this to
24 our crystallographic etch. And what that does is --
10:18 25 what the term "crystallographic etch" means is that

10:18 1 there is a very strong dependence of etch rate on
2 crystal orientation or different crystal planes.
3 Okay?

4 And so, the slowest etch planes are the
10:18 5 ones that will expose themselves.

6 So if you do this correctly -- the
7 crystallographic etch, by the way, would be --
8 common examples is KOH solutions or TMAH solutions.
9 These are well-known solutions to achieve this. And
10:18 10 so, now we have the same photoresist.

11 The side surfaces are non-c-plane
12 surfaces. Those will etch in a chemical etch. The
13 top surface will not.

14 So we're going to undercut the mask a
10:19 15 little bit. And when you do this process, you will
16 end up with something that looks like this
17 (indicating).

18 And this wall is -- because it's a
19 crystalline plane, is 90 degrees.

10:19 20 And there's still a sloped portion below
21 that that evolves when you do this.

22 But that's what happens.

23 That's how you create a vertical wall in
24 gallium nitride, c-plane gallium nitride.

10:19 25 MR. DOSHI: Okay. So let's mark

10:19 1 this as....

2 A. That's Diagram C after the etch.

3 And you will notice there's still some

4 sloped portions down at the bottom.

10:20 5 When you get near the bottom, it exposes a

6 plane here. And that's what gives these slopes -- a

7 slower edge plane.

8 MR. DOSHI: Okay. Let's mark

9 this as 2002.

10:20 10 We'll put it in 1382.

11 (Whereupon, Exhibit 2002 was marked for

12 identification.)

13 MR. DOSHI: Thank you.

14 BY MR. DOSHI:

10:20 15 Q. And so, this is A, B, and C panels. And

16 the C panel is in red, which is after the

17 crystallographic etch.

18 Is that correct?

19 A. Yes. It recesses in because it undercuts

10:20 20 the resist a little bit.

21 It doesn't recess much, but it exposes

22 that slow etch plane.

23 All the other planes will be removed

24 because they etch quickly.

10:21 25 Q. Okay. You earlier testified that there

10:21 1 are no additional processes that are disclosed by
2 Saxler.
3 A. None of the references disclose what I put
4 in that diagram.

10:21 5 And you'll notice there's additional
6 vertical penetration when you do that
7 crystallographic etch. And that could be quite
8 problematic for a HEMT device, because there's so
9 much going on near the surface.

10:21 10 So it's not surprising that they don't use
11 this step.

12 Q. So since they don't use that step, in your
13 opinion they cannot achieve these 90-degree
14 sidewalls.

10:21 15 Is that correct?

16 A. That is the only way it is known to be
17 done.

18 Q. Okay. So let me ask again.

19 So since Saxler doesn't use the steps that
10:22 20 you've described here in Exhibit 2002, Saxler does
21 not -- or cannot achieve a 90-degree sidewall.
22 Correct?

23 A. That's correct -- or Yoshida, for that
24 matter.

10:22 25 COURT REPORTER: Excuse me.

10:22

10:22

10:23

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What was that term, "Yoshida"?

THE WITNESS: It's the author of another primary reference of prior art.

COURT REPORTER: Would you spell that for me.

THE WITNESS: Y-o-s-h-i-d-a.

COURT REPORTER: Thank you.

BY MR. DOSHI:

Q. So this discussion started with Paragraph 52. And I believe my question that started this was whether Saxler can...discloses -- or provides support for vertical sidewalls of the cap layer.

And we went down this path. And your conclusion is that it does not.

Is that correct?

A. That's what one skilled in the art would know: Without a crystallographic edge, it doesn't exist.

Q. Okay. Let's talk about how we get to the figure that you put together -- or you asked somebody to put together for you --

A. Okay.

Q. -- on Page 41 of your declaration for '347.

10:24 1 Would the precursor to that have a gate
2 contact on top?
3 MS. SPECHT: Objection;
4 foundation.
10:24 5 Q. Okay.
6 A. I don't know what you mean by "precursor"?
7 Q. Okay. So if we were to make the structure
8 that is depicted on Page 41, it would start with the
9 substrate. Correct?
10:25 10 A. Yes.
11 Q. And a channel layer on top of that?
12 A. Yes.
13 Q. And a barrier layer on top of that?
14 A. Yes.
10:25 15 Q. And then a cap layer, probably, extending
16 all the way through, right, across the top of the
17 structure, over the barrier layer?
18 A. It doesn't contact -- it doesn't come in
19 contact with the Ohmic contacts. But....
10:25 20 Q. Not yet.
21 A. Huh?
22 Q. Not yet.
23 I'm trying to go through the fabrication
24 process for this.
10:25 25 A. Oh, okay.

10:25 1 Q. Does that make sense to you?
2 A. The fabrication process?
3 Q. Yes.
4 A. Sure, yeah.
10:25 5 Q. So then what you have in green on Page 41
6 would likely go across. Correct?
7 A. Yes. That layer has to be removed to
8 place the Ohmic contacts.
9 Q. Okay. So once the contacts are in, would
10:25 10 it look a lot like Figure 1B of Saxler?
11 A. No.
12 Q. No?
13 A. No. 1B is a strange cartoon. It's not --
14 let me make sure I'm talking about the right figure.
10:26 15 It's an idealized cartoon.
16 I've never seen a device built that way,
17 where the sides of the Ohmics are able to butt up
18 against the cap layer -- you're not going to be able
19 to fabricate that.
10:26 20 You could fabricate something that is
21 intended to -- you know, this can be like a, I don't
22 know, some sort of a crude design.
23 But there's no way to place Ohmic contacts
24 and butt them up against that cap layer with no gap
10:26 25 in between, as shown.

10:26 1 There's no standard process to do that.

2 Q. Okay. And then once the Ohmic contacts
3 are in, then the gate contact -- how is that formed
4 on top of the cap layer?

10:27 5 A. That can be formed multiple ways, but
6 the....

7 Probably the most straightforward is: You
8 pattern that -- you do this before you place the
9 Ohmics. You can put the Ohmics after -- and they
10:27 10 can go in either order. But to me, it looks
11 straightforward to....

12 The green goes all the way across. Then
13 you etch the -- you plasma etch the green layer.
14 And then you -- one way to do it.

10:27 15 And remember, there's always multiple ways
16 of building these things.

17 So then you...you, with some technique,
18 evaporate or sputter metal on the surface. And you
19 put resist on that and etch the metal away.

10:28 20 And in other embodiments where we bring in
21 other references, we'll use a self-aligned structure
22 to place that gate.

23 But it can be done multiple ways.

24 Q. And so, that would involve masking and
10:28 25 etching steps, I think you said. Right?

10:28 1 A. Yeah. You have to mask the gate.
2 But you can etch the green and the gate
3 metal using the same mask. That would be what we
4 would refer to as a "self-aligned" process.

10:29 5 Q. And where is that? -- in Saxler?
6 A. No. We bring in the self-aligned with
7 other references: Beach and Ahn.
8 Wait -- Ahn's only in one of these cases.
9 I don't want to get confused.

10:29 10 Where is that grounds -- that thing right
11 there.
12 Q. I'll represent Ahn is in '347. So....
13 And that's what we're talking about right
14 now.

10:29 15 A. All right. I'm just going to
16 double-check.
17 Q. Yeah.
18 (Witness reading.)
19 A. And, yes, Ahn -- you're correct.

10:29 20 So Ahn's in this case.
21 Q. Okay. So Saxler does not talk about
22 self-alignment?
23 A. It may be in there, but I don't -- I don't
24 recall it's in there. I don't think it is.

10:30 25 Saxler has other references that -- like

10:30 1 Sheppard, Smith -- that give a lot of details on
2 fabrication, if you're interested.

3 Q. And you discussed those in your
4 declaration. Correct?

10:30 5 A. Correct.

6 Q. Figure 1A has a cap layer that is higher
7 than the Ohmic contact. And in 1B, it shows that
8 it's about the same height.

9 Do you see that?

10:31 10 A. Yes.

11 Q. That's different thicknesses of the cap
12 layer?

13 (No response.)

14 Q. Does that represent different thicknesses
10:31 15 of the cap layer? Sorry.

16 A. To be honest with you, I don't know what
17 1B represents because it's not something you can
18 fab.

19 What it clearly shows is: There's no
10:31 20 recess.

21 Q. And what about Figure 1A; do you think
22 that's a fair representation of what Saxler's trying
23 to achieve?

24 A. Yes. You'll note that the vertical scale
10:32 25 of these diagrams is exaggerated, so you could see

10:32 1 details of the epitaxial layer.
2 But aside from that, yes.
3 Q. Do you expect the gate contact of
4 Figure~1A to be centered, as depicted?
10:32 5 A. There are -- without self-alignment, it's
6 certainly possible to use lithographic techniques to
7 place that in the center, yes.
8 Q. But for 1B, it's not possible to be
9 abutting -- the cap layer abutting on the contact.
10:32 10 Right?
11 A. Yeah. I just don't know how you build
12 something like that.
13 MR. DOSHI: All right. Good
14 time for a break?
10:33 15 THE WITNESS: Okay.
16 MR. DOSHI: Off the record.
17 (Whereupon, a recess was taken
18 from 10:33 a.m. until 10:47 a.m.)
19 BY MR. DOSHI:
10:47 20 Q. We are still talking about Saxler. I want
21 to take you to Figure 1A.
22 Are you there?
23 A. Figure 1A?
24 Q. Yeah.
10:47 25 A. Yeah. We were on Page 41, I guess?

10:47 1 Q. Well, I'm going to take you to Saxler,
2 actually.
3 A. Oh, okay.
4 Q. Figure 1A.
10:47 5 A. All right.
6 (Pause.)
7 A. Okay.
8 Q. Okay. And in your opinion, is that an
9 enhancement mode transistor?
10:48 10 A. Figure 1A?
11 Q. Yeah -- let's back up.
12 You opine on enhancement mode and
13 depletion. Right?
14 A. Yes.
10:48 15 Q. Okay. And you know what "enhancement
16 mode" means. Correct?
17 A. Yes, I do.
18 Q. What is an enhancement mode transistor? --
19 generally speaking.
10:48 20 A. Generally speaking, when there's 0 volts
21 applied to the gate, it....
22 The device is in an off state, and you
23 have to apply a positive bias to the gate to turn
24 the device on.
10:49 25 And that's generally what people would

10:49 1 call "enhancement mode" -- although, it has other
2 meanings as well.
3 But in the context of this, I think that's
4 a good representation.

10:49 5 Q. Okay. In your opinion, is Figure 1A an
6 enhancement mode transistor?

7 A. As it's drawn, it would be a depletion
8 mode device unless the gate contact penetrated deep
9 into the barrier layer, which -- that's not the way
10:49 10 it's shown.

11 Q. And I think you state that in
12 Paragraph 146 of your declaration, which I believe
13 is on Page -- it is on Page 75.

14 A. Yes. On the fourth line from the bottom,
10:50 15 yeah.

16 Q. Great. And then if we turn back to
17 Saxler, Figure 1B.

18 Now, before the break, we were talking
19 about how the cap layer -- that this is -- let me
10:50 20 rephrase.

21 Before the break, you testified that
22 Figure 1B may not have a cap layer that abuts the
23 Ohmic contact.

24 Is that a fair representation?

10:50 25 A. I think what I said was: It would not be

10:50 1 straightforward at all to fabricate such a
2 structure.

3 Q. Okay. Is it possible to etch the cap
4 layer, deposit a metal over the cap layer and into
10:51 5 the vias, if you will, next to the cap layer?

6 A. Wait a minute. Are we talking 1B? Or....

7 Q. Yeah, I'm talking 1B.
8 I'm just -- I'm trying to understand.
9 You said that there aren't any mechanisms
10:51 10 by which -- processes by which you can form 1B.
11 Is that right?

12 A. Yes. It's basically because the Ohmic
13 contacts button and are perfectly aligned and butt
14 up against the cap layer. That's the way it's
10:51 15 drawn.

16 Q. Okay.

17 A. And they're also the same thickness --
18 which would rarely be the case.

19 Q. So if we go to 72, though -- Paragraph 72
10:52 20 of Saxler.

21 A. Oh, Saxler.

22 Q. Yeah.

23 A. Okay.

24 Q. At the fourth from the bottom, it says:
10:52 25 In such a case....

10:52 1 Do you see that?

2 A. Yes.

3 Q. It says:

4 A dope region would not
10:52 5 extend to the Ohmics contacts,
6 which may be isolated from the
7 dope region by an insulating
8 region such as a silicon
9 nitride layer or gap.

10:52 10 Do you see that?

11 A. Yes.

12 Q. Does that imply that there are instances
13 where the dope region would contact the Ohmic
14 contacts?

10:52 15 MS. SPECHT: Objection; form.

16 A. I would say no. It will do the device no
17 good to do that. It'll only potentially introduce
18 some shunt conductance to the 2D gas, a very bad
19 thing. So I don't think so.

10:53 20 You'd have a gap.

21 Q. So 72 says:

22 Further, in certain
23 embodiments of the present
24 invention....

10:53 25 Right?

10:53 1 And then, it continues that:
2 ...the doped region would
3 not extend to the Ohmic
4 contacts.

10:53 5 Are there instances -- are there
6 embodiments contemplated by Saxler where the cap
7 layer extends from Ohmic contact to Ohmic contact
8 without the doped layer -- Dope Region 40?

9 MS. SPECHT: Objection; form.

10:53 10 A. So your question was -- would you just
11 repeat the question, please.

12 Q. Sure. Does Saxler contemplate a cap layer
13 that contacts both Ohmic contacts?

14 A. That's certainly what's shown in 1B.

10:54 15 But, remember, Saxler has a lot of
16 different structures for cap layers and some of them
17 are insulating.

18 So if the cap layer's insulating, it would
19 function.

10:54 20 Q. Okay.

21 A. If it's conducting, it would be a
22 disaster.

23 Q. Why would it be a disaster?

24 A. Because when you apply a gate potential,
10:54 25 you're trying to modify the two-dimensional electron

10:54 1 gas. And you want all of the conduction, all the
2 drain current in the device, to come from the
3 two-dimensional electron gas, because that's what's
4 gated.

10:54 5 If you have a conducting cap layer in 1B,
6 there would always be current flowing from source
7 to -- or electron flow or current from drain to
8 source that would be going through the cap layer
9 that wouldn't be affected, necessarily, by the gate
10:55 10 bias.

11 So you never want a parallel conduction
12 path to the two-dimensional electron gas.

13 Q. And so, going back to 1B, is that in
14 your -- well, is Figure 1B an enhancement mode
10:56 15 transistor?

16 A. If the cap layer were p-doped at the
17 correct amount and the thickness was correct, it
18 could be an enhancement mode device.

19 Q. When you say "thickness is" -- I think you
10:56 20 said "correct" -- what do you mean by that?

21 "Thickness," meaning the height or the
22 width?

23 A. The height.

24 Q. Okay. Does Saxler say "enhancement mode"?
10:57 25 I think you said it does not. Right?

10:57 1 COURT REPORTER: Did you say --
2 what?

3 MR. DOSHI: Sorry.

4 COURT REPORTER: I'm sorry.

10:57 5 Q. Does Saxler say that -- does Saxler use
6 the term "enhancement mode"?

7 A. My recollection is it doesn't, but I'll be
8 happy to look for it.

9 Q. No. I think -- Paragraph 99 on Page 53 of
10:57 10 your declaration, I believe you say -- well, you do
11 say:

12 Although Saxler does not
13 use the phrase "enhancement
14 mode," this transistor indeed
10:57 15 constitutes a normally off
16 enhancement mode gallium
17 nitride transistor when these
18 p-type dopants are placed in
19 the cap layer.

10:57 20 Do you see that?

21 A. You're on Page 53?

22 Q. Yes; Paragraph 99.

23 A. Okay. Well, that's....

24 If you remove the recess and add p-doping
10:58 25 to the cap layer, you can turn -- you can easily

10:58 1 turn Saxler's device into an enhancement mode
2 device.

3 That p-cap layer is what -- that's the
4 primary difference between a depletion and
10:58 5 enhancement mode device.

6 So they're very compatible with each other
7 because they only differ by, you know, that one
8 feature to go from a depletion mode to an
9 enhancement mode.

10:58 10 So, you know, one skilled in the art would
11 be familiar with both.

12 Q. In your opinion, would that be -- would
13 Figure 1B be a reasonably well working enhancement
14 mode transistor?

10:59 15 A. I think you'd want to separate the Ohmics
16 from the cap layer, because that structure, as
17 shown, would have these shunt problems I was talking
18 about, potentially.

19 Q. And the 2DEG -- where is the 2DEG depleted
10:59 20 in Figure 1B?

21 A. I think it'd be useful to make another
22 drawing.

23 Q. Okay.

24 A. I think if I -- if I do the drawing for
11:00 25 1A, it will encompass everything in both figures.

11:00 1 Q. I'm specifically asking about 1B, because
2 you said that it could be in enhancement mode.
3 I'm trying to understand --
4 A. Well, so can 1A if you remove the recess
11:00 5 and p-dope the cap.
6 So --
7 Q. Right.
8 A. -- what I was going to do is do it for the
9 modified structure, because....
11:00 10 Q. No -- yeah, but I'm more interested in 1B,
11 because -- I understand your position in
12 Paragraph 146 --
13 A. Okay.
14 Q. -- regarding 1A.
11:00 15 But I'm talking about 1B and how that
16 would function as an enhancement mode transistor.
17 A. Okay. All I'm doing in Diagram A is
18 trying to reproduce Figure 1B.
19 Okay. So I'm going to indicate the
11:01 20 boundaries between the Ohmics -- and I forgot to put
21 the gate on.
22 And so, you could now think about
23 producing a profile of the electron gas, which is
24 getting at the heart of your question, across a
11:02 25 device from source to drain.

11:02 1 So I'll call this the "source" over here,
2 and "gate," and the "drain."

3 Okay. So the 2D gas is, more or less, the
4 same under the Ohmic contact. So you have a 2D gas
11:02 5 here and here (indicating).

6 So no matter what biases you apply, you're
7 always going to have a 2D gas in those regions.

8 Q. So just for the record, "2DEG," right, is
9 what you're referring to?

11:02 10 A. 2-Dimensional Electron Gas -- "2DEG."

11 I don't like that term, but that's all
12 right.

13 And then -- so this is when the device is
14 in the off state. Okay?

11:03 15 And so, the negative charge associated
16 with that p-type layer, that comes from the acceptor
17 impurities you dope it with.

18 That negative charge -- and so, we're not
19 applying any gate bias -- that negative charge is
11:03 20 sufficient in density to deplete all of the 2D --
21 the "2DEG," if you like -- out of the channel.

22 So the...it would look something like this
23 (indicating).

24 And so, this is a -- I'll call it the
11:03 25 sheet concentration of the 2D electron gas as a

11:04 1 function of position.
2 This is for -- it's in the off state and
3 low drain bias, just because it's easier to draw
4 that way. Okay?

11:04 5 And then you apply a....
6 And by the way, it doesn't matter if
7 there's gaps between the source and the gate. It's
8 just -- it's just not something that matters.
9 So in other words, you can have gaps in
11:04 10 this channel, and the 2D gas will still be induced
11 when it's in the on state.
12 So now on Diagram C, we'll draw in the on
13 state. Nothing's changed about the Ohmic contacts
14 and the 2D gas concentration under them.

11:05 15 So this is meant to be the same. The 2D
16 gas hasn't changed under the Ohmics.
17 Now, if you forward biases to turn this
18 on, you can actually and you will actually increase
19 the 2D gas concentration -- it depends on how hard
11:05 20 you turn it on -- over what's under the Ohmic
21 contacts.
22 So at low drain bias, it would actually
23 look like this when it's on.
24 And that same figure would apply to 1A.
11:05 25 But you have to modify it because there's sloped

11:05 1 sidewall shown.

2 So the acceptor densities -- the sheet

3 density, which is a product of the volume density

4 times the thickness, it changes as you move through.

11:05 5 So there's a more gradual transition in

6 1A, but it basically looks the same.

7 MR. DOSHI: Okay. Let's mark

8 this drawing as Exhibit 2003 for 1382 --

9 2003.

11:06 10 COURT REPORTER: Should I put

11 "1382" on there for you?

12 No? Okay.

13 MS. SPECHT: You can use the

14 same exhibit in both proceedings if you

11:06 15 want. So just leave it.

16 (Whereupon, Exhibit 2003 was marked for

17 identification.)

18 BY MR. DOSHI:

19 Q. Okay. In your explanation, you said it

11:06 20 depends on how hard you turn it on.

21 What did you mean by that?

22 A. Okay. There's something called a

23 "threshold voltage." That's the onset of

24 conduction.

11:06 25 Q. Um-hum.

11:06 1 A. And as you increase the gate voltage above
2 the threshold voltage, you're inducing more and more
3 2D gas under that gate region.

4 Q. Okay. And earlier you had indicated that
11:07 5 the thickness may need to be reduced for 1B and for
6 the -- for it to operate as enhancement mode?

7 A. I can't say anything about that. There's
8 no dimensions on here.

9 But I'm just saying, you have to have the
11:07 10 right sheet density of negative charge to fully
11 deplete the 2D gas out of the channel if you want it
12 to be normally off.

13 Q. Okay. And a gate, as depicted in
14 Figure~1B, would that require additional voltage for
11:07 15 it to be turned on as an enhancement mode?

16 A. Well, you'll design the enhancement mode
17 device by placing the proper amount of negative
18 charge -- negative sheet charge is what counts -- to
19 deplete the 2D gas.

11:07 20 So the...that will produce a threshold
21 greater than zero if it's in enhancement mode.

22 So the further you drive it beyond
23 0 volts -- say you drive it at 1 volt -- in fact, we
24 could add another feature to that diagram, if you
11:08 25 want, to illustrate that.

11:08 1 Q. Okay. Can we put that in red?
2 A. Yeah.
3 Q. So you're going to take back 2003 --
4 I'm just stating this for the --
11:08 5 A. No, I gotcha.
6 Q. -- for the record.
7 I'm going to hand you back 2003, and
8 you're going to add red.
9 A. Yeah, we'll put it in red.
11:08 10 So...say this is a gate voltage. That's
11 approximately equal or greater than the threshold
12 voltage.
13 And then in blue -- which I seem to have
14 lost -- oh, there it is -- the threshold -- the gate
11:09 15 voltage is considerably larger than that. So, I
16 don't know, say it's approximately the threshold
17 voltage plus a couple of volts.
18 There is a limit to how hard you can drive
19 the gate. And so, 2 volts would be driving it
11:09 20 pretty hard if the threshold was near zero.
21 So it might look something like that.
22 And by the way, this is -- both -- all of
23 these are for low drain bias, these diagrams.
24 Q. Okay. Thank you.
11:09 25 A. Um-hum.

11:09 1 Q. Let's go back to Paragraph 72 of the
2 Saxler reference -- you have so many paragraphs, you
3 don't know which one to reach for.

4 And specifically right in the middle of
11:11 5 the paragraph, it talks about a "JHEMT."

6 A. Yes.

7 Q. Are you familiar with "JHEMTs," Junction
8 HEMTs?

9 A. Of course.

11:11 10 Q. Okay. Is that in enhancement mode?

11 A. No.

12 Q. Okay.

13 A. That's not to say they can't be.

14 But the way it's described here, it would
11:11 15 be in depletion mode -- and it's a bad idea.

16 Q. Let's go to Paragraph 63 of Saxler.

17 Okay. And this -- Paragraph 63, this acts
18 as the cap layer. Correct?

19 A. Yes.

11:13 20 Q. And the formation of the cap layer.
21 Right?

22 A. The Paragraph 63?

23 Q. Yes.

24 A. Yeah, it's suggesting you use epitaxial
11:13 25 growth techniques to produce it.

11:13 1 Q. And we talked about that earlier.
2 It's basically putting down that cap layer
3 in green and you modify it -- bigger, Saxler.
4 Right?

11:13 5 A. Yes. There's no lithographic processing
6 that occurs yet. So it's a planar film.

7 Q. So in 64, we're talking about KOH and
8 etching.

9 And is -- in 2002 -- in Exhibit 2002,
11:14 10 which is the drawing that you made, you -- I
11 think -- oh, you have -- I think you have before you
12 2002, the drawing -- the first drawing that you
13 made.

14 Do you have it?

11:14 15 A. Where is it?
16 I thought I gave it up, but -- oh, it's
17 over here.

18 MS. SPECHT: There it is.

19 Q. I apologize. Here it is.

11:14 20 A. Okay.

21 Q. I see "KOH" in your notations there.
22 So --

23 A. Yes.

24 Q. -- is that the same KOH etching materials?

11:14 25 A. As soon as you add -- that's KOH with UV

11:15 1 stimulation of the etch. And that's not how
2 crystallographic etches are done, usually. So it's
3 kind of a different animal.

4 If they -- you could have KOH solutions
11:15 5 that don't effectively crystallographic etch. If
6 it's a crystallographic etch, it'll say it.

7 Q. And do you understand Paragraph 64 to be
8 etching the cap layer to drop in the Ohmic contacts?

9 A. Well, they said this etch is done to
11:16 10 expose the underlying barrier layer.

11 And that's where the contacts are placed,
12 either directly on the barrier -- or, if you look at
13 Figure 1A, they're actually recessed into the
14 barrier.

11:16 15 Generally, you get better Ohmic contacts
16 if you recess them into the barrier.

17 In fact -- well, I won't go into any more
18 detail on that.

19 MR. DOSHI: I'm handing you
11:18 20 what's been previously marked as
21 Exhibit 1006, which is Yoshida.

22 (Whereupon, Exhibit 1006, previously
23 marked, was presented to the witness.)

24 BY MR. DOSHI:

11:18 25 Q. Have you seen this document before?

11:18 1 A. Yes.
2 Q. Okay.
3 A. It's in the binder here.
4 Q. Okay. If you want to use your binder
11:18 5 copy, that's fine, so long as there are no notes on
6 it.
7 A. Okay.
8 Q. We've been talking about Saxler
9 enhancement mode.
11:18 10 Is Yoshida an enhancement mode transistor?
11 A. Yes. There's support for that in here.
12 Q. And Yoshida has a gate structure. Right?
13 A. Yes.
14 Q. Yeah. And do you agree that Yoshida
11:19 15 deposits and etches the gate material first, before
16 the gate contact?
17 MS. SPECHT: Objection; form.
18 A. I don't recall. So I'd like to look.
19 Q. Sure.
11:19 20 A. It can certainly be done either way,
21 but....
22 (Witness reading.)
23 A. Okay. I'm ready to answer the question,
24 but I forgot the exact language. I don't know if
11:22 25 you could repeat the question.

11:22 1 Q. Yoshida has a fairly clear process,
2 correct? -- in terms of creating a structure?
3 MS. SPECHT: Objection; form.
4 A. He has several paragraphs describing
11:22 5 fabrication.
6 And in the conventional art, he describes
7 one scenario.
8 The source electrode and
9 drain electrode are loaded --
11:23 10 as a further example, a gate
11 electrode is loaded via a
12 p-type layer.
13 I'm not sure that implies the order of
14 process for that particular paragraph.
11:23 15 And then there's paragraph -- so that was
16 Paragraph 2. Paragraph 6, it says:
17 After performing
18 conventional photolithography
19 and etching of the n-type AlGaIn
11:23 20 layer, a gate electrode,
21 source, and drain electrode are
22 loaded on.
23 That's certainly....
24 And that particular paragraph doesn't
11:23 25 imply any order of processing. One skilled in the

11:23 1 art would read that as you could do it either way.
2 And then there's another -- if I can find
3 it -- discussion of the fabrication, which appears
4 in Paragraph 23.

11:24 5 In 23 it would seem to suggest source and
6 drain contacts come in first, I think. It's not
7 like -- do you see what it says?

8 Lastly, etching away and
9 masking the opening of the SiO₂
11:24 10 film beneath it, the source and
11 drain electrodes were masked
12 with the SiO₂ film.

13 And then later, the gate electrodes were
14 loaded.

11:25 15 So that suggests the gate came after the
16 source and drain.

17 Does that answer your question?

18 But the other disclosures seem to imply
19 you could do it in any order.

11:25 20 Q. And the others -- you're talking about
21 paragraphs 2 and 6. Correct?

22 A. Well, 2 is conventional art. So maybe we
23 shouldn't....

24 But 6 -- there's one sentence that says
11:25 25 you do all this stuff. It doesn't tell you -- it

11:25 1 seems to suggest any order will work.

2 Q. Is 6 under the heading of "Conventional

3 Art"?

4 A. It may be -- well, I don't....

11:25 5 Q. Because I'm looking at Paragraph 8 at the

6 bottom there. It says:

7 Problems the invention

8 seeks to solve.

9 A. Okay.

11:26 10 (Witness reading.)

11 A. Okay. Well, anyway, the -- Paragraph 23

12 seems to suggest that the gate came....

13 (Witness reading.)

14 A. Even in 23, it's not clear what the order

11:26 15 of the process is, because it almost suggests that

16 what they're doing is: They said they've got an

17 SiO₂ film, which is an insulator over the whole

18 thing. And then they mask it and open up holes in

19 that film.

11:26 20 And then the source, drain electrodes were

21 masked....

22 (Witness reading.)

23 A. Okay. It says:

24 The source, drain --

11:27 25 source and -- source electrode,

11:27 1 drain electrode --
2 They call that "G." I don't know why. I
3 think that's a typo.
4 -- are masked with the
11:27 5 film and gold was deposited....
6 Somewhere along the line, they got to
7 expose the Ohmic contacts.
8 And so, the entire process isn't here.
9 So the gate's formed. It seems to suggest
11:28 10 the Ohmic contacts are covered up with SiO2.
11 So the Ohmic contacts really aren't
12 completed until you expose the metal so that you can
13 operate the device.
14 So that, by itself....
11:28 15 You know -- you get my point?
16 The source-drain contact process wasn't
17 finished until after the gate. It was started
18 before the gate. So you call that "gate first, gate
19 last"? How about "first or last"?
11:28 20 Q. Okay. Could we go to Paragraph 19.
21 A. Yeah.
22 Q. Okay. So Paragraph 19 -- and actually,
23 through 21 -- it talks about...talks about the
24 process. Correct?
11:29 25 A. That's all talking about the epitaxial

11:29 1 part of the process.

2 Q. Got it.

3 And then Paragraph 22, what is it

4 referring to there?

11:29 5 A. You're dry etching to etch away the p-type

6 GaN, except where the gate -- except where the gate

7 electrode was to be loaded, exposing the n-type.

8 (Witness reading.)

9 A. So....

11:29 10 (Witness reading.)

11 A. Okay. They clearly start the Ohmic

12 process before the gate.

13 But the -- lastly, Paragraph 23, they

14 don't seem to finish the Ohmic process till after

11:30 15 the gate.

16 So I guess you could call it either way.

17 Q. What significance does that last -- in the

18 last two sentences -- I mean, that last sentence

19 say?

11:31 20 And I'm in Paragraph 22 --

21 A. Okay.

22 Q. -- second-to-the-last line.

23 And it starts with:

24 ...and metal Al deposited

11:31 25 on the exposed n-type --

11:31 1 A. Wait a minute. Which -- I thought you
2 said "22"?

3 Q. "22," yeah -- second-to-last line.

4 A. Okay.

11:31 5 Q. And --

6 A. Okay. I see it now.

7 Q. Is that metal aluminum?

8 A. Yes.

9 Q. And so, that's deposited on the exposed
11:31 10 n-type indium gallium nitride layer 4?

11 A. Yes.

12 So that's the Ohmic metal.

13 Q. That's the....

14 A. It's not a usual Ohmic metal, but on
11:31 15 n-GaN, it'll work.

16 Q. So 4 is aluminum. Okay.

17 And then it says, in 23:

18 Lastly, after etching away
19 the masking and opening the
11:32 20 silicon dioxide film beneath
21 it, the source electrode and
22 drain electrode locations were
23 masked with silicon dioxide
24 film.

11:32 25 Do you see that?

11:32 1 A. Yes.

2 Q. And then it says:

3 Au --

4 Gold?

11:32 5 A. Yes.

6 Q. (Continued reading:)

7 -- was deposited in the

8 opening portions, and gate

9 electrodes G were loaded above

11:32 10 the p-type GaN layer 5 to

11 fabricate the HEMT shown in

12 Figure 1.

13 Do you see that?

14 A. Yes.

11:32 15 Q. Okay. And, if we turn to --

16 A. But that's -- Figure 1 doesn't appear like

17 what's described in 23, because the SiO2 isn't shown

18 there. And it obviously was removed to get to that

19 figure.

11:33 20 So one could conclude that the Ohmic

21 contact process wasn't finished until the SiO2 was

22 removed, which is not shown here.

23 I mean, it certainly started before the

24 gate was deposited.

11:33 25 I'm just pointing that out. That's all.

11:34 1 Q. Okay. Let's go to Paragraph 17. And that
2 talks a little bit about the gate material.

3 Do you agree?

4 A. Yes.

11:34 5 Q. Okay. So here it says:

6 The operation of the p-n
7 junction immediately under the
8 gate electrode G enables
9 voltage control....

11:34 10 Do you see that?

11 A. Yes.

12 Q. Okay. And so, that is describing the
13 operation of Figure 1?

14 A. The operation of what?

11:34 15 Q. "Figure 1."

16 A. Yes.

17 Q. Okay. So for Yoshida to be turned on, you
18 would need to apply a positive voltage to the gate.

19 Is that correct?

11:36 20 A. Yeah.

21 There's additional support for that in
22 Paragraph 23.

23 Q. Okay. I'm there.

24 A. They apply a gate voltage of 3 volts, and

11:36 25 that's -- the device is turned on, and it exhibits a

11:36

1 drain saturation voltage -- meaning, it's acting
2 like an enhancement mode transistor.

3 That's really the purpose of the p-type
4 region under the gate.

11:36

5 MR. DOSHI: All right. Let's go
6 off the record.

7 (Whereupon, the deposition recessed for
8 lunch at 11:36 a.m.)

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A F T E R N O O N S E S S I O N

(12:28 p.m.)

BY MR. DOSHI:

Q. Welcome back, Dr. Shealy.

A. Thank you.

Q. We went to -- can we go to -- this is Exhibit 1003, your declaration. And go to Exhibit 1020 -- I mean, I'm sorry -- Paragraph --

A. This is the '347 still?

Q. Yes -- yeah.

It's Page 53. It's Paragraph 100.

At the bottom there, you cite Sheppard.

And this is in relation to the enhancement mode issue.

And does Sheppard use the term "enhancement mode"?

A. I don't recall.

Q. Okay.

A. It's been a while since I've read Sheppard.

MR. DOSHI: Okay.

All right. I'm handing you what's been previously marked as Exhibit 1021.

(Whereupon, Exhibit 1021, previously

12:30 1 marked, was presented to the witness.)
2 BY MR. DOSHI:
3 Q. And do you recognize this document?
4 A. Yes. This is Sheppard.
12:31 5 Q. And if you look at....
6 On Page 53, you cite to Figure 1F.
7 And 1F seems --
8 A. Yes.
9 Q. -- to look a lot like Saxler's 1A.
12:31 10 Do you agree?
11 (Pause.)
12 A. It seems to be nearly identical.
13 Q. Okay.
14 (Pause.)
12:33 15 Q. Thanks for bearing with me. I lost my
16 place here.
17 All right. Let's switch topics a little
18 bit.
19 Paragraph 95 of '347, which is on Page 50,
12:34 20 you have -- you refer to Beach. Correct?
21 A. Correct.
22 MR. DOSHI: Okay.
23 (Whereupon, Exhibit 1008, previously
24 marked, was presented to the witness.)
12:34 25 Q. I'm handing you what's been previously

12:34 1 marked as 1008.

2 A. Okay. Thank you.

3 Q. All right. And that's Beach -- yes?

4 A. Yes, it is.

12:35 5 Q. Okay. And in 95, you rely on Beach for an
6 alleged self-aligned etching technique.

7 Is that right?

8 A. That's correct.

9 Q. And in Paragraph 96 on Page 51 of your
12:35 10 declaration, Beach does not disclose horizontal
11 ledges. Right?

12 A. That's correct.

13 Q. Okay. And Beach Figure 1 doesn't disclose
14 side surfaces that extend horizontally. Right?

12:36 15 A. What Beach figure shows is a -- you know,
16 it's drawn as a vertical wall. It's an idealized
17 drawing, of course.

18 Well, one would expect it to have some
19 curvature.

12:37 20 Q. And that is -- I think you use the word
21 "machine tolerance" in your declaration.

22 Is that right?

23 A. You might want to point me to that. I
24 don't remember using that term.

12:37 25 Q. Okay. "Manufacturing tolerances," maybe?

12:37 1 A. That I remember, yeah.

2 Q. Okay. And is that why you would -- are

3 the manufacturing tolerances why you would -- why

4 you -- it's your opinion that a person of ordinary

12:38 5 skill in the art would have understood Beach to have

6 some slope to its sidewalls?

7 MS. SPECHT: Objection; vague.

8 A. Beach is used for the self-aligned

9 process. And the shape of the wall is not really

12:38 10 relevant to the way it's used in the combination.

11 Q. Okay. I'm going to switch to your other

12 declaration. So this is '355.

13 This is for 1482 -- 1382 -- 1884.

14 I'm sorry. Third time's a charm.

12:41 15 Okay. And I'm on Page 34.

16 And there you have petitioner's claim

17 construction. Do you see that, up at the top of --

18 A. Yes.

19 Q. -- Page 34?

12:42 20 And you use that for your analysis?

21 Well, let me rephrase that.

22 You use that in your analysis, that claim

23 construction.

24 Is that right?

12:42 25 A. Yes. But I -- we considered both

12:42 1 constructions. And the patents are invalid under
2 both construction.

3 Q. Okay. And this relates to the
4 substantially -- this relates to side surfaces
12:42 5 extending.

6 Is that right?

7 A. Yes.

8 Q. Okay. And here you say that:

9 The bottom of the p-type
12:42 10 gate material is more than 10%
11 wider than the top of the
12 material.

13 Right?

14 A. That's what -- yes, that's what's there.

12:42 15 Q. Okay. And is -- in your opinion, is 10%
16 within manufacturing tolerance?

17 A. I think you need to explain that a little
18 better.

19 Q. Okay. So you used the term "manufacturing
12:43 20 tolerance" in your declaration. Right?

21 A. "Manufacturing" and "alignment accuracy"
22 or something along those lines.

23 Q. Okay. And I'm just trying to understand
24 how much of a variation would that be, in your
12:43 25 opinion, in terms of --

12:43 1 A. 10 percent?

2 Q. Yeah.

3 A. Well, I still don't know the context of

4 the question. I'm not quite sure what you're asking

12:43 5 me to --

6 Q. Okay. Let's go back to Exhibit 2002,

7 which I'm handing you back.

8 A. Okay.

9 Q. And in Panel B, you said that there would

12:44 10 be some sloping of the sidewalls. Correct?

11 A. Yes.

12 Q. All right. And you said that's a function

13 of the etching process. Right?

14 A. Yes.

12:44 15 Q. Okay. How much of a tolerance is there

16 for the chemicals or the etching processes that are

17 taking place in Saxler, for example?

18 MS. SPECHT: Objection; form.

19 A. The trouble I'm having is the use of the

12:44 20 word "tolerance."

21 I mean, how -- to what extent can these

22 sidewalls extend? -- is that...?

23 That depends entirely. That can be --

24 vary quite a bit by the etching process.

12:45 25 Okay. You never get, you know, near

12:45 1 vertical. There's always some slope.
2 But it can be exaggerated, depending on
3 how you tune the etching process.
4 Q. All right. If you're trying to etch
12:47 5 vertical sidewalls, how much wider would you expect
6 the bottom of the material to be than the top, based
7 on the manufacturing tolerances that you describe in
8 your declaration?
9 A. I guess the tolerance to me means the
12:47 10 variation from one -- you know, if you do it 100
11 times, how tight is the distribution?
12 Q. I see.
13 A. Is that...?
14 Q. Okay. So Paragraph 91 -- no, page 91 --
12:47 15 of '335, the same one.
16 A. Okay.
17 (Pause.)
18 Q. You know what, Dr. Shealy -- I'm sorry --
19 forget that.
12:48 20 A. Okay.
21 MR. DOSHI: We can go off the
22 record.
23 (Whereupon, a recess was taken
24 from 12:48 p.m. until 12:50 p.m.)
12:48 25 (Whereupon, Exhibit 1009, previously

12:48 1 marked, was presented to the witness.)
2 BY MR. DOSHI:
3 Q. I'm handing you what's been previously
4 marked as Exhibit 1009.
12:50 5 And that is Shenoy, right?
6 A. Yes.
7 Q. Okay. So do you understand Shenoy to be a
8 hypothetical model?
9 A. Shenoy has a model in it. And the Board
12:51 10 had a few comments on Shenoy, which I'd like to
11 address.
12 Can I do that now?
13 Q. We can get there.
14 A. Okay.
12:51 15 Q. And then, Shenoy teaches an isotropic
16 etching process. Right?
17 A. Yes.
18 Q. What is "isotropic," in your -- in your
19 opinion?
12:51 20 A. It means the material you're etching
21 etches at the same rate in all directions.
22 Q. Okay. And what are the materials that
23 are...what are the materials that are employed by
24 Shenoy -- or that are being etched in Shenoy?
12:51 25 A. It's a metal film.

12:52 1 Q. Um-hum. And it's etching to two films, or
2 one?

3 A. Just one.

4 Q. Okay. And there's an insulator at the
12:52 5 bottom. Correct?

6 A. Correct.

7 Q. Okay. Does that spread the etching in the
8 horizontal way?

9 A. If the....

12:52 10 Whatever -- it does in this case.

11 But whatever is under it, if it doesn't
12 etch, it will enhance the sideways etching -- or the
13 "undercut," if you like.

14 Q. "Undercut" meaning under the photoresist?

12:52 15 A. Yes. It's shown by "U" in this diagram,
16 Figure 1.

17 Q. Okay. So....

18 (Pause.)

19 MR. DOSHI: I'm handing you what
12:53 20 has been previously marked as
21 Exhibit 1020.

22 (Whereupon, Exhibit 1020, previously
23 marked, was presented to the witness.)

24 BY MR. DOSHI:

12:55 25 Q. And do you recognize the document?

12:55 1 A. Yes.

2 Q. And what is it?

3 A. Excuse me?

4 Q. What do you recognize it to be?

12:55 5 A. The Uemoto reference, which is referenced

6 in the declaration.

7 Q. Okay. And turning to Figure 5, which I

8 believe you referenced in your declaration -- do you

9 see that?

12:55 10 A. Yes.

11 Q. Okay. And Page 101 of the '335

12 declaration, I think you blow that image up a bit?

13 A. Yes.

14 Q. And does Uemoto show substantially equal

12:56 15 widths?

16 A. Could you explain which widths on the

17 diagram you're talking about.

18 Q. Sure. The ledges, basically.

19 A. Below the brighter metal?

12:56 20 Q. Correct, yeah.

21 A. I would not call those "substantially

22 equal ledges," no.

23 Q. Okay. Let's go back to Beach.

24 Sorry -- I'm jumping around a little bit.

12:57 25 I asked you previously whether you rely on

12:57 1 this -- or I think you testified that this -- you
2 relied on this for the self-alignment piece.
3 Is that right?
4 A. Yes.

12:57 5 Q. Okay. And when we say "self" -- when you
6 say "self-alignment," are you referring to -- and
7 I'm looking at Figure 1, which you rely on in your
8 declaration.
9 Is that right?

12:57 10 A. Yes.

11 Q. And 26 and 24 are etched at the same time.
12 Right?
13 A. Yes.

14 Q. Okay. And that presupposes that 26 and 24
12:58 15 have been formed before the etching process. Right?
16 A. Yes.

17 Q. Okay. And 24 is the gate electrode?
18 A. Let's double-check that.
19 (Witness reading.)

12:58 20 A. 24 is the gate metal.
21 Q. Which serves as the electrode?
22 A. Yes.

23 MR. DOSHI: Let's take ten
24 minutes. I might be wrapping up.
12:59 25 Off the record.

12:59 1 (Whereupon, a recess was taken
2 from 12:59 p.m. until 1:11 p.m.)
3 MR. DOSHI: I'll pass the
4 witness.
01:11 5 MS. SPECHT: Then we're going to
6 take one more break.
7 MR. DOSHI: Say it again?
8 MS. SPECHT: Ten minutes.
9 MR. DOSHI: Oh, okay.
01:25 10 (Whereupon, a recess was taken
11 from 1:11 p.m. until 1:25 p.m.)
12 MS. SPECHT: Ready?
13 MR. DOSHI: Yep.
14 MS. SPECHT: All right.
01:25 15 EXAMINATION
16 BY MS. SPECHT:
17 Q. Okay, Dr. Shealy. Do you recall, just a
18 moment ago, counsel for EPC asking you about the
19 Shenoy reference, which is Exhibit 1020?
01:26 20 A. 1009.
21 Q. Exhibit 1009, yes.
22 A. Yes, I do recall.
23 Q. And you mentioned during your testimony --
24 you actually asked permission during your testimony
01:26 25 to explain the model in Shenoy.

01:26 1 Do you remember asking that?

2 A. Yes.

3 Q. And since you were denied your request to
4 explain Shenoy's model, can you explain Shenoy's
01:26 5 model now?

6 A. Yes. Shenoy describes isotropic etching
7 through a photoresist window.

8 So a POSITA would know that isotropic
9 etching can be done a variety of ways, and one way
01:27 10 is the example given in Shenoy: EMM.

11 There's other techniques of isotropic
12 etching which involve using liquid metal etches that
13 are especially formulated for specific metals.

14 And they've been around a very long time,
01:27 15 common metals that would be used in a process like
16 this -- nickel, aluminum, tungsten. There's a long
17 list of solutions that have been developed for this
18 purpose.

19 And these solutions, unlike the technique
01:27 20 used in Shenoy, do not require an external applied
21 potential.

22 So in any case, Shenoy's model also
23 possesses symmetry. And that same symmetry is
24 present in the Yoshida and Saxler reference.

01:28 25 So the Board was interested in symmetry

01:28 1 because it was listed under "Assumptions."
2 And the -- if you're -- because symmetry
3 is present in the structure, symmetry is a valid
4 assumption. It doesn't need to be assumed, but it
01:28 5 cuts down the number of computations to complete the
6 model.
7 So symmetry is built in by the structure
8 that's being modeled. Okay? And it mirrors the
9 symmetry of, as I said, Yoshida and Saxler.
01:29 10 The other point about Shenoy is: The
11 metal film that's being etched is under the
12 insulator -- or is over the insulator. The
13 insulator's under the metal.
14 When we make this combination and -- of
01:29 15 Yoshida, Saxler, or vice versa, with Beach --
16 Beach is used for the self-alignment.
17 Shenoy is used for the undercut.
18 So when we make this combination, there's
19 not a insulator under the metal, there's a
01:29 20 semiconductor layer, as the Board pointed out.
21 In our case, it's either a p-type gallium
22 nitride or it could be p-type aluminum gallium
23 nitride cap -- capping layer in the terminology of
24 Saxler.
01:30 25 However, the metal that sits on that --

01:30 1 top of that semiconductor surface -- and the
2 sidewalls, presumably, have already been exposed --
3 those surfaces deplete the semiconductor of holes.

4 This is a p-type semiconductor dope of
01:30 5 magnesium, and it would normally have holes. But
6 because of these side surfaces, the holes are
7 depleted away from the surface where the etching is
8 occurring.

9 And what that means is, is that the
01:30 10 semiconductor layer behaves as an insulator just
11 like Shenoy's structure, because there are no mobile
12 charges near the etching region in the
13 semiconductor. Okay?

14 The other point that affects the edge is
01:31 15 that -- the fact that -- and the majority of these
16 liquid metal etches that I've referred to, they
17 don't touch the gallium nitride.

18 Gallium nitride is a pretty tough material
19 to etch, and a lot of these etches will not etch it.

01:31 20 So that -- that's, again, like Shenoy:
21 The insulator is not being etched in Shenoy. In
22 this case, the p-type cap below the metal was not
23 being etched when we make the combination.

24 Okay. The other thing the Board had to
01:31 25 say was, they commented on -- Shenoy's model does

01:31 1 focus on the angle of the metal that results from
2 the etch, which is related to the angle of the
3 photoresist.

4 The angle of the metal is not what we're
01:32 5 relying for in this combination.

6 We're using Shenoy to provide the undercut
7 of the metal. Okay? So we're not relying on it for
8 the -- for anything related to the mask-wall angle.

9 The undercut, as shown in Shenoy, is not
01:32 10 really a strong function of that angle anyway. So
11 we're relying on it for undercut. So....

12 And the other comment they made is
13 something about the film thickness.

14 I say "something" because they have
01:32 15 concerns. And so, I'm not sure exactly what they
16 are. But the film thickness, when you do an
17 undercut like this -- as you increase the film
18 thickness, the undercut increases. That's the major
19 effect of the film thickness.

01:32 20 So the undercut, in general, is on the
21 order -- that lateral dimension, on the order of the
22 thickness of the metal -- not exactly, but it's on
23 the same order.

24 I don't know if that answered your
01:33 25 question.

01:33 1 Q. That answers my question very thoroughly.
2 But I do have a couple of followups.
3 So at the very beginning of your earlier
4 answer, you mentioned that Shenoy had techniques
01:33 5 other than EMM.

6 Is that what you testified to?

7 A. Well, when a --

8 MR. DOSHI: Objection.

9 A. When a person of skill looks at Shenoy,
01:33 10 they're going to see that there are many other
11 isotropic etching techniques that can benefit from
12 Shenoy's work -- I mean, that's one way to say it.

13 And furthermore, the EMM technique that
14 Shenoy employs, there's nothing wrong with applying
01:33 15 that in our combination with Yoshida and Saxler and
16 Beach and Shenoy. The EMM technique will work fine
17 to do that. It's an option for the fabrication
18 engineer.

19 MS. SPECHT: So let's switch
01:34 20 gears and talk about Exhibit 2002 that you
21 drew for EPC's counsel earlier.

22 So we can just grab that -- and
23 go ahead and pass 2003 as well. And I'll
24 hand him that one.

01:34 25 Thank you.

01:34

1 BY MS. SPECHT:

2 Q. So Dr. Shealy, looking at 2002, does
3 Step-B apply to the prior art in this case?

4 A. Yes.

01:34

5 Q. Are there any references that you've
6 relied on in this case that Step B is not
7 representative of?

8 A. No. I mean, you said, Are there any
9 references that represent something other than this?

01:35

10 The only way to etch these surfaces in
11 these references is a plasma etch, and all plasma
12 etches produce this sloped sidewall.

13 Q. And can you explain what Step C is as well
14 and which references Step C is representative of.

01:35

15 A. Step C has been known in the art for quite
16 a while. It's a -- it's called a crystallographic
17 etch. And there are specific etch chemistries used
18 to do it.

19 But it will expose those -- it can expose
01:35 20 a perfect 90-degree plane because it's based on the
21 crystal itself.

22 And so, it's -- this is -- you know,
23 literally, this is an exposed plane with not many
24 atomic steps in it. So that's why we say it's
01:36 25 almost a perfect 90-degree angle.

01:36 1 The other part of your question: This
2 does not appear in any of the art in this case.

3 Q. Let's now talk about Exhibit 2003, which
4 I'm going to pass to you as well.

01:36 5 Exhibit 2003 is based on Figure 1B?

6 A. Yes.

7 Q. Of the Saxler reference. Right?

8 A. Yes.

9 Q. And do you recall asking EPC's counsel if
01:36 10 you could instead draw a figure related to your
11 modified 1A of Saxler's reference?

12 A. Yes.

13 Q. Can you draw a representative diagram
14 using your modified 1A?

01:37 15 A. Okay. So we need to start with the
16 modified....

17 I'll label this "A" in this diagram.

18 All I'm doing in the "A" illustration is
19 attempt to reproduce the -- in fact, it wouldn't be
01:37 20 a bad idea to look at it.

21 (Witness reading.)

22 A. Okay. This is the simplified diagram of
23 the modified Figure 1A, where the recess is removed
24 and p-dopants are added in the capping layer.

01:38 25 And so, now we need to identify the

01:38 1 regions where the sloped walls are.
2 And now we'll draw the -- in
3 Illustration~B, we'll draw -- what was -- where is
4 the other one? -- we'll draw the off condition to
01:39 5 correspond to the other diagram.
6 Okay. So again, we have an electron gas
7 underneath the source and drain contact.
8 As you enter the slope part of the region,
9 you're picking up negative charge. So that causes a
01:40 10 gradual depletion of the electrons out of the 2D gas
11 in that region.
12 And so, basically, it looks very similar
13 to the other diagram of 1A, except the -- there's a
14 broader transition because of the sloped regions on
01:40 15 that p-type cap.
16 That's assuming it's, more or less,
17 uniformly doped -- which is the way it appears in
18 Yoshida anyway, by the way.
19 Okay. And then there's one other diagram
01:40 20 we can make -- we'll call "C."
21 And this is for the Ahn condition. Both
22 are for low drain bias.
23 Okay. So in this case, you have a 2D
24 electron gas under the source and drain contacts,
01:41 25 just like we had before.

01:41 1 And now we'll assume that we're driving
2 the gate to a reasonable level, where we've actually
3 increased the concentration over what's in the --
4 over what's in the -- under the contacts.

01:41 5 And so, it looks something like this
6 (indicating).

7 Very similar, except during -- in these
8 regions, the distribution of electrons is smeared
9 out.

01:42 10 So other than that, it's very similar.

11 Q. And in the diagram that you've just drawn,
12 which I'm going to label Exhibit 1032 in just a
13 minute, is there a gap between the cap layer and the
14 Ohmic contacts?

01:42 15 A. Yeah, I kind of -- I mean, it's a little
16 more exaggerated than what it was in the original
17 drawing. But it's basically the same.

18 MS. SPECHT: Okay. So let's
19 mark that paper Petitioner's Exhibit 1032.

01:42 20 And we'll use the same one in
21 both proceedings -- no need to put a
22 proceeding number on.

23 (Whereupon, Exhibit 1032 was marked for
24 identification.)

01:42 25 MS. SPECHT: And with that, pass

01:42

1 the witness.

2 FURTHER EXAMINATION

3 BY MR. DOSHI:

4 Q. Just a couple of questions.

01:42

5 You were talking about Shenoy and the
6 insulator. Right?

7 A. Yes.

8 Q. Okay. And is there an insulator in
9 Saxler?

01:42

10 A. The....

11 Semiconductors behave as conductors
12 sometimes and insulators in others.

13 If you deplete the mobile charge out of
14 the semiconductor, it behaves as an insulator. It
01:43 15 won't support any current flow, because there's no
16 mobile charge in it.

17 And that's what happens when you surround
18 this p-type layer with surfaces and a metal.

19 Metal depletes mobile charge. And a
01:43 20 surface terminated with air -- or even a liquid
21 etch, for that matter -- will also deplete the
22 mobile charge.

23 So that layer is more or less devoid of
24 mobile charge. So it behaves like an insulator.

01:43

25 Q. And what about the underlying barrier

01:43 1 layer?

2 A. The underlying barrier layer has -- it

3 basically is used to confine electrons below it.

4 It's devoid -- there's no charge in that layer.

01:43 5 What it's there for is to provide a

6 potential barrier to confine the electrons below

7 that barrier.

8 Q. Would it serve as an insulator?

9 A. What's that?

01:44 10 Q. Would the barrier layer serve as an

11 insulator?

12 A. It would not conduct if you -- there's no

13 mobile charge. So in that sense, you could say it

14 behaves like an insulator.

01:44 15 Most people wouldn't call a semiconductor

16 an insulator. But they certainly can behave like an

17 insulator.

18 Q. So you were saying that the etching

19 process of Shenoy, it uses the insulator to spread

01:44 20 the horizontal etching.

21 Is that -- is my understanding correct?

22 A. The fact that it doesn't etch --

23 Q. Yeah.

24 A. -- enhances the lateral etching.

01:44 25 Q. Well, isn't it going to etch the barrier

01:44 1 layer, though?

2 A. No. The barrier layer is covered up.

3 Q. With what?

4 A. It's covered up with the -- when you do

01:45 5 this gate processing, if the Ohmics are there,

6 they're going to be covered up.

7 If it's done first, they're not there.

8 But it's still -- that surface is going to be

9 covered up.

01:45 10 Q. Isn't there a cap between the p-n and the

11 Ohmic contacts? Didn't you just testify to that?

12 A. Are we talking vertically?

13 Q. You were talking about 1A, right? -- right

14 now --

01:45 15 A. Yeah.

16 Q. -- recently.

17 And what I'm asking is the barrier

18 layer --

19 A. Oh, no --

01:45 20 (Simultaneous speaking.)

21 A. No, there's -- there's no conduction

22 there.

23 And when you perform this process of

24 etching this metal, this -- if you do Ohmic first,

01:45 25 you're going to cover those up with a -- and you'll

01:45 1 cover them up with a -- you typically would cover it
2 up, just as you read in Yoshida, with SiO₂. It's a
3 very common material to....

4 If you want to process something over here
01:45 5 and have this not influence the process, you cover
6 it up with an insulator.

7 Q. And when you cover it up, you're doing
8 selective covering. Correct?

9 So you're using a masking process, in
01:46 10 other words?

11 A. You would have to -- it would take a
12 masking process to open a window where you're going
13 to do the gate work and cover up the Ohmics.

14 Q. So you'd have to put in the silicon
01:46 15 oxide --

16 A. That's one way to do it, yeah.

17 Q. -- and then you're going to etch the
18 window. Right?

19 A. And the SiO₂ --

01:46 20 Q. Right.

21 A. -- to expose the gate region.

22 Q. Okay. And then you expose the gate
23 region. Correct?

24 A. Yeah.

01:46 25 Q. All right. You do your etching process.

01:46 1 And then do you --

2 A. You got to put the metal down first.

3 Q. Okay. And then do you remove the silicon

4 oxide?

01:46 5 A. Yes.

6 MR. DOSHI: Okay. All right.

7 That's it.

8 MS. SPECHT: No further

9 questions on our side.

01:46 10 MR. DOSHI: Okay.

11 COURT REPORTER:

12 Confidentiality? Read and sign?

13 Anything I need to know?

14 MS. SPECHT: We'll say read and

01:46 15 sign, but....

16 The Board doesn't really let you

17 read and sign, but we'll say we will just

18 in case.

19 COURT REPORTER: Okay.

01:46 20 MR. DOSHI: Off the record.

21 (Time noted: 1:46 p.m.)

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DEPONENT'S SIGNATURE

Please be advised I have read the foregoing deposition, pages 1 through 110, inclusive. I hereby state there are:

(Check one)

_____ No corrections

_____ Corrections per attached

JAMES RICHARD SHEALY, PH.D.

- (X) Reading and signing was requested.
() Reading and signing was waived.
() Reading and signing was not requested.

Should the signature of the witness not be affixed to the deposition, the witness shall not have availed himself of the opportunity to sign or the signature has been waived.

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ERRATA SHEET

**NAME OF CASE: Innoscience, et al. v. EPC
Corporation**

DATE OF DEPOSITION: May 16, 2024

NAME OF WITNESS: JAMES RICHARD SHEALY, PH.D.

Reason Codes:

1: To clarify the record.

2: To conform to the facts.

3: To correct transcription error.

Page _____	Line _____	Reason _____
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JAMES RICHARD SHEALY, PH.D. DATE

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DECLARATION UNDER PENALTY OF PERJURY

I am the witness in the foregoing deposition.

I have read the foregoing deposition or have had read to me the foregoing deposition, and having made such changes and corrections as I desired, I certify that the same is true in my own knowledge.

I hereby declare under penalty of perjury that the foregoing is true and correct.

In witness whereof, I hereby subscribe my name this _____ day of _____, 2024.

JAMES RICHARD SHEALY, PH.D.

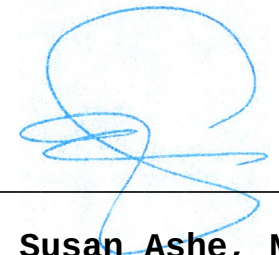
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CERTIFICATE

I, SUSAN ASHE, a Registered Merit Reporter and Notary Public, hereby certify that the foregoing is a true and accurate transcript of the deposition of said witness, who was first duly sworn by me on the date and place hereinbefore set forth.

I FURTHER CERTIFY that I am neither attorney nor counsel, nor related to or employed by any of the parties to the action in which this deposition was taken, and further that I am not a relative or employee of any attorney or counsel employed in this action, nor am I financially interested in this case.

Dated this 20th day of May 2024.



Susan Ashe, Notary Public

for the Commonwealth of Virginia

My commission expires: January 31, 2027.
Notary Registration Number: 100809.

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