UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,

Petitioner, v.

EFFICIENT POWER CONVERSION CORPORATION,

Patent Owner.

IPR2023-01382

U.S. Patent Nos. 9,748,347

Declaration of E. Fred Schubert, PhD.

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Cited Exhibit List

Exhibit	Description of Exhibit
1001	U.S. Patent No. 9,748,347 B2 to Cao et al. ("the '347 patent")
1003	Declaration of Dr. James Richard Shealy
1006	Certified Translation of Japanese Patent Publication No. JP H11 261053 to Yoshida ("Yoshida")
1007	U.S. Patent Application Publication No. US 2006/0108606 A1 to Saxler et al. ("Saxler")
1008	U.S. Patent Application Publication No. US 2007/0007547 A1 to Beach ("Beach")
1009	R.V. Shenoy and M. Datta, Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining, 143 J. Electrochemical Soc'y, pp. 544-549 (1996) ("Shenoy")
1010	U.S. Patent No. 5,905,274 to Ahn et al. ("Ahn")
1011	U.S. Patent Application Publication No. US 2010/0258843 A1 to Lidow et al. ("Lidow")
1014	Chua Xu et al., The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaN/GaN Heterostructure, 28 IEEE Electron Device Letters, pp. 942-944 (2007) ("Xu")
1015	U.S. Patent Application Publication No. US 2002/0066908 A1 to Smith ("Smith")
1017	U.S. Patent Application Publication No. US 2009/0072272 A1 to Suh et al. ("Suh")
1018	X. Hu et al., Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate, 36 Electronics Letters, pp. 753-754 (2000) ("Hu")

1019	U.S. Patent Application Publication No. US 2005/0087763 A1 to Kanda et al. ("Kanda")
1020	Yasushiro Uemoto et al., A Normally-off AlGaN/GaN Transistor with RonA=2.6Ωcm2 and BVds=640V Using Conductivity Modulation, 2006 International Electron Devices Meeting, IEEE (2006) ("Uemoto")
1021	U.S. Patent Application Publication No. US 2006/0019435 A1 to Sheppard et al. ("Sheppard")
1027	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 ("Beach-II")
1028	Petitioner and Complainant's Proposed Claim Construction, ITC 337 TA-1366
2004	Certified Transcript of Oral Deposition of Dr. James Shealy
2007(347)	Petition for Inter Partes Review of U.S. Patent. No. 10,312,335
2007(335)	Petition for Inter Partes Review of U.S. Patent. No. 9,748,347
2006	Curriculum Vitae of Dr. E. Fred Schubert
EX2008	Evidentiary Hearing Transcript, pages 741-984 (Inv. No. 337-TA-1366) (Public)
EX2009	Respondents' Post-Hearing Initial Brief (Inv. No. 337-TA-1366)

I. Introduction

1. My full name is Eric Fred Schubert, Ph.D., and I have been retained as a technical expert by Blank Rome LLP, counsel for Patent Owner Efficient Power Conversion Corporation ("Patent Owner" or "EPC") to provide expert opinions with respect to claims 1-3 of U.S. Patent 9,748,347 (the "'347 patent") in connection with *Inter Partes* Review Proceeding No. IPR2023-01382 and claims 1-7 of U.S. Patent 10,312,335 (the "'335 patent", collectively "the Patents") in connection with *Inter Partes* Review Proceeding No. IPR2023-01384 (collectively, "the IPRs"), each initiated by Petitioners Petitioner (Zhuhai) Technology Company, Ltd., and Petitioner America, Inc. (collectively, "Petitioner" or "Innoscience").

2. This is my declaration detailing my opinions in the above-captioned *Inter Partes* Review Proceeding. The opinions expressed are my own, and I have personal knowledge of the facts stated herein. If called for deposition, I will be prepared to testify competently to the facts and opinions herein.

3. To the extent necessary, in addition to what is included in this report, I am prepared to testify to additional technical background as necessary and elaborate on the opinions and theories expressed herein.

4. I am being compensated at my standard rate for my study and testimony in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this *Inter Partes* Review Proceeding. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

II. Background

A. Qualifications and Professional Experience

5. I am an active tenured full professor in the Department of Electrical, Computer, and Systems Engineering at Rensselaer Polytechnic Institute (RPI) located in Troy, New York.

6. I earned the U.S. equivalents of a Ph.D. in 1986, a Master of Science in 1981, and a Bachelor's degree in 1978, all in Electrical Engineering, from the University of Stuttgart in Germany.

7. From 1985 to 1995, I was initially a post-doctoral member of the technical staff, and later a member of the technical staff, principal investigator, and member of management at AT&T Bell Laboratories Murray Hill, New Jersey. Subsequently, from 1995 to 2002, I was a tenured full professor in the Department of Electrical and Computer Engineering at Boston University. I also served as the director of Boston University's Semiconductor Devices Research Laboratory. In 2002, I joined the faculty of RPI where I held multiple positions including the Wellfleet Senior Constellation Professor and Head of the Future Chips Constellation with appointments in the Department for Electrical, Computer, and Systems Engineering and the Department for Physics, Applied Physics and Astronomy. In 2008-2009, I served as the founding director for RPI's Engineering Research Center for Smart Lighting, which was funded by the National Science Foundation at a volume of $40 million for over 10 years.

8. My Curriculum vitae (CV) is submitted as Exhibit 2006 for both Matters. As shown by my CV, I have been working in the field of semiconductors, including gallium nitride (GaN) technology, doping in semiconductors, and high-electron mobility transistors (HEMTs) for over twenty-five years.

9. I am named as co-inventor in more than 35 U.S. patents and have co-authored more than 300 publications. I authored the books "Doping in III-V Semiconductors" (1993), "Delta Doping of Semiconductors" (1996), "Physical Foundations of Solid-State Devices" (2015) and the first, second, and third editions of "Light-Emitting Diodes" (2003, 2006, and 2018); the latter book is known as a standard textbook in the field of LEDs, and the book has been translated into Russian,

Japanese, and Korean. My publications have been well recognized by the technical community as illustrated by the more than 40,000 citations that my publications have received.

10. I have received several awards for my technical contributions. They include: Senior Member IEEE (1993); Literature Prize of Verein Deutscher Elektrotechniker for my book "Doping in III-V-Semiconductors" (1994); Fellow SPIR (1999); Alexander von Humboldt Senior Research Award (1999); Fellow IEEE (1999); Fellow OSA (2000); Boston University Provost Innovation Award (2000); Discovery Magazine Award for Technological Innovation (2000); R&D 100 Award for RCLED (2001); Fellow APS (2001); RPI Trustees Award for Faculty Achievement (2002 and 2008); honorary membership in ETA Kappa Nu (2004); 25 Most Innovative Micro- and Nano- Products of the Year Award of R&D Magazine (2007); and Scientific American 50 Award (2007).

11. I have been working on and am familiar with various types of transistors, including field-effect transistors (FETs), metal-semiconductor FETs (MESFETs), metal oxide semiconductor FETs (MOSFETs), metal-insulator-semiconductor FETs (MISFETs), and HEMTs. My general expertise is in the field of electrical engineering and applied physics, including semiconductors, processing, and devices. My specific expertise is in the field of semiconductor materials (such as GaN), semiconductor devices, semiconductor integrated circuits, ohmic contacts, Schottky contacts, HEMTs, and optoelectronic devices such as light-emitting diodes (LEDs). My work has included the design, growth, fabrication, and testing of semiconductor devices as well as the employment of these devices in a variety of applications. I have made pioneering contributions to the following technical fields that are relevant to the present matter: HETMs, two-dimensional electron gas (2DEG) structures, polarization effects in GaN materials, delta-doping of semiconductors, monolayer doping of semiconductors, integrated circuit

fabrication processes, Schottky contacts, ohmic contacts, polarization-enhanced ohmic contacts, delta-doped ohmic contacts, non-alloyed ohmic contacts, fabrication technologies for HEMTs, parallel conduction in HEMTs, and theory of FETs. In particular, I am familiar with both the design of such transistors and the manufacturing processes used for FETs.

12. There are two main types of materials used for FETs. The first type of material being silicon and the second type of material being group III-V semiconductors, such as GaN. My research and development work included the design of FETs, epitaxial growth of FET wafers, the fabrication of FETs, the assessment of specific performance parameters of FETs, and the theory of FETs.

13. I have written several publications on FET technology, specifically HEMTs, as detailed in my CV (EX2006). My publications and U.S. patents on technology relevant to the present matter include, but are not limited to the following:

- J. E. Cunningham, E. F. Schubert, and W. T. Tsang, "Delta doped ohmic metal to semiconductor contacts" U.S. Patent No. 4,772,934, issued on September 20, 1988.
- J. E. Cunningham, E. F. Schubert, and W. T. Tsang, "Field-effect transistor having a delta-doped ohmic contact" U.S. Patent No. 4,780,748, issued on October 25, 1988.
- E.F. Schubert, K. Ploog, H. Dämbkes., and K. Heime: Selectively doped n-AlGaAs/transistors. Part I: Effect of parallel conductance" Applied Physics A33, 63 (1984).
- E. F. Schubert, K. Ploog, H Dämbkes., and K. Heime "Selectively doped n-AlGaAs/GaAs heterostructures with high-mobility two-dimensional electron gas for field-effect transistors. Part II: Hot electron effects" Applied Physics A33, 183 (1984).
- E. F. Schubert, J. E. Cunningham, W. T. Tsang, and T. H. Chiu "Delta-doped ohmic

contacts to n-GaAs" Applied Physics Letters 49, 292 (1986) and Applied Physics Letters 49, 984 (1986).

- Y.-L. Li, E. F. Schubert, J. W. Graff, A. Osinsky, and W. F. Schaff "Low-resistance ohmic contacts to p-type GaN" Applied Physics Letters 76, 2728 (May 2000).
- T. Gessmann, Y.-L. Li, E. L. Waldron, J. W. Graff, and E. F. Schubert "Ohmic contacts to p-type GaN mediated by polarization fields in thin InGaN capping layers" Applied Physics Letters 80, 986 (Feb. 2002).
- T. Gessmann, Y.-L. Li, E. L. Waldron, and E. F. Schubert "Novel type of ohmic contacts to p-doped GaN using polarization fields in thin InGaN capping layer" J. of Electronic Materials 80, 416 (May 2002).
- T. Gessmann, J. W. Graff, Y.-L. Li, E. L. Waldron, and E. F. Schubert "Ohmic contact technology in III-V nitrides using polarization effects in cap layers" Proceedings of the Lester Eastman conference on high-speed devices (Sept. 2002).
- T. Gessmann, J. W. Graff, Y.-L. Li, E. L. Waldron, and E. F. Schubert "Ohmic contacts to III-V nitrides using polarization effects of cap layers" Journal of Applied Physics 92, 3740 (October 2002).
- Seung Cheol Han, Jae-Kwan Kim, Jun Young Kim, Dong Min Lee, Jae-Sik Yoon, Jong-Kyu Kim, E. F. Schubert, and Ji-Myon Lee "Ohmic contacts to N-face p-type GaN using Ni/Au for the fabrication of polarization inverted light-emitting diodes" Journal of Nanoscience and Nanotechnology 13, 5715 (Aug. 2013).
- Dissertation by E. F. Schubert, "Modern Schottky gate field-effect transistors based on III-V semiconductors" (University of Stuttgart, Germany, 1986).
- "Physical Foundations of Solid-State Devices" (Book, Google Books, Mountain

View CA, 2015).

14. Further, at RPI, I regularly teach on the subject of microelectronics, including FETs and microelectronic fabrication technologies. In our research laboratories at RPI, we routinely measure the properties of FETs including their ON resistance, contact resistance, and amplification. We also assess structural aspects of semiconductor devices, such as FETs, utilizing techniques such as SIMS (secondary ion mass spectrometry), AES (Auger electron spectroscopy), SEM (scanning electron microscopy), TEM (transmission electron microscopy), and ellipsometry.

15. For a complete list of my professional experiences, please see my CV.

16. I am being compensated at my standard rate for my study and testimony in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this Review Proceeding. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

B. Scope of Declaration

17. For each of the IPRs, I have been asked to review and analyze the Petition (Paper 1, "Pet.('347)" for the '347 Patent and "Pet.('335)" for the '335 Patent"), Patent Owner's Preliminary Response (Paper 7), Petitioner's Reply (Paper 8), Patent Owner's Sur-Reply (Paper 10), the Decision Granting Institution (Paper 11, "Institution"), and Dr. Shealy's Declaration (Exhibit 1003), for each of the IPRs. I note that the papers and exhibits are numbered similarly for each of the IPRs. In considering these documents, I have also been asked to review all exhibits and prior cited or relied on therein. Further, I have been asked to provide my independent analyses and opinions regarding these documents.

18. I have also been asked to provide my opinions as to whether a person of ordinary skill in the art (POSA) would have found the claims 1-3 of the '347 patent and claims 1-7 of the

’335 patent obvious in view of certain prior art, discussed below, and how a POSA would have understood the claimed invention in formulating that opinion.

19. For the purposes of my Declaration, I have been asked to assume that the priority date of the Patents is April 8, 2009.

III. Person of Ordinary Skill

20. Based on the description in the ’347 patent (and the ’508 patent from which it claims priority) and the relevant art discussed during the prosecution history and cited on the patent, I believe that a person of ordinary skill in the art in the contact of the ’347 patent would have possessed at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN. Relevant graduate education could substitute for the professional work experience. However, the difference between Innoscience’s proposed POSA and EPC’s proposed POSA would not affect the outcome of this proceeding or change his opinion in any material manner.

IV. Legal Framework

21. I understand that it is the burden of Petitioner to prove invalidity, and the burden of proof never shifts to the Patent Owner to prove validity.

22. I further understand that in “an inter partes review, the burden of persuasion is on Petitioner to prove unpatentability by a preponderance of the evidence, and that burden never shifts to the patentee.”

23. I further understand that factual determinations behind a finding of obviousness include: (1) the scope and content of the prior art, (2) the level of ordinary skill in the prior art, (3) the differences between the claimed invention and the prior art, and (4) secondary considerations of non-obviousness.

24. I further understand that secondary considerations of non-obviousness include commercial success, long felt but unresolved need, copying by others, and the failure of others, and can be used as evidence to show non-obviousness. I understand there must be a nexus between the evidence and the merits of the claimed invention.

25. I further understand that obviousness is determined at the time of the invention, and that hindsight recreation of the claimed invention is impermissible. In other words, what would be obvious to us at the filing of the Petition should not be considered as to what would have been obvious at the time of the invention (2009). I understand that it is not enough to show what a POSA could have done to show obviousness, but rather what a POSA would have been motivated to do at the time of the invention. I further understand that it is not enough to show obviousness what a POSA would have done when presented with two or more references, but what a POSA would have been motivated to select those references and combine them to arrive at the claimed invention.

26. I further understand that prior art cannot be combined if the proposed combination and/or modification renders the prior art unsatisfactory for its intended purposes or that the proposed combination and/or modification destroys the operability of the prior art including its combinations.

27. I further understand that an obviousness determination requires that a POSA would have perceived a reasonable expectation of success in making the invention in light of the prior art.

V. Technical Background

A. Background on nitride transistors

28. GaN FETs are known for their ability to carry greater current and withstand higher voltages than their silicon counterparts. GaN has a higher band gap energy than prior generation

silicon and therefore can be operated at a higher temperature before its properties degrade. The band gap refers to the gap between the valence band – a lower energy band filled with electrons – and the conduction band – a higher energy band to which electrons can be excited if the material absorbs a certain amount of energy. GaN devices that are smaller than silicon devices can provide a similar or lower ON resistance because dielectric breakdown (arcing) does not readily occur in GaN even at shorter distances between a source and a drain.

29. GaN is a piezoelectric material, which means that its crystal produces an electric field when strained. When a thin layer of aluminum gallium nitride (AlGaN) is added to the surface of the GaN, a substantial strain can be created, resulting in an electrical field that attracts electrons to the GaN surface. That attraction of electrons results in the formation of a two-dimensional electron gas (2DEG) that is highly conductive and able to carry a large current. The 2DEG is a thin sheet of free electrons located at the interface between two semiconductor layers, typically a GaN buffer layer and an AlGaN barrier layer. The barrier and buffer layer and associated 2DEG extend across the surface of a wafer, so that the 2DEG can serve as an electron channel between the source and drain of a field-effect transistor. The GaN buffer and AlGaN barrier layers, and associated 2DEG, are the basis of HEMTs, such as those described by the methods of manufacturing disclosed by the Patents.

B. FET structure

30. The structure of a general type of GaN FET, such as the ones disclosed in the Patents, includes a substrate, for example, a silicon substrate, a nucleation layer, to the III-N epitaxial layers (e.g., AlGaN), a III-N buffer layer, a III-N barrier layer, and an optional p-type gate semiconductor material (e.g., p-GaN). A FET further includes three metal contacts/electrodes: source, gate and drain.

31. The source electrode serves as the source of electrons that flow from the source,

through the 2DEG electron channel (below the gate), to the drain. The drain electrode drains the electrons flowing in the electron channel towards the drain. The gate electrode is a control electrode that regulates the flow of electrons in the electron channel. Appropriate voltage on the gate electrode allows the transistor to be switched between the OFF state and the ON state. It is desirable that the gate current is zero, so that no power is expended when controlling the current flow between source and drain. The gate current is frequently referred to as gate "leakage" current, indicating that it is known to be undesirable. The gate leakage current has two components, a bulk leakage current and a surface leakage current. The bulk leakage current flows from the gate electrode, through the barrier layer, to the 2DEG. The surface leakage current flows from the gate electrode along the surface of the gate semiconductor material to the 2DEG.

32. A GaN transistor can include a variety of structures. The transistor is supported by the substrate that provides a stable mechanical support for the thin epitaxial layers grown on the substrate. Nucleation layer(s) may be provided on the substrate that nucleates epitaxial growth on the substrate. A buffer layer, for example, a GaN buffer layer, that serves as the host material for the 2DEG electron channel located between the source and drain. In some transistors, the GaN buffer layer or regions of the GaN buffer layer can be undoped to attain a high electron mobility. A barrier layer, for example an AlGaN barrier layer, can be grown on top of the buffer layer and has the purpose of inducing the 2DEG in the GaN buffer layer. On top of the barrier layer, a p-type GaN (p-GaN) gate semiconductor can be grown. The p-GaN gate semiconductor layer can have multiple functions, including increasing the gate turn-on voltage (compared with a Schottky gate) and/or depleting the 2DEG (to create E-mode transistors).

33. The GaN transistor layers may include a variety of dopants, that is, intentionally added impurities to the semiconductor material. One type of dopants are known as donor dopants

whose purpose in the semiconductor material is to donate electrons to the conduction band, thereby creating free electrons available for transport; since the electrons are negative, one may refer to the conductivity as negative-type or n-type conductivity. In short, they can make the material more conductive. A second type of dopants are acceptors whose purpose is to accept electrons from the valence band thereby creating free holes available for transport; since holes are positive, one may refer to the conductivity as positive-type or p-type conductivity.

34. Silicon (Si) is a common donor dopant in GaN. As an example of how doping works in these crystalline structures, Si preferentially occupies Ga sites in the GaN crystal. Since Si is a group-IV element, and Ga is a group-III element, Si has one loosely bound excess electron that can be donated to the conduction band, thereby enabling n-type conductivity. Magnesium (Mg) is another type of acceptor dopant in GaN. Magnesium preferentially occupies Ga sites in the GaN crystal; and since, Mg is a group-II element, and Ga is a group—III element, Mg has one fewer electron than the Ga atom it replaces. The "missing" electron may be filled by an electron from the valence band, thereby creating a free hole in the valence band and causing p-type conductivity.

C. Enhancement mode v. Depletion mode transistors

35. GaN transistor devices may be categorized as (1) a depletion-mode (D-mode or normally ON) FET or (2) a enhancement-mode (E-mode or normally OFF) FETs Depletion-mode FETs maintain an "ON" state at zero gate-source voltage allowing current to flow, while enhancement-mode FETs maintain an "OFF" state preventing current from flowing at zero gate source voltage. Depletion-mode FETs can deplete the 2DEG located near the junction of two layers having different band gaps. Specifically, in depletion-mode FETs, an electron channel that exists in the 2DEG at zero gate voltage is depleted by applying a negative gate voltage, thereby turning the FET OFF. Conversely, enhancement-mode FETs have no electron channel in the

2DEG at zero gate voltage because the electron channel has been depleted by the structure of the enhancement-mode FET, and an electron channel can be induced by applying a positive gate voltage, thereby turning the FET ON. Depletion-mode FETs are easier to fabricate, and enhancement-mode FETs can at times be more desirable. This is because an enhancement-mode FET is an electrical switch that normally is in its OFF state, so that current is blocked and thus is safe. In contrast, a depletion-mode FET is an electrical switch that is normally in its ON state, so the current is not blocked. In short, in an electrical failure, it would be safer for a FET to be in the OFF state and prevent flow of electricity.

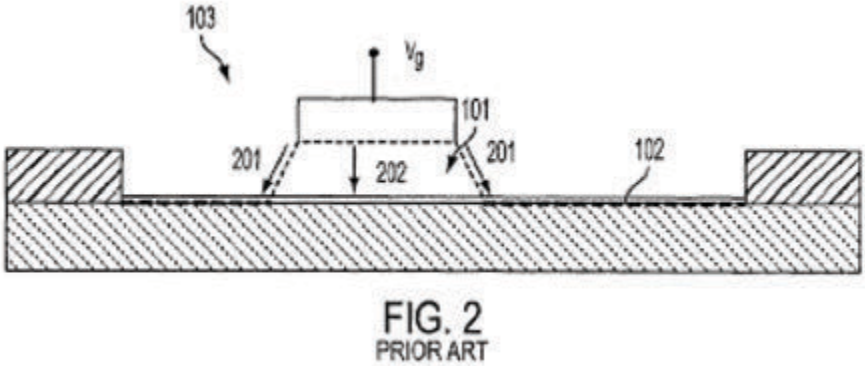
VI. Disclosure of the Patents

36. The ’335 Patent is a divisional of the ’347 Patent, thus the patents have a common disclosure. The Patents describe an enhancement mode GaN (Gallium Nitride) MISFET (Metal Insulator Semiconductor Field Effect Transistor) with self-aligned ledges and a method for forming such.

37. As further discussed in §IV.C, GaN transistor devices may be categorized into two different categories: (1) depletion-mode FETs and (2) enhancement-mode FETs. *See* the ’347 Patent, 1:45-58 (I cite to the ’347 Patent for consistency). The Patents are specifically directed to reducing a gate current between a gate leakage and a 2DEG region in an enhancement mode GaN transistor. See *Id*., 1:20-22.

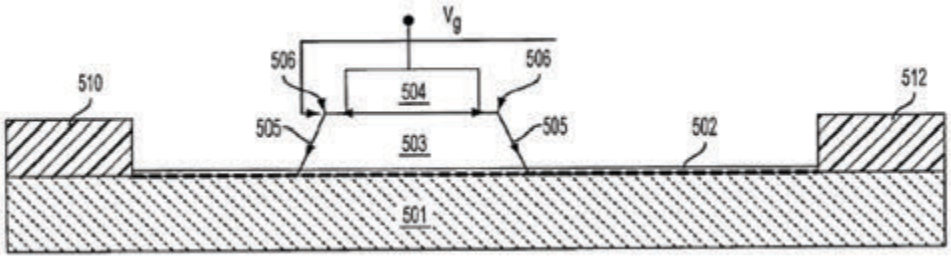
38. The Patents explain that a gate leakage current in GaN high electron mobility transistors occurs between the gate contact above gate material 101 and the 2DEG region 102 below and adjacent to the gate material along gate leakage current paths 201 (along the sidewalls of gate material 101) and 202 (through the bulk of gate material 101). *See id.* at FIG. 2 (reproduced below), 1:64-2:3. It was further identified that the gate leakage current of the prior art structure occurs predominantly along gate leakage current path 201, e.g., along the edge of the gate material.

See *id.* at FIGs. 3A, 3B, and 4 (demonstrating that an increased number of gate p-type semiconductor sidewall edges increases the gate leakage current).



The '347 Patent, Fig. 2

39. GaN FETs are known for their ability to carry greater current and withstand higher voltages than their silicon counterparts. In particular, the Patents, as shown below, innovatively teach a gate structure with an elongated surface path length that reduces the gate leakage of the device. Due to the enhanced surface path length of the elongated ledges and sidewalls of the device, there is a lower gate leakage during operation. The gate leakage current can be reduced by lengthening the gate leakage current path at the edges of the gate p-type semiconductor material by including a pair of ledges that extend horizontally towards the source and drain contacts, as shown in Fig. 5 (reproduced below). The Patents describe the ledges as self-aligned. *See id.* at 2:41-43.



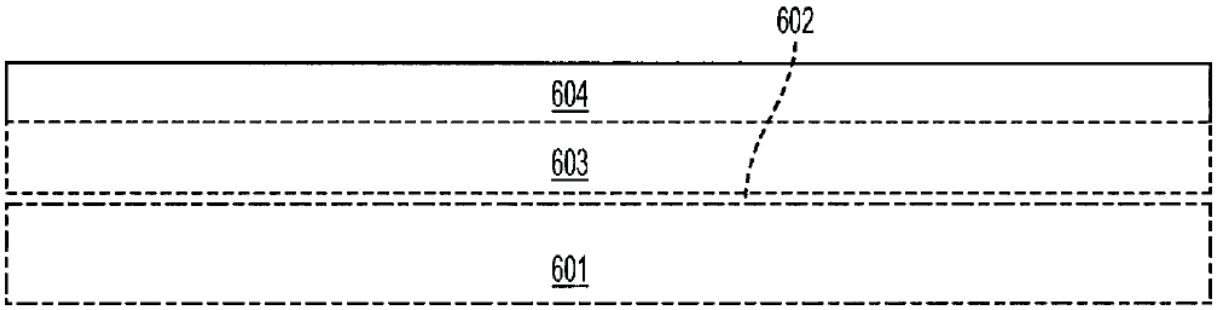
The '347 Patent, Fig. 5

40. In FIG. 5 above, the gate p-type semiconductor material 503 is positioned below

the gate metal 504 and above barrier layer 502. In some embodiments, the barrier layer is formed of AlGaN. *See id.* at 3:41-43. Gate p-type semiconductor material 503 includes ledges 506 on each side of gate metal 504. The sidewalls of gate metal 504 define a width of the gate metal which is narrower than the width of the narrowest portion of gate p-type material 503. The width of gate metal 504 being narrower than gate p-type material 503 effectively forms a pair of horizontal ledges 506 at the top of gate p-type material 503. The sidewalls, or edges, of the gate p-type material, which track reference number 505, extend respectively towards the source and drain material. In this embodiment, the narrowest portion of gate material 503 is at the top of the gate p-type material, from where the sidewalls of the gate p-type material descend towards the barrier layer, and the width of the gate p-type material increases.

41. The Patents further describe a method of manufacturing a GaN FET with the gate structure as described above.

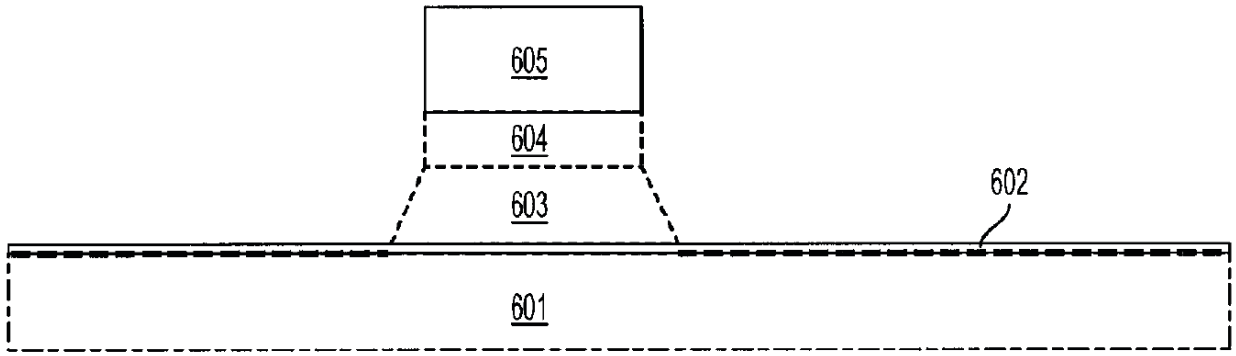
42. As shown in FIG. 6A (below), the base structure of the device is first formed with a base layer 601 of gallium nitride (GaN), a barrier layer 602 of aluminum gallium nitride (AlGaN) formed on the GaN layer 601, and a layer of p-type gate material 603 formed on the barrier layer 502, over which the gate metal 604 is deposited. *See id.* at 4:10-16.



The '347 Patent, Fig. 6A

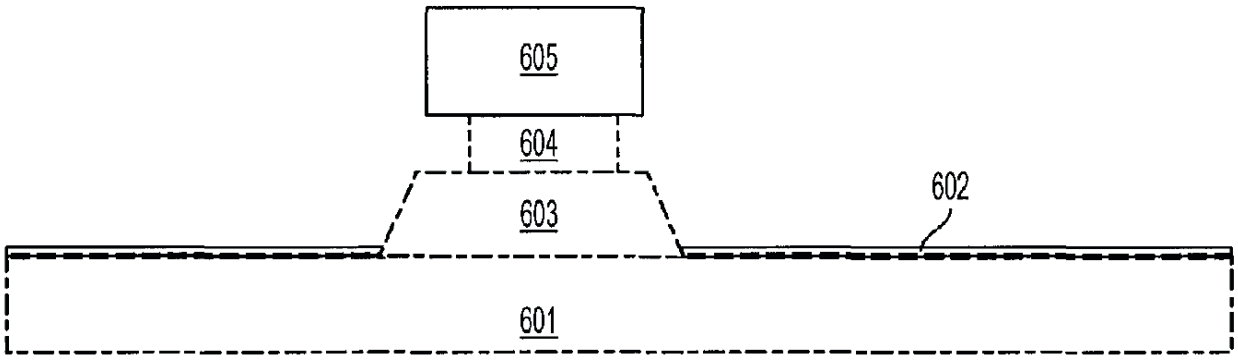
43. Next, as shown in FIG. 6B (below), a photoresist 605 is deposited and the gate metal 604 is then etched. The p-type gate material 603 is also etched in a manner that results in

the gate structure depicted in FIG. 6B. *See id.* at 4:17-20.



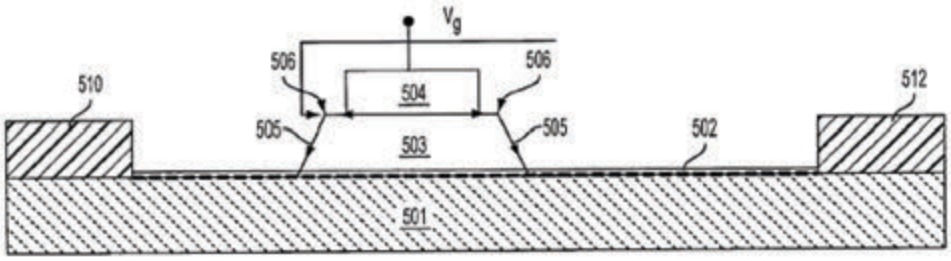
The '347 Patent, Fig. 6B

44. As shown in FIG. 6C (below), the gate metal 604 is then etched, which results in the gate metal having a width less than the planar upper surface of the p-type gate material 603. This second etching step results in the formation of the ledges 506 of the p-type gate material 603. *See id.* at 4:20-25.



The '347 Patent, Fig. 6C

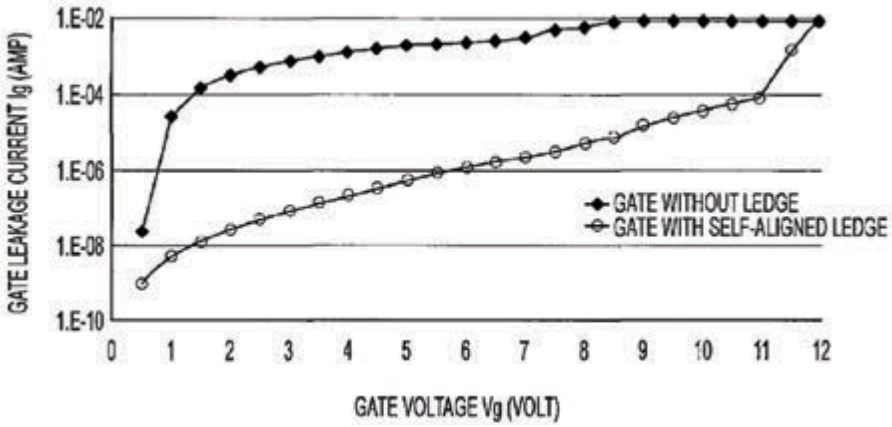
45. The photoresist 605 is then removed. Contact metals for the drain and source contacts can be separately deposited using conventional fabrication techniques, but their formation will not be described herein so as to not unnecessarily obscure the aspects of the invention. The method results in the gate with self-aligned ledges (as shown in FIG. 5) with the function as described above. *See id.* at 4:26-33.



The '347 Patent, Fig. 5A

46. As further illustrated in the transmission electron microscopy scan (TEM) of Fig. 7B, substantially equal ledges are formed through this self-aligned process.

47. Fig. 8 of the '347 patent provides data showing that the gate with self-aligned ledges has significantly lower gate leakage current than conventional gates without ledges when the transistor device is in the ON state.*See id.* at 4:41-45.



The '347 Patent, Fig. 8

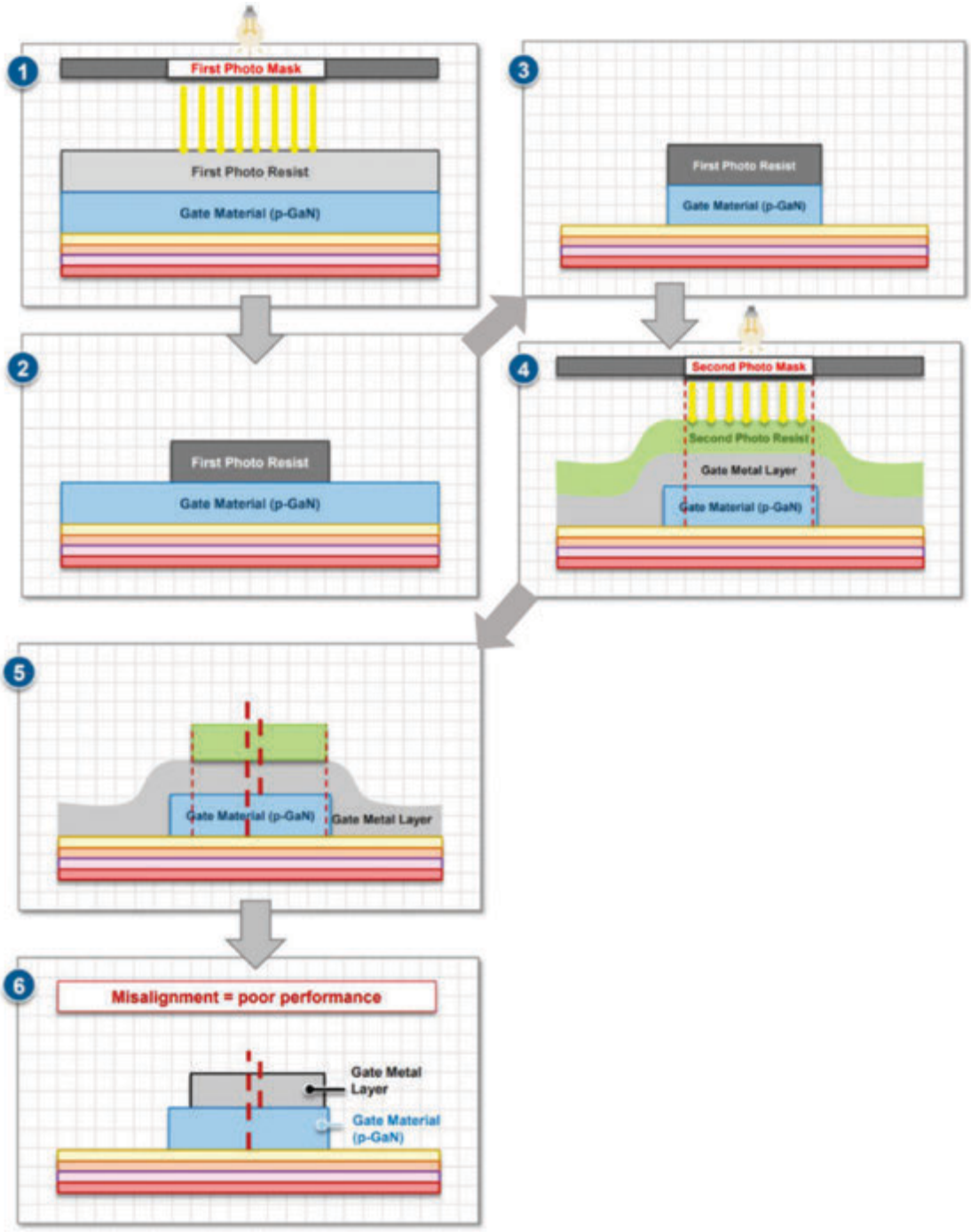
48. The described method is vastly superior to forming gate ledges using separate masks. In the process of using separate masks, a photoresist mask is applied to the unetched structure after the p-type gate material is deposited on the barrier layer of the device. In this instance, the first photomask is used to pattern and etch the gate metal to a minimum CD. A second photomask is then used to pattern and etch the p-type material with a wider CD than the gate metal. One significant disadvantage noted by the inventors of this two mask process is misalignment

between the gate metal and the p-type gate material.*See, e.g.*, **The '347 Patent**, 4:46-57.

49. In a self-aligned process, such as in the '347 patent, a single photo-mask is used to pattern and etch more than one feature thereby resulting in a self-aligned structure, whereby two features are automatically aligned with one another. The self-aligned structure is achieved because the single photo-mask pattern is used to pattern the photoresist which is then used to pattern (by etching) the first layer as the etching process proceeds downward from the top of the wafer towards the substrate. After the first layer has been etched, the photoresist can either remain or be removed because the first etched layer has now been etched to accord with the pattern transferred from the photo-mask. Then, the second layer/feature can be etched with either the photoresist and/or the top layer/feature serving to protect the portion of the second layer/feature from being etched. Through these steps, the top layer/feature and the second layer/feature share the same pattern from the photo-mask and are automatically aligned ("self-aligned") with each other. For example, with respect to the '347 patent, the patent teaches using a single photo-mask to pattern and etch both the gate metal and the gate semiconductor material. *Id*. at 4:7-28.

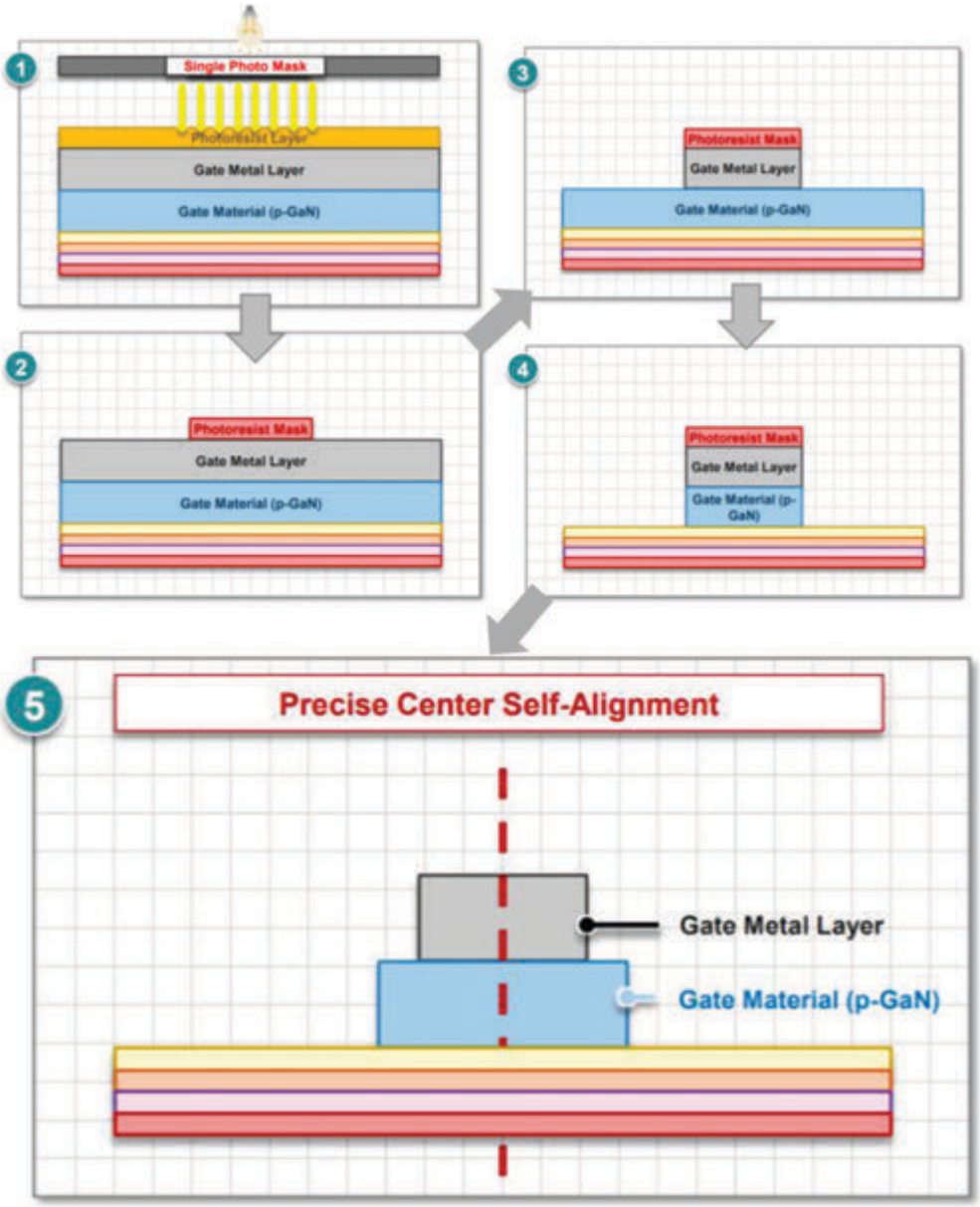
50. Self-aligned processes provide for multiple benefits to the transistor due to the lack of overlay errors. Due to such a process, the minimal critical dimension, e.g., the smallest dimension possible, as limited by photolithography, can be achieved for the gate contact. Without such a process, the gate semiconductor material (or other layers) below the gate metal had to be wider than the gate metal to accommodate for expected misalignment that occurs when more than one photo-mask is used. For example, because a feature must first be etched using a first photo-mask, and then a subsequent photo-mask would need to be aligned to that etched first feature to pattern and etch the second feature. Such second alignment generally results in misalignment thereby requiring a wider gate semiconductor material than is desired or necessary to accommodate

the two sequentially fabricated patterns. In short, naturally there is some alignment error when using two photo-masks, thereby causing overlay deviations (overlay deviations and overlay errors are used synonymously). This particular misalignment issue is solved by the ’347 patent, which uses one photo-mask to pattern multiple features and avoid misalignment, thereby only requiring the gate semiconductor material to be as wide as the desired width of the gate metal because the gate metal can be above the same width gate semiconductor material post etching. To better illustrate the differences between a self-aligning process and self-aligned structure versus a two photo-mask process, I include the following figures. An example of a form of misalignment is shown on the right due to the double photo-mask process. As can be seen, the two-photo-mask process results in the centers of the two features, specifically, the gate metal and gate semiconductor material, being out of alignment.



51. In contrast, the ’347 patent describes a single photo-mask process that achieves a self-aligned gate structure. This process advantageously results in a self-aligned gate structure with ledges of substantially equal widths, which is otherwise not achievable. A graphic representation of an embodiment of the process resulting in a self-aligned gate structure disclosed

in the ’347 patent is shown below:



52. With respect to the above Figure, step 1 illustrates: the post-epitaxial structure that includes transition layers under a gate semiconductor material, a gate metal, and a photoresist layer, the application and exposure of the photoresist layer using a single photo-mask to pattern the photoresist layer in a photolithography process (step 1), completion of the photolithography process of the photoresist (step 2), an etching step resulting in an etched gate metal using the

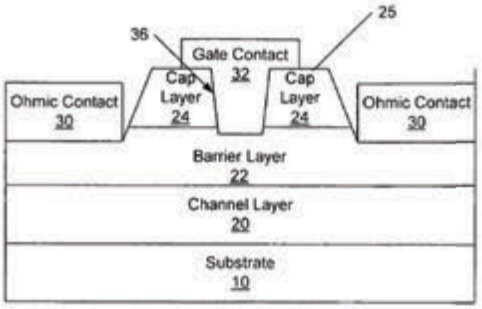
patterned photoresist (step 3), an etching step resulting in an etched gate semiconductor material (step 4) self-aligned with the gate metal, and an etch step resulting in a shaped gate metal and removal of the photoresist layer (step 5).

VII. Overview of References relied on by Petitioner

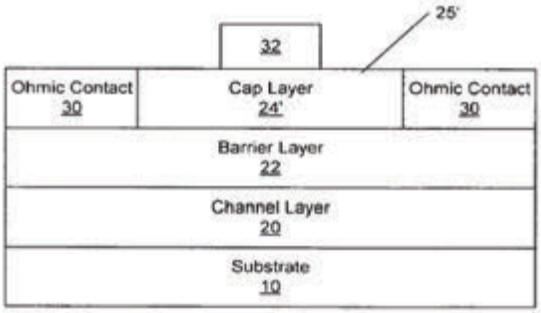
A. Saxler

53. Saxler describes a HEMT that includes a gallium nitride channel layer 20 deposited on a substrate 10 using buffer layers, transition layers, and/or nucleation layers. See EX1007 ¶57. A barrier layer 22 is provided on the channel layer 20. The channel layer 20 is a Group III-nitride having a conduction band edge energy lower than a conduction band edge energy of barrier layer 22. *Id.* ¶¶58-59. The interaction between the barrier layer 22 and channel layer 20 induces carrier concentration at the interface. *Id.* Source and drain ohmic contacts 30 are located on opposite sides of a gate 32 and graphically depicted as being located above the barrier layer. *Id.*, Figs. 1A-B.

54. The gate 32 is disposed on a cap layer 24, 24' (or 34, 34'), which is described as moving the top (outer) surface of the device physically away from the channel layer, which may reduce electrical effects of the surface. EX1007 ¶61. The cap layer 34, 34' is shown and described as two distinct embodiments - one with a recessed gate structure (Figs. 1A, 2B, hereinafter "recessed embodiment(s)") and one with a non-recessed gate structure (Figs. 2B, 1A, hereinafter "non-recessed embodiment(s)"). Both embodiments are depletion-mode HEMTs. Both embodiments are depletion-mode HEMTs.

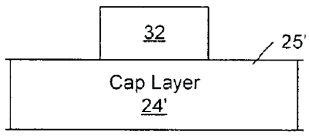
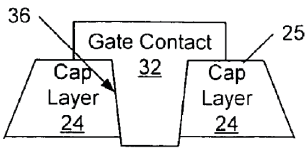


EX1007, Fig. 1A



EX1007, Fig. 1B

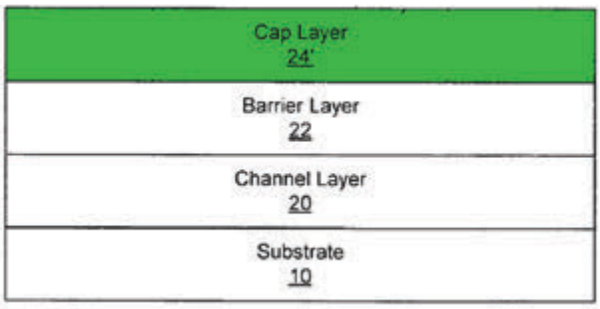
55. As can be seen in Fig. 1A, Saxler shows the cap layer 34' of the recessed embodiment as two distinct regions on either side of the gate with slanted sidewalls. On the other hand, as can be seen in Fig. 1B, Saxler shows the non-recessed gate structure as a rectangle extending from ohmic contact 30 to ohmic contact 30. Indeed, Saxler describes a number of structural and functional distinctions between the recessed embodiment and the non-recessed embodiment, including the shape, thickness, doping, and function of the cap layer. EX1007, Figs. 1A, 1B, 2A, 2B, ¶¶7, 12, 14, 27, 62, 70, 71, 73, 74, 76, 81. Saxler is deliberate in describing these distinctions and does not provide any suggestion of combining or interchanging features or parameters between the distinct non-recessed and recessed embodiments. Some of the distinctions between the embodiments are summarized in the table below.

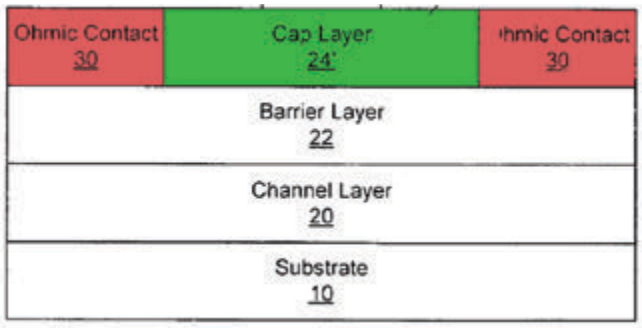
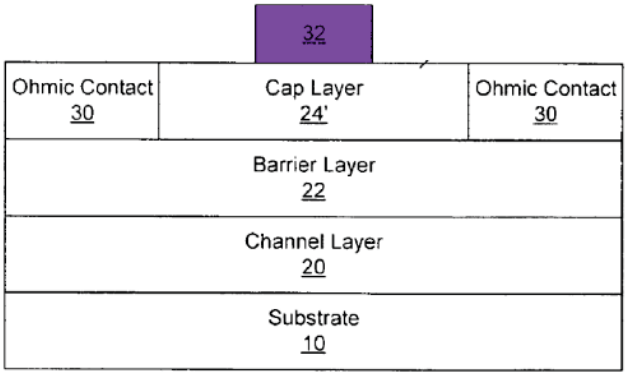
Feature(s) of Saxler	52. Non-Recessed Embodiment	53. Recessed Embodiment
Shape of cap layer and gate contact (Fig. 1B, 1A, *see also* Fig. 2A, 2B)		

Thickness of cap layer (Paragraph [0027], *see also* [0081])	"from about 2 Å to about 20 Å"	"from about 5 to about 5000 Å"
Level of doping of cap layer (Paragraph [0071], *see also* [0073])	"should be sufficiently high so as to reduce leakage current… and be the dominant 'surface' state but not so high as to [] introduce traps or leakage paths by becoming a conductive layer"	"a high level of p-type dopants may be provided such that the cap layer 34′ may be provided as a conductive layer"
Dopant concentration of cap layer (Paragraph [0012])	"from about 10^{18} to about 10^{21} cm^{-3}"	"more heavily doped than 10^{21} cm^{-3}"
Thickness of doped region (Paragraph [0012], *see also* [0014], [0070], [0071], [0073])	"into the cap layer from about 2.5 Å to about 50 Å"	"into the cap layer from about 20 Å to about 5000 Å"
Increased concentration of Al (Paragraph [0007], *see also* [0062])	"extends into the cap layer from about 2.5 Å to about 100 Å"	"extends into the cap layer from about 30 Å to about 1000 Å"

56. Saxler describes the gate contact 32 is made of nickel (Ni), platinum (Pt), nickel silicide ($NiSi_x$), copper (Cu), palladium (Pd), chromium (Cr), tungsten (W), and/or tungsten silicon nitride (WSiN). *See id.* at ¶ [0066]. The cap layer 34, 34', which, in a particular embodiment, can be magnesium (Mg) doped GaN and/or a Mg-doped AlGaN. *Id*. at ¶ [0069].

57. Saxler describes a "gate-last" fabrication process in which the cap layer 34, 34' is layered and etched to form the source and drain contacts, followed by the gate contact being deposited. EX1007 ¶¶ 63-66. Steps of Saxler's process are illustrated below.

Step	Process
1	"the cap layer 24, 24′ may be provided by conventional epitaxial growth techniques." 

2	"as is further illustrated in FIGS. 1A and 1B, ohmic contacts 30 are provided on the barrier layer 22. A patterned mask and etch process may be used to expose the underlying barrier layer 22… as is further illustrated in FIGS. 1A and 1B, ohmic metal is patterned to provide ohmic contact material patterns that when annealed provide the ohmic contacts 30." [0064] 
3	"the gate contact 32 may also be formed on the cap layer 24′ as illustrated in FIG. 1B." 

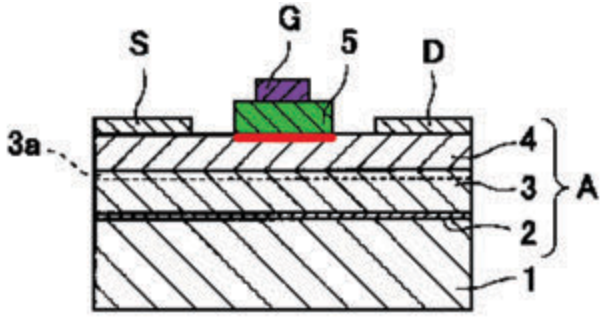
58. Saxler does not disclose a process to fabricate its gate structure beyond a general description of a potassium hydroxide (KOH) etching step that makes regions for source and drain contacts. EX1007 ¶¶64-66.Because *Saxler* teaches the use of multiple photomasks, it does not disclose a self-aligned (single photomask) process for gate formation. *Saxler* does not disclose nor suggest how to etch its cap layer or intended structural designs or configurations for its cap

layer. However, *with respect to forming the ohmic contacts 30*, Saxler describes a "patterned mask and etch process may be used to expose the underlying barrier layer." *Id*. at ¶64.Saxler does not disclose whether a dry or wet etching or patterning process is used.

B. Yoshida

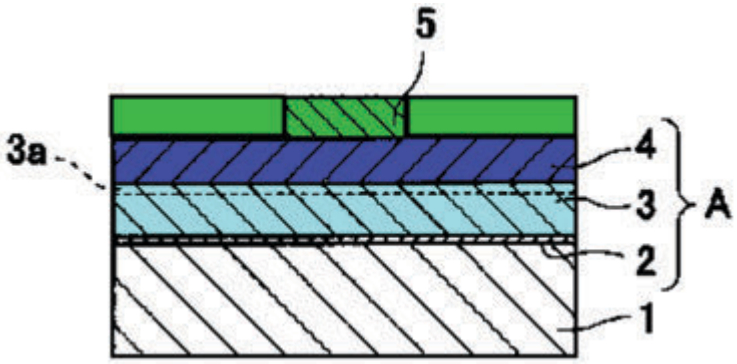
59. Yoshida discloses an enhancement mode GaN HEMT comprised of a semi-insulating substrate (1), a buffer (GaN) layer (2), an i-type semiconductor (GaN) layer (3), an n-type semiconductor (InGaN) layer (4), and a p-type GaN layer (5).

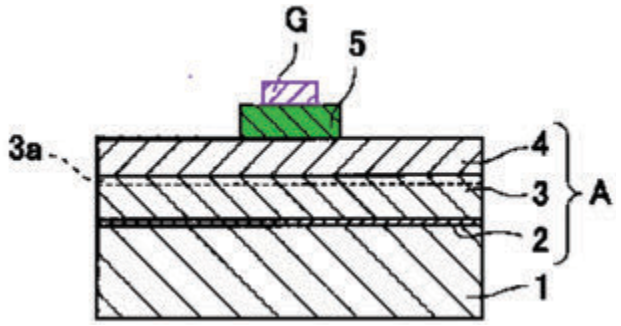
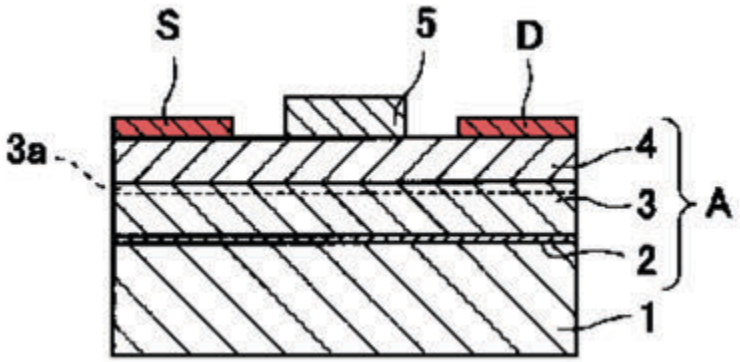
60. A pn junction formed "immediately under the gate electrode G enables voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility." EX1007 ¶17.

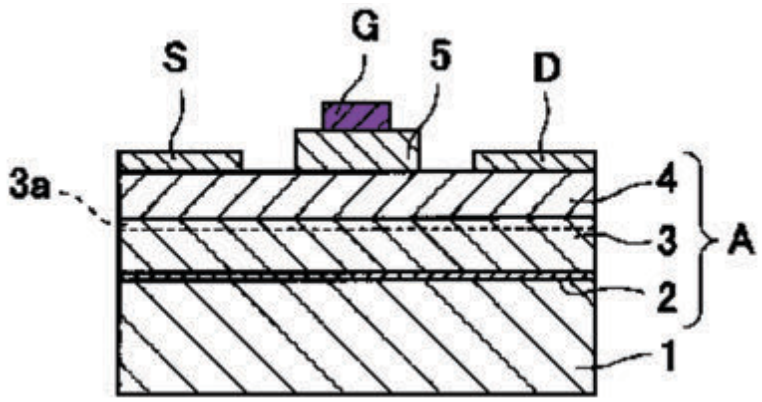


EX1007, Fig. 1 (annotated)

61. Yoshida specifically discloses that the HEMT is formed by a "gate-last" process where the p-type GaN layer 5 is deposited and etched to form the source and drain contacts S, D before the gate electrode G is deposited. More specifically Yoshida discloses "an etchant to etch away the p-type GaN layer except where the gate electrode was to be loaded." Yoshida discloses a specific order of steps as follows:

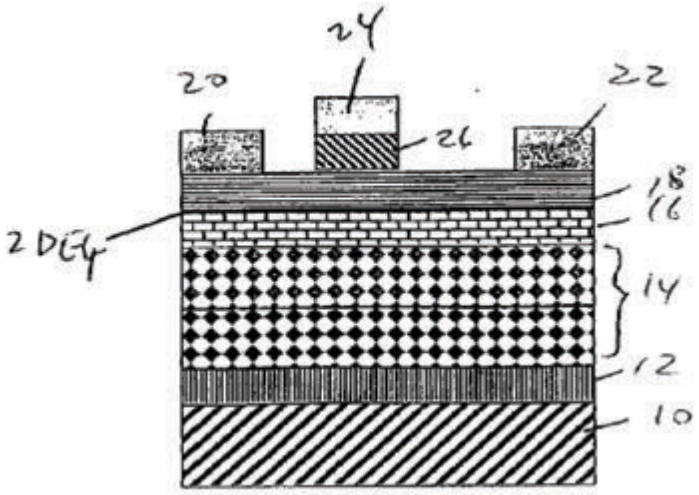
Step	Process
1	"First, a GaN buffer layer 2 with a thickness of 50 Å was deposited on a semi-insulating Si single-crystal substrate 1 by epitaxial growth… the N source was then switched over… the growth temperature increased to 850°C, and epitaxial growth resulted in the deposit of an i-type GaN layer 3 with a thickness of 5000Å… epitaxial growth was continued at a growth temperature of 850°C to deposit an ntype AlGaN layer 4 at a thickness of 500Å…. deposition operation continued to deposit a p-type GaN layer 6 with a thickness of 500 Å on the n-type AlGaN layer 4." ¶¶[0019]-[0021]  **EX1007, Fig. 1 (annotated)**

2	"Dry etching was then performed using a plasma-converted mixture of hydrogen, argon, and methane as an etchant to etch away the p-type GaN layer except where the gate electrode was to be loaded and exposing the n-type InGaN layer 4." ¶[0022]  **EX1007, Fig. 1 (annotated)**
3	"An SiO2 film was then deposited by plasma CVD to cover the entire surface, and after patterning with photoresist, the area including the part where the gate electrode was to be loaded was masked, [leaving] the portion where source and drain electrodes were to be loaded open" ¶[0022]
4	"metal Al deposited on the exposed n-type InGaN layer 4 to load source electrode S and drain electrode D." ¶[0022]  **EX1007, Fig. 1 (annotated)**

5	"Lastly, after etching away the masking and opening the SiO2 film beneath it, the source electrode S and drain electrode G locations were masked with SiO2 film, Au was deposited in the opening portions, and gate electrodes G were loaded above the p-type GaN layer 5 to fabricate the HEMT shown in Fig. 1." ¶[0023]  **EX1007, Fig. 1 (annotated)**

C. Beach

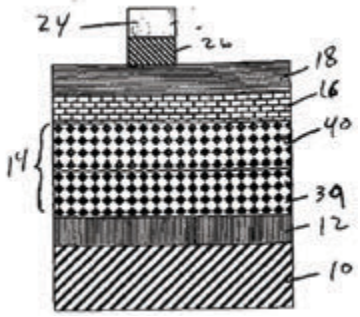
62. Beach describes a III-Nitride enhancement-mode semiconductor device, including a gate barrier layer under the gate. EX1008, Abs., Title. Beach describes a transistor (image below) including substrate 10, bonding layer 12, first III-N buffer body 14, first III-N semiconductor body 16, second III-N semiconductor body 18, first and second power electrodes 20, 22, gate barrier 26, and gate arrangement 24. *See id*. ¶¶31-32.



EX1008, Fig. 1

63. In a preferred embodiment, gate barrier 26 is an AlInGaN alloy, which can be, for example, AlGaN. *Id*. ¶ [0032]. In preferred embodiments, first III-N semiconductor body 16 is AlGaN and second III-N semiconductor body 18 is GaN. *Id*. *Beach* describes the equivalent of a 2DEG region formed at the heterojunction of first III-N semiconductor body 16 and second III-N semiconductor body 18.

64. Beach further describes the formation of its gate structure. The gate structure of gate arrangement 24 and gate barrier 26 are patterned and etched to form a self-aligned gate arrangement (*i.e.* a "gate-first" process). *Id*. ¶40, Fig 2F.



EX1008, Fig. 2F

65. Beach describes fabricating the gate structure before the ohmic contacts 20, 22 are

formed on the device. *See, e.g.*, *id*.

D. Shenoy

66. Shenoy is an article exploring the theoretical shape evolution that occurs in through-mask electrochemical micromachining (EMM) through mathematical modeling. EX1009, Abstract. *Shenoy* is not directed to the formation of GaN based semiconductors and/or HEMTs. *Shenoy* further does not disclose or suggest methods of manufacturing an enhancement-mode GaN transistor. *Shenoy* further does not address self-aligned structures.

67. Instead, Shenoy theoretically explores how deviations in photoresist mask wall angle affect the directionality of the subsequent etching process. Further, because Shenoy is based on a mathematical model, its disclosure relies upon theoretical assumptions that would not necessarily be applicable in practice, or true with respect to enhancement-mode GaN transistors and their applicable materials. EX1009, 2-3. Particularly, *Shenoy* describes the shape of an ideal evolving EEM etching cavity but does not explicitly or implicitly instruct a POSA how to etch a gate structure (including the gate metal), any particular desired patterning designs, or methods or desires to achieve particular sidewall designs. Instead, *Shenoy* is entirely ambivalent to any desired design. Further, *Shenoy* does not disclose or suggest that its etching methods or theoretical mathematical results would be applicable to GaN based materials.

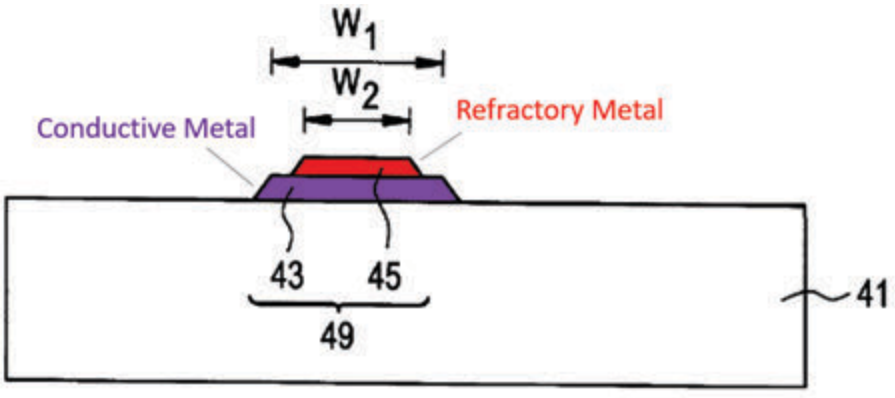
E. Ahn

68. *Ahn* is directed to thin film transistors for liquid crystal displays and discloses etching of a double-layered metal gate. EX1010, 1:5-10; 3:27-29. A thin film transistor is a special type of FET where the transistor is made by thin film deposition. For example, thin film transistors are grown on a supporting (but non-conducting) substrate, such as glass. This differs from the GaN HEMTs, where the semiconductor material typically is the substrate, such as a silicon wafer. Because the layers are thin and they are grown on inert substrates, rather than on semiconductor

wafers, the semiconductor must be deposited in a dedicated process, distinct from GaN HEMTs. Because typical substrates will deform or melt at high temperatures, the deposition process must be carried out under relatively low temperatures compared to traditional electronic material processing. The most common application for thin film transistors is TFT LCDs, an implementation of liquid-crystal display technology, where the transistors are embedded within the panel itself (due to their thinness or low profile), reducing crosstalk between pixels and improving image stability.

69. Ahn establishes that prior art gates in LCD transistors are made of a single layer of aluminum to reduce its wiring resistance, but the single layer metal gate has an issue of causing defects such as hillock. *Id.* at 1:17-19. Thus, Ahn is specifically directed to the development of a double-layered metal gate as a substitute for a single-layered metal gate to overcome the problem of the hillock. *Id.* at 1:20-23, 3:21-26.

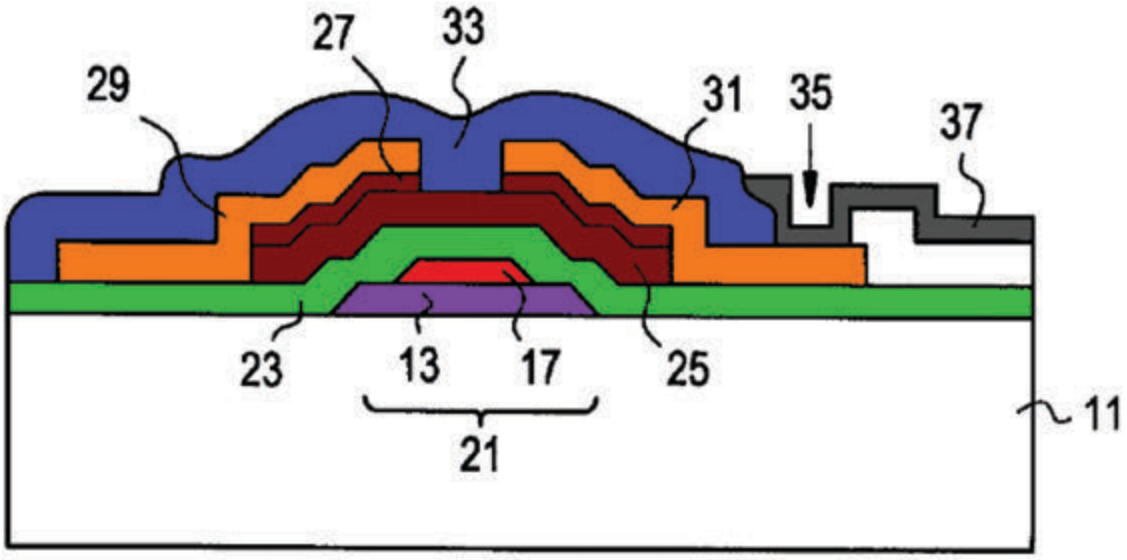
70. The double-layered metal is specifically of a bottom conductive metal layer 43 (Al, Cu, or Au) and a top refractory metal layer 45 (Mo, Ta, or Co). EX1010, 4:33-38.



EX1010, Fig. 4C (annotated)

71. As further illustrated below, the thin film transistors in Ahn have a layering structure of the double-layered gate 21 deposited on a substrate 11. Thin film transistors are named for the very reason that thin film transistors are constituted by thin films to enable the overlap of

the gate and electrode components. A first insulating layer 23 ("gate oxide layer") is deposited on the double-layered gate 21. EX1010, 2:22-26. Semiconductor and ohmic contact layers 25 and 27 are formed by sequentially depositing undoped polycrystalline silicon and heavily doped silicon on the gate oxide layer 23. *Id.* at 2:26-31. Source and drain electrodes 29, 31 are layered on the semiconductor and ohmic contact layers 25 and 27, and a second insulator 33 is deposited on the entire surface of the structure. *Id.* at 2:32-36. The semiconductor contact layer 25 provides a connection between the source and drain electrodes 29, 31 that is controlled by the gate 21. *Id.* at 2:36-38; Fig. 1F. The thin film transistor is still a FET, thus the overlying gate oxide layer 23 has to be thin (on the order of 10 nm) to be sure that double-layer metal gate structure can apply a magnetic field to the semiconductor contact layer 25.

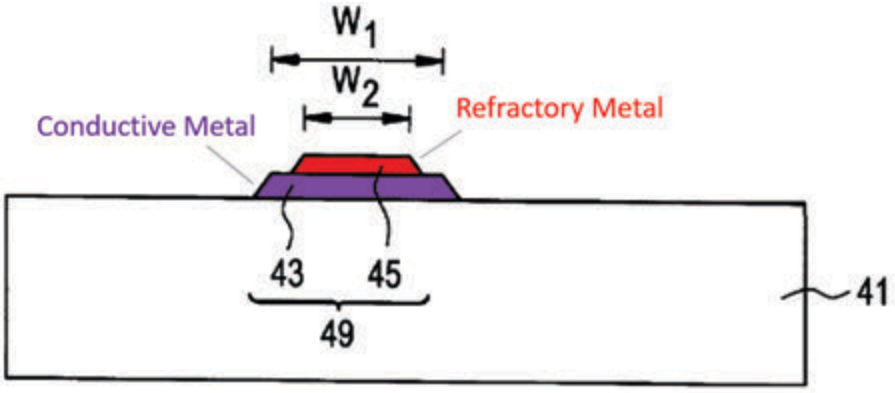


EX1010, Fig. 1F (annotated)

72. Ahn recognizes that "the source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and non overlapped with the gate." EX1010, 1:34-38. Thus, Ahn is concerned about deterioration of the gate oxide layer 23 due to this vertical arrangement in that the gate oxide layer 23 thinly

separates the semiconductive layer 25 from the gate 21. Deterioration of the gate oxide layer 23 may cause an electrical connection between the semiconductive layer 25 and the gate 21 causing a short circuit. EX1010, 1:34-38.

73. Ahn attempts to cure this problem of the double-layered metal potentially deteriorating the thin gate oxide layer 23 by making the width W1 of the bottom conductive metal layer 43 (Al, Cu, or Au) intentionally greater than the width W2 of the top refractory metal layer 45 (Mo, Ta, or Co), as further illustrated below. EX1010, 4:46-52.



EX1010, Fig. 4C (annotated)

74. The vertical arrangement, the double-layered metal gate, and the gate oxide layer of Ahn are not remotely applicable to an enhancement mode transistor. Ahn does not teach or disclose the functional use of GaN material in a gate structure nor any p-doping in its gate material. Ahn is solely directed to layering metal materials for a double layer metal gate and the cause of deterioration of the thin gate oxide layer that would cause disconnection or a short circuit. Ahn's lack of relevance to GaN transistors is further apparent from its discussion of the formation of a pixel electrode 65, "which is electrically connected to the drain electrode 59 through the contact hole 63." EX1010, 7:4-6. That pixel electrode – not a feature of GaN transistors – is present because Ahn is directed to thin film transistors with divergent structure, produced with a divergent method and for a divergent application, relating to liquid crystal displays. *Id.*, 1:5-10.

'347 PATENT

VIII. Ground 1 (Claims 1-3) of the '347 Patent - Saxler in view of Beach and Shenoy

A. Overview

75. In Ground 1, Petitioner asserts that Saxler in view of Beach and Shenoy renders obvious claims 1-3 of the '347 Patent. Petition, p. 24.

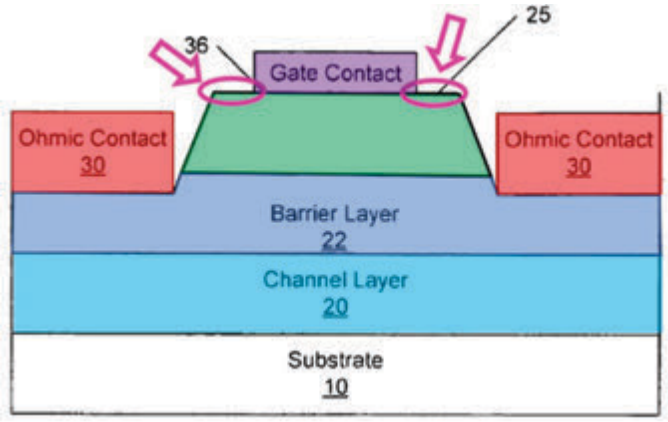
76. Initially, Petitioner misrepresents the teachings of Saxler by "mix[ing] and match[ing]" features and parameters of two distinct embodiments of Saxler to arrive at the gate structure of the '347 patent. Saxler contains absolutely no suggestion or motivation for the proposed combination of the two distinct embodiments. But the hypothetical transistor proposed by Petitioner would not operate as an enhancement-mode transistor, because Saxler describes depletion-mode transistors, not enhancement-mode transistors.

77. Petitioner recognizes that Saxler does not disclose a self-aligned technique for forming its gate structure, and therefore disregards Saxler's gate formation method and instead shoehorns the self-aligned technique of Beach, an enhancement mode transistor. But using the Beach gate formation process to form Saxler's gate would remove the source and drain metallization formed by Saxler. Moreover, the subsequent gate semiconductor etching process of Beach will remove the barrier layer in the source and drain regions and etch through the 2DEG and into the channel layer, resulting in a non-working device. So Petitioner substitutes a mathematical model of EMM etching from Shenoy that is unpredictable at best and is not even disclosed to be used to form a transistor. But Shenoy's process is not applicable and would not work to form a transistor because it requires an insulating layer underlying the metal layer. Even if a POSA were to apply the EMM etching of Shenoy, it would etch at least the claimed ledges (underlying the gate metal). This meandering path of reengineering would not be obvious to POSA and, in any event, would not arrive at the claimed method.

B. A POSA would not consider the gate recess of Saxler as "optional"

78. Saxler discloses two distinct embodiments with divergent parameters

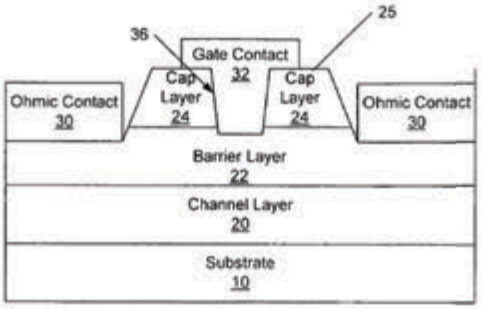
79. Petitioner alleges that "Saxler's gate contact may be recessed or non-recessed (i.e., flat). Saxler, [0052],[0066]. According to Petitioner, removal of the gate recess from the embodiment of Fig. 1A results in the following structure. Shealy, ¶081." Pet.('347) 25.



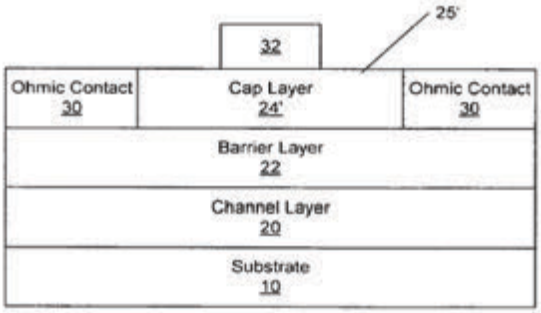
Pet.('347) 25

80. Petitioner further alleges that "although [Fig. 1A] depicts its gate recess may separate its cap layer into two portions in some embodiments, the recess in Saxler's cap layer 24 is optional, and where not employed the cap is a continuous material. Saxler, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [121]." Pet. ('347) 45.

81. I respectfully disagree. As further discussed in §VII.A, Saxler discloses two distinct embodiments. A first, recessed embodiment is illustrated in FIGS. 1A, 2B having a bifurcated recessed cap layer where the gate contact intersects and divides the cap layer. A second non-recessed embodiment is illustrated in FIG. 1B, 2A with a non-recessed gate contact positioned on top of the cap layer.

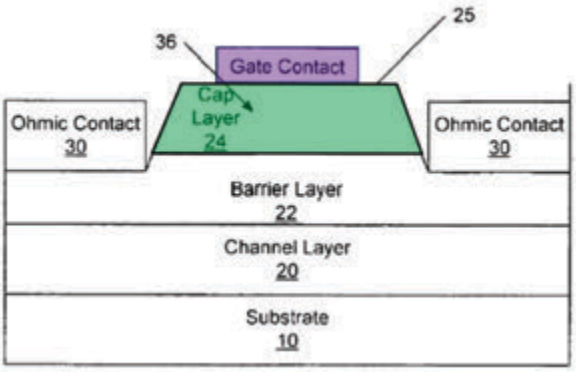


EX1007, Fig. 1A



EX1007, Fig. 1B

82. Petitioner proposes to selectively modify Saxler by removing the recess (36) in the cap layer (24) of Fig. 1A (the recessed embodiment) and copying and pasting the gate contact (32) from Fig. 1B (the non-recessed embodiment) on top of the modified cap layer (24). Petitioner later refers to this "modified" rendition of Saxler as "where the gate is not utilized" (Pet.('347) 25), but the "modified" rendition is clearly not supported by or suggested by Saxler. Indeed, a POSA would not have "at once envisage[d]" the modified figure of Saxler as alleged by Petitioner.

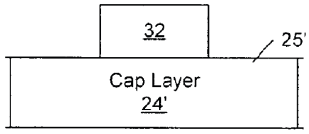
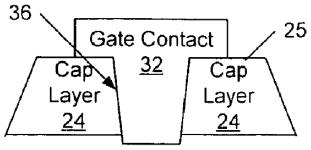


Pet.('347) 41

83. Not only is this faulty premise not supported by Saxler, but the cited passages of Saxler actually contradict Petitioner's premise by highlighting the structural and functional distinction of the cap layer 24 in the recessed embodiment and the cap layer 24' in the non-recessed embodiment.

84. For example, as relied on by the Petitioner, ¶[0012] discloses "in particular

embodiments of the present invention without a gate recess, the doped region extends into the cap layer from about 2.5 Å to about 50 Å" and "in particular embodiments of the present invention with a gate recess, the doped region extends into the cap layer from about 20 Å to about 5000 Å." Petitioner alleges that, because the recessed embodiment and the non-recessed embodiment are described in the same paragraph, they are structurally equivalent except for the presence of the gate recess. However, ¶[0012] as an example explicitly describes the embodiments as "*particular* embodiments of the present invention without a gate recess" and "*particular* embodiments of the present invention with a gate recess" (emphasis added) while distinguishing the depth of the doped regions between the non-recessed embodiment (about 2.5 Å to about 50 Å) and the recessed embodiment (20 Å to about 5000 Å). Additional exemplary distinctions are summarized below.

Feature(s) of Saxler	Non-Recessed Embodiment	Recessed Embodiment
Shape of cap layer and gate contact Fig. 1B, 1A, *see also* Fig. 2A, 2B		
Thickness of cap layer ¶27	"from about 2 Å to about 20 Å"	"from about 5 to about 5000 Å"
Level of doping of cap layer ¶71, *see also* ¶73	"should be sufficiently high so as to reduce leakage current… and be the dominant 'surface' state but not so high as to [] introduce	"a high level of p-type dopants may be provided such that the cap layer 34′ may be provided as a conductive layer"

	traps or leakage paths by becoming a conductive layer"	
Dopant concentration of cap layer ¶12	"from about 10^{18} to about 10^{21} cm^{-3}"	"more heavily doped than 10^{21} cm^{-3}"
Thickness of doped region ¶12, *see also* ¶¶14, 70, 71, 73	"into the cap layer from about 2.5 Å to about 50 Å"	"into the cap layer from about 20 Å to about 5000 Å"
Increased concentration of Al ¶7, *see also* ¶62	"extends into the cap layer from about 2.5 Å to about 100 Å"	"extends into the cap layer from about 30 Å to about 1000 Å"

85. As is evident from the above table, the cap layer of the recessed embodiment is thicker, with a higher concentration of doping and a doping layer that extends further into the cap layer, than the non-recessed embodiment. EX1007 Figs. 1A-B, ¶¶12, 13, 14, 70, 71, 27, 81.

86. When asked at his deposition about these structural and functional distinctions in Saxler, Dr. Shealy was unable to support his position that these passages disclose an "optional" gate recess. EX2004, 38:12-19. ("It was pretty clear what was stated in those paragraphs").

87. A POSA would recognize that Saxler makes substantial structural and functional changes to the cap layer 24 due to the presence of the recessed gate contact 32 compared to the

cap layer 24' in the non-recessed embodiment. For example, as noted above, the layer of the recessed embodiment is thicker with a higher concentration of doping and a doping layer that extends further into the cap layer than the non-recessed embodiment. EX1007 Figs. 1A-B, ¶¶12, 13, 14, 70, 71, 27, 81. A POSA would understand that the non-recessed embodiment is consistent with surface doping. This is supported by the fact that the thickness of the cap layer (34) is only "from about 2 Å to about 20 Å" not even a handful of lattice constants.[1] EX1007 ¶[0027]. In contrast, the thickness of the doped region 40 of the cap layer 34 is "from about 5 Å to about 5000 Å." *Id*. That is, the maximum thickness of the doped region of the non-recessed embodiments is **250** times thinner than that of the recessed embodiments, with very limited overlap with respect to the range of the recessed embodiment. Furthermore, the dopant concentration is further divergent between the two embodiments. EX1007 ¶¶12, 73. Thus, Saxler does not provide any suggestion to POSA of the dopant concentration or the thickness of the dopant for Petitioner's hypothetical transistor. Furthermore, the dopant concentration is further divergent between the two embodiments. EX1007 ¶¶12, 73. Thus, Saxler does not provide any suggestion to POSA of the dopant concentration or the thickness of the dopant for Petitioner's hypothetical transistor.

88. Saxler also changes the shape of the cap layer 24 as illustrated in Figure 1A to receive the recessed gate by producing two separate, thicker cap layers 24 and tapers the edges of the cap layers 24 due to this increased thickness. Saxler does not taper the side surfaces of the cap 24' in the non-recessed embodiment due to at least to the reduced thickness.

89. Indeed, Petitioner's expert, Dr. Shealy, explicitly opines that the non-recessed

[1] The GaN lattice constant along the growth direction is about 5 Å, so that 20 Å is less than 5 × 5 Å (less than a handful of lattice constants).

embodiment and the recessed embodiment are not functionally equivalent, conceding that "with the recess, *Saxler*'s device is not enhancement mode (always off)." EX1003 ¶146. Dr. Shealy reiterated in his deposition that Fig. 1A is depletion mode. EX2004, 59:5-10 ("as it's drawn, it would be a depletion mode device.")

90. However, removing the recess in Fig. 1A would not make Petitioner's modified/proposed transistor functional. In other words, contrary to Petitioner's assertion, the gate recess is not "optional", due to the numerous divergent features of the two distinct embodiments. EX1007, Figs. 1A, B, 2A, 2B, ¶¶7, 12, 14, 27, 62, 70, 71, 73, 74, 76, 81.

91. For at least these reasons, Saxler does not provide a POSA guidance to selectively "mix and match" features of the recessed and non-recessed embodiment of Saxler.

92. Dr. Shealy's rational of "take all the embodiments and bring in which ones you want, depending on what you're trying to accomplish" (EX2004, 38:3-5) ignores the fundamental principle that there must be a motivation to combine, and the combination must result in an operable device.

93. Paragraph [0052] of Saxler does not obviate the requirement for a motivation to combine the recessed and non-recessed embodiments of Saxler

94. At his deposition, Dr. Shealy revealed that Petitioner's position is, that the recessed embodiment and non-recessed embodiment of Saxler, can be combined into modified Figure 1A, relying solely on ¶52. EX2004, 38:12-25, 39:1-5. Dr. Shealy is of the opinion that paragraph [0052] of Saxler allows you to "take all the embodiments and bring in which ones you want, depending on what you're trying to accomplish." EX2004, 39:3-5. However, Saxler itself does not provide any indication that Saxler is "trying to accomplish" an enhancement mode transistor. Rather, it is only Petitioner trying to "mix and match" the features of Saxler "trying to accomplish"

an enhancement mode transistor.

95. Petitioner's reliance on paragraph [0052] as a substitute for motivation to combine is misplaced. Paragraph [0052] is nothing more than attorney legalese. Paragraph [0052] states:

96. Exemplary devices according to some embodiments of the present invention are schematically illustrated in FIGS. 1A through 6. Thus, while embodiments of the present invention are described herein with reference to a recessed gate structure or a non-recessed gate structure, other embodiments of the present invention may include or not include a gate recess. Accordingly, embodiments of the present invention should not be construed as limited to the particular exemplary embodiments described herein but may include any suitable structure having a cap layer and/or passivation layer as described herein.

97. Paragraph [0052] does NOT state that the features of the recessed and non-recessed gate structure can be combined, but that only states that "other embodiments of the present invention may include or not include a gate recess."

98. Indeed, as explained above, the features and parameters of the recessed and non-recessed embodiments are vastly different and, absent hindsight of claim 1, cannot be combined to produce an operative transistor without substantial modification.

99. When asked about his interpretation of ¶[0052], Dr. Shealy could only provide one specific example that he would consider patentable in view of Saxler - a microwave gate - because "you're not going to load a microwave gate with this cap layer. It will introduce too many parasitics." EX2004, 43:22-24. Dr. Shealy's position is that ¶[0052] permits virtually any modification of Saxler (except a microwave gate), with no motivation needed, and without consideration of operativeness.

100. Saxler discloses two distinct embodiments, with the recessed embodiment having

a substantially large range of parameters. If it was held that a POSA could freely "mix and match" the features and parameters of Saxler "depending on what you're trying to accomplish" based on a generic catch-all paragraph of ¶[0052], presumably many granted and pending (enhancement and depletion mode) patents on unrelated transistors would be rendered invalid.

101. ¶52 of Saxler is nothing more than a "catch-all" paragraph written by a patent attorney, commonly used in many patent applications, from my understanding. ¶52 of Saxler does not provide support to POSA to modify ("mix and match") the transistors of Saxler to produce the particular structure as claimed.

102. Here, Petitioner appears to be relying on the undisclosed "other embodiments" mentioned in ¶52 of Saxler that "may include or not include a gate recess" to somehow support the specific combination of features that Petitioner is attempting to assemble in order to arrive at the claimed invention through hindsight reconstruction. Although ¶[0052] of Saxler says "embodiments of the present invention should not be construed as limited to the particular exemplary embodiments," it is only reasonable to consider that the disclosure of Saxler must be "limited" to what is actually disclosed. Importantly, ¶[0052] of Saxler does not mention anything about **combining** features of the recessed and the non-recessed embodiments. Even if there was such a mention in Saxler, the technical disclosure of Saxler would not provide sufficient guidance to POSA to produce the claimed structure.

103. Petitioner further cites ¶66 of Saxler that actually cuts against the Petitioner's position in disclosing that "the gate contact may be a 'T' gate as illustrated in FIG. 1A and may be fabricated using conventional fabrication techniques. The gate contact 32 may also be formed on the cap layer 24' as illustrated in FIG. 1B and may be fabricated using conventional fabrication techniques." These two sentences just briefly and distinctly describe the two embodiments, as

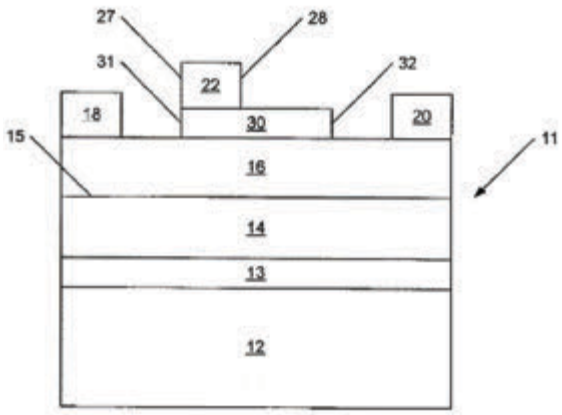
illustrated in each of FIG. 1A and 1B. The two sentences clearly indicate that they cannot be read together to describe a combined embodiment because each sentence concludes in that the respective cap layer embodiment "may be fabricated using conventional fabrication techniques."

104. Dr. Shealy's rationale of "take all the embodiments and bring in which ones you want, depending on what you're trying to accomplish" EX2004, 38:3-5) perfectly reveals Petitioner's intention and hindsight -- Petitioner is trying to reengineer the recessed embodiment of Saxler to "accomplish" the claimed invention.

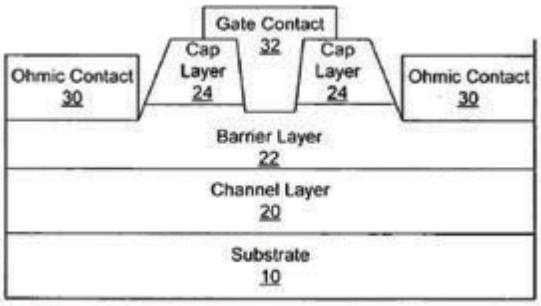
105. More specifically, Petitioner starts their analysis with the recessed embodiment of Fig. 1A but removes the recess to arrive at their hypothetical non-recessed modified Fig. 1A gate structure. However, Saxler discloses a non-recessed embodiment. EX1007 Fig. 1B. As discussed above, Saxler's recessed and non-recessed embodiments each have specific and different parameters. EX1007 Figs. 1A-B, ¶¶12, 13, 14, 70, 71, 27, 81. Petitioner provides no reason for starting with the non-recessed embodiment of Saxler if the goal is to achieve a non-recessed transistor. Clearly, the only reason is hindsight reconstruction of the claimed invention.

106. Smith and Sheppard are consistent with the structural distinctions between Saxler's recessed and non-recessed embodiments

107. The structural and functional distinctions between the non-recessed embodiment and the recessed embodiment are even further evident when considering Smith and Sheppard, both of which are relied on by Petitioner and incorporated by reference in Saxler. Pet.('347) 26, 32.



EX1015 (Smith), Fig. 3



EX1021 (Sheppard), Fig. 1F

108. Smith teaches a non-recessed gate electrode 22 and a "thin" GaN-based cap segment 30 referring to FIG. 3, similar to the non-recessed embodiment of Saxler. EX1015 ¶33. More specifically, Smith teaches that the cap segment 30 is "preferably between about 10-60 Å in thickness." Id. Consistent with the non-recessed embodiment of Saxler, Smith teaches away from the "surfaces extending horizontally" as claimed, disclosing "preferably, the source-side sidewall 31 of the cap segment 30 is substantially aligned to the source-side sidewall 27 of the gate electrode 26."

109. In another embodiment, Sheppard teaches a gate contact (32) recessed through "a relatively thick cap layer 24" (similar to the recessed embodiment of Saxler), where "typically, the cap layer 24 may have a thickness of from about 2 nm to about 500 nm. For example, a cap layer 24 of SiN and GaN may have a thickness of about 300 nm." EX1021 ¶¶42-43.

110. Thus, there are clear structural distinctions between the "thin" cap segment 30 of Smith having a *non-recessed* gate electrode 22 and "aligned" sidewalls, and the "relatively thick" cap layer 24 of Sheppard having a *recessed* gate 32, as similarly discussed by Saxler as discussed above.

111. Petitioner applies circular logic in addressing Smith. Pet.('347) 26-27. Petitioner cites Smith to generally allege that "Smith discloses non-recessed gate electrodes in stacked

structures similar to Saxler's recessed stacked gate structure. Smith, [0033], [0041], Figs. 3, 5B." Pet.('347) 27. However, Petitioner does not explain how the stacked structures of the non-recessed gate electrodes of Smith are "similar" to Saxler's recessed embodiment. Indeed, Petitioner alleges that Smith teaches away from the gate recess of the recessed embodiment (Fig. 1A), asserting that "Smith states that 'there is no benefit to recessing the gate down to the barrier layer' in GaN HEMT devices 'because the top surface of GaN is generally not conductive.' Id., [0010]."

112. Thus, Petitioner modifies the recessed embodiment of Saxler based on the non-recessed structure of Smith because Smith is "similar", while, at the same time, Petitioner acknowledges that Smith teaches away from the recessed gate structure of that embodiment. EX1015 ¶10 ("no benefit to recessing the gate down to the barrier layer"). This modification by Petitioner is nothing but an attempt to arrive at the non-recessed structure of Smith, but with the sloped sidewalls of the recessed embodiment of Saxler. The non-recessed structure of Smith is clearly structurally more closely analogous to the non-recessed embodiment of Saxler. As discussed above, Saxler, Smith, and Sheppard provide clear structural and functional differences between recessed gate structures and the non-recessed recessed gate structures.

C. Petitioner's modification of Saxler does not result in a method for manufacturing an operational enhancement-mode transistor

113. In analyzing the IPRs, I was informed by EPC Counsel that I can assume that the preambles of each of the claims are limiting, in that Petitioner needs to prove that the prior art discloses or renders obvious an enhancement-mode transistor.

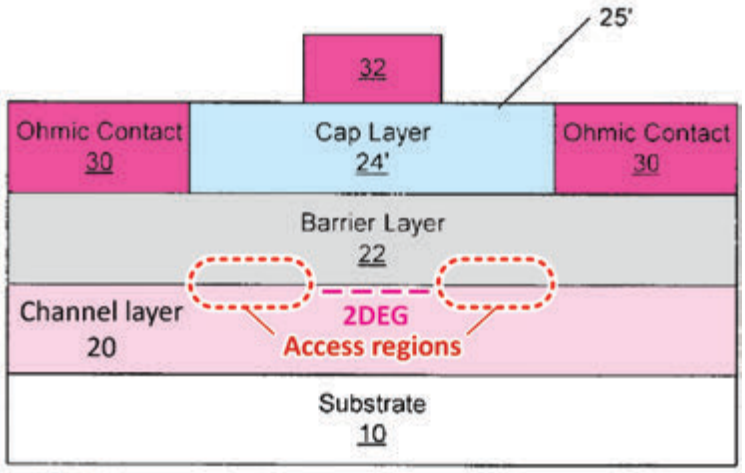
114. As further discussed in §VII.A above, Saxler discloses depletion mode transistors only, and not enhancement mode transistors. EX1003 ¶099 ("Saxler does not use the phrase 'enhancement mode'").

115. I agree with Petitioner that the transistor of the recessed embodiment of Fig. 1A is

not enhancement mode due to the recessed gate structure Pet.('347)55-56; EX1003 ¶146 ("with the recess, Saxler's device is not enhancement mode (always off)"); EX2004, 59:5-10 ("as it's drawn, it would be a depletion mode device.")

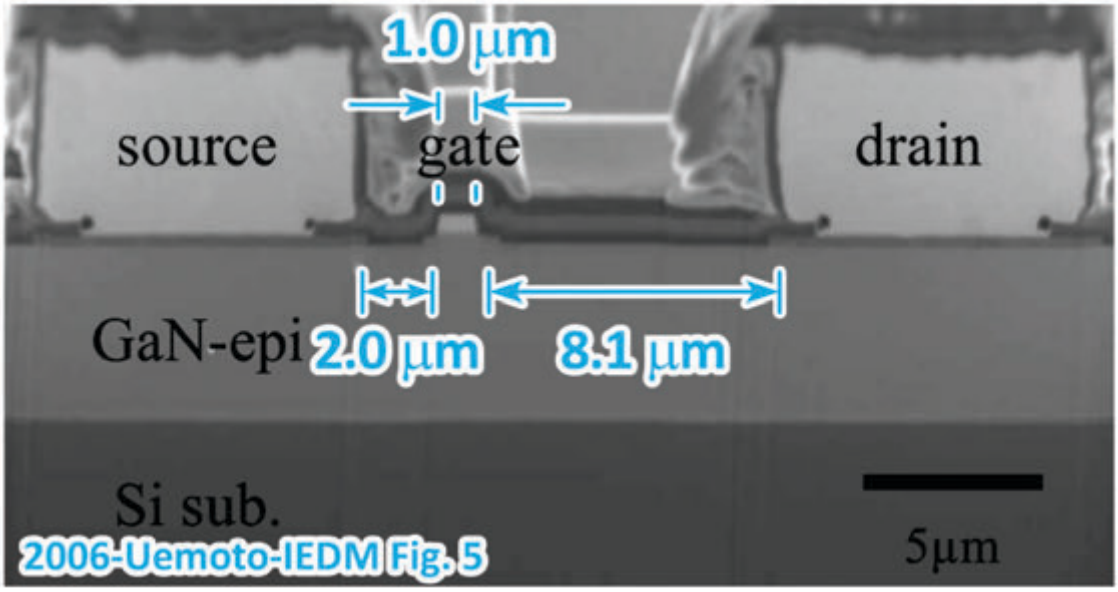
116. I also agree with Petitioner that the non-recessed transistor is not a functional enhancement mode transistor because the cap layer 24' extends from ohmic contact 30 to ohmic contact 30. EX2004, 52:13-19 ("1B is a strange cartoon… I've never seen a device built that way, where the sides of the Ohmics are able to butt up against the cap layer -- you're not going to be able to fabricate that."); 65:16-18 ("that structure, as shown, would have these shunt problems I was talking about, potentially.")

117. As acknowledged by Dr. Shealy, Saxler's cap layer 34 in Fig. 1B reaches all the way from S to D (source to drain), including the access regions that are located between the S & G (source and gate) electrodes, as well as between the G & D (gate & drain) electrodes.



118. When a voltage is applied to the gate electrode, a 2DEG is induced substantially below the gate electrode but, importantly, not under the entirety of the cap layer 24 of Saxler (that is, not all the way from S to D). As a result, Dr. Shealy's proposed E-mode transistor (which Saxler never discloses) could not be switched ON.

119. For example, looking at the SEM image of Uemoto (EX1020) for exemplary dimensions, the G length of the transistor is about 1.0 μm, the S-to-G distance is 2.0 μm, and the G-to-D distance is about 8.1 μm.

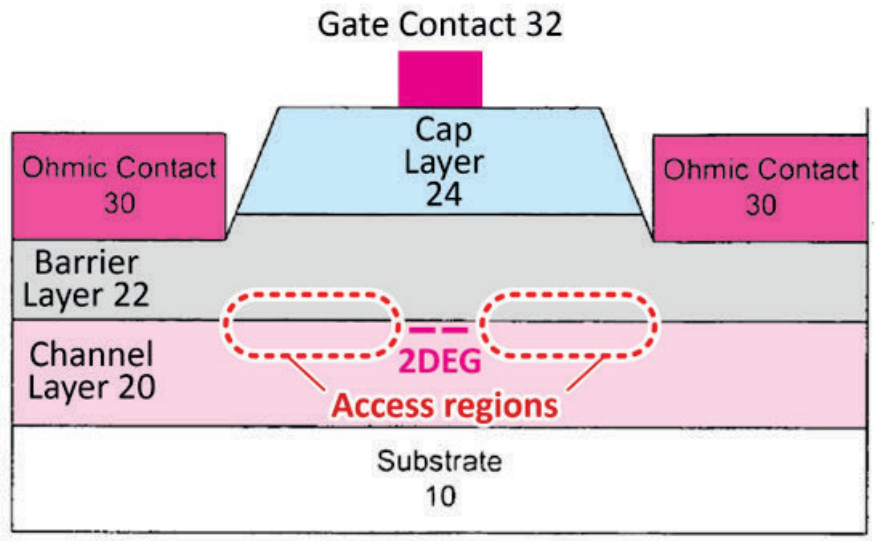


120. EX1020, Fig. 5 (annotated)

121. Any contention that a 1.0 μm gate could induce a 10 μm long 2DEG channel contradicts the principles of elementary electrostatics. The distance between an inducing charge and an induced charge is minimized because opposite charges attract each other. Proposing that a charge would induce an opposite charge at a remote location violates the principle of energy minimization. Nature always strives to minimize energy, in the present case, the electric field energy. This is accomplished by the distance between inducing charge and induced charge being minimized. The minimization of electric field energy is the foundation for the well-known fact that positive charges and negative charges attract each other.

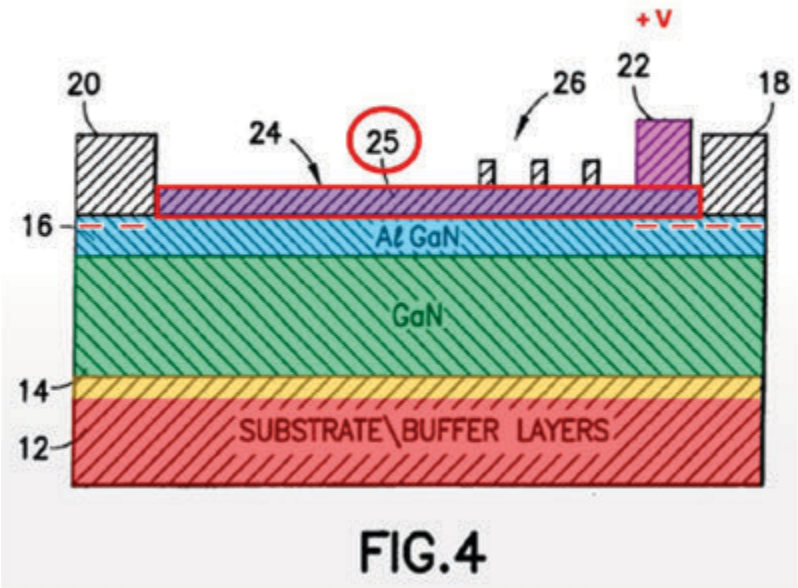
122. Even Petitioner's hypothetical transistor cannot be a functional enhancement mode transistor based at least on the geometry of the cap layer, which extends substantially or entirely all the way from source to drain (and including the access regions). The geometry of the cap layer

24 prevents the transistor of Saxler from operating in enhancement mode because the access regions would remain depleted of free electrons (and thus the access regions are electrically resistive), even for a positive gate voltage, thereby making it impossible to switch the transistor to its ON state. Without application of voltage to an overlying gate, the 2DEG cannot in substantially the entire access regions extending from ohmic contact 30 to ohmic contact 30 because the access regions would remain depleted.



123. Petitioner confirmed this operation in an ITC proceeding between the parties. There, for a transistor that has a GaN layer that extends from source to drain, Petitioner agreed that the 2DEG is not reconstituted between the source and the drain when a positive voltage—necessary for enhancement-mode operation—is applied to the gate. EX2008 at 938:1-10. When such a positive voltage (+v) is applied, as shown below, the 2DEG (represented as red dash "–") is *only* reconstituted substantially under the gate, which is insufficient to turn the device ON because the 2DEG is not continuous between the source and drain contacts. *Id.* Petitioner's expert in the ITC proceeding admitted as much during his redirect examination at trial, referring to the image below, noting that "…you can establish a 2DEG with a positive voltage on an enhancement-

mode, and the question here is, is that the 2DEG doesn't – **it's not continuous all the way from the source to the drain**…" *Id*. at 938:5-10 (emphasis added). *See also* EX209 at 41.



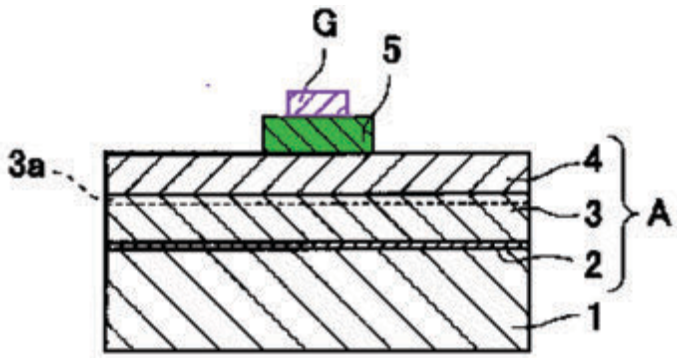
EX2009 at 41

124. Even assuming that Dr. Shealy is correct that it would be possible to apply a sufficiently high voltage to replenish the electrons in the access regions, a POSA would not produce an enhancement mode circuit in this manner.

125. Cap layers in depletion mode transistors can extend substantially the entire length between the ohmic contacts because the transistor is normally ON and the cap layer only needs to pinch off the current by depleting the 2DEG under the gate to turn the transistor OFF. On the other hand, enhancement mode transistors are normally OFF, and the situation is reversed, and the 2DEG must be replenished under the p-type gate material.

126. Dr. Shealy's theory that a sufficiently high voltage could replenish electrons in the 2DEG from source to drain is not practical. As disclosed, for example, in Yoshida, enhancement mode transistors are designed to provide voltage control with a small amount of carrier injection. EX1006 ¶17. This is produced in Yoshida by "etch[ing] away the p-type GaN layer except where

the gate electrode was to be loaded and exposing the n-type InGaN layer 4." [0022]. Thus, a POSA would understand that the cap layer is designed in an enhancement-mode transistors such that only a small portion of the 2DEG needs to be replenished to turn it ON.



EX1006, Fig. 1

127. Indeed, Petitioner's expert from the ITC proceeding admitted that he has no quantitative basis for his theory that a sufficiently high voltage could replenish electrons in the 2DEG; he conceded that he has neither modeled nor simulated any part of this theory. Ex. 2008 at 938:19-939:8. The expert's vague instructions to a POSA are, thus, to "play with" various aspects, with the understanding that even if such a device were to exist (and it does not), it would have "lots of leakage" due to the massive amount of voltage passing through the gate. *Id*. at 939:5-8. That is precisely why a POSA would not have been motivated to apply such a high voltage.

128. Thus, a POSA would have no reason to convert the depletion mode transistor of Saxler, having the cap layer 24 extending entirely or substantially entirely between the ohmic contacts, to an enhancement mode transistor. The modification proposed by Petitioner, even if possible, would require excessive voltage to be applied to turn the transistor ON (assuming that it would even turn ON), undesirable for enhancement mode transistors. EX1006 ¶17. The modification would also improperly change the principle operation of Saxler, in being a depletion-mode transistor. Paragraph [0049] explains the purpose of p-type doping of region 40 at the top

of the cap layer: "the dopants at the outer surface of the device may segregate to dislocations in the cap layer and, thereby, reduce gate leakage along the dislocations." Id. ¶[0049] Indeed, Saxler points out that the dopants "segregate to dislocations" rather than depleting the 2DEG. Id. Paragraph [0049] further explains that "a shallow dopant in the bulk crystal may have characteristics of a deep level when at a dislocation" which is "especially true in the case of p-type [...] dopants." Id. Thus, the shallow acceptors of Saxler do not even act as acceptors once they "segregate to dislocations." If the shallow dopants do not act as acceptors, the cap layer cannot function in enhancement mode. That is, the dopants that Dr. Shealy envisions as regular, shallow p-type dopants, are in fact characteristics of "deep level" dopants. This fact would be perceived as problematic and de-motivating by a POSA, because, contrary to Dr. Shealy's assertions, "deep levels" are generally not suitable to deplete a 2DEG. As a result, a POSA would be discouraged taking the path Dr. Shealy envisions.

D. Petitioner makes many vague, unsupported statements and premises with reference to Saxler

129. Contrary to Petitioner's assumption, Saxler does not disclose "precise" and central alignment of the gate electrode on the cap layer, and actually explicitly discloses that the gate electrode is to be "offset"

130. Petitioner bases ground 1 on reverse engineering the hypothetical transistor derived from Fig. 1A of Saxler in proposing "a known, obvious way to create that structure." Pet.('347) 35.

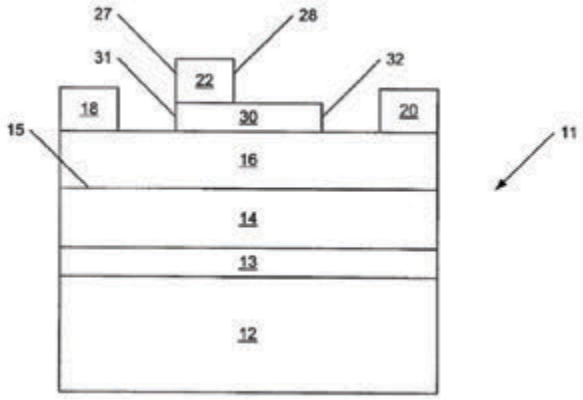
131. Petitioner further alleges that "although not explicitly disclosed, a POSITA would have understood that Saxler uses a photomask to etch the gate because Saxler requires precise positioning achievable using this conventional approach." Pet.('347) 24.

132. However, Petitioner does not provide any support for the statement that "Saxler

requires precise positioning" nor that Saxler discloses any centrally aligned gate structure. Petitioner seems to primary rely on the schematics of Figs. 1A, B to allege that "precise positioning" is required. However, a POSA would not rely on dimensions from schematics as illustrated in Fig. 1A for reverse engineering.

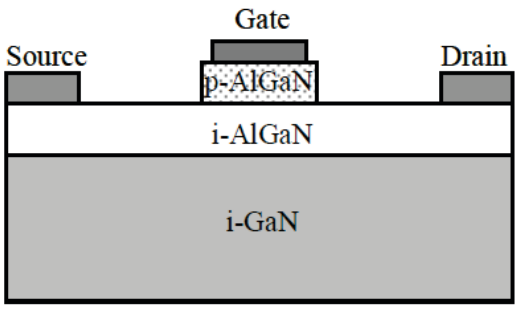
133. Saxler explicitly discloses that "the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device and are not intended to limit the scope of the present invention." EX1007 ¶42. Thus, Saxler explicitly states that the drawings cannot be relied on for exact dimensions or direct alignment in that "the precise shape of a region" (positioning) is not required. Indeed, Petitioner and Dr. Shealy repeatedly discredit the drawings of Saxler in citing a "principle" that the transistor schematics are not illustrative of the device. Pet.('347) 90-91; EX2004, 53:13, 53:16-25, 56:24-57:1, 60:17-18, 82:16-19.

134. The only disclosure of the relative position of the gate electrode on the cap layer is that "in particular embodiments where the ohmic contacts 30 provide source and drain contacts (as in the present invention), the recess may be offset… closer to the source contact than the drain contact" (EX1007 ¶65) which is consistent with the disclosure of Smith as incorporated (EX1007 ¶42, EX1015 ¶¶41-42).



EX1015, Fig. 3

135. Furthermore, Petitioner later relies on Uemoto which illustrates a similar schematic of a centrally aligned gate with an actual SEM image showing the gate with an "offset" gate electrode "closer to the source contact than the drain contact." Pet.('347) 90-92; EX1020, Figs. 1, 5; EX2004, 94:21-22 (Dr. Shealy acknowledging that the structure of Uemoto does not have substantially equal ledges).



EX1020, Fig. 1

Pet.('347) 92 (EX1020, Fig. 5 modified)

136. Thus, Petitioner does not provide any support for the statement that "Saxler requires precise positioning" nor that Saxler discloses any centrally aligned gate structure.

137. Furthermore, Saxler does not provide any disclosure or suggestion of etching the gate electrode and cap layer with a single photoresist

138. In addressing [1g]: Petitioner alleges "Saxler also discloses or at least renders obvious etching the gate metal using the same photoresist." Pet.('347) 43. This statement is directly negated by Dr. Shealy's in the deposition. More specifically, Dr. Shealy admits that Saxler does not disclose "using the same mask." EX2004, 55:1-7 ("we bring in the self-aligned with other references: Beach and Ahn").

139. In addressing [1i], Petitioner alleges that "Lidow, the prior application, notes this approach was conventional, stating that ledges in a 'conventional enhancement-mode transistor' are made using separate masks for the p-type gate material and gate metal. Lidow, [0006], Fig. 1;

Shealy, [124]." Pet.('347) 47. However, the use of separate masks as allegedly disclosed in Lidow does not provide any support for "etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal" as claimed [1i].

140. In addressing [1i]: etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal, Petitioner alleges that "Saxler renders obvious making these ledges by etching the gate metal. Shealy, [126]." Pet.('347) 48. However, ¶126 of Dr. Shealy's Deposition does not provide any additional explanation or underlying reasoning for this conclusory statement in addressing [1i]. Furthermore, Dr. Shealy again admits that Saxler does not disclose self-alignment. EX2004, 55:1-7 ("we bring in the self-aligned with other references: Beach and Ahn").

141. Petitioner appears to understand the weakness of this vague Saxler alone obviousness interpretation. Thus, Petitioner explicitly relies on Beach and Shenoy for Ground 1.

E. A POSA would not modify Saxler with the "self-aligned" technique of Beach

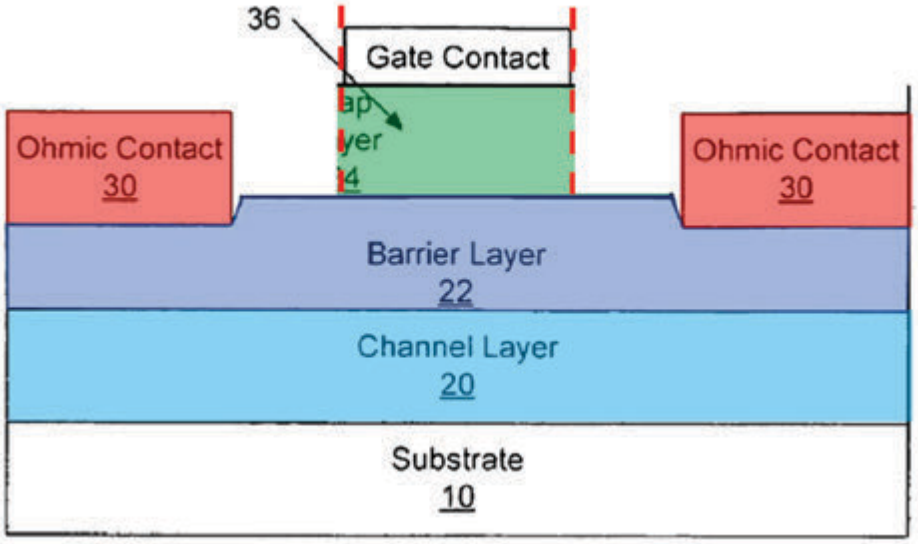
142. The "self-aligned" technique of Beach would not produce the sloped sidewalls of Saxler, as relied on by Petitioner

143. Petitioner alleges that "it would have been obvious to modify Saxler with Beach's self-aligned technique." Pet.('347) 32. Petitioner further alleges "Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet.('347) 35.

144. The basic premise of Petitioner is that Saxler requires "precise" and direct alignment of the gate electrode on the center axis of the cap layer, solely based on Figs. 1A, 1B. However, Saxler directly contradicts this assumption. Saxler does not disclose any centrally aligned structures but rather discloses the gate contact being "offset… closer to the source contact

than the drain contact," directly contradicting the "precise" central alignment assumption taken by Petitioner in applying Beach. EX1007 ¶¶42, 65.

145. Furthermore, as acknowledged by Dr. Shealy, applying Beach's self-aligned technique would either cut off or not form the horizontally extending "sloped" side surfaces that Petitioner relies on from Fig. 1A of Saxler and in the hypothetical transistor, as illustrated below.



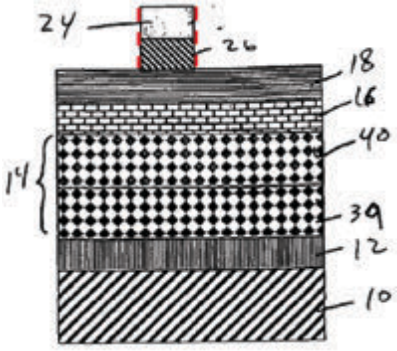
Pet.('347) 45 (showing etching from Beach)

146. I do not agree with Petitioner's drawing for the following reason. To the extent the Beach gate fabrication process is used on a transistor structure having ledges and slanted sidewalls, the Beach process does not preserve but removes these ledges and slanted sidewalls. Indeed, Dr. Shealy explained "what Beach figure shows is a -- you know, it's drawn as a vertical wall. It's an idealized drawing, of course. Well, one would expect it to have some curvature." EX2004, 87:15-19. Thus, Dr. Shealy directly undercuts Petitioner's assertion that "Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet.('347) 35. Applying the Beach self-aligned technique to Saxler would not produce the sloped sidewalls as illustrated in Saxler but would instead produce

intentionally vertical sidewalls with potentially "some curvature."

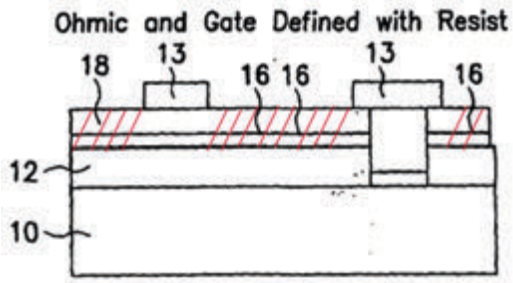
147. I note that Petitioner relies on the sloped walls as exactly illustrated in Fig. 1A because it is "a fair representation of what Saxler is trying to achieve" except for the vertical scale showing detail of the epitaxial layer. EX2004, 56:21-25. Furthermore, Petitioner specifically relies on those sloped walls for dimensions. Pet.('347) 46, 67. Thus, modifying Saxler with the self-aligned technique of Beach would not result in the "sloped sidewalls" of Saxler as illustrated in Fig. 1A and relied on by Petitioner.

148. *Beach* defines the "self-aligned gate arrangement" based on "gate arrangement 24 over gate barrier 26, as illustrated in FIG. 2F." FIG. 2F illustrates the stacked gate arrangement as having vertically aligned sidewalls. *Beach* does not provide any indication of the stack of the gate arrangement 24 and gate barrier 26 being formed in any other way, including "*side surfaces… that extend horizontally*" as claimed.

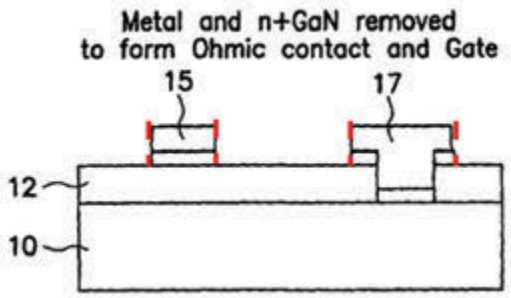


EX1008, Fig. 2F (annotated)

149. This is consistent with Beach-II (as also relied on, Pet.('347) 29, 42, 43) that discloses "**after material 18 has been removed from device 14 in regions <u>not covered by photoresist 13</u>**, photoresist 13 is stripped off and the resultant structure is subjected to a low temperature anneal step." ¶49.

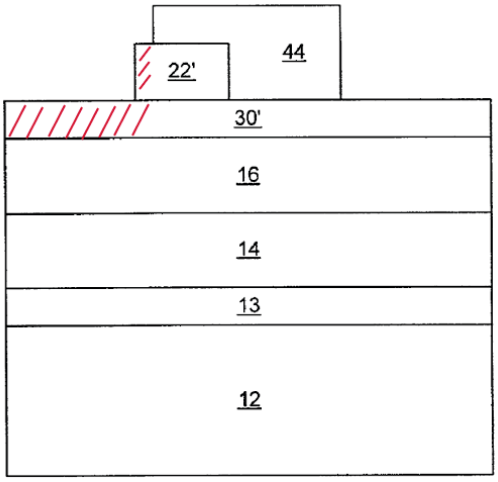


EX1027, Fig. 1D (annotated)

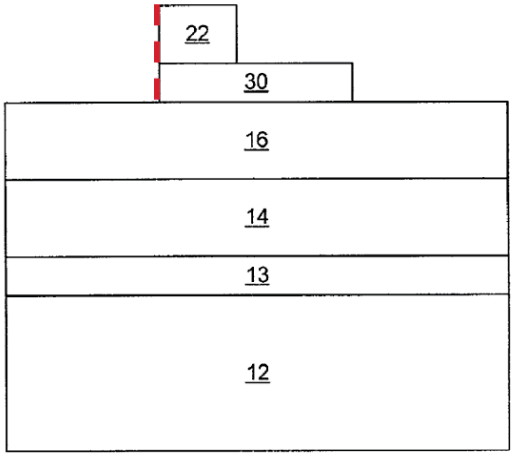


EX1027, Fig. 1E (annotated)

150. This is further consistent with Smith (incorporated by Saxler and also relied on by the Petitioner, Pet.('347) 43) that discloses "an etch mask 44 is deposited on the GaN cap layer 30′ which partially overlaps the gate metal 22′ so as to define the source-side sidewall of the gate electrode 22 and the GaN cap segment 30 and the drain-side sidewall of the GaN cap segment 30.As illustrated in FIG. 6B, **the exposed portion of the GaN cap layer 30′ is etched away, leaving <u>one sidewall of the GaN cap segment 30 self-aligned with a sidewall of gate electrode 22</u>** and to expose portions of the AlGaN barrier layer 16."

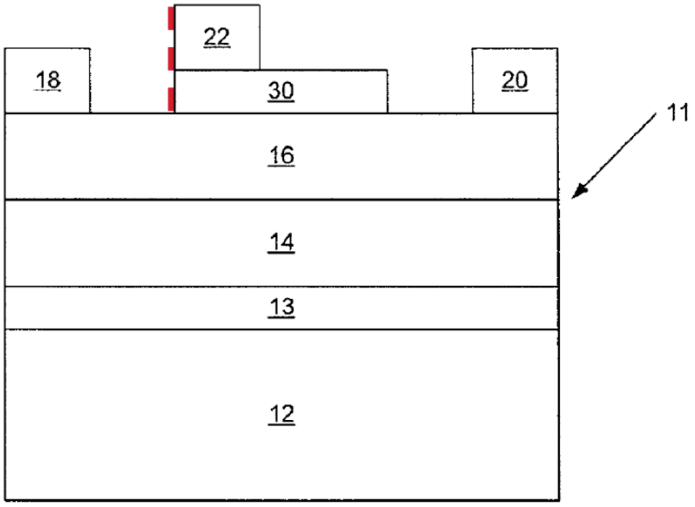


EX1015, Fig. 6A (annotated)



EX1015, Fig. 6B (annotated)

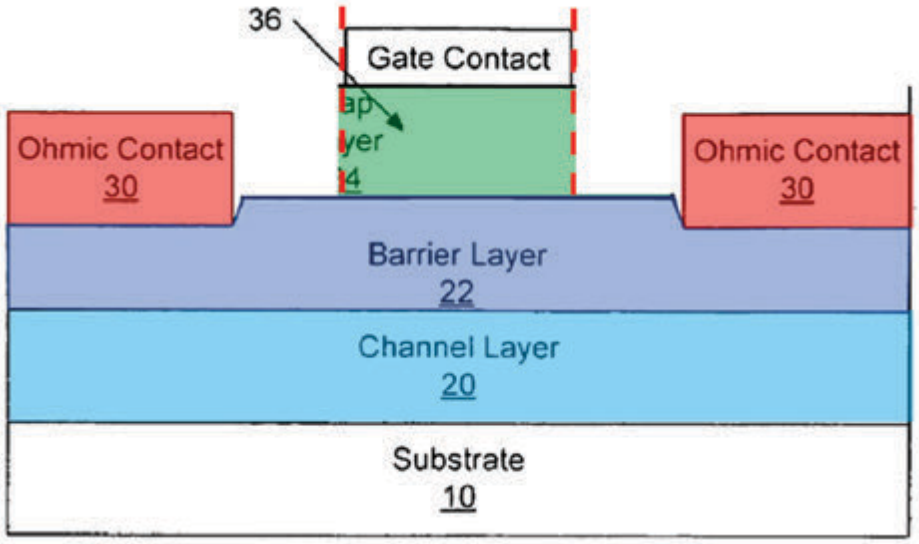
151. Indeed, *Smith* explicitly teaches away from sloped side walls in that "it is preferable to have the cap segment 30 be spaced apart from the source electrode 18 as small a distance as is reasonable in light of manufacturing limitations." EX1015 ¶36.



EX1015, Fig. 4C

152. Thus, *Smith* as incorporated by *Saxler* and relied on by Petitioner belies Petitioner's assertion that it would have been obvious to modify the non-recessed embodiment of *Saxler* with the "tapered" horizontal walls of the recessed embodiment. Indeed, the teaching in *Smith* of placing "the cap segment 30 [] spaced apart from the source electrode 18 as small a distance as is reasonable in light of manufacturing limitations" would likely exclude the allegedly intentionally formed tapered sidewalls in the recessed embodiment of Saxler.

153. In sum, the "self-align" technique of *Beach* (which is consistent with Beach-II (EX1027) and Smith (EX1015) as also cited) is directed to **self-aligning <u>sidewalls</u>** of two layer components by forming vertical sidewalls vertically aligned. Even assuming that one of ordinary skill in the art would be able to etch the "*ledges*" as further claimed, the "self-alignment" technique of *Beach* would not form "side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively" based on Petitioner's interpretation. Thus, "modify[ing] Saxler with Beach's self-aligned technique" as alleged by Petitioner would at least substantially etch or not form the "tapered sidewalls" as relied on in Saxler (Pet.('347) 35), as annotated in red broken lines below. There is no suggestion in the cited references otherwise.



Pet.('347) 45 (showing etching from Beach)

154. I do not agree with Petitioner's drawing for the following reason: To the extent the Beach gate fabrication process is used on a transistor structure having ledges and slanted sidewalls, the Beach process does not preserve but removes these ledges and slanted sidewalls. Petitioner does not produce any teaching in any of the references of "forming a photoresist over the gate metal; etching the gate metal and the p-type gate material, <u>wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer</u>" as claimed. If anything, the self-aligned techniques of Beach, Beach-II and Smith would intentionally form vertical walls with potentially "some curvature." EX2004, 87:15-19.

155. [Reserved]

156. Furthermore, the etching technique of Beach is incompatible with Saxler. Beach discloses N-polar (nitrogen-polar) technology (¶10), while Saxler discloses Ga-polar (gallium-polar) technology. The two polarities cannot be combined, mixed, or synthesized, because they are mutually exclusive opposites. The Beach etching is specific to N-polar GaN and starts with a

"smart-cut" substrate-removal process which is unsuitable for the Ga-polar structures of Saxler. Due to the N-polar orientation of Beach, a POSA would not have used Beach as guidance to modify the teachings of Saxler. Further, the devices described in each reference are substantially different, and the teachings of Beach would not have been incorporated by a POSA into the structure and method of manufacture described in Saxler.

F. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner's reasoning

157. Petitioner alleges that "it would have been obvious to combine Saxler with Beach and Shenoy's techniques of masking and etching the gate metal and p-type gate material using a single photomask when making Saxler's non-recessed GaN HEMT device." Pet.('347) 43-44.

158. Shenoy involves electrochemical etching – etching with an applied voltage, an applied electric field, and an electrical current flowing. However, because the method of Shenoy is performed under very controlled conditions, a POSA would not have considered Shenoy to modify the teachings of Saxler as modified by Beach. Shenoy describes electrochemical etching, a highly specialized etching method with little relevance to the process described in either the '347 Patent or Saxler. Indeed, electrochemical etching can only be used in conjunction with conductive materials and insulator materials, and therefore would not have been considered based on the KOH etching described in Saxler.

159. More specifically, the process of Shenoy in forming the undercut U on the metal film is explicitly dependent on the positioning of the metal film <u>on an underlying insulator</u> and <u>in isolation of other components that could be etched</u>. Indeed, Shenoy explicitly discloses "EMM of metal films <u>supported by insulating substrates</u> involve single-sided through-mask metal removal. The isotropic nature of the metal removal process leads to undercutting of the mask." EX1009, 1.

160. As further discussed in the "Model Development", Shenoy discloses "the

parameters that characterize the shape evolution during through-mask EMM are (Fig. 1): (i) aspect ratio, h/L, (ii) spacing to opening ratio, α/L, (iii) metal film thickness ratio, b/L, and (iv) mask wall angle, β. The aspect ratio, spacing to opening ratio, and the mask wall angle influence the current distribution at the electrode. On the other hand, the metal film thickness ratio determines **the extent to which EMM must proceed before the underlying insulator is exposed**. The influence of these parameters on the undercut, U, and the etch factor are of interest. The etch factor is defined as the ratio of the maximum etched depth to the undercut, (d/U). **Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal wall angle, χ**." EX1009, 1.

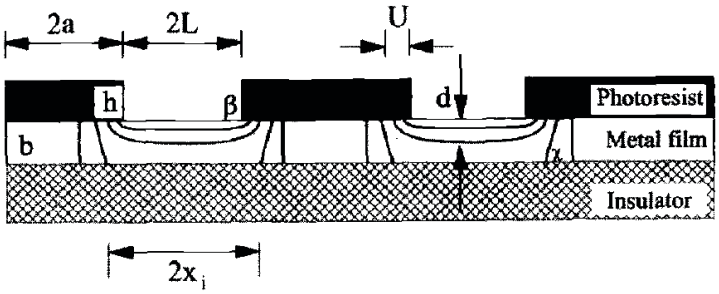
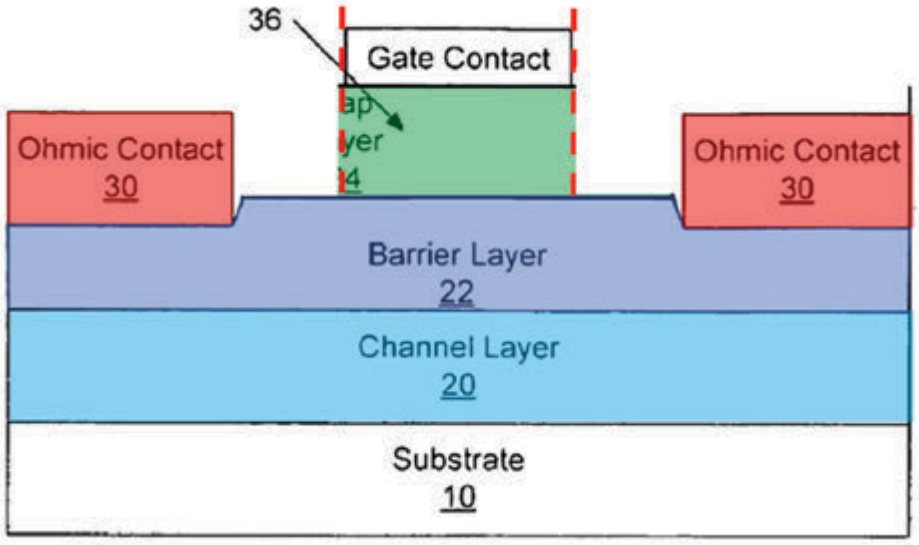


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

161. The basic science is that electric field lines generally terminate at electrical terminals. In Shenoy, the metal layer is provided with a certain electrical potential and the electric field lines terminate at the metal surface. Electrical current flows, and the etching process occurs, at the metal surface. The electrochemical etching process occurs where the field lines terminate and where the current flows. Below Shenoy's metal layer is an insulator and no electrical current flows into the insulating layer (the insulating layer has no net charge, is overall neutral, and has no electrical potential applied to it). Thus, the electric field lines would then spread laterally after reaching the insulator.

162. A POSA would not have modified the method of Saxler as modified by Beach further based on Shenoy because the cap layer (24) and gate contact (32) of Saxler would already be in place on the transistor and etched by the technique of Beach to expose the sidewalls of the gate contact (32).



Pet.('347) 45 (showing etching from Beach)

163. The cap layer (24) of Saxler does not function as an insulator as intended by Petitioner and required by the process of Shenoy.

164. At his deposition, Dr. Shealy alleged "gallium nitride is a pretty tough material to etch, and a lot of these etches will not etch it. So that – that's again like Shenoy: The insulator is not being etched in Shenoy." EX2004, 99:18-19.

165. However, as Dr. Shealy apparently recognizes, gallium nitride is not an insulator. There is a clear distinction between "a pretty tough material" and an insulator as required by Shenoy. Shenoy specifically models the etching based on current distribution and not "tough[ness]." Furthermore, Dr. Shealy is referring to "liquid metal etches" when mentioning "a lot of these etches" (EX2004, 97:11-13, 9:14-17), which are not cited in the petition and thus have

no bearing to the present claims.

166. Shenoy specifically states that "Faraday's law has been used to determine the rate at which the anode surface recedes [is etched away]… The current distribution has been obtained by solving the distribution of the electric potential in the electrolyte as governed by Laplace's equation." EX1009, 3. I note that "Faraday's law" and "Laplace's equation" equally apply to metals as well as semiconductors, thereby elucidating that the metal as well as the semiconductor is being etched away when Shenoy is applied to the transistor of Saxler.

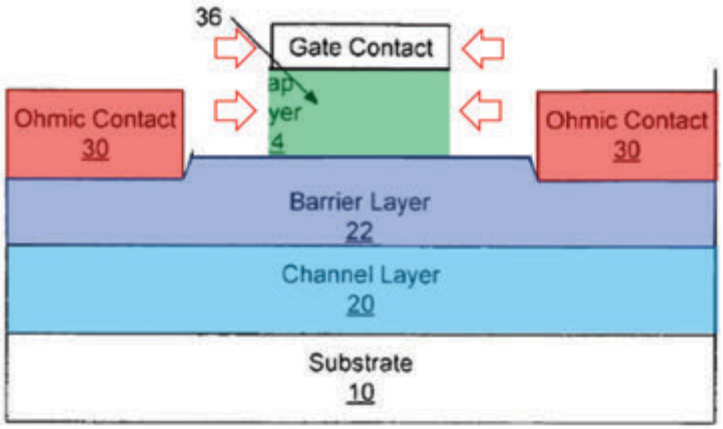
167. Shenoy specifically models the etching based on equation 5, as reproduced below.

> The current distribution at the anode has been combined with Faraday's law to determine the evolution of the metal surface. The rate, r, at which the anodic surface recedes is
>
> $$r = \frac{M\theta}{nF\rho} i \qquad [5]$$
>
> where M is the molecular weight of the metal, n is the metal dissolution valence, ρ is the density of the metal film, F is Faraday's constant, and θ is the current efficiency of metal dissolution which is assumed to be constant at 100%.

EX1009, 3

168. In applying equation 5, the current distribution i would be zero for insulators (such as SiO2), thereby showing that no etching would occur in the insulator (SiO2) underlying Shenoy's metal layer, consistent with Shenoy's proposed results. However, a current distribution would occur in the gallium nitride because it is not an insulator, thus etching would occur contrary to Petitioner's proposed modification. Indeed, Electrochemical etching is a common etching technique for GaN, demonstrating that GaN is being etched by the etching technique. In contrast, electrochemical etching cannot be used for SiO2 because it is an insulator. Accordingly, the etching process of the Shenoy will etch both, the gate metal as well as the p-type GaN.

169. In further addressing GaN, Dr. Shealy alleges that "this is a p-type semiconductor dope of magnesium, and it would normally have holes. But because of these side surfaces, the holes are depleted away from the surface where the etching is occurring. And what that means is, is that the semiconductor layer behaves as an insulator just like Shenoy's structure, because there are no mobile charges near the etching region in the semiconductor." EX2004, 99:4-13.



170. I disagree with this statement because neither Saxler nor Beach teach any passivating of the GaN material. The cap layer of Saxler would still be conductive and thus be etched. However, even assuming that this is true, the side surfaces that would be etched by Beach in the proposed modification are not relevant to the method of Shenoy. Rather, the spread or undercutting is induced by an **underlying** insulator. EX1009, 1 ("the extent to which EMM must proceed before the underlying insulator is exposed… Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal wall angle, χ.")

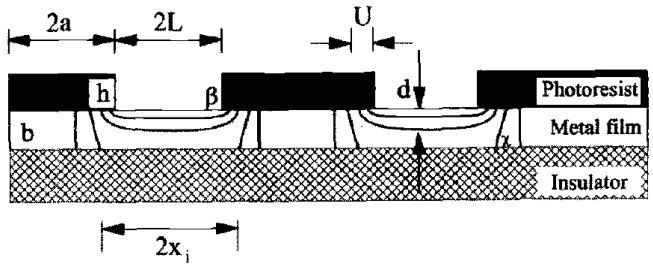
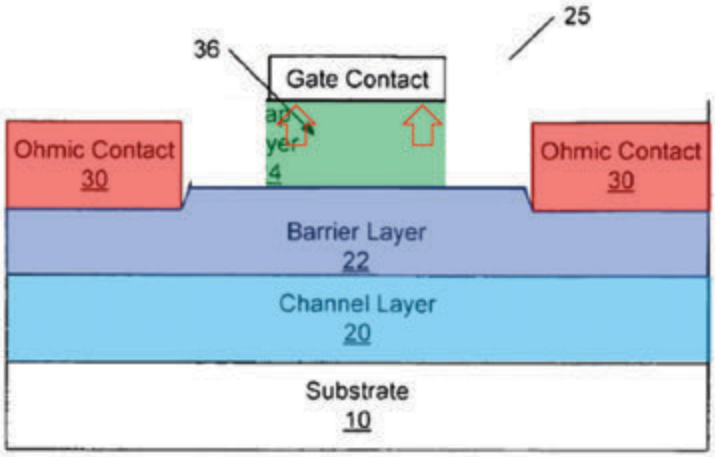


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

171. The etched side surfaces that Dr. Shealy is referring to would not underlie the gate contact. Rather when comparing the mathematical setup of the Shenoy to the transistor of Saxler, the portion of the cap layer 34 underlie the gate contact 32 in Saxler would actually be the surfaces pointed out in red arrows below. These surfaces would not have been etched by the self-aligned process of Beach. Those same surfaces of the cap layer 34 are also relied on by Petitioner for the claimed ledges.



Pet.('347) 45 (annotated)

172. Even assuming Dr. Shealy reasoning (which I disagree with), the surfaces of the cap layer 34 underlying the gate contact would still "have holes" because it would not have been etched (EX2004, 99:4-13) by the Beach process and thus not act as an insulator. Therefore, the underlying surfaces of the cap layer 34 would be etched along with the gate contact in the etching process of Shenoy, thus not be retained as ledges.

173. Therefore, in addition to Beach, the actual teaching of Shenoy undercuts Petitioner's motivation in "Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet.('347) 35. Applying the etching of Shenoy would etch at least the alleged ledges of the cap layer 34 in

Saxler that would underlie the gate contact in Petitioner's proposed method. Thus, applying the method of Shenoy would not produce the hypothetical modified structure of Saxler, as alleged by Petitioner.

174. For at least these reasons, a POSA would not use Shenoy's "mathematical model" and apply it to Saxler. What will happen is unpredictable at best. Shenoy's etching process is not a selective etching with the exclusion of perfect insulators. The POSA would realize that the etching process may proceed downward (rather than sideways). The POSA would have no guidance with respect to the electrochemical etching process. Shenoy is silent on the chemistry employed and Saxler do not employ an electrochemical etching process.

175. Shenoy reports that the etching process is "isotropic." If we trust this disclosure, then the etching process proceeds in all directions at the same rate absent an insulator, and the GaN materials below the metal would be etched as well. So, purely based on Shenoy's "mathematical model" and "isotropic" teachings, the process proposed by Petitioner would not produce the results desired by Petitioner.

G. A POSA would not have found it obvious to combine Saxler, Beach, and Shenoy

176. Petitioner has not articulated a reason for POSA to combine all three references

177. Petitioner does not articulate a reason to combine Saxler, Beach and Shenoy, so Petitioner has left it to Patent Owner and the Board to fill in the gaps between the proposed combinations of Saxler with Beach and Shenoy. Petitioner's failure to explain a reason to combine all three references, including the specific process sequence that allegedly follows from the prior art, undermines Patent Owner's ability to respond to the obviousness contentions.

178. Petitioner fails to provide specifics on how the proposed method would actually be performed. Importantly, Petitioner has not provided a fabrication process sequence, neither in a

narrative, nor in a pictorial manner. I do not know the fabrication process sequence Petitioner is envisioning. Petitioner repeatedly relies on reasoning such as "no more than simple substitution" and "known methods that would be predictably implemented" (Pet.('347) 34), but never provides a specific process sequence. By doing so, Petitioner atempts to avoid the conflicts & incompatibilities that arise from the proposed combinations being addressed.

179. Petitioner mischaracterizes the method of Saxler as being "flexible" in alleging complete freedom to modify Saxler.

180. Petitioner alleges "Sheppard, incorporated to disclose methods of fabricating GaN HEMTs (Saxler, [0046], [0068]), describes a flexible approach to masking and etching. It notes that 'operations described as multiple steps could be combined into a single step' (and vice versa), making the choice of Beach's manufacturing steps no more than simple substitutions. Sheppard, [0058]; Shealy, [095]." Pet.('347) 34.

181. However, "flexibility" is no substitute for motivation. Furthermore, splitting a single described step into multiple steps or combining multiple described steps into a single step as described by Sheppard does not support Petitioner's proposed reinvention of Saxler's process and structure.

182. For example, Saxler does not disclose any "self-aligned" structures, thus there would be no motivation to apply the "self-aligned" technique of Beach. This is further evident from Petitioner's reliance on the "self-aligned" technique of Smith for an intermediate step before applying the Shenoy process. Furthermore, the process of Shenoy cannot be implemented into the process of Saxler as modified by Beach without undue experimentation, as discussed in §VIII.E. Thus, recreating the claimed process by piecing together 1) some steps of Saxler, 2) some steps of Beach, and 3) some steps of Shenoy to arrive at the claimed invention goes far beyond the

"flexible" approach as suggested by Sheppard.

183. Throughout Ground 1, Petitioner seemingly continues to apply Dr. Shealy's "mix and match" rationale to "take all the embodiments and bring in which ones you want, depending on what you're trying to accomplish." However, this rationale actually requires substantial modifications and improper hindsight according to "what you're trying to accomplish."

184. For at least those reasons, *Saxler* in view of *Beach* and *Shenoy* does not render obvious claims 1-3 of the '347 Patent.

IX. Ground 2 (Claims 1-3) of the '347 Patent - Saxler in view of Yoshida, Beach, and Shenoy

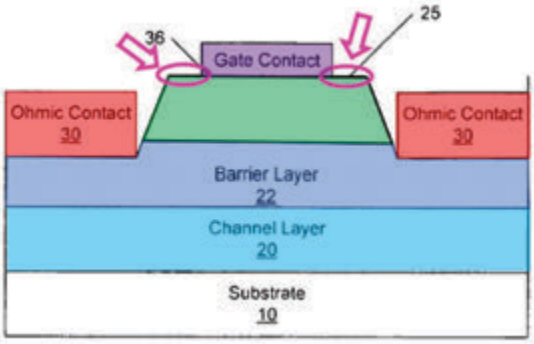
A. Overview

185. In Ground 2, Yoshida is relied upon for its non-recessed gate structure. However, Saxler already discloses a non-recessed embodiment. Petitioner provides no reason why a POSA would be motivated by Yoshida to modify Saxler's recessed embodiment to eliminate the recessed gate contact.

186. Petitioner also applies faulty logic in trying to apply Beach and Shenoy, as further discussed in §VII.D-G.

B. A POSA would not modify the recessed embodiment of Saxler by removing the recess based on Yoshida

187. Petitioner largely relies on the same reasoning as Ground 1 by – again – starting with the hypothetical "non-recessed Saxler embodiment." Pet.('347) 60-65. Petitioner alleges "implementing Yoshida's non-recessed gate in Saxler's stacked gate structure results in the following combined structure, which is the same arrangement as Saxler's non-recessed embodiment. Shealy, [137]." Pet.('347) 51.



Pet.('347) 52

188. In Ground 1, the Petitioner proposes modifying the recessed embodiment of *Saxler* based on the non-recessed embodiment of Saxler to arrive at the same structure illustrated above. Here in Ground 2, Petitioner appears to be relying on the same reasoning to modify the recessed embodiment of Saxler based on the non-recessed structure of Yoshida to arrive at the same end result.

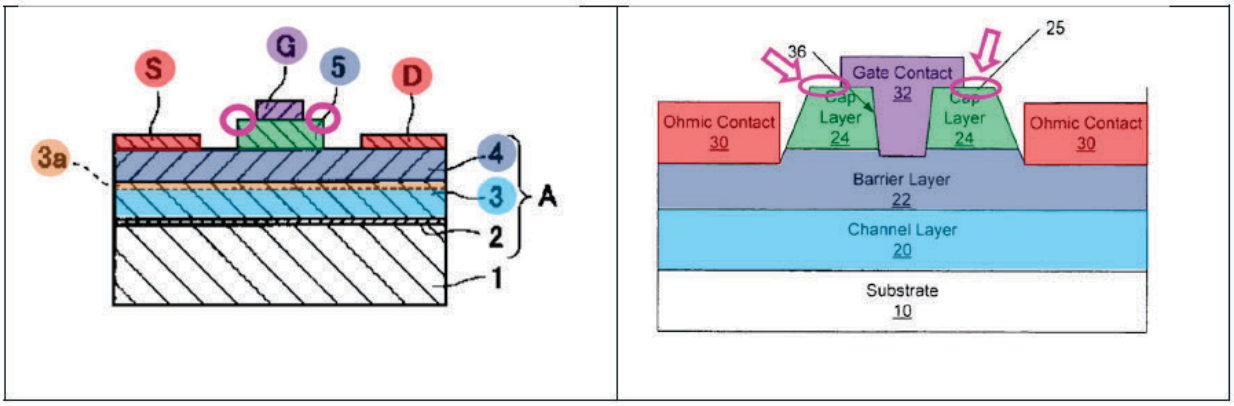
189. Petitioner's reference to "the same arrangement as Saxler's non-recessed embodiment" appears to be directed to the hypothetical selective "mix and match" of elements between the recessed embodiment of Saxler and the non-recessed embodiment of Saxler, that is in fact not described in or suggested by Saxler.

190. As discussed in §VIII.B, Petitioner's proposed modification in Ground 1 to arrive at the modified structure is improperly based on hindsight. Saxler explicitly teaches away from this modification by disclosing a number of structural and functional distinctions between the recessed embodiment and the non-recessed embodiment.

191. Petitioner appears to apply the same exact reasoning here in Ground 2 which is improper for at least the same reasons as addressed in §VIII.B.

192. Fig. 1A of Saxler and Yoshida are not "the same layers performing the same functions."

193. In referring to the recessed embodiment of *Saxler*, the Petitioner alleges "*Saxler* and *Yoshida* disclose compatible enhancement-mode GaN HEMT devices comprising the same layers performing the same functions, including a stacked gate structures having a cap layer and gate metal. Shealy, [140]… They use the same arrangement of layers, as the below comparison illustrates. Shealy, [140]." Pet.('347) 52.



Yoshida, Fig. 1, *Saxler*, Fig. 1A

Pet.('347) 53

194. This is misleading at best. Dr. Shealy explicitly opines that the recessed embodiment of Saxler would not be functionally equivalent with a non-recessed embodiment, stating that "with the recess, Saxler's device is not enhancement mode (always off)", and modifying the Saxler's recessed embodiment by "remov[ing] the recess to create an enhancement mode device and realize the benefits of a normally off device which renders it suitable for high power applications." EX1003 ¶146. Thus, at least according to Dr. Shealy, Saxler and Yoshida would <u>not</u> have "the same layers performing the same functions" as alleged by the Petitioner. Indeed removing the recess in an attempt to turn Saxler into an enhancement-mode device would substantially change the principle-operation of Saxler in being a depletion-mode transistor.

195. These statements by Petitioner are also inconsistent with the disclosure of *Saxler*. As further discussed in §VIII.B, *Saxler* describes a number of distinguishing structural and

functional aspects between the recessed embodiment and the non-recessed embodiment, including the shape, thickness, doping, and function of the cap layer. EX1017, Figs. 1A, B, 2A, 2B, and ¶¶7, 12, 14, 27, 62, 70, 71, 73, 74, 76, 81. In sum, Saxler discloses that the layer of the recessed embodiment is thicker, with a higher concentration of doping, and a doping layer that extends further into the cap layer than the non-recessed embodiment. EX1007 Figs. 1A-B, ¶¶12, 13, 14, 70, 71, 27, 81. Thus, Saxler would not remove the recess from the recessed embodiment in view of Yoshida for at least the very same reasons that Saxler does not disclose a non-recessed embodiment with the parameters of the recessed embodiment. Saxler's embodiments are distinct without any reason to "mix and match" as again implied by Petitioner here.

196. The statement that Saxler and Yoshida having "the same layers performing the same functions" is further contradictory of the modification, because POSA would not perform any modifications of Saxler in view of Yoshida if Yoshida discloses "the same layers performing the same functions."

C. Petitioner's apparent modification of Saxler does not produce a method for manufacturing an operational enhancement-mode transistor

197. Petitioner refers back to Ground 1 to address the preamble for Ground 2. Pet.('347) 57.

198. However, as further discussed in §VI.A, Saxler discloses depletion mode transistors and not enhancement mode transistors. EX1003 ¶099 ("Saxler does not use the phrase 'enhancement mode'");

199. As acknowledged by Dr. Shealy, the recessed embodiment of Fig. 1A is not enhancement mode. Pet.('347) 55-56; EX1003 ¶146 ("with the recess, Saxler's device is not enhancement mode (always off)").

200. As further provided by Dr. Shealy, the non-recessed embodiment of Fig. 1B would

not be a functional enhancement mode transistor because the cap layer 24' extends from ohmic contact 30 to ohmic contact 30. EX2004, 52:13-19 ("1B is a strange cartoon… I've never seen a device built that way, where the sides of the Ohmics are able to butt up against the cap layer -- you're not going to be able to fabricate that."); 65:16-18 ("that structure, as shown, would have these shunt problems I was talking about, potentially.")

201. Indeed, the hypothetical transistor proposed by Petitioner extends substantially the entire length between ohmic contacts 30. This is inconsistent with enhancement mode transistors, as previously discussed.

202. As provided by Yoshida, enhancement mode transistors are intended to provide voltage control with a small amount of carrier injection. EX1006 ¶17. This is produced in Yoshida by "etch[ing] away the p-type GaN layer except where the gate electrode was to be loaded and exposing the n-type InGaN layer 4." EX1006 ¶22.

203. Thus, a POSA would have no reason to modify the depletion mode transistors of Saxler having the cap layer 24 extending entire or substantially entirely between the ohmic contact 30 to somehow be retrofitted to produce an enhancement mode transistor. The design proposed by Petitioner would require excessive voltage to be applied to turn the transistor ON (assuming that it would even turn ON), undesirable for enhancement mode transistors. EX1006 ¶17.

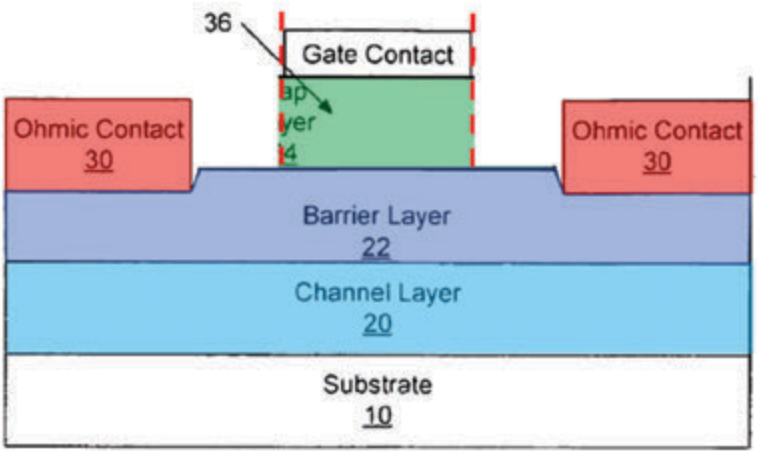
204. Petitioner alleges that "the Saxler-Yoshida gate structure is the same as the non-recessed Saxler structure. §VIII.A; Shealy, [150]. The combination of Saxler-Yoshida with Beach and Shenoy would have been obvious to predictably improve gate alignment and symmetry while reducing manufacturing steps and costs. §VII.A.5; Shealy, [150]." Pet.('347) 56.

205. [RESERVED]

D. The "self-aligned" technique of *Beach* would not produce the sloped sidewalls of Saxler, as relied on by Petitioner

206. Furthermore, Petitioner further cites Ground 1 in alleging that "the Saxler-Yoshida combination discloses the same stacked, stepped gate structure as the non-recessed Saxler embodiments. §VIII.A.2; Shealy, [158]. It would have been obvious to combine Saxler-Yoshida with Beach and Shenoy, disclosing [1f] for the same reasons explained for Saxler, Beach, and Shenoy. §§VIII.A.3, VII.B.7; Shealy, [112]-[115], [158]." Pet.('347) 57.

207. However, Beach does not preserve but removes sloped sidewalls. In addition, Beach does not preserve but removes ledges. As discussed in §VII.E and acknowledged by Dr. Shealy, applying Beach's self-aligned technique would either cut off or not form the horizontally extending "sloped" side surfaces that Petitioner relies on from Fig. 1A of Saxler and in the hypothetical transistor, as illustrated below.



Pet.('347) 45 (as modified based on Beach)

208. Indeed, Dr. Shealy explained "what Beach figure shows is a -- you know, it's drawn as a vertical wall. It's an idealized drawing, of course. Well, one would expect it to have some curvature." EX2004, 87:15-19.

209. Thus, Dr. Shealy directly undercuts Petitioner's motivation in that "Saxler discloses

such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet.('347) 35. Applying the Beach self-aligned technique to Saxler would not preserve but remove the sloped sidewalls as illustrated in Saxler but would rather produce intentionally vertical sidewalls with potentially "some curvature". Thus, a POSA would not modify Saxler with the self-aligned technique of Beach as alleged by Petitioner to arrive at the "sloped sidewalls" of Saxler.

E. The mathematical model of Shenoy would not produce the intended structure and would etch the GaN material based on Petitioner's reasoning

210. Petitioner alleges that "the Saxler-Yoshida gate structure is the same as the non-recessed Saxler structure. §VIII.A.2; Shealy, [150]. The combination of Saxler-Yoshida with Beach and Shenoy would have been obvious to predictably improve gate alignment and symmetry while reducing manufacturing steps and costs. §VII.A.5; Shealy, [150]." Pet.('347) 56.

211. Petitioner further relies upon Ground 1 in alleging "Saxler, Beach and Shenoy render obvious [1i]. §VII.B.10; Shealy, [163]-[164]. Saxler-Yoshida, Beach and Shenoy also renders obvious this limitation under either construction. Shealy, [164]. The Saxler-Yoshida combination discloses the same stacked, stepped gate structure as the non-recessed Saxler embodiments. §VIII.A.2; Shealy, [164]. It would have been obvious to combine Saxler-Yoshida with Beach and Shenoy, disclosing [1i] for the same reasons. §§VIII.A.3, VII.B.10; Shealy, [124]-[127], [164]." Pet.('347) 58-59.

212. However, as further discussed in §VII.E, Shenoy discloses that the spread of the EMM to perform the undercutting is induced by an **underlying** insulator. EX1009, 1 ("the extent to which EMM must proceed before the underlying insulator is exposed… Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal wall angle, χ.")

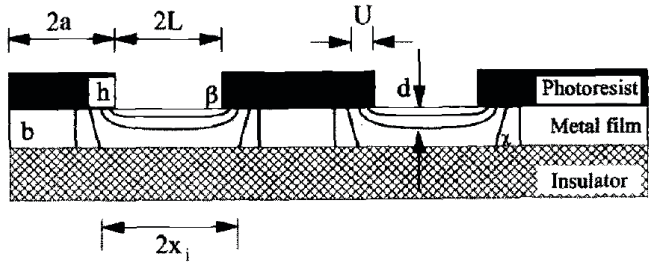
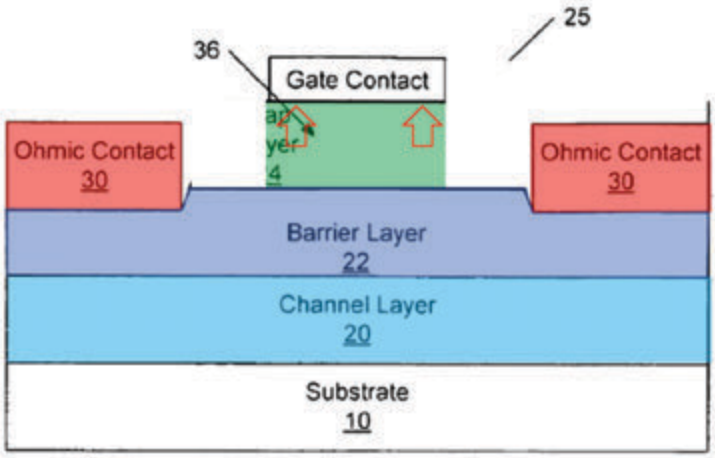


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

213. When comparing the mathematical setup of the Shenoy to the transistor of Saxler, the surface of the cap layer 34 in Saxler (as pointed out below by red arrows) that would underlie the gate contact 32 and form the ledges would not have been etched by the self-aligned process of Beach.



Pet.('347) 45 (annotated)

214. According to Dr. Shealy's reasoning, the surfaces of the cap layer 34 underlying the gate contact 32 would still "have holes" because it has not been etched (EX2004, at 99:4-13) and thus not act as an insulator. Therefore, the surfaces of the cap layer 34 underlying the gate contact 32 would be etched along with the gate contact in the etching process of Shenoy, thus not be retained.

215. Therefore, in addition to Beach, the actual teaching of Shenoy undercuts Petitioner's motivation in "Saxler discloses such sloped sidewalls with the claimed ledges, and Beach and Shenoy would have provided a known, obvious way to create that structure." Pet.('347) 35. Applying the etching of Shenoy would etch at least the surfaces of the cap layer 34 in Saxler underlying the gate contact that Petitioner relies on for the ledges. Thus, applying the method of Shenoy would not produce the hypothetical structure of Saxler, as alleged by Petitioner.

F. A POSA would not have found it obvious to combine Saxler, Yoshida, Beach, and Shenoy

216. Petitioner largely relies on the same reasoning as applied Ground 1. Petitioner attempts to modify the recessed embodiment of Saxler with the non-recessed structure of Yoshida instead of the non-recessed embodiment of Saxler to arrive at the same structure. Pet.('347) 51.

217. Thus, as further addressed in §§VII.B, Petitioner reiterates Dr. Shealy's logic of "mix and match" elements "depending on what you're trying to accomplish" throughout Ground 2 in trying to accomplish the claimed method.

218. Petitioner follows a similar meandering path of reengineering in Ground 2 that would not be obvious to POSA to arrive at the claimed method.

219. For at least those reasons, *Saxler* in view of *Yoshida*, *Beach*, and *Shenoy* does not render obvious claims 1-3 of the '347 Patent.

X. Ground 3 (Claims 1-3) of the '347 Patent - Saxler in view of Ahn

A. Overview

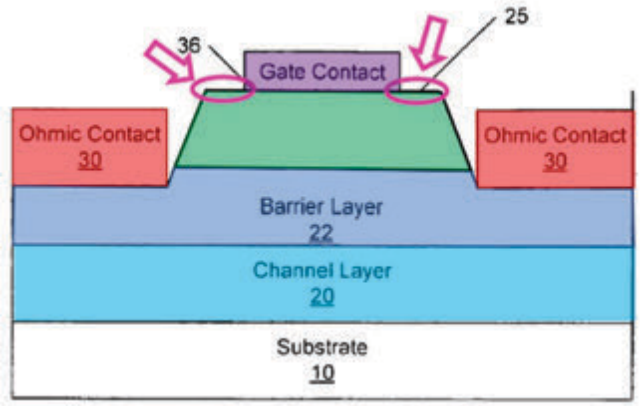
220. In Ground 3, Petitioner relies on the same unsupported structure of Saxler as discussed with respect to Grounds 1 and 2. Petitioner just relies on Ahn (instead of Beach and Shenoy) to reverse engineer that unsupported structure of Saxler. Petitioner does not even address which method of Ahn is being applied. Pet.('347) 63. ("Ahn teaches many ways to obtain the non-

recessed Saxler gate.") Indeed. Ground 3 suffers from the same fatal flaws as the other grounds without *ever presenting a description of the actual proposed modified prior art process*. Rather, Petitioner simply picks and chooses different *features* of the prior art and abstractly asserts that the combination renders the claims obvious, without explaining how the proposed combination would fit into an overall process to arrive at the claimed invention or even which process Petitioner is relying on.

B. A POSA would not consider the gate recess of Saxler as "optional" and Dr. Shealy's "mix and match" actually implies substantial modifications

221. Petitioner alleges "to the extent Saxler alone does not explicitly disclose masking and etching the gate contact or self-aligned etching, Ahn renders this obvious." Pet.('347) 60.

222. Petitioner further alleges "the combination would yield the same structure as the non-recessed Saxler embodiment" as follows:



Pet.('347) 62

223. In Ground 3, Petitioner largely relies on the same reasoning as Ground 1 in citing the hypothetical "non-recessed Saxler embodiment" (Pet.('347) 60-65) produced in Ground 1 and reproduced above. Thus, Petitioner is relying on Ahn to teach another method of forming the structure of Petitioner's proposed hypothetical gate structure, as shown on page 62 of the petition.

224. However, as further discussed in §VIII.B, Saxler does not disclose the structure that Petitioner is relying on in Ground 3. The hypothetical structure is based on Petitioner's improper attempt to "mix and match" parameters from two distinct embodiments "depending on what you're trying to accomplish." More specifically, Petitioner is attempting to "mix and match" the outer perimeter of the recessed embodiment of Fig. 1A and the non-recessed gate structure of Fig. 1B.

225. Saxler describes a number of additional distinguishing structural and functional aspects between the recessed embodiment and the non-recessed embodiment, including the shape, thickness, doping, and function of the cap layer. See EX1007, Figs. 1A, B, 2A, 2B, ¶¶7, 12, 14, 27, 62, 70, 71, 73, 74, 76, 81. Petitioner's proposed "Saxler's non-recessed stacked gate structure" relied on in Ground 3 is not based on motivation or reasoning, but rather hindsight reconstruction.

C. Petitioner's modification of Saxler does not produce a method for manufacturing an operable enhancement-mode transistor

226. Petitioner refers back to Ground 1 to address the preamble for Ground 3. Pet.('347) 64.

227. However, as further discussed in §§VII.A; VIII.C, Saxler discloses depletion mode transistors and not enhancement mode transistors. EX1003 ¶099 ("Saxler does not use the phrase 'enhancement mode'");

228. As acknowledged by Dr. Shealy, the recessed embodiment of Fig. 1A is not enhancement mode. Pet.('347) 55-56; EX1003 ¶146 ("with the recess, Saxler's device is not enhancement mode (always off)").

229. As further provided by Dr. Shealy, the non-recessed embodiment of Fig. 1B would not be a functional enhancement mode transistor because the cap layer 24' extends from ohmic contact 30 to ohmic contact 30. EX2004, 52:13-19 ("1B is a strange cartoon… I've never seen a device built that way, where the sides of the Ohmics are able to butt up against the cap layer --

you're not going to be able to fabricate that."); 65:16-18 ("that structure, as shown, would have these shunt problems I was talking about, potentially.")

230. Indeed, even the hypothetical transistor proposed by Petitioner extends substantially the entire length between ohmic contacts 30. This is inconsistent with enhancement mode transistors.

231. As provided by Yoshida, enhancement mode transistors are intended to provide voltage control with a small amount of carrier injection. EX1006 ¶17. This is produced in Yoshida by "etch[ing] away the p-type GaN layer except where the gate electrode was to be loaded and exposing the n-type InGaN layer 4." EX1006 ¶22.

232. Thus, a POSA would have no reason to modify the depletion mode transistors of Saxler having the cap layer 24 extending entirely or substantially entirely between the ohmic contact 30 to somehow be modified to produce an alleged enhancement mode transistor. The modified design of Petitioner would require excessive voltage to be applied to turn the transistor ON (assuming that it would even turn ON), undesirable for enhancement mode transistors. EX1006 ¶17. The modification would also improperly change the principle operation of Saxler, in being a depletion-mode transistor.

D. A POSA would have no motivation to modify the method of Saxler based on Ahn

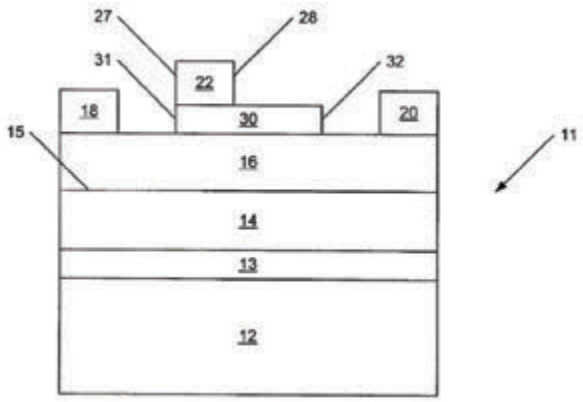
233. Petitioner's analysis is based on a faulty premise that Saxler intends for a centrally aligned gate electrode.

234. Petitioner alleges that "a POSITA would have found it obvious to modify Saxler with Ahn's approach for making a stepped gate in a thin-film transistor to improve alignment. Shealy, [174] (citing Ahn, Abstract, 3:41-58, 6:15-26, 7:7-14-46, Figs. 4A-4C)." Pet.('347) 63.

235. Petitioner's assumption that Saxler would desire "alignment," specifically central

alignment (as taught by Ahn), is solely based on Fig. 1A. Saxler explicitly discloses that "the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device." EX1007 ¶42. Thus, Saxler is explicitly stating that the drawings cannot be relied on for exact dimensions or direct alignment in that "the precise shape of a region" is not intended to limit the scope.

236. The only disclosure of the relative position of the gate electrode on the cap layer is that "the recess may be offset between the source and drain contacts such that the recess, and subsequently the gate contact 32, is closer to the source contact than the drain contact." EX1007 ¶65. This offset positioning is further consistent with Smith, as expressly incorporated by reference. EX1007 ¶42. Smith explicitly discloses that the gate electrode is intentionally aligned or substantially aligned with the source-side of the source-side segment of the GaN cap segment 30, and if not "may be detrimental to the device." EX1015 ¶¶41-42.



EX1015, Fig. 3

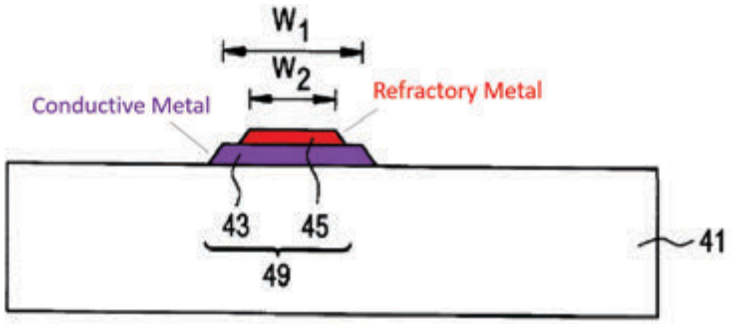
237. Thus, Saxler does not mention the gate electrode being directly aligned centrally with the cap layer. Saxler only discloses the gate electrode "may be offset… closer to the source contact than the drain contact." EX1007 ¶65. This intentional "offset" is inconsistent with the modifications proposed by Petitioner in applying the method of Ahn.

238. In other words, Saxler has no aligned structures, so a POSA would not have any motivation of applying a self-aligned technique absent hindsight, in here Dr. Saxler is "trying to accomplish" the claimed invention.

239. Ahn teaches a substantially different gate structure from Saxler solving an unrelated problem and different etching methods

240. As further discussed in §VII.E, Ahn is specifically directed to the development of a double-layered metal gate as a substitute for a single-layer to prevent deterioration of a gate oxide layer that would produce a short circuit with vertically aligned source and drain electrodes 29, 31. A thin film transistor is a special type of FET where the transistor is made by a specific thin film deposition, diverging from GaN HEMTs.

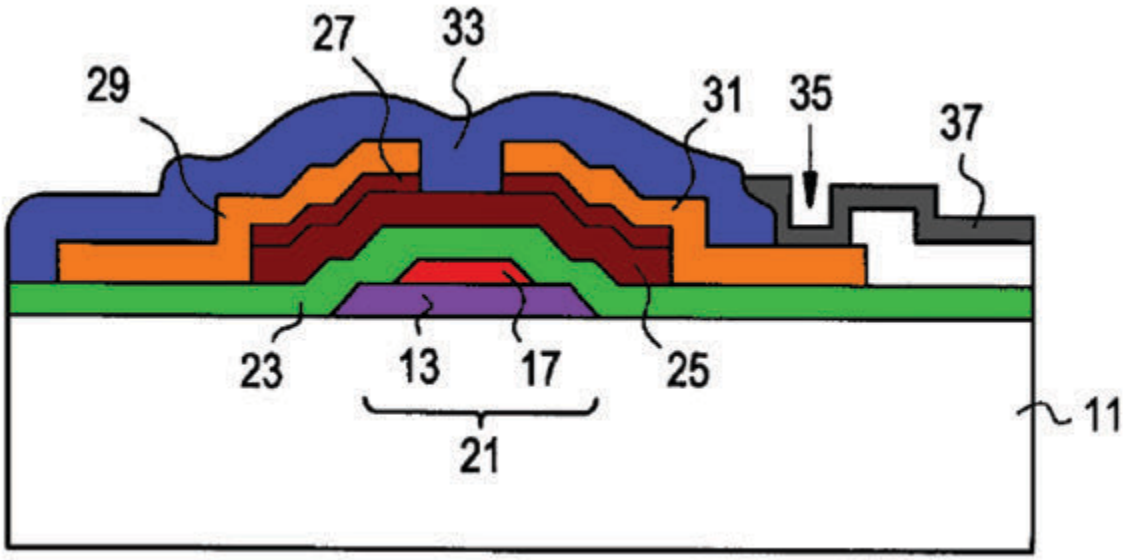
241. The double-layered metal gate is formed of a lower metal layer 43 of a conductive metal (Al, Cu, or Au) in contact with the substrate 41 and a top metal layer 45 of a refractory metal (Mo, Ta, or Co) overlying the bottom conductive metal layer 43.



EX1010, Fig. 4C

242. As further illustrated below, the gate oxide layer 23 is deposited between the double-layered metal gate 21 and semiconductor and ohmic contact layers 25 and 27 that provide a connection between the source and drain electrodes 29, 31. Thus, Ahn is concerned about deterioration of the gate oxide layer 23 due to this vertical arrangement in that the gate oxide layer 23 thinly separates the semiconductive layer 25 from the gate 21. Deterioration of the gate oxide

layer 23 may cause an electrical connection between the semiconductive layer 25 and the gate 21 causing a short circuit. EX1010, 1:36-38; Fig. 1F.



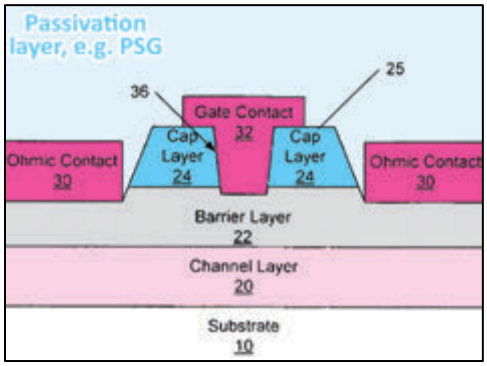
EX1010, Fig. 1F

243. Saxler is not a thin film transistor nor has relevant analogous structure. Saxler does not have a thin gate oxide layer 23 separating the gate and the source and drain electrodes 29, 31. Furthermore, Saxler does not disclose a gate structure of a double-layer metal structure.

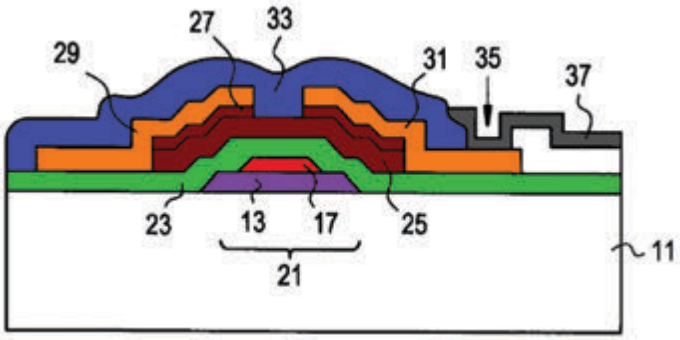
244. The functioning and layering of GaN HEMTs such as Saxler is completely different from that of thin film transistors such as Ahn. For example, the ohmic contacts 30 of Saxler do not overlap with the gate not is the gate separated by a thin gate oxide layer from a semi-conductive layer. Rather, as Dr. Shealy states the components in Saxler are laterally spaced apart by a significant distance to avoid a short circuit. EX2004, 65:15-18. The 2DEG in Saxler is formed underneath the gate structure, and not above as in Ahn. Furthermore, the barrier layer 22 in Saxler separates the gate contact from the channel layer 20, forming the 2DEG connecting the ohmic contacts 30. Saxler does not layer the ohmic contacts 30 above the gate contact 32 as in Ahn. Thus, any deterioration of any overlaying passivation layer would not have the same effect as that

in the layered structure of Ahn.

245. Furthermore, any passivation layer above the GaN HEMTs such as Saxler is substantially thick (e.g., 500 nm to 1,000 nm) compared to the thin gate oxide layer 23 of Ahn that is on the order of 10 nm. Additionally, the passivation layers of GaN HEMTs such as Saxler are often made of a different material than thin film transistors, such as PSG (phospho silicate glass) or BPSG (boro phospho silicate glass), where Boron and/or Phosphorus are added to make the glass tend to flow (rather than being rigid) so that pin-holes are rare or absent.



EX1007, Fig. 1A



EX1010, Fig. 1F

246. Furthermore, Ahn attempts to cure these problems of the double-layered metal gate by making the width W1 of the bottom conductive metal layer 43 intentionally greater than the width W2 of the top refractory metal layer 45. EX1010, 4:46-52. Saxler, on the other hand, has a metal gate contact 32 layered on a GaN cap layer 24. Thus, any structure of the double-layered metal gate of Ahn is not relevant to the gate structure of Saxler. The differences in the gate structure are highlighted by the fact that Ahn creates a slanted sidewall in the conductive metal layer 13 of the gate 21 which would result in a huge leakage current, contrary to assertions by Petitioner for the tapered sidewalls of Saxler.

247. Although both Ahn and Saxler relate to transistors, the types of transistors are substantially different. Ahn relates to silicon thin-film transistors for an LCD. EX1010, 12-16.

Saxler relates to GaN HEMTS (high-electron-mobility transistors) that are epitaxially grown. The etching chemistries and etching dynamics (e.g. crystallographic etching) of metals (such as aluminum, Al) and semiconductors (such as gallium nitride, GaN) are divergent. The etching of a material cannot be considered in isolation, but specific etching techniques are applied to specific materials, and the etching of the gate 21 does not involve etching a GaN material.

248. Furthermore, this structure of the double metal layer gate of Ahn is not relevant to that of Saxler that discloses an AlGaN based cap layer 34, 34' that extends substantially the entire length or the entire length between ohmic contacts and a gate contact 32 disposed on the cap layer 34, 34'.

249. Thus, the deterioration of the thin gate oxide layer 23 of Ahn would not be relevant to Saxler. Thus, a POSA would not modify the gate structure of Saxler based on that of the thin film transistor of Ahn.

XI. Ground 4 (Claims 1-3) of the '347 Patent - Yoshida in view of Saxler, Beach, and Shenoy

A. Overview

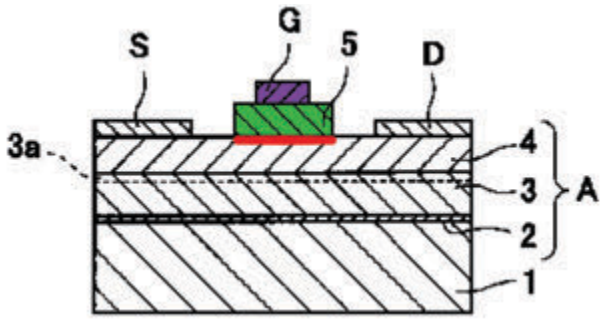
250. Petitioner relies heavily on Fig. 1 of Yoshida and its schematic. Pet.('347) 97. However, as further discussed in §VII.D, these type of schematics do not represent an actual transistor with respect to the geometrical dimensions and their respective ratios. Pet.('347) 90-91; EX2004, 53:13; 53:23-57:1, 60:17-18, 90:25-91:1; EX1007 ¶42.

251. Indeed, Petitioner specifically relies on the ledges depicted in the figure of Yoshida. These ledges are typical for transistors that are manufactured with the gate last approach that Yoshida clearly describes, where the p-type GaN material 5 is etched before the gate contact G is deposited. EX1006 ¶22 ("etch[ed] away… except for where the gate electrode was to be loaded"). In the two mask process, it is known that the p-type GaN material 5 is etched to be wider than the

gate contact G to ensure that the gate contact G is received properly. The '347 Patent at 4:52-54. However, neither Yoshida nor Petitioner provide any functional purpose for these ledges, thus a POSA would not perform additional unnecessary etching steps to produce unnecessary features.

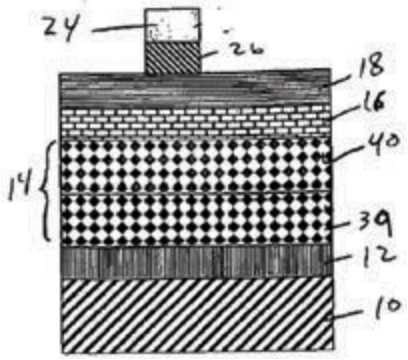
252. Yoshida explicitly distinguishes its method from "conventional photolithography and etching" (EX1006 ¶¶6, 8) directly contradicting Petitioner's assertion that "a POSITA would have known many ways to create Yoshida's… structure and would have used these methods interchangeable" (Pet.('347) 97).

253. The method of Yoshida is specifically designed to manufacture an enhancement mode transistor to locate the pn junction of a p-type GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility." EX1006 ¶17.



EX1006, Fig. 1 (annotated)

254. Even assuming that Yoshida could be produced by the self-aligned process of Beach, thus there would be no motivation for additional etching, such as that disclosed by the mathematical model of Shenoy.



EX1008, Fig. 2F

255. Thus, similar to Grounds 1-3, Petitioner seemingly continues Dr. Shealy's logic of "mix and match" elements from Yoshida, Saxler, Beach, and Shenoy "depending on what you're trying to accomplish", specifically to accomplish the claimed method.

B. Neither Petitioner nor Yoshida characterizes Yoshida's method as being "flexible" as relied on by the Board

256. The Board appears to be mistaken in referring to "Yoshida's flexible method." Institution 50. Yoshida does not describe its method as being flexible, nor does Petitioner characterize it as such. Yoshida actually distinguishes the process from forming the gate structure with "conventional photolithography and etching" in that the transistors produced by those "conventional" methods "cannot be said to have sufficient electron mobility to meet recent demands for still higher speed operations." EX1006, 6, 8. Thus, Yoshida relies on a specific process of forming its transistor.

257. In describing its own method, Yoshida describes its process in ¶¶19-23 with transitional terms including "first… then… then… then… lastly..." This is acknowledged by Dr. Shealy in stating "Yoshida specifically discloses: (i) depositing a p-type GaN layer 5 onto AlGaN layer 4 (Yoshida, [0021]); (ii) dry etching the 'p-type layer except where the gate electrode was to be loaded' (Yoshida, [0022]); (iii) depositing an SiO2 film over the entire surface (id.); (iv) patterning with a photoresist, and masking where the gate electrode was to be loaded (id.); (v)

depositing source and drain electrodes (id.); (vi) 'etching away the masking and opening the SiO2 film (Yoshida, [0023]); (vii) masking the source and drain electrodes; and (viii) depositing Au to form the gate electrode (id.)." EX1003 ¶204. Dr. Shealy later stated that "it's not clear what the order of the process is" in his deposition (EX2004, 78:14-15) which just contradicts this prior statement in his Declaration.

258. Furthermore, Yoshida describes its process for example with such specificity in exact growth temperatures, deposition conditions, and timing of transitions in metal supplies. EX1006 ¶¶17-23.

259. Due to this specificity in order and processes, a POSA would recognize that Yoshida's method is not flexible.

C. Yoshida teaches away from using other methods of manufacturing its gate

260. Yoshida actually distinguishes the process from forming the gate structure with "conventional photolithography and etching" in that the transistors produced by those "conventional" methods "cannot be said to have sufficient electron mobility to meet recent demands for still higher speed operations." EX1006, 6, 8. Thus, Yoshida relies on a specific process of forming its transistor.

261. Thus, Yoshida directly contradicts Petitioner's assertion that "a POSITA would have known many ways to create Yoshida's… structure and would have used these methods interchangeable" (Pet.('347) 97) where Yoshida expressly distinguishes its method from "conventional photolithography and etching." EX1006 ¶¶6, 8.

262. As further discussed herein, the process of Yoshida is specifically intended to design a transistor with a pn junction of a p-type GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection, and the controlled voltage

further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility." EX1006 ¶17.

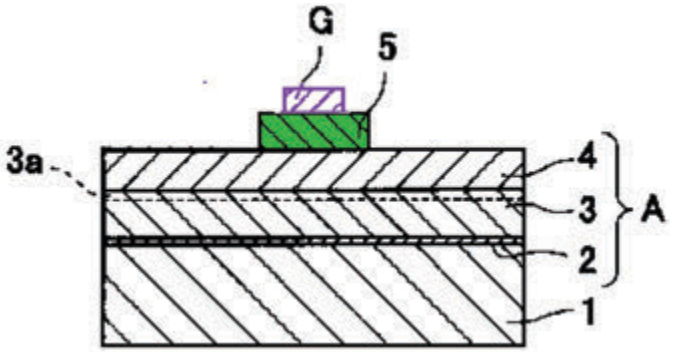
263. This configuration and functionality is not produced by the methods relied on by Petitioner, specifically Saxler and Shenoy that are directed to producing completely different transistor configurations or even theoretical mathematical models as discussed herein.

264. For at least these reasons, Petitioner's proposed modification of Yoshida's method in grounds 4 and 5 in "trying to accomplish" (EX2004, 38:3-5) the claimed invention is improper.

D. A POSA would have no reason to form ledges on Yoshida after the self-aligned process of Beach

265. Petitioner alleges "a POSITA would have found it obvious to use Beach and Shenoy's techniques to self-align the p-type gate material and gate metal and isotropically etch the gate metal using a single mask to obtain self-aligned ledges." Pet.('347) 72.

266. I respectfully disagree. To the extent that there are ledges and slanted sidewalls before the Beach process, the Beach process removes these features (ledges & slated sidewalls). In addition, the Beach process does neither create ledges nor slanted sidewalls. As discussed in §§VII.B, X.A, the transistor of Yoshida is formed by a process where the p-type GaN layer 5 is layered and "etch[ed] away… except for where the gate electrode was to be loaded" (prior to loading the gate electrode G). EX1006 ¶22.

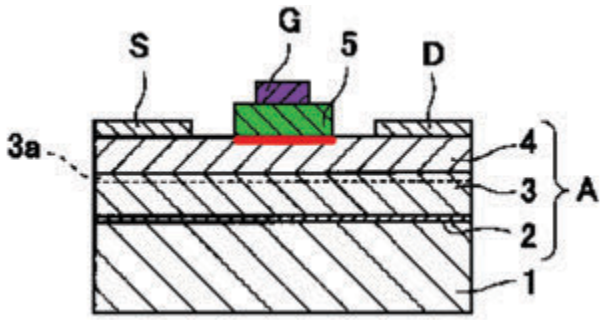


EX1006, Fig. 1 (annotated)

267. Although the p-type GaN layer 5 is illustrated as being formed wider than the gate G, that structure is typical for processes where the p-type GaN layer 5 is patterned before the gate electrode G is loaded to provide a wider platform to be sure that the gate electrode is received on the p-type GaN layer 5 without overhang. The '347 Patent at 4:52-54.

268. This is consistent with the references that Petitioner cites to show a pair of ledges, where the ledges are common when the base is patterned before the electrode metal is deposited. EX1011 Fig. 1, ¶6 ("processed with two different photomasks"); EX1018 at Fig. 1, Page 1 ("Transistors were then fabricated with… source-drain contacts… Ni/Au contacts were then deposited over the selective area grown *p*-GaN regions."); EX1017, Figs. 5-6; ¶56 ("Referring to FIG. 5, the p-type Al_z GaN cap layer 11 is etched to define a gate region where the p-type Al_zGaN cap 11 is located. Referring to FIG. 6, a gate 17 with a schottky contact… are formed on the Ga-face to form an assembly.") EX1007 Fig. 1B, ¶¶61-65 (as discussed herein).

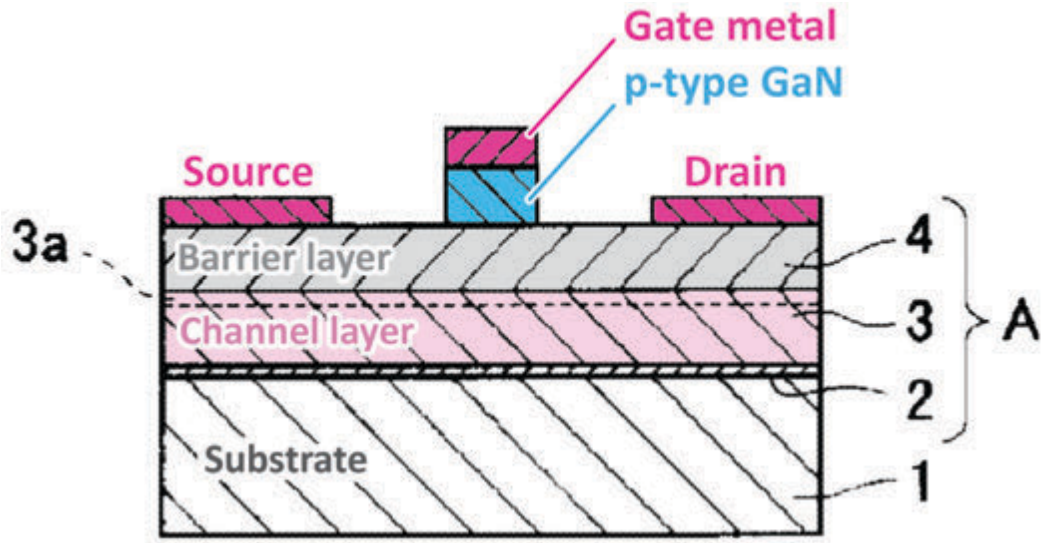
269. Yoshida does not describe any operational function of the illustrated ledges after the gate electrode is loaded. EX1006 ¶22 ("etch[ed] away… except for where the gate electrode was to be loaded"). Rather, as previously discussed, the transistor of Yoshida is assembled to locate the pn junction of a p-type GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility." EX1006 ¶17.



EX1006, Fig. 1 (annotated)

270. Thus, the intended transistor design of Yoshida is to align the pn junction with the gate electrode G ("immediately under") for "voltage control with a small amount of carrier injection." EX1006 ¶17. This is obtained in the gate-last approach of Yoshida by "etch[ing] away the p-type GaN layer except for where the gate electrode was to be loaded." EX1006 ¶22.

271. Even assuming POSA were to modify the process of Yoshida by replacing it with the "self-aligned" technique of Beach (although I disagree that such a modification would be appropriate), this "self-aligned" technique would achieve what Yoshida intends. The p-type GaN layer 5 would be "etch[ed] away… except for where the gate electrode was [] loaded" because the gate electrode G would be self-aligned with the p-type GaN layer 5. EX1006 ¶22. Thus, the pn junction of a p-type GaN layer 5 would be "immediately under" the gate electrode G. EX1006 ¶17. The direct alignment of the gate electrode G with the pn junction would optimize "voltage control with a small amount of carrier injection" as is the intended result of Yoshida. EX1006 ¶17.



EX1008, Fig. 1 (modified)

272. Thus, a POSA would have no reason to perform additional etching steps to form the claimed ledges that have no operational function after the gate metal G is loaded on the p-type GaN layer 5. Indeed, Petitioner provides no motivation or reasoning for POSA to perform additional etching steps to form ledges that have no operational function after the gate electrode G is loaded on the p-type GaN layer 5.

273. Unnecessary etching would add manufacturing costs and steps, producing a less efficient method, contrary to Petitioner's assertions. Pet.('347) 32, 35, 48, 54, 55. Petitioner merely relies on the depiction of Yoshida in Fig. 1, which is a transistor formed by the p-type GaN layer 5 being etched before the gate electrode G. Fig. 1 also does not illustrate the manufactured gate structure. Indeed, performing unnecessary etching steps (such as that described in Shenoy) to produce extraneous structure without any operational function would be counter to Petitioner's motivations of "eliminating masking and etching steps," "reduc[ing] steps and costs" and predictably creating the "stacked gate structure more efficiently." Pet.('347) 32, 35, 48, 56, 64, 77; EX1003 ¶¶93, 205.

274. Selectively etching the gate electrode G after being loaded on the p-type material 5

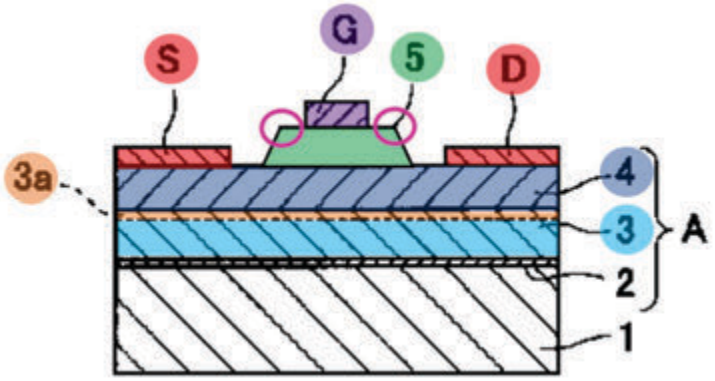
would be contrary to the intention of Yoshida because it would intentionally reduce the width of the gate electrode G relative to the pn junction creating non-overlapping segments of the pn junction, thus reducing "voltage control" by increasing the required amount of carrier injection.

E. A POSA would not modify Yoshida with side walls extending horizontally

275. A POSA would not modify Yoshida with the tapered side walls of Saxler, as proposed by Petitioner.

276. Petitioner alleges that "it would have been obvious to modify Yoshida's transistor with the sloped sidewalls of Saxler's capping layer to reduce gate leakage. Shealy, [197]. The combination calls for nothing more than the simple substitution of Saxler's sidewalls to predictably make an enhancement-mode GaN HEMT. Id." Pet.('347) 73.

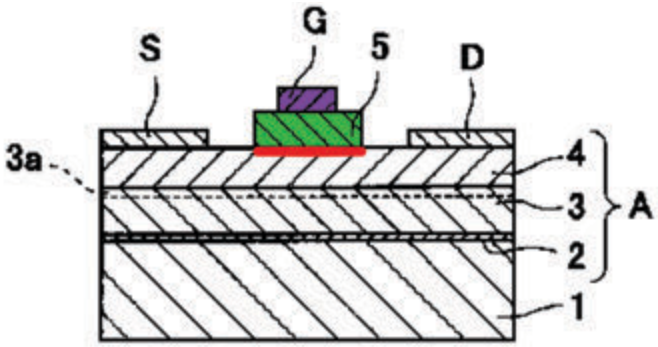
277. Petitioner further alleges "implementing Saxler's sloped sidewalls in Yoshida's layer 5 results in the following combined structure. Shealy, [196]." *Id*.



Pet.('347) 73

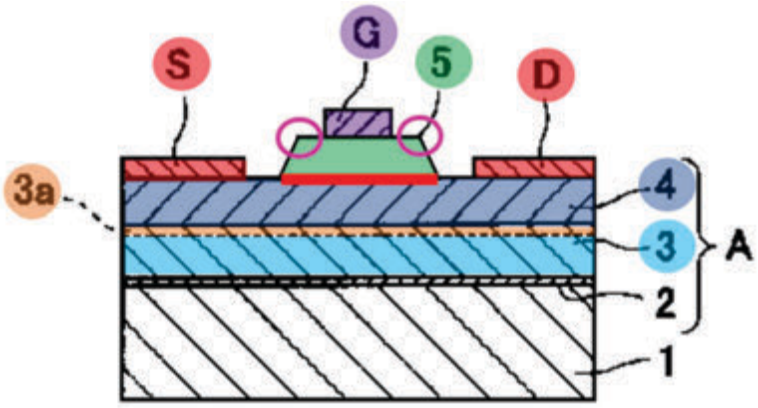
278. I respectfully disagree. As discussed above in §§VII.B, X.A, the transistor of Yoshida is formed by a specific process where the p-type GaN layer 5 is layered and "etch[ed] away… except for where the gate electrode was to be loaded" (prior to loading the gate electrode G). EX1006 ¶22. The transistor of Yoshida is assembled to position the pn junction of a p-type

GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility." *Id*. ¶17.



EX1006, Figs. 1 (annotated

279. Thus, Yoshida teaches away from adding the alleged sloped sidewalls of Saxler's capping layer to the p-type GaN layer 5 because doing so would intentionally widen the pn junction relative to the gate electrode G creating misalignment, thus reducing "voltage control" by increasing the required amount of carrier injection and reducing high-speed electron mobility.



Pet.('347) 73 (annotated)

280. Furthermore, as discussed above in §§VII.A, VIII.B and addressed by Dr. Shealy,

the recessed embodiment of Saxler as relied on by Petitioner is not an enhancement mode transistor. EX1003 ¶146. Thus, Saxler does not support Petitioner's motivation of "reduc[ing] gate leakage." Pet.('347) 73-74, EX1003 ¶197.

281. Accordingly, Petitioner's assertion that "it would have been a simple substitution of Yoshida's vertical sidewalls with Saxler's sloped sidewalls to predictably yield an enhancement-mode GaN HEMT. Id" (Pet.('347) 74) is meritless. In other words, modifying an enhancement-mode GaN HEMT of Yoshida with features of a **depletion-mode** HEMT of Saxler (EX1003) "**to predictably yield an enhancement-mode GaN HEMT**" is illogical.

282. Petitioner further asserts that "while Yoshida and Saxler disclose slightly different topologies for their stacked gate structures, these structures perform identical functions in both references, which is, as Yoshida puts it, to control voltage 'with a small amount of carrier injection' and 'enable[] control of current flowing between channels' at high voltage. Yoshida, [0017]; Saxler, [0065]." This assertion is misleading at best. Petitioner takes direct questions from ¶[0017] of Yoshida, but ¶[0065] of Saxler does not come close to what Petitioner is alleging.

283. Petitioner's reliance on manufacturing tolerances is misdirected.

284. Petitioner further alleges that "Yoshida alone renders obvious sloped sidewalls that extend horizontally towards source and drain contacts under Patent Owner's construction" based on manufacturing tolerances. Pet.('347) 90-91.

285. More specifically, Petitioner alleges that "although Yoshida draws substantially vertical sidewalls of p-type layer 5, a POSITA would have known a sidewall drawn vertically would have a slight slope when built in a practical device. Pet.('347) 90-91. For example, Saxler notes that, in practice, 'an etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features.' Saxler, [0042]; Shealy, [230]." Pet.('347) 90-91.

286. Even considering such a broad interpretation of Yoshida (which I disagree with), Petitioner fails to address the claim construction of the term "forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer." Indeed, the claim interpretation of vertical surfaces always having some sort of imperfections in "a slight slope when built in a practical device" or "tapered, rounded or curved features" would not meet the claim construction proposed by either the Petitioner or the Patent Owner as reproduced below. For example, although still not straight, etching may extend at an angle inwardly to undercut the material, thus would not potentially create a wider base.

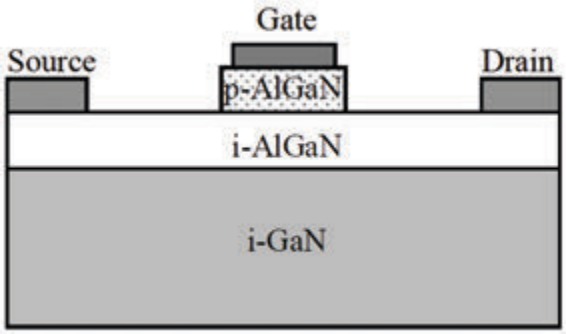
Petitioner's Proposed Claim Construction	Patent Owner's Proposed Claim Construction
"forming side surfaces of the ptype gate material such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces that contact the barrier layer"	"forming side surfaces of the ptype gate semiconductor material such that the bottom of the material, which contacts the barrier layer, is wider than the top of the material"

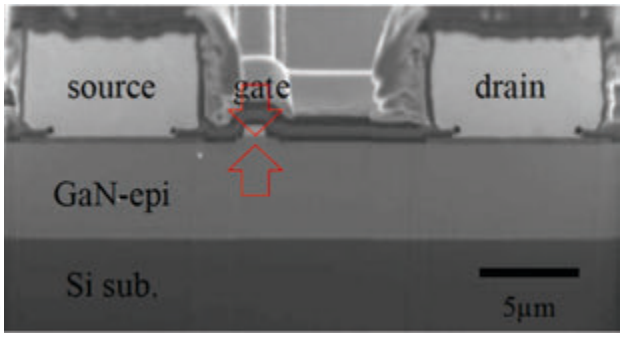
EX1028

287. In addressing Uemoto, the Petitioner alleges "as another example, a 2006 IEEE paper on a GaN HEMT with a similar gate structure to Yoshida depicts its p-AlGaN gate layer having vertical sidewalls in its drawings (Fig. 1) but shows sloped sidewalls extending horizontally towards source and drain contacts in a microscope image of a device built according to the drawings. Uemoto, Figs. 1-2, Fig. 5; Shealy, [230]." Paper 1 at p. 91.

288. However, it should be noted that the SEM image in Fig. 5 illustrates the gate layer as such a fine sliver of material and having the same color (medium gray) as the underlying GaN-

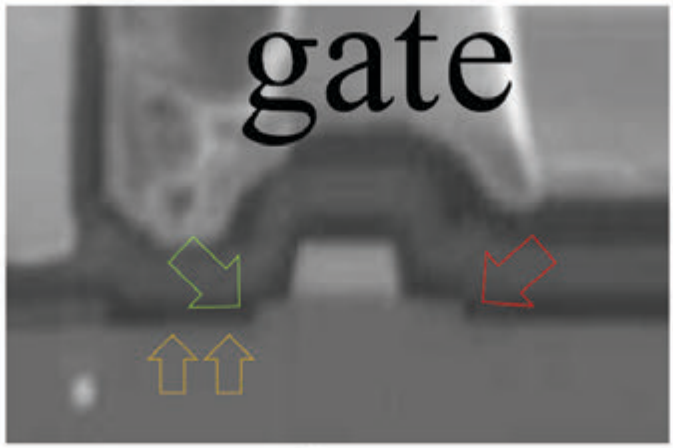
epi layer. The sliver of material is barely visible in Fig. 5.





EX1020, Fig. 1(a) **EX1020, Fig. 5**

289. Digitally zooming in on such a small region of Fig. 5 creates such extreme pixelation and potential artifacts that any type of horizontal extension of the sidewalls is not ascertainable.



EX1020, Fig. 5 (heavily magnified)

290. As best represented above, even with the pixelation, a POSA would not consider the sidewall on the drain side (as pointed out in red) and the sidewall on the source side (as pointed out in green) of what the Petitioner would rely on for the p-type gate material to be considered "extend[ing] horizontally towards the… drain contacts" as claimed. It should be noted that there is severe pixelation or artifacts due to the magnification, but there also appears to be the pixels of

the p-type gate blending into the pixels of a raised and pixelated upper surface of the GaN-epi layer and/or barrier layer (as pointed out in orange). This representation cannot reasonably support the Petitioner's position, especially in view of the Petitioner's and Patent Owner's claim constructions, as outlined above.

291. Thus, Uemoto provides evidence that "side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer" are not "necessarily" formed during etching of a p-doped GaN material. Thus, Uemoto contradicts Petitioner's statement that "a POSITA would have known a sidewall drawn vertically would have a slight slope when built in a practical device." Furthermore, even considering the disclosure in Saxler, it does not address both sidewalls and that the bottom of the allegedly p-doped GaN material, which contacts the barrier layer, being wider than the top of the material as the term is construed.

292. Furthermore, Petitioner fails to provide any relationship between the etching of Saxler or Uemoto with that of Yoshida. A POSA would understand that there are numerous different ways of etching a material, each with their own parameters and drawbacks. Petitioner does not provide any supporting evidence that the etching performed in Saxler or Uemoto is the same as that in Yoshida.

293. [RESERVED]

294. In any case, Petitioner fails to make such a case, and only engages in the exercise of probabilities or possibilities. Indeed, in his deposition, Dr. Shealy acknowledges the possibility of vertical sidewalls. EX2001, 46:3-5. Dr. Shealy also acknowledges the possibility of achieving an "undercut" (EX2001, 47:6-10) so that the sidewalls are formed extending inwardly; e.g., forming a gate material having whereby the top of the gate material is wider than the bottom of

the gate material – this is exactly opposite of what the claims require. I agree with Dr. Shealy in that vertical and undercut sidewalls are a possibility, such that horizontally extending sidewalls are not "necessarily" present in Yoshida. Furthermore, Petitioner fails to provide any motivation to modify Yoshida with the horizontally extending walls produced by certain manufacturing tolerances. Yoshida explicitly does not desire horizontally extending sidewalls.

295. [RESERVED]

296. [RESERVED]

297. [RESERVED]

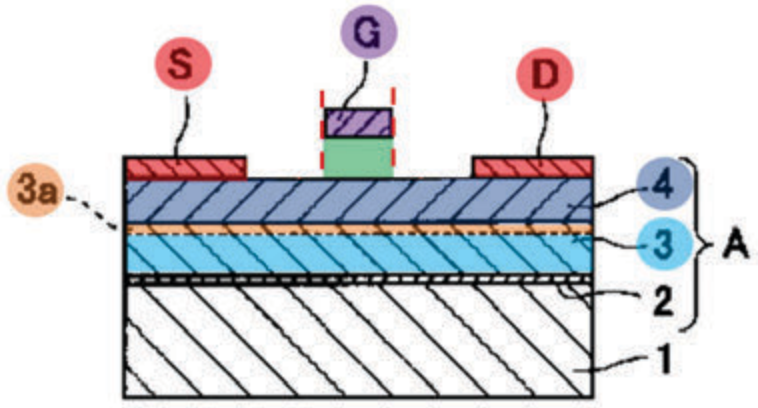
298. [RESERVED]

299. . [RESERVED]

F. The "self-aligned" technique of *Beach* would not produce the sloped sidewalls of Saxler, as relied on by Petitioner

300. Petitioner alleges that "a POSITA would have found it obvious to use Beach's approach to create and symmetrically align Yoshida-Saxler gate structure for improved performance. Beach, [0040], Fig. 1; Shenoy, 2-3; Shealy, [207]." Pet.('347) 79.

301. However, as further discussed in §VII.E and acknowledged by Dr. Shealy, applying Beach's self-aligned technique would either cut off or not form the horizontally extending "sloped" side surfaces that Petitioner relies on from Fig. 1A of Saxler and in the hypothetical transistor, as illustrated below.



Pet.('347) 73 (modified by Beach self-aligned process)

302. Indeed, Dr. Shealy explained "what Beach figure shows is a -- you know, it's drawn as a vertical wall. It's an idealized drawing, of course. Well, one would expect it to have some curvature." EX2004, at 87:15-19.

303. Thus, Dr. Shealy directly undercuts Petitioner's motivation arguments of applying Beach to form the sidewalls of Fig. 1A of Saxler. Pet.('347) 79. Applying the Beach self-aligned technique to Petitioner's Yoshida-Saxler combination would not produce the sloped sidewalls as illustrated in Saxler, but would instead produce intentionally vertical sidewalls with potentially "some curvature". Thus, a POSA would not modify Saxler with the self-aligned technique of Beach as alleged by Petitioner to arrive at the "sloped sidewalls" of Saxler. To the extent that there are ledges and slanted sidewalls before the Beach gate formation process, the Beach process removes these features (ledges & slated sidewalls). In addition, the Beach process does neither create ledges nor slanted sidewalls. Dr. Shealy has utterly failed to show that ledges and slanted sidewalls could be created after Beach's self-aligned gate formation process. And it is my opinion that Petitioner has clearly not met its burden to show these features (ledges & slanted sidewalls) can be created after Beach's self-aligned gate formation process.

G. The mathematical model of Shenoy would not produce the intended structure and would etch the GaN material based on Petitioner's reasoning

304. Petitioner (by incorporated Ground 1) alleges that "as previously explained, Shenoy discloses simple isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks. Shenoy, 2-3; Shealy, [208]; §VII.A.3. Thus, an ordinary artisan would have found it obvious to use Beach's self-aligned method of making Yoshida-Saxler's stacked gate structure in a GaN HEMT and use Shenoy's methods to undercut the gate electrode and create Yoshida-Saxler's horizontal ledges. Shealy, [209]." Pet.('347) 79-80.

305. However, as discussed in §VII.F, Shenoy discloses that the spread of the EMM to perform the undercutting is induced by an **underlying** insulator. EX1009, 1 ("the extent to which EMM must proceed before the underlying insulator is exposed… Once the insulator is exposed, metal dissolution continues in the lateral direction leading to a change in metal wall angle, χ.")

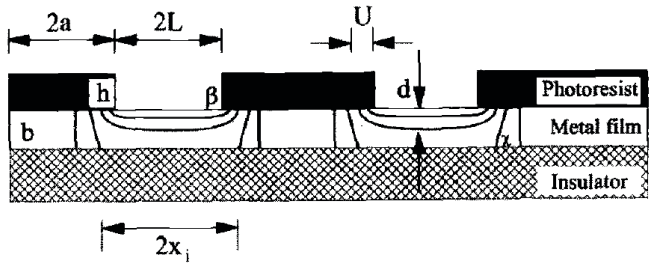
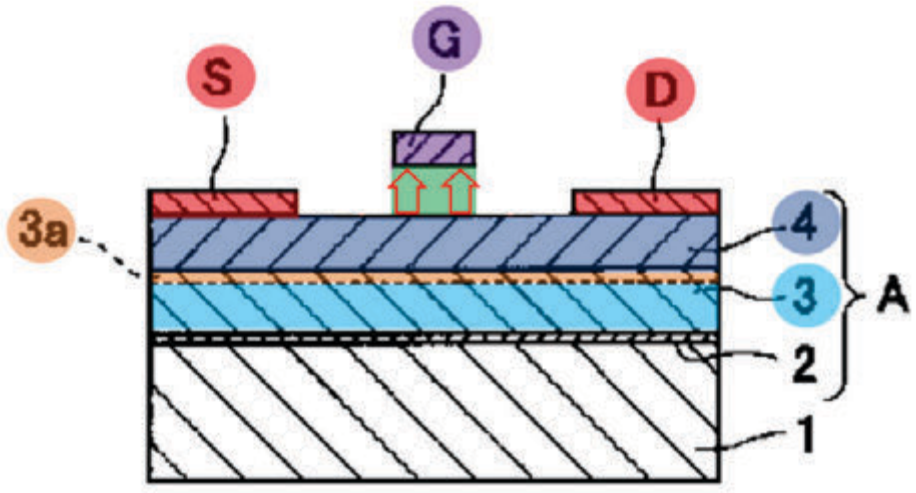


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

EX1009, Fig. 1

306. Comparing the proposed setup of Shenoy to the transistor of Saxler, the portion of the p-type GaN layer 5 in Yoshida (as pointed out below by the arrows in red) that would underlie the gate contact G and form the ledges would not have been etched by the self-aligned process of Beach.



Pet.('347) 73 (annotated)

307. Even accepting Dr. Shealy's reasoning (which I disagree with), the surfaces of the p-type GaN layer 5 underlying the gate metal G would still "have holes" because it would not have not been etched (EX2004, 99:4-13) and thus not act as an insulator. Therefore, the surface of the p-type GaN layer 5 underlying the gate metal G would be etched along with the gate contact G in the etching process of Shenoy, and thus not be retained as ledges.

308. Therefore, in addition to Beach, Shenoy undercuts Petitioner's motivation in "making Yoshida-Saxler's stacked gate structure." **Pet.('347)** 79. Applying the etching of Shenoy would etch at least the surfaces of p-type GaN layer 5 underlying the gate contact G that Ptitioner relies on for the ledges. Thus, applying the method of Shenoy would not produce Petitioner's "Yoshida-Saxler's stacked gate structure.

309. For at least these reasons, a POSA would not use Shenoy's "mathematical model" and apply it to Yoshida-Saxler. What would happen is unpredictable. Shenoy's etching process is not a selective etching with the exclusion of perfect insulators. A POSA would realize that the etching process would proceed downward (rather than sideways). The POSA would have no guidance with respect to the electrochemical etching process. Shenoy is silent on the chemistry

employed and Saxler do not employ an electrochemical etching process.

310. Shenoy reports that the etching process is "isotropic." If we trust this disclosure, then the etching process proceeds in all directions at the same rate absent an insulator, and the GaN materials below the metal would be etched as well. So, purely based on Shenoy's "mathematical model" and "isotropic" teachings, the process proposed by Petitioner would not produce the results desired by Petitioner.

H. A POSA would not have found it obvious to combine Yoshida, Saxler, Beach, and Shenoy

311. For the same reasons as discussed in §VIII.G, a POSA would not have found it obvious to modify Yoshida, Saxler, Beach, and Shenoy.

XII. Ground 5 (Claims 1-3) of the '347 Patent - Yoshida in view of Ahn

A. Overview

312. In Ground 5, Petitioner attempts to reverse engineer Yoshida similar to Ground 4, but relies on the method of Ahn instead of Beach and Shenoy. This is improper for at least the reasons provided in §XI.

313. [Reserved]

314. Furthermore, according to Petitioner, Yoshida's gate structure is already aligned on the p-type GaN material, i.e. forming symmetrical ledges on opposing sides. Ex2007(347) 83 ("these ledges are symmetric on either side of the gate metal").

315. Thus, I respectfully disagree that a POSA would look to another method "to improve alignment and precision" and "to improve alignment and symmetry between layers" of the gate electrode on the p-type GaN material when, according to Petitioner, the ledges of the p-type GaN material are already "symmetric on either side of the gate metal." Ex2007(347) 83

316. Yoshida is a "gate-last" process, Ahn is a "gate-first" process. A POSA would not

have looked to a "gate-last" process to modify a gate first process. Furthermore, the gate structure of Ahn has no relevance to that of Yoshida as discussed in §X.D with respect to Saxler.

B. Neither Petitioner nor Yoshida characterizes Yoshida's method as being "flexible" as relied on by the Board

317. As further addressed in §XI.B, the Board is mistaken in referring to "Yoshida's flexible method." Institution 50. Yoshida does not describe its method as being flexible, nor does Petitioner characterize it as such.

318. Yoshida actually distinguishes the process from forming the gate structure with "conventional photolithography and etching" in that the transistors produced by those "conventional" methods "cannot be said to have sufficient electron mobility to meet recent demands for still higher speed operations." EX1006, 6, 8.

319. Yoshida provides specificity to its method in order (as acknowledged by Dr. Shealy) and processes. EX1006 ¶¶17-23; EX1003 ¶204. Due to this specificity in order and processes, a POSA would recognize that Yoshida's method is not flexible.

320. Indeed, Yoshida directly contradicts Petitioner's statement that "a POSITA would have known many ways to create Yoshida's… structure and would have used these methods interchangeable" by expressly distinguishing from "conventional photolithography and etching." EX1006 ¶¶6, 8.

321. As further discussed herein, the process of Yoshida is specifically intended to design a transistor with a pn junction of a p-type GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility." EX1006 ¶17.

322. This configuration and functionality are not produced by the methods relied on by Petitioner, specifically Ahn, that are directed to producing completely different transistor configurations as discussed herein.

323. For at least these reasons, Petitioner's reengineering of Yoshida's method in Ground 5 in an attempt to produce other ways of "trying to accomplish" (EX2004, 38:3-5) the claimed invention is improper.

C. Yoshida teaches away from using other methods of manufacturing its gate

324. As addressed in §XI.C, Yoshida teaches away from using other methods of manufacturing its gate.

D. A POSITA would have no reason to form ledges on Yoshida after aligning the gate metal on the p-type GaN material

325. As addressed in §XI.D, a POSA would not perform an additional etching step to form ledges even assuming that a POSA would perform a first self-aligning step in etching both layers.

E. A POSA would not modify Yoshida with horizontally extending sidewalls

326. As addressed in §XI.E, a POSA would not modify Yoshida with horizontally extending side walls.

F. Yoshida teaches away from using other methods of manufacturing its gate

327. As addressed in §XI.B-C, Yoshida teaches away from "conventional" etching techniques.

G. A POSA would have no motivation to modify the method of Yoshida based on Ahn

328. Petitioner begins its analysis based on a faulty premise that Yoshida has a centrally

aligned gate electrode based on Fig. 1

329. Similar to Grounds 1-4, Petitioner attempts to reverse engineer Fig. 1 of Yoshida in Ground 5. More specifically, Petitioner alleges "using Ahn's techniques to create Yoshida's gate structure would lead to the following device, which is substantially the same as Yoshida's original device but with the widths W1 and W2 and inclined sidewalls of Ahn's device. Shealy, [240]." Pet.('347) 97.

330. Indeed, Petitioner relies heavily on what is shown in the schematic of Fig. 1 in Yoshida, while also discrediting transistor schematics of Fig. 1 in Yoshida, as not being valid. Pet.('347) 90-91; EX2004, 53:13; 53:23-57:1, 60:17-18, 81,16-19; 90:25-91:1; EX1007 ¶42.

331. Specifically, Petitioner alleges "though Yoshida draws substantially vertical sidewalls of p-type layer 5, a POSITA would have known a sidewall drawn vertically would have a slight slope when built in a practical device. Id. A POSITA would have been familiar with this principle. Shealy, [204] (citing Saxler, [0042]; Uemoto, Figs. 1-2, 5)." Petitioner doubles down on that statement, asserting that "any constructed embodiment [of a p-type GaN material] would <u>necessarily</u> extend at least slightly on the bottom due to manufacturing tolerances" although they are most commonly illustrated in patent drawings as a rectangle. Pet.('347) 67-68, 75; EX2004, 90:25-91:1. As also in ¶42, Saxler discloses "the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region of a device" which a POSA would understand is in accordance with the principle relied on by Petitioner.

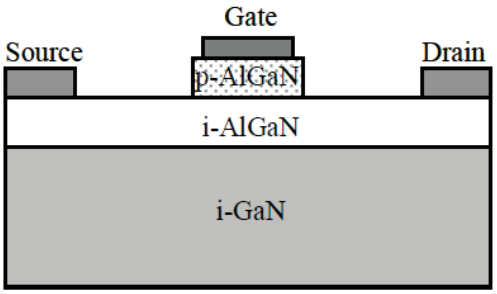
332. Furthermore, in his deposition, Dr. Shealy specifically stated that "the vertical scale of these diagrams is exaggerated, so you could see details of the epitaxial layer." EX2004, 56:26-57:1. Dr. Shealy's statement was with reference to Saxler, but would also apply to Yoshida where Fig. 1 illustrates the barrier layer (4) as having about the same width as the underlying channel

layer (3), while disclosing that the channel layer (3) is 10 times the thickness of the barrier layer (4). EX1006 ¶21. Furthermore, Dr. Shealy stated that "Figure 1 doesn't appear like what's described in 23, because the SiO2 isn't shown there. And it obviously was removed to get to that figure." 90:25-91:1

333. Thus, Dr. Shealy and Petitioner substantially discredit the schematics of Fig. 1 in Yoshida for being inaccurate and unreliable. At the same time, Petitioner bases its invalidity position on the premise that Yoshida's schematics can be relied on for the exact centering of the gate contact G in Fig. 1 for reverse engineering Yoshida. This feature is conveniently the aspect of Yoshida that Petitioner needs in "trying to accomplish" the claimed invention.

334. Furthermore, Petitioner relies on Uemoto "as another example, a 2006 IEEE paper on a GaN HEMT with a similar gate structure to Yoshida depicts its p-AlGaN gate layer having vertical sidewalls in its drawings (Fig. 1) but shows sloped sidewalls extending horizontally towards source and drain contacts in a microscope image of a device built according to the drawings." Pet.('347) 76.

335. Similar to Yoshida, Uemoto also shows in the schematic of Fig. 1 that the gate contact is centered on the p-type material. On the other hand, the microscope image of Fig. 5 provides evidence of a substantial offset in the device built according to the drawings.

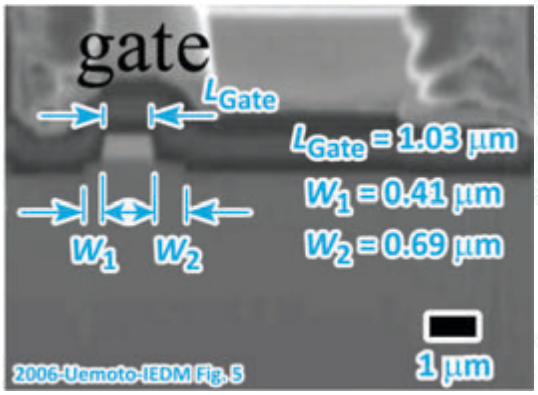


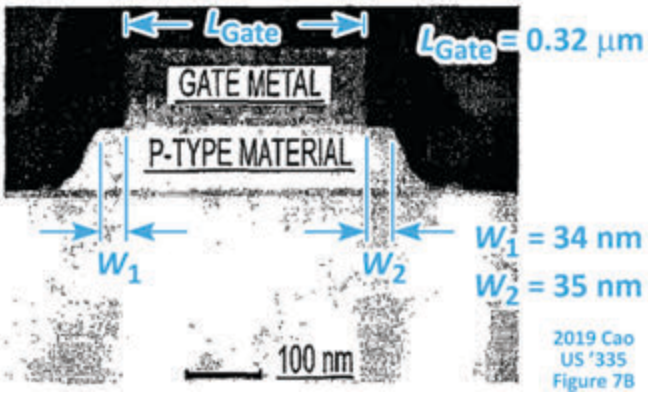
EX1020, Fig. 1

Pet.('347) 92 (EX1020, Fig. 5 annotated)

336. Analysis of the image of Uemoto (as below left) reveals that the difference between

the lengths of the ledges is about 68% which is in contrast to the image of Fig. 7B in the '357 patent that shows about a 3% difference.





EX1020, Fig. 5 (annotated) **The '347 Patent, Fig. 7B (annotated)**

337. Thus, I agree with Dr. Shealy that the gate of Uemoto does not have "substantially equal ledges" when in fact the transistor is schematically shown with the gate metal being in direct alignment with a central axis of the underlying layer. Pet.('347) 76-77; EX2004, 94:5-22. In contrast, the present patent has clear support for "substantially equal ledges."

338. For at least these reasons, Fig. 1 of Yoshida cannot be relied upon to show central alignment of the gate contact.

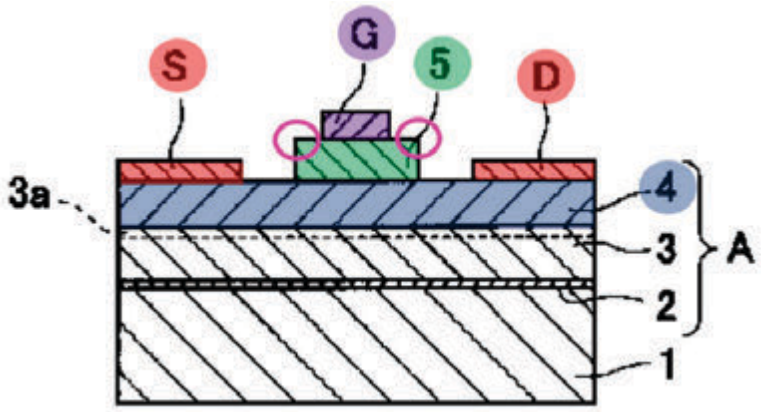
339. Petitioner fails to provide specifics on how the proposed method would actually be performed. Importantly, as discussed in §VIII.G, Petitioner has not provided a fabrication process sequence, neither in a narrative, nor in a pictorial manner. I do not know the specific fabrication sequence Petitioner is envisioning. That fabrication process sequence should follow from the prior art and meet the claim limitations of the challenged patent.

340. Petitioner contradicts its own positions. Petitioner asserts that a POSA would be motivated to modify Yoshida in order "to improve alignment and precision" (Pet.('347) 98) and "to improve alignment and symmetry between layers" (Pet.('347) 99).

341. However, according to Petitioner, Yoshida's gate structure is already aligned on the

p-type GaN material, i.e. forming symmetrical ledges on opposing sides. Ex2007(347) (other Petition) 83.

342. More specifically, Petitioner asserts that "Yoshida's gate electrode is narrower than layer 5, thereby exposing horizontal ledges that extend past the respective sidewalls of the gate electrode and toward the source and drain. Yoshida, [0022]-[0023], Fig. 1; Shealy, [214]. **These ledges are symmetric on either side of the gate metal** (i.e., having substantially equal widths). Yoshida, Fig. 1; Shealy, [214]. Yoshida thus discloses this element (Ground 4)." EX2007(347) 83.



EX2007(347) 83 (annotating EX1006, Fig. 1)

343. Thus, I respectfully disagree that a POSA would look to another method "to improve alignment and precision" and "to improve alignment and symmetry between layers" of the gate electrode on the p-type GaN material when, according to Petitioner, the ledges of the p-type GaN material are already "symmetric on either side of the gate metal." EX2007(347) 83.

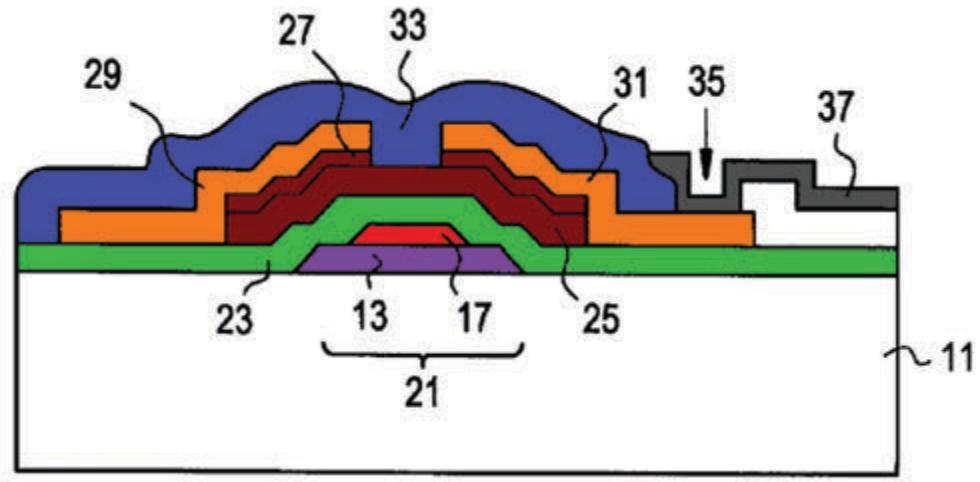
344. Petitioner's interpretation of Yoshida varies depending upon Petitioner's particular goal -- the ledges of Yoshida are either already "symmetric on either side of the gate metal" or Yoshida's process should be modified "to improve alignment and symmetry between layers." This vacillation provides further evidence of Petitioner's reliance on hindsight in "trying to

accomplish" the specific claimed invention.

345. Ahn teaches a substantially different gate structure from Yoshida solving an unrelated problem and different etching methods.

346. As addresses in §§VII.E, X.D, the thin film transistor of Ahn would not provide sufficient reason to modify Yoshida.

347. Ahn is directed to a thin film transistor having a double-layer metal gate structure to prevent deterioration of a thin overlying gate oxide layer 23 to avoid a short circuit with vertically aligned source and drain electrodes 29, 31. A thin film transistor is a special type of FET where the transistor is made by a specific thin film deposition, diverging from GaN HEMTs.

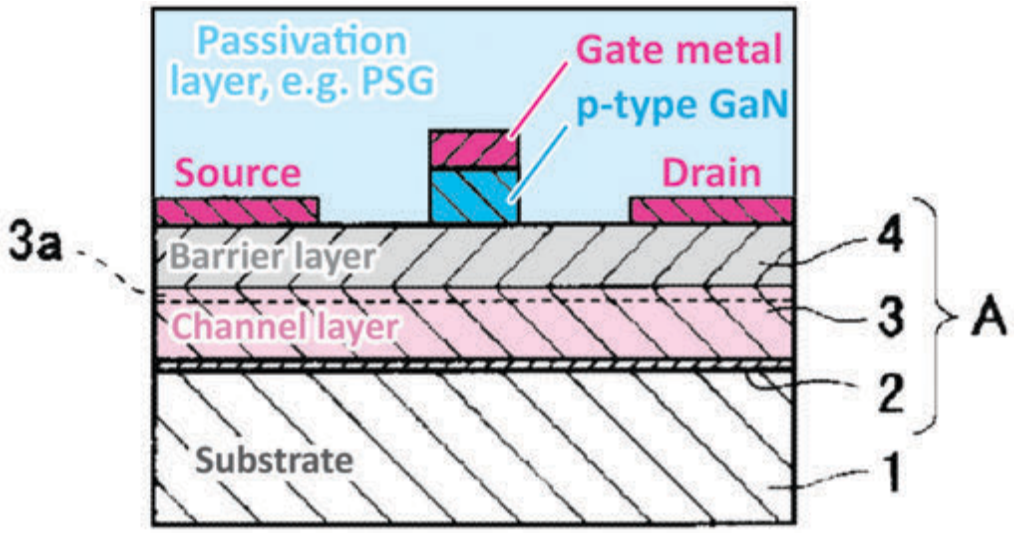


EX1010, Fig. 1F (annotated)

348. Petitioner vaguely alleges that the structure of Ahn "improves performance and prevents deterioration." Pet.('347) 95. However, those improvements are not applicable to GaN HEMTs such as Yoshida, especially to the detriment of the voltage control. §VII.B.

349. Yoshida is not a thin film transistor nor have relevant analogous structure. Saxler does not have a thin gate oxide layer 23 separating the gate and the source and drain electrodes 29, 31. Furthermore, Yoshida does not disclose a gate structure of a double-layer metal structure.

350. For example, as similarly discussed with reference to Saxler, the source and drain of Yoshida do not overlap with the gate contact nor is the semi-conductive layer separated by a thin gate oxide layer from the gate contact, thus there is no concern in Yoshida for a short circuit as in Ahn (EX1010, 1:35-38). Rather, as Dr. Shealy states each of the components are laterally spaced apart by a sufficient distance to avoid a short circuit. EX2004, 65:15-18 (referencing another GaN transistor in Saxler). The 2DEG in Yoshida is formed underneath the gate structure, and not above as in Ahn. Any passivation layer in Yoshida above the gate is much thicker (e.g., 500 nm to 1,000 nm) than the gate oxide layer 23 of Ahn, and would also likely be a different material deposited in a different manner than the thin gate oxide layer 23 of Ahn.



EX1006, Fig. 1 (modified)

351. Thus, the deterioration of the thin gate oxide layer 23 of Ahn would not be of concern to Yoshida because Yoshida's structure is substantially divergent from thin film transistors. Therefore, a POSA would not modify the gate structure of Yoshida based on that of the thin film transistor of Ahn, especially to the detriment of the voltage control of Yoshida.

H. Petitioner provides no evidence that the slower rate of etching of the cap layer relative to the metal contact has the exact proportionality as that in Ahn to similarly etch such small dimensions precisely

352. In referencing the different etching rates, Ahn specifically discloses that the etching is successful in forming the double step structure "because of the etching material and metals used for the first and second metal layers of the gate" (EX1010, 7:23-24), where the first metal layer 43 is a conductive metal (Al, Cu, or Au), the second metal layer 45 is a refractory metal (Mo, Ta, or Co) (*Id*., 5:42-47), and the etching material is a mixture of phosphoric acid H3 PO4, acetic acid CH3 COOH and nitric acid HNO3 (*Id*., 7:21-23).

353. Merely stating "a POSITA would have understood that Yoshida's layer 5, which was a p-type doped semiconductor, would have had a slower rate of dissolution than its metallic gate contact" and found it obvious to use Ahn's approach" (Pet.('347) 98) does not provide sufficient "articulated reasoning with some rational underpinning" as required. Petitioner provides no "articulated reasoning" on the complex interactions of any known etching material with the specific doped semiconductor of the gate material of Saxler and the specific metals of the gate contact of Saxler, as required in the specific relative etching rates of the proposed modification in view of Ahn.

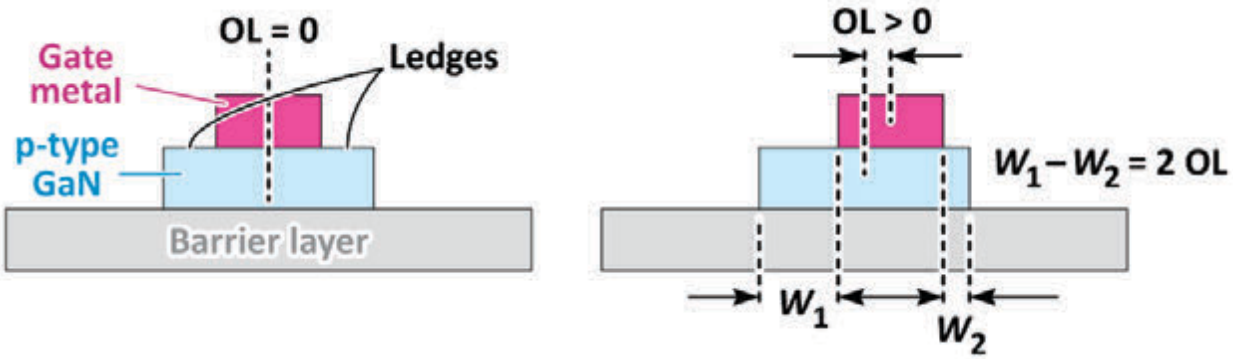
'335 Patent

XIII. Ground 1 (Claims 1-7) of the '335 Patent – Saxler in view of knowledge of a POSITA

A. Overview

354. Saxler precludes the claimed "pair of horizontal ledges" with "substantially equal widths." Saxler forms the gate cap layer **before** the source and drain contacts (see Saxler [0064]-[0066]). Accordingly, the two features (Saxler's cap layer and the gate contact) are fabricated by two different photolithographic processes. The two processes require that the narrow gate metal stripe be photolithographically aligned to the cap layer stripe (gate semiconductor material stripe). The two photolithography processes are subject to inherent and unavoidable "overlay deviations"

(OL). The gate contact and the associated gate semiconductor material ("cap layer") are both relatively narrow. For example, the gate length may be 1.0 µm or less (whereas the gate width can be, for example, 1,000 µm or more). As a consequence, the gate contact and the gate semiconductor material are subject to inherent and unavoidable overlay deviations that precludes "a pair of horizontal ledges" with "substantially equal widths." Specifically, the pair of ledges will have a difference in width that is equal to twice the overlay deviation. This is illustrated in the figure below. The overlay deviation ("OL deviation") directly translate into a width difference of the pair of horizontal ledges," that is, the difference in width is 2 x OL. The width difference of the ledges is not shown in the drawings of Saxler. This is not surprising since the "substantially equal width" ledges described in the '335 patent include nanometer ledge-widths differences that could not be depicted in patent drawings without an exploded view of the gate, annotated with dimensions.

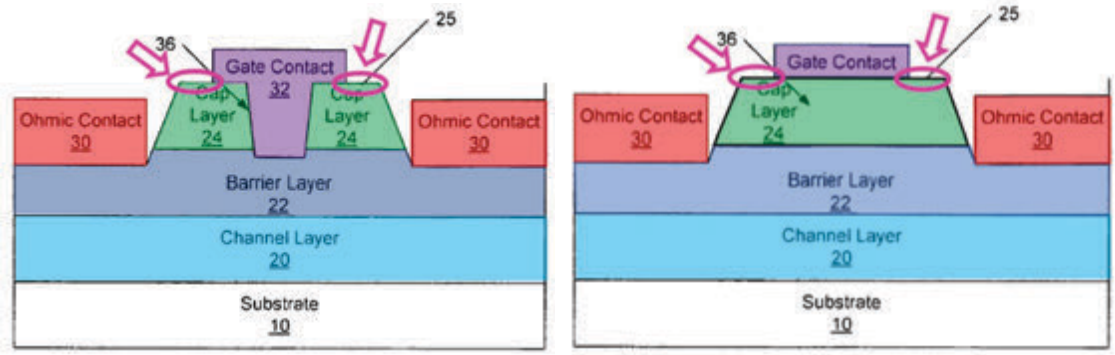


355. [Reserved]

B. Saxler does not disclose "substantially equal ledges"

356. Petitioner alleges "under Ground 1, Saxler depicts its gate contact is narrower than its cap layer, thereby exposing horizontal ledges with substantially equal widths that extend past the respective sidewalls of the gate and toward the source and drain, as shown in Figure 1A below.Saxler, Fig. 1A; Shealy, [132]-[133]… A POSITA would have understood Saxler's gate

contact in non-recessed embodiments (or embodiments where the recess did not extend through the cap layer) would similarly be narrower than the cap layer to expose the horizontal ledges. Shealy, [133]. Saxler thereby discloses or at least renders [1f] obvious (Ground 1).Id." Pet.('335)



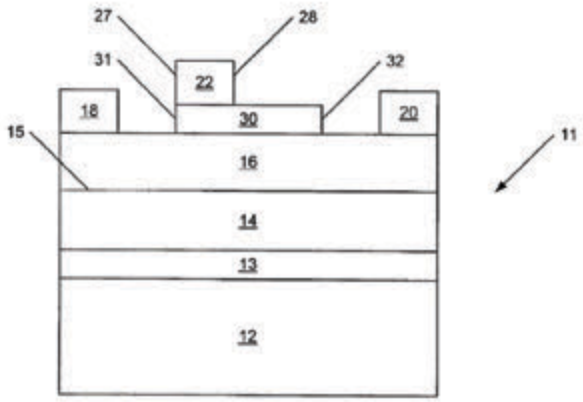
Pet.('335) 50

357. I respectfully disagree.

358. Saxler only discloses that the gate contact is offset of a central axis of the cap layer

359. Saxler does not provide any type of reasoning or valid disclosure that the gate electrode 32 should be centered on the cap layer 24 to produce "substantially equal ledges" as claimed.

360. The only disclosure in Saxler of the relative position of the gate electrode on the cap layer is that "**the recess may be offset** between the source and drain contacts such that the recess, and subsequently **the gate contact 32, <u>is closer to the source contact than the drain contact</u>**." EX1007 ¶65. This offset positioning is further consistent with Smith, as expressly incorporated by reference and relied on by Petitioner. EX1007 ¶46. Smith explicitly discloses that the gate electrode is intentionally aligned or substantially aligned with the source-side of the source-side segment of the GaN cap segment 30, and if not "may be detrimental to the device." EX1015 ¶¶41-42.



EX1015, Fig. 3

361. [Reserved]

362. [Reserved]

363. Thus, Saxler does not provide any disclosure of the gate electrode being directly aligned with a central axis of the cap layer, but does provide disclosure of the gate electrode being intentionally "offset… closer to the source contact than the drain contact." EX1007 ¶65.

364. This intentional "offset" Saxler and Smith is directly inconsistent with Petitioner's reliance on the Saxler disclosing "substantially equal ledges." Petitioner disregards this disclosure and improperly relies only on the drawings of Saxler to support their position.

365. Saxler explicitly discloses that drawings are "schematics" and "their shapes are not intended to illustrate the precise shape of a region of a device."

366. As acknowledged by Petitioner, it is well known in the art that Fig. 1A, 1B of Saxler (and similar drawings of transistor structures) are not intended to, and cannot be relied upon, as showing the actual structure of a transistor with the geometric dimensions (and their rations) drawn to scale. Indeed, Saxler refers to the figures as a "schematic" throughout the disclosure. ¶¶31-36, 42, 52. More specifically, Saxler discloses that "the regions illustrated in the figures are schematic in nature and **their shapes are not intended to illustrate the precise shape of a region of a**

device." ¶[0042].

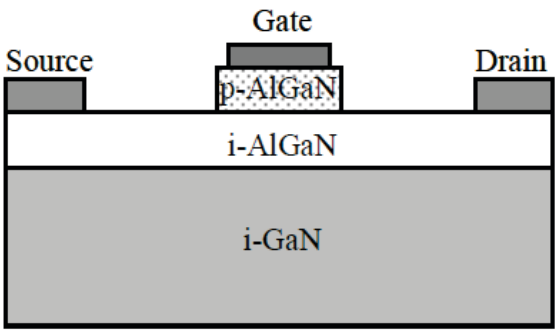
367. Petitioner selectively and inconsistently applies this "principle" of Saxler in paragraph [0042] that "shapes are not intended to illustrate the precise shape of a region of a device.". For example, Petitioner relies upon this principle in asserting that lines illustrated to be vertical are typically in fact not vertical. EX1007 ¶42 ("an etched region illustrated as a rectangle will, typically, have tapered, rounded or curved features.") Petitioner further asserts that "any constructed embodiment [of a p-type GaN material] would <u>necessarily</u> extend at least slightly on the bottom due to manufacturing tolerances" although they are most commonly illustrated in patent drawings as a rectangle. Pet.('335) 67-68, 75; EX2004, 90:25-91:1.

368. Furthermore, in his deposition, Dr. Shealy specifically conceded that "the vertical scale of these diagrams is exaggerated, so you could see details of the epitaxial layer." EX2004, 56:26-57:1. That is consistent with both Figs. 1A and 1B which show that the barrier layer 22 is about the same thickness as the channel layer 20 and the substrate 10, which would not be the case. Furthermore, Fig. 1B shows that the gate contact 32 is the same thickness which "would rarely be the case." EX2004, 60:17-18. Further with reference to Fig. 1B, Dr. Shealy states that "there's no way to place Ohmic contacts and butt them up against that cap layer with no gap in between, as shown." EX2004, 53:23-25. Dr. Shealy explicitly calls Fig. 1B of Saxler "a strange cartoon." EX2004, 53:13.

369. Thus, Dr. Shealy and Petitioner repeatedly discredit the schematics of Saxler as inaccurate. At the same time, Petitioner bases its primary obviousness argument on the premise that Saxler's schematics can be relied upon as disclosing ledges of "substantially equal widths" as claimed in the '335 patent. Petitioner cannot have it both ways, Petitioner later relies on microscopic images in Uemoto that disproves their reliance on the schematics in Saxler.

370. Petitioner later relies on Uemoto "as another example, a 2006 IEEE paper on a GaN HEMT with a similar gate structure to Yoshida depicts its p-AlGaN gate layer having vertical sidewalls in its drawings (Fig. 1) but shows sloped sidewalls extending horizontally towards source and drain contacts in a microscope image of a device built according to the drawings." Pet.('335) 76.

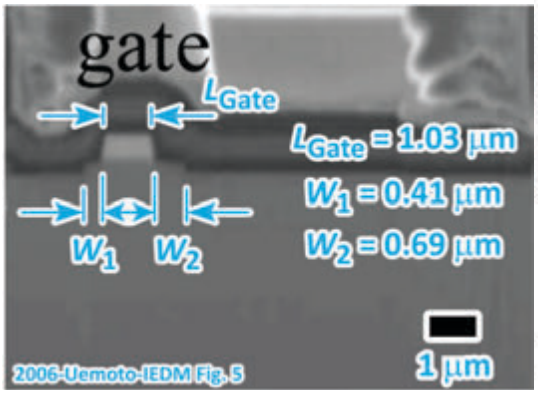
371. Similar to Saxler, Uemoto also shows in the schematic of Fig. 1 that the gate contact is centered on the p-type material. On the other hand, the microscopy image of Fig. 5 provides evidence of a substantial offset in the device built according to the drawings.

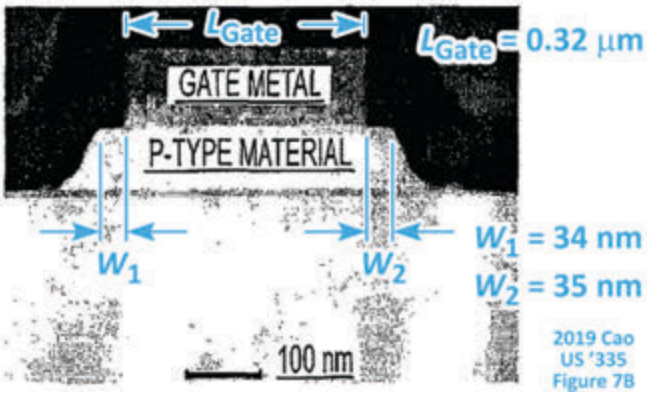


EX1020, Fig. 1

Pet.('335) 92 (EX1020, Fig. 5 annotated)

372. As shown in the image of Uemoto (below left), the difference between the lengths of the ledges is about 68% which is in contrast to the image of Fig. 7B in the '335 Patent that shows about a 3% difference.





EX1020, Fig. 5 (annotated) The '347 Patent, Fig. 7B (annotated)

373. Thus, I agree with Dr. Shealy that the gate of Uemoto does not have "substantially equal ledges" even though the transistor is schematically shown with the gate metal directly aligned with the central axis of the underlying layer. Pet.('335) 76-77; EX2004, 94:5-22.

374. Indeed, the gate alignment of the image in Uemoto is consistent with that of the actual disclosure in Saxler and Smith (as incorporated) in the gate electrode is offset of the p-type GaN material toward the source side. Further similar to Saxler, Uemoto is built according to the gate-last approach.

375. Therefore, the basic premise that Petitioner is relying on in the schematic of Fig. 1 in Saxler anticipating "substantially equal ledges" is not based on sound reasoning.

376. Furthermore, Petitioner does not provide any articulated reasoning with rationale underpinning that a POSA would be motivated to centrally align the gate metal on the underlying GaN material. Based on the actual disclosure of Saxler and Smith (as incorporated), if there was any intentional placement of the gate electrode relative to the GaN material, a POSA would offset the gate electrode toward the source-side of the GaN material and intentionally not form "substantially equal ledges" as claimed.

C. Saxler does not have "self-aligned" ledges

377. In the context of the '335 patent, the term "self-aligned" results in structural limitations of having ledges of equal or substantially equal widths. Saxler does not disclose "self-aligned" ledges.

378. [Reserved]

379. [Reserved]

380. [Reserved]

381. [Reserved]

382. [Reserved]

383. [Reserved]

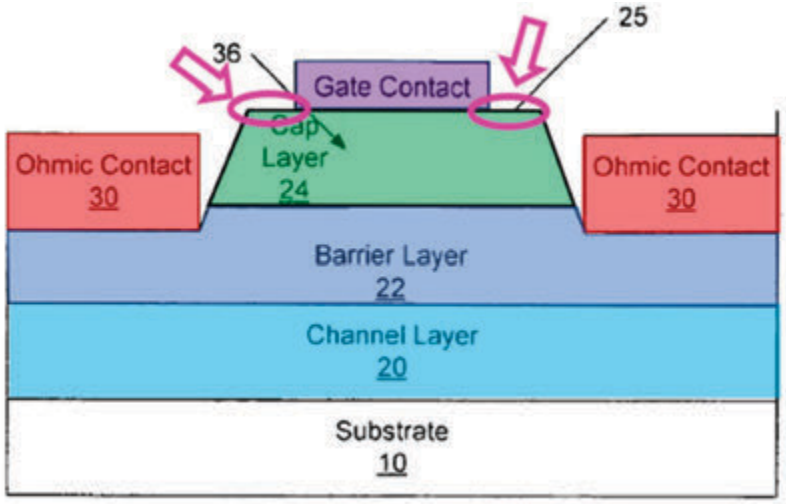
384. [Reserved]

385. [Reserved]

386. [Reserved]

D. Petitioner contradicts itself on whether the gate structure of Saxler is symmetric or not

387. In addressing Grounds 1 and 2, Petitioner alleges "these ledges are symmetric on either side of the gate" in relying on the Petitioner's hypothetical gate structure produced based on Saxler to address claims 1, 2, 5, and 7. Pet.('335) 51. However, in Ground 3, Petitioner attempts to reverse engineer Saxler to "improve… symmetry." Pet.('335) 61.



Pet.('335) 51

388. A POSA would not look to another method to "improve… symmetry" as in Ground 3 when, according to Petitioner, the gate structure of Saxler is already aligned with ledges of the p-type GaN being "symmetric on either side of the gate metal" as in Grounds 1 and 2.Ex2007 83. Thus, the motivation is insufficient.

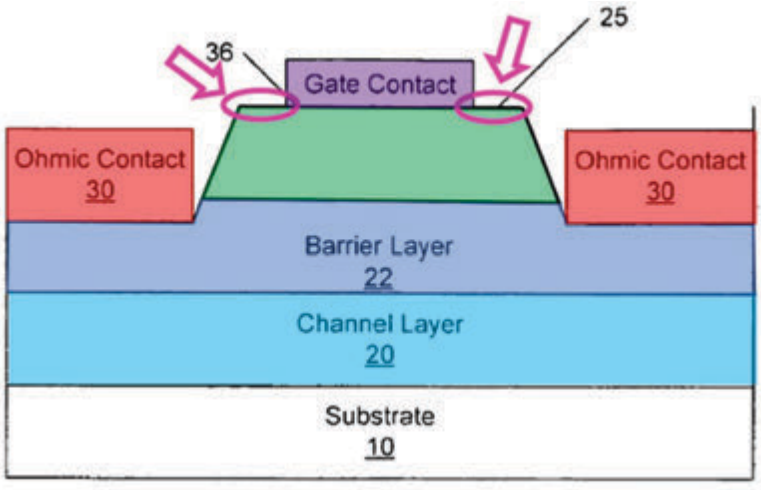
389. It should be readily apparent that Petitioner is picking and choosing its

interpretation of Saxler in whether the gate of Saxler is "symmetric" or whether Petitioner wants to reverse engineer Saxler for "more… symmetry."

390. This provides further evidence of Petitioner relying on hindsight in "trying to accomplish" the specific claimed invention.

E. A POSA would not consider the gate recess of Saxler as "optional"

391. Petitioner alleges "Saxler's gate contact may be recessed or nonrecessed (i.e., flat). Saxler, [0052], [0066]… Where the gate recess is not utilized, Saxler has the following structure. Shealy, [091]." Pet.('335) 25-26.



Pet.('335) 26

392. For the same reasons as discussed in §VIII.B, the relied on modified non-recessed embodiment is not disclosed by Saxler.

F. Petitioner's modification of Saxler does not produce an enhancement-mode transistor

393. Petitioner alleges that to the extent limiting, Saxler discloses or renders obvious the preamble. Shealy, [108]-[109]. Saxler discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer. Saxler, [0007]-[0010], [0046], [0059]-[0064], Figs. 1A, 1B; Shealy, [108]. This constitutes a normally-off enhancement-

mode GaN transistor when the cap is doped p-type. Shealy, [108]." Pet.('335) 35.

394. For the same reasons as discussed in §VIII.C, Petitioner's proposed transistor would not be an enhancement-mode transistor.

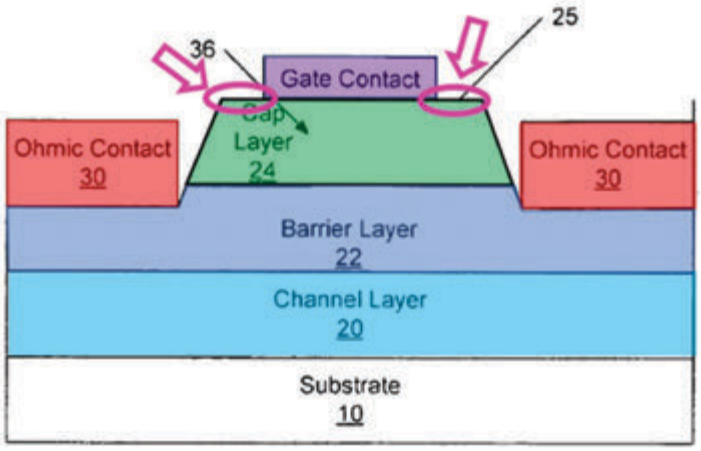
XIV. Ground 2 (Claims 1-7) of the '335 Patent – Saxler in view of Yoshida

A. Overview

395. Petitioner attempts to apply the same logic as Ground 1, but relies on Yoshida for its non-recessed gate structure. However, Saxler already discloses a non-recessed embodiment. Petitioner provides no reason why a POSA would be motivated by Yoshida to modify Saxler's recessed embodiment to eliminate the recessed gate contact. Thus, as further addressed in §IX, a POSA would not modify Saxler based on Yoshida to arrive at the claimed invention.

B. Saxler in view of Yoshida does not disclose "substantially equal ledges"

396. Petitioner alleges "Saxler in view of Yoshida also renders obvious [1f] (Ground 2). Shealy, [134]. Saxler-Yoshida's gate contact is narrower than its cap layer, thereby exposing horizontal ledges that extend past the respective sidewalls of the gate and toward the source and drain. Yoshida, [0022]-[0023], Fig. 1; Saxler, [0046], Figs. 1A-1F; Shealy, [134]. These ledges are symmetric on either side of the gate (i.e., having substantially equal widths). Shealy, [134]." Pet.('335) 50-51.



Pet.('335) 51

397. Petitioner is relying on the same modified figure as Ground 1. POSA would understand that the hypothetical schematic does not provide support for "substantially equal ledges" for the same reasons as discussed in §XIII.B.

C. Saxler in view of Yoshida does not disclose "self-aligned" ledges

398. Petitioner jointly addresses claim 2 and element [5f] for Grounds 1 and 2. Pet.('335) 51, 54. Thus, Ground 2 are additionally improper with respect to claim 2 and element [5f] for at least the reasons provided in §XIII.C.

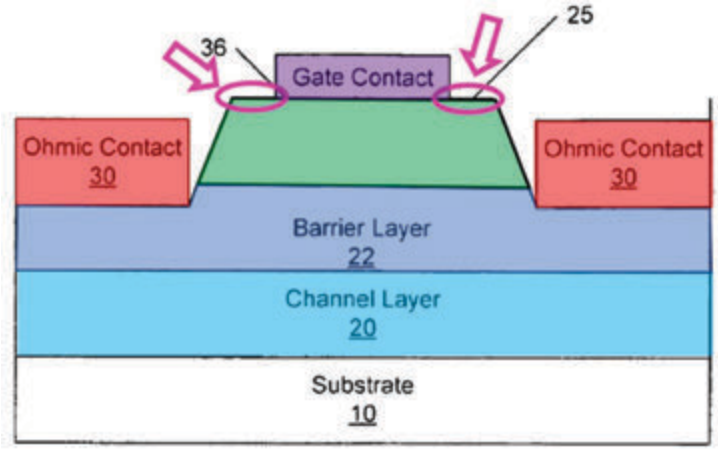
D. Petitioner contradicts themselves on whether the gate structure of Saxler is symmetric or not

399. In addressing Grounds 1 and 2, Petitioner alleges "these ledges are symmetric on either side of the gate" in relying on the Petitioner's hypothetical gate structure produced based on Saxler to address claims 1, 2, 5, and 7. Pet.('347) 51. However, in Ground 3, Petitioner attempts to reverse engineer Saxler to "improve… symmetry." Pet.('335) 61.

400. Thus, as discussed in §XIII.D, this provides further evidence of Petitioner relying on hindsight in "trying to accomplish" the specific claimed invention.

E. A POSA would not modify the recessed embodiment of Saxler by removing the recess based on Yoshida

401. Petitioner alleges "implementing Yoshida's non-recessed gate in Saxler's stacked gate structure results in the following combined structure. Shealy, [095]. Note that this results in the same arrangement as Saxler's non-recessed embodiment:" Pet.('335) 28.



Pet.('335) 29

402. For the same reasons as discussed in §VIII.B, POSA would not modify the recessed embodiment of Saxler by removing the recess based on Yoshida.

F. Petitioner's modification of Saxler does not result in an enhancement-mode transistor

403. Petitioner jointly addresses element [1p] for Grounds 1 and 2. Pet.('335) 34. Thus, element [1p] is additionally improper for at least the reasons provided in §VIII.C.

XV. Ground 3 (Claims 2 and 5-7) of the '335 Patent – Saxler in view of Yoshida, Beach, and Shenoy

A. Overview

404. Instead of relying on Saxler's own disclosed method, Petitioner attempts to improperly reverse engineer Saxler-Yoshida based on Beach and Shenoy. However, that is improper as I address in §§VIII-IX.

B. A POSA would not modify the recessed embodiment of Saxler by removing the recess based on Yoshida

405. Petitioner relies on the same rationale of modifying Saxler based on Yoshida, as in Grounds 1 and 2. Pet.('335) 65-67. Thus, Ground 3 is improper for at least the reasons provided in §§VIII.B, IX.B.

406. [Reserved]

407. [Reserved]

408. [Reserved]

C. The "self-aligned" technique of *Beach* would not produce the sloped sidewalls of Saxler-Yoshida, as relied on by Petitioner

409. For the same reasons as addressed in §§VIII.E, IX.D, a POSA would not modify Saxler-Yoshida based on Beach to arrive at the claimed invention.

D. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner's reasoning

410. For the same reasons as addressed in §§VIII.F, IX.E, a POSA would not modify Saxler-Yoshida based on Shenoy to arrive at the claimed invention.

E. A POSA would not have found it obvious to combine Saxler, Yoshida, Beach, and Shenoy

411. For the same reasons as discussed in §§VIII.G, IX.F, as POSA would not have found it obvious to combine Saxler, Yoshida, Beach, and Shenoy.

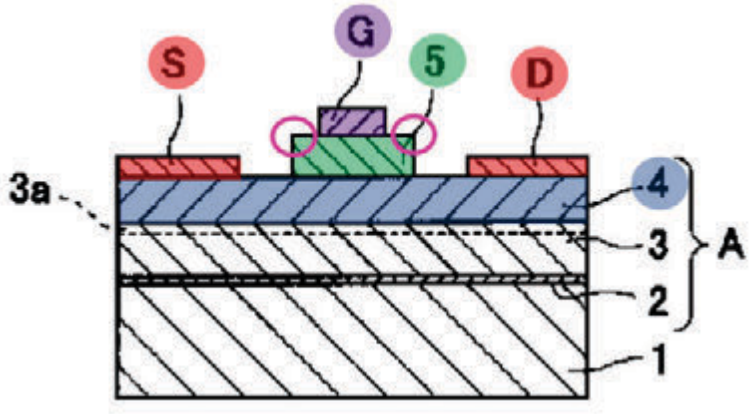
XVI. Ground 4 (Claims 1-7) of the '335 Patent – Yoshida in view of knowledge of a POSITA

A. Overview

412. As in Ground 1, Petitioner again improperly relies heavily on prior art transistor schematics that are not drawn to scale and do not represent an actual transistor with geometrical dimensions (and their ratios) drawn to scale. The figures do not disclose the claimed "substantially equal ledges." As I explain below, a gate contact cannot be aligned onto a p-type GaN gate material with "substantially equal ledges" using the two-mask approach of the prior art. Thus, the prior art gates would not have "self-aligned" ledges, nor does Petitioner properly address this feature.

B. Yoshida does not disclose "substantially equal ledges"

413. Petitioner alleges "Yoshida's gate electrode is narrower than layer 5, thereby exposing horizontal ledges that extend past the respective sidewalls of the gate electrode and toward the source and drain. Yoshida, [0022]-[0023], Fig. 1; Shealy, [214]. These ledges are symmetric on either side of the gate metal (i.e., having substantially equal widths). Yoshida, Fig. 1; Shealy, [214]. Yoshida thus discloses this element (Ground 4)." Pet.('335) 83.



Pet.('335) 83

414. As discussed in §XIII.B, Petitioner is improperly relying on transistor schematics for an actual transistor with geometrical dimensions (and their ratios) drawn to scale. As acknowledged by Petitioner, it is well known in the art that transistor schematics cannot be relied on for showing the actual structure of a transistor with geometrical dimensions (and their ratios) drawn to scale. Pet.('335) 75-77. Indeed, Petitioner applies a "principle" from Saxler that you cannot rely on the schematics of Yoshida for geometrical dimensions (and their ratios) drawn to scale of a transistor. *Id* (citing Saxler ¶42). Petitioner selectively and inconsistently applies this "principle" from Saxler to Yoshida.

415. Dr. Shealy and Petitioner repeatedly discredit transistor schematics for being inaccurate. Pet.('335) 90-91; EX2004, 53:13, 53:16-25, 56:24-57:1, 60:17-18, 82:16-19. Indeed,

Petitioner alleges that "figure 1 doesn't appear like what's described in 23, because the SiO2 isn't shown there. And it obviously was removed to get to that figure." EX2004, 82:16-19. At the same time, Petitioner bases its invalidity position on the unreasonable premise that the only features that Petitioner alleges are accurate are the exact features that Petitioner needs for their position.

C. Petitioner's contradicts its own positions

416. Petitioner explicitly alleges that Fig. 1 of Yoshida discloses ledges that "are symmetric on either side of the gate metal… Yoshida thus discloses [1f]." However, in Ground 5 of IPR2023-01382 as discussed in §XII, Petitioner attempts to modify Yoshida by producing the gate structure with a self-aligning method "to improve alignment and symmetry between layers." Ex2007(335) 98.

417. Thus, Petitioner is inconsistent in whether the gate structure of Yoshida has ledges that "are symmetric on either side of the gate metal." If the gate structure of Yoshida is already produced with ledges that "are symmetric on either side of the gate metal," a POSA would not have any motivation to modify Yoshida with a self-aligned method "to improve alignment and symmetry between layers" as alleged in the related proceeding.

D. Yoshida does not have "self-aligned" ledges

418. In the context of the '335 patent, the term "self-aligned" results in structural limitations of having ledges of equal or substantially equal widths. Yoshida does not disclose "self-aligned" ledges.

419. [Reserved]

E. A POSA would not have modified Yoshida with the sloped sidewalls of Saxler

420. Petitioner alleges "Yoshida renders obvious sloped sidewalls that extend

horizontally towards source and drain contacts if the claimed extension of the side surfaces is interpreted to include any amount extension beyond a perfectly vertical sidewall, as Patent Owner contends."

421. As addressed in §XI.E, a POSA would not find it obvious to modify Yoshida with sloped sidewalls.

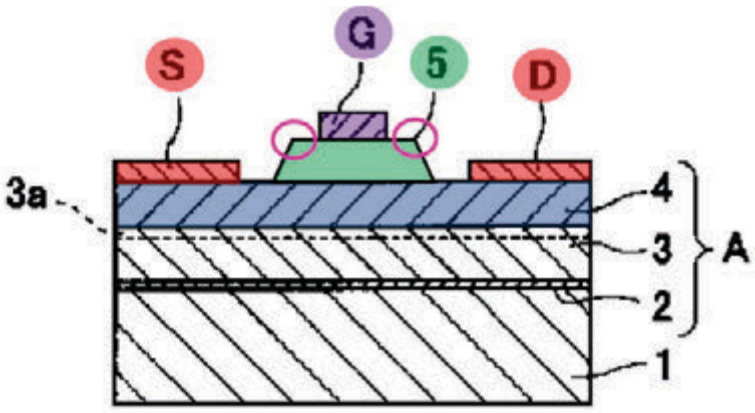
XVII. Ground 5 (Claims 1-7) of the '335 Patent – Yoshida in view of Saxler

A. Overview

422. Petitioner attempts to apply the same logic as Ground 4, but also attempts to apply sloped sidewalls from Saxler to Yoshida. This logic would be improper for at least the reasons as discussed in §XVI.

B. Yoshida does not disclose "substantially equal ledges"

423. Similar to Ground 4, Petitioners alleges "the combination of Yoshida and Saxler also renders obvious [1f] (Ground 5). Shealy, [215]." Pet.('335) 83.



Pet.('335) 83

424. Thus, Petitioner does not provide any additional reasoning in Ground 5, that is not in Ground 4. Therefore, Ground 5 is insufficient for at least the reasons provided for Ground 4 in §XVI.B.

425. In Ground 4, I note that Petitioners relies on the statement that "Yoshida thus discloses this element" in referring to the "substantially equal widths" [1f]. Pet.('335) 83.

426. On the other hand, Ground 5 states "the combination of Yoshida and Saxler also renders obvious [1f]." Pet.('335) 83. However, Petitioner does not provide any obviousness rational with respect to the "substantially equal widths" [1f]. Thus, the statement of "renders obvious" must refer to the modification of Yoshida with the tapered walls of Saxler as illustrated by Petitioner (Pet.('335) 83) and not be related to "substantially equal widths" [1f].

C. Petitioner's contradicts its own positions

427. Petitioner explicitly alleges that Fig. 1 of Yoshida discloses ledges that "are symmetric on either side of the gate metal… Yoshida thus discloses [1f]." However, in Ground 5 of IPR2023-01382 as discussed in §XII, Petitioner attempts to modify Yoshida by producing the gate structure with a self-aligning method "to improve alignment and symmetry between layers." Ex2007(335) 98.

428. Thus, Petitioner is inconsistent in whether the gate structure of Yoshida has ledges that "are symmetric on either side of the gate metal." If the gate structure of Yoshida is already produced with ledges that "are symmetric on either side of the gate metal," a POSA would not have any motivation to modify Yoshida with a self-aligned method "to improve alignment and symmetry between layers" as alleged in the related proceeding.

D. Yoshida does not have "self-aligned" ledges

429. In the context of the '335 patent, the term "self-aligned" results in structural limitations of having ledges of equal or substantially equal widths. Yoshida does not disclose "self-aligned" ledges.

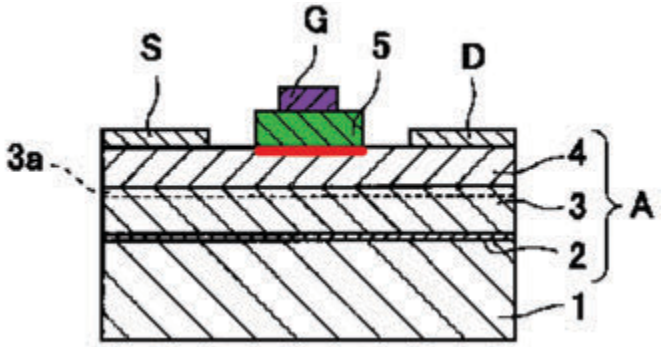
430. [Reserved]

E. A POSA would not have modified Yoshida with the sloped sidewalls of

Saxler

431. Petitioner alleges that "it would have been obvious to modify Yoshida's transistor with the sloped sidewalls of Saxler's capping layer to reduce gate leakage. Shealy, [185]-[189]. The combination calls for nothing more than the simple substitution of Saxler's sidewalls to predictably make an enhancement-mode GaN HEMT. Id. And a POSITA would have recognized Saxler's sidewalls would have reliably reduced Yoshida's gate leakage, making the combination obvious. Id."

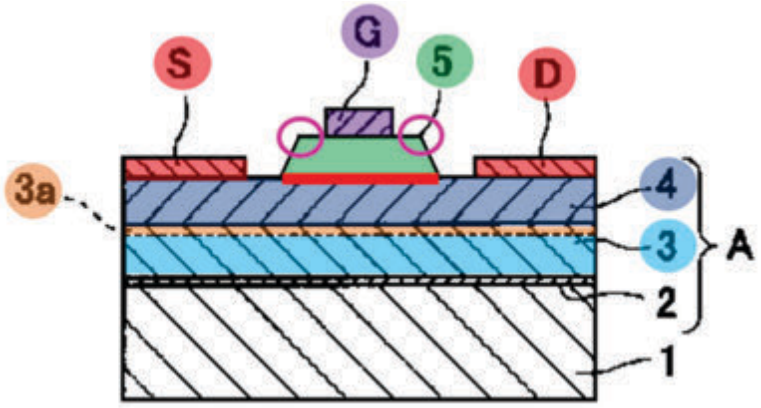
432. As discussed above in §§VII.B, XI.A-C, the transistor of Yoshida is formed by a specific process where the p-type GaN layer 5 is layered and "etch[ed] away… except for where the gate electrode was to be loaded" (prior to loading the gate electrode G). EX1006 ¶22. The transistor of Yoshida is assembled to position the pn junction of a p-type GaN layer 5 "immediately under" the gate electrode G for "voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels, such that the 2-dimensional electron gas layer 3a can be controlled at high voltage, increasing the trapping effect on electrons in the 2-dimensional electron gas layer 3a and allowing high-speed electron mobility." *Id.* ¶17.



EX1006, Figs. 1 (annotated)

433. Thus, Yoshida teaches away from adding the alleged sloped sidewalls of Saxler's capping layer to the p-type GaN layer 5 because doing so would intentionally widen the pn junction

relative to the gate electrode G creating misalignment, thus reducing "voltage control" by increasing the required amount of carrier injection and reducing high-speed electron mobility. Indeed, the tapered sidewalls added from Saxler would just provide excessive surface area that cannot receive the gate electrode G, contrary to the intentional shape of the p-type GaN layer 5 of Yoshida. EX1006 ¶22 ("etch[ed] away… except for where the gate electrode was to be loaded").

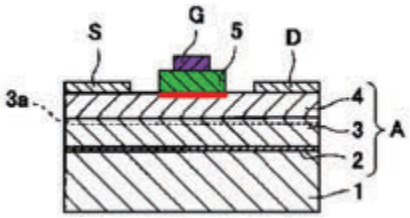


Pet.('335) 73 (annotated)

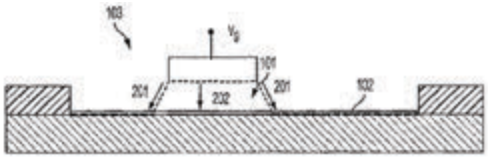
434. Furthermore, as discussed above in §§VII.A, VIII.C and addressed by Dr. Shealy, the recessed embodiment of Saxler as relied on by Petitioner is not an enhancement-mode transistor (EX1003 ¶146), thus does not provide any guidance on "predictably mak[ing] an enhancement-mode GaN HEMT" as relied on by Petitioner. The cap layer of Saxler extends substantially the entire width between the source and the drain (EX1007, Fig. 1A) while Yoshida intends to limit the width of its p-type GaN layer (EX1006 ¶22).

435. Petitioner cites additional prior art and Applicant's own specification. Pet.('335) 71. However, none of the references discloses an enhancement-mode GaN HEMT with <u>both</u> ledges and horizontally extending sidewalls. In other words, Yoshida arguably has ledges for loading the gate electrode but intends to limit the width of its p-type GaN layer (EX1006 ¶22) while Fig. 2 of the present application has horizontally extending sidewalls but no ledges (because it is self-aligned). A POSA would not apply the horizontally extending sidewalls of Fig. 2 to the

gate-last structure of Yoshida in forming both ledges and horizontally side walls because it would undesirably increase the PN junction reducing "voltage control" by increasing the required amount of carrier injection and reducing high-speed electron mobility. EX1006 ¶22.



EX1006, Figs. 1 (annotated)



The '347 Patent, Fig. 2

436. Thus, a POSA would not modify the gate-last enhancement-mode transistor of Yoshida with tapered sidewalls from the depletion-mode transistor of Saxler nor the self-aligned process from the present application. I believe any such modification would be based purely on hindsight.

437. A POSA would not modify Yoshida based on Saxler to arrive at the claimed invention.

XVIII. Ground 6 (Claims 2 and 5-7) of the '335 Patent – Yoshida in view of Saxler, Beach, and Shenoy

A. Overview

438. Instead of relying on Yoshida's own disclosed method, Petitioner attempts to improperly reverse engineer Yoshida-Saxler based on Beach and Shenoy. However, that is improper as I address in §§VIII, IX. Petitioner also mentions Ahn, which would still be improper as I address in §§X, XII.

B. The "self-aligned" technique of *Beach* would not produce the ledges of Yoshida-Saxler, as relied on by Petitioner

439. Petitioner alleges that "to the extent Patent Owner disagrees that the 'self-aligned' recitations of claims 2 and 5 are product-by-process elements that have no patentable weight

(§§VII.B (Claim Construction), X.D (Claim 2), X.G.7 ([5f])), the combination of Yoshida, Saxler, Beach, and Shenoy renders obvious claims 2 and 5-7. Shealy, [232]-[259]." Pet.('335) 88.

440. For the same reasons as addressed in §VIII.E, a POSA would not modify Saxler-Yoshida based on Beach to arrive at the claimed invention.

C. The mathematical model of Shenoy would not produce the intended structure by etching at least the underlying ledges based on Petitioner's reasoning

441. For the same reasons as addressed in §§VIII.F, IX.E, a POSA would not modify Yoshida-Saxler based on Shenoy to arrive at the claimed invention.

D. A POSA would not have found it obvious to combine Yoshida, Saxler, Beach, and Shenoy

442. For the same reasons as discussed in §§VIII.G, IX.F, as POSA would not have found it obvious to modify Yoshida, Saxler, Beach, and Shenoy.

I, E. Fred Schubert, do hereby declare and state, that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code and may jeopardize the validity of the application or any patent issuing thereon.

Executed on: June 18, 2024

Location: Billings, MT

By: