Filed: September 19, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD., AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01384
U.S. Patent 10,312,335

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT 10,312,335

TABLE OF CONTENTS

I. Introduction 1

II. Technological Background 2

III. The '335 Patent 8

A. Overview 8

1. The alleged invention 8

2. Self-aligned ledges 11

B. Prosecution History 13

1. Allowance of the '335 Patent 13

2. Priority claim 14

IV. Statement of Precise Relief Requested 16

A. Claims 16

B. Grounds 17

V. Statement of Facts 17

VI. Level of Ordinary Skill 18

VII. Claim Construction 18

A. "side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer" 19

B. "self-aligned" ledges 23

VIII. Grounds 1 and 2: *Saxler*, Alone (Ground 1) or in View of *Yoshida* (Ground 2) Renders Obvious Claims 1-7 24

A. Overview of Grounds 1 and 2 24

1. Ground 1: *Saxler* 25

2. *Yoshida* 27

3. Ground 2: The combination of *Saxler* in view of *Yoshida* 28

4. Ground 2: Motivation to Combine 29

B. Independent Claim 1 35

1. [1p] An enhancement-mode GaN transistor, comprising: 35

2. [1a] a GaN layer; 36

3. [1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 37

4. [1c]: a source contact and a drain contact formed on the barrier layer; 38

5. [1d]: a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and 39

6. [1e]: a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material, ... 45

7. [1f]: wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively. 48

C. [Claim 2]: wherein the pair of horizontal ledges of the p-type gate material are self-aligned. 51

D. [Claim 3]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN). 52

E. [Claim 4]: wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width 52

F. Independent Claim 5 52

1. [5p] An enhancement-mode GaN transistor, comprising:.....52

2. [5a] a GaN layer;.....53

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer; 53

4. [5c]: a source contact and a drain contact formed on the barrier layer;.....53

5. [5d]: a p-type gate material formed above the barrier layer and between the source and drain contacts;.....53

6. [5e]: a gate metal disposed on the p-type gate material,.....53

7. [5f]: wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and.....54

8. [5g]: (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer. 54

G. [Claim 6]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN).....55

H. [Claim 7]: wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.....55

IX. Ground 3: *Saxler* in View of *Yoshida*, *Beach*, and *Shenoy* Renders Obvious Claims 2 and 5-7 57

A. Overview of Ground 3.....57

1. *Beach* 57

2. *Shenoy* 58

3. Motivation to Combine 59

B. [Claim 2] 64

C. Independent Claim 5 65

1. [5p] 65

2. [5a] 65

3. [5b] 65

4. [5c] 65

5. [5d] 66

6. [5e] 66

7. [5f] 66

8. [5g] 66

D. [Claim 6] 66

E. [Claim 7] 67

X. Grounds 4 and 5: *Yoshida*, Either Alone or In View of *Saxler* Renders Obvious Claims 1-7 67

A. Ground 4: *Yoshida* Alone 67

B. Ground 5 68

1. Ground 5: The Combination of *Yoshida* in View of *Saxler* 68

2. Ground 5: Motivation to Combine 69

C. Independent Claim 1 71

1. [1p] 71

2. [1a] 72

3. [1b] 72

4. [1c] 74

5. [1d] 74

6. [1e] 81

7. [1f] 83

D. [Claim 2] 84

E. [Claim 3] 84

F. [Claim 4] 84

G. Independent Claim 5 85

1. [5p] 85

2. [5a] 85

3. [5b] 85

4. [5c] 85

5. [5d] 86

6. [5e] 86

7. [5f] 86

8. [5g] 87

H. [Claim 6] 87

I. [Claim 7] 87

XI. Ground 6: *Yoshida* in View of *Saxler*, *Beach*, and *Shenoy* Renders Obvious Claims 2 and 5-7 88

A. Overview of Ground 6 88

1. Motivation to Combine 88

B. [Claim 2] 92

C. Independent Claim 5 94

1. [5p] 94

2. [5a] 94

3. [5b] 95

4. [5c] 95

5. [5d] 95

6. [5e] 95

7. [5f] 95

8. [5g] 96

D. [Claim 6] 96

E. [Claim 7] 97

XII. Discretionary Denial Is Not Warranted 97

A. *Fintiv* Denial Is Improper 97

B. 35 U.S.C. § 325(d) Denial Is Improper 98

XIII. Mandatory Notices 98

A. Real Party-in-Interest 98

B. Related Matters 98

C. Lead and Back-Up Counsel 99

XIV. Grounds for Standing 101

XV. Conclusion 101

Table of Authorities

Page(s)

Cases

CUPP Comput. AS v. Trend Micro Inc.
53 F.4th 1376 (Fed. Cir. 2022) 18

Honeywell Int'l Inc. v. Universal Avionics Sys. Corp., 488 F.3d 982, 990
(Fed. Cir. 2007).....20

In re Thorpe
777 F.2d 695 (Fed. Cir. 1985) ..... passim

Intel Corp. v. PACT XXP Schweiz AG
61 F.4th 1373 (Fed. Cir. 2023) 33, 71

Kamstrup A/S v. Axioma Metering UAB
43 F.4th 1374 (Fed. Cir. 2022) ..... passim

KEYnetik, Inc. v. Samsung Elecs. Co.
837 F. App'x 786 (Fed. Cir. 2020) 20

KSR Int'l Co. v. Teleflex Inc.
550 U.S. 398 (2007)..... 33, 71

Phillips v. AWH Corp.
415 F.3d 1303 (Fed. Cir. 2005) 18

United Therapeutics Corp. v. Liquidia Techs., Inc.
74 F.4th 1360 (Fed. Cir. 2023) 24, 51, 54, 64

Statutes

35 U.S.C. § 102.....13

35 U.S.C. § 102(b) 16

35 U.S.C. § 103.....17

35 U.S.C. § 311.....16

35 U.S.C. § 325(d) 98

Regulations

37 C.F.R. § 42.100(b) 18

37 C.F.R. § 42.22(c).....17

TABLE OF EXHIBITS

Exhibit	Description
Ex. 1001	U.S. Patent No. 10,312,335 B2 to Cao et al. ("the '335 patent")
Ex. 1002	Prosecution History of the '335 patent
Ex. 1003	Declaration of Dr. James Richard Shealy ("Shealy")
Ex. 1004	Curriculum Vitae of Dr. James Richard Shealy
Ex. 1005	Japanese Patent Publication No. JP H11-261053 to Yoshida
Ex. 1006	Certified Translation of Japanese Patent Publication No. JP H11-261053 to Yoshida ("*Yoshida*")
Ex. 1007	U.S. Patent Application Publication No. US 2006/0108606 A1 to Saxler et al. ("*Saxler*")
Ex. 1008	U.S. Patent Application Publication No. US 2007/0007547 A1 to Beach ("*Beach*")
Ex. 1009	R.V. Shenoy and M. Datta, *Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*, 143 J. Electrochemical Soc'y, pp. 544-549 (1996) ("*Shenoy*")
Ex. 1010	U.S. Patent No. 5,905,274 to Ahn et al. ("*Ahn*")
Ex. 1011	U.S. Patent Application Publication No. US 2010/0258843 A1 to Lidow et al. ("*Lidow*")
Ex. 1012	U.S. Patent No. 9,748,347 to Cao et al. ("the '347 patent")
Ex. 1013	Prosecution History of the '347 patent
Ex. 1014	Chua Xu et al., *The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaN/GaN Heterostructure*, 28 IEEE Electron Device Letters, pp. 942-944 (2007) ("*Xu*")
Ex. 1015	U.S. Patent Application Publication No. US 2002/0066908 A1 to Smith ("*Smith*")

Exhibit	Description
Ex. 1016	U.S. Patent Application Publication No. US 2006/0273347 A1 to Hikita et al. ("*Hikita*")
Ex. 1017	U.S. Patent Application Publication No. US 2009/0072272 A1 to Suh et al. ("*Suh*")
Ex. 1018	X. Hu et al., *Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate*, 36 Electronics Letters, pp. 753-754 (2000) ("*Hu*")
Ex. 1019	U.S. Patent Application Publication No. US 2005/0087763 A1 to Kanda et al. ("*Kanda*")
Ex. 1020	Yasushiro Uemoto et al., *A Normally-off AlGaN/GaN Transistor with $R_{on}A=2.6\Omega cm^2$ and $BV_{ds}=640V$ Using Conductivity Modulation*, 2006 International Electron Devices Meeting, IEEE (2006) ("*Uemoto*")
Ex. 1021	U.S. Patent Application Publication No. US 2006/0019435 A1 to Sheppard et al. ("*Sheppard*")
Ex. 1022	Order Granting Defendants' Unopposed Motion for Stay Pending ITC Proceeding, Case No. 2:23-cv-04026-AB-AS, Central District of California (July 27, 2023)
Ex. 1023	Dietrich W. Widmann, *Metallization for Integrated Circuits Using a Lift-Off Technique*, 11 IEEE Journal of Solid-State Circuits, pp. 466-471 (1976) ("*Widmann*")
Ex. 1024	Reserved
Ex. 1025	Declaration of Kelley Hayes Greenhill
Ex. 1026	Declaration of Shauna Wiest
Ex. 1027	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 ("*Beach-II*")
Ex. 1028	Petitioner and Complainant's Proposed Claim Construction, ITC 337-TA-1366

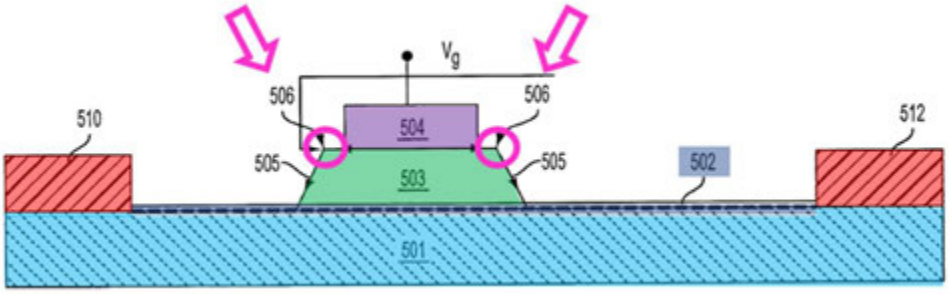
Exhibit	Description
Ex. 1029	C. S. Suh et al., "p-GaN/AlGaN/GaN Enhancement-Mode HEMTs, 2006 64th Device Research Conference, June 2006, pp. 163-164 ("Suh 2006")

*Emphasis added unless otherwise noted.

I. Introduction

Petitioner request *inter partes* review and cancellation of claims 1-7 of U.S. Patent No. 10,312,335 ("the '335 patent") (Ex. 1001).

Independent claims 1 and 5 describe a conventional enhancement-mode gallium nitride (GaN) high electron mobility transistor (HEMT) device, including a **GaN channel layer** below an **AlGaN barrier**. Ex. 1001, claims 1, 5. The claims require a stacked gate structure resting on the barrier layer between **source** and **drain electrodes**. *Id.* That gate structure has two layers: a **p-type gate material** with sloped sidewalls below an overlying **gate metal** contact and a two-dimensional electron gas (**2DEG**) formed when a current is applied to the gate metal. *Id.* The patent admits that ***all*** these features were conventional. Ex. 1001, 1:21-2:30, Figs. 1-2, 3A-3B; Shealy, [0044]-[0045].



Ex. 1001, Fig. 5.[1]

[1] All figures in this Petition containing color are annotated.

The claims also require that the width of the gate metal is less than the width of the top of p-type gate material, giving rise to a pair of horizontal **ledges** on the p-type gate material's surface to either side of the gate metal. Ex. 1001, claims 1, 5. These **ledges** are the '335 patent's sole point of alleged novelty. But such ledges were *also* well known and conventional, long found in the prior art. *Yoshida* (Ex. 1005; Ex. 1006), published in 1999, shows such ledges in a gate structure of a GaN HEMT consisting of a gate metal stacked on a p-type GaN material (*Yoshida*, Fig. 1). So does *Hu* (Ex. 1018), published in 2000 (*e.g.*, *Hu*, Fig. 1); *Smith* (Ex. 1015), published in 2002 (*e.g.*, *Smith*, Fig. 3); *Saxler* (Ex. 1007), published in 2006 (*e.g.*, *Saxler*, Figs. 1A, 2B, [0052]); and *Suh* (Ex. 1017), published in 2009 (*e.g.*, *Suh*, Fig. 6).

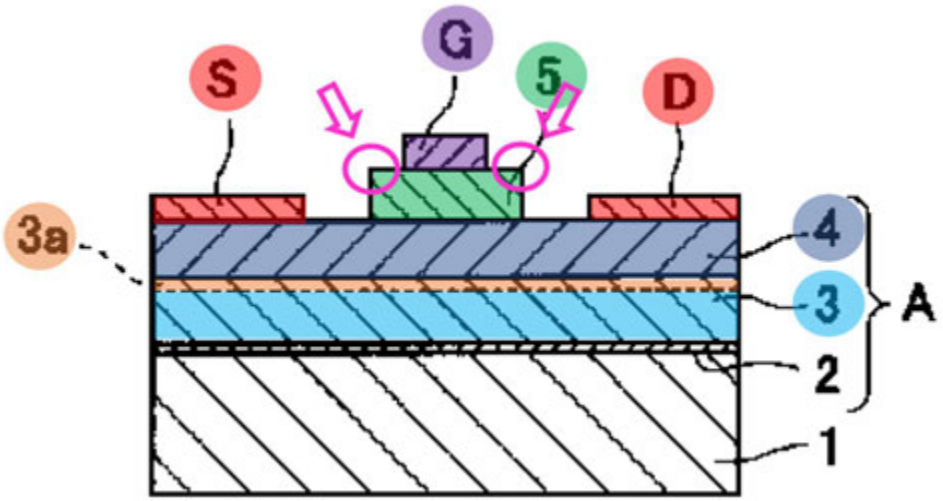
II. Technological Background

GaN power transistors have a large band gap, which drives up breakdown voltage and makes them attractive for high power applications. Ex. 1001, 1:30-49; Shealy, [055]. They were well known long before the '335 patent. *E.g.*, *Smith*, [0004]-[0010] (discussing "well known" features of GaN HEMT devices). Conventional features of such transistors include a **GaN channel** and **AlGaN barrier** layers, at the heterojunction of which a **two-dimensional electron gas (2DEG) region** forms, as well as **source** and **drain electrodes**, and a gate structure

including **GaN gate materials** under a **gate metal**. Ex. 1001, 1:28-2:26; *Yoshida*, Abstract; *Suh*, [0002]-[0005], [0015], Figs. 1, 6-7; Shealy, [055]].

Enhancement-mode GaN transistors are normally off, meaning no drain current flows through the 2DEG without applying positive voltage to the gate. Ex. 1001, 1:50-53, 1:64-2:2; *Hu*, 1; Shealy, [056]. These devices achieve the normally-off state in part with a **GaN layer**, often doped p-type, in the gate structure under a **gate metal**, which increases the gate voltage to a positive value. Ex. 1001, 1:50-53, 1:64-2:2; *Hu*, 1; Shealy, [055].

Example GaN HEMT arrangements in publications ranging from 1999 through 2009, the earliest claimed priority date of the ’335 patent, are shown below. Shealy, [057]. Note the **horizontal ledges** at the surface of the **p-type GaN gate materials**:



Yoshida, Fig. 1 (1999).

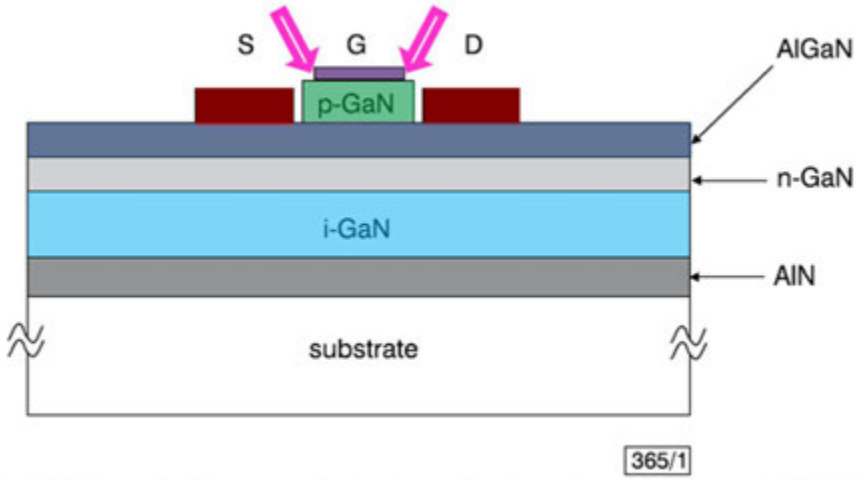


Fig. 1 *Schematic diagram of structure of pn junction regrown gate HFET*

Hu, Fig. 1 (2000).

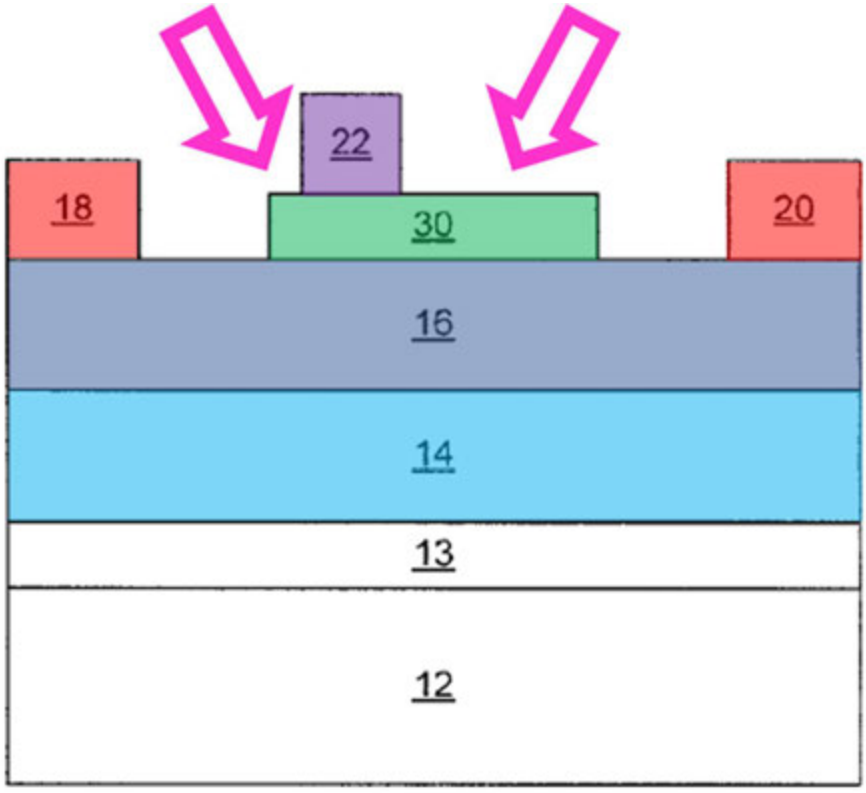
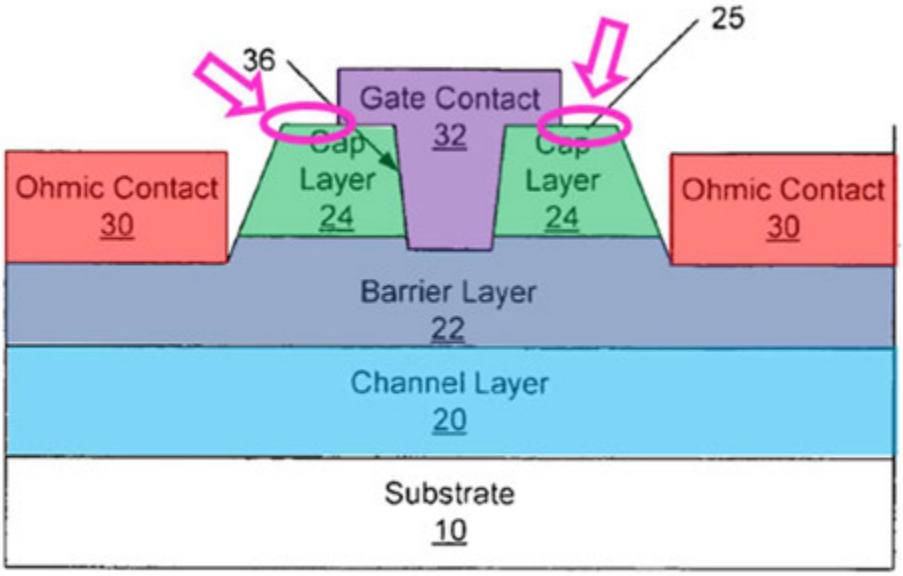
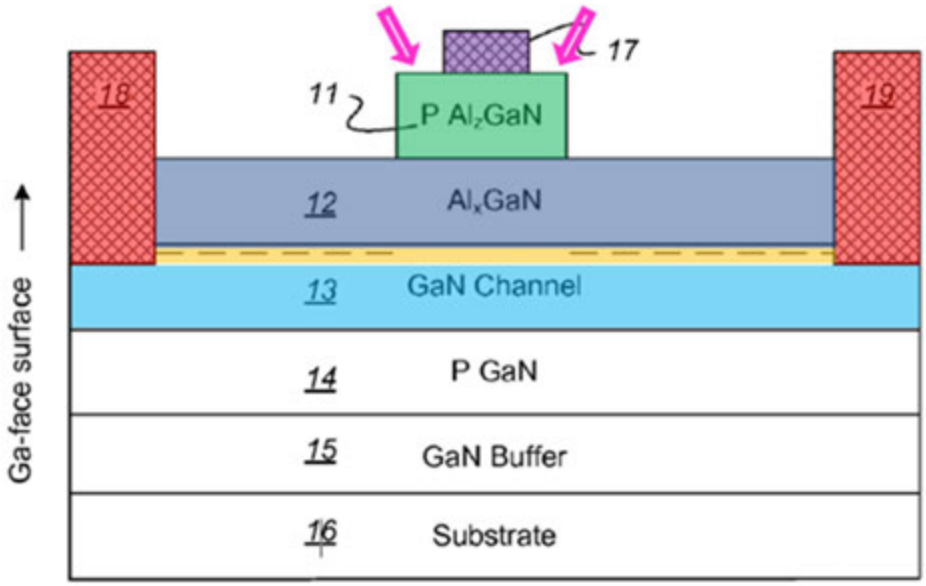


Figure 5B

Smith, Fig. 5B (2002).



Saxler, Fig. 1A (2006).



Suh, Fig. 6 (2009).

As these examples illustrate, the sole point of alleged novelty of the ’335 patent, **horizontal ledges** at the surface of **p-type GaN gate materials**, were common—as were the other features of the claims. Shealy, [058].

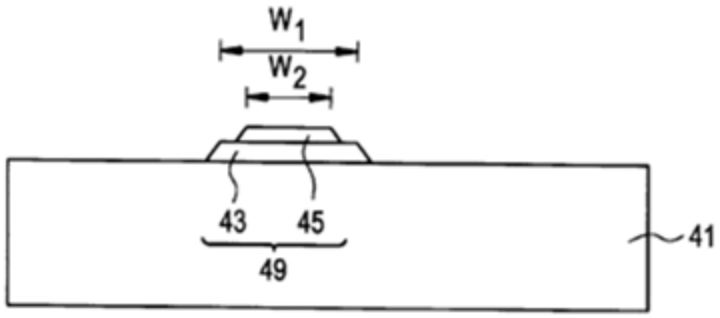
The prior art also included many different methods of manufacturing features of GaN HEMT devices. Shealy, [059] (citing *Beach*, [040]; *Ahn*, *Xu*, *Saxler* [064]; *Sheppard* [0044]). For example, single-mask techniques to self-align stacked gate structures were long known. *Beach*, [0040]; Shealy, [059]. Conventional etching techniques achieved sloped sidewalls, which were known to increase leakage paths. Ex. 1001, 1:64-2:8, Fig. 2; *Saxler*, [0064], Figs. 1A-1B; *Ahn*; *Xu*; *Sheppard*, [0044]; Shealy, [059]. And it was conventional to create undercuts under photomasks to isotropically etch metals. *Shenoy*; Shealy, [059].

A POSITA would have been familiar with many methods of making stepped gate structures with **horizontal ledges**, including (i) sequential masking and etching steps, (ii) lift off techniques, and (iii) self-aligned techniques. Shealy, [060] (citing *Yoshida*, [0022]-[0023]; *Hu*, 1; *Smith*, [0040]-[041]; *Saxler*, [0064]-[0066]; *Suh*, [056]). For example, *Yoshida* discloses masking and etching the p-type GaN **layer 5**, then depositing the **gate electrode**. *Yoshida*, [0022]-[0023]; Shealy, [060]. *Hu* grows gate layers in "selective areas defined by openings in an SiO_2 mask." *Hu*, 1; Shealy, [060]. *Smith* fabricates its gate structure by patterning the **GaN cap layer**, using conventional etching to remove portions of it, then forming a **gate electrode** on the GaN segment. *Smith*, [0040]-[0041]; Shealy, [060]. *Smith* also uses "conventional photolithographic techniques and mask alignment tools" to align the edges of a cap layer and gate in some embodiments, i.e., ***self-alignment***. *Smith*,

[0041]; Shealy, [060]. *Saxler* discloses sequential masking, etching, and deposition steps to form its stacked gate structure. *Saxler*, [0064]-[0066]. *Suh* likewise etches "to define a gate region where the p-type Al_zGaN cap 11 is located," and depositing the gate on top. *Suh*, [0056].

Beach makes a self-aligned two-layer gate structure using a single photomask. *Beach*, [0040], [0045], [0054]; Shealy, [061]. *Ahn*, published in 1999, likewise uses a single mask and further discloses isotropic and anisotropic etching techniques to create stacked gate structures having stepped features and sloped sidewalls, as shown below. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C; Shealy, [061].

FIG. 4C



Ahn, Fig. 4C.

In addition, long before the '335 patent, *Shenoy* discloses techniques to isotropically etch and undercut metal layers below masks, which a POSITA would understand would be one method of forming stepped gate structures. *Shenoy*, 2-3; Shealy, [062].

Lift-off had similarly been known for decades for creating stepped structures. Ex. 1023; Shealy, [062].

Typical GaN HEMT devices thus included every feature of the claimed enhancement-mode transistor and they disclosed methods of making such a transistor. Shealy, [0055]-[063].

III. The ’335 Patent

A. Overview

1. The alleged invention

The ’335 patent describes and claims an enhancement-mode GaN power transistor. Ex. 1001, 1:21-26, 2:34-57, Fig. 5, claims 1-7; Shealy, [044]. It asserts that conventional prior art GaN HEMT devices suffered from high gate leakage current between the gate and 2DEG region. Ex. 1001, 1:21-2:30; Shealy, [044]. The ’335 patent admits that conventional GaN enhancement-mode devices included **a GaN channel layer**, **an AlGaN barrier layer**, **source** and **drain electrodes**, and a gate structure consisting of a **p-type GaN layer with sloped sidewalls** and an overlying **gate metal**—all features that are in the claims of the ’335 patent. Ex. 1001, 1:21-2:30, Figs. 1-2, 3A-3B, claims 1-7; Shealy, [044]. The ’335 patent even depicts numerous prior art systems with these features and identifies the known leakage paths in Figure 2 (**path 201** along the sloped sidewalls, 202 through the p-type GaN layer). Ex. 1001, 1:21-2:30, Figs. 1-2, 3A-3B; Shealy, [044].

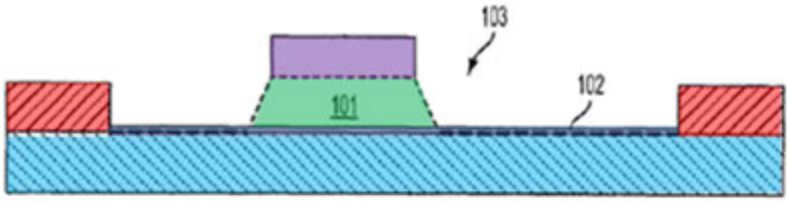


FIG. 1
PRIOR ART

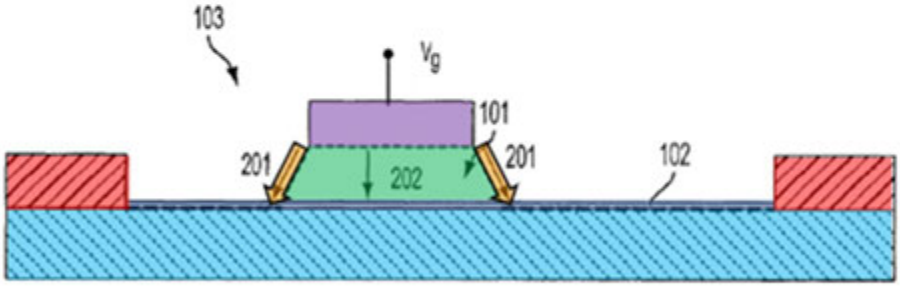


FIG. 2
PRIOR ART

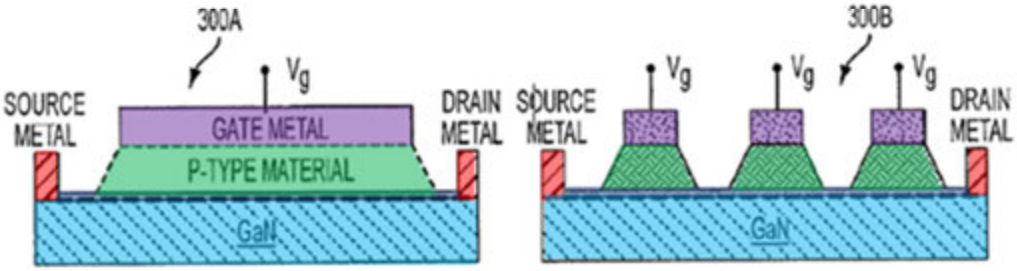
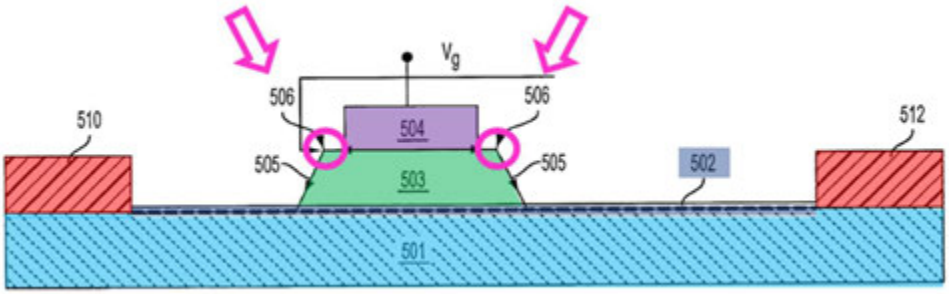


FIG. 3A
PRIOR ART

FIG. 3B
PRIOR ART

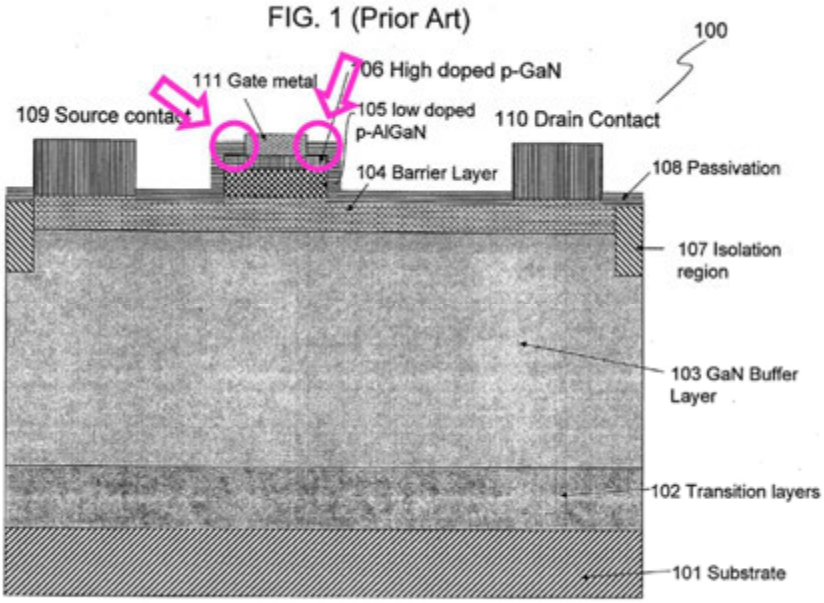
Ex. 1001, Figs. 1-2, 3A-3B.

As a purported solution to the problem of gate leakage, the '335 patent declares it adds ***just one purportedly novel feature***: a pair of **ledges** on the p-type gate material, on either side of the gate metal. Ex. 1001, 2:34-57, 3:65-4:12, 4:40-51, Figs. 1-2, 3A-3B, 4-5, 7A-7B, 8, claims 1-7; Shealy, [045].



Ex. 1001, Fig. 5.

But, such ledges were known in the field many years before the ’335 patent, and the claims were obvious over the prior art. Shealy, [046], [057]-[058] (citing *Yoshida*, *Hu*, *Smith*, *Saxler*, *Suh*); *infra* §§VIII-XI (Grounds 1-6). Indeed, the ’335 patent’s priority application *Lidow* notes this limitation was conventional. *Lidow*, [0006], Fig. 1; Shealy, [046].



Lidow, Fig. 1.

2. Self-aligned ledges

In some claimed embodiments, the ’335 patent makes its **ledges** using a self-alignment process. Ex. 1001, 4:14-39, claims 2, 5; Shealy, [047]. Figures 6A-6C disclose a method of making these “self-aligned ledges.” Ex. 1001, 4:14-39; Shealy, [047]. Priority applications also disclose “self-aligned gate” structures having symmetric ledges but do not describe the details of Figures 6A-6C. *E.g.*, *Lidow*, Abstract, [0008], [0022]-[0023], [0029]-[0030], [0036], [0038], [0040], [0044], [0046], claims 1, 6, 9, 10, 23; Shealy, [047].

In the ’335 patent, the self-aligned method includes forming **GaN layer 601**, **AlGaN layer 602**, and **p-type gate material 603**, then depositing the **gate metal 604** as Figure 6A depicts. Ex. 1001, 4:14-39; Shealy, [048]. The self-aligned method then applies **photoresist 605**, etches the gate metal, and etches the p-type gate material so that the outer walls **p-type gate material 603** and **gate metal** align as shown in Figure 6B. Ex. 1001, 4:14-26; Shealy, [048].

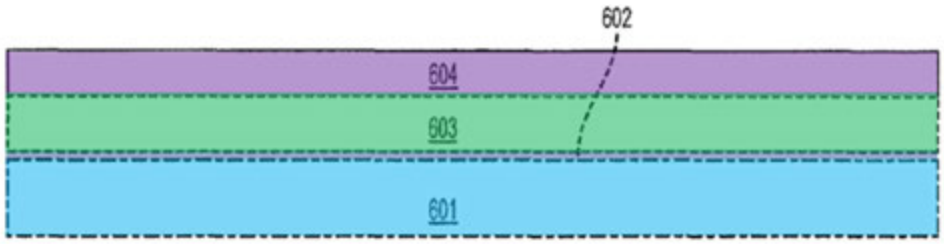


FIG. 6A

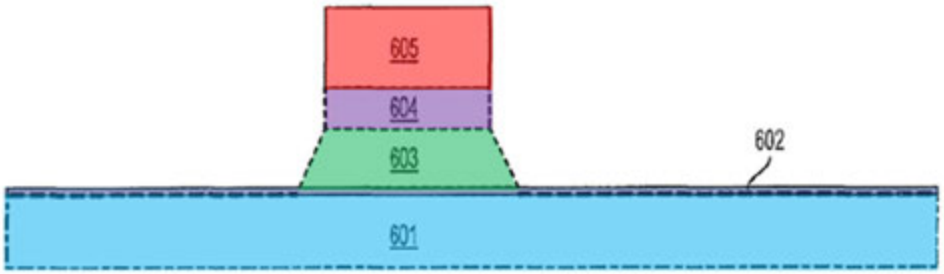


FIG. 6B

Ex. 1001, Figs. 6A-6B.

The ’335 patent discloses that one way to complete the “self-aligned” ledges is to next “isotropically” etch the **gate metal** and undercut the same **photomask**, as shown in Figures 6B-6C. Ex. 1001, 4:23-39; Shealy, [049].

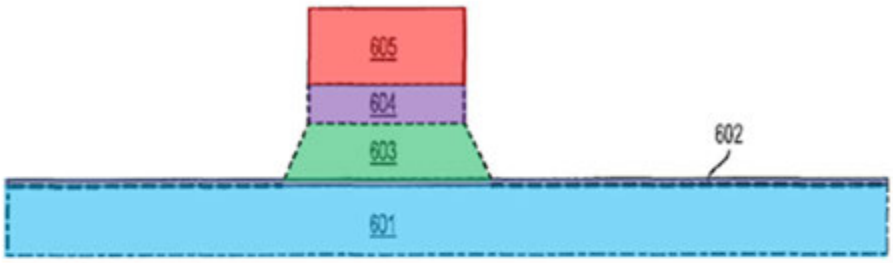


FIG. 6B

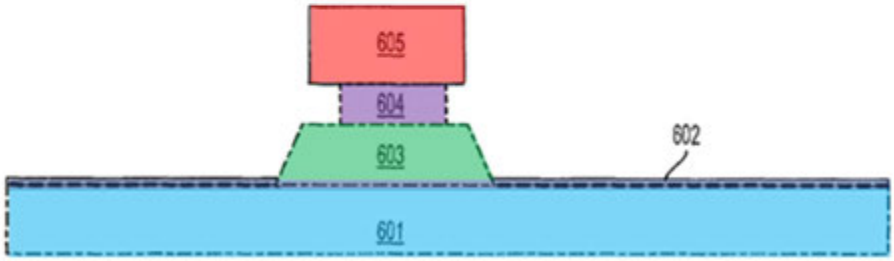


FIG. 6C

Ex. 1001, Figs. 6B-6C.

B. Prosecution History

1. Allowance of the ’335 Patent

The ’335 patent was filed on July 20, 2017, as U.S. Application 15/655,438. Ex. 1001, cover. The independent claims included the p-type gate metal material, overlying gate metal, and a pair of horizontal ledges, but did not include the sloped sidewall features. Ex. 1002, 77-79. The application received one non-final Office Action rejecting claims 1-3, 5-8, and 10-11 under 35 U.S.C. § 102 as anticipated by *Hikita* (Ex. 1016). Ex. 1002, 36-43. To overcome the rejection, the applicant amended the independent claims to include sloped sidewalls. Ex. 1002, 34-35, 7-15.

The Examiner then allowed the claims, stating that the combination of the sloped sidewalls and horizontal ledges were allowable. Ex. 1002, 12.

2. Priority claim

The ’335 patent claimed priority as a division of prior Application No. 14/447,069 (U.S. Patent No. 9,748,347 (“the ’347 patent”)), which claimed priority to U.S. Provisional Patent Application No. 61/860,976, filed August 1, 2013. Ex. 1001, cover & p. 2. The ’347 patent in turn claimed priority as a continuation-in-part to U.S. Application No. 13/838,792, which was a division of U.S. Application No. 12/756,960, filed April 8, 2010, and claimed priority to U.S. Provisional Patent Application No. 61,167,777, filed April 8, 2009. *Id.*; ’347 patent, cover & p. 2. However, this second priority claim was only raised after the Examiner rejected the claims over the alleged priority application, *Lidow*, which was, in fact, disclosed as admitted prior art *by the Applicant* before making the belated priority claim.

During prosecution of the parent application that became the ’347 patent, the applicant filed a Petition for Unintentional Delayed Priority to obviate a rejection over *Lidow* (U.S. 2010/0258843A1, Ex. 1011), a prior art reference the applicant had previously disclosed to the Patent Office. Ex. 1013, 95-128, 250. Incredibly, despite already admitting the reference was prior art through an IDS, the applicants reversed their previous representation and instead *claimed priority as a*

continuation-in-part to Lidow itself, utilizing a "Petition for ***Unintentionally*** Delayed Domestic Benefit Claim," including the required sworn statement by the prosecuting attorney that the "entire delay" was "unintentional," and that the petition was filed "immediately upon discovery." Ex. 1013, 104-05, 118-19. This petition was filed over a year after the applicant corrected domestic priority for errors in the filing receipt on the same day it submitted *Lidow* as prior art (Ex. 1013, 250, 282-90), and months after the Office cited *Lidow* as invalidating prior art (Ex. 1013, 227-34). The Office nonetheless granted the Petition without investigating the basis for the attestation of unintentional delay, Ex. 1013, 95-103, and the parent eventually issued as the '347 patent, *id.*, 1.

Because of this history, Petitioner disagree that the present application properly claims priority to U.S. Application Nos. 12/756,960, 13/838,792, and 61/860,976, and contend that this patent is unenforceable for inequitable conduct on the part of the prosecuting attorney for submitting a false petition. But for the acceptance of this false petition, *Lidow* is invalidating prior art. Petitioner intend to challenge this priority claim in a separate *Ex Parte* Reexamination (EPR) proceeding.

For purposes of this petition, however, Petitioner nevertheless assume priority to the filing of the earliest application in the priority claim, which is April 8, 2009.

Also, for purposes of this petition alone, Petitioner assume that the claims find support in that provisional application just as the Examiner found support for the claims of the ’347 patent in *Lidow*. Ex. 1013, 52, 75-76, 84-86. The apparatus claims of the ’335 patent covers substantially the same subject matter as the resultant structure of the method claims of the ’347 patent. Ex. 1001; Ex. 1012; Shealy, [051].

IV. Statement of Precise Relief Requested

A. Claims

Petitioner request review and cancellation of claims 1-7 under 35 U.S.C. § 311.

Prior Art

Yoshida (Ex. 1005, Ex. 1006), which published September 24, 1999, is prior art to the ’335 patent under pre-AIA 35 U.S.C. § 102(b).
Saxler (Ex. 1007), which published May 25, 2006, is prior art to the ’335 patent under pre-AIA 35 U.S.C. § 102(b).
Beach (Ex. 1008), which published January 11, 2007, is prior art to the ’335 patent under pre-AIA 35 U.S.C. § 102(b).
Shenoy (Ex. 1009), which published February 22, 1996, is prior art to the ’335 patent under pre-AIA 35 U.S.C. § 102(b).

The examiner did not have the benefit of any of these references.

B. Grounds

Ground	Challenged Claims	Basis	Prior Art
1	1-7	§ 103	*Saxler* in view of the knowledge of a POSITA
2	1-7	§ 103	*Saxler* in view of *Yoshida*
3	2, 5-7	§ 103	*Saxler* in view of *Yoshida*, *Beach*, and *Shenoy*
4	1-7	§ 103	*Yoshida* in view of the knowledge of a POSITA
5	1-7	§ 103	*Yoshida* in view of *Saxler*
6	2, 5-7	§ 103	*Yoshida* in view of *Saxler*, *Beach*, and *Shenoy*

V. Statement of Facts

Pursuant to 37 C.F.R. § 42.22(c), the following statement of facts set forth the state of enhancement-mode GaN transistors at the time of the ’335 patent’s earliest claimed priority date of April 8, 2009.

1. Before April 8, 2009, the following were known:

   a. a GaN layer;

   b. an AlGaN barrier layer disposed on the GaN layer;

   c. source and drain electrodes disposed on the AlGaN barrier layer;

   d. a gate structure disposed on the barrier layer between source and drain electrodes;

e. a gate structure with a p-type GaN layer with sloped sidewalls that extended horizontally towards the source and drain electrodes; and

f. a gate structure with an overlying gate metal.

2. Before April 8, 2009, self-aligned gate structures were known.

VI. Level of Ordinary Skill

A person of ordinary skill in the art ("POSITA") with respect to the '335 patent would have possessed at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field, and at least two years of experience in semiconductor device design and/or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Shealy, [052]-[053]. Additional education could substitute for professional experience and vice versa. *Id.*

VII. Claim Construction

The Board construes claims using the standard of *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 37 C.F.R. § 42.100(b); *CUPP Comput. AS v. Trend Micro Inc.*, 53 F.4th 1376, 1380 (Fed. Cir. 2022). Under this standard, claim terms receive their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the specification, prosecution history, and extrinsic evidence. *Phillips*, 415 F.3d at 1314-19.

A. "side surfaces [extending/that extend] horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer"

Independent claim 1 recites that the p-type gate material has "side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer." Claim 5 includes the same limitation but with "that extend" instead of "extending" and "contact" instead of "contacting." In a related matter, Patent Owner and Petitioner have agreed that these terms should be construed. *See* Ex. 1028. The parties have proposed the following constructions:

Petitioner's	Patent Owner's
"side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer"	"p-type gate material having side surfaces extending horizontally such that the bottom of the material is wider than the top of the material"

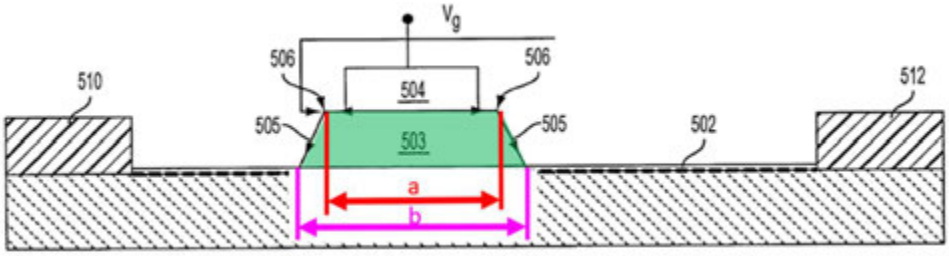
The challenged claims are unpatentable under both constructions. But to the extent the Board construes the term, Petitioner's proposed construction should apply. Shealy, [070]-[076].

The construction agrees with the disclosure of the prior application, *Lidow*, which provides support for the present claims (§III.B (Prosecution History)). *Lidow* asserts the advantage of using sloped sidewalls in a p-type GaN gate layer to reduce gate leakage. *Lidow*, [0041]-[0042], Fig. 8. *Lidow* specifically teaches that a "base that is more than 10% wider than the top" advantageously "causes a longer path for electrons to travel between the gate metal 17 and the 2DEG along the pGaN side wall," thereby "result[ing] in lower gate leakage." *Id.*, [0042]. *Lidow* depicts the same p-type layer and gate structure as the '335 patent. *Id.*, Fig. 8; Ex. 1001, 3:49-64, Fig. 5; Shealy, [072].

The construction also adheres to the purpose of the '335 patent—reducing gate leakage, including through the conventional method of sloping the sidewalls to increase the length of sidewall leakage path 201. Ex. 1001, Abstract, 1:21-26, 2:20-48, 3:65-4:12, 4:40-51, Figs. 2, 4, 7A-7B, 8; Shealy, [073]. *See Honeywell Int'l Inc. v. Universal Avionics Sys. Corp.* 488 F.3d 982 (Fed. Cir. 2007) (construing claim to be consistent with the "purpose of" the limitation); *see also KEYnetik, Inc. v. Samsung Elecs. Co.*, 837 F. App'x 786, 793 (Fed. Cir. 2020) (reversing Board construction that would "eviscerate[] the purpose of the invention").

Lidow provides no other guidance on how much slope is sufficient to achieve reduced gate leakage. Within the field, at least slightly sloped sidewalls are common—few structures, if any, have perfectly vertical sidewalls in practice, even if depicted as vertical in functional diagrams. Shealy, [074], [203]-[205] (citing *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5); *infra* §X.C.5 (Ground 4, [1d]). To distinguish its purported invention from the prior art and gain the alleged benefits of lower gate leakage due to a longer leakage path, *Lidow* unequivocally describes controlling the shape of the p-type GaN material during etching to achieve a base 10% wider than the top. *Lidow*, [0041]-[0042]. Petitioner's construction makes this distinction clear.

The construction likewise accords with the '335 patent's disclosure. For example, the '335 patent depicts a p-type gate material with sloped side surfaces whose bottom surface is more than 10% wider than the top. Ex. 1001, Figs. 5, 6C, 7B; Shealy, [075].



Ex. 1001, Fig. 5.

Width "b" above is approximately 30% wider than width "a," and the same holds true for Figures 6C and 7B. *Id.*

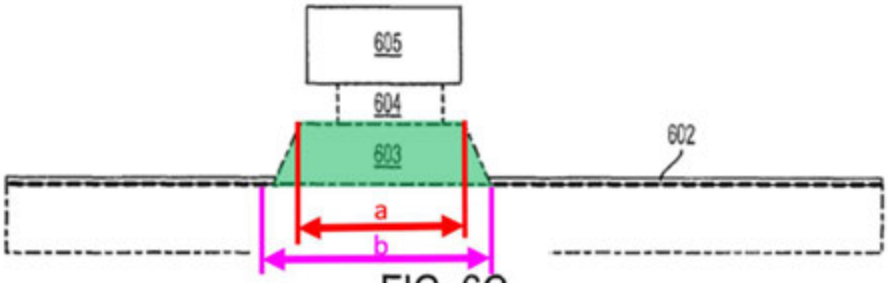


FIG. 6C

Ex. 1001, Fig. 6C.

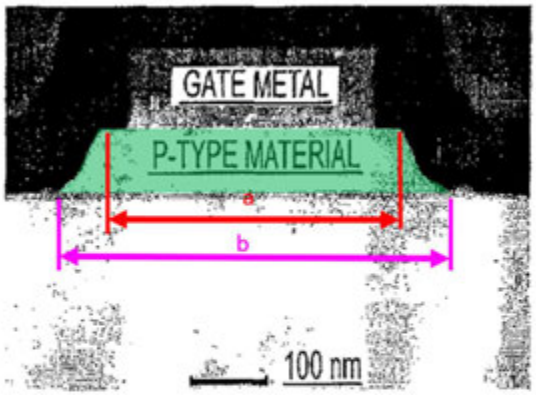


FIG. 7B

Ex. 1001, Fig. 7B.

Examining Patent Owner's construction, any reference that discloses this term under Petitioner's construction will also disclose this term under Patent Owner's. because Petitioner'ss construction also requires that the bottom of the p-type gate material is wider than the top. Shealy, [076]. Therefore, all Petitioner's arguments below will apply under either construction. However, if Patent Owner's broader

construction is accepted, the patent is unpatentable under an additional ground, Ground 4.

B. "self-aligned" ledges

Claims 2 and 5 recite a transistor that requires "self-aligned" ledges. These are "product-by-process" limitations. In the '335 patent, a "self-aligned" ledge refers to a process for making the claimed gate structure and does not describe the structure itself. Ex. 1001, 4:14-39; *Lidow*, Abstract, [0008], [0022]-[0023], [0029]-[0030], [0036], [0038], [0040], [0044], [0046], Figs. 6A-6C, claims 1, 6, 9, 10, 23; Shealy, [077]-[085]. The '335 patent unambiguously describes that "the gate contact includes a p-type gate material 503 formed on the barrier layer 502 and includes ledges 506 ***that are created by a self-aligned process*** at the top corners of the p-type gate material 503." Ex. 1001, 3:49-53; Shealy, [078]. The patent repeatedly refers to this "self-aligned manufacturing ***process***." Ex. 1001, 3:13-15, 3:49-53, 3:65-4:39, 4:52-63, Figs. 6A-6B.

Claim 3 of the '347 patent illustrates that "self-aligned" ledges refers to how the ledges are made, not what they are. Shealy, [079]. It recites "[t]he ***method*** according to claim 1, wherein the pair of ledges of the p-type gate material ***are self-aligned***." This is consistent with how a POSITA would have understood the term. Shealy, [080]-[085] (citing *Smith*, [0041]-[0044], Fig. 4C; *Beach*, [0040]; *Suh 2006*, 1, Fig. 1).

Claims 2 and 5 of the ’335 patent thus plainly recite product-by-process steps in a device claim, which lend no patentable weight. Ex. 1001, claims 2, 5. “The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” *In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985) (citations omitted); *Kamstrup A/S v. Axioma Metering UAB*, 43 F.4th 1374, 1381-83 (Fed. Cir. 2022) (finding “cast in one piece” in claim to flow meter a product-by-process element that gives no patentable weight); *United Therapeutics Corp. v. Liquidia Techs., Inc*., 74 F.4th 1360, 1373 (Fed. Cir. 2023) (“As these claims are product claims, they are anticipated by a disclosure of the same product irrespective of the processes by which they are made.”).

VIII. Grounds 1 and 2: *Saxler*, Alone (Ground 1) or in View of *Yoshida* (Ground 2) Renders Obvious Claims 1-7

A. Overview of Grounds 1 and 2

Saxler discloses the arrangement of semiconductor layers and structures of claims 1-7. In some embodiments its gate metal is not recessed. *Saxler*, [0052]. These embodiments render obvious claims 1-7 (Ground 1). Shealy, [086]-[0150].

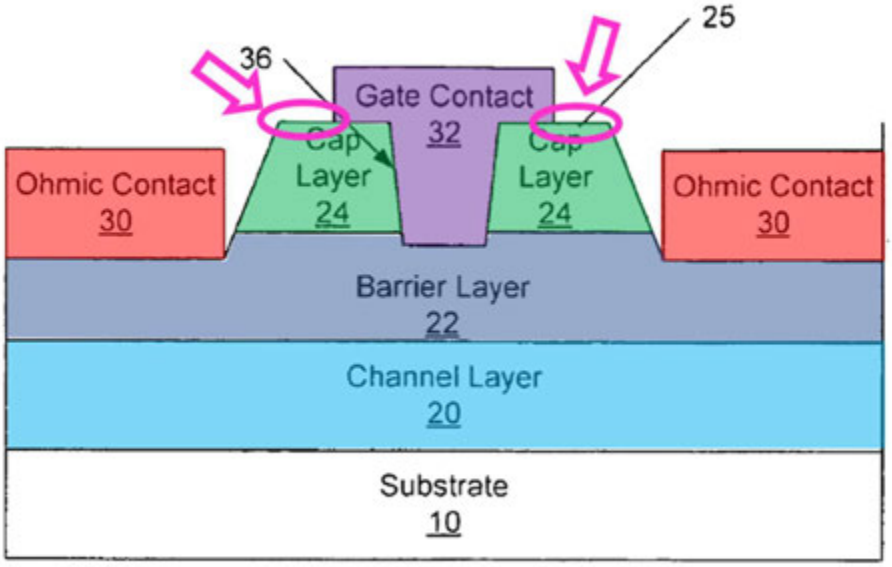
To the extent Patent Owner argues that *Saxler*’s cap layer does not render the claims obvious because its figures depict the recessed gate rather than the non-recessed embodiments, despite the explicit disclosure the recess is optional, *Yoshida*

also discloses and depicts a very similar device with a p-type gate material without a gate recess. The combination of *Saxler* and *Yoshida* renders obvious claims 1-7 (Ground 2). Shealy, [086]-[150].

1. Ground 1: *Saxler*

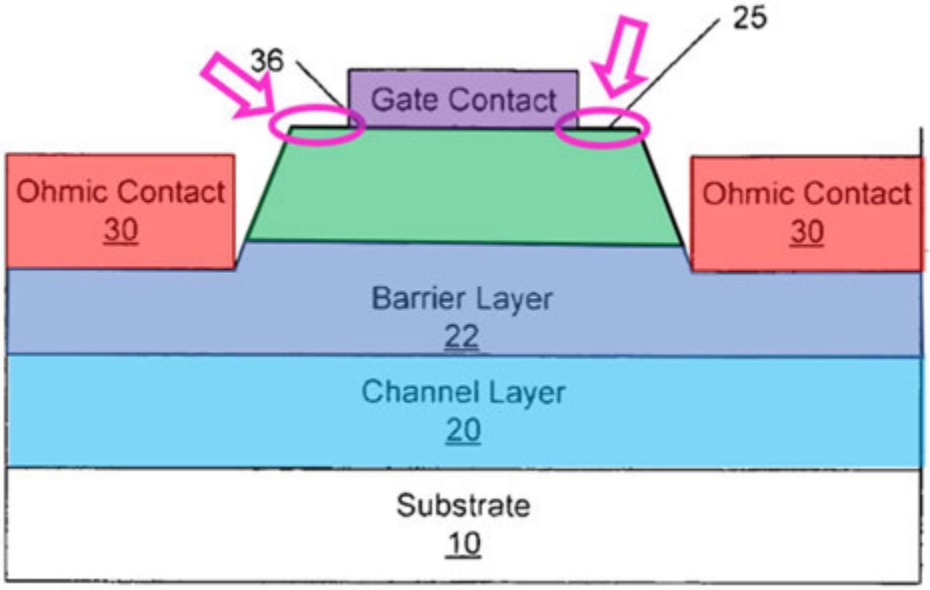
Saxler discloses a GaN transistor with high breakdown voltage. *Saxler*, [0006], [0007]-[0030], Figs. 1A, 2B; Shealy, [089]. As shown below, *Saxler*'s **channel layer 20** is a GaN over silicon, and *Saxler*'s **barrier layer 22** is a Group III-nitride that may be AlGaN. *Saxler*, [0057]-[0060], Figs. 1A, 2B; Shealy, [089]. *Saxler* discloses "induc[ing] a **two-dimensional electron gas**" at the interface of these layers. *Saxler*, [0004], [0059] Shealy, [089]. *Saxler* discloses **source** and **drain** contacts. *Saxler*, [0065]; Shealy, [089].

Saxler further discloses a stacked gate structure above the **barrier layer 22** consisting of a **cap layer** and **gate contact** that is metal. *Saxler*, [0061]-[0063], [0066], [0071]-[0073], [0076], [0087], Figs. 1A, 2B; Shealy, [090]. The **cap** layer may be p-typed doped GaN and doped in a subregion or throughout. *Saxler*, [0013], [0069], [0071], [0073]; Shealy, [090]. *Saxler*'s gate contact may be recessed or non-recessed (i.e., flat). *Saxler*, [0052], [0066]. Where utilized, *Saxler*'s recessed contact may be a T-shaped into the cap layer, and in some embodiments, it extends through the cap layer into the barrier layer, while in other embodiments it does not contact the barrier layer. *Saxler*, [0065]; Shealy, [090].



Saxler, Fig. 1A.

Where the gate recess is not utilized, *Saxler* has the following structure. Shealy, [091].



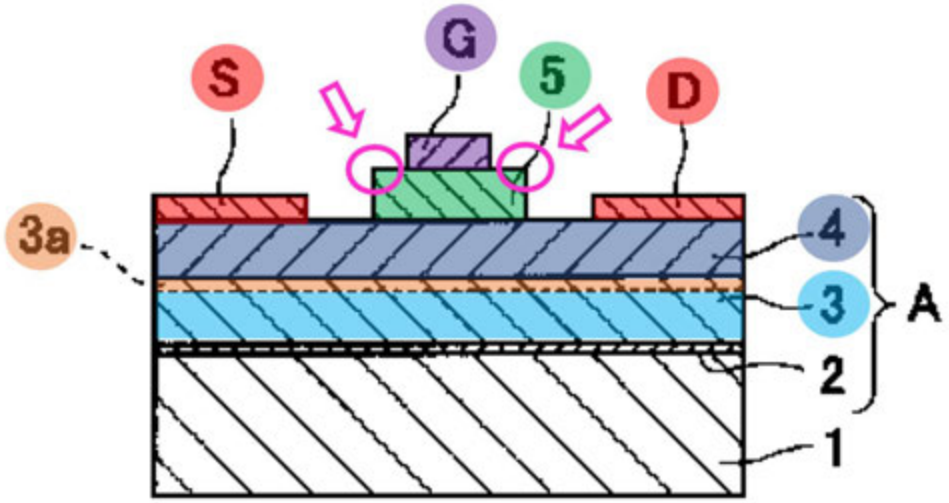
Saxler, Fig. 1A (modified).

2. *Yoshida*

Yoshida, which published ten years before the earliest possible priority of the ’335 patent, also discloses a normally-off enhancement-mode GaN transistor having a p-type GaN layer below the gate that “enables voltage control with a small amount of carrier injection,” an arrangement that was conventional by the time of the ’335 patent. *Yoshida*, [0017], [0015], Fig. 1; Shealy, [092]. *Yoshida* improves breakdown voltages over prior art GaN transistors. *Yoshida*, [0008]-[0009]; Shealy, [092].

Yoshida’s **layer 3** is a GaN grown over silicon nitrate like *Saxler*’s, and **layer 4** is an n-type semiconductor, with **2DEG 3a** forming at their interface. *Yoshida*, Abstract, [0010], [0013], [0019]; Shealy, [093]. It includes a **source** and **drain** contact. *Yoshida*, Abstract, [0009].

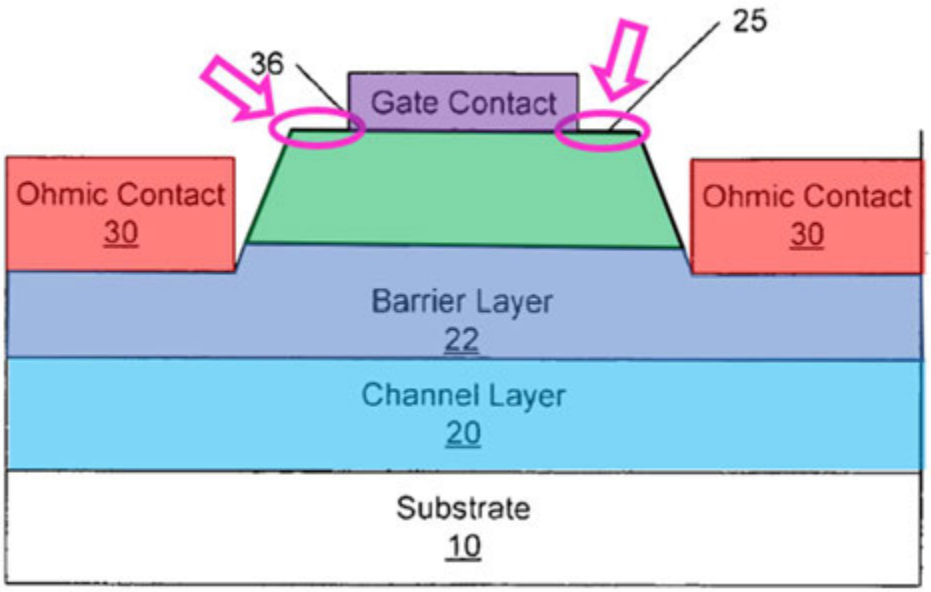
Yoshida also discloses a stacked gate structure consisting of a **doped GaN layer** above the **semiconductor layer 4** and an overlying **gate metal**. *Yoshida*, Abstract, [0015]; Shealy, [094]. Its gate structure includes a pair of **horizontal ledges** on either side of the gate metal. *Yoshida*, Fig. 1; Shealy, [094].



Yoshida, Fig. 1.

3. Ground 2: The combination of *Saxler* in view of *Yoshida*

Implementing *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure results in the following combined structure. Shealy, [095]. Note that this results in the same arrangement as *Saxler*'s non-recessed embodiment:

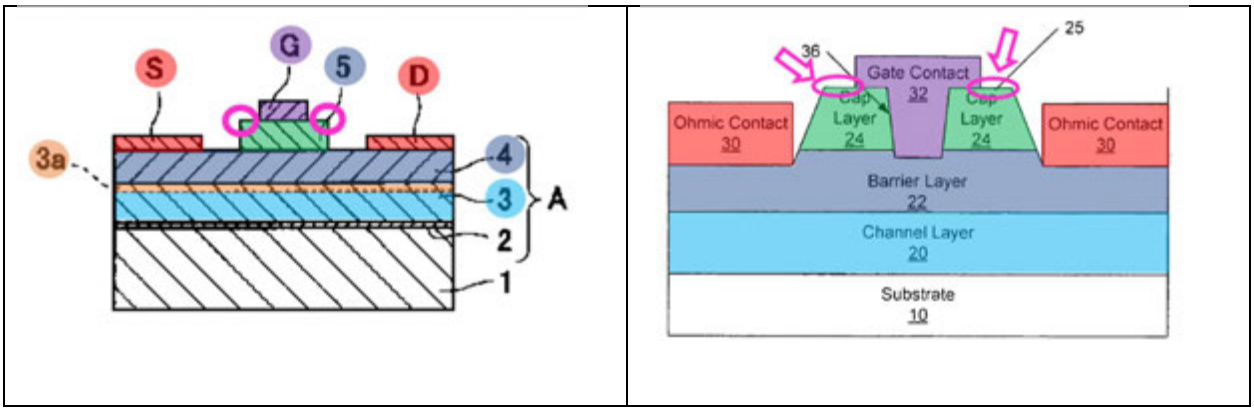


Saxler, Fig. 1A (modified).

4. Ground 2: Motivation to Combine

It would have been obvious to implement *Yoshida*'s non-recessed gate in *Saxler*'s stacked gate structure. Shealy, [096]-[106].

Saxler and *Yoshida* disclose compatible enhancement-mode GaN HEMT devices comprising the same layers performing the same functions, including stacked gate structures having a cap layer and gate metal. Shealy, [097]. Both describe gallium nitride HEMTs with improved breakdown voltages over the prior art. *Yoshida*, [0008]-[0009]; *Saxler*, [0006], [0007]-[0030]; Shealy, [097]. Unsurprisingly, these transistors share numerous overlapping features—they use the same arrangement of layers, as the below comparison illustrates. Shealy, [097].

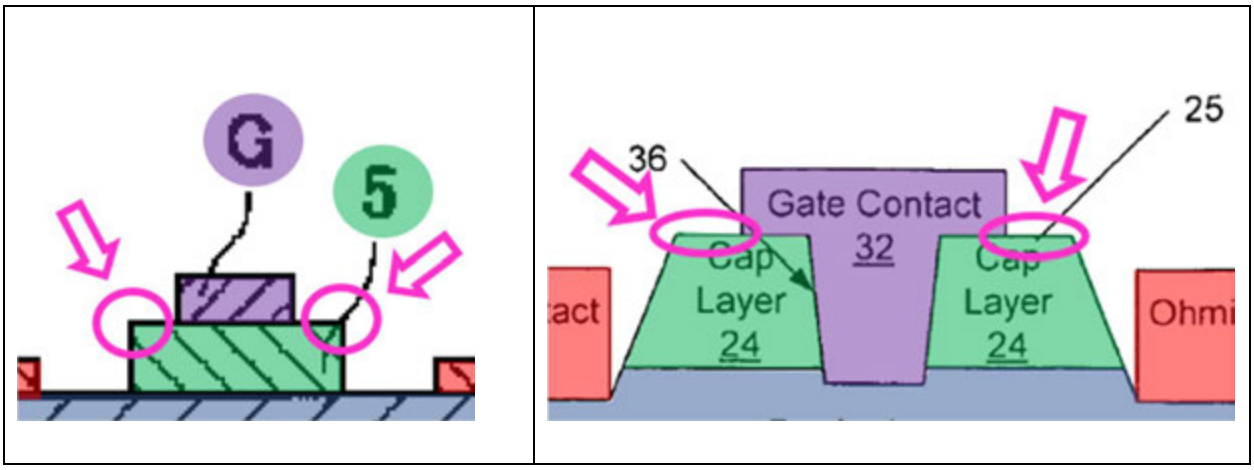


Yoshida, Fig. 1, *Saxler*, Fig. 1A (**2DEG region** present, but not shown).

Yoshida's **layer 3** is GaN over a silicon substrate, as is *Saxler*'s **channel layer 20**. *Yoshida*, [0012], [0019]; *Saxler*, [0057]-[0058]; Shealy, [098]. *Yoshida*'s **layer 4** is an n-type semiconductor, just like embodiments of *Saxler*'s **barrier layer 22**. *Yoshida*, Abstract, [0010], [0013]; *Saxler*, [0059]-[0060]; Shealy, [098]. Both have **2DEG regions** formed at the junction of these two layers. *Yoshida*, [0016]; *Saxler*, [0004], [0006], [0008]. Both references have **source**, **drain**, and **gate metal** contacts. *Yoshida*, Abstract, [0009]; *Saxler*, [0065]-[0066]. And both disclose a **doped layer** above the **barrier** and in contact with the **gate metal**. *Yoshida*, Abstract, [0015]; *Saxler*, [0069], Figs. 1A, 2B; Shealy, [098].

The specific form of their stacked gate differs between references but performs the same function—to control voltage "with a small amount of carrier injection" and "enable[] control of current flowing between channels" at high voltage. *Yoshida*, [0017]; *Saxler*, [0065]; Shealy, [099].

In *Saxler*'s pictured embodiments, the metal occupies a recess in the cap layer extending into the barrier layer, touching the barrier layer, or not touching the barrier layer. *Saxler*, Abstract, [0007]-[0008], Figs. 1A, 2B, Shealy, [100]. *Yoshida*'s gate metal, in contrast, sits flush on top of layer 5. *Yoshida*, Fig. 1; Shealy, [100]. Those structures are shown below.



Yoshida, Fig. 1, *Saxler*, Fig. 1A.

However, *Saxler* repeatedly discloses that its gate recess is optional. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88. While its figures do not explicitly depict a ***stacked*** gate structure having a gate contact and cap layer isolated from the source and drain contacts and without a gate recess, this disclosure would at a minimum render the claimed structure obvious. Shealy, [101]. To the extent Patent Owner disagrees with *Saxler*'s optional disclosure of the recess renders this structure obvious (Ground 1), *Yoshida* further renders the claimed structure obvious (Ground 2).

A POSITA would have been motivated and found it obvious to combine *Saxler*'s gate structures with *Yoshida*'s gate structure and accompanying fabrication techniques. Shealy, [102]-[106] (citing *Saxler*, *Sheppard*, *Yoshida*, *Smith*). A POSITA would have been familiar with many methods of making such stacked, stepped structures (§II, Technological Background) and combined *Saxler* and *Yoshida* to simplify manufacturing and decrease costs. Shealy, [060]-[062] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [102]. *Saxler* references and incorporates *Sheppard* (Ex. 1021) as disclosing "[s]uitable structures and techniques for fabricating GaN-based HEMTs" according to *Saxler*'s purported invention. *Saxler*, [0046] (referencing Ser. No. 10/897,726), [0068] (same). *Sheppard* discloses complicated and exacting manufacturing processes to create a gate recess and deposit the gate metal. *Id.*, [0043], [0046]-[0051], [0053]-[0056], Figs. 1C-1F, 2A-2B, Fig. 3. Its GaN cap layer may be "about 2 nm to 500 nm thick," and the thin AlGaN underlying barrier layer is between "0.1 nm and about 40 nm." GaN. *Id.*, [0040], [0042]; Shealy, [103]. Accordingly, tolerances when manufacturing the gate recess are extremely small. Shealy, [103]. This raises complexity and costs of manufacturing to avoid costly out-of-tolerance defects. Shealy, [103].

To avoid these problems, a POSITA would have been motivated to use *Saxler*'s non-recessed gate contact in its stacked gate structure in combination with *Yoshida*'s gate structure and accompanying fabrication techniques. A POSITA

would have recognized this as a suitable option for solving such problems. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007); *Intel Corp. v. PACT XXP Schweiz AG*, 61 F.4th 1373, 1379-81 (Fed. Cir. 2023). A POSITA would have been familiar with a wide variety of stacked gate structures in GAN HEMT devices, including many without recessed gates. Shealy, [104].

A POSITA would have further been motivated to remove the gate recess to turn *Saxler*'s device into an enhancement mode device, thus realizing the benefits of reduced power consumption and suitability for high power applications. *Suh*, 1; Shealy, [057]-[063] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [103].

Indeed, *Saxler* recognizes still other HEMT structures would be compatible with its disclosure, including *Smith*'s devices which it incorporates by reference. *Saxler*, [0087]; Shealy, [105]. *Smith* discloses non-recessed gate electrodes in stacked structures similar to *Saxler*'s recessed stacked gate structure. *Smith*, [0033], [0041], Figs. 3, 5B. *Smith* states that "there is no benefit to recessing the gate down to the barrier layer" in GaN HEMT devices "because the top surface of GaN is generally not conductive." *Id.*, [0010]; Shealy, [105]. And although it briefly discloses using T-shaped gate electrodes for "microwave and RF" applications (*Smith*, [0017], [0034], claim 20), *Smith* otherwise only describes and depicts stacked gate structures having a **GaN cap layer** with a non-recessed **gate electrode**

(*id.*, [0033]-[0037], [0039]-[0043], claim 1, Figs. 3, 4A-4C, 5A-5B); Shealy, [105]. Like *Saxler*, *Smith*'s GaN HEMT also includes a **GaN channel layer** and **AlGaN barrier layer** (inducing a **2DEG region**), and **source** and **drain electrodes**. *Smith*, [0030]-[0037], [0041]; Shealy, [105]. A POSITA would thus have understood non-recessed electrodes were a suitable option for *Saxler*'s GaN, which bears substantially the same layers and structure. Shealy, [105].

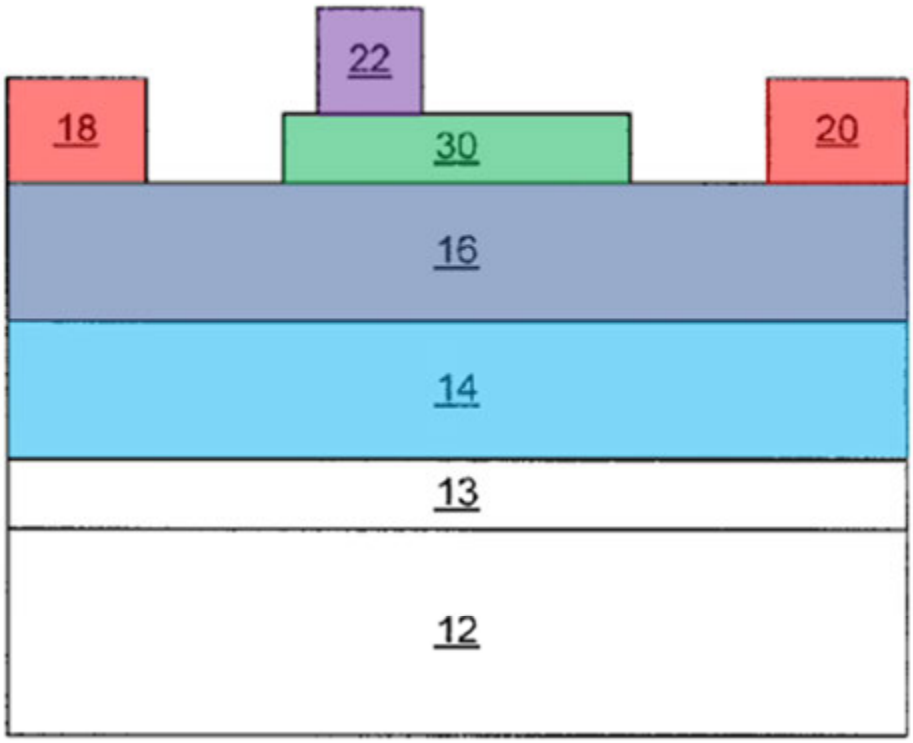


Figure 5B

Smith, Fig. 5B.

In view of the many options for stacked gate structures in GaN HEMT, including *Saxler*'s non-recessed stacked gate structures, a POSITA would have found the combination of *Yoshida*'s non-recessed gate arrangement in *Saxler*'s gate arrangement nothing more than the simple substitution of known elements to predictably yield an enhancement mode GaN HEMT device. Shealy, [057]-[063], [096]-[106].

B. Independent Claim 1

Saxler in view of the knowledge of a POSITA (Ground 1) and in view of *Yoshida* (Ground 2) renders obvious claim 1. Shealy, [107]-[134].

1. [1p] An enhancement-mode GaN transistor, comprising:

To the extent limiting, *Saxler* discloses or renders obvious the preamble. Shealy, [108]-[109]. *Saxler* discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer. *Saxler*, [0007]-[0010], [0046], [0059]-[0064], Figs. 1A, 1B; Shealy, [108]. This constitutes a normally-off enhancement-mode GaN transistor when the cap is doped p-type. Shealy, [108].

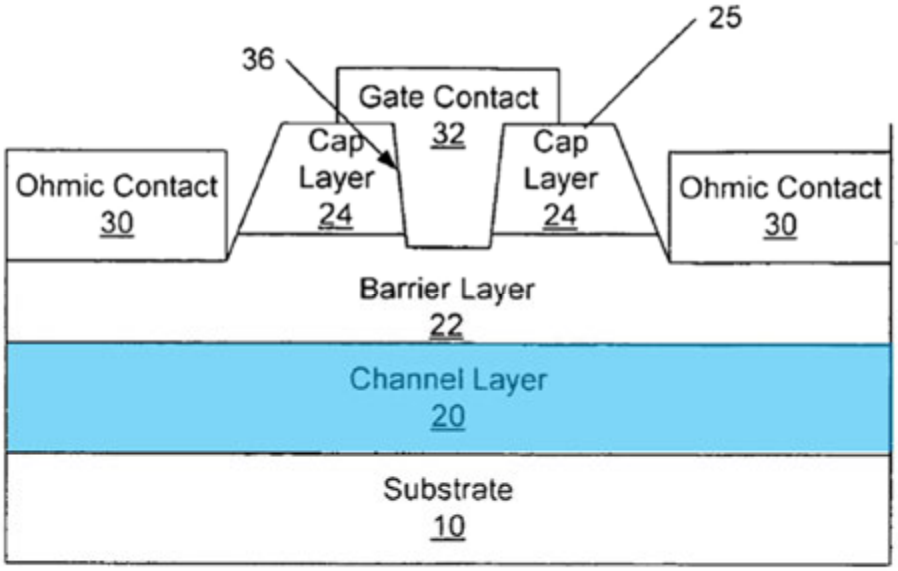
A POSITA would have understood *Saxler*'s transistors to be enhancement-mode GaN transistors at least because of their gate structure. Shealy, [109] (citing *Sheppard*, [0014], [0040], [0042], Fig. 1F). For example, *Sheppard*, which *Saxler* expressly incorporates (*Saxler*, [0046], [0068], (referencing Ser. No. 10/897,726)),

likewise discloses a GaN high-mobility transistor that includes a doped GaN cap layer below the gate and above an AlGaN barrier layer, where the cap layer "moves the top surface of the device physically away from the channel, which may reduce the effects of the surface," constituting a normally-off enhancement-mode GaN transistor when the cap is doped p-type. *Sheppard*, [0014], [0040], [0042], Fig. 1F; Shealy, [109].

2. [1a] a GaN layer;

The '335 patent admits [1a] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B; Shealy, [110].

Saxler discloses a **GaN channel layer** (Grounds 1-2). *Saxler*, [0007], [0010], [0016], [0058], [0069], Figs. 1A-1F; Shealy, [110]-[111].

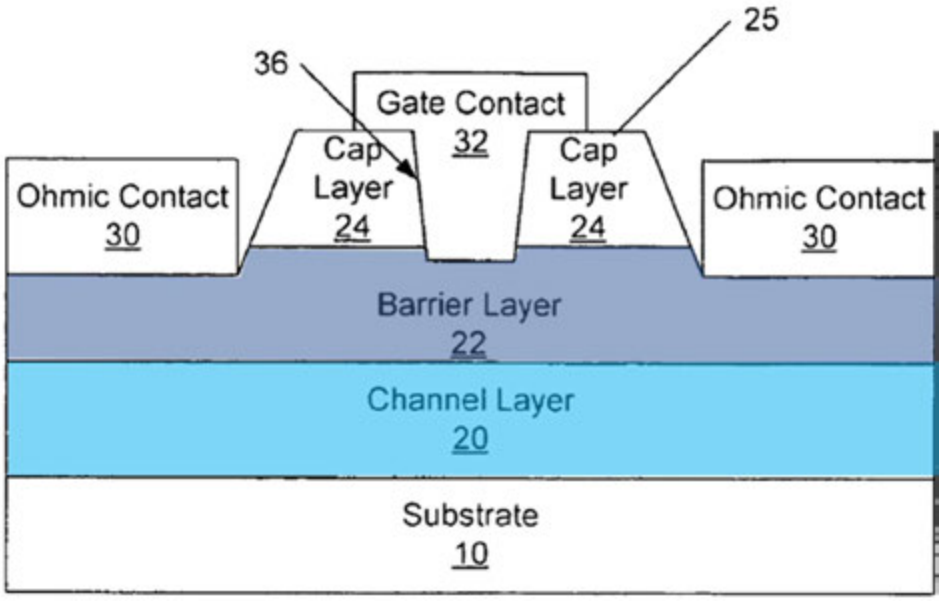


Saxler, Fig. 1A.

3. [1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

The '335 patent admits [1b] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B; Shealy, [112].

Saxler discloses [1b] (Grounds 1-2). Shealy, [112]-[115]. *Saxler*'s **barrier layer 22** is disposed on its GaN **channel layer**. *Saxler*, Abstract, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B.



Saxler, Fig. 1A.

Saxler's barrier layer may be an AlGaN layer. *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B; Shealy, [114]. The '335 patent likewise discloses that the claimed barrier layer may be an AlGaN layer, which is covered in

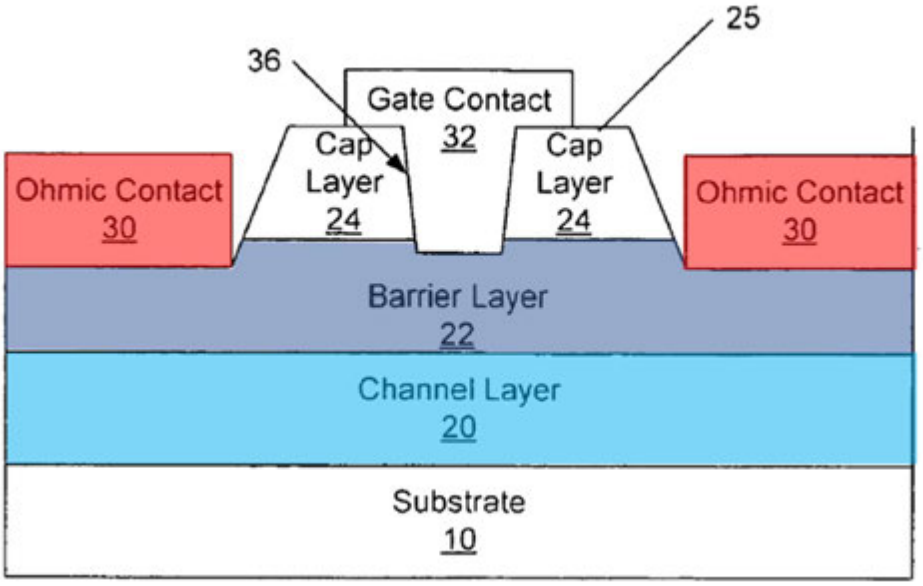
the dependent claims. Ex. 1001, 1:42-63, 3:37-48, 4:16-22, claims 3, 6; Shealy, [114].

Saxler further discloses "induc[ing] a **two-dimensional electron gas**" at the interface of the first GaN layer and second AlGaN layer. *Saxler*, [0004], [0059] ("induce a significant carrier concentration at the interface between the channel layer 20 and the barrier layer 22"); Shealy, [115].

4. [1c]: a source contact and a drain contact formed on the barrier layer;

The '335 patent admits [1c] was conventional. Ex. 1001, 1:64-2:19, Figs. 1-2, 3A-3B; Shealy, [116].

Saxler discloses "ohmic contacts 30" that may "provide **source** and **drain contacts**" formed on barrier layer 22 (Grounds 1-2). *Saxler*, [0065], Figs. 1A, 2B; Shealy, [116]-[117].



Saxler, Fig. 1A.

5. [1d]: a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

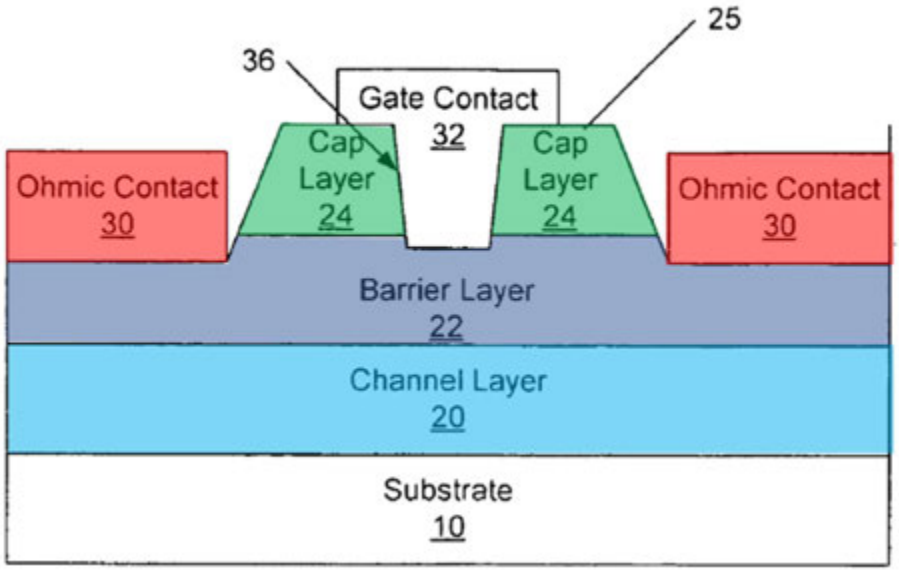
The ’335 patent admits [1d] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B; Shealy, [118].

Saxler alone (Ground 1) and/or in view of *Yoshida* (Ground 2) renders obvious [1d] under either parties’ construction of the side surfaces limitation. Shealy, [118]-[126].

Under Ground 1, *Saxler*’s **cap layer** discloses a p-type gate material. *Saxler*, [0013], [0069], [0071], [0073]; Shealy, [120]. The **cap layer** resides above an

AlGaN **barrier layer**, as claim 1 of the '335 patent requires. *Saxler*, [0010], [0059]-[0063], Figs. 1A, 2B; Shealy, [120].

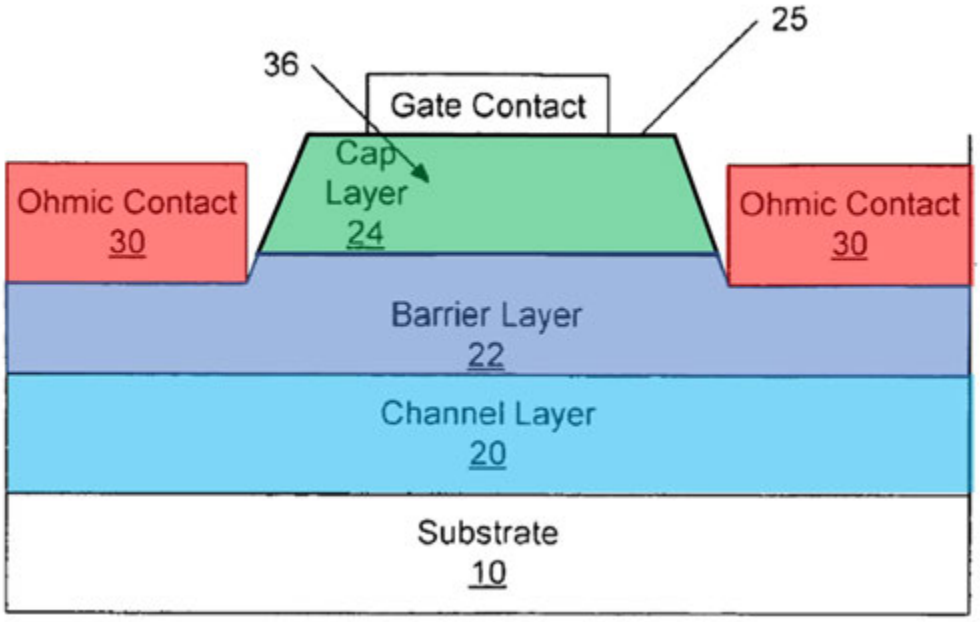
Saxler's **cap layer** has side surfaces extending horizontally towards the **source** and **drain contact**, and contacting the barrier layer. *Saxler*, [0064], Figs. 1A, 2B; Shealy, [121].



Saxler, Fig. 1A.

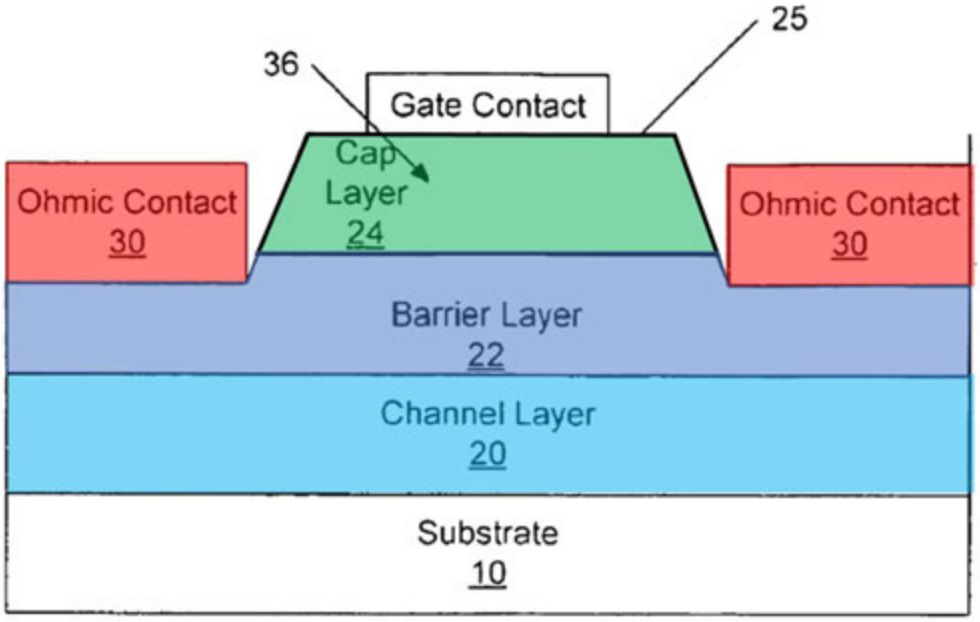
Saxler discloses "***a*** p-type gate material … having side surface**s**" as recited in claim 1. Although it depicts its gate recess may separate its cap layer into two portions in some embodiments, the recess in *Saxler*'s cap layer 24 need not be present and need not extend through the cap layer 24 and into the barrier layer. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [122]. *Saxler* thus discloses or at least renders

obvious a single p-type gate material having two side surfaces that extend horizontally towards the source and drain. Shealy, [123].



Saxler, Fig. 1A (modified).

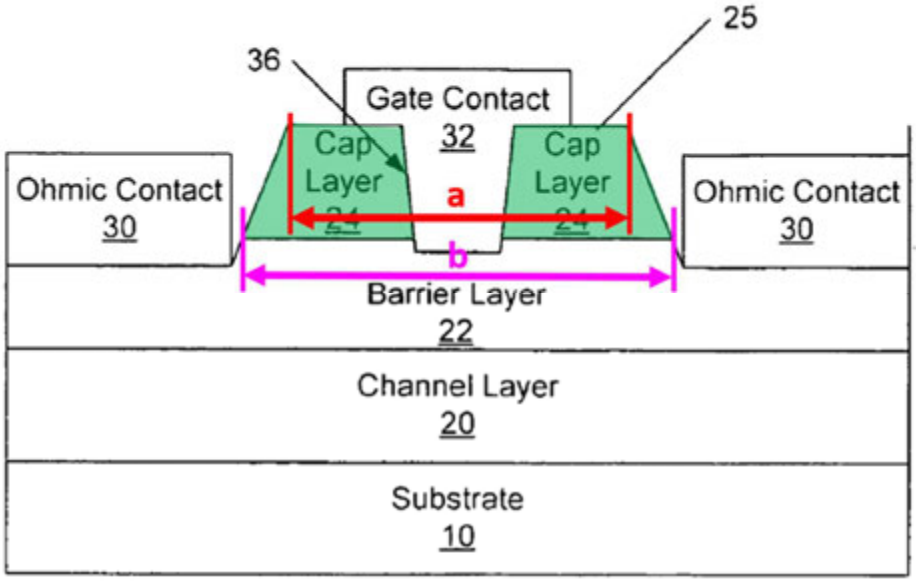
To the extent Patent Owner argues that *Saxler* does not disclose [1d] because its figures do not depict a single p-type gate material having side surfaces extending towards the source and drain, the *Saxler*-*Yoshida* combination of Ground 2 renders it obvious. Shealy, [123]. It would have been obvious to combine *Saxler* and *Yoshida*, resulting in the same figure as the *Saxler* non-recessed embodiment. Shealy, [123]; §VIII.A.4 (Ground 2, Motivation to Combine).



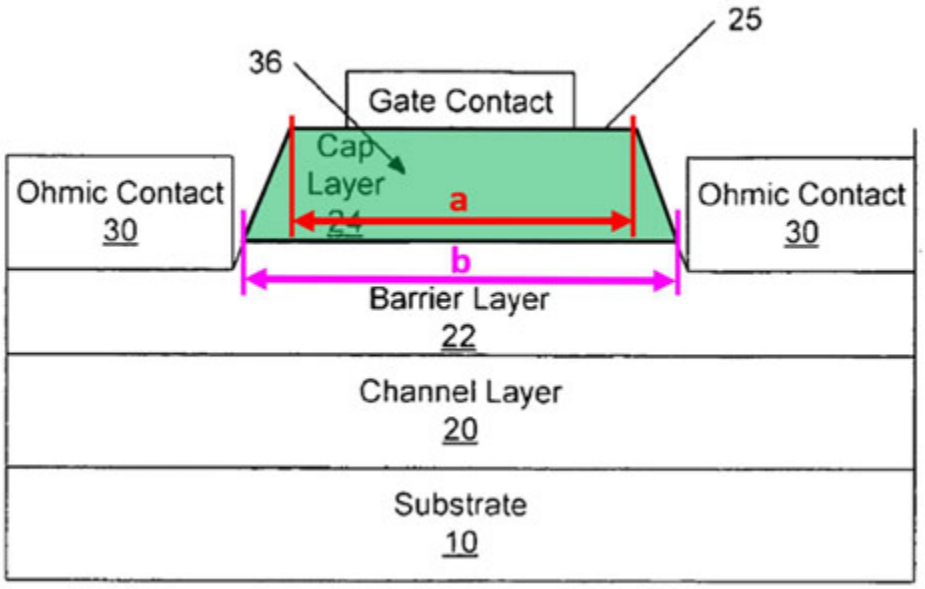
Saxler, Fig. 1A (modified).

<u>Mapping Under Petitioner's Construction</u>

Both *Saxler* alone (Ground 1) or *Saxler-Yoshida* in combination (Ground 2) discloses and renders obvious side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer, which is the proper construction. Shealy, [124]; §VII.A (Claim Construction). In either the recess or non-recess *Saxler* embodiments, the bottom of the **cap layer** (length "**b**," below) is more than 10% wider than the top (length "**a**") (Ground 1). Shealy, [124].

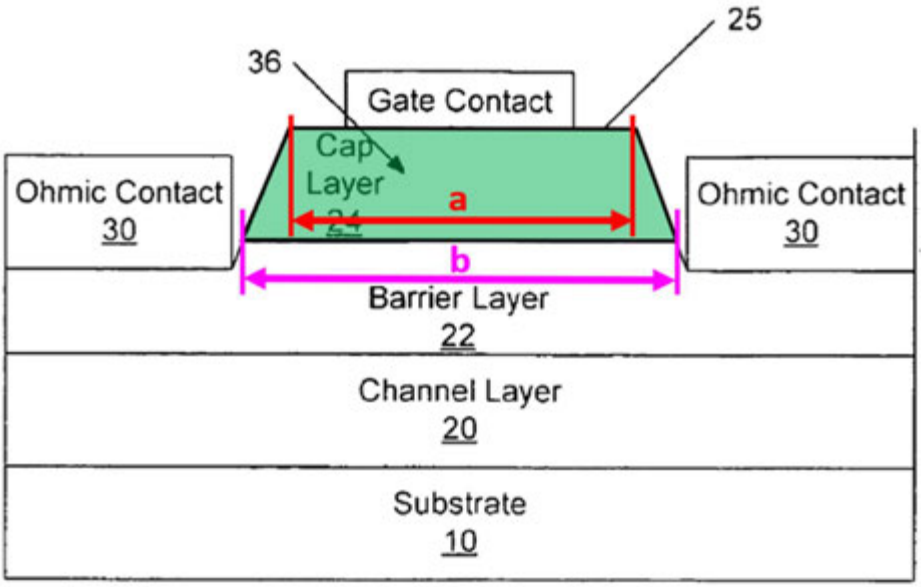


Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

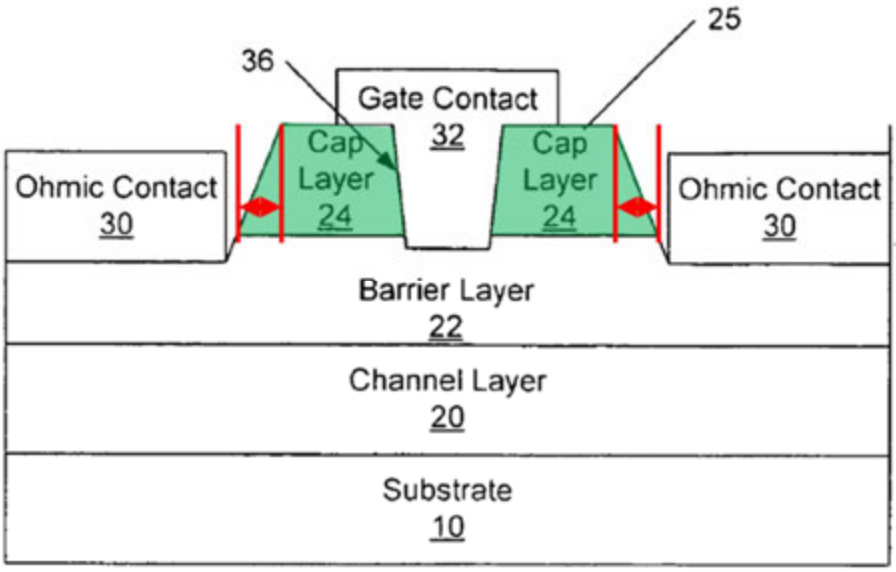
Likewise, in *Saxler-Yoshida*, the bottom of the **cap layer** (length "**b**," below) is more than 10% wider than the top (length "**a**") (Ground 2). Shealy, [125].



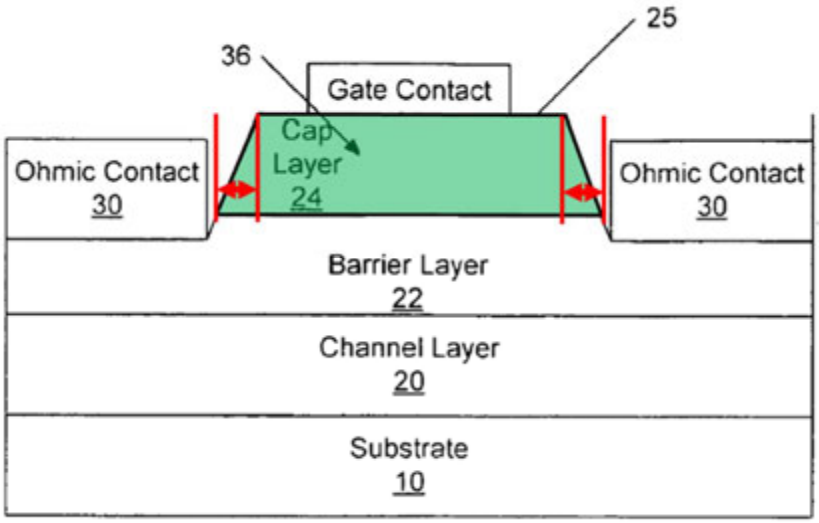
Saxler, Fig. 1A (modified).

<u>Mapping Under Patent Owner's Construction</u>

Both *Saxler* alone (Ground 1) or the *Saxler-Yoshida* in combination (Ground 2) discloses and renders obvious side surfaces of the p-type gate material *such that the bottom of the material is wider than the top of the material* under Patent Owner's construction. Shealy, [126].



Saxler, Fig. 1A.

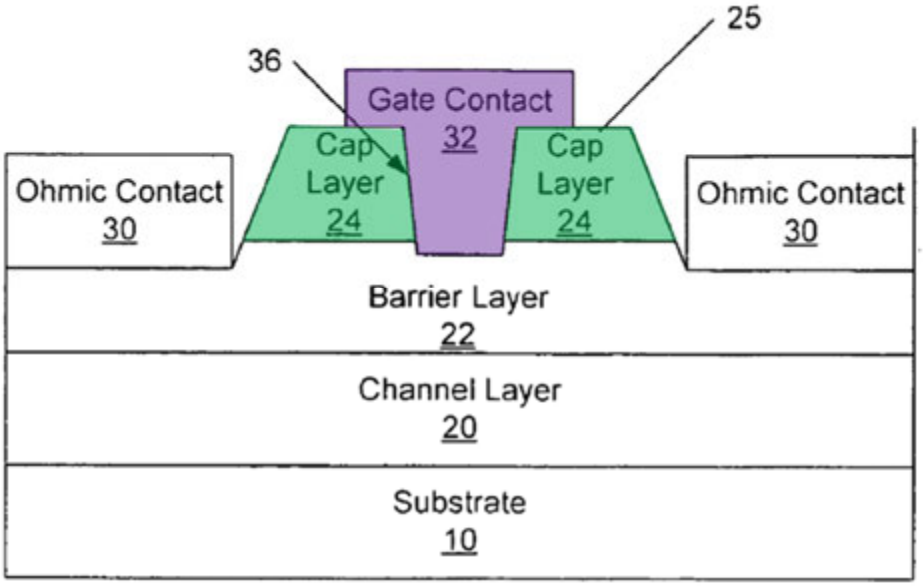


Saxler, Fig. 1A (modified).

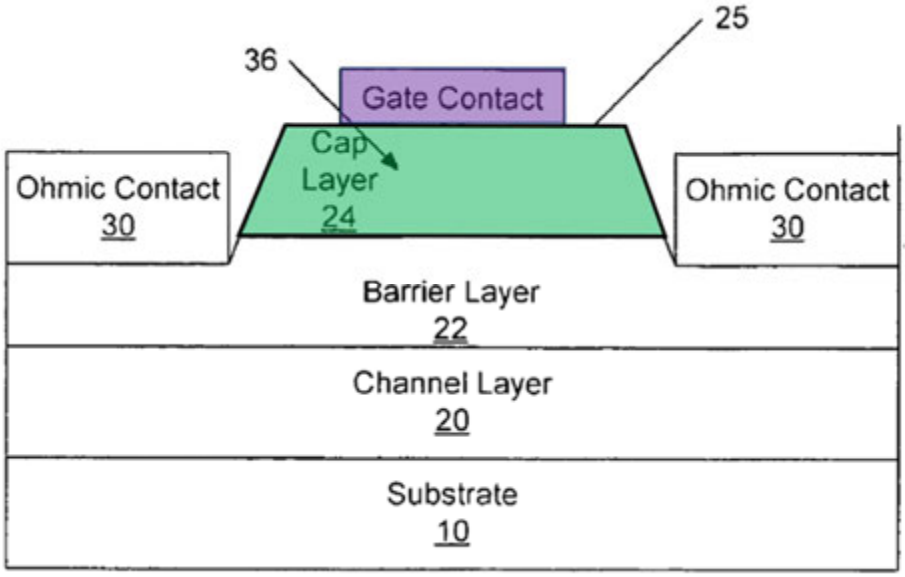
6. [1e]: a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

The patent admits [1e] was conventional and depicts numerous prior art devices disclosing [1e]. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A; Shealy, [127].

Saxler alone renders obvious [1e] (Ground 1). Shealy, [127]-[130]. *Saxler*'s **gate contact** is a gate metal (e.g., "Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WsiN") formed on its **cap layer**. *Saxler*, [0066], Figs. 1A, 2B; Shealy, [128]. As explained, in some embodiments *Saxler* lacks a gate recess and does not separate the **cap layer** into distinct portions. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]–[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [128]; §VIII.B.5 (Grounds 1-2, [1d]). In either embodiment, the sidewalls of its **gate contact** extend vertically towards the **cap layer** just as in the recessed embodiments depicted in Figures 1A and 2B. Shealy, [128].



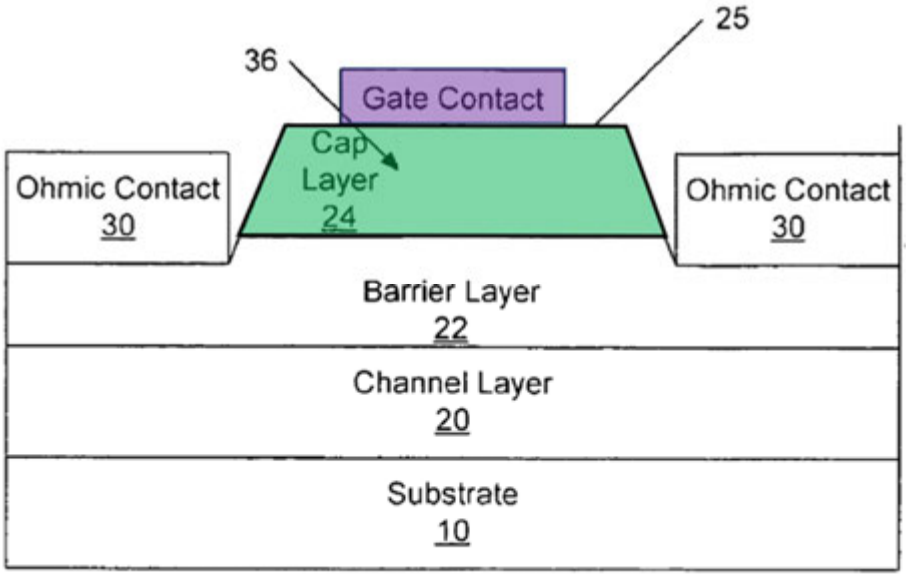
Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

Saxler in view of *Yoshida* also renders obvious [1e] (Ground 2). Shealy, [129]-[130]. Like *Saxler*'s gate contact, *Yoshida*'s **gate electrode** is a metal formed on its p-type GaN **layer 5**. *Yoshida*, [0016]; Shealy, [129]; §X.C.6 (Grounds 1-2, [1e]). It would have been for a POSITA to select a suitable metal for the combined *Saxler*-*Yoshida* system. Shealy, [129]. Gates were conventional in GaN HEMTS and included in both references, and a POSITA would have selected a metal for the gate as a simple design choice, depending on the properties of the system. Shealy, [129] (citing *Yoshida*, [0002]-[0006], [0016] (disclosing "Au/Pt, Al, and the like" as examples of *Yoshida*'s gate electrode)).

Further, the sidewalls of *Saxler-Yoshida*'s **gate contact** extend towards the **cap layer**, as required by [1e] and shown below. *Yoshida*, Fig. 1; *Saxler*, Fig. 1F; Shealy, [130].



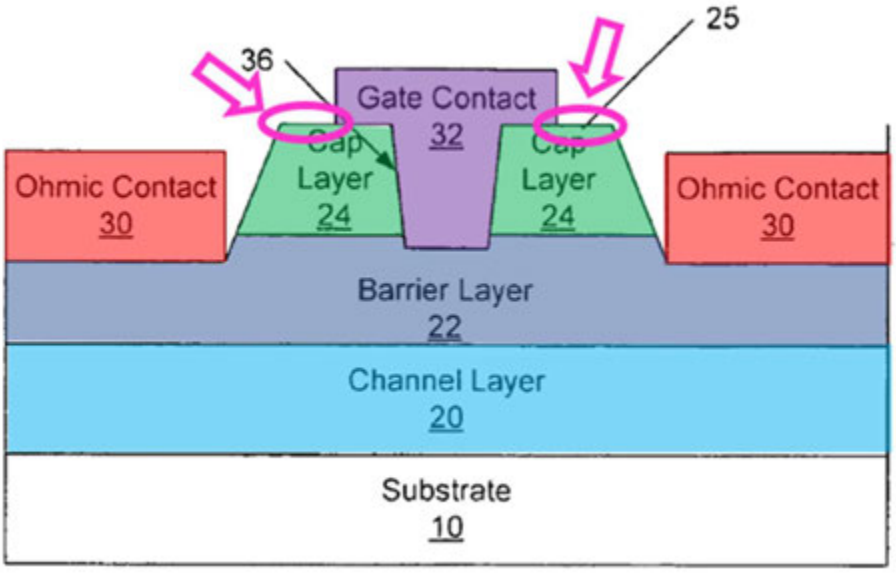
Saxler, Fig. 1A (modified).

7. [1f]: wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

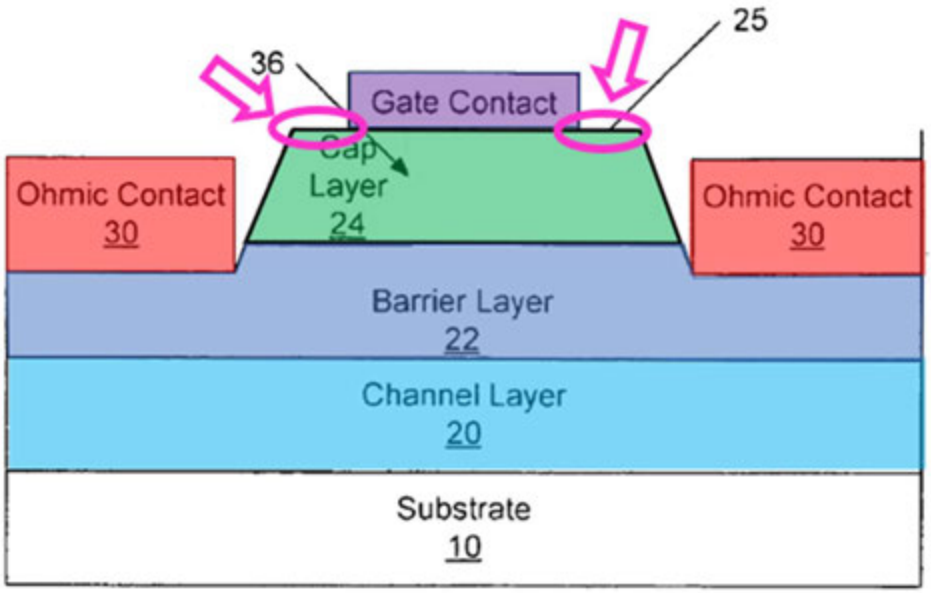
[1f] is the only limitation of independent claim 1 that the '335 patent does not admit is found in the prior art. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A; Shealy, [131]. *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2) renders it obvious. Shealy, [131]-[134]. Yet the priority application *Lidow* notes this limitation was conventional, stating that ledges in a "conventional enhancement mode transistor"

are made using separate masks for the p-type gate material and gate metal. *Lidow*, [0006], Fig. 1.

Under Ground 1, *Saxler* depicts its **gate contact** is narrower than its **cap layer**, thereby exposing **horizontal ledges** with substantially equal widths that extend past the respective sidewalls of the **gate** and toward the **source** and **drain**, as shown in Figure 1A below. *Saxler*, Fig. 1A; Shealy, [132]-[133]. In some embodiments, *Saxler*'s gate recess is not present or does not separate the **cap layer** into distinct portions. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88; Shealy, [133]; §VIII.B.5 (Grounds 1-2, [1d]). A POSITA would have understood *Saxler*'s **gate contact** in non-recessed embodiments (or embodiments where the recess did not extend through the **cap layer**) would similarly be narrower than the **cap layer** to expose the **horizontal ledges**. Shealy, [133]. *Saxler* thereby discloses or at least renders [1f] obvious (Ground 1).*Id*.



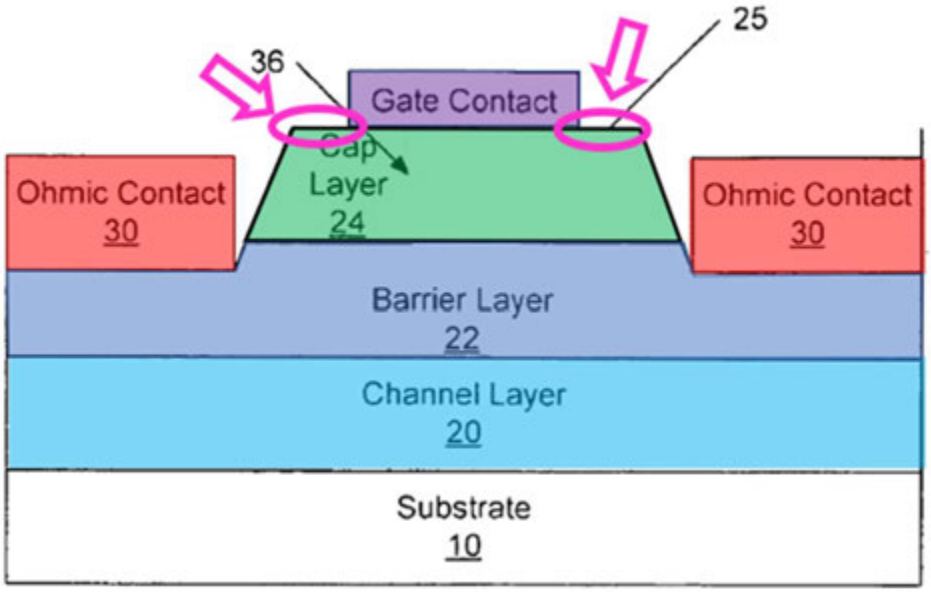
Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

Saxler in view of *Yoshida* also renders obvious [1f] (Ground 2). Shealy, [134]. *Saxler-Yoshida*'s **gate contact** is narrower than its **cap layer**, thereby exposing **horizontal ledges** that extend past the respective sidewalls of the **gate** and toward

the **source** and **drain**. *Yoshida*, [0022]-[0023], Fig. 1; *Saxler*, [0046], Figs. 1A-1F; Shealy, [134]. These ledges are symmetric on either side of the gate (i.e., having substantially equal widths). Shealy, [134].



Saxler, Fig. 1A (modified).

C. [Claim 2]: wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

Claim 2 is drawn to a device but is a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §VII.B (Claim Construction); *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373.

For reasons explained for [1f], claim 2 is obvious over *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2). Shealy, [135]; §VIII.B.7 (Grounds 1-2, [1f]).

D. [Claim 3]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

Saxler discloses claim 3 for the reasons explained for [1b] (Grounds 1-2). *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B]; Shealy, [136]; §VIII.B.3 (Grounds 1-2, [1b]).

E. [Claim 4]: wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width

Claim 4 recites nothing more than that the gate metal is narrower than the p-type gate material, which is already required by [1f] under either Party's construction. As explained for [1f], *Saxler* alone (Ground 1) and/or in view of *Yoshida* (Ground 2) renders obvious this arrangement. *Yoshida*, [0022]-[0023], Fig. 1; *Saxler*, [0014], [0046], claims 1, 18, 20, 29, Fig. 1F; Shealy, [137]; §VIII.B.7 (Grounds 1-2, [1f]).

F. Independent Claim 5

Saxler in view of the knowledge of a POSITA (Ground 1) and in view of *Yoshida* (Ground 2) renders obvious claim 5. Shealy, [138]-[147].

1. [5p] An enhancement-mode GaN transistor, comprising:

[5p] is identical to [1p]. *Saxler* discloses or at least renders it obvious for the reasons explained for [1p] (Grounds 1-2). Shealy, [139]; §VIII.B.1 (Grounds 1-2, [1p]).

2. [5a] a GaN layer;

[5a] is identical to [1a]. *Saxler* discloses it for the reasons explained for [1a] (Grounds 1-2). Shealy, [140]; §VIII.B.2 (Grounds 1-2, [1a]).

3. [5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[5b] is identical to [1b]. *Saxler* discloses it for the reasons explained for [1b] (Grounds 1-2). Shealy, [141]; §VIII.B.3 (Grounds 1-2, [1b]).

4. [5c]: a source contact and a drain contact formed on the barrier layer;

[5c] is identical to [1c]. *Saxler* discloses it for the reasons explained for [1c] (Grounds 1-2). Shealy, [142]; §VIII.B.4 (Grounds 1-2, [1c]).

5. [5d]: a p-type gate material formed above the barrier layer and between the source and drain contacts;

Saxler discloses [5d] for reasons previously explained for[1d] (Grounds 1-2). Shealy, [143]; §VIII.B.5 (Grounds 1-2, [1d]). As explained for [1d], *Saxler*'s cap layer is a p-type GaN, and the cap layer is disposed between source and drain contacts. *Saxler*, [0013], [0064], [0069], [0071], [0073], Figs. 1A, 2B; Shealy, [143]; §VIII.B.5 (Grounds 1-2, [1d]).

6. [5e]: a gate metal disposed on the p-type gate material,

[5e] is included in [1e]. *Saxler* discloses [5e] for the reasons explained for [1e] (Grounds 1-2). Shealy, [144]; §VIII.B.6 (Grounds 1-2, [1e]).

7. [5f]: wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

Claim 5 is drawn to a device but [5f] includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §VII.B; *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373. [5f] otherwise is identical to [1f]. For reasons explained for [1f], [5f] is obvious over *Saxler* alone and/or in view of *Yoshida*. Shealy, [145]-[146]; §VIII.B.7 (Grounds 1-2, [1f]).

Saxler's gate contact is narrower than the underlying cap layer, resulting in the horizontal ledges that extend past sidewalls of the gate metal towards the source contact and drain contact. *Saxler*, [0064]-[0066], Figs. 1A-1B, 2B; Shealy, [146]; §VIII.B.7. The combination of *Saxler* and *Yoshida* also includes these features. Shealy, [146]; §§VIII.A (Overview of Grounds 1-2), VIII.A.4 (Ground 2, Motivation to Combine), VIII.B.7 (Grounds 1-2, [1f]).

8. [5g]: (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

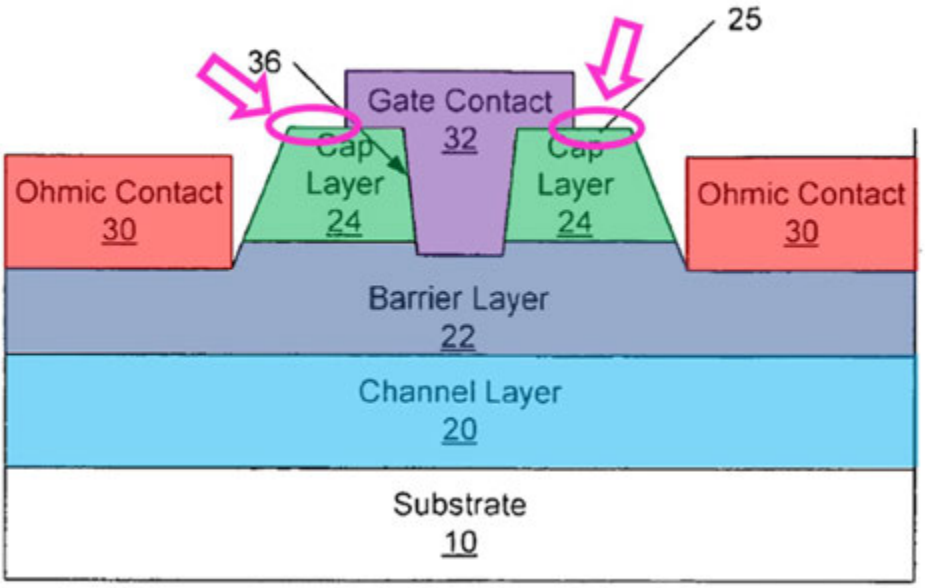
[5g] is identical to [1d]. For reasons explained for [1d], *Saxler* in view of the knowledge of a POSITA (Ground 1) and in view of *Yoshida* (Ground 2) renders obvious [5g]. Shealy, [147]; §VIII.B.5 (Grounds 1-2, [1d]).

G. [Claim 6]: wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

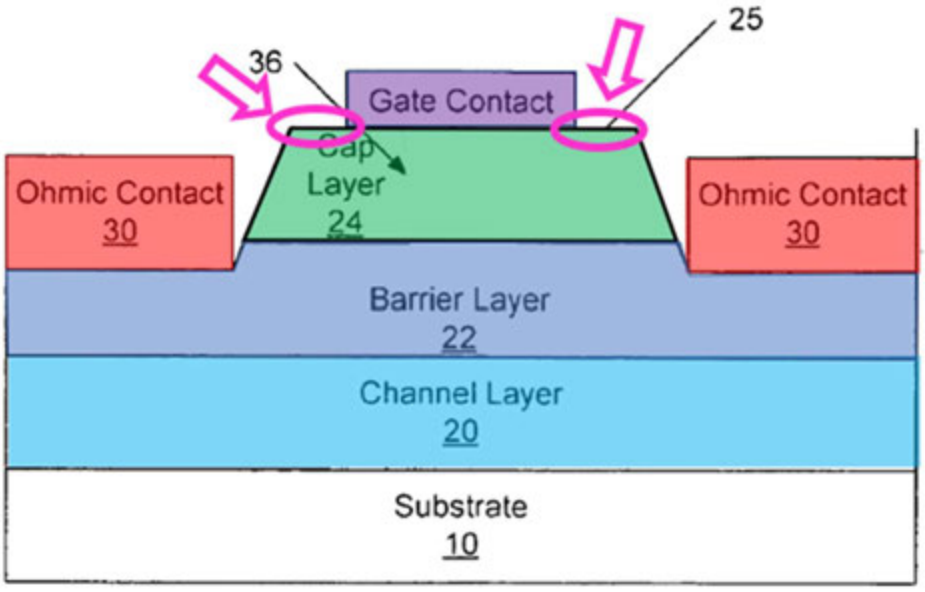
As explained for [1b], *Saxler* discloses an AlGaN barrier layer (Grounds 1-2). *Saxler*, [0007], [0010], [0016], [0058]-[0059], [0069], Figs. 1A, 2B; Shealy, [148]; §§VIII.B.3 (Grounds 1-2, [1b]), VIII.D (Grounds 1-2, Claim 3).

H. [Claim 7]: wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

As explained for [1d] and [1f], *Saxler* discloses its **cap layer** has **symmetric ledges** on either side the **gate contact**, including in embodiments where the cap layer is not recessed. *Saxler*, Abstract, [0012]-[0013], [0027], [0052], [0064], [0070]-[0071], [0073], claims 3, 14, 21, 27, 31, 88, Figs. 1A, 2B; Shealy, [149]; §§VIII.B.5 ([1d]), VIII.B.7 ([1f]). *Saxler* alone thus renders obvious claim 7 (Ground 1).

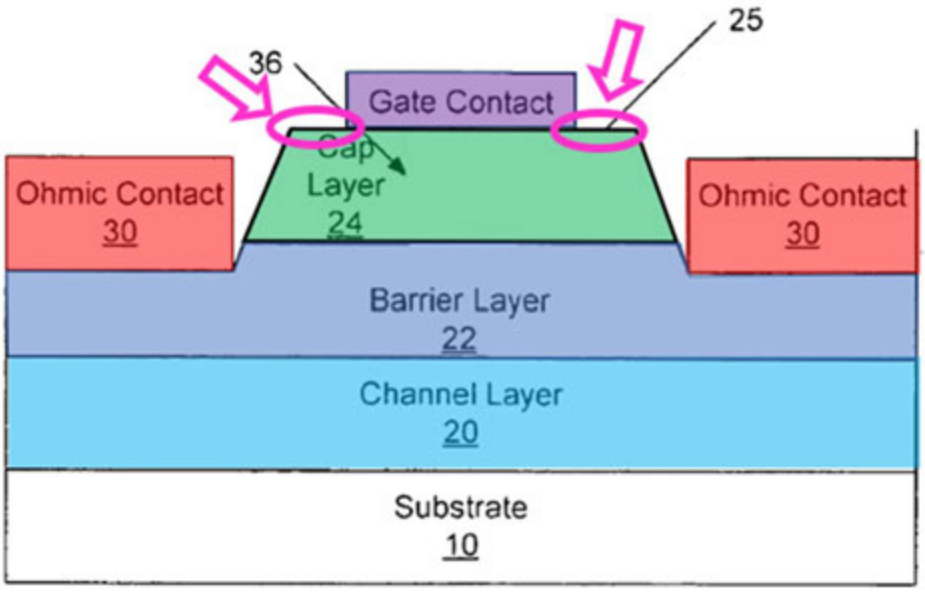


Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

Saxler-Yoshida also includes these features (Ground 2). Shealy, [150]; §VIII.B.7 (Grounds 5, [1f]).



Saxler, Fig. 1A (modified).

IX. Ground 3: *Saxler* in View of *Yoshida*, *Beach*, and *Shenoy* Renders Obvious Claims 2 and 5-7

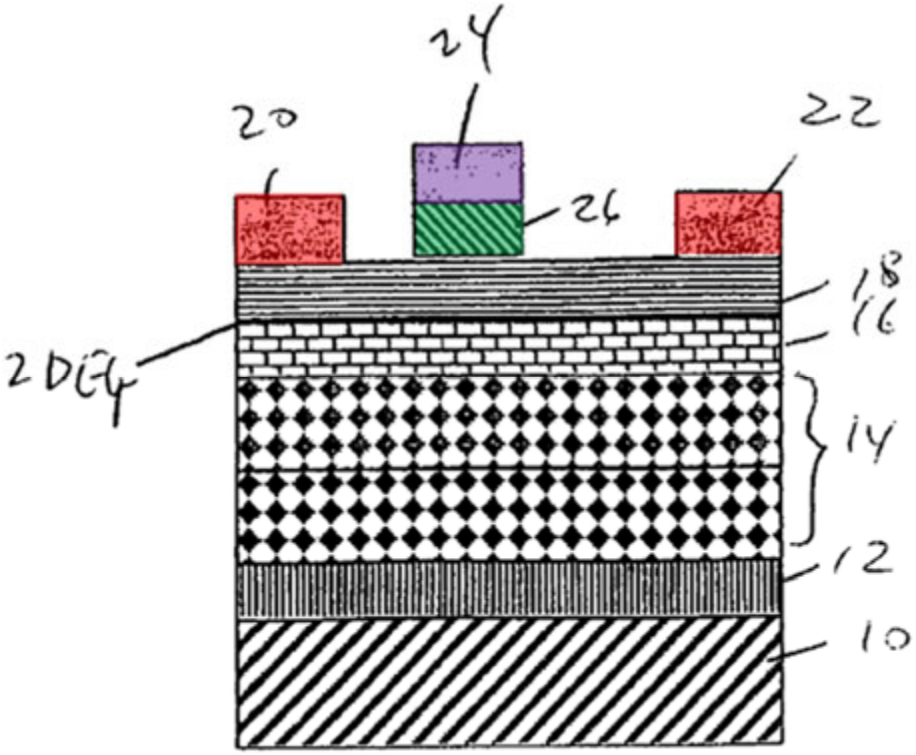
A. Overview of Ground 3

To the extent Patent Owner disagrees that the "self-aligned" recitations of claims 2 and 5 are product-by-process elements that have no patentable weight (§§VII.B, VIII.C, VIII.F.7), the combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* renders obvious claims 2 and 5-7. Shealy, [151]-[181].

1. *Beach*

Beach discloses GaN enhancement-mode devices. *Beach*, Abstract, [0003]-[0018]. *Beach* teaches a self-aligned method of making stacked gate structures in GaN HEMT devices using a single mask. *Id.*, [0040], [0045], [0054]; Shealy, [152]. Another *Beach* publication describes the same approach. *Beach-II*, [0047]-[0048], Figs. 1D-1E; Shealy, [152]. *Beach* discloses steps to deposit and pattern layers with a single mask to arrive at **gate barrier 26** and **gate arrangement 24** above a p-n junction and between **power electrodes**, as shown below. *Beach*, [0040]; Shealy, [152]. Such self-aligned techniques were common in the field as of relevant date for the '335 patent. Shealy, [152]. *Beach*'s "gate arrangement 24"

includes a gate electrode, gate barrier 26 is a GaN semiconductor. *Id.*; *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F.



Beach, Fig. 1.

2. *Shenoy*

Shenoy discloses isotropic etching techniques for undercutting metal below photoresist masks. *Shenoy*, 2-3; Shealy, [153]-[154]. Its techniques for controlling "**undercut U**," illustrated in Figure 1, evolves symmetrically on both sides of a symmetric photomask such that the width of the etched metal structure is less than the photomask. *Shenoy*, 2-3; Shealy, [153]. *Shenoy*'s methods were conventional for etching metals in semi-conductors as of the relevant date of the '335 patent. Shealy,

[153] (citing *Shenoy* and noting it published "well over a decade" before the '335 patent's claimed priority date) .

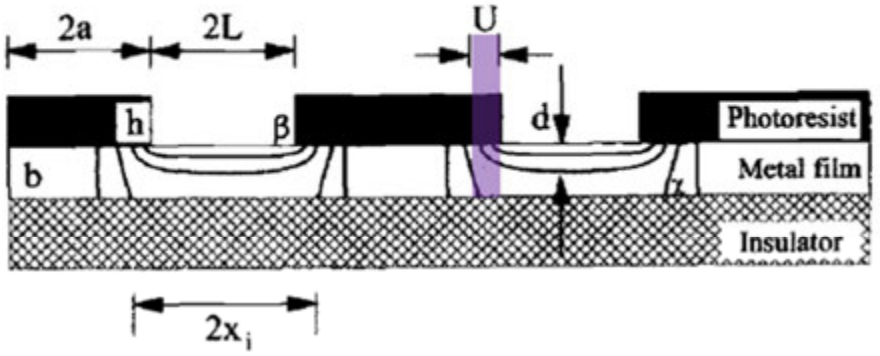


Fig. 1. Schematic diagram of a patterned metal film supported on an insulator.

Shenoy, Fig. 1.

At least as of April 8, 2009, and as early as its publication date of February 22, 1996, *Shenoy* was publicly available and disseminated. *See Shenoy*, 1; Ex. 1025, ¶¶16-26 (Declaration of Kelley Hazel); Shealy, [154]. A POSITA designing GaN transistors routinely accessed similar scholarly articles and would have looked to *Shenoy* for its techniques of etching metals. Shealy, [154].

3. Motivation to Combine

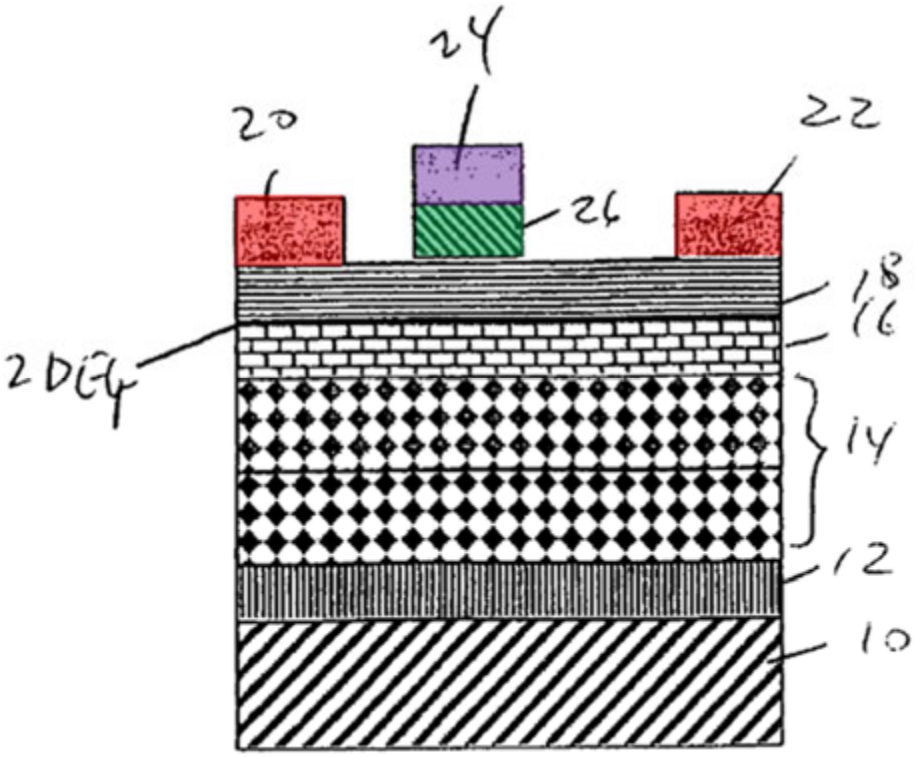
A POSITA would have found it obvious to make the stacked gate structure consisting of a cap layer and gate contact of the *Saxler-Yoshida* GaN HEMT device using the methods of *Beach* and *Shenoy*.§VIII.A.4 (Ground 2: Motivation to Combine); Shealy, [155]-[164].

The *Saxler-Yoshida* combination uses a sequence of steps to arrive at that stacked gate structure. *Saxler*'s process includes: (i) forming cap layer 24 on the barrier layer (*Saxler*, [0061], Fig. 1B); (ii) masking and etching the cap layer "to expose the underlying barrier layer 22," for formation of ohmic contacts 30, which creates sloped sidewalls of the cap layer (*id.*, [0064], Figs. 1A-1B); (iii) patterning to deposit the ohmic contacts (*id.*); (iv) removing the mask in non-recessed embodiment or optionally using a second mask to etch and form a gate recess (*id.*, [0065]); (v) removing the mask (*id.*, [0064]-[0066]); and (v) forming a gate contact (*id.*, [0066]). Shealy, [156]. *Sheppard*, incorporated by *Saxler* to disclose methods of fabricating *Saxler*'s GaN HEMTs (*Saxler*, [0046], [0068]), describes a similar process. *Sheppard*, [0044]-[0051], Figs. 1A-1F. In the *Saxler-Yoshida* combination, step (iv) would employ the non-recessed option. Shealy, [157]; §VIII.A.4 (Ground 2: Motivation to Combine). To reliably locate the gate metal, a POSITA would have understood a second patterning step would have been performed, and that second mask would be removed. Shealy, [156]-[158] (citing *Saxler*, [0046], [0061], [0064]-[0066], [0068], Figs. 1A-1B; *Sheppard*, [0044]-[05051], Figs. 1A-1F). A POSITA would have been motivated to simplify this process and reduce costs by using fewer masking steps. *Id*.

A POSITA would have been familiar with many ways to create *Saxler-Yoshida*'s stepped gate structure and would have used these methods

interchangeably. Shealy, [060]-[062] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [159]; §II (Technological Background, discussing common methods to create stepped gate structures). A POSITA would have found it obvious to modify *Saxler-Yoshida* by using *Beach*'s self-aligned technique and *Shenoy*'s isotropic etching to arrive at that same gate structure, which would improve reproducibility and symmetry of the gate contact with respect to the cap layer. Shealy, [159]. *Ahn* discloses this same approach for making a stepped gate in a thin-film transistor. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C; Shealy, [159]. POSITA would have been further motivated to use this approach to reduce masking steps and reduce costs. Shealy, [159].

Beach teaches a method of making stacked gate structures in GaN HEMT devices that uses a single mask and ensures alignment of layers. *Beach*, [0040], [0045], [0054]; *Beach-II*, [0047]-[0048]; Shealy, [160]. *Beach*'s gate structure includes the "gate arrangement 24," which comprises a gate electrode and an underlying "gate barrier 26," a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Shealy, [160]. *Beach*'s process (i) deposits "**gate barrier 26**" and "**gate arrangement 24**" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits **power electrodes**. *Beach*, [0040]; Shealy, [160]. Such self-aligned techniques were common in the field as of relevant date. Shealy, [160].



Beach, Fig. 1.

A POSITA would have found it obvious to use *Beach*'s approach to create *Saxler-Yoshida*'s gate structure, which would have improved alignment between layers. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3; Shealy, [161]-[164]. It would have been obvious to look to *Beach* for its simple methods of making stacked gate structures. Shealy, [161] (citing *Sheppard* [0058]; *Saxler* [0046], [0068]). Indeed, *Sheppard*, expressly incorporated by *Saxler* to disclose methods of fabricating GaN HEMTs (*Saxler*, [0046], [0068]), describes a flexible approach to masking and etching. It notes that "operations described as multiple steps could be combined into a single step" and vice versa, making the choice of *Beach*'s manufacturing steps no more than simple substitutions. *Sheppard*, [0058]; Shealy, [161].

Beach does not disclose steps to create the **horizontal ledges** of *Saxler-Yoshida*'s stacked gate structure following its self-aligned process. As previously explained, *Shenoy* discloses simple isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks. *Shenoy*, 2-3; Shealy, [162]; §IX.A.2 (*Shenoy*).

Saxler and *Sheppard*, incorporated by reference to disclose methods of forming gate structures (*Saxler* [0046] (referencing Ser. No. 10/897,726), [0068] (same)), each describe using several conventional techniques to etch the cap layer and generate the slope sidewalls shown in their figures. *Saxler*, [0064], Figs. 1A-1B; *Sheppard*, [0044], Figs. 1B-1C. Shealy, [163].

A POSITA would have found it obvious to use *Beach*'s self-aligned method of making *Saxler-Yoshida*'s stacked gate structure in a GaN HEMT and use *Shenoy*'s methods to undercut the **gate electrode** and create *Saxler-Yoshida*'s **horizontal ledges** and **slope cap** layer. Shealy, [164]. Such a combination of steps was already known in the art for creating stepped, stacked transistor gates. *Ahn*; Shealy, [164]. A POSITA would have found the combination a simple substitution of *Beach*'s and *Shenoy*'s known methods that could be predictably implemented in *Saxler*'s flexible method of manufacturing to improve alignment and symmetry between layers and reduce steps and costs. *Saxler*, [0046], [0068]; *Sheppard*, [0058]; Shealy, [164].

B. [Claim 2]

Claim 2 is drawn to a device but is a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §VII.B (Claim Construction); *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373. The combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* nevertheless render obvious claim 2, even if it did lend patentable weight. Shealy, [165]-[168].

Beach discloses a stacked "***self-aligned*** gate arrangement" using a single photo mask to etch both the "gate arrangement 24" (gate electrode) and the underlying "gate barrier 26" (GaN semiconductor) that is the same process depicted in the '335 patent at Figures 6A-6B. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Ex. 1001, 4:14-26; *Beach-II*, [0047]-[0048], Figs. 1D-1E; Shealy, [166]; §§III.A.1 ('335 Patent Overview), IX.A.1 (Ground 3, *Beach*), XI.A.1 (Ground 3, Motivation to Combine), XI.B (Ground 3, Claim 2), IX.A.3 (Ground 3, Motivation to Combine).

Shenoy discloses etching a photomask to isotropically undercut the metal layer below the photomask that is the same process depicted in Figures 6B-6C of the '335 patent. *Shenoy*, 2-3; Ex. 1001, 4:23-39; Shealy, [167]; §§III.A.1 ('335 Patent Overview), IX.A.2 (Ground 3, *Shenoy*), XI.A.1 (Ground 3, Motivation to Combine), XI.B (Ground 3, Claim 2), IX.A.3 (Ground 3, Motivation to Combine).

It would have been obvious to use *Beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make the gate structure of *Saxler*-*Yoshida*. Shealy, [168]; §IX.A.3 (Ground 3, Motivation to Combine). That approach involved simple substitutions of known manufacturing techniques that could be implemented in *Saxler*'s flexible method of manufacturing. Shealy, [168]; §IX.A.3 (Ground 3, Motivation to Combine).

C. Independent Claim 5

The combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* renders obvious claim 5. Shealy, [169]-[178].

1. [5p]

As explained in Grounds 1-2, *Saxler* discloses [1p]. Shealy, [170]; §VIII.F.1 (Grounds 1-2, [5p]).

2. [5a]

As explained in Grounds 1-2, *Saxler* discloses a GaN layer. Shealy, [171]; §VIII.F.2 (Grounds 1-2, [5a]).

3. [5b]

As explained in Grounds 1-2, *Saxler* discloses [5b]. Shealy, [172]; §VIII.F.3 (Grounds 1-2, [5b]).

4. [5c]

As explained in Grounds 1-2, *Saxler* discloses [5c]. Shealy, [173]; §VIII.F.4 (Grounds 1-2, [5c]).

5. [5d]

As explained in Grounds 1-2, *Saxler* alone and/or in combination with *Yoshida* discloses [5d]. Shealy, [174]; §VIII.F.5 (Grounds 1-2, [5d]).

6. [5e]

As explained in Grounds 1-2, *Saxler* alone and/or in combination with *Yoshida* discloses [5e]. Shealy, [175]; §VIII.F.6 (Grounds 1-2, [5e]).

7. [5f]

Claim 5 is drawn to a device, but [5f] includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §VII.B (Claim Construction); *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373. Nevertheless, the combination of *Saxler*, *Yoshida*, *Beach*, and *Shenoy* renders obvious [5f]. Shealy, [176]-[177].

As explained in Grounds 1-2, *Saxler* alone and/or in combination with *Yoshida* includes the structural features of [5f]. Shealy, [177]; §VIII.F.7 (Grounds 1-2, [5f]). And as explained in Ground 3, the *Saxler*-*Yoshida* combination in view of *Beach* and *Shenoy* discloses that these ledges are self-aligned, as claimed. Shealy, [177]; §VIII.F.7 (Grounds 1-2, [5f]).

8. [5g]

Saxler alone and/or in view of *Yoshida* discloses [5g] for reasons explained for Grounds 1-2. Shealy, [178]; §VIII.F.8 (Grounds 1-2, [5g]).

D. [Claim 6]

Saxler discloses claim 6 for reasons explained for Grounds 1-2. Shealy, [179]; §§VIII.B.3 (Grounds 1-2, [1b]), VIII.C (Grounds 1-2, Claim 2), VIII.G (Grounds 1-2, Claim 6).

E. [Claim 7]

Saxler alone and/or in view of *Yoshida* includes the features of claim 7 for reasons explained for Grounds 1-2. Shealy, [180]-[181]; §VIII.H (Grounds 1-2, claim 7).

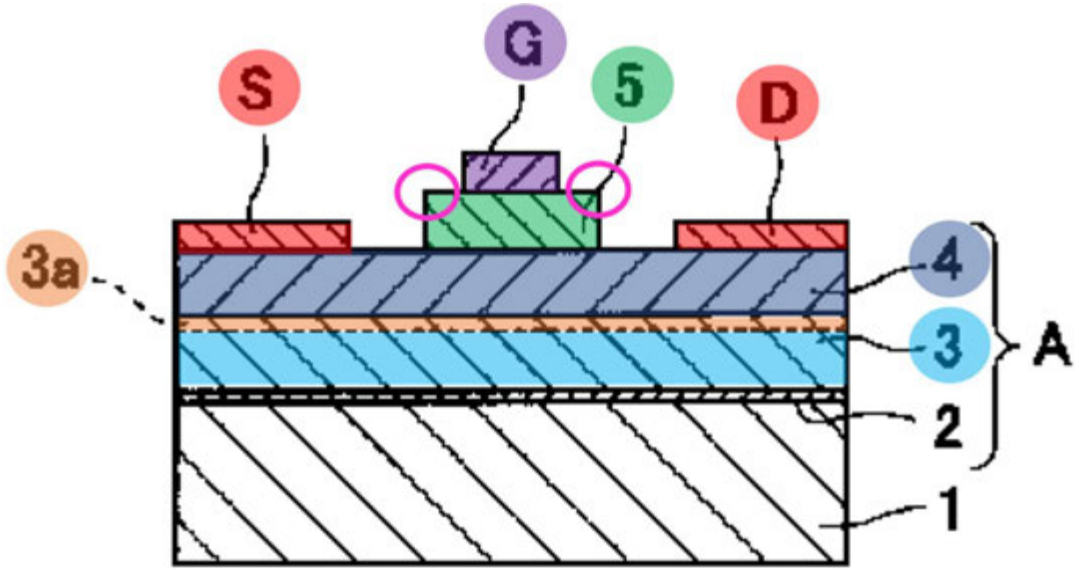
Further, *Beach*'s method of self-aligning the gate structure in combination with *Shenoy*'s methods of symmetrically undercutting the gate metal would have yielded symmetric ledges in the *Saxler*-*Yoshida* device. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3; Shealy, [181]; §§IX.A.3 (Ground 3, Motivation to Combine), IX.B (Ground 3, Claim 2).

X. Grounds 4 and 5: *Yoshida*, Either Alone or In View of *Saxler* Renders Obvious Claims 1-7

A. Ground 4: *Yoshida* Alone

Yoshida discloses the arrangement of semiconductor layers and structures of claims 1-7, including the claimed ledges. Although *Yoshida* depicts that the walls of its p-type GaN material are vertical and not sloped as required by [1d] and [5g], sloped sidewalls were common and obvious, at least because perfectly vertical sidewalls were rare in practice. Under Patent Owner's construction of the slope terms ("p-type gate material having side surfaces extending horizontally such that

the bottom of the material is wider than the top of the material"), a POSITA would know any constructed embodiment would necessarily extend at least slightly on the bottom due to manufacturing tolerances. Shealy, [182], [203]-[205] (citing *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5); *Yoshida* thus renders obvious claim 1-7 (Ground 4) under at least Patent Owner's construction of the slope terms. Shealy, [182], [190]-[205], [210]-[231].



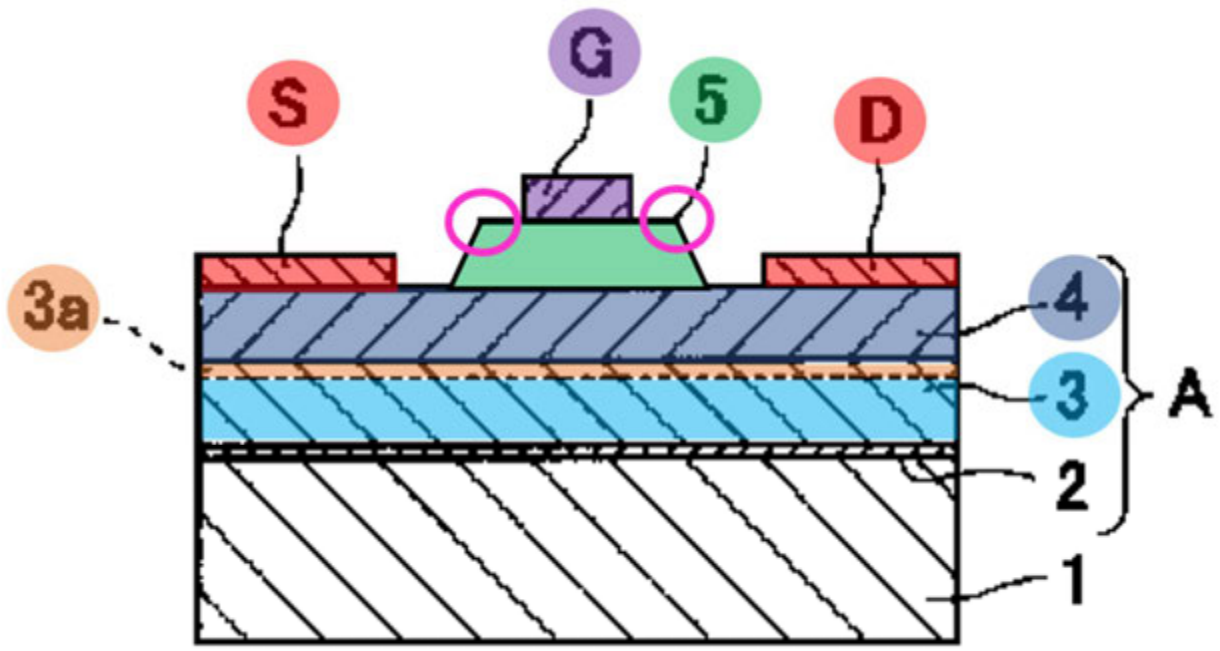
Yoshida, Fig. 1.

B. Ground 5

1. Ground 5: The Combination of *Yoshida* in View of *Saxler*

To the extent Patent Owner disagrees, however, and also under Petitioner's construction of the slope terms, *Saxler* discloses such sloped sidewalls under either construction, and the combination of *Yoshida* and *Saxler* also renders obvious claims 1-7 (Ground 5). Shealy, [183]-[231].

Implementing *Saxler*'s **sloped sidewalls** in *Yoshida*'s **layer 5** results in the following combined structure. Shealy, [184].



Yoshida, Fig. 1 (modified).

2. Ground 5: Motivation to Combine

It would have been obvious to modify *Yoshida*'s transistor with the sloped sidewalls of *Saxler*'s capping layer to reduce gate leakage. Shealy, [185]-[189]. The combination calls for nothing more than the simple substitution of *Saxler*'s sidewalls to predictably make an enhancement-mode GaN HEMT. *Id.* And a POSITA would have recognized *Saxler*'s sidewalls would have reliably reduced *Yoshida*'s gate leakage, making the combination obvious. *Id.*

The references are compatible for the reasons explained in Ground 2. Shealy, [186]; §VIII.A.4 (Motivation to Combine). In view of these many similarities, it

would have been obvious to incorporate *Saxler*'s known sloped **cap layer** sidewalls into *Yoshida* p-type **layer 5**. Shealy, [186]. Indeed, sloped sidewalls were conventional, as the '335 patent admits. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A; Shealy, [186]. The '335 patent provides "conventional schematic[s] [of an] enhancement mode GaN transistor" depicting just such sloped sidewalls. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A; Shealy, [186]. The angle of *Saxler*'s sloped sidewall is typical for known mesa structures. Shealy, [186]. It would have been a simple substitution of *Yoshida*'s vertical sidewalls with *Saxler*'s sloped sidewalls to predictably yield an enhancement-mode GaN HEMT. Shealy, [186].

A POSITA would have readily understood how to implement the combination. Shealy, [187]. *Saxler* discloses conventional etching techniques for straightforwardly forming its sloped sidewalls. *Saxler*, [0064]; Shealy, [187]. *Yoshida* also forms its p-type **layer 5** through etching. *Yoshida*, [0022]; Shealy, [187]. It would have been a simple substitution to employ *Saxler*'s etching approach to predictably shape *Yoshida*'s sidewalls. Shealy, [187].

Accordingly, a POSITA would have recognized that *Saxler* provided a known option for shaping the sidewalls of *Yoshida*'s p-type **layer 5**, and the combination would have been obvious.

A POSITA would have additionally recognized that *Saxler*'s sloped sidewalls would have beneficially reduced *Yoshida*'s leakage losses and found the

combination obvious. Shealy, [189]. It was known that leakage in transistors included mesa edge currents and that sloped walls led to longer leakage paths and thereby lowered gate leakage. *Id.*; *Xu*, 1; *Kanda*, [0013], [0027], [0144], [0157], Fig. 12A. The '335 patent itself recognizes that capping structures in prior art enhancement-mode GaN transistors with sloped sidewalls had a known "gate leakage current path 201 [that] flows along the sidewall of the p-type gate material 101." Ex. 1001, 1:64-2:8, Fig. 2. A POSITA would have understood that the geometry of *Saxler*'s sloped sidewalls provided longer leakage paths than *Yoshida*'s vertical sidewalls, thereby lowering gate leakage. Shealy, [189]. That improvement makes *Saxler*'s sloped sidewalls a suitable option, motivating the combination. *KSR*, 550 U.S. at 417 (a motivation arises when a known technique that "improve[d] one device … would improve similar devices in the same way."); *Intel*, 61 F.4th at 1379-81.

C. Independent Claim 1

Yoshida in view of the knowledge of a POSITA (Ground 4) and in view of *Saxler* (Ground 5) renders obvious claim 1, under Patent Owner's construction and either construction, respectively.

1. [1p]

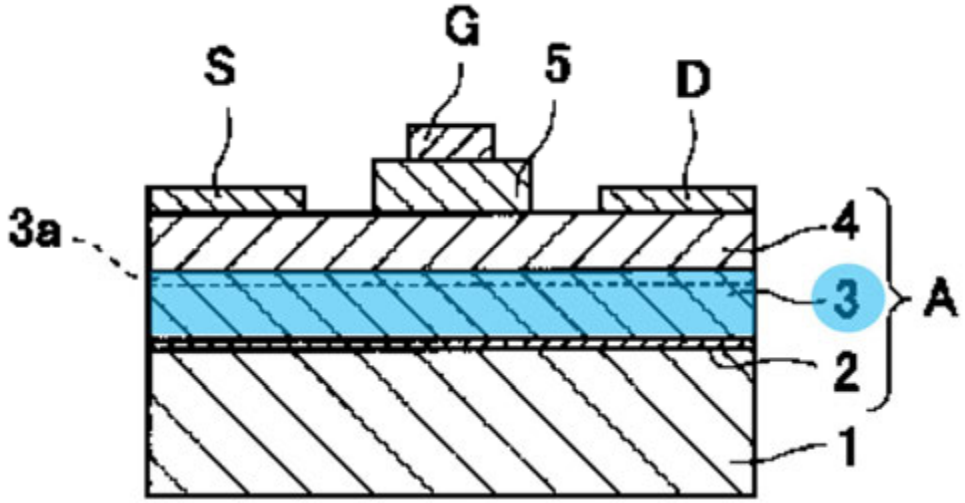
To the extent limiting, *Yoshida* discloses the preamble (Grounds 4-5). Shealy, [191]. *Yoshida* discloses a GaN high-mobility transistor that includes a p-type GaN

layer below the gate, which "enables voltage control with a small amount of carrier injection," constituting a normally-off enhancement-mode GaN transistor. *Yoshida*, [0017], [0015], Fig. 1; Shealy, [191].

2. [1a]

The '335 patent admits enhancement-mode GaN HEMT devices typically included a GaN layer. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B; Shealy, [192].

Yoshida discloses a GaN layer (Grounds 4-5). *Yoshida*'s teaches that "i-type GaN is [a] particularly preferrable" embodiment of "**layer 3**," which is an intrinsic or undoped GaN. *Yoshida*, Abstract, [0012], Fig. 1; Shealy, [192]-[193].



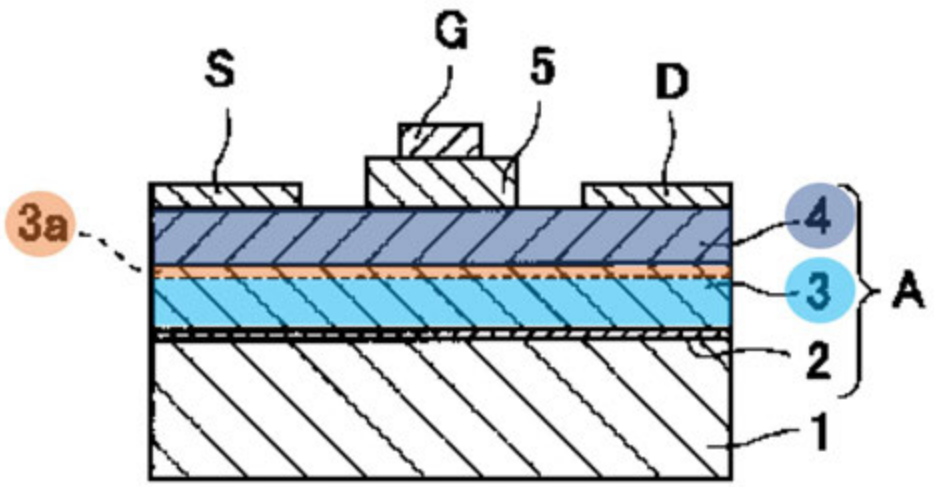
Yoshida, Fig. 1.

3. [1b]

The '335 patent admits [1b] was conventional. It notes GaN HEMTs "typically include[d] a barrier layer of AlGaN adjacent to a layer of GaN," inducing

a 2DEG at the AlGaN-GaN interface. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B; Shealy, [194].

Yoshida also discloses [1b] (Grounds 4-5). Shealy, [194]-[195]. *Yoshida*'s "**layer 4**" is a barrier layer disposed on GaN **layer 3**. *Yoshida*, Abstract, [0010], [0013], Fig. 1; Shealy, [195]-[196].



Yoshida, Fig. 1.

Yoshida identifies that "n-type AlGaN is [a] favorable" choice for **layer 4**. *Yoshida*, Abstract, [0010], [0013], Fig. 1; Shealy, [196]. The '335 patent likewise discloses that the claimed barrier layer may be an AlGaN layer, which is covered in dependent claims. Ex. 1001, 1:42-63, 3:37-48, 4:16-22, claims 3, 6; Shealy, [196].

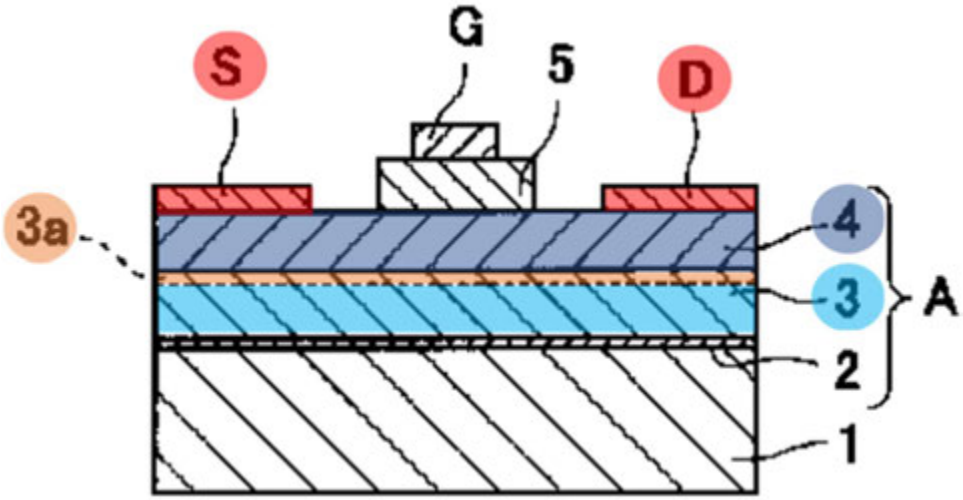
Yoshida further discloses "**two-dimensional electron gas layer 3a** is ***formed at the*** heterojunction ***interface*** between n-type semiconductor **layer 4** and i-type

semiconductor **layer 3**, and more specifically at the topmost portion of i-type semiconductor **layer 3**." *Yoshida*, [0016]; Shealy, [197].

4. [1c]

The contacts of [1c] were entirely conventional, as the '335 patent admits. Ex. 1001, 1:64-2:19, Figs. 1-2, 3A-3B; Shealy, [198].

Yoshida discloses **source** and **drain electrodes** (contacts) that are "directly loaded" (formed) on barrier **layer 4** (Grounds 4-5). *Yoshida*, Abstract, [0014], [0022], Figs. 1-2, 3A-3B; Shealy, [198]-[199].



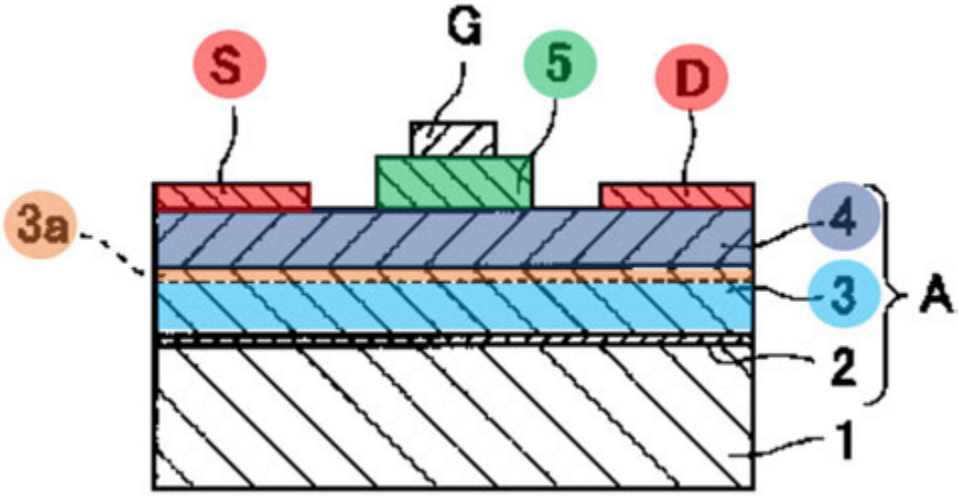
Yoshida, Fig. 1.

5. [1d]

The '335 patent admits [1d] was conventional. Ex. 1001, 1:42-2:26, Figs. 1-2, 3A-3B; Shealy, [200].

Yoshida in view of the knowledge of a POSITA (Ground 4) and in view of *Saxler* (Ground 5) renders obvious [1d]. Shealy, [200]-[209].

Yoshida's **layer 5** is "a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces … contacting the barrier layer," as recited in claim 1. **Layer 5** may be a single- or double-layer comprising a "p-type GaN." *Yoshida*, Abstract, [0009], [0015], [0018], claim 2; Shealy, [202].

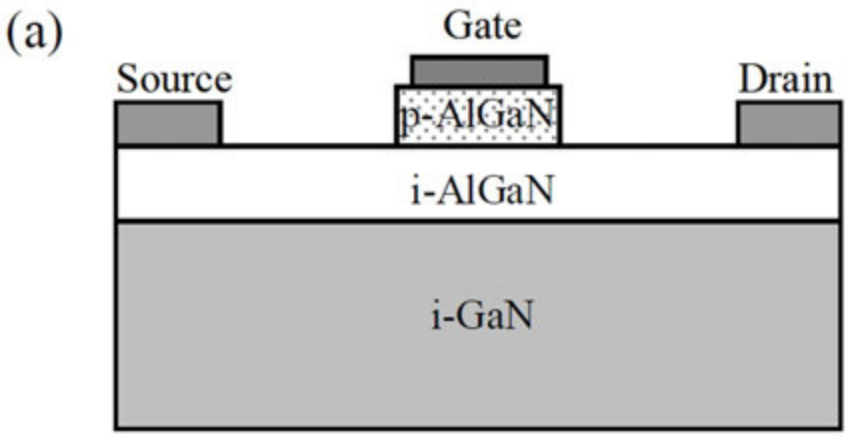


Yoshida, Fig. 1.

Mapping Under Patent Owner's Construction (Ground 4-5)

Ground 4: *Yoshida* renders obvious sloped sidewalls that extend horizontally towards source and drain contacts if the claimed extension of the side surfaces is interpreted to include any amount extension beyond a perfectly vertical sidewall, as Patent Owner contends. Shealy, [203]-[205] (citing *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5). Although *Yoshida* draws substantially vertical sidewalls of p-type **layer 5**, a POSITA would have known a sidewall drawn vertically would have a slight slope when built in a practical device. *Id.*

A POSITA would have been familiar with this principle. Shealy, [204] (citing *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5). For example, *Saxler* notes that, in practice, "an etched region illustrated as a rectangle will, typically, have ***tapered***, rounded or curved features." *Saxler*, [0042]; Shealy, [204]. As another example, a 2006 IEEE paper on a GaN HEMT with a similar gate structure to *Yoshida* depicts its p-AlGaN gate layer having vertical sidewalls in its drawings (Fig. 1) but shows sloped sidewalls extending horizontally towards source and drain contacts in a microscope image of a device built according to the drawings. *Uemoto*, Figs. 1-2, Fig. 5; Shealy, [204].



Uemoto, Fig. 1(a) (drawing).

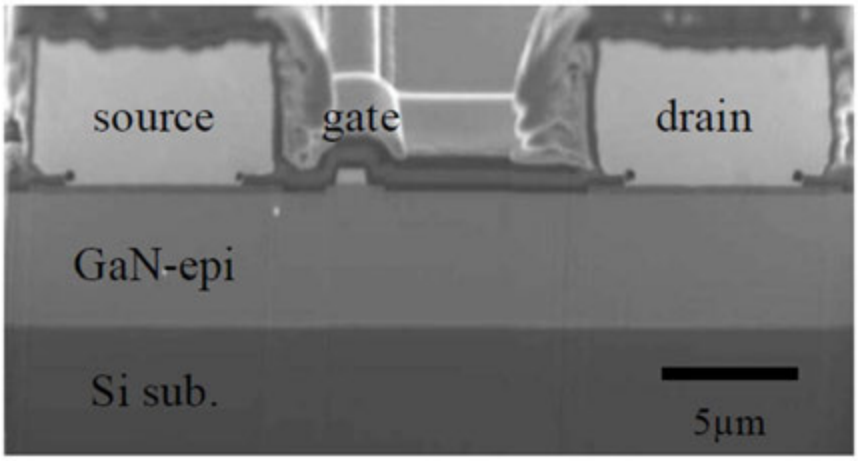
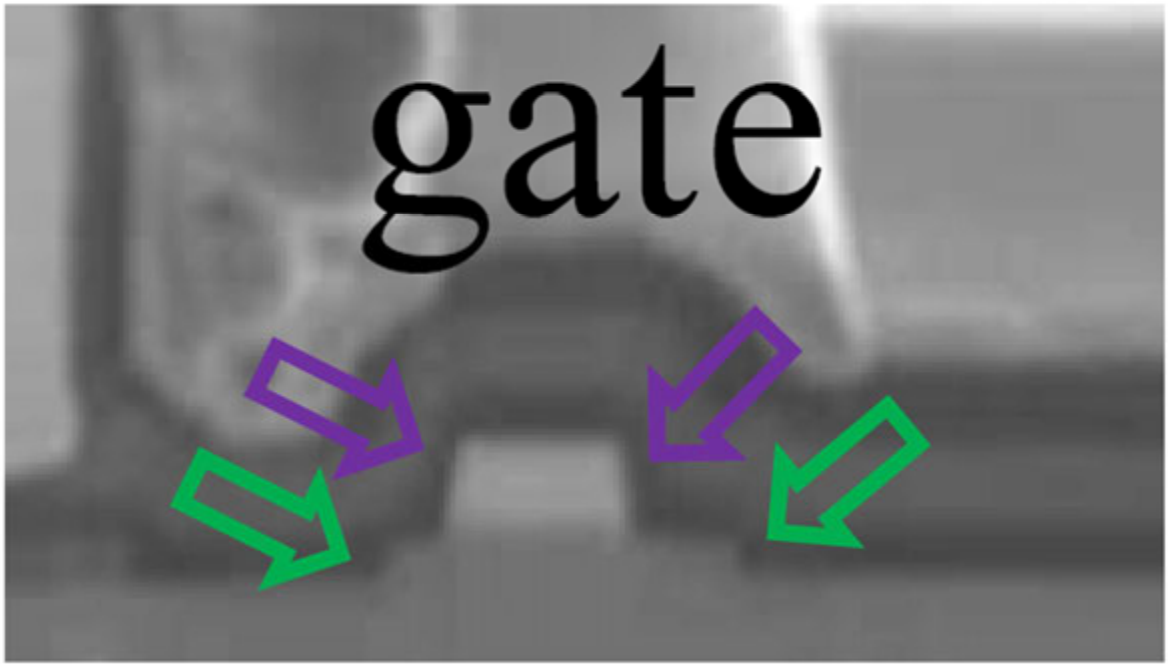


Fig.5 Cross sectional SEM image of GIT on a Si substrate.

Uemoto, Fig. 5 (microscope image).



Uemoto, Fig. 5 (showing sloped sidewalls of the **p-AlGaN** layer and **gate metal**).

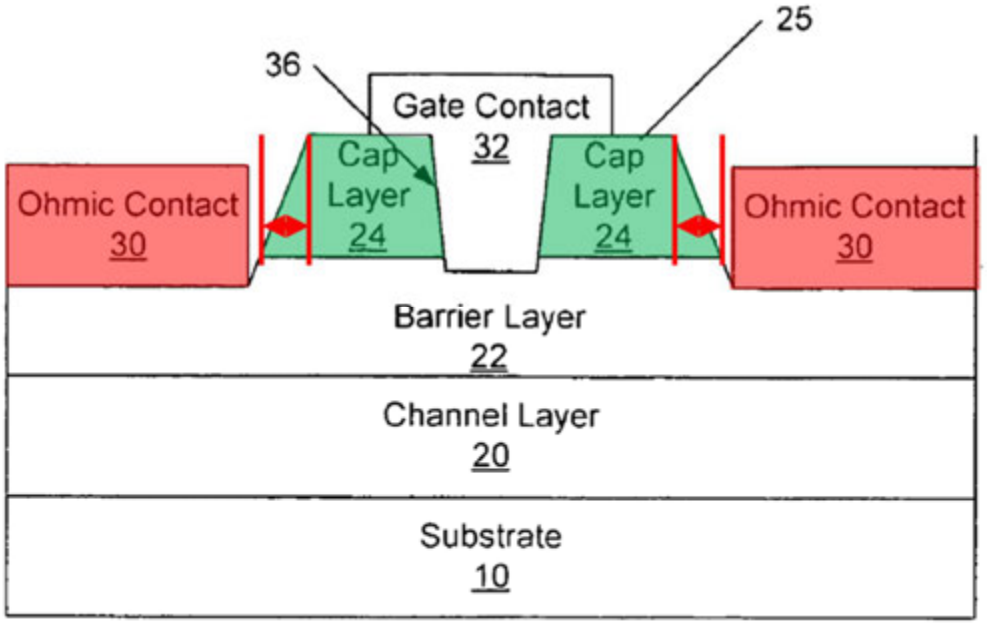
If the construction of the claimed side surfaces is interpreted to cover any amount extension beyond a perfectly vertical sidewall, a POSITA would have

recognized that *Yoshida*'s sidewalls would have had a taper in practical implementations, and *Yoshida* alone thereby renders obvious [1d] (Ground 4). Shealy, [203]-[205] (citing *Saxler*, [0042]; *Uemoto*, Figs. 1-2, 5).

Ground 5: *Yoshida*'s drawing shows substantially vertical sidewalls of layer 5. *Yoshida*, Fig. 1. While a POSITA would know those sidewalls do extend towards the **source** and **drain contacts** under Patent Owner's construction in real life, in the diagram the sidewalls are perfectly vertical. *Saxler*, however, discloses "the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact," as recited in claim 1, and it would have been obvious to incorporate these features into *Yoshida*'s structure. Shealy, [206]-[209].

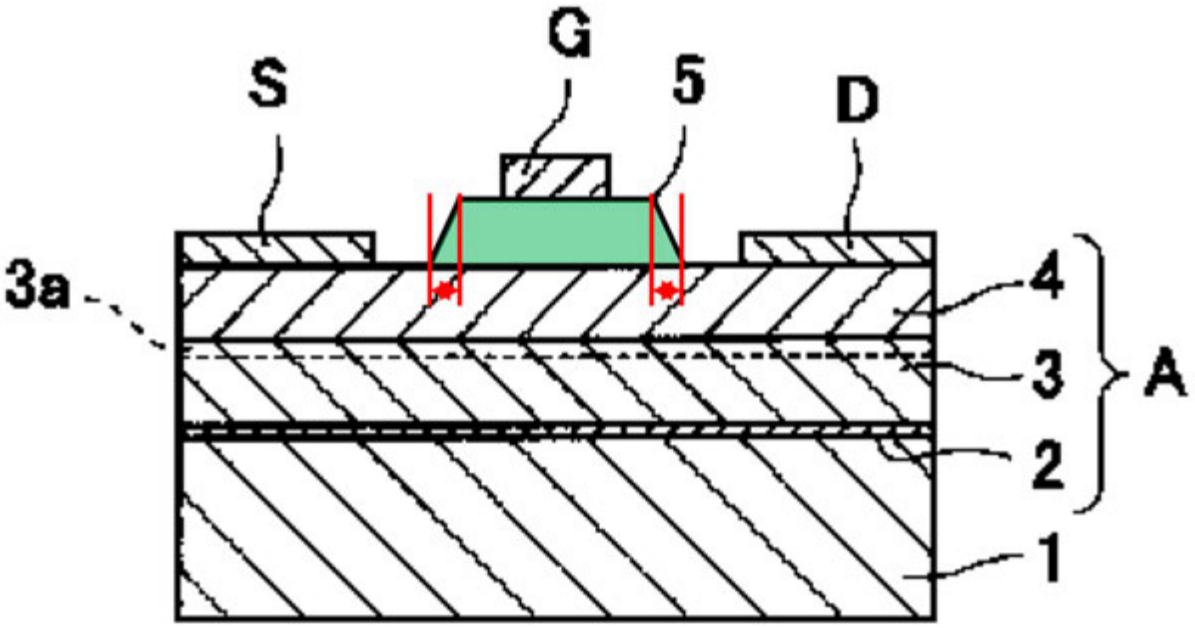
Like *Yoshida*'s layer 5, *Saxler*'s **cap layer** is a p-type gate material that may be doped p-type in a subregion or throughout the layer. *Saxler*, [0013], [0069], [0071], [0073]; Shealy, [207]. The **cap layer** resides above an AlGaN **barrier layer**, just like *Yoshida*'s **layer 5** and as claim 1 of the '335 patent requires. *Saxler*, [0010], [0059]-[0063], Figs. 1A, 2B; Shealy, [207]. The **cap layer** may take several forms, including "p-type dopant," which may be doped in a region of the cap layer or incorporated throughout. *Saxler*, [0069]; Shealy, [207].

Saxler's **cap layer** has side surfaces extending horizontally towards the **source** and **drain contact** under Patent Owner's construction. *Saxler*, [0064], Figs. 1A, 2B; Shealy, [208].



Saxler, Fig. 1A.

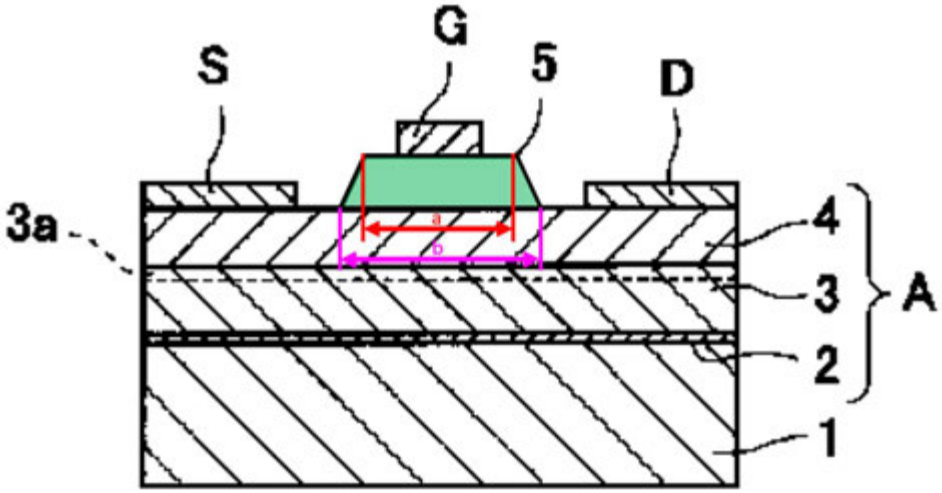
It would have been obvious to combine the sloped sidewalls of *Saxler*'s doped **cap layer** into *Yoshida*'s p-type **layer 5** such that they horizontally extended towards the **source** and **drain contacts** in the *Yoshida-Saxler* device, resulting in a similarly sloped structure. Shealy, [208]; §X.B.2 (Ground 5, Motivation to Combine).



Yoshida, Fig. 1 (modified).

Mapping Under Petitioner's Construction (Ground 5)

The combined *Yoshida-Saxler* device has side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer, which is the proper construction. Shealy, [209]; §VII.A (Claim Construction). In the combined structure, the bottom of the **p-type gate material** (length "**b**," below) is more than 10% wider than the top (length "**a**"). Shealy, [209].

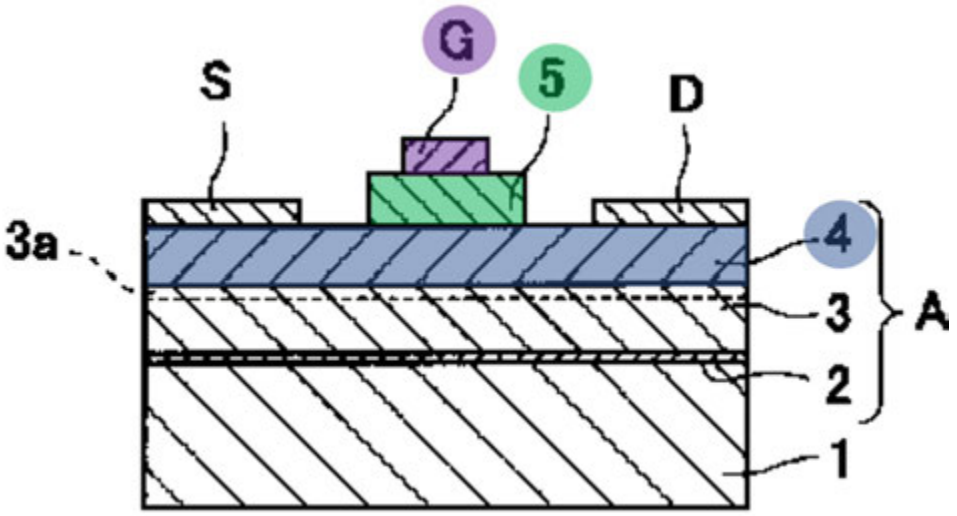


Yoshida, Fig. 1 (modified).

6. [1e]

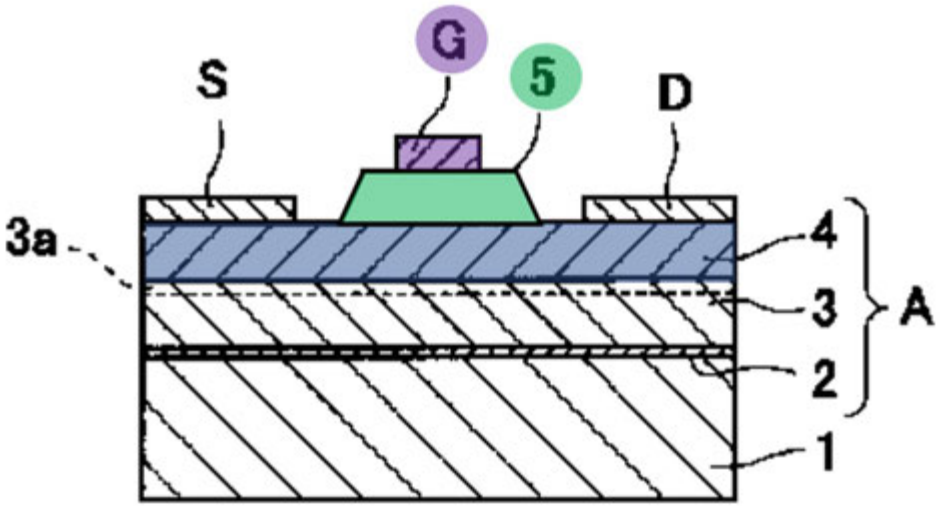
The patent admits the features of [1e] were conventional and depicts numerous prior art devices disclosing [1e]. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A; Shealy, [210].

Yoshida discloses [1e] (Ground 4). Shealy, [210]-[212]. *Yoshida*'s "**gate electrode**" is a metal (e.g., "Au/Pt, Al") formed on p-type **layer 5**. *Yoshida*, Abstract, [0006], [0009]-[0010], [0016], [0022]-[0023], claim 1, Fig. 1; Shealy, [211]. Its sidewalls extend towards **layer 5**, vertically. *Yoshida*, Fig. 1; Shealy, [211].



Yoshida, Fig. 1.

The *Yoshida-Saxler* combination (Ground 5) likewise discloses a gate metal with sidewalls that extend towards the **p-type GaN layer** (Ground 5). Shealy, [212].

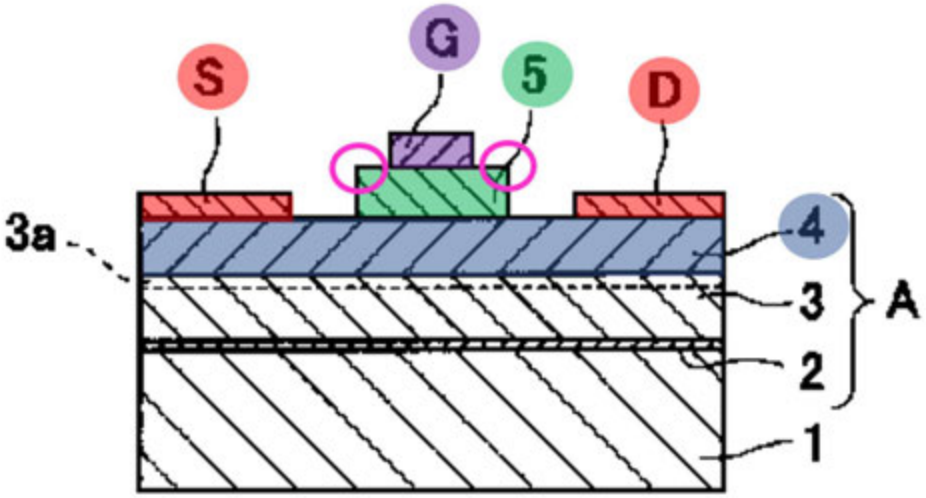


Yoshida, Fig. 1 (modified).

7. [1f]

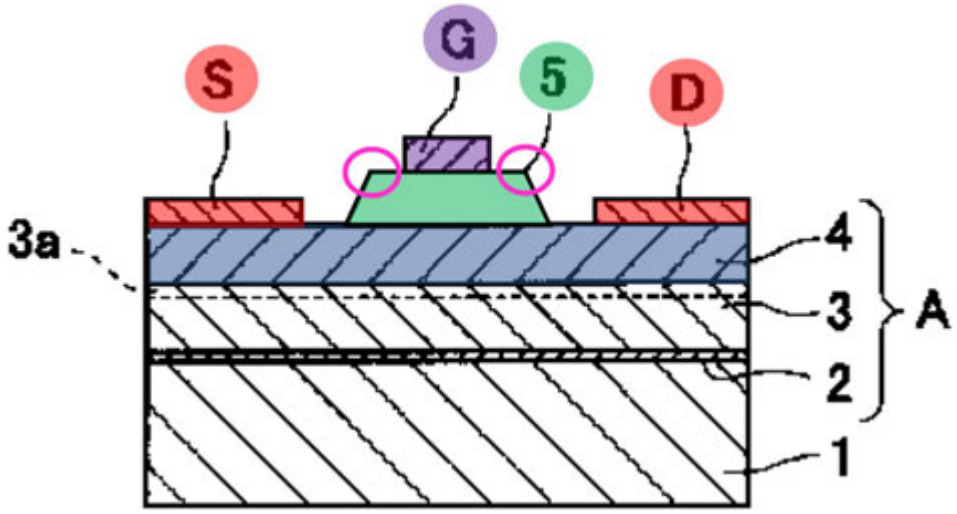
[1f] is the only feature of independent claim 1 that the '335 patent does not admit is found in the prior art. Ex. 1001, 1:28-2:26, Figs. 1-4, 7A; Shealy, [213]. *Yoshida* discloses it. Shealy, [213]-[214].

Yoshida's **gate electrode** is narrower than **layer 5**, thereby exposing **horizontal ledges** that extend past the respective sidewalls of the **gate electrode** and toward the **source** and **drain**. *Yoshida*, [0022]-[0023], Fig. 1; Shealy, [214]. These ledges are symmetric on either side of the gate metal (i.e., having substantially equal widths). *Yoshida*, Fig. 1; Shealy, [214]. *Yoshida* thus discloses this element (Ground 4).



Yoshida, Fig. 1 (modified).

The combination of *Yoshida* and *Saxler* also renders obvious [1f] (Ground 5). Shealy, [215].



Yoshida, Fig. 1 (modified).

D. [Claim 2]

Claim 2 is drawn to a device but is a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §VII.B (Claim Construction); *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373.

Thus, claim 2 does not further limit claim 1 for unpatentability purposes and, for reasons explained for [1f], claim 2 is obvious over *Yoshida* and *Saxler* (Grounds 4-5). Shealy, [216]-[217]; §X.C.7 ([1f]).

E. [Claim 3]

Yoshida discloses that layer 4 comprises AlGaN. *Yoshida*, Abstract, [0010], [0013] ("n-type AlGaN is favorable"), [0021], Fig. 1; Shealy, [218]; §X.C.3 ([1b]).

F. [Claim 4]

Claim 4 recites nothing more than that the gate metal is narrower than the p-type gate material, which is already required by [1f]. And as explained for [1f], *Yoshida* alone and/or in view of *Saxler* discloses a **gate electrode** narrower than **layer 5**. *Yoshida*, [0022]-[0023], Fig. 1; Shealy, [219]; §X.C.7 ([1f]).

G. Independent Claim 5

Yoshida in view of the knowledge of a POSITA (Ground 4) and in view of *Saxler* (Ground 5) renders obvious claim 5. Shealy, [220]-[229].

1. [5p]

[5p] is identical to [1p]. *Yoshida* discloses it for the reasons explained for [1p]. Shealy, [221]; §X.C.1 (([1p]).

2. [5a]

[5a] is identical to [1a]. *Yoshida* discloses it for the reasons explained for [1a]. Shealy, [222]; §X.C.2 ([1a]).

3. [5b]

[5b] is identical to [1b]. *Yoshida* discloses it for the reasons explained for [1b]. Shealy, [223]; §X.C.3 ([1b]).

4. [5c]

[5c] is identical to [1c]. *Yoshida* discloses it for the reasons explained for [1c]. Shealy, [224]; §X.C.4 ([1c]).

5. [5d]

Yoshida discloses [5d]. Shealy, [225]. As explained for [1d], *Yoshida*'s **layer 5** may be a single- or double-layer comprising a "p-type GaN," disposed between source and drain contacts. *Yoshida*, Abstract, [0009], [0015], [0018], claim 2; Shealy, [225]; §X.C.5 ([1d]).

6. [5e]

The recitations of [5e] are included in [1e]. *Yoshida* discloses [5e] for the reasons explained for [1e]. Shealy, [226]; §X.C.6 ([1e]).

7. [5f]

Claim 5 is drawn to a device but [5f] includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §VII.B (Claim Construction); *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373. [5f] otherwise has the same requirements as [1f]. Thus, for reasons explained for [1f], [5f] is obvious over *Yoshida* alone (Ground 4) and in view of *Saxler* (Ground 5). Shealy, [227]-[228]; §X.C.7 ([1f]).

Yoshida's gate electrode is narrower than the underlying p-type GaN layer, resulting in the horizontal ledges of the p-type gate material that extend past sidewalls of the gate metal towards the source contact and drain contact as required by [5f] (Ground 4). *Yoshida*, [0022]-[0023], Fig. 1; Shealy, [228]; §X.C.7 ([1f]). The combination of *Yoshida* and *Saxler* also includes these features (Ground 5). Shealy, [228]; §§X.B.2 (Motivation to Combine), X.C.7 ([1f]).

8. [5g]

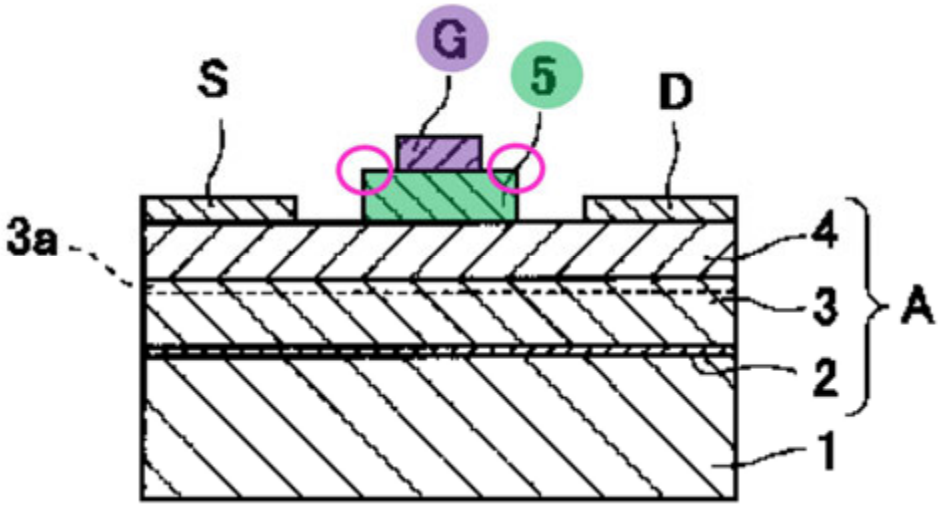
[5g] has the same requirements as [1d]. For the reasons explained for [1d], *Yoshida* in view of the knowledge of a POSITA (Ground 4) and in view of *Saxler* (Ground 5) renders obvious [5g]. Shealy, [229]; §X.C.5 ([1d]).

H. [Claim 6]

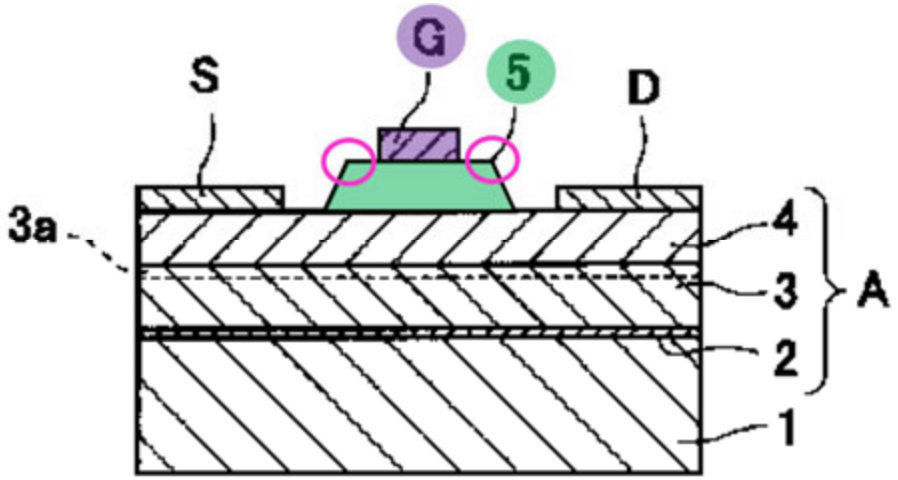
Yoshida discloses claim 6 for the reasons explained for [1b] (Grounds 4-5). Shealy, [230]; §§X.C.3 ([1b], X.E (Claim 3).

I. [Claim 7]

As explained for [1f], *Yoshida* discloses its **p-type gate material** has **symmetric ledges** on either side the **gate metal**, as shown below (Ground 4). *Yoshida*, Fig. 1; Shealy, [231]; §X.C.7 ([1f]). *Yoshida-Saxler* also includes these features, as shown below (Ground 5). Shealy, [231]; §§X.B.2 (Motivation to Combine), X.C.7 ([1f]), X.D (Claim 2).



Yoshida, Fig. 1.



Yoshida, Fig. 1 (modified).

XI. Ground 6: *Yoshida* in View of *Saxler*, *Beach*, and *Shenoy* Renders Obvious Claims 2 and 5-7

A. Overview of Ground 6

To the extent Patent Owner disagrees that the "self-aligned" recitations of claims 2 and 5 are product-by-process elements that have no patentable weight (§§VII.B (Claim Construction), X.D (Claim 2), X.G.7 ([5f])), the combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious claims 2 and 5-7. Shealy, [232]-[259].

1. Motivation to Combine

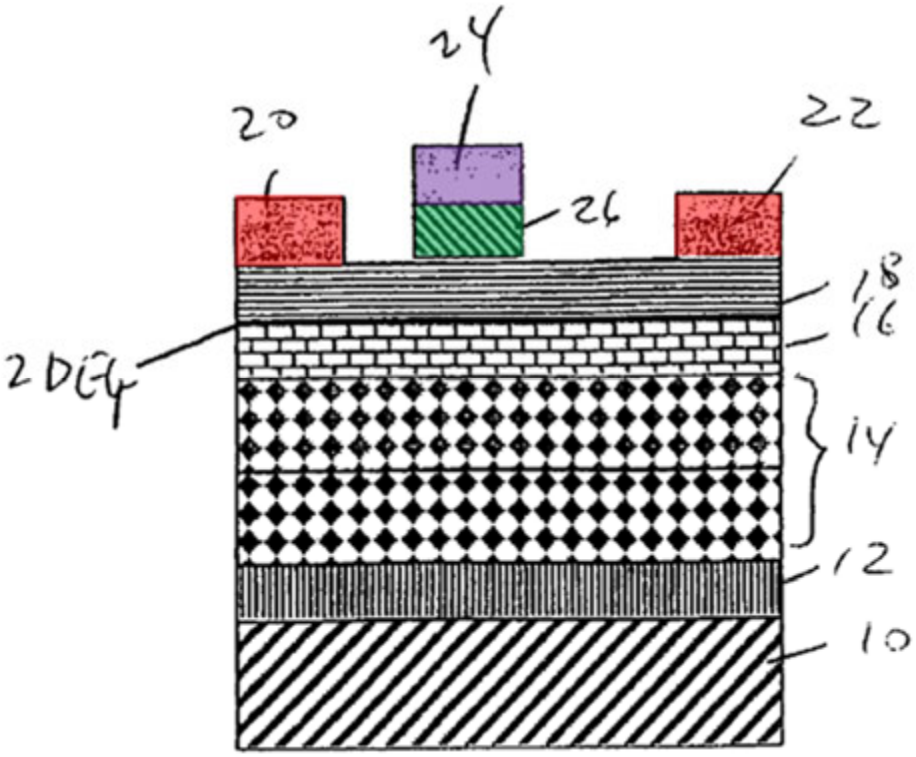
A POSITA would have found it obvious to make the stacked gate structure of the *Yoshida-Saxler* GaN HEMT device using the methods of *Beach* and *Shenoy*. §X.B.2 (Motivation to Combine); Shealy, [233]-[240].

The *Yoshida-Saxler* combination uses a sequence of steps to arrive at a stacked gate structure with a p-type GaN layer and a gate electrode. *Yoshida*, [0021]-[0022]; Shealy, [234]. Specifically, *Yoshida* discloses: (i) depositing a p-type GaN layer 5 onto AlGaN layer 4 (*Yoshida*, [0021]); (ii) dry etching the "p-type GaN layer except where the gate electrode was to be loaded" (*Yoshida*, [0022]); (iii) depositing an SiO_2 film over the entire surface (*id.*); (iv) patterning with a photoresist, and masking where the gate electrode was to be loaded (*id.*); (v) depositing source and drain electrodes (*id.*); (vi) "etching away the masking and opening the SiO_2 film", (*Yoshida*, [0023]); (vii) masking the source and drain electrodes; and (viii) depositing Au to form the gate electrode (*id.*). Shealy, [234]. That process thus requires two masks. Shealy, [234]. In the *Yoshida-Saxler* combination, etching step (ii) would simply employ *Saxler*'s conventional etching techniques to create sloped sidewalls. Shealy, [234]; *Saxler*, [0064]; §X.B.2 (Motivation to Combine).

A POSITA would have been familiar with many ways to create *Yoshida-Saxler*'s stepped gate structure and would have used these methods interchangeably. Shealy, [060]-[062] (citing *Beach*, *Saxler*, *Ahn*, *Xu*, *Sheppard*, *Smith*, *Hu*, *Shenoy*), [235]; §II (Technological Background, discussing common methods to create stepped gate structures). A POSITA would have found it obvious to modify *Yoshida-Saxler* by using *Beach*'s self-aligned technique and *Shenoy*'s isotropic etching to arrive at that same gate structure, which would have improved efficiency by

eliminating masking and etching steps and would have ensured symmetry of the gate metal with respect to the p-gate material. Shealy, [235]. *Ahn* discloses this same approach for making a stepped gate in a thin-film transistor. *Ahn*, Abstract, 3:41-58, 6:15-26, 7:7-14, Fig. 4C; Shealy, [235].

Beach teaches a more efficient method of making stacked gate structures in GaN HEMT devices using fewer steps because it uses a single mask. *Beach*, [0040], [0045], [0054]; Shealy, [236]. *Beach*'s gate structure includes the "gate arrangement 24," which comprises a gate electrode, and an underlying "gate barrier 26," a GaN semiconductor. *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Shealy, [236]. *Beach*'s process (i) deposits "**gate barrier 26**" and "**gate arrangement 24**" layers, (ii) patterns the stack with a mask, (iii) etches to obtain the stack, and (iv) deposits **power electrodes**. *Beach*, [0040]; Shealy, [236]. Such self-aligned techniques were common in the field as of relevant date. Shealy, [236].



Beach, Fig. 1.

A POSITA would have found it obvious to use *Beach*'s approach to create *Yoshida-Saxler*'s gate structure, which would have reduced masking steps, thereby driving down manufacturing time and cost. Shealy, [237]. It would have been obvious to look to *Beach* for its simple methods of making stacked gate structures. *Id.* A POSITA would have further recognized that *Beach*'s self-aligned gate would have symmetrically aligned *Yoshida-Saxler* gate structure layers for improved performance. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3; Shealy, [237].

Beach does not disclose steps to create the **horizontal ledges** of *Yoshida-Saxler*'s stacked gate structure following its self-aligned process. But as previously explained, *Shenoy* discloses simple isotropic etching techniques for symmetrically

undercutting metal layers below photoresist masks. *Shenoy*, 2-3; Shealy, [238]; §IX.A.2 (*Shenoy*).

Saxler and *Sheppard*, incorporated by reference to disclose methods of forming gate structures (*Saxler* [0046] (referencing Ser. No. 10/897,726), [0068] (same))), each describe using several conventional techniques to etch the cap layer and generate the slope sidewalls shown in their figures. *Saxler*, [0064], Figs. 1A-1B; *Sheppard*, [0044], Figs. 1B-1C. Shealy, [239]

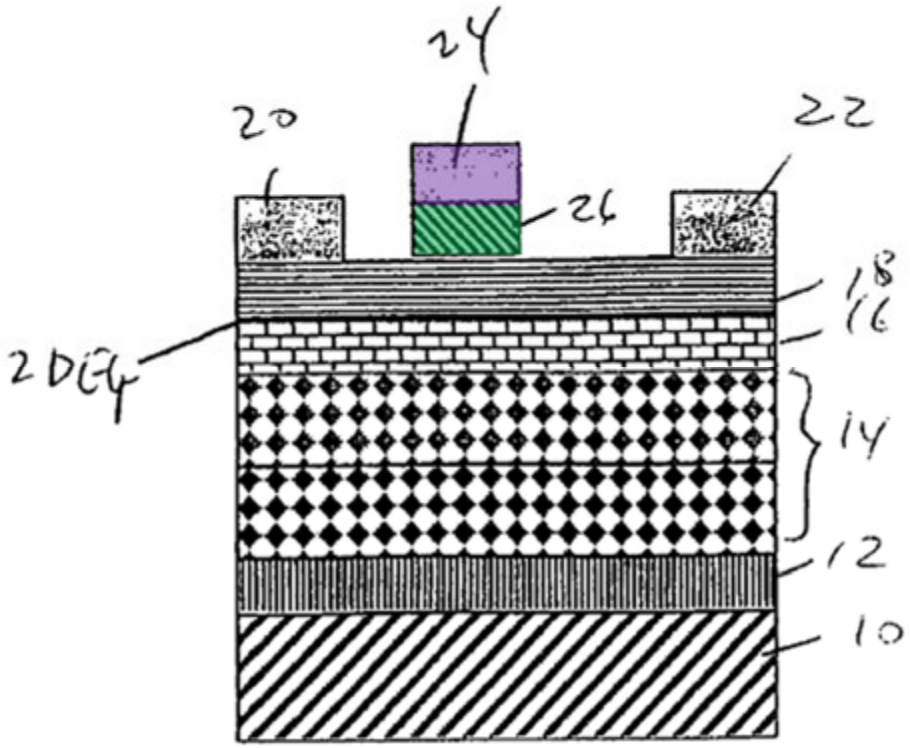
Thus, an ordinary artisan would have found it obvious to use *Beach*'s self-aligned method of making *Yoshida-Saxler*'s stacked gate structure in a GaN HEMT and use *Shenoy*'s methods to undercut the **gate electrode** and create *Yoshida-Saxler*'s **horizontal ledges**. Shealy, [233]-[240]. A POSITA would have found the combination a simple substitution of *Beach*'s and *Shenoy*'s known methods to predictably create *Yoshida-Saxler*'s stacked gate structure more efficiently and symmetrically. *Id.*

B. [Claim 2]

Claim 2 is drawn to a device but is a product-by-process claim for "self-aligned" ledges, which lends no patentable weight. §VII.B (Claim Construction); *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373. The combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* nevertheless

render obvious claim 2, even if "self-aligned" lends patentable weight. Shealy, [241]-[244].

Beach discloses a stacked "***self-aligned*** gate arrangement" using a single photo mask to etch both the "**gate arrangement 24**" (gate electrode) and the underlying "**gate barrier 26**" (GaN semiconductor). *Beach*, [0032]-[0033], [0040], Figs. 1, 2E-2F; Shealy, [242]; §XI.A.1 (Motivation to Combine). *Beach*'s process is the same self-aligned process for forming stacked gate structures depicted in the '335 patent at Figures 6A-6B. Ex. 1001, 4:14-26; Shealy, [242]; §§III.A.1 ('335 Patent Overview), XI.A.1 (Motivation to Combine). The resulting structure has self-aligned sidewalls. *Beach*, [0040], Figs. 1, 2E-2F; Shealy, [242].



Beach, Fig. 1.

Shenoy discloses etching a photomask to isotropically undercut the metal layer below the photomask. *Shenoy*, 2-3; Shealy, [243]. Such undercutting is the same process described in Figures 6B-6C of the '335 patent, which is one way to form the claimed "self-aligned ledges." Ex. 1001, 4:23-39; §§III.A.1 ('335 Patent Overview), XI.A.1 (Motivation to Combine).

It would have been obvious to use *Beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make the gate structure of *Yoshida-Saxler*. Shealy, [244]; §XI.A.1 (Motivation to Combine). That approach would have reduced manufacturing time and costs and reliably improved symmetry. Shealy, [244]; §XI.A.1 (Motivation to Combine).

C. Independent Claim 5

The combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious claim 5. Shealy, [245]-[256].

1. [5p]

As explained in Grounds 4-5, *Yoshida* discloses [5p]. Shealy, [246]; §X.G.1 (Grounds 4-5, [5p]).

2. [5a]

As explained in Grounds 4-5, *Yoshida* discloses a GaN layer. Shealy, [247]; §X.G.2 (Grounds 4-5, [5a]).

3. [5b]

As explained in Grounds 4-5, *Yoshida* discloses [5b]. Shealy, [248]; §X.G.3 (Grounds 4-5, [5b]).

4. [5c]

As explained in Grounds 4-5, *Yoshida* discloses [5c]. Shealy, [249]; §X.G.4 (Grounds 4-5, [5c]).

5. [5d]

As explained in Grounds 4-5, *Yoshida* discloses [5d]. Shealy, [250]; §X.G.5 (Grounds 4-5, [5d]).

6. [5e]

As explained in Grounds 4-5, *Yoshida* discloses [5e]. Shealy, [251]; §X.G.6 (Grounds 4-5, [5e]).

7. [5f]

Claim 5 is drawn to a device but [5f] includes a product-by-process element by requiring "self-aligned" ledges, which lends no patentable weight. §VII.B; *Thorpe*, 777 F.2d at 697; *Kamstrup*, 43 F.4th at 1381-83; *United Therapeutics*, 74 F.4th at 1373. Nevertheless, the combination of *Yoshida*, *Saxler*, *Beach*, and *Shenoy* renders obvious [5f], even if "self-aligned" lends patentable weight. Shealy, [252]-[255].

As explained in Grounds 4-5, *Yoshida* alone and the *Yoshida-Saxler* combination includes the structural features of [5f]. Shealy, [253]; §§X.A (Overview

of Grounds 4-5), X.B.2 (Grounds 4-5, Motivation to Combine), X.G.7 (Grounds 4-5, [5f]). And as further explained above in Ground 6, the *Yoshida-Saxler* combination in view of *Beach* and *Shenoy* discloses that these ledges are self-aligned, as claimed. Shealy, [254]; §§XI.A.1 (Ground 6, Motivation to Combine), XI.B (Ground 6, Claim 2).

It would have been obvious to use *beach*'s self-alignment method and *Shenoy*'s undercutting techniques to predictably make the gate structure of *Yoshida-Saxler*. Shealy, [255]; §XI.A.1 (Motivation to Combine). That approach would have reduced manufacturing time and costs and reliably improved symmetry. Shealy, [255]; §XI.A.1 (Motivation to Combine).

8. [5g]

Yoshida in view of *Saxler* discloses [5g] for reasons explained for Grounds 4-5. Shealy, [256]; §X.G.8 (Grounds 4-5, [5g]).

D. [Claim 6]

Yoshida discloses claim 6 for reasons previously explained for Grounds 4-5, [1b]. Shealy, [257]; §§X.C.3 (Grounds 4-5, [1b]), X.D (Grounds 4-5, Claim 2), X.H (Grounds 4-5, Claim 6).

E. [Claim 7]

As previously explained for Grounds 4-5, *Yoshida* alone and the *Yoshida-Saxler* combination includes the features of [5f]. Shealy, [258]; §§X.G.7 (Grounds 4-5, [1f]), X.I (Grounds 4-5, Claim 7).

As explained for Ground 6, *Beach*'s method of self-aligning the gate structure in combination with *Shenoy*'s methods of symmetrically undercutting the gate metal would have yielded symmetric ledges in the *Yoshida-Saxler* device, as required by claim 7. *Beach*, [0040], Fig. 1; *Shenoy*, 2-3; §§XI.A.1 (Ground 6, Motivation to Combine), XI.B (Ground 6, Claim 2), XI.C.7 (Ground 6, [5f]); Shealy, [258]-[259].

XII. Discretionary Denial Is Not Warranted

A. *Fintiv* Denial Is Improper

In view of the Office's interim guidance dated June 21, 2022 ("Interim Procedures"), *Fintiv* does not apply to this case. The Interim Procedures state "the PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding," so the parallel ITC Investigation does not implicate *Fintiv*. Interim Procedures, 7.

Moreover, the *Fintiv* factors in view of the parallel district court action weigh strongly in favor of institution because the district court case has minimal investment from the Court or Parties, does not have a trial date, and has been stayed. Ex. 1022; *Efficient Power Conversion Corp. v. Innoscience (Zhuhai) Tech. Co.*, No. 2:23-cv-04026, Dkt. 26 (C.D. Cal. July 27, 2023).

B. 35 U.S.C. § 325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017), favor institution. *See also Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-11 (PTAB Feb. 13, 2020) (precedential).

Advanced Bionics, step 1, and *Becton, Dickinson* factors (a), (b), and (d) favor institution because none of the references in this Petition were before the Office during prosecution. *See* Ex. 1002; Ex. 1001. The references are also not cumulative of the prosecution prior art because cited art teaches and renders obvious all challenged claims.

In a forthcoming EPR request, Petitioner intend to challenge the '335 patent's priority claim to *Lidow* and earlier patent applications for inequitable conduct. §III.B.2 (Prosecution History, Priority Claim). Any such EPR does not weigh against institution of this IPR Petition because the proceedings present no overlap in issues or grounds—this IPR assumes priority to April 8, 2009. *Id.*

XIII. Mandatory Notices

A. Real Party-in-Interest

Petitioner and real parties-in-interest are Innoscience (Zhuhai) Technology Company, Ltd., Innoscience America, Inc., and Innoscience (Shuzou) Technology Company, Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '335 patent is involved in:

Name	Number	Court	Filed
Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd.; Innoscience, Inc.; Innoscience America, Inc.	2:23-cv-04026-AB-AS	CDCA	May 24, 2023
In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same	337-TA-1366	ITC	May 26, 2023

The '335 patent is related to U.S. Patent Nos. 8,404,508; 8,890,168; and 9,748,347.

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Petitioner consent to electronic service at the following email address Innoscience-EPC-IPRs@finnegan.com.

XIV. Grounds for Standing

The ’335 patent is available for IPR, and Petitioner are not barred or estopped from requesting IPR.

XV. Conclusion

Petitioner request institution of *inter partes* review and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 19, 2023

/Lionel M. Lavenue/
Lionel Lavenue
Reg. No. 46,859

CLAIM APPENDIX

1. **[1p]** An enhancement-mode GaN transistor, comprising:

   [1a] a GaN layer;

   [1b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

   [1c] a source contact and a drain contact formed on the barrier layer;

   [1d] a p-type gate material formed above the barrier layer, the p-type gate material having side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

   [1e] a gate metal disposed on the p-type gate material, the gate metal having sidewalls extending towards the p-type gate material,

   [1f] wherein the p-type gate material comprises a pair of horizontal ledges that extend past the respective sidewalls of the gate metal and toward the source contact and the drain contact, respectively, the pair of horizontal ledges having substantially equal widths from the sidewalls of the gate metal to the side surfaces of the p-type gate material, respectively.

2. The enhancement-mode GaN transistor according to claim 1, wherein the pair of horizontal ledges of the p-type gate material are self-aligned.

3. The enhancement-mode GaN transistor according to claim 1, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

4. The enhancement-mode GaN transistor according to claim 1, wherein the p-type gate material has a first width between the side surfaces of the p-type gate material and the gate metal has a second width between sidewalls of the gate metal, the second width being less than the first width.

5. **[5p]** An enhancement-mode GaN transistor, comprising:

[5a] a GaN layer;

[5b] a barrier layer disposed on the GaN layer with a 2DEG region formed at an interface between the GaN layer and the barrier layer;

[5c] a source contact and a drain contact disposed on the barrier layer;

[5d] a p-type gate material formed above the barrier layer and between the source and drain contacts;

[5e] and a gate metal disposed on the p-type gate material,

[5f] wherein the p-type gate material comprises: (i) a pair of self-aligned ledges that extend past sidewalls of the gate metal towards the source contact and drain contact, respectively; and

[5g] (ii) side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contact the barrier layer.

6. The enhancement-mode GaN transistor according to claim 5, wherein the barrier layer comprises aluminum gallium nitride (AlGaN).

7. The enhancement-mode GaN transistor according to claim 5, wherein the pair of self-aligned ledges are symmetric with respect to the gate metal.

37 C.F.R. § 42.24(D) CERTIFICATION

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), Petitioner certify that this petition complies with the requirements of 37 C.F.R. § 42.24. Excluding parts of this Petition exempted under § 42.24(a), this Petition contains 13,730 words, as measured by the word-processing system used to prepare this paper.

Dated: September 19, 2023 By: /Lionel Lavenue/
Lionel Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), the undersigned certifies that on September 19, 2023, a copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent 10,312,355, the associated Powers of Attorney, and Exhibits 1001-1023, 1025-1029, were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's Patent Center website for the '335 patent:

Dipu Doshi
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1825 Eye Street, NW
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Dated: September 19, 2023

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