

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01382
U.S. Patent No. 9,748,347

PATENT OWNER'S SUR-REPLY

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I. Introduction

Petitioner abandons its position from Grounds 1 and 3 by acknowledging Saxler fails to disclose the non-recessed embodiment and instead attempts to establish a new position under “obviousness law.” Paper 19, 5 (“Reply”). Because the Petition originally relied on Saxler as disclosing a non-recessed recessed gate (which is self-contradictory), Petitioner now pivots to obviousness based on hindsight motivation from *other grounds* (i.e., Ground 2). Reply, 3-7.

These new theories are foreclosed by statute, precedent, and Board guidelines. *See* 35 U.S.C. §312(a)(3) (requiring petitions identify “with particularity...the grounds on which the challenge to each claim is based”). Accordingly, these new obviousness positions cannot cure the Petition’s invalidity position deficiencies and should be disregarded in their entirety. Consolidated Trial Practice Guide, 84 Fed. Reg. 64,280, 73 (November 2019) (“TPG”).

Regarding Ground 2, a POSITA would have known converting the depletion-mode transistor of Saxler into an enhancement-mode transistor would result in a transistor that would “not be an ideal device” due to the excessive voltage requirements, resulting in “lots of leakage,” and therefore would not have been motivated to make such a modification. Paper 17, 28-34 (“POR”). As explained by Patent Owner, the extension of Saxler’s cap layer between the ohmic contacts relative to the size of the gate contact renders the device inoperable, which

contradicts any motivation and highlights Petitioner's hindsight. *Id.*, 28-34.

For Grounds 4 and 5, Petitioner attempts to reverse engineer FIG. 1 of Yoshida to achieve the goals of the '347 patent. *Id.*, 55-64. Petitioner cannot refute that the ledges of the gate structure in Fig. 1 are not desired or intended by design; they are simply a byproduct of the method disclosed by Yoshida requiring etching the GaN layer wide enough to better ensure that the gate contact that is loaded *after GaN etching* is loaded onto the GaN layer. *Id.*, 57-61. Petitioner's proposed method of etching the gate metal to form ledges after the gate structure is already formed would only introduce unnecessary steps and cost to produce structure that has no function and frustrate Yoshida's purpose (e.g., etching away pGaN *except* where the gate contact is to be loaded to form the pn junction immediately under the gate contact for voltage control). *Id.*, 61. In its Reply, Petitioner again improperly tries to introduce a new theory of obviousness that is unsupported by the Petition or expert testimony, and should not be considered. TPG, 73.

Indeed, the Petition and Reply have overarching flaws in that Petitioner is looking backwards by using the '347 claims and disclosure as a template to reverse engineer what is shown in the prior art figures. POR, 2-4. These figures, as acknowledged by Petitioner, cannot be relied on as being representative of an actual transistor. *Id.*, 34-36, 65. Indeed, Petitioner repeatedly tries to piece together method steps from disparate references with improper hindsight to recreate the

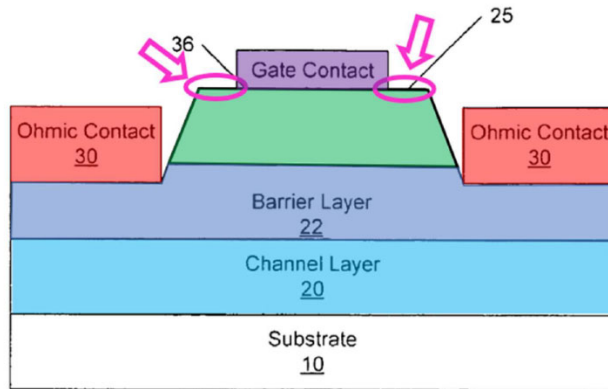
innovative method as claimed. *Id.*, 2-4.

II. Statement of facts

The Board need not accept the purported material facts as admitted; indeed, it is discretionary. 37 CFR §42.23. Patent Owner does not admit the individual elements were known or obvious in combination because Petitioner never made that part of its statement of facts. Moreover, Petitioner's arguments regarding its statement of facts underscores the hindsight nature of its arguments. Petitioner also improperly attempts to bring in other sections of the Petition into the Statement of Facts. Reply 2-3.

III. Petitioner abandons its position that Saxler discloses a non-recessed, recessed embodiment and that Saxler discloses an enhancement-mode transistor (Grounds 1 and 3)

Grounds 1 and 3 are based on a hypothetical non-recessed recessed embodiment. Paper 1, 25-26, 31, 62 ("Pet."). The Petition declared that the non-recessed recessed embodiment was disclosed by Saxler by arguing that "Saxler's gate contact may be recessed or non-recessed (i.e., flat). Where the gate recess is not utilized, Saxler would result in the following structure." *Id.*, 25-26 (internal citation omitted). The Petition specifically relies on the figure below that is not found in Saxler, but refers to it to as "Saxler's non-recessed embodiment." *Id.*, 31, 62.



Saxler, Fig. 1A (modified).

Pet., 25

In his deposition, Dr. Shealy clarifies that “Saxler’s non-recessed embodiment” was based on ¶[0052] of Saxler and his opinion is that he “mix and match” and “take all the embodiments and bring in which ones you want, depending on what you’re trying to accomplish.” EX2004, 39:3-5, 40:1-8, 41:24-42:1. Petitioner concedes that “Dr. Shealy’s testimony accurately reflects obviousness law” in his interpretation of ¶[0052] of Saxler. Reply, 6.

By citing “obviousness law”, Petitioner contradicts its earlier position that Saxler *discloses* Saxler’s non-recessed embodiment instead now relying on *modifying* the disclosure of Saxler. *Id.* Thus, this is not a scenario where a POSITA is selecting a disclosed embodiment, but instead one where a POSITA would be creating a new embodiment based upon the disclosure. And because Petitioner now admits Saxler must be modified, a motivation to modify with an expectation of success is required. *Id.*; *In re O’Farrell*, 853 F.2d 894, 904 (Fed. Cir. 1988).

Furthermore, Petitioner concedes that Saxler does not disclose “a normally off enhancement-mode GaN transistor” by requiring modification to make an enhancement-mode device. *Id.*¹

IV. The Petition failed to provide motivation for modification to arrive at “Saxler’s non-recessed embodiment” (Grounds 1 and 3)

Relying on Saxler’s purported disclosure, the Petition fails to provide any support for Petitioner’s *new* position that a POSITA would *modify* Saxler’s recessed embodiment by removing its recess. Having to pivot to “obviousness law,” Petitioner attempts to cure this deficiency by 1) introducing a new theory of obviousness under *KSR*², and 2) repeatedly citing passages of the Petition (and Dr. Shealy’s testimony) that were *not* relied on in either Grounds 1 or 3.

A petitioner cannot argue in a reply that it would have been obvious to modify the prior art where the petition argued only that the prior art disclosed a particular claim limitation. *Yita LLC v. MacNeil IP LLC*, 69 F.4th 1356, 1365-67 (Fed. Cir. 2023); TPG, 73. An argument that a POSITA would have modified the prior art is a “meaningfully distinct contention” from arguments limited to what the prior art

¹ See also POR, 28-34; EX1003 ¶146 (“with the recess, Saxler’s device is not enhancement-mode (always off)” with reference to the recessed embodiments); Reply, 9 n.2 (relying on a modification of separating the ohmic contacts from the cap layer to turn the non-recessed embodiments (Fig. 1B) into enhancement-mode).

² *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007).

reference teaches. *Yita* at 1367.

In an attempt to find motivation, Petitioner points to its Petition, which states that “a POSITA would thus have understood non-recessed electrodes were a suitable option for Saxler’s cap.” Reply, 3, 7; Pet., 24-28. Obviousness concerns whether a skilled artisan not only *could have made but would have been motivated to make the* combinations or modifications of prior art to arrive at the claimed inventions. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1074 (Fed. Cir. 2015). Petitioner fails to identify a *motivation to make* the proposed combination. This is especially relevant because Saxler already discloses that a non-recessed electrode is “a suitable option” in FIG. 1B, which Petitioner refuses to address. *Compare* POR, 28 *with* Reply, 8 (“irrelevant analysis of Figure *1B*”). Thus, Pet., 24-28 in allegedly identifying a non-recessed electrodes as “a suitable option,” is irrelevant to any motivation for removing the recess from FIG. 1A.

Petitioner also points to its Petition to allege that “it would have been obvious to remove Figure 1A’s recess to make an enhancement mode device.” Reply, 5; Pet., 35-36. However, the Petition provides no such statement. Rather, it states that “a POSITA would have understood that Saxler’s transistors were enhancement-mode GaN transistors at least because of their gate structure.” Pet., 35-36. Thus, Grounds 1 and 3 rely only on Saxler *disclosing* enhancement-mode transistors and do not provide any articulated reasoning for the modification of Saxler now proposed

under §103.

Petitioner alleges that Dr. Shealy's deposition statement that ¶[0052] allows you to "mix and match" and "bring in which [embodiments] you want, depending on what you're trying to accomplish," adheres to *KSR*. Reply, 6. First, *KSR* does not allow a POSITA to simply "mix and match" embodiments to "accomplish" an invalidity analysis. *See Belden*, 805 F.3d at 1074. The new "mix and match" argument fails to provide adequate motivation because it lacks any articulated reasoning for removing a recess from a recessed gate despite Saxler disclosing a suitable non-recessed embodiment. Second, the "mix and match" argument is not disclosed by the Petition. Thus, relying on this new obviousness rationale would be improper. TPG, 73.

Petitioner further argues that ¶[0052] "expressly acknowledges Saxler's recess is optional in every figure" and "*Saxler itself* tells a POSITA to remove Figure 1A's recess." Reply, 5. Paragraph ¶[0052] of Saxler states the possibility of "other embodiments . . . may include or not include a gate recess" without illustrating or further describing those "other embodiments." Dr. Schubert points out that Petitioner's proposed modification based on the generic statement of ¶[0052] would allow practically any modification without requiring any motivation to combine or expectation of success. EX2005 ¶¶99-102. Petitioner's interpretation would thus eviscerate any requirement to identify a motivation to combine for a POSITA and

allow all hindsight depending on what “[he’s] trying to accomplish.” EX2005 ¶¶99-100. Petitioner’s rationale is clearly hindsight. POR, 26-28.

The hindsight continues in “mix[ing] and match[ing]” parameters to supposedly arrive at an enhancement-mode device. Reply, 3-4. Saxler only discloses depletion-mode transistors, and any such modification would require optimizing a number of parameters (including the shape of the cap layer) to change its principle of operation without any direction or expectation of success. POR, 49; *In re O’Farrell*, 853 F.2d at 904.

Petitioner points to the Petition and the Shealy declaration for an alleged motivation. Reply, 3-7³; Pet., 55-56; EX1003 ¶¶[146]-[148]. However, Pet. 55-56 does not address Grounds 1 or 3, and only addresses Ground 2 (Saxler in view of Yoshida) and the cited paragraphs [146]-[148] were similarly only cited in Ground 2 and not Grounds 1 or 3.

Petitioner further argues motivation for the first time in that removing the recess of Saxler’s Figure 1A removes steps to form a recess in its gate. Reply, 7. However, that motivation is not found in the Petition nor supported by expert testimony and should not be considered. TPG, 73. Additionally, Dr. Schubert specifically explained that Petitioner’s reliance on Smith in the Petition is merely

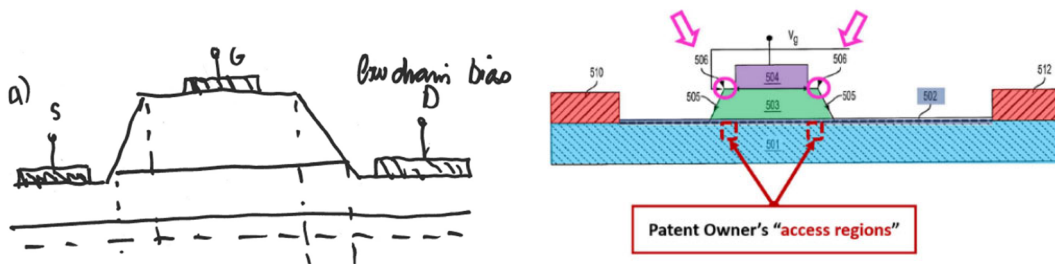
³ Petitioner’s citation to Shealy, ¶[103] appears to be a typo referring to the ’335 counterpart, and should be Shealy, ¶[146].

“circular logic” starting with a recessed embodiment of Saxler and attempting to find disclosure in Smith to arrive at a non-recessed embodiment, while completely ignoring the non-recessed embodiments taught by Saxler (or Smith). EX2005 ¶¶107-112; Pet, 27.

Indeed, Petitioner fails to provide any motivation and expectation of success. And with good reason: it makes no sense to have a non-recessed, recessed embodiment. EX2005 ¶¶104-112. The Petition is riddled with hindsight bias in selecting a recessed gate structure and then removing the recess where the reference itself describes a distinct non-recessed gate structure embodiment. *Id.*

V. Even considering the proposed modification to Saxler, it would still not be a functional enhancement-mode transistor (Grounds 1-3)

As discussed in §III, Petitioner admits that none of the embodiments of Saxler (neither FIG. 1A nor FIG. 1B) are enhancement-mode without modification. POR, 28; Reply, 9 n.2. Furthermore, Patent Owner addresses the proposed modification that extends the entire or substantially the entire length between the ohmic contacts. POR, 29-32, 49-50. Petitioner also provides a new argument that “the patent has the same ‘access regions’ as modified Figure 1A (shown below), and it purports to operate in enhancement mode.” Reply, 9-10.



Reply, 10-11

Petitioner cannot reasonably make the statement that the depletion-mode gate structure of Saxler is the “same” as that in the ’347 patent. Initially, Petitioner is confused on the fundamental term “access regions” which refers to the lengths of the *2DEG between the gate and the source and drain*, respectively, and not *just the region underneath the cap layer*. POR, 29. Petitioner’s proposed transistor has the cap layer 24 extending the entire or substantially the entire width of the access regions, while typical enhancement-mode transistors (including in the ’347 patent) do not. Reply, 9 (reproduced above); POR, 29-32.

Dr. Schubert explains that depletion-mode transistors and enhancement-mode transistors operate differently. POR, 30-32 (citing EX2005). A depletion-mode transistor is normally-on and only needs to “pinch off” the 2DEG at one point to turn the transistor off, such that the width of the gate material underneath the gate electrode, as compared to the width of the gate electrode, does not matter. *Id.* As a result, the gate material can extend the entire or substantially the entire length between the ohmic contacts and still function in depletion-mode. *Id.* Alternatively, enhancement-mode transistors deplete the 2DEG underneath the gate material to be

normally off. *Id.* When a positive voltage is applied to the gate electrode, the 2DEG generally underneath the gate electrode is replenished. *Id.* If the gate material is too much wider than the gate electrode, under normal conditions, the entire 2DEG under the gate material would not be replenished, and the device would not be able to turn on. *Id.*

Dr. Schubert finds that Petitioner's proposed transistor based on FIG. 1A of Saxler would require excessive voltage to be applied to turn the transistor ON based on the relative size of the cap layer. *Id.*, 28-32. **Petitioner's** ITC expert, Dr. Lebby, agreed and opined that a similar gate arrangement would "not be an ideal device" if implemented as an enhancement-mode device, due to the excessive voltage demand resulting in "lots of leakage." *Id.*, 31-32; EX2005 ¶123. Thus, there is no motivation to make the modification resulting in a leakier transistor.

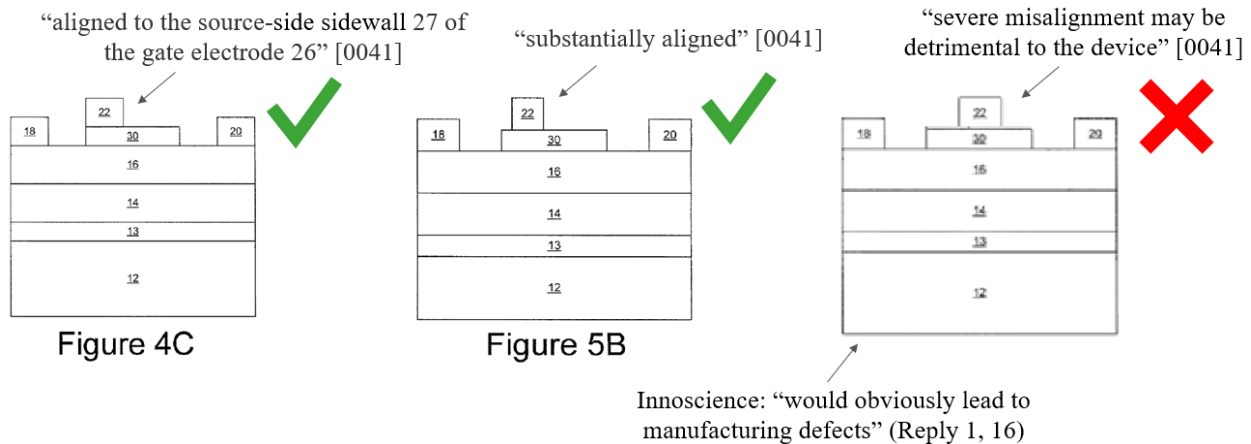
Accordingly, a POSITA would not be motivated to produce an enhancement-mode device in the manner suggested by Petitioner at least because of the required excessive voltage requirements to operate in enhancement-mode. POR, 30-32; *In re Ratti* 270 F.2d 810, 813 (C.C.P.A. 1959). That is, a POSITA would not be motivated to remove the gate recess of the depletion-mode transistor in FIG. 1A of Saxler in view of itself or Yoshida to arrive at an enhancement-mode device, because the resulting transistor "would not be an ideal device" and have "lots of leakage." POR, 31-32; EX2005 ¶123.

VI. Petitioner’s new motivation for the “precise position” of Saxler actually teaches away from its proposed modification in view of Beach, Shenoy, and Ahn (Grounds 1-3)

In citing ¶¶[0041]-[0044] of Smith, Petitioner newly states that “imprecise gate positioning would obviously lead to manufacturing defects, so a POSITA would have been motivated to improve gate alignment and positioning.” Reply, 1, 16. This is pure attorney argument not supported by the Petition, and actually contradicts Petitioner’s own proposed modifications.

Petitioner’s reliance on reverse engineering the “schematic” of FIG. 1 is misdirected, and Patent Owner established that Saxler does not disclose a centrally aligned electrode. POR, 34-35, 65; EX2005 ¶235; EX1007 ¶[0042] (“[T]he regions illustrated in *the figures are schematic* in nature and *their shapes are not intended to illustrate the precise shape of a region of a device.*” (emphasis added)). Indeed, Petitioner and Dr. Shealy repeatedly discredit the accuracy of Saxler’s drawings. POR, 35-36, 65; EX2005 ¶133; Pet., 90-91 (citing EX1003 ¶230); EX2004, 53:13, 16-25, 56:24-57:1, 60:17-18, 82:16-19.

Furthermore, ¶[0041] of Smith (as repeatedly relied on by Petitioner as being incorporated in Saxler) explicitly discloses that “severe misalignment [from the source-side sidewall of the GaN cap] may be detrimental to the device.” POR, 35; EX2005 ¶236.



Saxler’s “precise positioning” (illustrating EX1015)

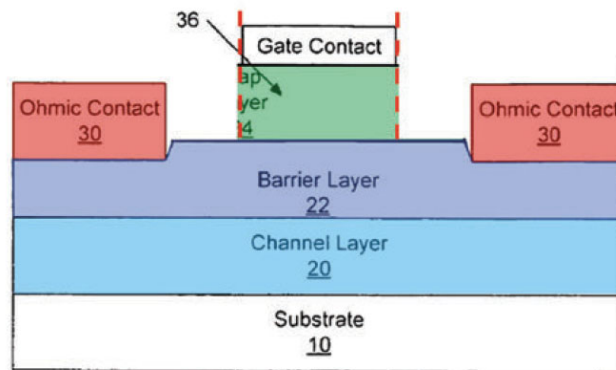
Thus, Saxler’s “precise positioning” relates to the edge surface and not the central location and teaches away from Petitioner’s own proposed modification of centrally aligning the gate electrode (severe misalignment from the source-side sidewall of the GaN cap) in view of Beach, Shenoy, and Ahn because it “may be detrimental to the device” (EX1015 ¶[0041]) and “would obviously lead to manufacturing defects” (Reply, 1, 16). MPEP 2141.02-IV; *W.L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552 (Fed. Cir. 1983) (“prior art must be considered in its entirety, including disclosures that teach away from the claims”).

VII. Petitioner proposes a new combination of Saxler and Beach unsupported by the Petition (Grounds 1, 2, and 4)

The Petition states “[a] POSITA would have found it obvious *to make the stacked gate structure of Saxler’s non-recessed embodiments using Beach’s and Shenoy’s methods.*” Pet., 31 (emphasis added). And, “[i]t would have been obvious *to create Saxler’s gate structure with Beach’s approach for improved alignment*

between layers. It would have been obvious to look to *Beach for its simple methods of making stacked gate structures*.” Pet., 34 (emphasis added, internal citations omitted).

In response, Dr. Schubert shows that all the “self-aligned” approaches cited by Petitioner (Smith, Beach, Beach-II) are for self-aligning *sidewalls*, and would result in cutting off, or not forming, the horizontally extending “sloped” side surfaces that Petitioner relies on from Fig. 1A of Saxler. POR, 38-39; EX2005 ¶¶148-153.



POR, 38

Recognizing its argument’s weakness, Petitioner now proposes a new “combination us[ing] Saxler’s etching technique to create sloped sidewalls when using Beach’s one-mask approach.” Reply, 13-14. This is inconsistent with and is unsupported by the Petition, and thus should not be considered. TPG, 73. The combination of the Petition is “to make the stacked gate structure of Saxler’s non-recessed embodiments using Beach’s and Shenoy’s methods” and fails to reference “Saxler’s etching technique” and how it would be modified based on Beach/Shenoy.

Pet., 31-32. Thus, this new combination from the Reply should not be considered for unpatentability. *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1329-1331 (Fed. Cir. 2019) (rejecting a new theory of unpatentability where petitioner argued a new combination of features from the same references for the first time in its reply).

Moreover, even if the combination were to be considered, the Reply fails to provide a step-by-step analysis of how the three disparate etching steps would be combined, why a POSITA would have combined them, and whether a POSITA would have had a reasonable expectation of success. Instead, Petitioner again retreats to vague reasoning such as “no more than simple substitution” and “known methods that would be predictably implemented” without providing the specific process sequences for the proposed combination. POR, 46-48. This is insufficient as a matter of law. *KSR*, 550 U.S. at 418 (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”)

VIII. Petitioner relies on irrelevant and conclusory statements to address Shenoy (Ground 1, 2, and 4)

As discussed above, Petitioner attempts to reverse engineer schematics of Saxler and Yoshida. Based on that strawman, Petitioner newly argues that Dr. Shealy’s mention of “liquid metal etches” (EX2004, 99:14-17) – that Petitioner

refers to as “many wet etches”– “would ‘work fine.’” Reply, 18. But reliance on these “wet etches” would be inappropriate because they are not cited in any Ground nor sufficiently tied to Shenoy. POR, 42. As such, this new argument should not be considered. TPG, 73.

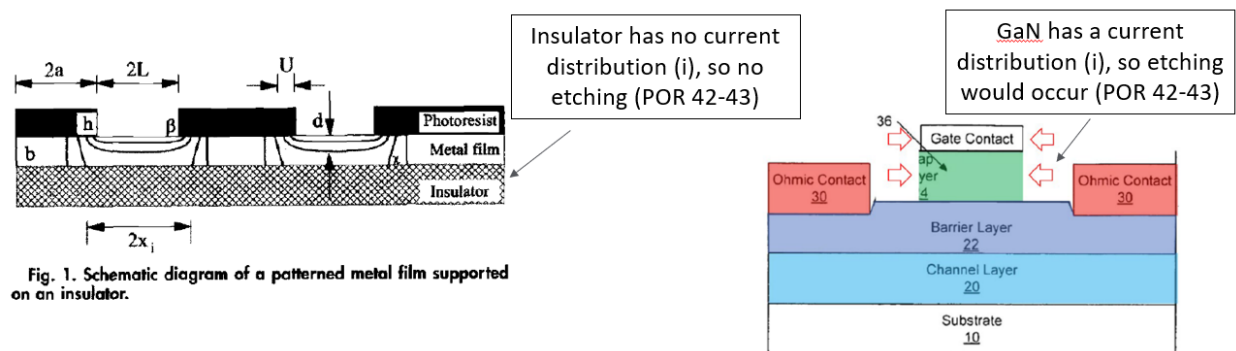
Even if considered, Dr. Shealy distinguishes these other etching techniques from Shenoy. EX2004, 97:19-21 (“[T]hese solutions [are] *unlike the technique used in Shenoy*. . . .” (emphasis added)). As such, the new argument fails.

Moreover, the new argument suffers from similar deficiencies as the arguments throughout the Petition. It relies on hindsight in Dr. Shealy’s statement that the wet etches “work fine” (Reply, 18), which is purely conclusory and cannot satisfy the reasonable expectation of success requirement.

Indeed, Dr. Shealy’s opinion that the approach would “etch the gate metal, not the p-type GaN layer” provides no supporting evidence. Reply, 18-19. Petitioner is specifically referring to a depleted “holes” theory of Dr. Shealy that directly contradicts the proposed modification. POR, 43-46, 62; EX2004, 98:25-99:13.

In contrast, Dr. Schubert actually addresses the principles of the mathematical model of Shenoy, and its reliance on an underlying insulator that is not present in the proposed modification. POR, 40-46. Dr. Schubert explains the equation of Shenoy’s mathematical model based on “Faraday’s law” and “Laplace's equation”

applies to both metals and semiconductors, in etching both the gate contact and the underlying GaN, because neither is an insulator. *Id.*



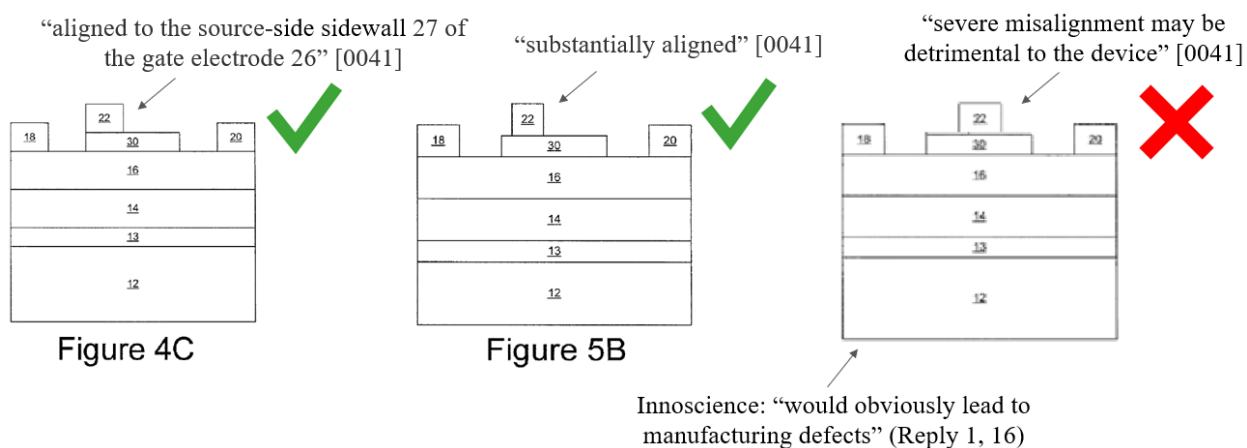
Petitioner argues for the first time that “Saxler repeatedly describes passivation techniques.” Reply, 18. First, Petitioner fails to make this argument in its Petition, and it should not be considered. TPG, 73. Second, even if considered, Petitioner fails to provide any explanation as to how or why a POSITA would incorporate the alleged “passivation techniques” into the relevant layer, when in the process it would have occurred, and whether there would have been a reasonable expectation of success, especially given how the alleged “passivation techniques” of Shenoy would affect the plurality of disparate etching steps of Saxler, Yoshida, and Beach.

Petitioner also newly argues that p-GaN material etches more slowly than the gate metal according to Shenoy (Reply, 18-19), which should not be considered. TPG, 73. This characterization of Dr. Shealy’s testimony is wrong, because the modification based on Shenoy was to *preserve* the ledges (Dr. Shealy: “they don’t

touch the gallium nitride” with reference to the many wet etches), which Patent Owner establishes is not how Shenoy would work. Pet., 93-94; EX2004, 99:14-19; POR, 42-43. Petitioner fails to provide how the relative etching rate is relevant to its application of Shenoy.

IX. Petitioner still does not provide any reason to modify Saxler with the method that produces the structure of Ahn (Ground 3)

Ground 3 again is based on the faulty premise of reverse engineering the hypothetical “non-recessed Saxler embodiment.” POR, 51-52; Reply, 21-23. As discussed in § VI, Saxler does not disclose and actually teaches away from a centrally aligned electrode. POR, 34-36, 52.



Saxler’s “precise positioning” (illustrating EX1015)

Petitioner cannot provide any reason to disregard the explicit disclosure of Saxler in its modification based on an unrelated method of Ahn that produces a substantially different gate structure. POR, 52-54. Indeed, Petitioner relies on the rationale that Ahn “*would work* with Saxler” (Reply, 22 (emphasis added)), which

is legally insufficient because it fails to provide an articulated reasoning for *why* a POSITA would combine disparate teachings. *Belden*, 805 F.3d at 1074.

Thus, for the reasons discussed in POR (17-21, 34-36, and 52-54) and §XIV, a POSITA would not modify Saxler with the method of Ahn that forms an undesirable (centrally-aligned that “may be detrimental to the device”, §VI) and non-analogous gate structure (designed specifically for challenges of a thin-film transistor in preventing deterioration of thin overlying gate oxide layer, §XIV, POR, 52-54).

X. Yoshida does not disclose that its method is “flexible” (Grounds 4 and 5)

Petitioner alleges “Yoshida specifies no order of gate and ohmic contact formation, and it teaches finishing the gate *before* the ohmic contacts.” Reply, 23 (emphasis in original, internal citations omitted). Here, Petitioner relies on a self-serving conclusory statement in Dr. Shealy’s deposition, which is directly contradicted by Yoshida and Dr. Shealy himself. As Dr. Shealy states, Yoshida “specifically” discloses that the ohmic contacts are deposited and masked, then Au is deposited to form the gate electrode. POR, 55-56; EX1003 ¶204 (Dr. Shealy laying out steps (v)-(viii) of Yoshida). Additionally, Yoshida itself describes a specifically ordered process and does not explicitly tell a POSA to modify the order. POR, 13-15.

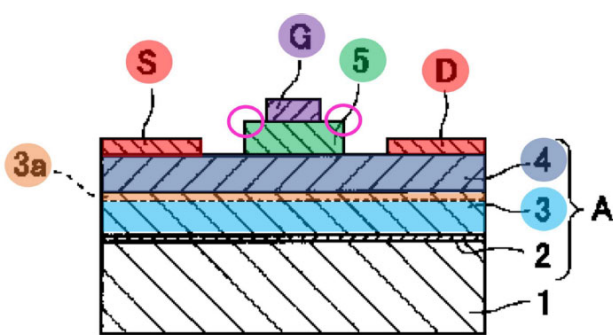
In falsely premising Yoshida’s method as flexible and citing *KSR*, Petitioner

attempts to take complete freedom to “mix and match” components from divergent references to try to piece together the claimed steps through hindsight. *Id.*, 2-3; *Belden*, 805 F.3d at 1074.

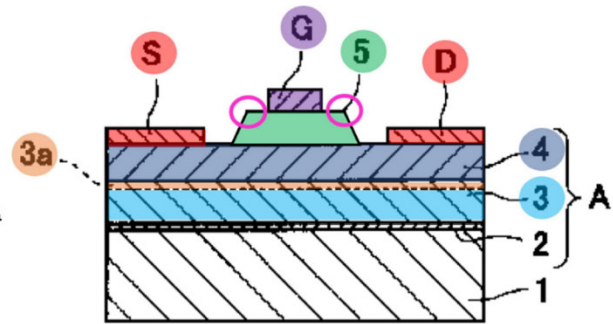
XI. Petitioner introduces a new obviousness rationale to modify Yoshida with Saxler’s sloped sidewalls (Ground 4)

Petitioner newly relies on an “alternative” obviousness rationale in “using Saxler’s etch within the p-GaN’s existing footprint creates sloped sides and maintains the same (or less) width at the bottom of the p-GaN.” Reply, 26 (internal citations omitted).

The Petition fails to make the argument that a POSITA could maintain the p-GaN's existing footprint. Rather, the Petition clearly relies on **adding** the sloped walls of Saxler to **widen** the p-type GaN material 5 of Yoshida. Pet., 73, 85-86.



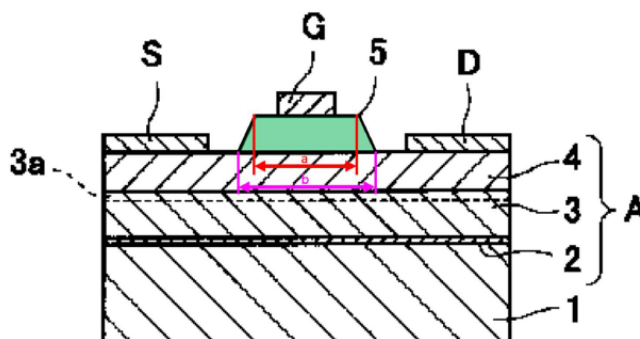
Yoshida, Fig. 1.



Yoshida, Fig. 1 (modified).

This is especially evident in Petitioner's reliance on dimensions of the widened p-type GaN material 5 in the modified transistor. Pet., 89-90. Petitioner specifically touts that the modification would increase the footprint of the p-type

GaN material 5 by “more than 10%.” *Id.*



Yoshida, Fig. 1 (modified).

For this reason alone, Petitioner’s “alternative” theory should be rejected.

Even if the Board were to consider Petitioner’s new obviousness rationale, the argument suffers from the same deficiencies as the obviousness rationale of the Petition. Patent Owner establishes that the transistor of Yoshida is assembled with the p-type GaN layer 5 “etch[ed] away . . . except for where the gate electrode was to be loaded” in order to position the pn junction of a p-type GaN layer 5 “immediately under” the gate electrode G for “voltage control with a small amount of carrier injection, and the controlled voltage further enables control of current flowing between channels.” POR, 13-15.

Thus, it is immaterial whether Petitioner proposes adding the sloped walls to the p-GaN 5 of Yoshida (as in the Petition) or reducing the size of the gate electrode G while maintaining the same footprint of the p-GaN 5 (as in the Reply), because both modifications would widen the p-GaN 5 *relative to* the gate electrode G such that the pn junction would not be “immediately under” the gate electrode G,

reducing the desired “voltage control” of Yoshida. EX2005 ¶¶277-279; POR, 61.

As discussed in §V, the structure and function of the depletion-mode cap layer of Saxler is substantially divergent from the enhancement-mode p-type GaN layer 5 of Yoshida. EX2005 ¶¶ 280-281.

Therefore, a POSITA would not modify Yoshida with the sloped sidewalls of Saxler.

XII. Petitioner tries to introduce new obviousness rationale for forming the “ledges” in Yoshida-Saxler (Ground 4)

Petitioner did not make the arguments in its Petition that it now makes despite its citation to the Petition. Reply, 25; Pet., 73-75. Petitioner never made the argument that “the Yoshida-Saxler combination, which includes *Yoshida’s ledges* (also found in Saxler) and Saxler’s sloped sidewalls *would increase leakage paths and result in lower leakage.*” *Id.* The Petition only provides arguments that *Saxler’s* sloped sidewalls are for increasing leakage paths and resulting in lower leakage. Pet., 73-75. This is especially evident by Petitioner’s reliance on FIGS. 1-4 and 7A of the ’347 patent that do not show ledges. *Id.* Neither the Petition nor Dr. Shealy provides any motivation for forming the ledges. Thus, this new argument that Yoshida’s ledges “would increase leakage paths and result in lower leakage” should be disregarded for being pure attorney argument and not supported by the Petition—with no motivation to combine and obvious hindsight. TPC, 73.

It is readily apparent that Petitioner begins its analysis with Yoshida, because

of what is shown in FIG. 1 and attempts to reverse engineer that structure while applying the teachings of the '347 patent. However, Dr. Shealy agrees that FIG. 1 does not represent the actual transistor of Yoshida in citing the “principle” of ¶[0042] of Saxler that transistor schematics do not represent transistors as manufactured. POR, 34-35, 65; Pet., 90-91 (citing EX1003 ¶230). This divergent structure of Yoshida is especially true as Petitioner attempts to completely reinvent Yoshida’s “gate-last” method to be “gate-first” based on Beach, Saxler, and Ahn. POR, 57-61.

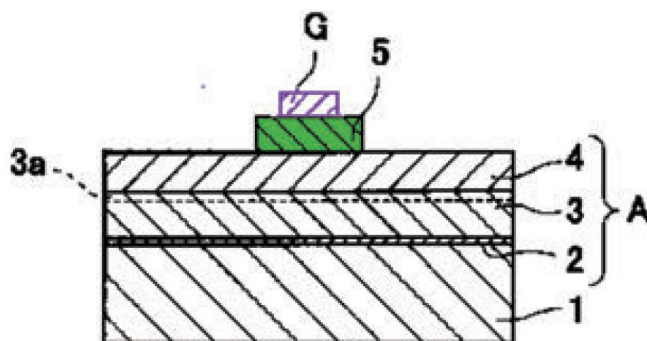
XIII. A POSITA would not etch “ledges” in Yoshida or Yoshida-Saxler after the gate metal is loaded and etched (Ground 4 and 5)

Initially, Petitioner agrees that the schematic of FIG. 1 does not represent a transistor as manufactured, in applying the “principle” of ¶[0042] in Saxler. POR, 34-35, 65; Pet., 90-91 (citing EX1003 ¶230).

Furthermore, Petitioner does not refute that the ledges of FIG. 1 are a byproduct of Yoshida’s approach of etching the p-type GaN layer 5 before loading the gate contact G, that Petitioner proposes modifying away from. POR, 57-61; Reply, 24-26. Petitioner does not refute that the p-type GaN layer 5 would be etched slightly wider in this “gate-last” approach (before the gate electrode is loaded) in order to receive the gate electrode without overhang. POR, 57-61. This is supported by the references that Petitioner relies on showing ledges. *Id.*, 58-59.

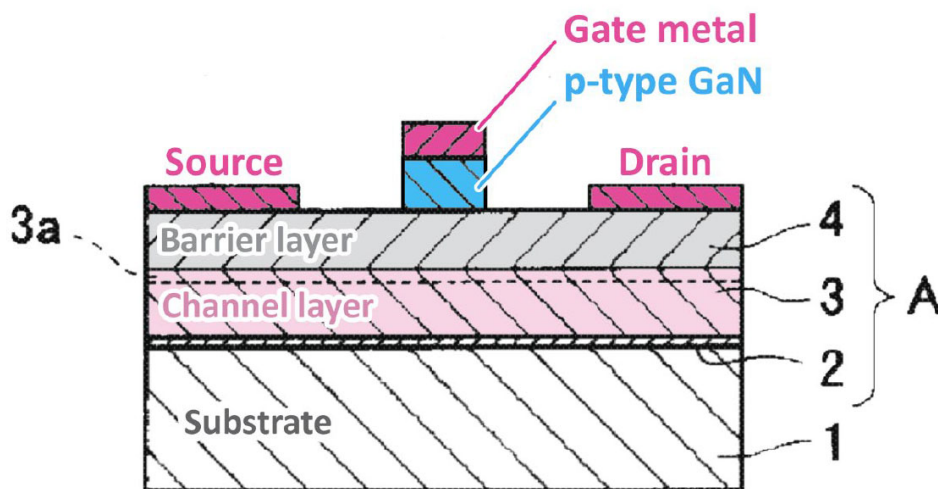
Indeed, Yoshida specifically discloses that its transistor is formed by a process where the p-type GaN layer 5 is layered and “etch[ed] away... except where the gate

electrode was to be loaded” such that the pn junction of the p-type GaN layer 5 is “immediately under” the gate electrode G when loaded for “voltage control with a small amount of carrier injection.” POR, 58-60; EX1006 ¶¶[0017], [0022].



EX1007, Fig. 1 (annotated)

Thus, Petitioner still does not provide a valid reason to add an unnecessary second etching step to form ledges in Yoshida after the gate metal is already loaded on the p-type GaN and initially etched to form the gate. POR, 57-61.



Yoshida after first etching step of Beach/Ahn

The ledges 1) would have no function because the gate metal would already

be loaded and etched simultaneously to form the gate (POR, 59-61), 2) would only frustrate Yoshida's purposes by being detrimental to voltage control by reducing the width of the gate metal relative to the pn junction (*Id.*, 61, 67, 69), and 3) would undesirably add manufacturing cost and steps as explicitly discouraged by Petitioner (*Id.*, 61, 64 (citing motivations from the Petition including "eliminating masking and etching steps," "reduc[ing] steps and costs" and predictably creating the "stacked gate structure more efficiently"))).

Thus, a POSITA would not perform an additional etching step to form the "ledges" in Yoshida or Yoshida-Saxler after the gate metal is loaded on the p-type GaN and initially etched to form the gate. *Id.*, 59-61.

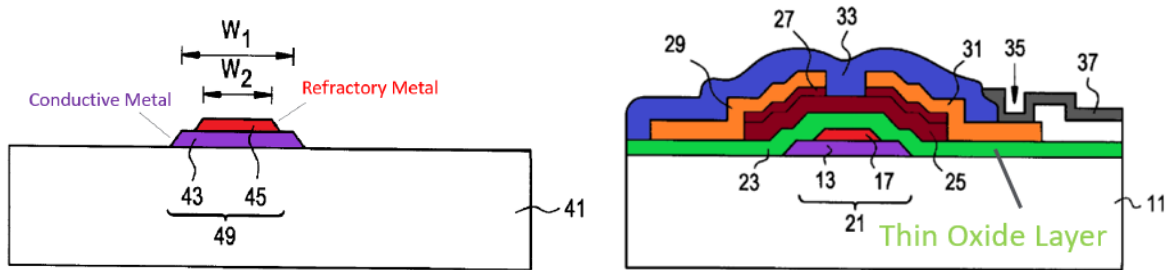
XIV. Petitioner still does not provide any motivation to modify Yoshida with the resultant structure of Ahn (Ground 5)

Petitioner now cites a conclusory motivation of "form[ing] the same gate structure as Yoshida more efficiently and with sloped side walls on the gate layers." Reply, 26-27.

However, as further discussed in §§XII-XIII, Patent Owner establishes that Fig. 1 does not represent the transistor as manufactured by Yoshida, and a POSITA would not perform a second etching step after the gate is already formed according to Petitioner's proposed combination.

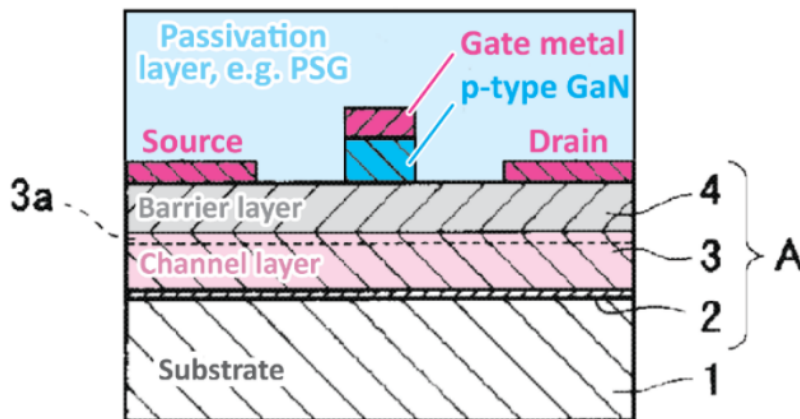
As discussed in POR (at 17-21, 34-36, 52-54, and 64-69), Patent Owner establishes that the method of Ahn is directed to performing two etching steps to

manufacture a specific double-step gate structure. The double-step gate structure is intended to reduce deterioration of a thin gate oxide layer 23, because deterioration in the thin gate oxide layer 23 would result in a short circuit with the vertically aligned semiconductor contact layer 25 and source and drain electrodes 29, 31 in the thin film transistor of Ahn. *Id.*, 18-21.



EX1010, Fig. 4C & Fig. 1F (Annotated)

Indeed, similar to Saxler, the deterioration of any overlying layer is not relevant to Yoshida, because Yoshida has a passivation layer that is much thicker, of a different material, and not vertically separating the gate from the semiconductor contact layer and source and drain electrodes. POR, 68-69. Thus, the double-step gate structure of Ahn and method of forming that structure to reduce the deterioration of the thin oxide layer of Ahn would not be relevant to the transistor of Yoshida. *Id.*



Yoshida after first etching step of Beach/Ahn with Passivation Layer

Petitioner does not address these structural and functional divergences of Ahn. Petitioner's arguments on the same field of endeavor and whether it "would work" does not provide sufficient "articulated reasoning" for obviousness. Reply, 27; *Belden* 805 F.3d at 1074.

Indeed, Petitioner still fails to address the complete lack of motivation for performing additional etching steps to create unnecessary ledges. MPEP 2141(IV); *W.L. Gore & Assoc., Inc.*, 721 F.2d at 1550. ("A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention.")

XV. Petitioner changes its motivation to avoid contradiction, and still fails to reconcile the contradiction (Ground 5)

Patent Owner rightfully pointed out that Petitioner is taking contradictory positions in the '347 patent and related U.S. Pat. 10,312,335 proceedings. POR, 65-66. For the '347 patent, Petitioner is modifying the method of Yoshida with a

motivation “to improve alignment and symmetry between layer,” while at the same time, Petitioner is taking a position that the layers are already aligned in citing FIG. 1 for the ’335 patent. *Id.*

In the Reply, Petitioner proposes a new motivation of “to prevent misalignment.” Reply, 1-2. This new motivation is not supported by the Petition nor any expert testimony, and is still inconsistent with Petitioner’s position with respect to the ’335 patent. Thus, the new theory of obviousness should be rejected. TPG, 73. Petitioner fails to provide any suggestion of a possibility of misalignment, and for the ’335 patent, Petitioner relies on a blanket statement that the gate of Yoshida is aligned. POR 66 (citing EX2007, 83). Thus, Petitioner still fails to reconcile the contradiction or demonstrate a motivation for a POSITA to make the combination.

This contradiction perfectly illustrates the hindsight that Petitioner relies on throughout the Petition in “trying to accomplish” the specific claimed invention. EX2004, 41:24-42:1; POR, 2-4.

XVI. Conclusion

For the foregoing reasons, Petitioner's challenge is deficient, and no claim should be held unpatentable.

Dated: October 22, 2024

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S SUR-
REPLY complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1).
According to the word count tool in Microsoft Word, the brief contains 5,568
words, excluding the parts of the document that are exempted by 37 C.F.R. §
42.24(a).

Dated: October 22, 2024

Respectfully submitted,

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Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S SUR REPLY** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

Petitioner-EPC-IPRs@finnegan.com

Dated: October 22, 2024

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