

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

Case IPR2023-01382
U.S. Patent 9,748,347 B2

PETITIONER'S NOTICE OF APPEAL

Pursuant to 35 U.S.C. §§ 141(c), 142, and 319 and 37 C.F.R. § 90.2(a), Petitioner Innoscience (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc. (“Innoscience”) hereby provides notice of appeal to the United States Court of Appeals for the Federal Circuit from the Final Written Decision of the Patent Trial and Appeal Board (“Board”) entered on March 25, 2025 (Paper No. 31) (“Final Written Decision”) and from all underlying orders, decisions, rulings, and opinions relating to the *inter partes* review of U.S. Patent No. 9,748,347 (“’347 patent”) in Case No. IPR2023-01382. This Notice is timely under 37 C.F.R. § 90.3(a)(1) and 37 C.F.R. § 90.3(b)(1), having been filed no later than sixty-three (63) days after issuance of the Order Denying Director Review of Final Written Decision (Paper 34).

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Petitioner states that the issues on appeal include, but are not limited to:

- the Board’s determination in finding claims 1-3 are not unpatentable;
- the Board’s factual findings, conclusions of law, or other determinations supporting or relating to the foregoing issues; and
- all other issues decided adversely to Petitioner in any orders, decisions, rulings, or opinions underlying or supporting the Final Written Decision.

A copy of the Final Written Decision is attached to this Notice.

Pursuant to 35 U.S.C. § 142 and 37 C.F.R. § 90.2(a)(1), this Notice is being filed with the Director of the United States Patent and Trademark Office, and a copy of this Notice is being concurrently filed with the Patent Trial and Appeal Board. In addition, a copy of this Notice and the required docketing fees are being filed with the Clerk's Office for the United States Court of Appeals for the Federal Circuit via CM/ECF in accordance with 37 C.F.R. § 90.2(a)(2), Federal Rule of Appellate Procedure 15, and Federal Circuit Rule 15.

Date: August 8, 2025

Respectfully submitted,

By: /Lionel M. Lavenue/
Lionel M. Lavenue, Reg. No. 46,859
Lead Counsel

CERTIFICATE OF SERVICE AND FILING

I hereby certify that on August 8, 2025, in addition to being filed and served electronically through the Patent Trial and Appeal Board's P-TACTS System, this **PETITIONER'S NOTICE OF APPEAL** was filed with and served on the Director of the United States Patent and Trademark Office via e-mail at the following:

Office of the General Counsel
U.S. Patent and Trademark Office
efileSO@uspto.gov

I also hereby certify that on August 8, 2025, this **PETITIONER'S NOTICE OF APPEAL** and the requisite docketing fees were filed with the Clerk's Office of the United States Court of Appeals for the Federal Circuit via CM/ECF.

I further hereby certify that on August 8, 2025, this **PETITIONER'S NOTICE OF APPEAL** was served by electronic mail on the following counsel for Patent Owner:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
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INNOSCIENCE AMERICA, INC.
Petitioner,

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EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01382
Patent 9,748,347 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY MCGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background*

Innoscence (Zhuhai) Technology Company, Ltd. and Innoscence America, Inc., (collectively “Petitioner”) filed a petition for an *inter partes* review (Paper 1 (“Pet.”)) challenging claims 1–3 of U.S. Patent No. 9,748,347 B2 (Ex. 1001 (“the ’347 Patent”)). Efficient Power Conversion Corporation (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). After receiving authorization from the Board, Petitioner filed a Reply to the Preliminary Response (Paper 8) and Patent Owner filed a Sur-reply (Paper 10). On March 26, 2024, we instituted an *inter partes* review of all of the challenged claims based on all of the grounds identified in the Petition. Paper 11 (“Inst. Dec.” or “Institution Decision”). Patent Owner filed a Response to the Petition (Paper 17, “Resp.”), Petitioner filed a Reply (Paper 19 (“Reply”)), and Patent Owner filed a Sur-reply (Paper 21, “Sur-reply”). We held an oral hearing for this proceeding on January 7, 2025, and a transcript of the hearing has been entered into the record. Paper 30 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). Based on the record before us, we conclude that Petitioner has not shown by a preponderance of the evidence that claims 1–3 of the ’347 patent are unpatentable.

B. *Related Matters*

The parties identify two matters involving the ’347 patent: *Efficient Power Conversion Corporation v. Innoscence (Zhuhai) Technology Co., Ltd*, 2:23-cv-04026-AB-AS (C.D. Cal. May 24, 2023) and *Certain Semiconductor Devices, and Methods of Manufacturing Same and Products*

Containing the Same, Inv. No. 337-TA-1366 (ITC May 26, 2023). Pet. 108; Paper 5 (Patent Owner’s Mandatory Notices), 2.

C. The ’347 Patent (Ex. 1001)

The ’347 patent, titled “Gate with Self-aligned Ledge for Enhancement Mode GaN Transistors,” filed July 30, 2014 and issued August 29, 2017, is directed to “[a]n enhancement-mode GaN transistor with reduced gate leakage current between a gate contact and a [two-dimensional electron gas (2DEG)] region and a method for manufacturing the same.” Ex. 1001, codes (45), (54), (57). The ’347 patent claims priority to a number of applications, including U.S. Patent Application 12/756,960, which published as Publication No. 2010/0258843 A1 (Ex. 1011, “Lidow”).

The ’347 patent states that GaN semiconductor devices are desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages. Ex. 1001, 1:25–27. These devices are based on structures that exhibit “high electron mobility,” and are referred to as, *inter alia*, high electron mobility transistors (HEMT). Ex. 1001, 1:29–33. GaN HEMT devices includes a nitride semiconductor with at least two nitride layers. Ex. 1001, 1:37–38. Different materials (e.g., AlGaN and GaN) on the semiconductor or on a buffer layer cause the layers to have different band gaps and also causes polarization, which contributes to a conductive “two dimensional electron gas” (2DEG) region near the junction of the two layers, and allows charge to flow through the device. Ex. 1001, 1:40–44. The ’347 patent further explains that the nitride layers that cause polarization typically include a barrier layer of AlGaN adjacent to a layer of GaN to include the 2DEG, which allows charge to flow through the device. Ex. 1001, 1:45–48.

The '347 patent explains that because the 2DEG region exists under the gate at zero gate bias, most nitride devices are “normally on,” or “depletion mode” devices. Ex. 1001, 1:49–51. However, if the 2DEG region is depleted (i.e., removed) below the gate at zero applied gate bias, the device can be an “enhancement mode” device. Ex. 1001, 1:51–53. In contrast to depletion mode devices, enhancement mode devices are normally off and require a positive bias applied at the gate in order to conduct current. See Ex. 1001, 1:46–58.

Figure 2 of the '347 patent, reproduced below, depicts a prior art enhancement-mode GaN transistor.

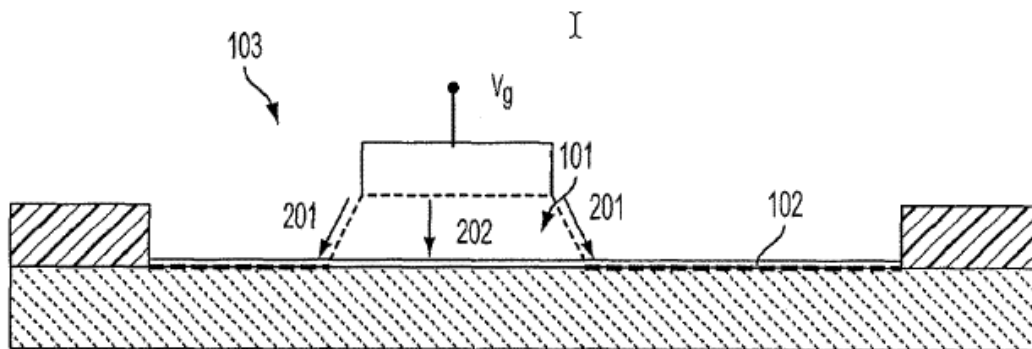


FIG. 2
PRIOR ART

Figure 2 depicts a conventional enhancement-mode GaN transistor having gate 103 comprising p-type material 101, and a 2DEG region 102 under gate 103, with two gate leakage current paths 201 and 202. Ex. 1001, 1:64–2:3, 2:63–65.

The '347 patent depicts an embodiment of the claimed invention in Figure 5, reproduced below.

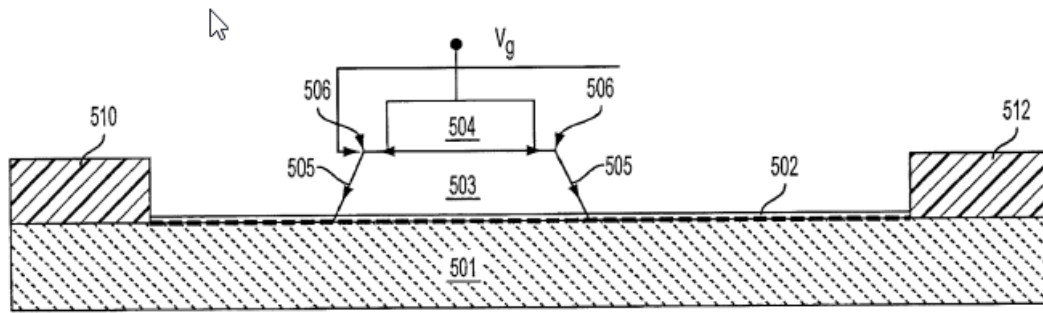


FIG. 5

Figure 5 shows a schematic diagram of a transistor device including GaN base layer 501, barrier layer 502, source metal 510 (i.e., source contact), drain metal 512 (i.e., drain contact), p-type gate material 503, gate metal 504, and horizontal ledges 506 on each side of gate metal 504. Ex. 1001, 3:5–7, 3:32–49.

The '347 patent states that the pair of horizontal ledges results in reduced gate leakage between the gate and the 2DEG region of an enhancement mode transistor as compared to an enhancement mode transistor lacking the self-aligned ledges. Ex. 1001, 1:20–24, 4:6–7, Fig. 8. The '347 patent states that a gate having self-aligned ledges has significantly lower gate leakage current than conventional gates without the ledges when the transistor device is in the ON state. Ex. 1001, 4:41–45. The '347 patent states that when a positive voltage is applied to the gate metal, the gate current path 505 travels horizontally along the upper edge of the p-type gate material 506 and then follows the diagonal path along the edge of the p-type gate material 503. Ex. 1001, 3:65–4:5.

Figure 5 also includes arrows showing gate current path 505 that travels horizontally along the ledges 506 and then follows the diagonal path along the edge of p-type gate material 503. Ex. 1001, 4:1–5. According to

the '357 patent, this structure results in reduced gate leakage current compared to conventional gates without ledges. Ex. 1001, 4:6–7.

The '347 patent further states that pair of ledges 506, which extend past sidewalls of gate metal 504, “have equal or substantially equal widths, i.e., the respective ledges are symmetric from the respective sidewalls of the gate metal to the side surfaces of the p-type gate material, which is due to the self-aligned manufacturing process.” Ex. 1001, 3:54–59. The '357 patent also describes an exemplary manufacturing process for forming a gate with self-aligned ledges, and depicts the steps in Figures 6A–6C, reproduced below. Ex. 1001, 4:8–33, Figs. 6A–6C.

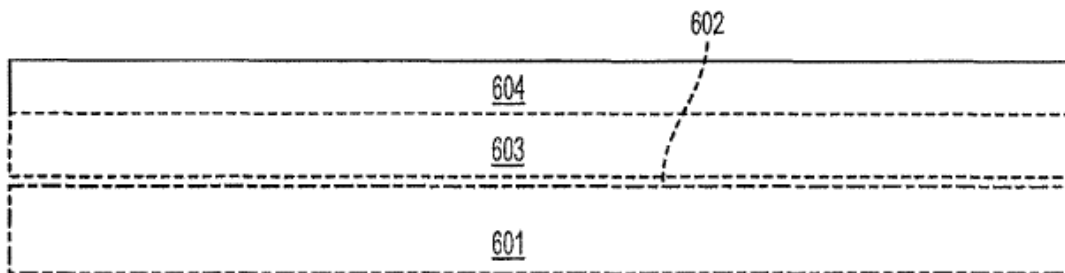


FIG. 6A

Figure 6A shows forming AlGaN barrier layer 602 on GaN base layer 601, forming a layer of p-type gate material 603 on barrier layer 602, and depositing gate metal 604 on p-type gate material 603. Ex. 1001, 4:10–16.

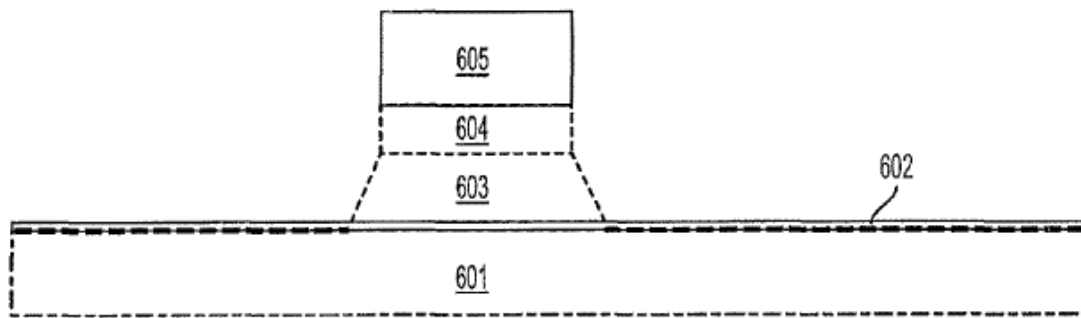


FIG. 6B

Figure 6B shows photoresist layer 605 deposited on gate metal 604, and the resulting structure after gate metal 604 and p-type gate material are etched. Ex. 1001, 4:17–20.

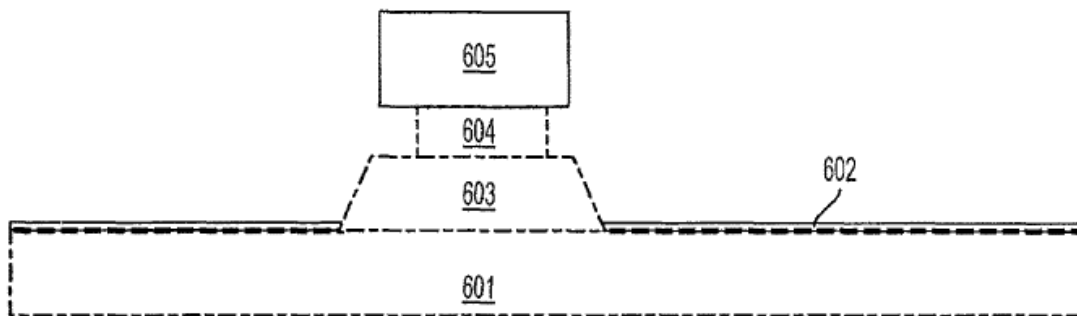


FIG. 6C

Figure 6C shows the resulting structure after gate metal 604 is etched isotropically such that gate metal 604 has a width less than the planar upper surface of p-type gate material 603. Ex. 1001, 4:20–23. According to the '347 patent, “[t]his second etching step results in the formation of the ledges 506 of the p-type gate material 603.” Ex. 1001, 4:23–25.

The '347 patent states that the self-aligned process illustrated in figures 6A–6C is “vastly superior to forming gate ledges using separate masks” due to the possibility of misalignment between the gate metal and p-type gate material when using a two-mask process. Ex. 1001, 4:46–57.

D. Illustrative Claim

Petitioner challenges claims 1–3 of the '347 patent. Independent claim 1 is reproduced below.

Claim 1:

[1p] A method for manufacturing an enhancement-mode GaN transistor, the method comprising:

[1a] forming a GaN layer;

[1b] forming a barrier layer on the GaN layer;

[1c] depositing source and drain contacts on the barrier layer;

[1d] depositing a p-type gate material on the barrier layer;

[1e] depositing a gate metal on the p-type gate material;

[1f] forming a photoresist over the gate metal;

[1g] etching the gate metal and the p-type gate material,

[1h] wherein the step of etching the p-type gate material comprises forming side surfaces of the p-type gate material that extend horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer; and

[1i] etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal.

Ex. 1001, 4:66–5:14 (labels and formatting added to correspond with Petitioner's designation of claim limitations (Pet. Claim Appendix)).

E. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–3 are unpatentable based on the following challenges:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3	103(a) ¹	Saxler, ² Beach, ³ Shenoy ⁴
1–3	103(a)	Saxler, Yoshida, ⁵ Beach, Shenoy
1–3	103(a)	Saxler, Ahn ⁶
1–3	103(a)	Yoshida, Saxler, Beach, Shenoy
1–3	103(a)	Yoshida, Ahn

Pet. 17. Petitioner relies on the declaration of James Richard Shealy, Ph.D. (Ex. 1003). Patent Owner relies on the declaration of E. Fred Schubert, Ph.D. (Ex. 2005).

II. ANALYSIS

A. Principles of Law

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity ... the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. The ’347 patent claims priority to applications filed before this date. April 10, 2010. *See* Ex. 1001, code (60). Thus, we apply the pre-AIA versions of §§ 102 and 103.

² US 2006/0108606 A1, published May 25, 2006 (Ex. 1007, “Saxler”).

³ US 2007/0007547 A1, published Jan. 11, 2007 (Ex. 1008, “Beach”).

⁴ R.V. Shenoy, et. al, *Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Micromachining*, J. ELECTROCHEM. SOC., Vol. 143, No. 2, 544, Feb. 1996 (Ex. 1009, “Shenoy”).

⁵ JP H11-261053, published Sept. 24, 1999 (Ex. 1005 (original language); Ex. 1006 (certified English translation), “Yoshida”).

⁶ US 5,905,247, issued May 18, 1999 (Ex. 1010, “Ahn”).

shifts to the Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The petition must identify with particularity the evidence that supports the grounds for the challenge to each claim. 35 U.S.C. § 312(a)(3).

A claim is unpatentable as obvious under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence,⁷ objective indicia of non-obviousness (i.e., secondary considerations). *Graham*, 383 U.S. at 17–18. “To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). We analyze Petitioner’s challenges according to the above-stated principles.

B. Claim Construction

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). In this context, claim terms “are

⁷ Patent Owner does not rely on any object indicia of non-obviousness in its arguments.

generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (citations omitted) (en banc). The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

In our Institution Decision, we noted that Petitioner stated that no claim construction was required to resolve any issues in dispute, but identified three terms whose construction was disputed in a related proceeding. Inst. Dec. 10–16. The three terms are: (1) “forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer” (“forming the side surfaces” limitation), (2) “etching the gate metal and the p-type gate material”, and (3) “etching the gate metal to form a pair of ledges,” and proposes constructions for each of these terms. Pet. 19–24 (citing, *inter alia*, Ex. 1028 (Petitioner and Complainant’s Proposed Claim Construction, ITC 337–TA-1366)).

We further noted that, although Patent Owner also agreed that no claim construction was required to resolve any issues in dispute, Patent Owner presented arguments disputing Petitioner’s proposed construction for “forming the side surfaces.” Inst. Dec. 10 (citing *See* Pet. 23; Prelim. Resp. 10).

In our Institution Decision, we declined to adopt Petitioner’s proposed construction of the “forming the side surfaces” limitation, which Petitioner asserted required “forming side surfaces of the p-type gate material *such that the bottom of the p-type gate material is more than 10% wider than the top of the material, leading to sloped side surfaces* that contact the barrier layer.” Inst. Dec. 15. We also stated that no further construction of this term, or any other term, was required for the purpose of institution. Inst. Dec. 16–17.

On a full record, we determine that no claim construction is required to render this Decision⁸. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”)).

C. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have had “at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field, and at least two years of experience in semiconductor device design and/or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies.” Pet. 19 (citing Ex. 1003 ¶¶ 52–53). Petitioner also contends that “[a]dditional education could substitute for professional experience and vice versa.”

⁸ Our Decision regarding whether or not the asserted art discloses or suggests the side surfaces limitations of step [1h] does not turn on which claim construction is adopted.

Pet. 19. Before institution, Patent Owner did not challenge Petitioner's definition or offer its own. *See* Prelim. Resp.

Following institution, Patent Owner proposes a slightly different definition, and states that a POSITA "would have possessed at least a four-year degree in electrical engineering, physics, material science, or a closely related field, and three years of professional work experience in the epitaxial growth, design, and fabrication of semiconductor electronic devices, including those of GaN." Resp. 11 (citing Ex. 2005 ¶ 20). Patent Owner further states that relevant graduate education could substitute for the professional work experience. Resp. 11.

Both parties agree that the differences between the definitions do not impact the analysis. Resp. 11; Reply 2.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner's proposal regarding the level of ordinary skill in the art. Based on our review of the '347 patent and the prior art of record, we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the '347 patent and the prior art. We also note that our Decision would be the same under either parties' definition.

D. Statement of Disputed Facts

Pursuant to 37 C.F.R. § 42.22(c), a petition "may include a statement of material facts." "Each material fact preferably shall be set forth as a separately numbered sentence with specific citations to the portions of the record that support that fact." *Id.* Petitioner provides a statement of facts relating the state of "enchantment [sic] mode GaN transistors at the time of the '347 patent's earliest claimed priority date." Pet. 18. Petitioner does not,

however, provide specific citations to the portions of the record that support these material facts. *Id.*

Patent Owner contends Petitioner’s statement of material facts “is materially deficient and should be ignored” because “Petitioner failed to include any citations to the record supporting any of its alleged facts.” Resp. 10. Petitioner’s failure to provide citations supporting its statements of material fact is highly problematic. It essentially shifts the burden of proving the facts are incorrect to Patent Owner, without Petitioner having to provide citations to support its assertions. We need not determine whether such an omission requires ignoring the statements of material fact in this case, however, because the recited material facts are either clearly supported by the evidence of record or not necessary to render a Decision in this case.

E. Overview of Asserted Prior Art

1. Saxler (Ex. 1007)

Saxler is a U.S. patent publication, titled “Cap Layers and/or Passivation Layers for Nitride-Based Transistors, Transistor Structures and Methods of Fabricating Same” discloses Group III-nitride high electron mobility transistors and methods for forming those transistors. Ex. 1007, code (54), ¶¶ 1, 7. In particular, Saxler is directed to HEMTs that include “a non-uniform aluminum concentration AlGaN based cap layer having a high aluminum concentration adjacent a surface of the cap layer that is remote from the barrier layer on which the cap layer is provided.” Ex. 1007, code (57). Saxler explains that having such a cap layer “may improve robustness of the device during processing and/or device operation” over conventional devices. Ex. 1007 ¶ 47.

Saxler discloses several embodiments of its claimed invention, including the transistors depicted in Figures 1A and 1B, reproduced below.

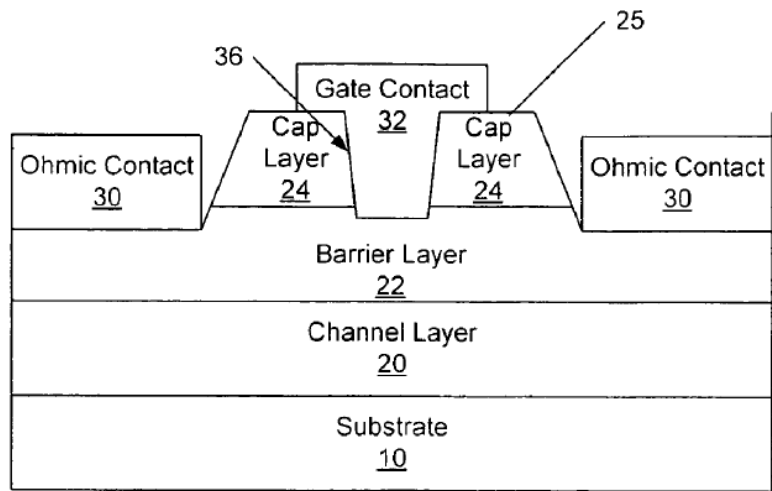


Figure 1A

Figure 1A of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and recessed gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66.

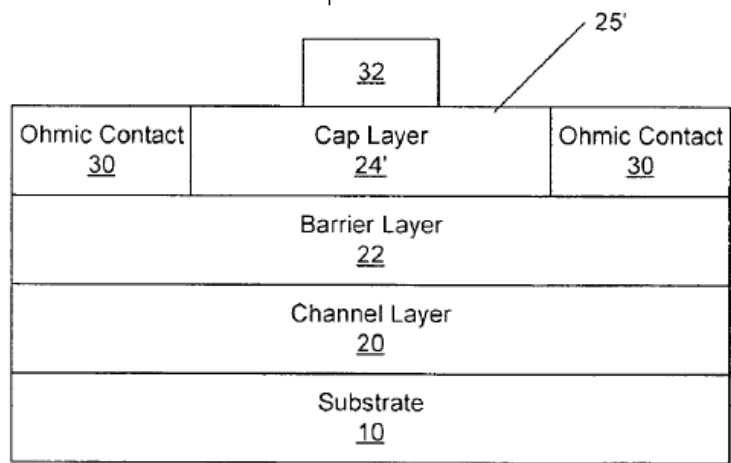


Figure 1B

Figure 1B of Saxler shows a cross-sectional schematic drawing illustrating a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and gate contact 32. Ex. 1007 ¶¶ 31, 57, 61, 66. In this embodiment, cap layer 24 does not have a recess, such that gate 32 is on cap layer 24. Ex. 1007 ¶¶ 61, 66.

Saxler describes the features of its various embodiments, including those with a gate recess and those without a gate recess. *See e.g.*, Ex. 1007 ¶¶ 12–13 (discussing the doped region of the GaN based cap layer in embodiments with and without a gate recess), 27 (discussing embodiments have a gate contact recessed into or on an AlN cap layer), 52 (stating other embodiments may include or not include a gate recess), 64, 73, 66 (describing suitable gate materials), 70 (describing suitable n-type dopants), 71 (describing suitable p-type dopants). Saxler also discloses methods for making transistors according to the embodiments described in the specification. Ex. 1007 ¶¶ 6, 68.

2. *Yoshida (Ex. 1006)*

Yoshida is a Japanese Patent Publication titled “High Mobility Transistor” that discloses novel GaN-based HEMT structures that can operate under the application of high voltages and at higher speeds. Ex. 1006 ¶¶ 1, 8. Yoshida depicts the basic structure of its claimed invention in Figure 1, reproduced below.

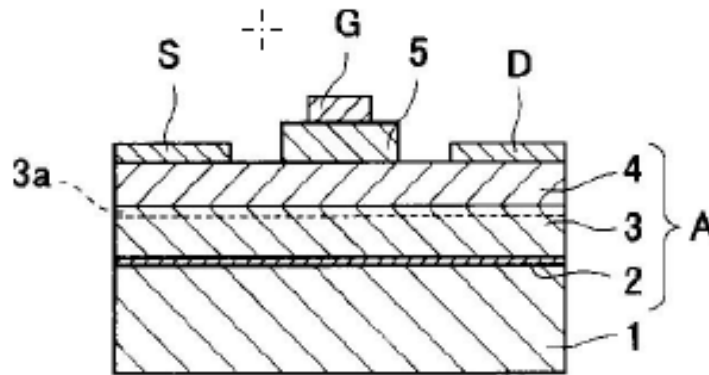


Figure 1 of Yoshida shows a cross-sectional view of a transistor having a stacked structure comprising buffer layer 2, i-type semiconductor layer 3, and n-type semiconductor layer 4 formed on semi-insulating substrate 1. Ex. 1006 ¶ 10. Figure 1 also shows gate electrode G on p-type semiconductor layer 5, as well as source electrode S and drain electrode D, all formed on n-type semiconductor layer 4. Ex. 1006 ¶ 10.

Yoshida discloses methods for fabricating the structure shown in Figure 1, including deposition and etching conditions. Ex. 1006 ¶¶ 19–23.

3. *Beach* (Ex. 1008)

Beach is a U.S. patent publication titled “III-Nitride Enhancement Mode Devices” that discloses a “normally OFF III-nitride power semiconductor device and a method for the fabrication thereof.” Ex. 1008 code (12), ¶ 9. Beach depicts an embodiment of its invention in Figure 1, reproduced below.

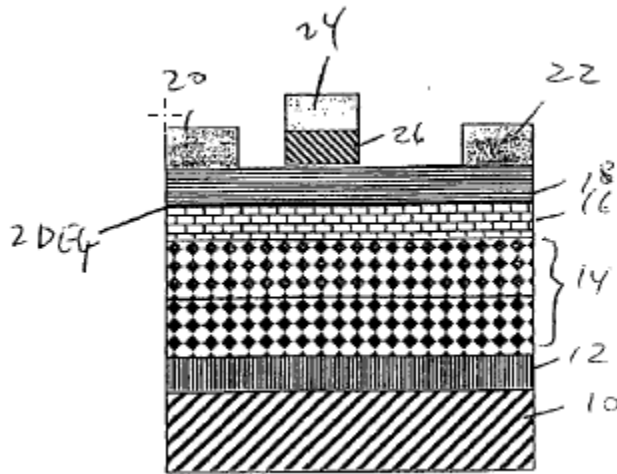


Figure 1 of Beach shows substrate 10, bonding layer 12, first III-nitride buffer body 14, first III-nitride semiconductor body 16, second III-nitride semiconductor body 18, first power electrode 20 and second power electrode 22, and gate arrangement 24, with gate barrier 26 disposed under gate arrangement 24 and over second III-nitride semiconductor body 18.
Ex. 1008 ¶¶ 31–32.

Beach describes a method for making the embodiment shown in Figure 1, wherein “[m]aterials for the gate arrangement are then deposited on gate barrier material 42 and the stack is patterned and etched to obtain gate arrangement 24 over gate barrier 26.” Ex. 1008 ¶ 40. Beach states that “the method as described results in a self-aligned gate arrangement.” Ex. 1008 ¶ 40. Beach further explains that a device made according to the first embodiment is advantageous because, *inter alia*, it is an enhancement-mode device and it includes “self-aligned gates.” Ex. 1008 ¶¶ 43–45.

4. Shenoy (Ex. 1009)

Shenoy is an article titled “Effect of Mask Wall Angle on Shape Evolution during Through-Mask Electrochemical Machining.” Ex. 1009, 1. Shenoy pertains to the development of a “mathematical model to predict

shape evolution during through-mask electrochemical micromachining (EMM).” Ex. 1009, 2.⁹ Shenoy explains that EMM is “receiving increasing attention in microfabrication for patterning, shaping, and finishing.”

Ex. 1009, 2. Shenoy further explains that in through-mask EMM, an exposed metal surface is removed by high-rate anodic metal dissolution, and etching can occur from a single side or both sides simultaneously.

Ex. 1009, 2. According to Shenoy, “[t]he isotropic nature of the metal removal process leads to undercutting of the [photoresist] mask,” and “knowledge of the metal removal rates and undercutting of the photoresist is, therefore, essential in designing the photoresist mask.” Ex. 1009, 2.

Shenoy states that EMM provides cost and environmental advantages over other fabrication techniques, and therefore “the predictability and control of metal wall profile and undercut are of particular interest.”

Ex. 1009, 2. In view of this, Shenoy investigates “the influence of the mask wall angle on the current distribution, the shape of the evolving cavity, and the etch factor.” Ex. 1009, 2.

5. *Ahn (Ex. 1010)*

Ahn is a U.S. patent titled “Thin-Film Transistor and Method of Making the Same” that issued on May 18, 1999. Ex. 1010, codes (45), (54). Ahn is directed to a thin-film transistor having a substrate, a gate having a double layered structure, and method of making same. Ex. 1010 at code

⁹ Citations to Shenoy are to page numbers added by Petitioner.

(57). Figure 4C of Ahn is shown below.

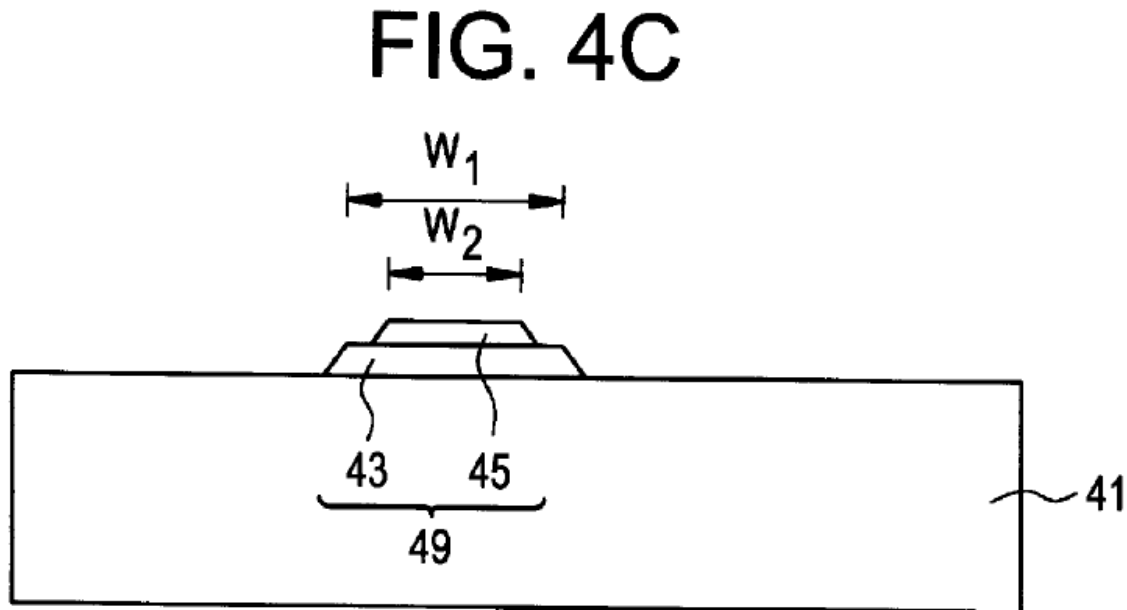


Figure 4C is a diagram depicting a step in the process for fabricating thin-film transistor. Ex. 1010, 5:38–40.

Ahn states that first metal layer 43 and second metal layer 45 result from a single photoresist step and form gate 49 having a double-layered metal structure. Ex. 1010, 6:27–30. Gate 49 has second metal layer 45 positioned substantially in the middle of first metal layer 43. Ex. 1010, 6:30–34.

F. Claims 1–3 – Alleged Obviousness over Saxler, Beach, and Shenoy (Ground 1)

Petitioner contends claims 1–3 of the '347 patent are unpatentable as obvious over Saxler, Beach, and Shenoy. Pet. 24–50; Reply 3–19. Patent Owner argues, *inter alia*, that (1) Petitioner has not shown a reason that a POSITA would have modified the depletion mode transistor of Saxler Figure 1 into the enhancement mode transistor of Petitioner's "Modified Figure 1," and (2) Petitioner has not sufficiently shown how the proposed

method would have the side surfaces (i.e., sidewalls) required by step [1h].
Resp. 21–48; Sur-reply 3–18.

For the reasons explained below, we agree with Patent Owner on both of these points, and therefore, we determine that Petitioner has not established by a preponderance of the evidence that claims 1–3 would have been obvious over Saxler, Beach, and Shenoy.

1. Claim 1

In general, Petitioner asserts that method claim 1 would have been obvious because the combination of Saxler, Beach, and Shenoy results in a process for manufacturing a transistor that has the same structure as the non-recessed embodiment of Saxler Modified Figure 1A, and the method meets the step limitations of claim 1. Pet. 24–49.

Petitioner states that Saxler discloses GaN transistors, such as the one shown below in Saxler Figure 1A, with Petitioner's color annotations added. Pet. 5, 25

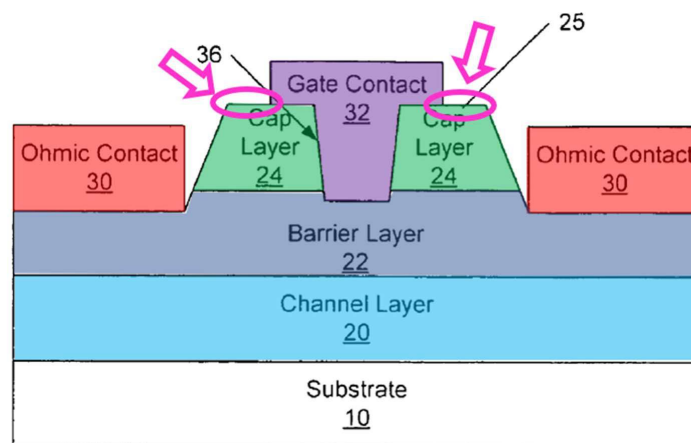
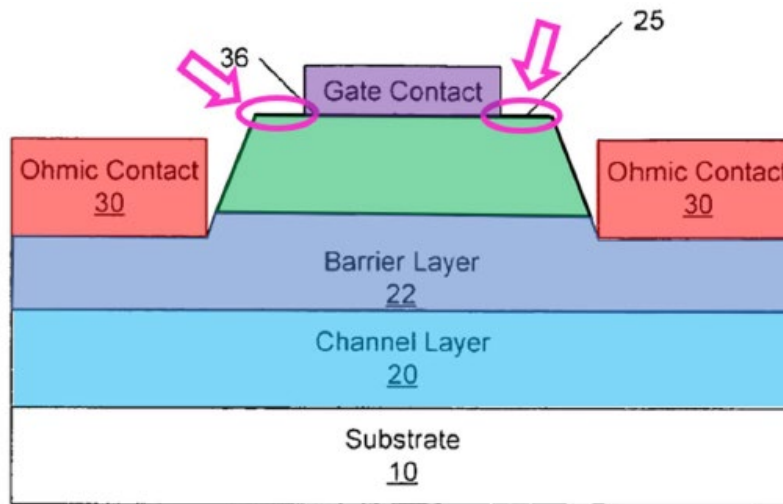


Figure 1A of Saxler shows a cross-sectional schematic view of a transistor having substrate 10, channel layer 20, barrier layer 22, ohmic contacts 30, cap layer 24, and gate contact 32. Petitioner has annotated Figure 1A to show channel layer 20 in light blue, barrier layer 22 in dark blue, cap layer

24 in green, gate contact 32 in purple, and source and drain contacts 30 in red. Pet. 5, 25; Ex. 1007, Fig. 1.

Petitioner asserts that Saxler’s gate contact may be “recessed or non-recessed” and that when the gate recess shown in Figure 1A is not utilized, Saxler would have the structure of Saxler Modified Figure 1A. Pet. 24–25 (citing Ex. 1007 ¶ 52, 66; Ex. 1003 ¶ 81).



Petitioner’s Modified Version of Saxler Figure 1A, with color annotations added, shows non-recessed gate contact 36 (purple), cap layer 32 (green), barrier layer 22 (dark blue), channel layer 20 (light blue), substrate 10, and source and drain contacts (red). Pet. 24–26.

Petitioner further states that “in some embodiments Saxler¹⁰ lacks a gate recess and does not separate the cap layer into distinct portions.” Pet. 40 (citing Ex. 1007, code (57), ¶¶ 12–13, 27, 52, 64, 70–71, 73, claims 3, 14, 21, 27, 31, 88; Pet. § VII.B.9; Ex. 1003 ¶ 111), Pet. 45 (stating the “recess in Saxler’s cap layer 24 is optional, and where not employed the cap

¹⁰ We omit the parties’ emphasis of reference names without specifying “emphasis omitted” throughout.

is a continuous material” and citing Ex. 1007, code (57), ¶¶ 12–13, 27, 52, 64, 70–71, 73, claims 3, 14, 21, 27, 31, 88; Ex. 1003 ¶ 121).

Petitioner contends Saxler discloses making the device of Modified Figure 1A using a series of steps and that the device includes every feature according to the method of the ’347 patent claims. Pet. 24–27, 35–49 (citing Ex. 1015 (“Smith”); Ex. 1021 (“Sheppard”) for gate structures and methods of making them¹¹).

For example, Petitioner asserts Saxler discloses or suggest a method for making an enhancement GaN transistor¹² by forming GaN channel layer 20, (light blue) [1a], forming barrier layer 22 (dark blue) [1b], depositing Ohmic source and drain contacts 30 (red) on the barrier layer [1c], and a p-gate material (cap layer 24 – green) on barrier layer 22 [1d]. Pet. 35–40 (citing Ex. 1007, code (57), ¶¶ 7–10, 13–14, 40, 42 46, 53–66, 69, 71–73 Figs. 1A, 1B, 1F; Ex. 1003 ¶¶ 99–108); *see also* Pet. 36 (stating a POSITA would have understood that Saxler’s transistors were enhancement mode transistors at least because of their gate structure and citing Ex. 1003 ¶ 100).

Petitioner asserts Saxler renders obvious step [1e] (i.e., depositing a gate metal on the p-type gate material) because Saxler’s gate contact is a metal, and in some embodiments—such as that of Saxler’s Modified Figure 1A—Saxler lacks a gate recess and does not separate the cap layer into distinct portions. Pet. 40–41 (citing, *inter alia*, Ex. 1003 ¶¶ 110–111; Ex. 1007 ¶¶ 12–13, 27, 52, 64, 66, 77–71, 73, Fig. 1A).

¹¹ Petitioner does not show that Smith or Sheppard disclose a transistor having the structure of Saxler Modified Figure 1A.

¹² Patent Owner disputes whether the transistor depicted in modified Figure 1A of Saxler would be an enhancement mode device. Resp. 28. We need not, and do not, resolve this dispute.

Petitioner asserts that it would have been obvious to form a photoresist over Saxler's gate metal as required by step [1f] because Saxler precisely positions its gate contact on the cap layer and a POSITA would have understood that using a photoresist over gate metal is a conventional and precise masking technique. Pet. 42 (citing Ex. 1003 ¶¶ 60–62). Petitioner also asserts that, under both parties' proposed claim constructions, Saxler discloses or suggest "etching the gate metal and p-type gate material" to form "side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer" and "etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal" as recited in steps [1g]–[1i]. Pet. 43–49. In particular, Petitioner asserts Saxler etches its cap layer "to expose the underlying barrier" and place the source and drain contacts. Pet. 44 (citing Ex. 1007 ¶ 64, Figs. 1A–1B; Ex. 1003 ¶ 120). According to Petitioner, the "sidewalls of the cap layer extend horizontally towards the source and drain contacts and contact the barrier layer in both recessed and [modified] non-recessed embodiments" and the bottom of the cap layer is more than 10% wider than the top. Pet. 44–45 (emphasis omitted) (citing Ex. 1003 ¶¶ 120, 123).

With respect to step [1i] (i.e., "etching the gate metal to form a pair of ledges on the p-type gate material below the gate metal"), Petitioner asserts that for conventional enhancement mode transistors, ledges are made using separate masks for the p-type gate material and gate metal and that it would have been obvious to use one mask to etch both the gate metal and cap layer to precisely place the gate and reduce manufacturing steps and costs.

Pet. 47–48 (citing *inter alia*, Ex. 1003 ¶ 126; Ex. 1011 ¶ 6, Fig. 1; Ex. 1003 ¶ 124).

Petitioner also relies on the combination of Saxler, Beach, and Shenoy for teaching the limitations of steps [1f]–[1i]. See Pet. 28–35, 48–49. In particular, Petitioner contends that Beach discloses a self-aligned method of making stacked gate structures in GaN HEMT devices using a single mask, and Shenoy discloses isotropic etching techniques for undercutting metal below photoresist masks. Pet. 28–29 (citing Ex. 1008 ¶¶ 40, 45, 54; Ex. 1009, 2–3). Petitioner contends it would have been obvious to make the stacked gate structure of Saxler’s non-recessed embodiments using the methods of Beach and Shenoy to, *inter alia*, reduce steps and costs, and improve reproducibility and symmetry of the gate structure layers, and that doing so would have been simple and predictable. Pet. 31–35 (citing, *inter alia*, Ex. 1011 (“Smith”) and Ex. 1010 (“Ahn”) as teaching self-alignment techniques; Ex. 1003 ¶ 93). Petitioner also notes that the ’347 patent was allowed without disclosing any particular method to obtain the claimed ledges because their manufacture was within the skill level of a POSITA. Pet. 34 (citing Ex. 1002, 25–30, 44–45, 74–76, 80–99; Ex. 1003 ¶¶ 57–63, 98).

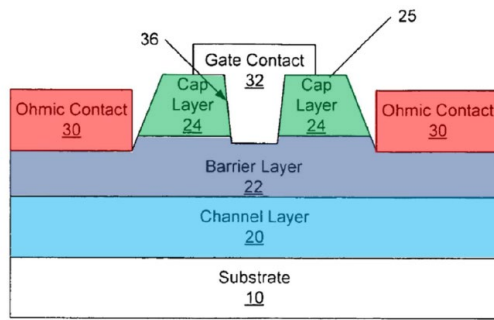
According to Petitioner, self-aligned techniques were common in the field as of the priority date of the ’347 patent, and Sheppard (Ex. 1021), incorporated by reference in Saxler to disclose methods of fabricating GaN transistors, describes a flexible approach to masking and etching. Pet. 33–34 (citing Ex. 1007 ¶¶ 46, 68; Ex. 1021 ¶ 58; Ex. 1003 ¶ 95). Petitioner further contends that a person of ordinary skill in the art would have created the stepped gate structure by using Beach’s self-aligned technique and Shenoy’s

isotropic undercutting to improve reproducibility and symmetry of the gate contact with respect to the gate layer. Pet. 34–35 (citing Ex. 1003 ¶¶ 57–63, 96–98). Petitioner also asserts Beach and Shenoy’s techniques reduce masking steps and costs. Pet. 34–35 (citing Ex. 1003 ¶ 159). Petitioner contends that using Beach’s manufacturing steps and Shenoy’s isotropic techniques would have involved simple substitutions that could be predictably implemented in Saxler’s flexible method of manufacturing. Pet. 35 (citing Ex. 1003 ¶ 98). Finally, Petitioner asserts that the ’347 patent was allowed without disclosing any particular methods to obtain the claimed ledges because such methods were within a POSITA’s ability. Pet. 35 (citing Ex. 1003 ¶¶ 57–63, 98; Ex. 1002, 29, 55).

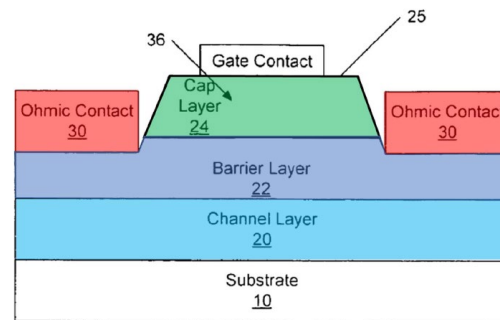
a) Whether Petitioner has Shown Saxler Discloses or Suggests the Non-Recessed GaN Transistor of “Modified Figure 1A”

As noted above, Petitioner’s unpatentability arguments are directed to methods for making the enhancement mode “non-recessed embodiment” of “Saxler Modified Figure 1A.” *See, e.g.*, Pet. 24–35 (stating the method resulting from the “combination of Saxler, Beach, and Shenoy would yield the same structure as the non-recessed Saxler embodiment”); Reply 3–12; *see also* Tr. 41:10–14 (stating grounds 1–3 rely on Beach and Shenoy techniques “as a particular way of making” Saxler Modified Figure 1A).

Patent Owner asserts that (1) Saxler does not disclose or suggest removing the gate recess from Saxler’s depletion mode transistor of Figure 1A and that (2) other than hindsight, Petitioner has not shown a reason that a POSITA would have been motivated to remove the recess in Saxler Figure 1A (below left) to arrive at the enhancement mode transistor of Modified Figure 1A (below right). *See* Resp. 23–28.



Saxler, Fig. 1A.



Saxler, Fig. 1A (modified).

Illustrated above is Saxler Figure 1A (left) depicting a depletion mode transistor having a recessed gate contact (32) and Petitioner’s “Modified Figure 1A” of Saxler (right) depicting an enhanced mode transistor that has been modified by Petitioner to remove the gate recess. *See* Pet. 44–45 (with Petitioner’s color annotations added).

In its Reply, Petitioner states a POSITA “would have had good reason to remove the recess: ‘to turn Saxler’s device into an enhancement mode device, thus realizing the benefits of reduced power consumption and suitability for high power applications.’” Reply 4–5 (citing Pet. 55–56; Ex. 1003 ¶¶ 146–148). At the oral hearing, Petitioner further clarified that it is not asserting that Saxler discloses the enhancement mode device of Saxler Modified Figure 1A, but rather is relying on “an obviousness theory because you need to make that modification,” as well as evidence that a “POSITA would have been motivated to remove that recess *in order to achieve the benefits of enhancement-mode.*” Tr. 26:16–20, 26:22–24 (emphasis added); *see also* Tr. 15:4–6 (stating “the petition shows that POSITA would have removed Saxler’s recess based not only on Saxler’s expressed teachings to do so, *but also to achieve an enhancement-mode device*”) (emphasis added).

Saxler does not disclose an embodiment with a non-recessed gate and sloped sidewalls, and we agree with Patent Owner that Petitioner does not sufficiently show a reason why a POSITA would have been motivated to

remove the recess in Saxler Figure 1A to arrive at the allegedly enhancement mode transistor of Modified Figure 1A. Contrary to Petitioner's assertions in its Reply and at the hearing, *the Petition makes no argument* that a POSITA would have removed the recess from Saxler Figure 1A *to realize the benefits of an enhancement mode transistor*. See Reply 4–5; Pet. 24–68. Rather, the Petition merely asserts that a POSITA would have understood that the gate recess of Figure 1A is optional without providing any persuasive reason why a POSITA would have removed the gate recess but retained the sloped sidewalls of Figure 1A. Pet. 25, 40, 45.

For example, Petitioner asserts that Saxler's gate contact may be "recessed or non-recessed" and that when the gate recess shown in Figure 1A is not utilized, Saxler would have the structure of Saxler Modified Figure 1A. Pet. 25 (citing Ex. 1003 ¶ 81; Ex. 1007 ¶ 52, 66); *see also* Pet. 40, 45 (citing Ex. 1007 ¶ 52). Neither of these paragraphs provide sufficient motivation to a POSITA to remove the gate recess from Saxler Figure 1A. Saxler paragraph 52 states:

Exemplary devices according to some embodiments of the present invention are schematically illustrated in FIGS. 1A through 6. Thus, while embodiments of the present invention are described herein with reference to a recessed gate structure or a non-recessed gate structure, other embodiments of the present invention may include or not include a gate recess. Accordingly, embodiments of the present invention should not be construed as limited to the particular exemplary embodiments described herein but may include any suitable structure having a cap layer and/or passivation layer as described herein.

Ex. 1007 ¶ 52.

Petitioner's expert, Dr. Shealy states that he understands paragraph 52 to mean that it is "fair game to pull the recess out of any of those figures

[Figures 1A through 6].” Ex. 2004, 39:12–21. Dr. Shealy, however, also clarifies that “[a]s I said before, I think you could take all the embodiments and bring in which ones you want, *depending on what you’re trying to accomplish.*” Ex. 2004, 40:24–41:1. During the hearing, Petitioner admitted that Dr. Shealy’s “statement to modify the reference depending on what you’re trying to accomplish” means that “a POSITA may modify *with reason to do so. A POSITA would have removed Saxler’s recess to obtain the benefits of enhancement-mode.*” Tr. 19:19–25. Again, the Petition does not provide a *reason* why a POSITA would have removed Saxler’s gate recess.

Moreover, Saxler’s Figure 1B provides an embodiment lacking a gate recess. The fact that Saxler already discloses an embodiment lacking a recess cuts against Petitioner’s argument that a POSITA would have removed the recess in Saxler Figure 1A to arrive at the structure in Modified Figure 1A. Petitioner has not demonstrated sufficiently why a POSITA would have removed the recess from Figure 1A to arrive at the structure in Modified Figure 1A when Figure 1B already discloses an embodiment lacking a recess.

The other paragraphs of Saxler cited by Petitioner (i.e., Ex. 1007 ¶¶ 12, 13, 27, 70, 71, and 73 cited at Pet. 40, 45) discuss characteristics of various embodiments of the invention that either have, or do not have, a gate recess, without stating that the gate recesses are interchangeable among the embodiments or that a gate recess could, or should, be removed from embodiments having such a recess. Nor do they indicate why a person of ordinary skill in the art would have done so. Similarly, Saxler’s claims recite limitations of transistors either having a recessed or non-recessed gate

contact but do not indicate that a gate recess could be removed from embodiments having a recess, or indicate why a person of ordinary skill in the art would have done so. *See* Pet. 40, 45 (both citing Ex. 1007, claims 3, 14, 21, 27, 31, 88). Petitioner also cites to Saxler’s abstract and paragraph 64. *See* Pet. 40, 45. Neither Saxler’s abstract nor paragraph 64 refer specifically to gate recesses. *See* Ex. 1007, code (57), ¶ 64. Paragraph 64 states that although Figures 1A and 1B depict recessed ohmic contacts “in some embodiments of the present invention, the ohmic contacts 30 need not be recessed.” Ex. 1007 ¶ 64. A statement that ohmic contacts need not be recessed does not disclose or suggest that a recessed gate contact need not be recessed.

Petitioner also cites to references incorporated by reference in Saxler for allegedly “disclosing non-recessed gate electrodes in stacked structures similar to Saxler’s recessed stacked gate structure” and methods for making such gate structures. *See, e.g.*, Pet. 26–28 (citing Ex. 1021 (“Sheppard”) ¶¶ 44–51, Figs. 1A–1F; Ex. 1015 (“Smith”) ¶¶ 10, 17, 33–37, 39–44, Figs. 3, 4A–4C, 5A–B, 6A–6C; Ex. 1003 ¶¶ 82–85). Petitioner asserts that a POSITA would have understood these non-recessed electrodes were a suitable option for Saxler’s cap. Pet. 26–28. Petitioner, however, does not point to any teaching in either Sheppard or Smith of a non-recessed gate structure having sloped sidewalls. Nor does Petitioner sufficiently explain how Sheppard’s or Smith’s structures are “similar” to Saxler’s recessed, stacked gate structure. As such, these cited references do not sufficiently support Petitioner’s contention that a POSITA would have been motivated to remove Saxler’s recessed gate from Saxler Figure 1A.

In its Reply, Petitioner also states that its proposed modification simplifies Saxler's Figure 1A by removing steps to form a recess in its gate. Reply 7 (citing Pet. 25, 27, 31–32, 45, 57). To the extent Petitioner is now arguing that it would have been obvious to remove the recess of Figure 1A to simplify the manufacturing process, this argument was not presented in the Petition and is thus untimely. Moreover, this argument is also not persuasive because it does not address the other embodiments in Saxler that lack a recess, such as Figure 1B. Petitioner has not shown why a POSTIA would have been motivated to modify Saxler's Figure 1A to arrive at Modified Figure 1A and avoid the recess forming steps where Saxler already discloses another embodiment made without recess forming steps. Ex. 1007, Fig. 1B.

Thus, for at least the above reasons, Petitioner fails to demonstrate by a preponderance of the evidence that claim 1 would have been obvious over Saxler, Beach, and Shenoy.

b) Whether Petitioner has Sufficiently Shown the Proposed Method Would Etch the p-Type Gate Material to Form the Side Surfaces of step [1h]

Petitioner initially relies on Beach and Shenoy for teaching methods to make Saxler's Modified Figure 1A. *See, e.g.*, Pet. 31 (stating a POSITA would have found it obvious to make the stacked gate structure of Saxler's non-recessed embodiment using Beach and Shenoy's methods); *see also*, *e.g.*, Tr. 41:10–20 (“bringing in . . . Beach and Shenoy techniques as a particular way of making that device,” i.e., non-recessed Saxler Modified Figure 1A). Subsequently, Petitioner asserts that Saxler discloses step [1h] under either Petitioner's or Patent Owner's proposed claim construction because Saxler etches its cap layer 24 such that the bottom of the cap layer is

more than 10% wider than the top.¹³ Pet. 44–46 (citing Ex. 1007 ¶¶ 12–13, 27, 52, 64, 70–71, 73, claims 3, 14, 27, 31, 88, Fig. 1A, “Modified Fig. 1A”; Ex. 1003 ¶¶ 120–123).

Patent Owner responds that Petitioner’s proposed method relies on Beach’s self-aligned technique, which would either cut off, or not form, the horizontally extending “sloped” side surfaces that Petitioner relies on from Saxler Fig. 1A. Resp. 38. Patent Owner asserts that because Beach’s etching technique would result in generally vertical sidewalls, not the sloped sidewalls of Saxler, Petitioner’s proposed combination does not teach a process that forms side surfaces of p-type gate material that extend horizontally toward the source and drain contact. Resp. 39 (citing Ex. 2005 ¶¶ 143–146).¹⁴

In its Reply, Petitioner asserts that combination would not “cut off” Saxler’s cap layer side walls because the combination “uses Saxler’s etching technique to slope the sidewalls with Beach’s single mask.” Reply 18 (citing Pet. 31–35).

We disagree with Petitioner because the Petition, when discussing how a POSITA would have combined Beach and Saxler, does not clearly

¹³ The parties agree that the sloped sidewalls of the p-GaN layer depicted in Saxler Figure 1A have “side surfaces of the p-type gate material that extend horizontally towards to source and drain contacts” as recited in step [1h] under either parties’ claim construction.

¹⁴ Patent Owner admits that there may potentially be “some curvature” to the sidewalls. Resp. 39. Petitioner however, does not rely on any potential “curvature” of the sidewalls following Beach’s etching to establish unpatentability, but rather on Saxler’s “sloped walls” depicted in Saxler Figure 1A and Modified Figure 1A having “a 10% slope” that is “wider on the bottom than the top.” See Pet. 45–46.

state that the combined process would use Saxler's etching technique with Beach's single mask process for making stacked gate structures. *See* Pet. 30–34 (citing, *inter alia*, Ex. 1003, 57–63, 89–98). As acknowledged by Petitioner, Beach's manufacturing steps, including Beach's etching steps, result in device having straight side walls. *See* Pet. 33 (citing Ex. 1008, Fig. 1 which depicts straight sidewalls). Rather than stating to use Saxler's etching steps with Beach's process, the Petition states that it would have been obvious to use “Beach's manufacturing steps” as they are “no more than simple substitutions.” Pet. 34. Moreover, the Petition explicitly describes Beach's single-gate method as including Beach's etching steps to be substituted for Saxler's multi-gate method. *See* Pet. 33 (stating that Beach's process (i) deposits both the gate barrier 26 and gate arrangement 24 layers, (ii) patterns the stack with a mask, (iii) *etches both layers* to obtain the stack, and (iv) deposits power electrodes and citing Ex. 1008, 40; Ex. 1003 ¶ 94). This further supports our understanding that Petitioner's proposed combination relies on Beach's, not Saxler's, etching steps.

Petitioner also states that it “would have been obvious to create Saxler's gate structure with Beach's approach for improved alignment between layers.” Pet. 34 (citing Ex. 1003 ¶ 95). Dr. Shealy further testifies that it “would have been obvious to look to Beach for its simple methods for making stacked gate structures.” Ex 1003 ¶ 95. The Petition also asserts that Saxler's “flexible approach to masking and etching,” makes the “choice of Beach's manufacturing steps no more than simple substitution.” Pet. 34.

Again, from these statements we do not understand Petitioner's argument to be that a person of ordinary skill in the art would have used Saxler's etching steps—as opposed to Beach's etching steps—with Beach's

single mask to etch away both underlying layers. Thus, the Petition fails to demonstrate sufficiently that the asserted combination of Saxler and Beach would result in a structure having sloped sidewalls, as opposed to the straight side walls resulting from Beach's etching steps.

Petitioner does note that the '347 patent was allowed without disclosing any particular method to etch the gate metal and obtain the claimed ledges because such methods were known. Pet. 35 (citing Ex. 1002, 25–30, 44–55, 74–76, 80–99; Pet. §§ II, III.B; Ex. 1003 ¶¶ 57–63).

Petitioner asserts that Saxler discloses “sloped sidewalls with the claimed ledges and *Beach and Shenoy would have provided a known, obvious way to create that structure.*” Pet. 35 (citing Pet. §§ VII.A.1, VII.4–5; Ex. 1003 ¶ 98) (emphasis added). This conclusory sentence and citation to the prosecution history also does not sufficiently show how using “Beach and Shenoy” would provide a known obvious way to create a structure having sloped sidewalls, as opposed to the straight side walls resulting from Beach's etching steps.

A petition must identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim.” 35 U.S.C. § 312(a)(3) Here, Petitioner merely provides general assertions about multiple references, without clearly identifying how, or why a POSITA would have been motivated, to modify the processes disclosed in those references to arrive at the claimed invention. Thus, the Petition does not state with particularity that Saxler's particular technique for etching is to be used instead of Beach's etching step when substituting Beach's self-aligned process for Saxler's two mask process. Nor does the Petitioner provide a sufficient reason, absent hindsight, why a POSITA would have been

motivated to combine the references to result in a process that forms Saxler's Modified Figure 1A.

Thus, for these additional reasons, Petitioner has not shown by a preponderance of the evidence that claim 1 would have been obvious over Saxler, Beach, and Shenoy.

2. *Claims 2–3*

Claim 2 depends from claim 1 and further requires that the step of etching the gate metal comprises etching the gate metal to reduce a width of the gate metal such that the width of the gate metal is less than a width of the p-type gate material. Ex. 1001, 5:15–18. Claim 3 depends from claim 1 and requires that the “pair of ledges of the p-type gate material are self-aligned.” Ex. 1001, 5:19–20. None of Petitioner's contentions regarding claims 2 and 3 remedy the deficiencies set forth above. *See* Pet. 49–50. Accordingly, Petitioner has not established by a preponderance of the evidence that claims 2–3 would have been obvious over Saxler, Beach, and Shenoy.

G. *Claims 1–3 – Alleged Obviousness over Saxler, Yoshida, Beach, Shenoy (Ground 2)*

Petitioner asserts that claims 1–3 of the '347 patent are unpatentable as obvious over Saxler in view of Yoshida, Beach, and Shenoy. Pet. 50–60; Reply 1–8. Patent Owner responds, *inter alia*, that Petitioner's arguments to combine Beach and Shenoy with Saxler and Yoshida are the same reasons set forth in ground 1 to combine Beach and Shenoy with Saxler, and thus fail for the same reasons set forth above in connection with ground 1. Resp. 50 (citing Resp. § VI.F [sic], pp. 37–39); Ex. 2005 ¶¶ 205–208.

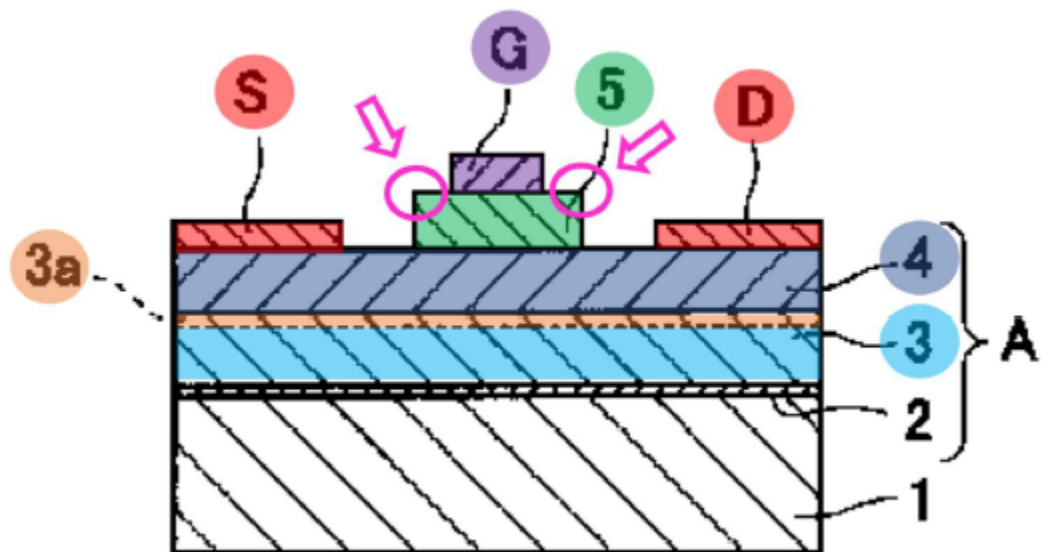
As explained below, we agree with Patent Owner that Petitioner fails to show a sufficient reason a POSITA would have combined Saxler-Yoshida

with Beach and Shenoy to arrive at the side surfaces limitations of step [1h] and, therefore, we determine that Petitioner has not established by a preponderance of the evidence that claims 1–3 would have been obvious over Saxler, Yoshida, Beach, and Shenoy.

1. Claim 1

Petitioner contends that “to the extent” Saxler alone does not render the non-recessed gate structure of Modified Figure 1 obvious as asserted in ground 1, “Yoshida further renders it obvious.” *See* Pet. 54; *see also* Pet. 52–56 (setting forth motivations to combine Saxler and Yoshida).

In particular, Petitioner states that both Saxler and Yoshida disclose compatible enhancement-mode GaN HEMT devices having the same layers, performing the same functions. Pet. 52–53. Petitioner states that Yoshida discloses an enhancement-mode device having stacked gate structures such as the one shown below in Yoshida Figure 1A, with Petitioner’s color annotations added.



Petitioner’s color annotated version of Yoshida Figure 1 shows a cross-sectional view of a transistor having GaN layer 3 (highlighted in light blue)

and n-type semiconductor layer 4 (highlighted in dark blue) formed over barrier layer 2 and substrate 1, with 2DEG 3a (highlighted in orange) forming at the interface of layers 3 and 4, source contact S and drain D (red), and a stacked gate structure above semiconductor layer 4 consisting of gate metal G (highlighted in purple) overlaying doped GaN layer 5 (highlighted in green). Pet. 50–51 (citing Ex. 1006, code (57), ¶¶ 9, 10, 13, 15, 19).

Petitioner contends that implementing Yoshida’s non-recessed gate structure in Saxler’s stacked gate structure would result in the same arrangement as Saxler’s non-recessed embodiment shown in modified Figure 1A of Saxler. Pet. 51–52. Petitioner asserts that it would have been obvious to combine Saxler’s stacked gate structure with Yoshida’s non-recessed gate structure because a person of ordinary skill in the art would have been familiar with a wide variety of stacked gate structures in GaN HEMT devices, including many without recessed gates, Saxler repeatedly teaches that its gate recess is optional, using Yoshida’s non-recessed gate fabrication techniques would simplify manufacturing and decrease costs, and the combination of *Yoshida*’s non-recessed gate arrangement in Saxler’s gate arrangement is nothing more than the simple substitution of known elements to predictably yield an enhancement mode GaN HEMT device. Pet. 54–56. Petitioner also asserts a POSITA would have removed Saxler’s gate recess to “turn Saxler’s device into an enhancement mode device, thus realizing the benefits of reduced power consumption and suitability for high power applications.” Pet. 52–55.

With respect to the limitations recited in steps [1f]–[1i], Petitioner states that because the Saxler-Yoshida gate structure is the same as the non-recessed Saxler structure of Modified Figure 1A, “it would have been obvious to combine Saxler-Yoshida with Beach and Shenoy, disclosing” steps [1f]–[1i] “for the same reasons” explained for Saxler, Beach, and

Shenoy set forth with respect to ground 1. Pet. 56 (citing Pet. § VII.A.5, [Pet. 31–35]), Pet. 57–59 (citing, *inter alia*, Pet. § VIII.A.2-A.3, VII.B.7–B.10).

Patent Owner responds, *inter alia*, that Petitioner’s arguments to use Beach and Shenoy’s methods that are based on ground 1 fail for the same reasons set forth above in connection with ground 1. Resp. 50 (citing Resp. § VI.F [sic], pp. 37–39); Ex. 2005 ¶¶ 205–208.

We agree with Patent Owner that Petitioner fails to show that a POSITA would have combined Saxler, Yoshida, Beach, and Shenoy to arrive at the side surfaces limitations of step [1h]. Similar to ground 1, Petitioner states that in the proposed combination, “Beach and Shenoy would be used to form Saxler-Yoshida’s gate structure.” Pet. 52 (citing Ex. 1003 ¶ 138). Petitioner relies on the same arguments in ground 2 to combine Saxler-Yoshida with Beach and Shenoy to arrive at the side surfaces limitations of step [1h] that it relied on in ground 1. *See, e.g.*, Pet. 58 (citing Petitioner’s arguments for ground 1). For the same reasons stated above in Section II.F.2.b regarding ground 1, Petitioner has not sufficiently shown that the combination of Saxler-Yoshida with Beach and Shenoy would arrive at the side surfaces limitations of step [1h]. Thus, Petitioner has not shown by a preponderance of the evidence that claim 1 would have been obvious over Saxler, Yoshida, Beach, and Shenoy.

2. Claims 2–3

Petitioner also asserts that claims 2–3, which depend from claim 1, would have been obvious over Saxler, Yoshida, Beach, and Shenoy. Pet. 59–60. None of Petitioner’s contentions regarding claims 2 and 3 remedy the deficiencies set forth above. Pet. 59–60. As such, Petitioner has

not established by a preponderance of the evidence that claims 2–3 would have been obvious over Saxler, Yoshida, Beach, and Shenoy.

H. Claims 1–3 – Alleged Obviousness over Saxler and Ahn (Ground 3)

Petitioner contends claims 1–3 of the '347 patent are unpatentable as obvious over Saxler and Ahn. Pet. 60–72; Reply 1–8. Patent Owner responds, *inter alia*, that because Ground 3 relies on the same structure based on the same rationale as ground 1 (i.e., Petitioner's Saxler Modified Figure 1A), that ground 3 is improper for at least the same reasons. Resp. 51–52 (citing, *inter alia*, Resp. § VII.B [Resp. 23–28]).

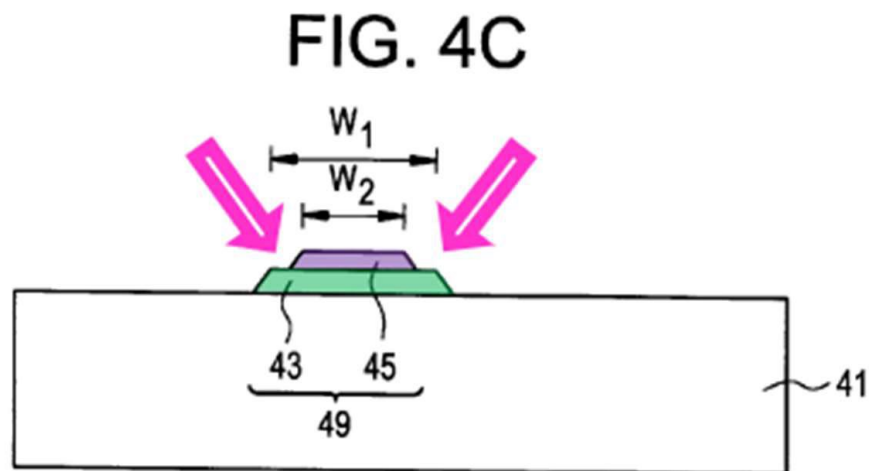
For the reasons explained below, we agree with Patent Owner that Petitioner's ground 3 arguments fail to sufficiently show that a person of ordinary skill in the art would have had reason to remove the gate recess shown in the depletion mode device of Saxler Figure 1A to arrive at non-recessed, allegedly enhancement mode device of Petitioner's "Modified Saxler Figure 1A," upon which Petitioner's unpatentability arguments rest. Therefore, we determine that Petitioner has not established by a preponderance of the evidence that claims 1–3 would have been obvious over Saxler and Ahn.

1. Claim 1

Petitioner contends that "to the extent Saxler alone does not explicitly disclose masking and etching the gate contact or self-aligned etching, Ahn renders this obvious." Pet. 60. Significantly, Petitioner does not rely on Ahn for (1) teaching or suggesting enhancement-mode GaN transistors or (2) providing a reason why a POSITA would have modified Saxler's Figure 1A to remove the gate recess in order to arrive at an enhancement mode

transistor. *See generally* Pet. 60–68; *see also* Pet. 62–63 (presenting arguments similar to those set forth for ground 1); Reply 21–23. Rather, Petitioner asserts that it would have been obvious “to make the Saxler’s non-recessed stacked gate structure [i.e., the “enhancement mode” structure of Saxler’s Modified Figure 1] using Ahn’s method of forming a transistor gate.” Pet. 62 (citing Ex. 1003 ¶¶ 172–176); *see also* Pet. 65–70 (asserting the combination of Saxler and Ahn render obvious steps [1f]–[1i]).

More particularly, Petitioner asserts that Ahn teaches using a single mask with isotropic and anisotropic etching to create stacked gate structures having stepped features and sloped sidewalls. Pet. 60 (citing Ex. 1010, code (57), 3:41–58, 6:15–26, 7:7–14, Figs. 4A–4C; Ex. 1003 ¶169). Ahn’s Figures 4A–4C, with Petitioner’s annotations added, are reproduced below.



Ahn Figure 4C is a diagram illustrating part of a process for fabricating a thin-film transistor, with color annotations added by Petitioner. Ex. 1010, 4:14–16.

Petitioner asserts that Ahn teaches using a single photomask to etch Ahn’s top gate metal layer (purple) and underlying layer (green) to have sloped sidewalls and a pair of horizontal ledges (pink arrows) on either side of the top gate material (purple). Pet. 60 (citing Ex. 1010, code (57), 3:41–58,

6:15–26, 7:7–14, Figs. 4A-4C; Ex. 1003 ¶ 169). Petitioner asserts that its layers are symmetric and their side surfaces preferably have an inclined shape. Pet. 60 (citing Ex. 1010, 6:12–37, Fig. 4C; Ex. 1003 ¶ 169).

Petitioner asserts that it would have been obvious to make Saxler's non-recessed stacked gate structure (i.e., Saxler's Modified Figure 1A) using Ahn's method of forming a transistor gate. *See* Pet. 62–64 (citing, *inter alia*, Ex. 1003 ¶¶ 57–63, 174; Pet. §§ II [Pet. 2–8], III.B [Pet. 12–16]). Petitioner contends that a POSITA would have been motivated to use a single mask as taught by Ahn, in place of Saxler's two mask process, to simplify the process and reduce costs. Pet. 63 (citing, *inter alia*, Ex. 1003 ¶ 91; Ex. 1007 ¶¶ 65–66).

Patent Owner argues that Petitioner has not shown a reason a POSITA would have modified Saxler Figure 1A to arrive at Petitioner's Modified Figure 1A for the same reasons set forth regarding ground 1. We agree with Patent Owner. Similar to its arguments for ground 1, in ground 3, the Petitioner does not provide any sufficient reason *why* a POSITA would have modified Saxler Figure 1A to arrive at modified Figure 1A or provide any reason why a POSITA would have had a reason to modify the depletion mode device of Figure 1A to the enhancement mode device of Modified Figure 1A.

As noted above, Petitioner does not rely on Ahn for either (1) teaching or suggesting enhancement-mode GaN transistors or (2) providing a reason why a POSITA would have modified Saxler's Figure 1A to remove the gate recess in order to arrive at an enhancement mode transistor. *See generally* Pet. 60–68; *see also* Pet. 62–63 (presenting arguments similar to those set forth for ground 1); Reply 21–23. Indeed, Ahn is not directed to GaN

transistors, let alone an enhancement-mode device, but rather is directed to thin film transistors for liquid crystal displays. *See* Ex. 2005 ¶ 74 (citing Ex. 1010, 7:4–6); *see also* Resp. 21 (stating that Ahn is directed to thin film transistors for liquid crystal displays); Reply 22.

Thus, similar to ground 1, Petitioner’s unpatentability arguments for ground 3 use Saxler’s non-recessed stacked gate structure (Modified Figure 1A) as a starting point for its unpatentability arguments. *See* Pet. 63 (discussing ways to create “Saxler’s stepped gate structure in its non-recessed embodiments”). For the same reasons set forth above in Section II.F.2.a, Petitioner has not sufficiently shown that a POSITA would have had reason to modify the depletion mode transistor of Saxler Figure 1A to remove the gate recess to arrive at Petitioner’s Modified Figure 1A.

Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 1 would have been obvious over Saxler and Ahn.

2. *Claims 2–3*

Petitioner also asserts that claims 2–3, which depend from claim 1, would have been obvious over Saxler and Ahn. Pet. 70–72. None of Petitioner’s contentions regarding claims 2 and 3 remedy the deficiencies set forth above. Thus, Petitioner has not established by a preponderance of the evidence that claims 2–3 would have been obvious over Saxler and Ahn.

I. *Claims 1–3 – Alleged Obviousness over Yoshida, Saxler, Beach, and Shenoy (Ground 4)*

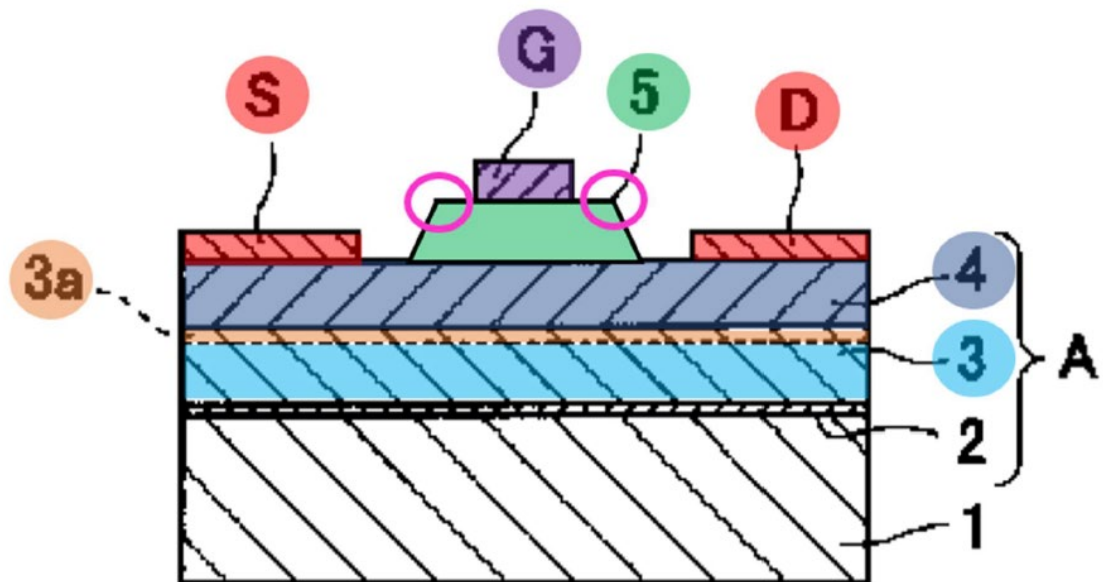
Petitioner asserts that claims 1–3 would have been obvious over the combination of Yoshida, Saxler, Beach, and Shenoy. Pet. 72–95; Reply 1–8. Patent Owner argues, *inter alia*, that Petitioner has not shown a sufficient reason that a POSITA would have etched gate metal of Yoshida or Yoshida-

Saxler to form a pair of ledges on the p-type gate material as required by step [1i]. Resp. 57–61; Sur-reply 23–25.

For the reasons explained below, we agree with Patent Owner, and therefore, we determine that Petitioner has not established by a preponderance of the evidence that claims 1–3 would have been obvious over Yoshida, Saxler, Beach, and Shenoy.

1. Claim 1

Petitioner asserts that “[i]mplementing Saxler’s sloped sidewalls in Yoshida’s layer 5 results in the following combined structure,” i.e., Modified Yoshida Fig. 1. Pet. 73. Petitioner states that in the combination, “the gate structure would have been made using Beach and Shenoy’s techniques.” Pet. 73.



Yoshida, Fig. 1 (modified).

Petitioner's Modified Yoshida Figure 1 is an enhancement mode transistor having gate G (purple), p-GaN layer 5 (green), source (S) and drain D (red). Pet. 73.

Petitioner contends that Yoshida or Yoshida and Saxler teach forming a GaN layer and a barrier layer, depositing source and drain contacts on the barrier layer, and depositing a p-type gate material and a gate metal as recited in steps [1a]–[1e]. Pet.72–84. Petitioner further asserts that although Yoshida does not expressly disclose forming a photoresist on the gate layer and etching the gate metal, as explained for ground 1, a POSITA would have found it obvious to mask and etch the gate metal in view of Saxler to precisely and reliably position the gate metal. Pet. 86–87 (citing, *inter alia*, Ex. 1003 ¶¶ 219, 222).

Petitioner further asserts that it would have been obvious to make the Yoshida-Saxler gate structure with Beach's and Shenoy's approach to use a single photomask over the gate metal with isotropic etching for the same reasons asserted with respect to ground 1. Pet. 87–88¹⁵.

With respect to step [1h], which requires etching the p-type gate material to form the recited side surfaces, Petitioner asserts that it “would

¹⁵ Petitioner's citations for support as to why it would have been obvious to make Yoshida-Saxler's gate structure with Beach and Shenoy's approach to using a single photomask over the gate metal with isotropic etching ultimately rely on its arguments set forth in ground 1. *See* Pet. 87–88 (citing Pet. § X.A.2 [Pet. 73–79]); *see also* Pet. 76 (stating it would have been obvious to make the stacked gate structure of the Yoshida-Saxler device for the same reasons explained for Saxler alone (ground 1) or the Saxler-Yoshida device (ground 2) and citing Pet. §§ VII.A.5 (Pet. 31–35 (ground 1)), VIII.A.3 (Pet. 52–56); *see also* Pet. 56 (ground 2) stating it would have been obvious to use the methods of Beach and Shenoy to fabricate the Saxler Yoshida gate structure for the same reasons discussed with respect to ground 1.

have been obvious to combine the sloped sidewalls of Saxler's doped cap layer into Yoshida's p-type layer 5 so that they horizontally extended towards the source and drain contacts in the Yoshida-Saxler device, resulting in the sloped structure" meeting the side surfaces limitation of step [1h]. Pet. 88–89 (citing Pet. § X.A.2 [Pet. 73–79]; Ex. 1003 ¶ 227).

Petitioner also asserts that it would have been obvious to make the Yoshida-Saxler gate structure with Beach's approach of using a single photomask over the gate metal to reduce gate leakage. Pet. 73–76, 90–92. Petitioner also asserts that Yoshida alone teaches sloped sidewalls that extend horizontally towards the source and drain under Patent Owner's claim construction because a POSITA would have known that sidewalls drawn vertically would have a slight slope when built in a practical device. Pet. 90–92 (citing Ex. 1007 ¶ 42; Ex. 1020 ("Uemoto¹⁶"), Figs. 1–2, 5; Ex. 1003 ¶ 230).

With respect to step [1i], which requires etching the gate metal to form a pair of ledges on the p-type gate material below the gate material, Petitioner asserts that the "gate structure would have been made using Beach and Shenoy's techniques." Pet. 73. Petitioner states Yoshida-Saxler teaches a stacked, stepped gate structure having a pair of ledges, as shown in Yoshida's modified Figure 1, and that it would have been obvious to make those ledges by masking and etching the gate metal using a single mask. Pet. 92 (citing Pet. §§ X.A.1–X.A.2 [Pet. 73–79], § X.B.7–X.B.9 [Pet. 86–92]; Ex. 1003 ¶¶ 197–209, 231). Dr. Shealy testifies that a POSITA would

¹⁶ Uemoto et al., *A Normally-off AlGaIn/GaN Transistor with $R_{on}A=2.6\Omega\text{cm}^2$ and $BV_{ds}=640\text{V}$ Using Conductivity Modulation*, IEEE Paper, 2006 (Ex. 1020).

have simply substituted Yoshida's vertical side walls of its p-GaN layer with Saxler's sloped sidewalls and this could be accomplished by simply substituting Saxler's etching approach to shape Yoshida's side walls.

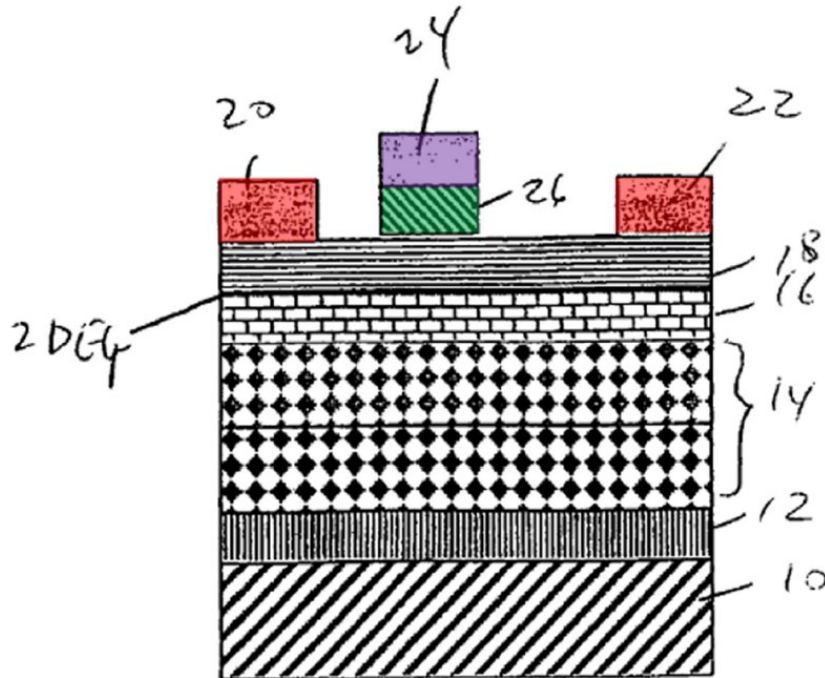
Ex. 1003 ¶¶ 197–200. Petitioner acknowledges that Yoshida deposits its gate metal for the gate electrode into a mask opening and does not disclose forming a photoresist on the gate and etching the gate metal. Ex. 1003 ¶ 202 (citing Ex. 1006 ¶ 22–23). Petitioner asserts that it would have been obvious to form a single photoresist over the gate metal to etch both the gate metal and the underlying layer because this method would result in greater precision and reliability when positioning the gate metal. Ex. 1003 ¶ 202.

Petitioner further argues that Yoshida-Saxler, Beach, and Shenoy render obvious etching the gate metal to form the ledges of [1i] because a POSITA would have found implementing Beach and Shenoy's techniques obvious. Petitioner asserts that Shenoy's method to isotropically etch the gate metal would generate the pair of ledges on Yoshida-Saxler's layer 5 and that it would have been obvious and predicable to combine Yoshida-Saxler's techniques with Beach's single mask process and Shenoy's isotropic etching to arrive at the Yoshida-Saxler structure. Pet. 93–94 (citing Ex. 1003 ¶¶ 197–209, 232).

Patent Owner responds that Petitioner fails to show a sufficient reason why a POSITA would have performed etching steps to form a pair of ledges as recited in step [1i]. Resp. 57–61. We agree with Patent Owner.

As described above, Petitioner argues that in ground 4, “the gate structure would have been made using Beach and Shenoy's techniques.” Pet. 73. Petitioner states that the self-aligned technique of Beach results in

the etching of both gate metal and p-type gate material as shown in Beach, Figure 1 below. Pet. 79.



Beach, Fig. 1.

Beach Figure 1, with color annotations added by Petitioner, depicts a cross sectional view of a semiconductor device having gate arrangement 24, gate barrier 26, first and second power electrodes (20, 22). Ex. 1008 ¶¶ 19, 31–32; Pet. 79.

Petitioner admits that Beach does not disclose steps to create the horizontal ledges of Yoshida-Saxler's stacked gate structure following its self-aligned process, but asserts that Shenoy discloses simple isotropic etching techniques for symmetrically undercutting metal layers below photoresist masks. Pet. 79. Petitioner asserts that it would have been obvious to use Shenoy's methods to undercut the gate electrode and create Yoshida-Saxler's horizontal ledges to predictably create Yoshida-Saxler's stacked gate structure more efficiently and symmetrically. Pet. 79–80.

Patent Owner persuasively argues that a POSITA would have no reason, other than hindsight, to undercut the gate electrode in the combined Yoshida-Saxler-Beach-Shenoy process. Resp. 57–61. In Yoshida’s process, the p-GaN layer is wider than the gate (i.e., has ledges) to ensure that when the gate metal is deposited, the gate electrode will not overhang the p-GaN layer. Resp. 58; Ex. 2005 ¶ 259. Yoshida does not provide any other purpose for its ledges. Thus, a POSITA would not have any reason to perform additional etching steps, such as those of Shenoy, to form claimed ledges that do not have any function after gate metal G is loaded onto the p-GaN layer using Beach’s self-aligning process. *See* Resp. 60. Petitioner has not identified any reason why a POSITA would perform the etch, other than to provide the Yoshida-Saxler structure. *See* Pet. 79–80. Performing unnecessary etching would add manufacturing costs and steps, producing a less efficient method, contrary to the motivations relied on by Petitioner. *See* Resp. 61 (citing Pet. 32, 35, 48, 54–56, 64, 77; Ex. 1003 ¶¶ 95, 205).

In its Reply, Petitioner asserts that the proposed method uses fewer masks and is more precise than a two-mask approach. Reply 35. Petitioner also asserts that Yoshida’s ledges “would increase leakage paths and result in lower leakage.” Reply 25 (citing Pet. 73–75; Ex. 1003 ¶¶ 197, 201).

Contrary to Petitioner’s assertions, however, the Petition did not argue that Yoshida’s (or Saxler’s) ledges would increase leakage paths and result in lower leakage. Rather, the Petition merely states that Saxler’s sloped sidewalls increase the leakage paths, resulting in lower leakage. Pet. 74–75. Neither the Petition nor Dr. Shealy provide any motivation for forming ledges after performing Beach’s etching steps.

Petitioner does not dispute that Yoshida's p-GaN layer is wider than the gate metal layer in order to receive the gate electrode without overhang. Nor does Petitioner dispute that Beach's etching steps would remove the ledges. *See generally* Reply; *see also* Pet. 79 (depicting Beach's single mask etching process as resulting in a structure with no ledges). Petitioner has not shown a sufficient reason why a POSITA would perform an additional etching step to form the ledges in the Yoshida or Yoshida-Saxler devices after the p-GaN and gate meal have been etched in Beach's process to form the gate. As such, Petitioner has not shown a reason that a POSITA would have performed step [1i] when combining the Yoshida, Saxler, Beach, and Shenoy.

Accordingly, Petitioner has not shown by a preponderance of the evidence that claim 1 would have been obvious over Saxler, Yoshida, Beach, and Shenoy.

2. *Claims 2–3*

Petitioner also asserts that claims 2–3, which depend from claim 1, would have been obvious over Yoshida, Saxler, Beach, and Shenoy. Pet. 94–95. None of Petitioner's contentions regarding claims 2 and 3 remedy the deficiencies set forth above. Thus, Petitioner has not established by a preponderance of the evidence that claims 2–3 would have been obvious over Yoshida, Saxler, Beach, and Shenoy.

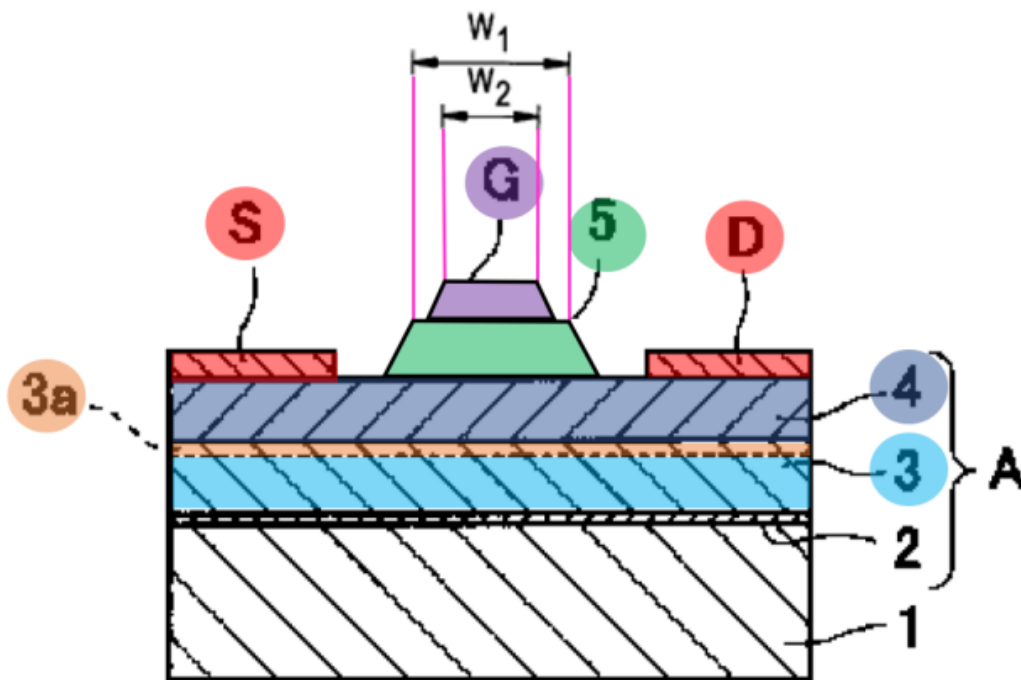
J. *Claims 1–3 – Alleged Obviousness over Yoshida and Ahn (Ground 5)*

Petitioner contends claims 1–3 of the '347 patent are unpatentable as obvious over Yoshida in view of Ahn. Pet. 95–106. Patent Owner argues, *inter alia*, that Petitioner fails to demonstrate sufficiently that a person of

ordinary skill in the art would have modified Yoshida in view of Ahn to provide the ledges recited in step [1i]. PO Resp. 64–70. For the reasons explained below, Petitioner has not established by a preponderance of the evidence that claims 1–3 would have been obvious over Yoshida and Ahn.

1. Claim 1

Petitioner asserts Yoshida discloses the preamble and steps [1a]–[1e] for the same reasons set forth above in Ground 4. Pet. 99 (citing Pet. §§ X.B.1–X.B.6). Petitioner further asserts that Yoshida and Ahn render obvious steps [1f]–[1i] and that combining Yoshida’s method with Ahn’s single mask process would result in the structure depicted in modified Figure 1 of Yoshida, reproduced below. Pet. 99–105.

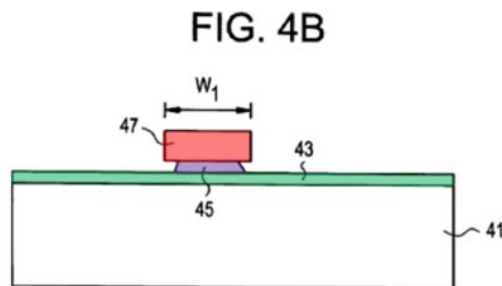
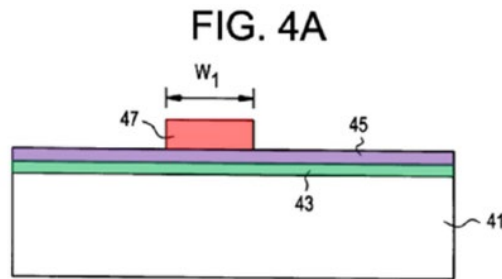


Yoshida, Fig. 1 (modified).

Petitioner’s “Modified Yoshida Figure 1” above depicts the structure that Petitioner asserts would result by combining Yoshida’s techniques with Ahn’s single mask process. Pet. 103–401 (citing Ex. 1010, 5:55–6:36, 7:7–46; Pet. § XI.A.2 [Pet. 97–99]; Ex. 1003 ¶ 259; Ex. 1006, Fig. 1).

Petitioner asserts that it would have been obvious to make Yoshida's gate structure using Ahn's approach of a single photomask over the gate metal to self-align the p-type gate material, improve symmetry, and reduce masking steps. Pet. 95, 99–100 (citing Pet. § XI.A.2 [Pet. 97–99]; Ex. 1010, 5:55–62, 6:27–37, 7:16–46, Figs. 4A–4C; Ex. 1003 ¶¶ 241–244, 252–254). Petitioner explains that Ahn teaches multiple ways to obtain Yoshida's gate structure, including etching both layers (1) simultaneously or (2) sequentially using a combination of wet and dry techniques. Pet. 98 (citing Ex. 1010, 3:41–58, 6:15–26, 7:7–14–46 [sic], Figs. 4A–C; Ex. 1003 ¶ 243). Petitioner contends that a POSITA would have found the combination a simple substitution of Ahn's known methods that would be predictably implemented when making Yoshida's device to improve alignment and symmetry between layers. Pet. 99 (citing Ex. 1003 ¶ 244).

With respect to forming a photoresist over the gate metal as recited in limitation [1f], Petitioner asserts that Ahn forms photoresist 47 over top the gate metal before etching, as shown in Ahn Figures 4A and 4B below.



Ahn, Figs. 4A-4B.

Ahn Figures 4A and 4B depict steps in the process for fabricating thin-film transistors having first metal layer 43 and second metal layer 45. Ex. 1010, 5:38–45.

With respect to limitation [1g], which requires “etching the gate metal and p-type metal,” Petitioner again states that Ahn’s single-mask technique teaches etching its top layer gate metal and underlying layer and that it would have been obvious and predictable to make Yoshida’s gate structure with Ahn’s single photomask etching approach. *See* Pet. 100–101 (citing Pet. § IX.A.2 [Pet. 97–99]; Ex. 1010, 5:55–6:36, 7:7–46; Ex. 1003 ¶ 254).

With respect to limitation [1h], which states that etching the p-type gate material forms p-type gate material side surfaces that “extend horizontally toward the source contact and drain contact,” respectively, and contact the barrier layer, Petitioner asserts that Yoshida alone teaches or suggests this limitation because it has at least slightly sloping sidewalls and very few structures, if any, have vertical sidewalls in practice. Pet. 101

(citing Ex. 1003 ¶ 526; Ex. 1007 ¶ 42; Ex. 1020 (“Uemoto”), Figs. 1–2, 5; Pet. § X.B.9). Petitioner further asserts that it would have been obvious to use Ahn’s single mask process to differentially etch multiple metal layers to obtain a narrower gate contact and ledges in stacked structure, with improved reproducibility, precision, and symmetry. *See, e.g.*, Pet. 101 (citing Ex. 1010, 5:55–6:36, 7:7–46; Pet. § XI.A.2; Ex. 1003 ¶¶ 241–244, 257).

With respect to limitation [1i], which requires etching the gate metal to form a pair of ledges on the p-type gate material below the gate material, Petitioner asserts that Ahn etches its top layer gate metal under a photoresist such that it is narrower than the underlayer layer to form a pair of ledges on either side of the top metal. Pet. 102 (citing Ex. 1010, 5:55–6:36, 7:7–46, Figs. 4A–4C; Ex. 1003 ¶ 258; Pet. § XI.A.2 [Pet. 97–99]). Petitioner asserts that Ahn teaches etching both layers by either etching both layers simultaneously or by etching them sequentially using combinations of wet and dry techniques. Pet. 98 (citing Ex. 1010 code (57), 3:41–58, 6:15–26, 7:7-14-46 [sic]; Ex. 1003 ¶ 244).

Patent Owner makes a number of arguments in response, including that Petitioner has not sufficiently shown that a POSITA would have formed ledges on Yoshida using the self-aligned process of Ahn. *See* Resp. 64. Patent Owner asserts that, for the same reasons set forth for ground 4 above, Petitioner has not shown any reason a POSITA would perform the additional, costly etching steps necessary in step [1i] to form the ledges because Petitioner has not shown any reason to form ledges other than hindsight. Resp. 64–69. Patent Owner also asserts that Petitioner has not shown that a POSITA would have understood that Yoshida’s layer 5 would

have a slower rate of dissolution than its metallic gate layer, and thus has not provided a sufficient “articulated reason” on the complex interactions of any known etching material with Yoshida’s metal and p-GaN layer to support Petitioner’s proposed modification based on the “specific relative etching rates.” Resp. 70

In its Reply, Petitioner asserts Ahn discloses a two-step process of (1) dry etching both layers under a single mask and (2) wet etching to undercut the top layer and that this method is independent of specific materials. Reply 26–27 (citing Ex. 1010, 7:7–14; Ex. 1003 ¶¶ 242–243; Pet. 98). Petitioner also responds to other Patent Owner arguments that we did not address. *See* Reply 26–28.

For reasons similar to those set forth in Section II.H.1 above, we agree with Patent Owner that Petitioner has not shown a sufficient reason a POSITA would have performed Ahn’s wet etching step to undercut Yoshida’s gate layer after dry etching both layers other than hindsight to achieve the structure shown in the ’347 patent. Petitioner’s statement that using Ahn’s wet etch to “predicably preserve the cap layer’s side walls” assumes that a POSITA would want to perform a second etching step and that a POSITA would have chosen the wet etch to preserve the side walls. Petitioner, however, does not explain *why* a POSITA would have wanted to perform the second etch to undercut the gate layer, other than to create ledges. As noted in Section II.H.1 above, Patent Owner persuasively explains, and Petitioner does not rebut, that Yoshida teaches having a wider p-type GaN layer than gate layer simply to ensure that the gate electrode can be deposited on the GaN layer without overhang. Resp. 58 (citing Ex. 1005 ¶ 259). Yoshida does not disclose any operational function of the illustrated

ledges after the gate electrode is loaded. Resp. 59. Thus, Petitioner has not shown why a POSITA would have performed Ahn's additional etching steps to form the claimed ledges when the ledges have no disclosed operational function after Yoshida's gate metal G is loaded on the p-GaN layer 5. Resp. 60. Thus, Petitioner has not shown any reason to undercut Yoshida's gate metal G to provide ledges, which would add manufacturing cost and steps, and produce a less efficient method, when there is no teaching as to any advantages of the ledges.

As such, Petitioner fails to show a sufficient reason a POSITA would have modified Yoshida in view of Ahn and, thus, does not demonstrate by a preponderance of the evidence that claim 1 would have been obvious over Yoshida and Ahn.

2. *Claim 2–3*

Petitioner also asserts that claims 2–3, which depend from claim 1, would have been obvious over Yoshida and Ahn. Pet. 104–106. None of Petitioner's contentions regarding claims 2 and 3 remedy the deficiencies set forth above. Thus, Petitioner has not established by a preponderance of the evidence that claims 2–3 would have been obvious over Yoshida and Ahn.

III. CONCLUSION

After reviewing the complete record developed during the course of the trial, we conclude that Petitioner has not satisfied its burden of demonstrating by a preponderance of the evidence that claims 1–3 of the '347 patent are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3	103(a)	Saxler, Beach, Shenoy		1–3
1–3	103(a)	Saxler, Yoshida, Beach, Shenoy		1–3
1–3	103(a)	Saxler, Ahn		1–3
1–3	103(a)	Yoshida, Saxler, Beach, Shenoy		1–3
1–3	103(a)	Yoshida, Ahn		1–3
Overall Outcome				1–3

IV. ORDER

For the reasons given, it is:

ORDERED that, Petitioner not established by a preponderance of evidence that claims 1–3 of the '347 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2023-01382
Patent 9,748,347 B2

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