

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.
AND INNOSCIENCE AMERICA, INC.,
Petitioner

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01383
Patent No. 8,404,508

PETITION FOR *INTER PARTES* REVIEW

TABLE OF CONTENTS

I.	PRELIMINARY STATEMENT	1
II.	TECHNOLOGY BACKGROUND.....	2
	A. GaN Transistors.....	2
	B. Fabrication of GaN Transistors with Photo Masks	4
	C. Self-Aligned Gate and P-GaN Layer	5
III.	THE '508 PATENT	6
IV.	Claim Construction.....	10
V.	STATEMENT OF PRECISE RELIEF REQUESTED	10
	A. Prior Art.....	10
	B. Challenges	11
VI.	LEVEL OF ORDINARY SKILL IN THE ART	11
VII.	STATEMENT OF FACTS	11
VIII.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	13
	A. Ground 1: Claims 1-3 Are Obvious over <i>Yoshida</i> , <i>Beach</i> , and <i>Sheppard</i>	13
	1. Overview of the Combination.....	13
	a. <i>Yoshida</i>	13
	b. <i>Beach</i>	15
	c. <i>Sheppard</i>	18
	d. Motivation to Combine <i>Yoshida</i> , <i>Sheppard</i> , and <i>Beach</i>	18
	2. Claim 1	25

a.	[1pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”	25
b.	[1a]: “nucleating and growing transition layers on a substrate;”	25
c.	[1b]: “growing an III Nitride EPI layer over the transistor [sic] layers;”	27
d.	[1c]: “growing an III Nitride barrier layer over the EPI layer;”	28
e.	[1d]: “growing a GaN layer with acceptor type dopants over the barrier layer;”	29
f.	[1e]:	30
g.	[1f]:	34
h.	[1g]:	35
3.	[Claim 2] “wherein the EPI layer is comprised of InAlGaN.”	39
4.	[Claim 3] “wherein the barrier layer is comprised of InAlGaN with a larger band gap than the buffer layer.”	40
B.	Ground 2: Claims 1-4 Are Obvious over <i>Hikita-347</i> , <i>Beach</i> , and <i>Sheppard</i>	42
1.	Overview of the Combination	42
a.	<i>Hikita-347</i>	43
b.	<i>Beach</i>	46
c.	<i>Sheppard</i>	46
d.	Motivation to Combine <i>Hikita-347</i> , <i>Sheppard</i> , and <i>Beach</i>	47
2.	Claim 1	51

a.	[1pre].....	51
b.	[1a].....	52
c.	[1b].....	54
d.	[1c].....	54
e.	[1d].....	55
f.	[1e].....	56
g.	[1f]	58
h.	[1g].....	60
3.	Claim 2.....	61
4.	Claim 3	64
5.	Claim 4.....	66
a.	[4pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”	66
b.	[4a]: “nucleating and growing transition layers on a substrate;”	66
c.	[4b]: “growing an InAlGa _N EPI layer over the transistor layers;”	66
d.	[4c]: “growing an InAlGa _N barrier layer over the InAlGa _N EPI layer;”	67
e.	[4d]: “growing an InAlGa _N layer with acceptor type dopants over the InAlGa _N barrier layer;”	68
f.	[4e]: “growing a GaN layer with acceptor type dopants over the doped InAlGa _N layer;”	70
g.	[4f]:	71
h.	[4g]:.....	73

i.	[4h]:.....	74
C.	Ground 3: Claim 5 Is Obvious over <i>Hikita-023</i> , <i>Beach</i> , and <i>Sheppard</i>	74
1.	Overview of the Combination.....	74
a.	<i>Hikita-023</i>	75
b.	<i>Beach</i>	76
c.	<i>Sheppard</i>	76
d.	Motivation to Combine <i>Hikita-023</i> , <i>Sheppard</i> , and <i>Beach</i>	77
2.	Claim 5	78
a.	[5pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”	78
b.	[5a]: “nucleating and growing transition layers on a substrate;”	79
c.	[5b]: “growing an InAlGaN EPI layer over the transistor layers;”	81
d.	[5c]: “growing an AlGaN barrier layer over the InAlGaN EPI layer;”	82
e.	[5d]: “growing an AlGaN layer with acceptor type dopants over the AlGaN barrier layer;”	82
f.	[5e]: “growing a GaN layer with acceptor type dopants over the doped AlGaN layer;”	83
g.	[5f]:	84
h.	[5g]:.....	86
i.	[5h]:.....	88
j.	[5i]:.....	89

IX.	DISCRETIONARY DENIAL IS NOT WARRANTED.....	90
A.	<i>Fintiv</i> Denial Is Improper	90
B.	35 U.S.C. § 325(d) Denial Is Improper	90
X.	MANDATORY NOTICES	92
A.	Real Party-in-Interest	92
B.	Related Matters.....	92
C.	Lead and Backup Counsel, and Service Information.....	92
XI.	GROUND FOR STANDING.....	94
XII.	CONCLUSION.....	95

PETITIONER’S EXHIBIT LIST

Exhibit	Description
Ex. 1001	U.S. Patent No. 8,404,508 to Lidow et al. (“the ’508 patent”)
Ex. 1002	Prosecution History of the ’508 patent (downloaded from Public PAIR)
Ex. 1003	Declaration of Dr. James Richard Shealy, Ph.D. (“Shealy”)
Ex. 1004	Japanese Patent Application Publication No. JPH11261053A to Yoshida, published September 24, 1999 (“ <i>Yoshida</i> ”), including certified English translation and certification
Ex. 1005	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 (“ <i>Beach</i> ”)
Ex. 1006	U.S. Patent No. 7,238,560 to Sheppard et al., published July 3, 2007 (“ <i>Sheppard</i> ”)
Ex. 1007	U.S. Patent Application Publication No. 2006/0273347 to Hikita et al., published December 7, 2006 (“ <i>Hikita-347</i> ”)
Ex. 1008	U.S. Patent Application Publication No. 2008/0079023 to Hikita et al., published April 3, 2008 (“ <i>Hikita-023</i> ”)
Ex. 1009	U.S. Patent Application Publication No. 2007/0007547 to Beach, published January 11, 2007 (“ <i>Beach-547</i> ”)
Ex. 1010	X. Hu et al., “Enhancement mode AlGa _N /Ga _N HFET with selectively grown <i>pn</i> junction gate,” Electronics Letters, vol. 36, no. 8, April 2000, pp. 753-754 (“ <i>Hu</i> ”)
Ex. 1011	Excerpts from Sorab K. Ghandhi, “VLSI Fabrication Principles” (2d ed. 1994) (“ <i>Ghandhi</i> ”)
Ex. 1012	C. S. Suh et al., “p-Ga _N /AlGa _N /Ga _N Enhancement-Mode HEMTs,” 2006 64th Device Research Conference, June 2006, pp. 163-164 (“ <i>Suh</i> ”)
Ex. 1013	Japanese Patent Application Publication No. JP 2007-066979A to Iwatani et al., published March 15, 2007 (“ <i>Iwatani</i> ”), including certified English translation and certification
Ex. 1014	S.-H. Jang et al., “High-quality Ga _N /Si(111) epitaxial layers grown with various Al _{0.3} Ga _{0.7} N/Ga _N superlattices as intermediate layer by MOCVD,” Journal of Crystal Growth, vol. 253, nos. 1-4, June 2003, pp. 64-70 (“ <i>Jang</i> ”)
Ex. 1015	E. Feltin et al., “Crack-Free Thick Ga _N Layers on Silicon (111) by Metalorganic Vapor Phase Epitaxy,” Physical Status Solidi A., vol. 188, no. 2, November 2001, pp. 531-535 (“ <i>Feltin</i> ”)

Exhibit	Description
Ex. 1016	U.S. Patent No. 5,223,724 to Green, published June 29, 1993 (“ <i>Green</i> ”)
Ex. 1017	U.S. Patent No. 6,211,000 to Spikes et al., published April 3, 2001 (“ <i>Spikes</i> ”)
Ex. 1018	U.S. Patent No. 5,225,360 to Shim et al., published July 6, 1993 (“ <i>Shim</i> ”)
Ex. 1019	U.S. Patent Application Publication No. 2005/0133818 to Johnson et al., published June 23, 2005 (“ <i>Johnson</i> ”)
Ex. 1020	U.S. Patent Application Publication No. 2007/0228416 to Chen et al., published October 4, 2007 (“ <i>Chen</i> ”)
Ex. 1021	M. Shimizu et al., “p-Type InGaN Cap Layer for Normally Off Operation in AlGaN/GaN Heterojunction Field Effect Transistors,” Japanese Journal of Applied Physics, vol. 47, no. 4, April 2008, pp. 2817-2819 (“ <i>Shimizu</i> ”)
Ex. 1022	U.S. Patent Application Publication No. 2009/0042344 to Ye et al., published February 12, 2009 (“ <i>Ye</i> ”)
Ex. 1023	U.S. Patent No. 6,316,793 to Sheppard et al., published November 13, 2001 (“ <i>Sheppard-793</i> ”)
Ex. 1024	U.S. Patent Application Publication No. 2008/0073652 to Sugimoto et al., published March 27, 2008 (“ <i>Sugimoto</i> ”)
Ex. 1025	C.-F. Zhu et al., “Effects of Rapid Thermal Annealing on the Structural Properties of GaN Thin Films,” IEEE Transactions on Electron Devices, vol. 48, no. 6, June 2001, pp. 1225-1230 (“ <i>Zhu</i> ”)
Ex. 1026	Excerpts from Stephen A. Campbell, “The Science and Engineering of Microelectronic Fabrication” (2d ed. 1994) (“ <i>Campbell</i> ”)
Ex. 1027	A.R. Woll et al., “GaN Nucleation and Growth on Sapphire (0001): Incorporation and Interlayer Transport,” Physical Review Letters, vol. 83, no. 21, November 1999, pp. 4349-4352 (“ <i>Woll</i> ”)
Ex. 1028	J.A. Smart et al., “AlGaN/GaN heterostructures on insulating AlGaN nucleation layers,” Applied Physics Letters, vol. 75, no. 3, July 1999, pp. 388-390 (“ <i>Smart</i> ”)
Ex. 1029	Y. Liu et al., “Demonstration of undoped quaternary AlInGaN/GaN heterostructure field-effect transistor on sapphire substrate,” Applied Physics Letters, vol. 86, May 2005, 223510 (“ <i>Liu</i> ”)
Ex. 1030	O. Ambacher et al., “Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures,” Journal of Physics: Condensed Matter, vol. 14, March 2002, 3399-3434 (“ <i>Ambacher</i> ”)

Exhibit	Description
Ex. 1031	Taiwanese Patent Application Publication No. TW200414540 A to Sheu et al., published August 1, 2004 (“ <i>Sheu</i> ”), including certified English translation and certification
Ex. 1032	Japanese Patent Application Publication No. JP 2007109830A to Mizutani et al., published April 26, 2007 (“ <i>Mizutani</i> ”), including certified English translation and certification
Ex. 1033	U.S. Patent No. 6,897,514 to Kouznetsov et al., published May 24, 2005 (“ <i>Kouznetsov</i> ”)
Ex. 1034	U.S. Patent Application Publication No. 2006/0006500 to Piner et al., published January 12, 2006 (“ <i>Piner</i> ”)
Ex. 1035	V. Kumar et al., “Field-Plated 0.25- μ m Gate-Length AlGaIn/GaN HEMTs With Varying Field-Plate Length,” IEEE Transactions on Electron Devices, vol. 53, no. 6, June 2006, pp. 1477-1480 (“ <i>Kumar</i> ”)
Ex. 1036	W. Saito et al. “Design and Demonstration of High Breakdown Voltage GaN High Electron Mobility Transistor (HEMT) Using Field Plate Structure for Power Electronics Applications,” Japanese Journal of Applied Physics, vol. 43, no. 4B, April 2004, pp. 2239-2242 (“ <i>Saito</i> ”)
Ex. 1037	U.S. Patent Application Publication No. 2006/0060895 to Hikita et al., published March 23, 2006 (“ <i>Hikita-895</i> ”)

I. PRELIMINARY STATEMENT

Petitioner requests *inter partes* review of U.S. Patent No. 8,404,508 and cancellation of claims 1-5.

All challenged claims are methods of forming enhancement mode Gallium Nitride (GaN) transistors, a well-known device. The '508 patent seeks to avoid using “two separate photo masks” to define the gate metal and the p-type GaN (or p-type AlGaN) material underneath the gate metal, respectively, explaining its disadvantages include high gate charge and increased manufacturing costs, which makes a self-aligned gate desirable. Ex. 1001, 1:65-2:18. The '508 patent's solution: pattern and etch both materials “using a single photo mask” so these layers are “automatically self-aligned.” *Id.*, 4:6-9, 4:41-44, 3:1-6. A single mask process purportedly “reduces manufacturing cost” and “minimiz[es] gate charge.” *Id.*, 4:6-11, 4:55-59.

But this single mask process was far from new. Not only was it a well-known technique, it was publicly disclosed in the GaN context by the second named inventor, Robert Beach, years earlier. *Beach* (Ex. 1005).

The transistor structures the '508 patent constructs were also not new, as the applicants themselves admit. Ex. 1001, 1:32-64. And the art applied here discloses semiconductor devices including the various claimed layers.

Because *Yoshida*, *Hikita-347*, or *Hikita-023* in combination with *Beach* and *Sheppard* render claims 1-5 obvious, the Board should institute and cancel all challenged claims.

II. TECHNOLOGY BACKGROUND

A. GaN Transistors

GaN was used in semiconductor transistor devices long before the earliest claimed priority date of the '508 patent, April 8, 2009.¹ Ex. 1003 (“Shealy”), ¶48. GaN is a III Nitride (III-N) material, a class of semiconductors that combine a group III element (e.g., indium or gallium) with nitride. Shealy, ¶48; Ex. 1001, 3:24-25 (“A III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$.”). It was well known that GaN material exhibits a large band gap. Consequently, GaN transistors have a higher breakdown voltage, making them attractive for high-power applications. Shealy, ¶48; Ex. 1001, 1:22-26 (background); *Hikita-347*, [0004].

It was also common to form layers of different materials on a substrate to produce a GaN transistor that has high electron mobility, often referred to as high electron mobility transistors (HEMT) or heterojunction field effect transistors

¹ Petitioner reserves the right to challenge the priority date here and/or in other proceedings.

(HFET). Shealy, ¶49; *Hikita-347*, [0004]; Ex. 1001, 1:22-42 (background). For example, an **AlGa****N**/**GaN** heterostructure was widely used to form HEMT devices before the '508 patent:

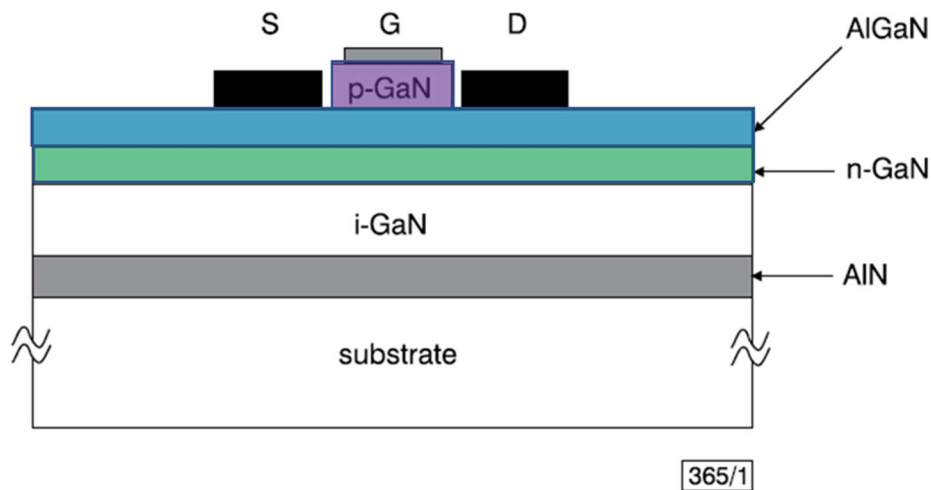


Fig. 1 *Schematic diagram of structure of pn junction regrown gate HFET*

Hu, Fig. 1.²

An “enhancement mode” GaN transistor is normally off. Shealy, ¶50; *Hikita-023*, [0006]. As shown above, an enhancement mode GaN transistor includes a p-type GaN (**p-GaN**) layer under the gate, so no drain current flows unless a gate voltage is applied. Shealy, ¶50; *Hu*, Fig. 1; *Hikita-023*, [0007]-[0008]. Such enhancement mode GaN transistors were known long before the '508 patent. Shealy, ¶50; *Hu*, 1-2. Indeed, the '508 patent itself admits all this was known. *Infra*, §III.

² All figures in this Petition containing color are annotated.

B. Fabrication of GaN Transistors with Photo Masks

Photo masks had been used to control physical dimensions and patterns of structures when manufacturing a semiconductor device for decades before the '508 patent. Shealy, ¶51.

The conventional masking process involves three steps:

1. A **mask**, or photo resistant pattern, is formed on a semiconductor structure. The **mask** may have openings on the surface.
2. The structure is etched to remove parts of the material not covered by the mask.
3. The mask is removed.

Shealy, ¶¶52-55; *Ghandhi*, 10-12, Figure 10.6(e)-(g); *Campbell*, 4, 5, Fig. 1.5(5).

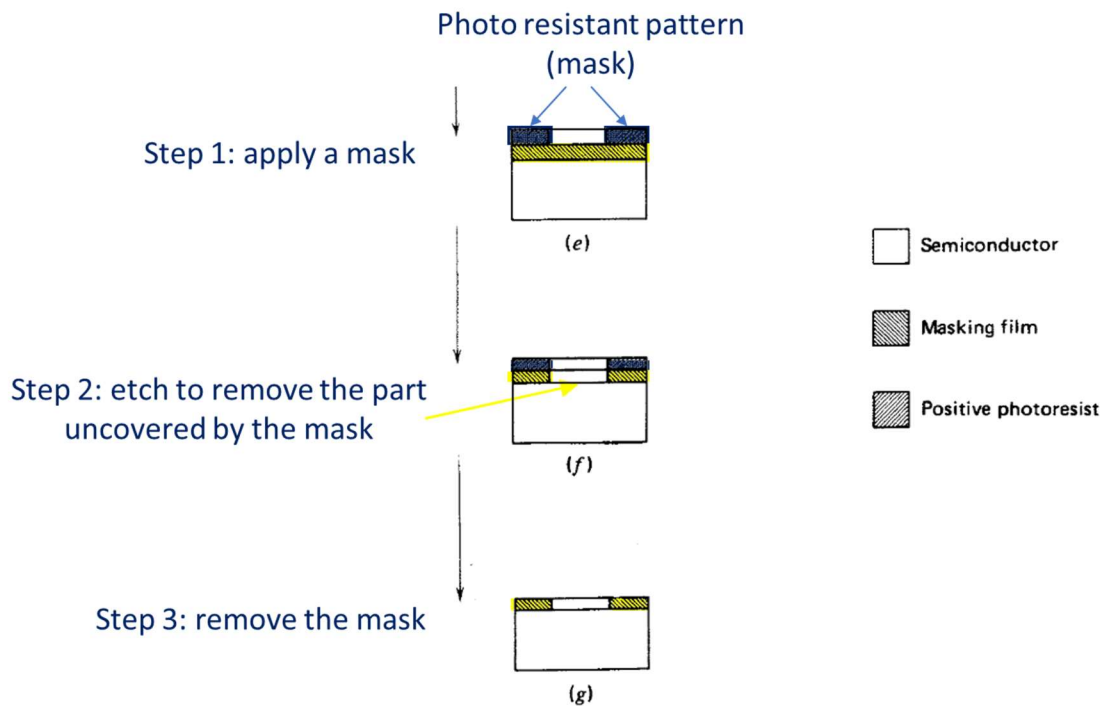


Fig. 10.6 Steps in opening a window in a masking film, using positive photoresist.

Ghandhi, Fig. 10.6(e)-(g).

The same masking process was used to form GaN transistors years before the '508 patent, including to form the ohmic contact, the doped GaN layer, and the gate contact. Shealy, ¶56; *Yoshida*, [0022]-[0023]; *Sheppard*, 8:55-63, 9:26-34; *Beach*, [0047].

C. Self-Aligned Gate and P-GaN Layer

In forming GaN transistors, self-aligned gate processes were desirable to align structures and avoid the cost of applying a second mask. Shealy, ¶57. GaN transistors with self-aligned gate and p-GaN layer were well known. The gate and

p-GaN layer could be perfectly aligned by using the gate as a mask to etch the p-GaN layer. Shealy, ¶57; *Suh*, 1; *Iwatani*, Fig. 4.

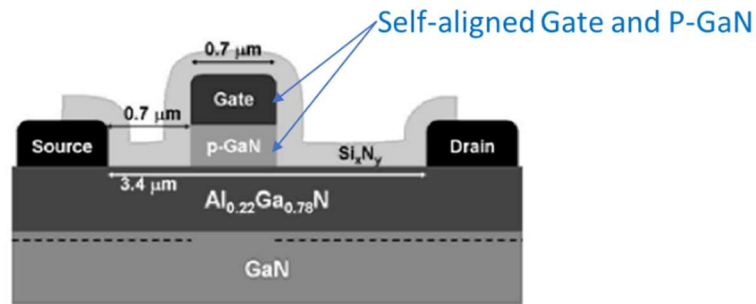
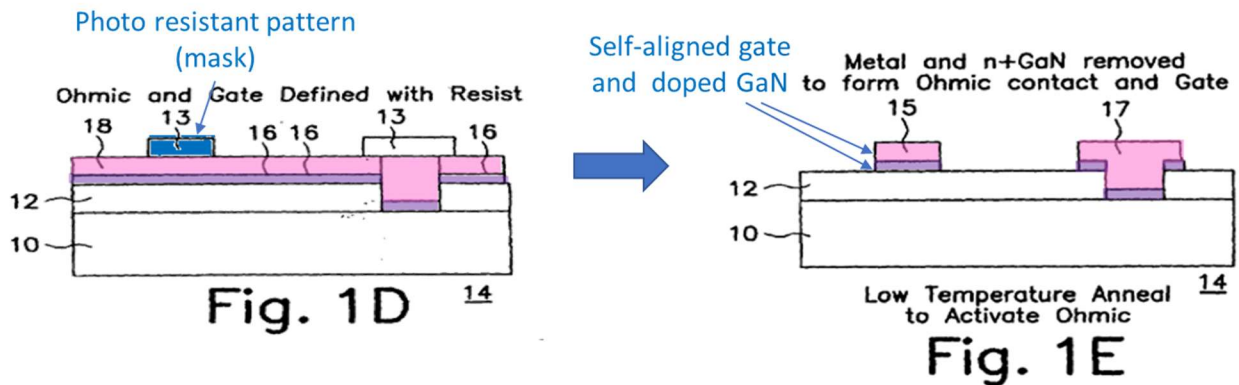


Fig. 1: Schematic cross section of the p-GaN/AlGaIn/GaN E-mode HEMT.

Suh, Fig. 1.

Using a single mask to etch the gate and doped GaN materials was also known. Shealy, ¶58; *Beach*, [0047].

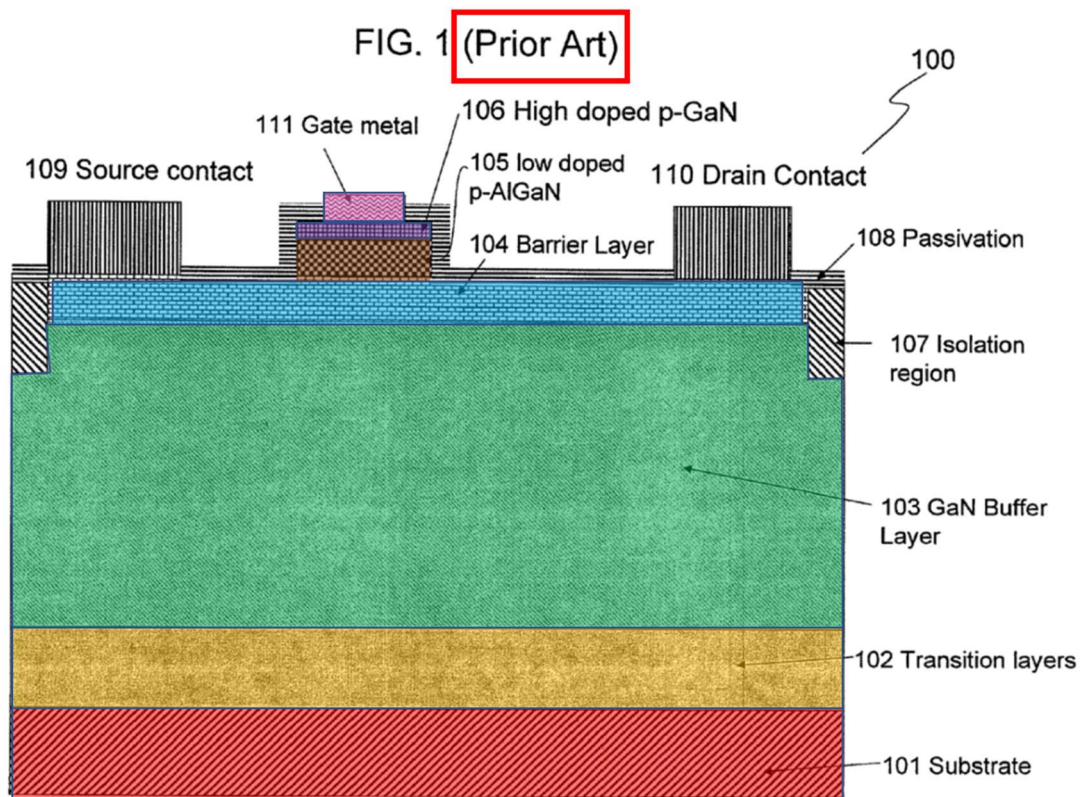


Beach, Figs. 1D, 1E.

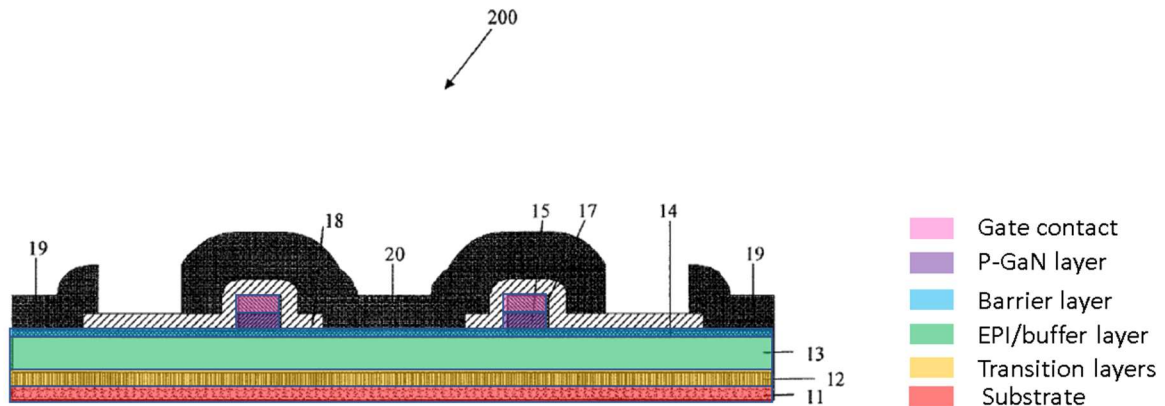
III. THE '508 PATENT

The '508 patent is directed to “[a]n enhancement-mode GaN transistor and a method of forming it.” Ex. 1001, Abstract.

The '508 patent admits that all the various layers grown on a substrate to form an enhanced mode GaN transistor in all of its embodiments were “conventional” and known in the “prior art,” including the **substrate**, **transition layers**, **GaN buffer layer**, **AlGaN barrier layer**, **p-type GaN layer**, the optional **p-type AlGaN layer**, as well as the source and drain contact and the **gate metal** formed on the device. *Id.*, 1:32-64. Compare the “prior art” Figure 1 with embodiment in Figure 2 shown below.

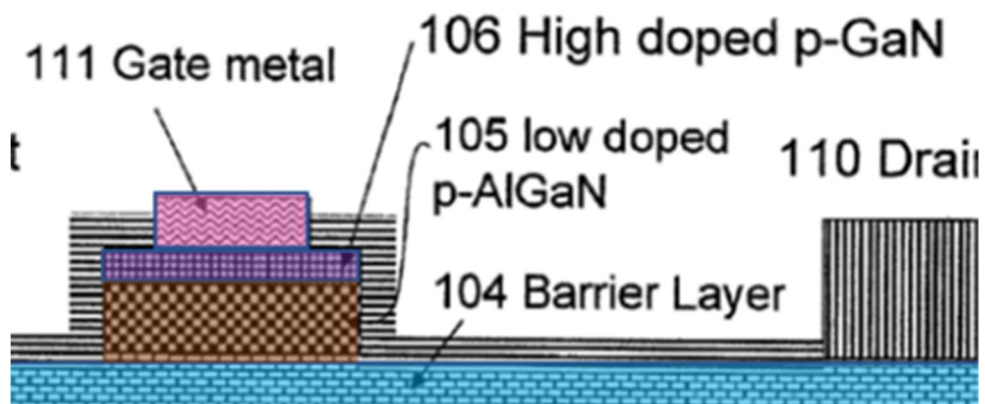


Ex. 1001, Fig. 1.



Ex. 1001, Fig. 2.

The embodiments in Figures 4 and 6 differ from Figure 2 by adding an additional layer of **p-type AlGa_N material** below the **p-type Ga_N layer**. Ex. 1001, 4:25-27, 4:61-64, Figs. 4, 6. But this additional structure was also admittedly prior art. *Id.*, 1:55-64, Fig. 1. Compare:



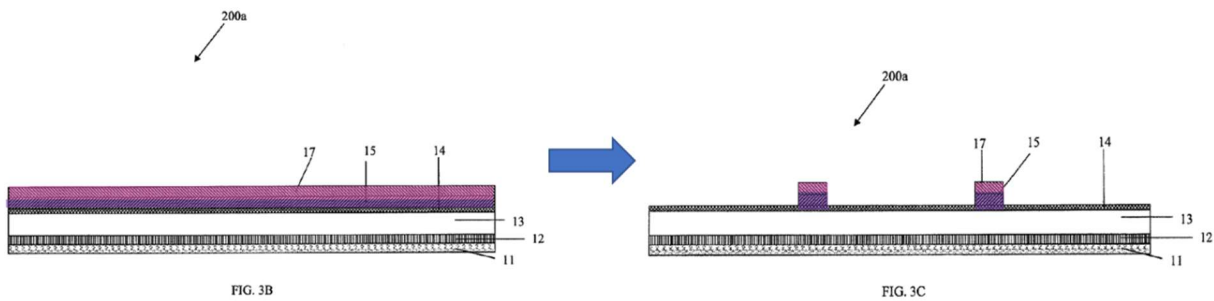
Ex. 1001, Fig. 1. (Prior art, cropped)



Ex. 1001, Figs. 4, 6 (cropped).

The '508 patent explains that, in the conventional enhancement mode GaN transistor, the **gate metal 111** and the **p-type GaN 106** or **p-type AlGaN 105** material underneath the gate metal are defined by “two different photo masks,” where the **first mask** is used to form the **p-type GaN 106** or **p-type AlGaN 105**, and the **second mask** is used to form the **gate metal 111**. Ex. 1001, 1:53-57, 1:65-2:5, Fig. 1.

The '508 patent's “invention” is to instead pattern and etch the gate metal and p-type GaN (and AlGaN) materials “using a single photo mask.” *Id.*, 3:1-6. Figure 3B shows **gate metal 17** and **p-type GaN layer 15** before the single photo mask is applied, and Figure 3C shows the structure after using the single photo mask to etch both layers. *Id.*, 3:39-50; *see also* 4:28-59, Figs. 5B-5C (etching gate metal, p-type GaN, and p-type AlGaN with one mask), 4:60-5:22, Figs. 7B-7D (etching gate metal and p-type GaN with one mask, and p-type AlGaN with a second mask to extend beyond the gate region).



Ex. 1001, Figs. 3B, 3C.

But both the “single mask” process and the resultant enhancement mode GaN transistor structure were already taught by the prior art applied in this Petition.

IV. Claim Construction

Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction.

V. STATEMENT OF PRECISE RELIEF REQUESTED

A. Prior Art

Exhibit	Patent No.	Publication Date	Prior Art Basis
1004	JPH11261053A (“Yoshida”)	September 24, 1999	§ 102(b) ³
1005	WO 2005/057624 (“Beach”)	June 23, 2005	§ 102(b)
1006	U.S. 7,238,560 (“Sheppard”)	July 3, 2007	§ 102(b)

³ Pre-AIA law applies.

1007	U.S. 2006/0273347 (“ <i>Hikita-347</i> ”)	December 7, 2006	§ 102(b)
1008	U.S. 2008/0079023 (“ <i>Hikita-023</i> ”)	April 3, 2008	§ 102(b)

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103	<i>Yoshida, Beach, and Sheppard</i>
2	1-4	§ 103	<i>Hikita-347, Beach, and Sheppard</i>
3	5	§ 103	<i>Hikita-023, Beach, and Sheppard</i>

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (POSITA) would have had at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa. Shealy, ¶69.

VII. STATEMENT OF FACTS

Pursuant to 37 C.F.R. § 42.22(c), the following statement of facts sets forth the state of GaN transistors at the time of the ’508 patent:

1. Enhancement mode GaN transistor is a normally-off GaN transistor.
2. P-type dopants are acceptor type dopants.
3. Before April 8, 2009, the following were known:
 - a. nucleating and growing transition layers on a substrate;
 - b. growing a III Nitride EPI layer over the transition layers;
 - c. growing a III Nitride barrier layer over the EPI layer;
 - d. growing a GaN layer with acceptor type dopants over the barrier layer;
 - e. depositing a gate contact layer on the doped GaN layer;
 - f. applying a gate photo resistant pattern;
 - g. etching away the gate contact layer outside the gate region;
 - h. etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
 - i. removing the gate photo resistant pattern;
 - j. depositing a dielectric layer;
 - k. applying a contact photo resistant pattern;
 - l. etching the dielectric layer to open the drain and source contact area;
 - m. removing the contact photo resistant pattern;
 - n. depositing an ohmic contact metal;
 - o. applying a metal photo resistant pattern;

- p. etching the ohmic contact metal;
- q. removing the metal photo resistant pattern; and
- r. performing rapid thermal annealing to form ohmic drain and source contacts.

VIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

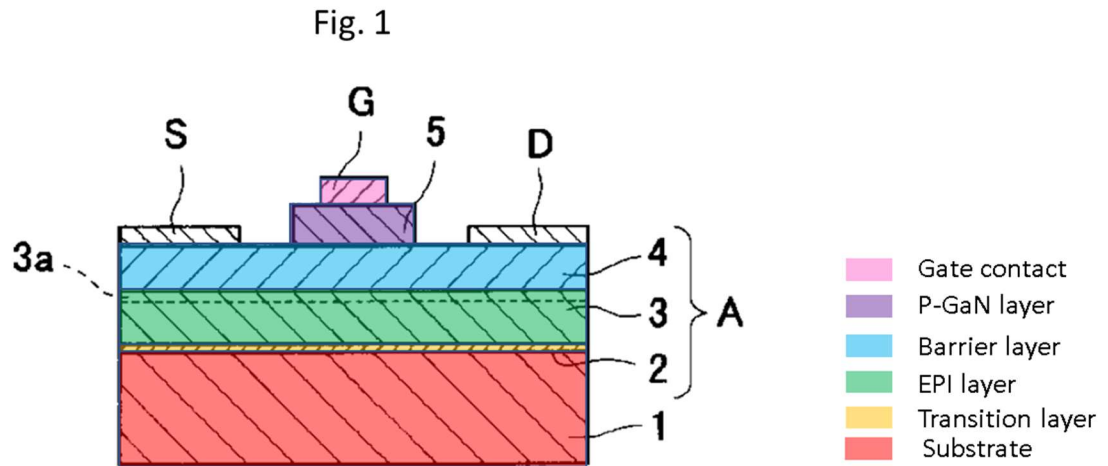
A. Ground 1: Claims 1-3 Are Obvious over *Yoshida*, *Beach*, and *Sheppard*

1. Overview of the Combination

Yoshida discloses growing various layers to form the device in claim 1 ([1pre]-[1d]), and the masking steps to open the drain and source contact area ([1f]). *Yoshida* does not explicitly disclose forming multiple transition layers in [1a]—but *Shepard* does. *Yoshida* also does not explicitly disclose the masking steps to etch the gate metal and p-GaN layer ([1e]) and the masking steps to form the ohmic drain and source contacts ([1g])—but *Beach* does. Together, *Yoshida*, *Sheppard*, and *Beach* render claims 1-3 obvious.

a. *Yoshida*

Like the '508 patent, *Yoshida* discloses a GaN HEMT. Compare *Yoshida*, [0001], [0009], [0010], [0019]-[0023], with Ex. 1001, 1:14-18, 3:10-4:5:



Yoshida, Fig. 1.

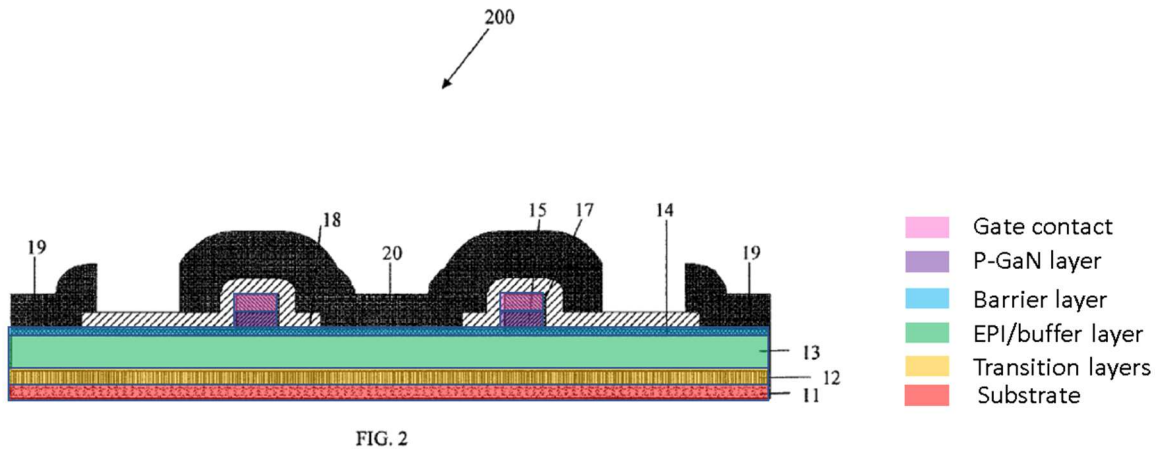


FIG. 2

Ex. 1001, Fig. 2.

Yoshida discloses how to form this GaN HEMT:

1. grow layers 2-5 over the **substrate 1** in this order;
2. etch away the **p-GaN layer** except where the **gate** is to be loaded;
3. deposit a dielectric layer to cover the entire surface;

4. apply a mask, open the source and drain contact area in the dielectric layer;
5. deposit the source and drain electrodes on the “exposed” **n-type AlGaN layer**;⁴
6. remove the mask and form the **gate contact** above the **p-GaN layer** to produce an enhancement mode GaN transistor.

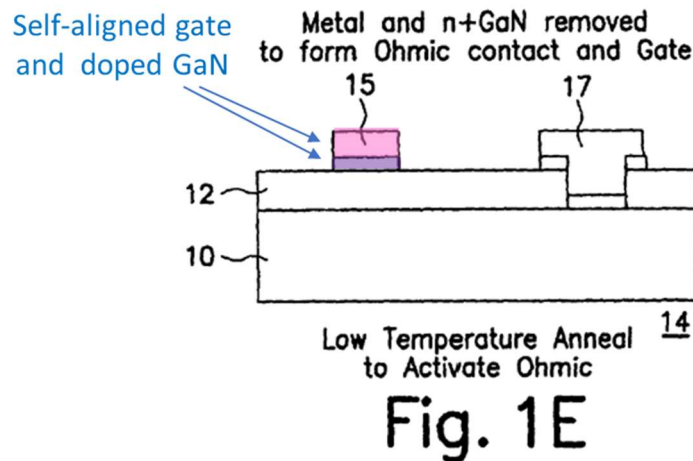
Yoshida, [0013], [0021]-[0023]; Shealy, ¶74.

b. *Beach*

Like the '508 patent, *Beach* discloses a GaN HEMT and uses masks to produce such a device. *Compare Beach*, [0004], [0024], [0040]-[0049], [0062], with Ex. 1001, 1:14-18, 3:10-4:5.

Beach discloses a GaN transistor with a self-aligned **gate contact 15** and **doped GaN layer** stack. *Beach*, [0047]-[0048]; Shealy, ¶77. The depicted GaN transistor also includes an AlGaN barrier layer 12 and a GaN buffer layer 10 to form an HEMT. *Beach*, [0004], [0039]-[0041]; Shealy, ¶77.

⁴ While *Yoshida* specifies “n-type AlGaN is favorable,” it also refers to InGaN for this layer. *Yoshida*, [0013].

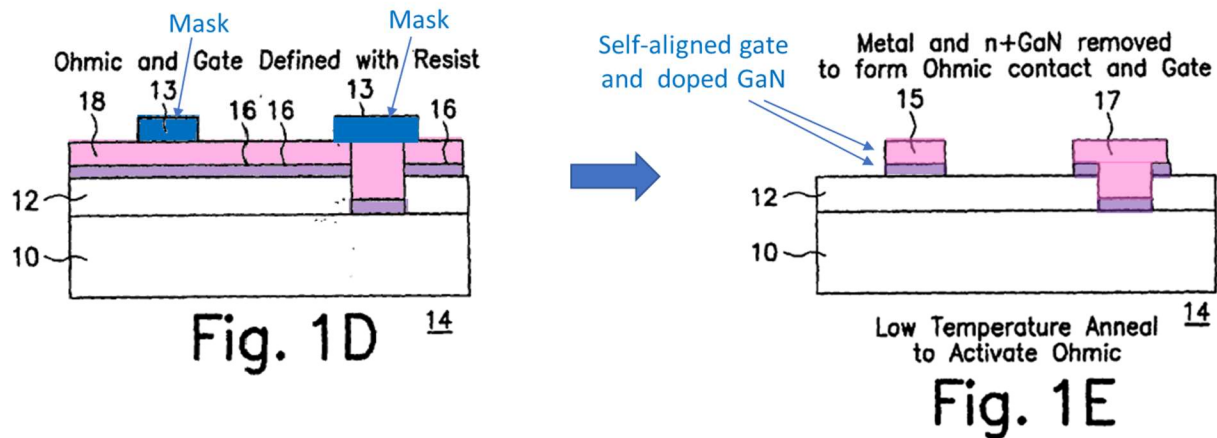


Beach, Fig. 1E.

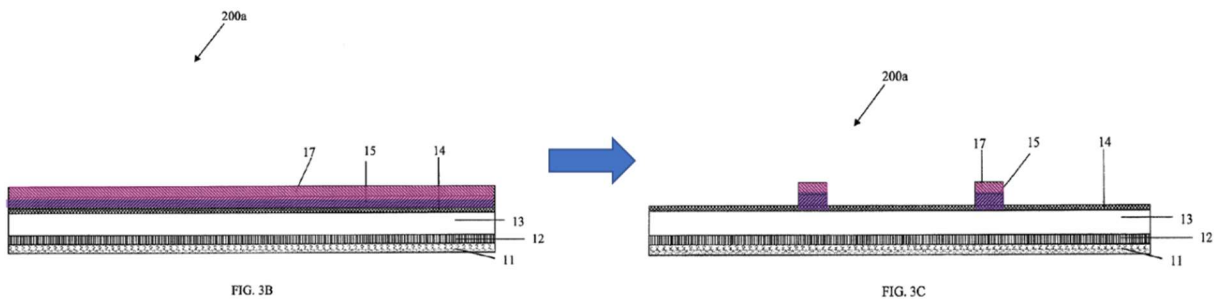
Beach discloses how to form the self-aligned gate and doped GaN stack:

1. grow **doped GaN layer 16**;
2. deposit **ohmic material 18** over it;
3. apply a **photo resistant pattern (mask) 13**;
4. etch the **ohmic material 18** and **doped GaN layer 16** using the **mask**;
5. remove the **mask**.

Beach, [0043]-[0045], [0047], [0049]. This is the same process claimed in the '508 patent. Compare:



Beach, Figs. 1D, 1E.



Ex. 1001, Figs. 3B, 3C.

Beach also discloses the claimed masking process to form the drain and source contacts. Figure 1D shows applying another **photo resistant pattern (mask) 13** to form the ohmic contact 17 (source/drain contact) then etching the **ohmic material 18** away except where protected by the **photo resistant pattern (mask) 13** to form an ohmic contact 17 (source/drain contact). *Beach*, [0047]; Shealy, ¶79.

c. *Sheppard*

Like the '508 patent, *Sheppard* discloses a GaN HEMT device and a method for providing such a device. *Compare Sheppard*, 2:30-38, 8:55-9:46, with Ex. 1001, 1:14-18, 3:10-4:5. *Sheppard* discloses growing various layers of materials over a substrate to form a GaN transistor, as shown below. *Sheppard*, 6:45-8:54. *Sheppard* discloses forming multiple transition layers between substrate 10 and channel layer 20. *Sheppard*, 6:58-65, 7:25-32.

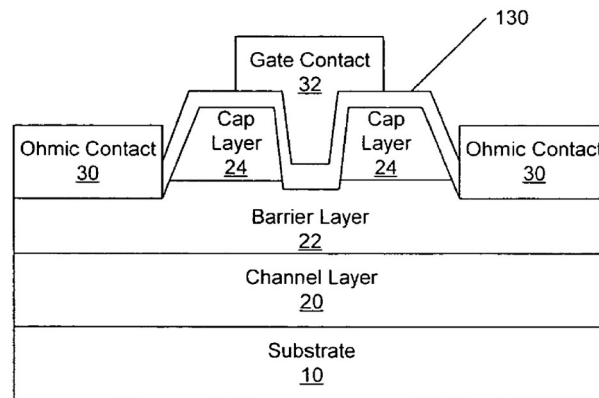


Figure 3

Sheppard, Fig. 3.

d. Motivation to Combine *Yoshida*, *Sheppard*, and *Beach*

Yoshida, *Sheppard*, and *Beach* are all directed to a GaN transistor and forming such a device using a multilayered epitaxial structure. *Yoshida*, [0009], [0019]-[0023]; *Sheppard*, 6:45-8:54; *Beach*, [0002], [0017]-[0018]. Shealy, ¶¶103,

124. A POSITA would have been motivated to modify *Yoshida* in view of *Sheppard* and *Beach*.

i. Motivation to Use *Sheppard*'s Multiple Transition Layers

Sheppard explains that providing additional transition layers on the substrate provides a benefit of strain balancing. *Sheppard*, 6:58-7:7. A POSITA would have been motivated to include multiple transition layers in *Yoshida*'s device to achieve an improved strain balancing effect, and to improve the crystalline quality of the various layers above the transition layers and reduce the crack of the materials of *Yoshida*'s device. Shealy, ¶¶103-104.

Both *Yoshida* and *Sheppard* are concerned with providing a high-quality GaN transistor and describe using silicon as a substrate material for their GaN-based devices. *Yoshida*, [0008]-[0011], [0019]; *Sheppard*, 5:58-6:7, 6:48-51, 7:19-23. A POSITA would have understood that there is a large thermal mismatch between GaN and silicon, typically causing extensive cracks in the post-growth cooling down process. Shealy, ¶104. *Yoshida* recognized this mismatch problem. *Yoshida*, [0011]. A POSITA would have recognized a single GaN transition layer, as in *Yoshida*, does not effectively release the strain resulting from the large lattice mismatch and large thermal expansion coefficient difference between GaN and silicon. Shealy, ¶104; *Jang*, 2 (explaining the difficulty to grow high-quality GaN

devices over silicon substrates due to the mismatch of the lattice constants and thermal expansion coefficients between GaN and silicon). A POSITA would have been motivated to incorporate additional transition layers, such as the AlN buffer layer and strain balancing transition layers taught by *Sheppard*, to improve the quality and reduce cracks in the growth of GaN epitaxy over silicon. Shealy, ¶104; *Feltin*, 1-2 (using AlN and GaN transition layers to achieve high-quality GaN devices); *Piner*, [0076]-[0079] (using compositionally-graded transition layers with varying composition of Aluminum to reduce crack).

A POSITA would have expected success because *Yoshida*'s device already includes a transition layer (GaN buffer layer 2), and *Yoshida* describes a method of growing the transition layer over a silicon substrate. Shealy, ¶105, *Yoshida*, [0011], [0019]. Further, the '508 patent admits that it was "conventional" to provide transition layers over a silicon substrate. Ex. 1001, 1:53-64 (background). The '508 patent does not explain how to nucleate and grow transition layers over a silicon substrate, because such process was routine, conventional, and well understood in the art. Shealy, ¶105. Providing multiple transition layers in *Yoshida*'s device would have thus required only conventional techniques in their ordinary and expected manner. *Id.*

ii. Motivation to Use *Beach*'s Single Mask Gate Process

A POSITA would have been motivated to use *Beach*'s single mask process to form the gate contact and doped GaN layer to improve *Yoshida*'s device and process in multiple ways. Shealy, ¶124.

First, *Beach*'s single mask process effectively achieves *Yoshida*'s objective of etching away the doped GaN layer except the area where the gate contact is to be loaded. Shealy, ¶125; *Yoshida*, [0022]. A POSITA would have recognized that *Beach*'s single mask process automatically achieves self-alignment between the gate contact and the doped GaN layer, improving the gate's alignment, and is thus desirable. Shealy, ¶125; *compare Beach*, Fig. 1E, *with Yoshida*, Fig. 1; *Beach*-547, [0043]-[0048] (describing self-aligned gates as advantageous); *Kouznetsov*, 3:42-61 (explaining that self-alignment decreases die size and cost).

Second, *Beach*'s single mask process is simpler. Shealy, ¶126. Compared to *Yoshida*'s process, which employs separate masks for each etching step, *Beach* uses a single mask to etch the gate and doped GaN layer, removing the additional second mask steps. *Id.*; *Beach*, [0047]. A POSITA would have understood that applying masks is a substantial undertaking during manufacturing, and the removal of any additional mask application simplifies the manufacturing process, reducing

cost. Shealy, ¶126; *Kouznetsov*, 3:55-61 (describing that uses the same photoresist mask to form the layers decreases process cost and complexity).

A POSITA would have expected success because applying a single mask to form the gate contact and doped GaN layer was a well-known and conventional technique. Shealy, ¶127. The '508 patent states that the etching of the gate contact and p-GaN layer using the same mask is performed by “any known technique,” because etching multiple layers of different materials using the same mask was routine, conventional, and well understood in the art. Ex. 1001, 3:45-50; Shealy, ¶127. Indeed, using the same mask to etch different layers of materials in semiconductor devices was known and implemented decades before the '508 patent. Shealy, ¶127; *Green*, 8:10-19 (etching the silicide layer and metal layer using a single mask), Figs. 6-7; *Spikes*, 4:39-5:3 (same), Figs. 1B-1C; *Shim*, 3:8-14 (same), Figs. 2C-2D.

Further, both *Yoshida* and *Beach*'s devices use the same GaN material for the layer underneath the gate contact, and can be etched the same way. Shealy, ¶128. To the extent EPC argues that the dopants applied to *Beach*'s GaN layer (n-type dopants in one embodiment) are not identical to the *Yoshida* dopants (p-type dopants), a POSITA would have understood that the impurities caused by the dopants are so dilute that they do not change the etching characters of the GaN material, and as a result, the same masking technique could apply. *Id.*

iii. Motivation to Use *Beach*'s Source and Drain Masking Process

A POSITA would have been motivated to use *Beach*'s masking process to form the ohmic source and drain contacts (or electrodes) to improve *Yoshida*'s device and process in multiple ways. Shealy, ¶143.

First, *Beach*'s masking process was a known-technique that effectively achieved *Yoshida*'s objective to form the source and drain electrodes. Shealy, ¶144; *Yoshida*, [0010], [0022]; *Intel Corp. v. PACT XXP Schweiz AG*, No. 22-1037, slip op. at 12-13 (Fed. Cir. Mar. 13, 2023) (under the “known-technique” rationale, the only motivation that is required to combine the references is that the solution offered by one reference be “suitable” for solving a problem of another reference). *Yoshida* does not disclose a process for forming the source and drain electrodes (ohmic source and drain contacts), and a POSITA would have appreciated that *Beach*'s masking process would produce the ohmic source and drain contacts in *Yoshida*'s transistor, allowing *Yoshida*'s transistor to perform its intended functions. Shealy, ¶144.

Second, *Beach*'s masking process is simpler compared to the alternative “lift-off” process. Shealy, ¶145. A POSITA would have understood that *Beach*'s masking process avoids manufacturing of the vertical profile of photoresist shape used in the lift-off process, thereby reducing cost. *Id.*

Third, Beach's masking process allows a source and gate connected field plate to be easily formed, which reduces electrical field at the gate corner and results in higher breakdown voltage at *Yoshida's* device. Shealy, ¶146; *Kumar*, 4; *Saito*, 1; *Hikita-895*, [0046]. Applying Beach's masking process, A POSITA could use the mask to extend the source ohmic contact region toward the gate contact, forming the plate. Shealy, ¶146. In contrast, the lift-off process requires a separate masking step to allow the source ohmic contact metal to extend beyond the designated opening, and as a result, requires additional processing to provide a field plate design. Shealy, ¶146; *Kumar*, 1; *Saito*, 2; *Hikita-895*, [0056]-[0057]. Therefore, a POSITA would have been motivated to use *Beach's* more flexible masking process to produce *Yoshida's* ohmic source and drain contacts. Shealy, ¶146.

A POSITA would have expected success because using a mask to pattern and etch ohmic metal to form source and drain contacts was a well-known and conventional technique. Shealy, ¶147. The '508 patent does not explain how to apply a mask to etch ohmic contact metal, because such process was routine, conventional, and well understood in the art. *Id.* Both *Yoshida's* and *Beach's* devices use ohmic contact metal to form source and drain contacts which could be etched with the same techniques. *Id.*; *Yoshida*, [0022], [0010] (metal Al); *Beach*, [0045] ("ohmic metal").

2. Claim 1

The combination of *Yoshida*, *Sheppard*, and *Beach* renders claim 1 obvious.

a. **[1pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”**

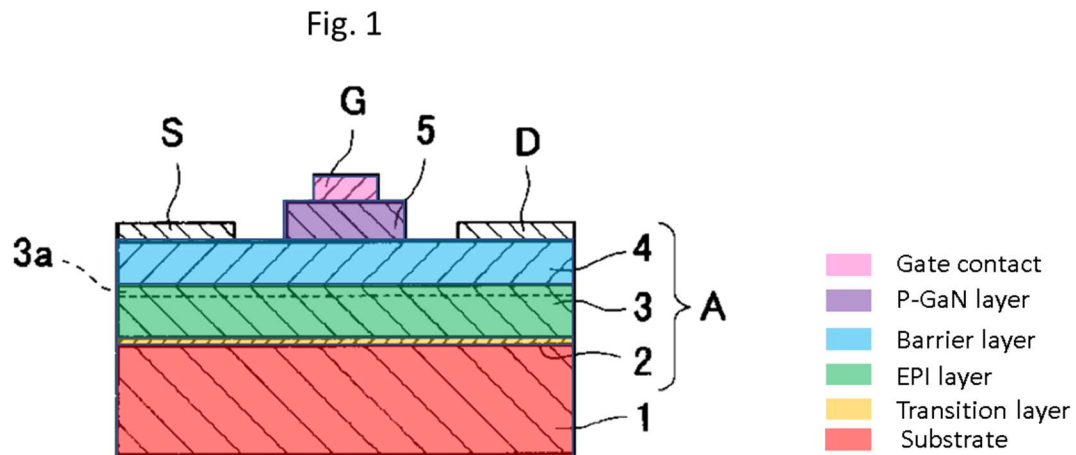
Yoshida discloses [1pre]. Shealy, ¶96.

Yoshida discloses a GaN high-mobility transistor that includes a p-type GaN layer below the gate, constituting a normally off enhancement mode GaN transistor. *Yoshida*, [0017], [0015], Fig. 1; Shealy, ¶97. *Yoshida* discloses a method of forming an enhancement mode GaN transistor, including growing epitaxial layers over a substrate and etching the p-type GaN layer with dry etching. *Yoshida*, [0019]-[0023].

b. **[1a]: “nucleating and growing transition layers on a substrate;”**

Yoshida in view of *Sheppard* renders obvious [1a]. Shealy, ¶98. *Yoshida* discloses nucleating and growing a transition layer on a substrate, and *Sheppard* discloses providing multiple transition layers on the substrate. *Id.*

Yoshida discloses growing a **GaN buffer layer 2** over a **substrate 1** (a silicon (Si) material) by epitaxial growth, as shown below. *Yoshida*, [0010]-[0011], [0019]; Shealy, ¶99.



Yoshida, Fig. 1.

GaN buffer layer 2 is a transition layer because it is an intermediate layer between the **substrate 1** and the **i-type GaN layer 3**. Shealy, ¶100; Ex. 1001, 3:26-29 (describing the **transition layers** as located above the **substrate** and underneath the **undoped GaN layer**).

Yoshida discloses applying known MOCVD and MOMBE methods to grow the transition layer (GaN buffer layer 2) on the silicon substrate. *Yoshida*, [0011], [0019]. A POSITA would have understood that growing a transition layer on a silicon substrate using the MOCVD and MOMBE methods includes an initial phase of nucleation and then growth of the transition layers. Shealy, ¶101; *Woll*, 1-2 (using MOMBE to nucleate and grow a thin GaN layer); *Smart*, 1 (growing a thin GaN nucleation layer). The '508 patent does not provide any description of the

nucleating process, confirming that nucleating a transition layer over a silicon substrate was a well-known technique to a POSITA. Shealy, ¶101.

To the extent *Yoshida* does not explicitly disclose providing multiple transition layers, *Sheppard* renders this obvious. *Sheppard* discloses a GaN transistor that includes multiple transition layers on a silicon substrate. *Sheppard*, 6:58-7:7, 7:25-32. *Sheppard* discloses providing an “AlN buffer layer” and additional “strain balancing transition layer(s)” to “provide an appropriate crystal structure transition” between the substrate and the remainder of the device. *Sheppard*, 6:58-7:7. A POSITA would have been motivated to include multiple transition layers in *Yoshida*’s device and expected success in doing so.

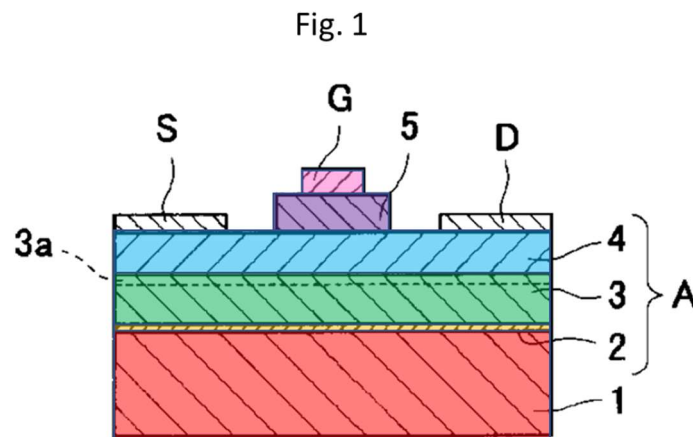
§VIII.A.1.d.i.

c. [1b]: “growing an III Nitride EPI layer over the transistor [sic] layers;”

Yoshida discloses [1b].⁵ Shealy, ¶106.

⁵ The “transistor layers” in [1b/4b/5b] lacks an antecedent basis. The ’508 patent describes a III Nitride EPI layer 13 over the transition layers 12 and does not describe any “transistor layers.” Ex. 1001, 3:26-29, Figs. 2, 3A. In this Petition, the “transistor layers” is considered as the “transition layers” in [1a/4a/5a].

Yoshida discloses growing an **i-type GaN layer 3** (or $\text{In}_x\text{Ga}_{1-x-y}\text{Al}_y\text{N}$ ($0 < x < 1$, $0 < y < 0.2$)) over the **buffer layer 2** (transition layer), as shown below. *Yoshida*, [0010], [0012], [0020].



Yoshida, Fig. 1.

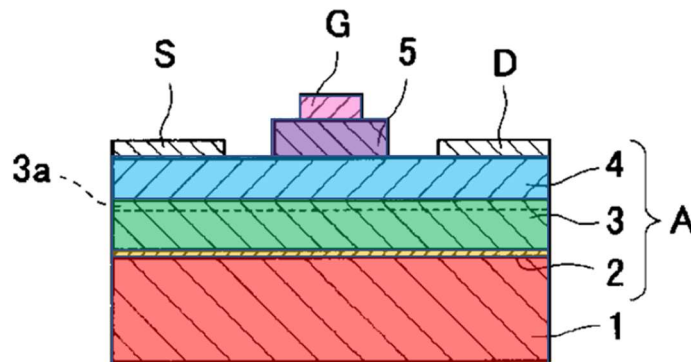
A POSITA would have understood that the **i-type GaN** or **i-type $\text{In}_x\text{Ga}_{1-x-y}\text{Al}_y\text{N}$ layer** is a III Nitride EPI layer because GaN and InAlGa_N are both III Nitride materials. Shealy, ¶108; Ex. 1001, 3:24-25, 3:26-31 (providing an “un-doped GaN buffer material” over the transition layers).

d. [1c]: “growing an III Nitride barrier layer over the EPI layer;”

Yoshida discloses [1c]. Shealy, ¶109.

Yoshida discloses growing a **n-type AlGa_N layer 4** (barrier layer) (or n-type $\text{In}_u\text{Ga}_{1-u-v}\text{Al}_v\text{N}$ ($0 < u < 1$, $0 < v < 0.5$)) over the **i-type GaN layer 3** (EPI layer), as shown below. *Yoshida*, [0013], [0021].

Fig. 1



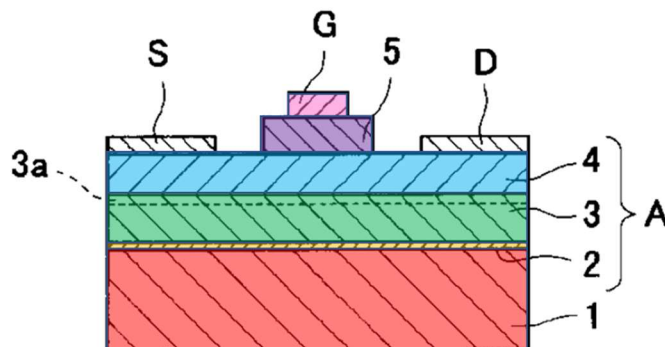
Yoshida, Fig. 1.

- e. [1d]: “growing a GaN layer with acceptor type dopants over the barrier layer;”

Yoshida discloses [1d]. Shealy, ¶112.

Yoshida discloses growing a **p-type GaN layer 5** over the **n-type AlGaN layer 4** (barrier layer), as shown below. *Yoshida*, [0009], [0015], [0021]. *Yoshida* discloses that metal Mg or cyclopentadienyl magnesium are examples of a p-type dopant. *Yoshida*, [0015].

Fig. 1



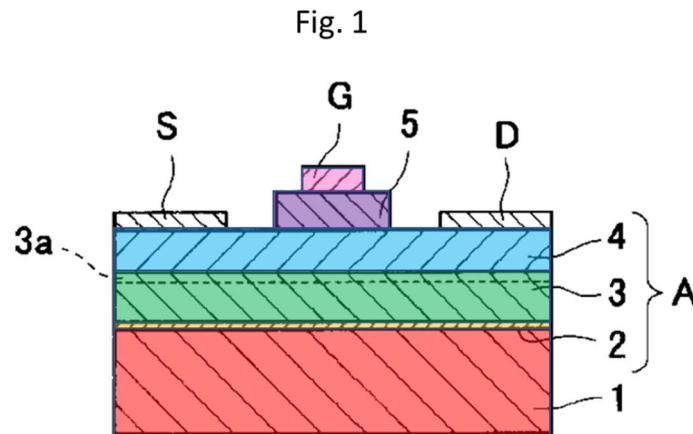
Yoshida, Fig. 1.

A POSITA would have understood that the p-type dopants in the **p-type GaN layer** are acceptor-type dopants. Shealy, ¶114. The '508 patent confirms that p-type dopants are acceptor-type dopants. Ex. 1001, 6:24-28 (explaining that p-type dopants are “acceptor-rich”), 3:26-31 (providing a “p-type GaN gate layer” over the AlGaN barrier layer).

- f. [1e]:
- “[1e1] depositing a gate contact layer on the doped GaN layer;
 - [1e2] applying a gate photo resistant pattern;
 - [1e3] etching away the gate contact layer outside the gate region;
 - [1e4] etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
 - [1e5] removing the gate photo resistant pattern;”

Yoshida in view of *Beach* renders obvious [1e]. Shealy, ¶115. *Yoshida* discloses etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact ([1e4]), and *Beach* renders obvious all steps in element [1e]. *Id.*

Yoshida discloses forming a **gate electrode G** (gate contact) over the **p-GaN layer 5**, as shown below. *Yoshida*, [0009], [0016], [0023].



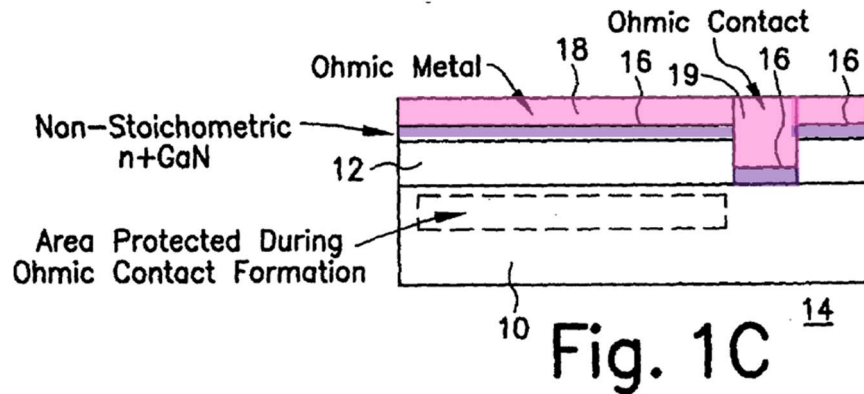
Yoshida, Fig. 1.

Yoshida discloses that, to form the p-GaN layer and gate contact, the p-GaN layer was etched away “except where the gate electrode was to be loaded.” *Yoshida*, [0022]. Then the gate electrode is loaded above the p-GaN layer. *Yoshida*, [0023]. Although Figure 1 shows that the p-GaN layer 5 extends beyond the gate contact, *Yoshida* discloses in the description that the p-GaN layer 5 is etched away “except where the gate electrode was to be loaded.” *Yoshida*, [0022]; Shealy, ¶117.

Yoshida does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the p-GaN layer and gate contact layer, nor does Figure 1 show a p-GaN layer and gate electrode of the same width, but *Beach* renders this obvious. Shealy, ¶118.

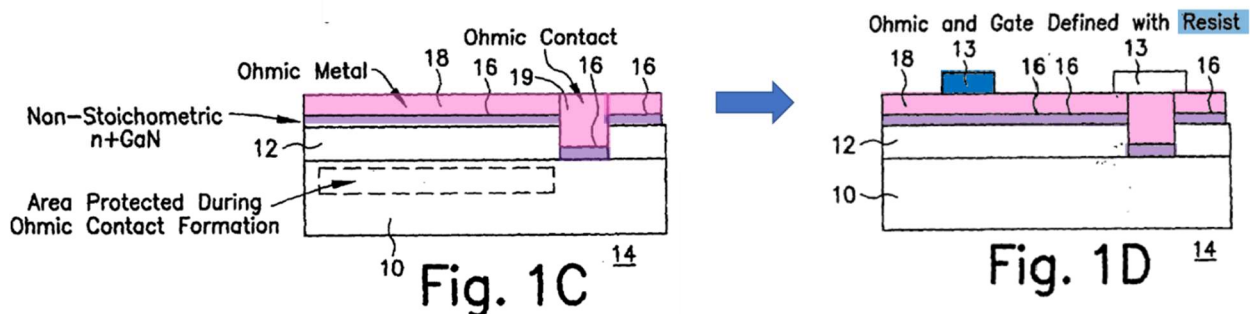
Beach discloses a method of forming a self-aligned gate and doped GaN layer using the steps of element [1e]. First, *Beach* discloses element [1e1], i.e.,

depositing an **ohmic material 18** (gate contact layer) on the **doped GaN layer 16**, as shown below. *Beach*, [0045] (“Material 18 [is] deposited over layer 16”).



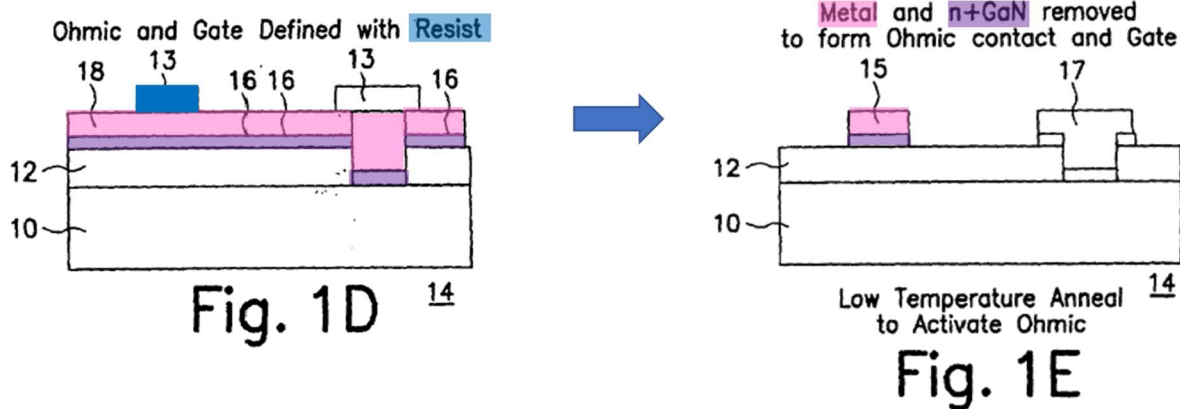
Beach, Fig. 1C.

Second, *Beach* discloses step [1e2], i.e., applying a **gate photo resistant pattern 13** (mask) to the structure, as shown below. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17”).



Beach, Figs. 1C, 1D.

Third, *Beach* discloses step [1e3], i.e., etching away the **gate contact layer** outside the gate region, and step [1e4], i.e., etching away the **doped GaN layer**, except a portion of the doped GaN layer beneath the gate contact, as shown below. *Beach*, [0047] (“After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.”).



Beach, Figs. 1D, 1E.

Fourth, *Beach* discloses step [1e5], i.e., removing the gate photo resistant pattern (mask). *Beach*, [0049] (“After material 18 has been removed from device 14 in regions not covered by photoresist 13, photoresist 13 is stripped off”); *Beach*, Fig. 1E (showing the photoresist 13 being removed).

A POSITA would have been motivated to apply *Beach*’s single mask process to form *Yoshida*’s device and expected success in doing so. §VIII.A.1.d.ii.

- g. [1f]:
- “[1f1] depositing a dielectric layer;
 - [1f2] applying a contact photo resistant pattern;
 - [1f3] etching the dielectric layer to open the drain and source contact area;
 - [1f4] removing the contact photo resistant pattern;”

Yoshida discloses [1f]. Shealy, ¶130.

First, *Yoshida* discloses that, after etching away the p-type GaN layer, “[a]n SiO₂ film was then deposited by plasma CVD to cover the entire surface.” *Yoshida*, [0022]. A POSITA would have understood that SiO₂ (silicon dioxide) is a material that has excellent dielectric properties and is commonly used as the dielectric material for semiconductor devices. Shealy, ¶131.

Second, *Yoshida* discloses “patterning [the SiO₂ film] with photoresist,” such that the portion the gate contact is “masked” and the portion to load the source and drain contacts are left “open.” *Yoshida*, [0022].

Third, *Yoshida* discloses the layer underneath the SiO₂ film (dielectric layer) is “exposed” to “load source electrode S and drain electrode D” after applying the photoresist pattern (mask). *Yoshida*, [0022]. A POSITA would have understood that the SiO₂ film (dielectric layer) in *Yoshida*’s device is etched to leave open the drain and source contact area because (1) the SiO₂ film (dielectric layer) is initially deposited to “cover the entire surface”; and (2) after applying the mask, the portion

of SiO₂ film (dielectric layer) covering the source and drain contact area are etched, such that the portion of layer underneath the SiO₂ film (dielectric layer) is exposed for loading the source and drain contacts “***on*** the exposed n-type InGaN [or AlGaN] layer 4.” Shealy, ¶133; *Yoshida*, [0013], [0021]-[0022] (emphasis added).

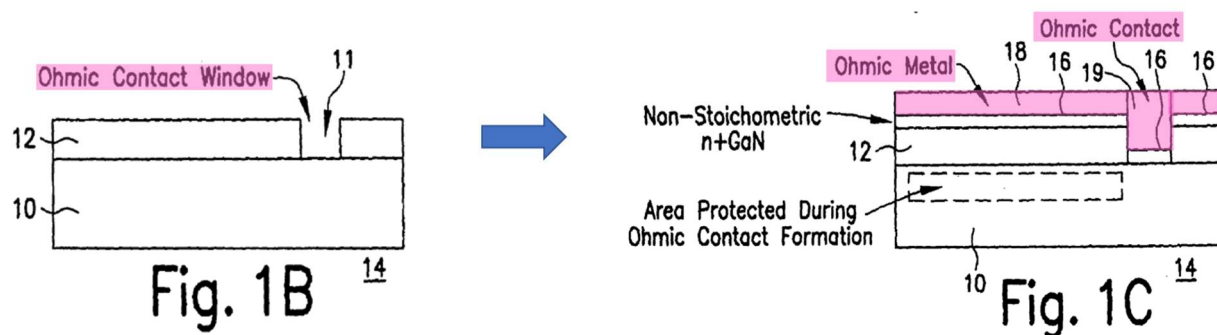
Fourth, *Yoshida* discloses “etching away the masking” after opening the source and drain contact area. *Yoshida*, [0023]. A POSITA would have also understood that, in semiconductor manufacturing, the masks used to pattern and form the device are to be removed because the masks are only tools to construct the device and not part of the device. Shealy, ¶134; *Ghandhi*, 12 (describing the “final step” of the masking process is “removal of the exposed photoresist”).

- h. [1g]:**
- “[1g1] depositing an Ohmic contact metal;**
[1g2] applying a metal photo resistant pattern;
[1g3] etching the Ohmic contact metal;
[1g4] removing the metal photo resistant pattern; and
[1g5] performing rapid thermal annealing to form
Ohmic drain and source contacts.”

Yoshida in view of *Beach* renders obvious [1g]. Shealy, ¶135. *Yoshida* discloses depositing metal Al (ohmic contact metal) on the n-type semiconductor layer 4 to load source electrode S and drain electrode D (ohmic source and drain contacts). *Yoshida*, [0022], [0010]; Shealy, ¶135.

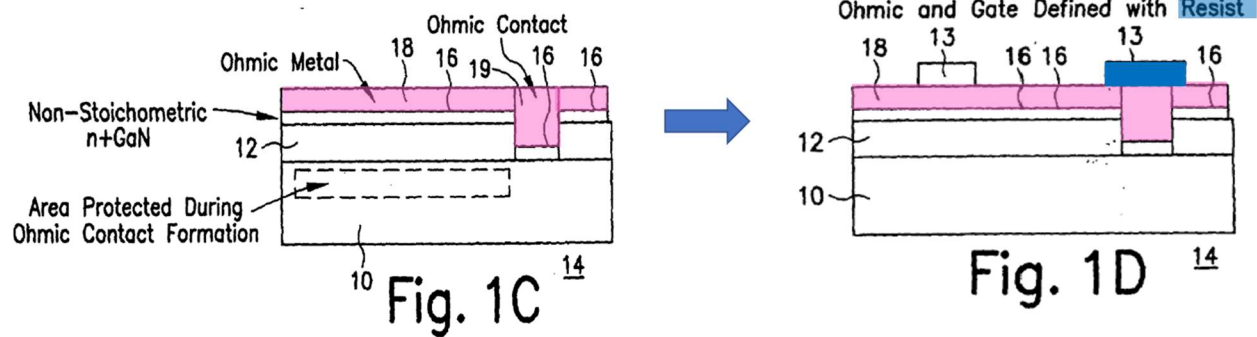
Yoshida does not explicitly disclose a process for forming the source and drain electrodes (ohmic source and drain contacts), but *Beach* renders obvious using the remaining steps in [1g] to form *Yoshida*'s ohmic source and drain contacts. Shealy, ¶136; *Yoshida*, [0010], [0022]; *Beach*, [0045]-[0047].

First, *Beach* discloses that an **ohmic contact metal 18** is deposited in ohmic contact window 11. *Beach*, [0045] (“Material 18 deposited over layer 16 and in ohmic contact window 11 ... may be an ohmic metal”).



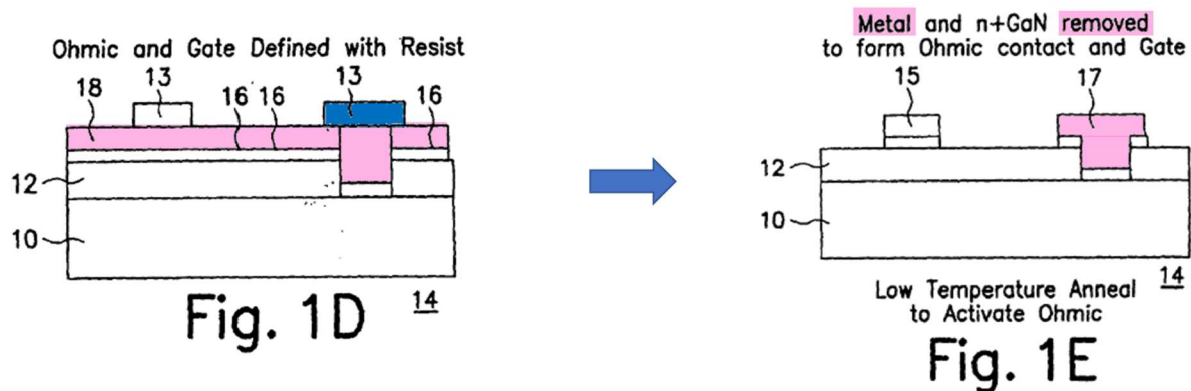
Beach, Figs. 1B, 1C.

Second, *Beach* discloses that a **metal photo resistant pattern 13 (mask)** is applied over the **ohmic contact metal 18**. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17.”).



Beach, Figs. 1C, 1D.

Third, *Beach* discloses that the **ohmic contact metal 18** is etched except the portion protected by the **mask**. *Beach*, [0047] (“After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13.”).



Beach, Figs. 1D, 1E.

Fourth, *Beach* discloses that the **mask** is removed. *Beach*, [0049] (“After material 18 has been removed from device 14 in regions not covered by photoresist 13, photoresist 13 is stripped off”).

Fifth, *Beach* discloses that thermal annealing is performed to form the source and drain contacts. *Beach*, [0049] (“The temperatures in the anneal step are below about 850°C, and preferably about 600°C. The low temperature anneal step activates ohmic contact 17.”), [0054] (“an anneal step is performed to activate ohmic contact 26, and the presence of protective layer 22 permits the anneal to take place at a lower temperature, such as 850°C, or preferably 600°C.”), Abstract (forming device contacts with “high temperature processing”). To the extent EPC argues that *Beach* does not explicitly disclose rapid thermal annealing, a POSITA would have found that *Beach* renders it obvious to perform rapid thermal annealing to form ohmic source and drain contacts in *Beach*’s and *Yoshida*’s devices (step [1g5]). Shealy, ¶141.

A POSITA would have been motivated to perform rapid thermal annealing instead of conventional furnace annealing to activate ohmic contacts because it was well known that rapid thermal annealing reduces thermal budget, lowers manufacturing cost, and increases production throughput of the semiconductor devices. Shealy, ¶141; *Campbell*, 6 (rapid thermal processing was developed to minimize the thermal budget); *Ye*, [0061] (performing RTA (rapid thermal annealing) at 500°C for 30 seconds to form source and drain ohmic contacts); *Hu*, 1 (performing RTA at 850°C for 1 minute to form source-drain contacts). A POSITA would have been motivated to perform rapid thermal annealing to activate

ohmic contacts because it was known to improve the structural and electronic properties of GaN materials, as well as providing a smoother surface of the contact, which improves circuit yield. Shealy, ¶141; *Zhu*, 5; *Campbell*, 9.

A POSITA would have had a reasonable expectation of success in performing rapid thermal annealing to activate ohmic contacts. Shealy, ¶141. Such technique was routine long before the '508 patent was filed and was commonly adopted in GaN semiconductor manufacturing to form a low-resistance ohmic contact in an efficient manner. *Id.*; *Johnson*, [0085] (performing rapid thermal annealing to form source-drain contacts); *Hu*, 1 (same); *Chen*, [0087] (same); *Shimizu*, 1 (same); *Ye*, [0061] (same). Therefore, it would have been obvious to perform rapid thermal annealing to activate the ohmic contacts in *Beach*'s and *Yoshida*'s devices. Shealy, ¶141.

A POSITA would have been motivated to apply *Beach*'s masking process to form *Yoshida*'s ohmic source and drain contacts and expected success in doing so. §VIII.A.1.d.iii.

3. [Claim 2] “wherein the EPI layer is comprised of InAlGaN.”

Yoshida discloses claim 2. Shealy, ¶148. As explained in [1b], *Yoshida* discloses that the EPI layer barrier layer is comprised of i-type $\text{In}_x\text{Ga}_{1-x-y}\text{Al}_y\text{N}$ ($0 < x < 1$, $0 < y < 0.2$). *Yoshida*, [0012]; §VIII.A.2.c.

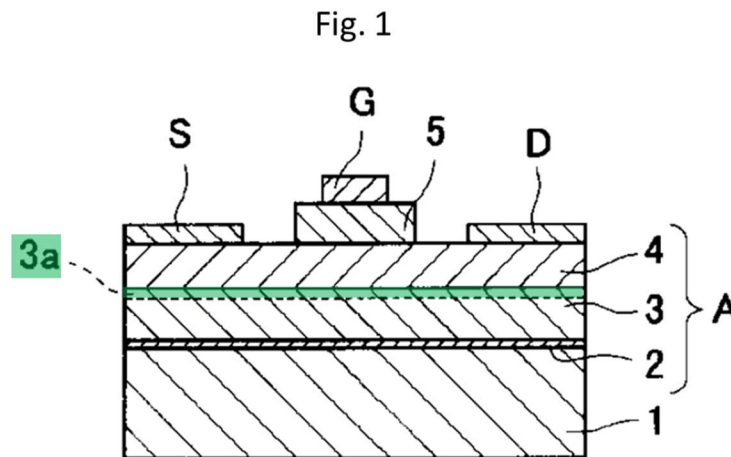
4. [Claim 3] “wherein the barrier layer is comprised of InAlGaN with a larger band gap than the buffer layer.”

Yoshida renders obvious claim 3.⁶ Shealy, ¶149.

As explained in [1c], *Yoshida* discloses that the barrier layer is comprised of n-type $\text{In}_u\text{Ga}_{1-u-v}\text{Al}_v\text{N}$ ($0 < u < 1$, $0 < v < 0.5$). *Yoshida*, [0013]; §VIII.A.2.d.

Yoshida discloses that the barrier layer (n-type semiconductor layer 4) and the EPI layer (i-type semiconductor layer 3) form a “two-dimensional electron gas” layer at a region near the junction of the two layers, which traps the electrons supplied from the barrier layer and allows high-speed electron mobility. *Yoshida*, [0016]-[0017], [0007]. *Yoshida* explains that a two-dimensional electron gas layer 3a is formed “at the topmost portion of i-type semiconductor layer 3,” as shown below. *Yoshida*, [0016].

⁶ The “buffer layer” lacks an antecedent basis. The ’508 patent describes the “undoped GaN buffer material 13” as the layer below the barrier layer 14, and in claim 1 the “EPI layer” is the layer below the barrier layer. Ex. 1001, 3:26-29, Figs. 2, 3A. In this Petition, the “buffer layer” is considered as the “EPI layer” in claim 1.



A POSITA would have understood that the barrier layer 4 needs to have a larger band gap than the EPI layer 3, such that the electrons originating in the wider band gap barrier layer 4 transfer to the two-dimensional electron gas layer. Shealy, ¶152; *Sheppard*, 1:33-38 (“a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity.”), 8:4-6 (“The barrier layer 22 may be a Group III-nitride and has a bandgap larger than that of the channel layer 20 and a smaller electron affinity than the channel layer 20.”); *Sheppard-693*, 1:47-50 (“electrons that originate in the doped, wider-bandgap semiconductor transfer to the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering.”); *Sugimoto*, [0107]-[0109] (describing that a two-dimensional electron gas is formed by

providing an AlGaN barrier layer with a wider band gap over the GaN buffer layer with a smaller band gap). A POSITA would have found it obvious that *Yoshida*'s barrier layer 4 has a larger band gap than the EPI layer 3 to form a two-dimensional electron gas layer in order for *Yoshida*'s high-mobility transistor (HEMT) to perform its intended functions. Shealy, ¶152.

B. Ground 2: Claims 1-4 Are Obvious over *Hikita-347*, *Beach*, and *Sheppard*

1. Overview of the Combination

Hikita-347 discloses the structure of the device in claim 1, including a substrate, a transition layer, an EPI layer, a barrier layer, a p-GaN layer, gate metal, and source and drain contacts. While *Hikita-347* does not explicitly disclose forming multiple transition layers ([1a]), *Sheppard* renders this obvious.

Hikita-347 also does not explicitly disclose the three masking steps ([1e], [1f], [1g]) to form the structure in claim 1, but *Beach* and *Sheppard* disclose these masking processes. As explained in Ground 1, *Beach* discloses the masking steps to etch the gate metal and p-GaN layer ([1e]) and the masking steps to form the ohmic drain and source contacts ([1g]). *Sheppard* discloses the masking steps to open the drain and source contact area ([1f]). It would have been obvious to use *Beach*'s and *Sheppard*'s masking processes to form *Hikita-347*'s device.

Hikita-347 also discloses growing various layers to form the device in claim 4 ([4a] through [4e]). *Hikita-347* does not explicitly disclose forming multiple transition layers ([4a]), using an InAlGaN for various layers ([4b]-[4d]), or the masking steps ([4f], [4g], [4h]) to form *Hikita-347*'s device.

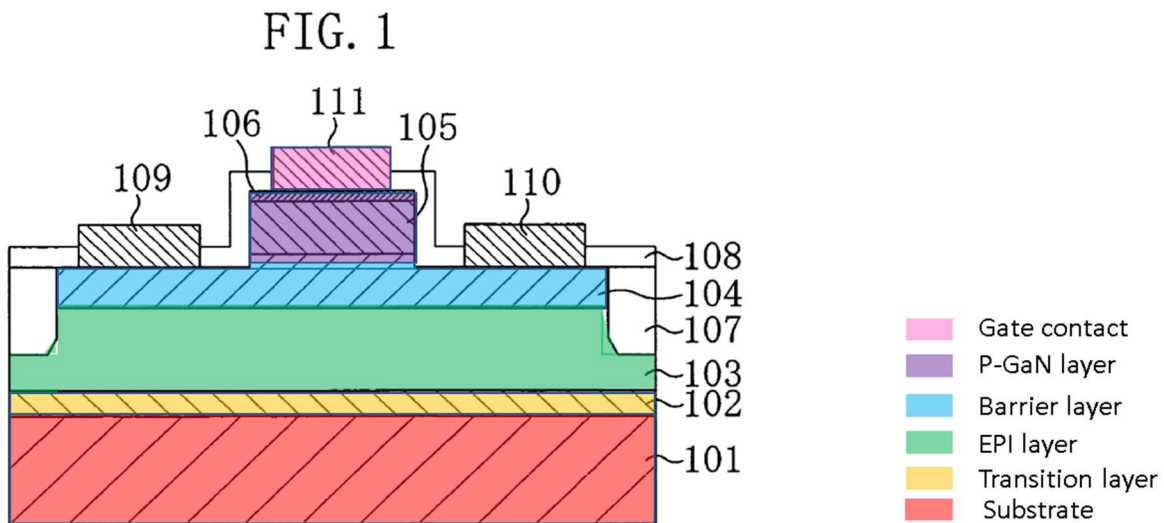
A POSITA would have found it obvious to form a p-type InAlGaN layer as the first p-type layer in *Hikita-347* ([4d]). *Sheppard* renders obvious forming multiple transition layers on a substrate ([4a]), using InAlGaN as a material for the EPI layer and barrier layer ([4b], [4c]), and the masking steps ([4g]) to open the drain and source contact area. And *Beach* renders obvious the masking steps to etch the gate metal and p-type GaN-based layers ([4f]) and the masking steps to form the ohmic drain and source contacts ([4h]).

a. *Hikita-347*

Like the '508 patent, *Hikita-347* discloses a GaN HEMT device and a method for providing such a device. Compare *Hikita-347*, [0013], [0033], [0038], [0040], [0055]-[0061], with Ex. 1001, 1:14-18, 3:10-4:5. *Hikita-347* discloses an enhancement mode GaN transistor that includes a **substrate 101**, a **buffer layer 102**, an **undoped GaN layer 103**, an **undoped AlGaN layer 104**, and a **p-type GaN layer 105**, a **gate contact 111**, and source and drain contacts 109 and 110—the same layers claimed by the '508 patent, with the sole exception being *Hikita-347*'s single depicted buffer layer 102, rather than multiple transition layers.

Hikita-347, Abstract, [0033]-[0035]. Although Figure 1 shows a second p-type GaN layer 106 over the p-type GaN layer 105, *Hikita-347* notes that it is not necessary to provide the second p-type GaN layer 106. *Hikita-347*, [0040].

Compare:



Hikita-347, Fig. 1.

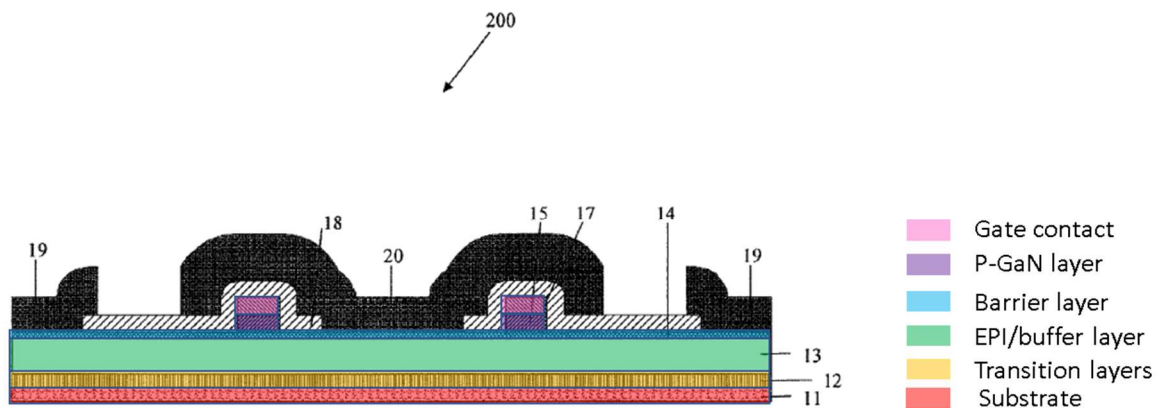
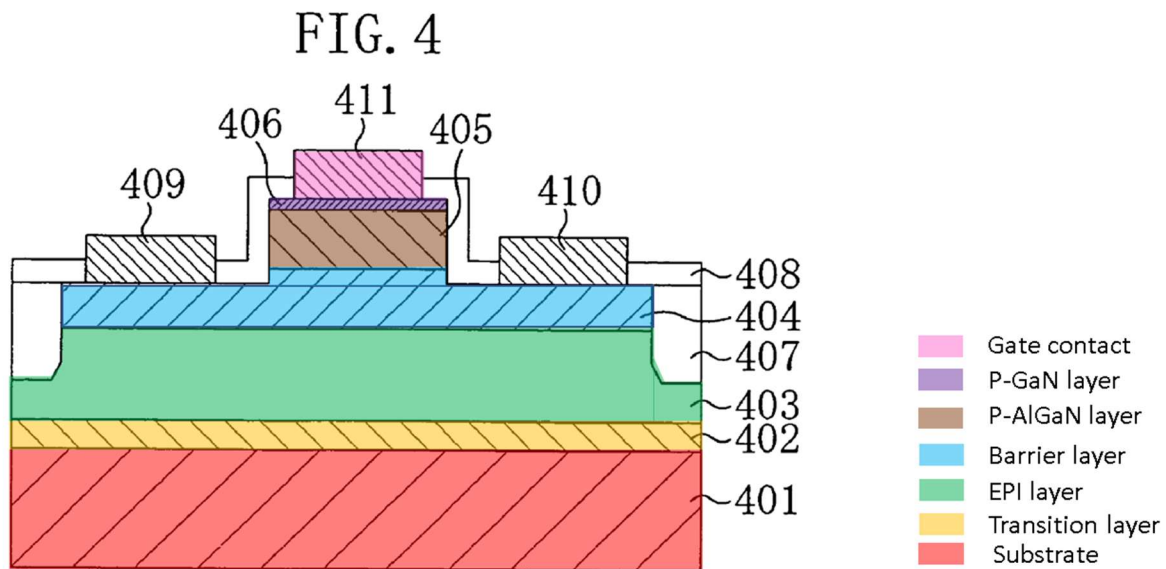


FIG. 2

Ex. 1001, Fig. 2.

Hikita-347 also discloses an enhancement mode GaN transistor that includes a first **p-type AlGaN layer 405** and a second **p-type GaN layer 406**. Compare:



Hikita-347, Fig. 4.

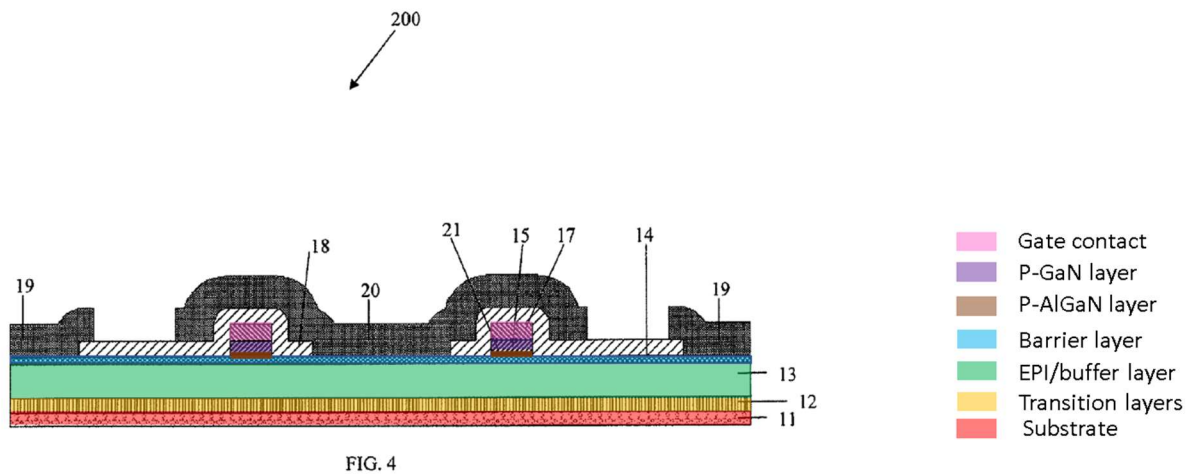


FIG. 4

Ex. 1001, Fig. 4.

Hikita-347 discloses that the GaN transistor is formed by the following steps. First, epitaxy layers are grown on a **substrate 101/401**, including (1) a

buffer layer 102/402, (2) an undoped GaN layer 103/403, (3) an undoped AlGaIn layer 104/404, and either (4) a p-GaN layer 105, or a p-type AlGaIn layer 405 and a p-type GaN layer 406. *Hikita-347*, [0013], [0033], [0056].

Second, the p-GaN layer 105, or p-type AlGaIn and p-type GaN layers 405/406 collectively, is etched away “in other part than the gate region.” *Hikita-347*, [0035], [0057]; Shealy, ¶87. Third, a dielectric layer (SiN film) 108/408 is formed to cover the entire surface with openings formed in the source and drain contact area and the gate area. *Hikita-347*, [0034], [0037], [0059]-[0061]. Finally, the source and drain contacts and the gate contact are formed to produce an enhancement mode GaN transistor. *Hikita-347*, [0013], [0037], [0060]-[0061]; Shealy, ¶87.

b. *Beach*

Hikita-347 does not explicitly show the use of a single mask to etch the gate material and p-type GaN material, or the process of etching the source and drain contact using a mask. But *Beach* does, as explained in Ground 1. §§VIII.A.2.f, VIII.A.2.h.

c. *Sheppard*

Hikita-347 arguably does not explicitly disclose multiple transition layers. But *Sheppard* does, as explained in Ground 1. §§VIII.A.1.c, VIII.A.2.b.

Hikita-347 does not explicitly show the process of forming openings in the dielectric layer (SiN film) 108. However, *Sheppard* does. *Sheppard* discloses using a mask pattern to open the ohmic contact area of the GaN transistor. *Sheppard* describes providing a **mask 40** and etching the cap layer to open windows for ohmic contacts (source/drain contacts) according to the mask, as shown below. *Sheppard*, 8:55-67. *Sheppard* discloses that cap layer includes SiN, a dielectric material. *Sheppard*, 3:21-23.

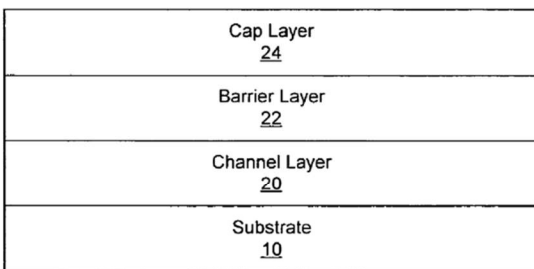


Figure 1B

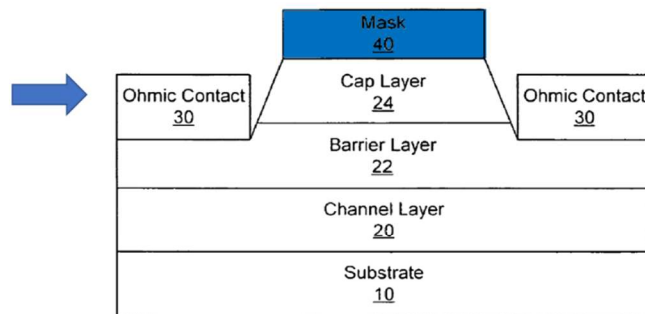


Figure 1C

Sheppard, Figs. 1B, 1C.

d. Motivation to Combine *Hikita-347*, *Sheppard*, and *Beach*

Like the *Yoshida* combination, *Hikita-347*, *Sheppard*, and *Beach* are all directed to GaN transistors and forming such a device using a multilayered epitaxial structure. *Hikita-347*, [0013], [0033], [0038], [0040], [0055]-[0061]; *Sheppard*, 6:45-8:54; *Beach*, [0002], [0017]-[0018]. Shealy, ¶¶163, 180. A

POSITA would have been motivated to modify *Hikita-347* in view of *Sheppard* and *Beach* as explained below.

i. Motivation to Use *Sheppard*'s Multiple Transition Layers

Like the *Yoshida* combination, both *Hikita-347* and *Sheppard* are concerned with providing a high-quality GaN transistor and both disclose using a different material for the substrate—here Sapphire, rather than Silicon as in *Yoshida*. *Hikita-347*, [0033], [0056]; *Sheppard*, 7:19-23; *Yoshida*, [0008]-[0011], [0019]. A POSITA would have been motivated to include multiple transition layers in *Hikita-347*'s device and would expected success for the same reasons explained in Ground 1, which apply to GaN transistors formed using a silicon or a sapphire substrate. Shealy, ¶162; §VIII.A.1.d.i. In addition, a POSITA would have been motivated to include multiple transition layers to improve the quality of *Hikita-347*'s GaN transistor by reducing the line defects formed during the growth of GaN epitaxy over sapphire. Shealy, ¶164; *Piner*, [0003]-[0004], [0076]-[0079], [0092].

ii. Motivation to Use *Beach*'s Single Mask Gate Process

Like the *Yoshida* combination, *Hikita-347* and *Beach* disclose a GaN device where the doped GaN layer is etched away except the gate region. *Hikita-347*, [0035], [0057]; *Beach*, [0043]-[0048]. In *Hikita-347*'s embodiment that includes

two p-type layers, both p-type layers are etched away in part other than the gate region. *Hikita-347*, [0057]. A POSITA would have been motivated to use *Beach*'s single mask process to form the gate contact and p-type GaN layer(s) in *Hikita-347*'s device and expected success for the same reasons explained in Ground 1. Shealy, ¶¶179, 229; §VIII.A.1.d.ii.

iii. Motivation to Use *Sheppard*'s Drain/Source Area Masking Process

Like *Hikita-347*, *Sheppard* discloses a GaN device with source and drain contacts. *Sheppard*, 3:16-27, 9:42-46. A POSITA would have been motivated to use the masking process to open the drain and source contact area, as taught by *Sheppard*, to improve *Hikita-347*'s device and process in multiple ways. Shealy, ¶201.

First, *Sheppard*'s masking process effectively achieves *Hikita-347*'s objective to open the drain and source contact area in the dielectric layer. Shealy, ¶193; *Hikita-347*, [0034], [0060]. *Hikita-347* does not disclose how to perform etching of the dielectric layer to open the drain and source contact area, and a POSITA would have appreciated that *Sheppard*'s masking process would allow etching of the dielectric layer to open the drain and source contact area, allowing *Hikita-347*'s transistor to perform its intended functions. Shealy, ¶193.

Second, *Sheppard*'s masking process enables the drain and source contact area to be formed at the desired locations. Shealy, ¶197. A POSITA would have understood that *Sheppard*'s masking process allows control of the etching such that only the dielectric layer at desired areas is etched and leaving the other part of the dielectric layer intact, and that such precision and control is essential for manufacturing of any semiconductor device. *Id.*

A POSITA would have expected success because using a mask to form openings in a dielectric layer of a semiconductor device was a well-known and conventional technique. Shealy, ¶195; *Yoshida*, [0022]. The '508 patent does not explain how to apply a mask to etch the dielectric layer, because using a mask to pattern and etch a dielectric layer was routine, conventional, and well understood in the art. Shealy, ¶195. Both *Hikita-347*'s and *Sheppard*'s devices use a SiN material in the layer where etching is performed to open the source and drain contact area. Shealy, ¶195; *Hikita-347*, [0034], [0060]; *Sheppard*, 8:37-39 (the cap layer includes a SiN layer), 9:15-25 (same). *Hikita-347*'s drain and source contact area could be opened using the masking process described by *Sheppard*, according to the known, routine process of masking and etching. Shealy, ¶195.

iv. Motivation to Use *Beach*'s Source and Drain Masking Process

Like the *Yoshida* combination, *Hikita-347* and *Beach* disclose forming source and drain contacts using ohmic metal. *Hikita-347*, [0034], [0060]; *Beach*, [0048]-[0049]. A POSITA would have been motivated to use *Beach*'s source and drain masking process to form the source and drain contacts in *Hikita-347*'s device and expected success for the same reasons explained in Ground 1. Shealy, ¶200; §VIII.A.1.d.iii.

2. Claim 1

a. [1pre]

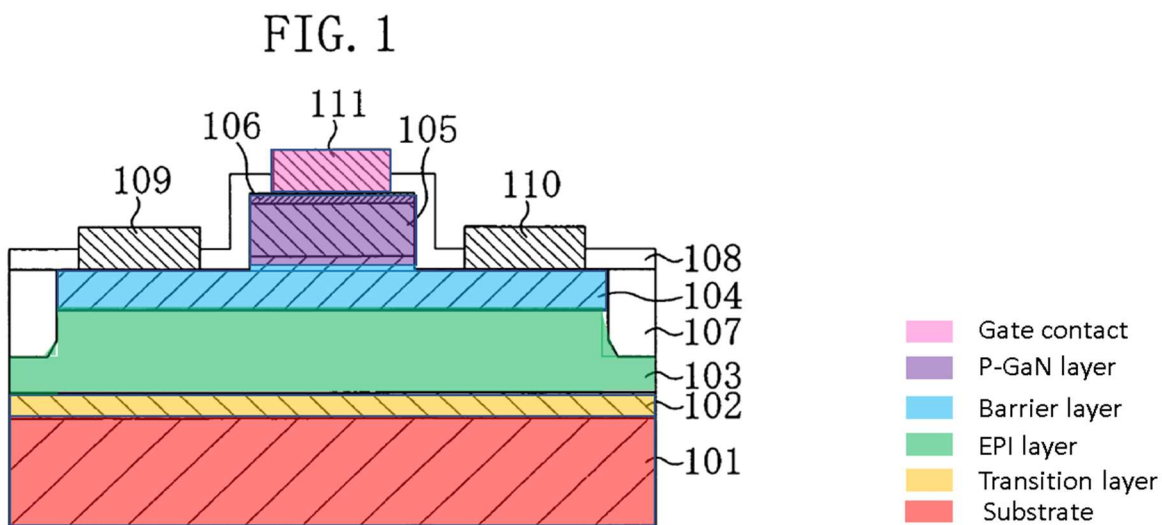
Hikita-347 discloses [1pre]. Shealy, ¶155.

Hikita-347 discloses a “normally OFF type” GaN transistor with a p-type GaN layer below the gate, constituting an enhancement mode GaN transistor. *Hikita-347*, [0038], Fig. 1; Shealy, ¶156. *Hikita-347* discloses a method of forming such an enhancement mode GaN transistor, including growing epitaxial layers over a substrate and etching the p-type GaN layer. *Hikita-347*, [0013], [0035], [0055]-[0061].

b. [1a]

Hikita-347 in view of *Sheppard* renders obvious [1a]. *Shealy*, ¶157. *Hikita-347* discloses nucleating and growing a transition layer on a substrate, and *Sheppard* discloses providing multiple transition layers on the substrate. *Id.*

Hikita-347 discloses growing an **AlN buffer layer 102** over a **substrate 101** by epitaxial growth, as shown below. *Hikita-347*, [0013], [0033]; *Shealy*, ¶158. *Hikita-347* discloses that the **substrate 101** is a sapphire material. *Hikita-347*, [0045], [0056].



Hikita-347, Fig. 1.

The **AlN buffer layer 102** is a transition layer because it is an intermediate layer between the **substrate 101** and the **undoped GaN layer 103**. *Shealy*, ¶159; Ex. 1001, 3:26-29 (describing **transition layers** above the **substrate** and underneath the **undoped GaN layer**).

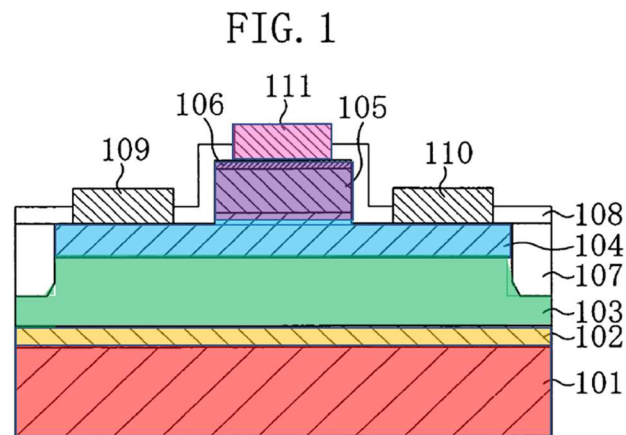
Hikita-347 discloses applying known a MOCVD method to grow the transition layer (AlN buffer layer 102) on the sapphire substrate. *Hikita-347*, [0033], [0056]. A POSITA would have understood that growing a transition layer on a sapphire substrate using the MOCVD method includes an initial phase of nucleation and then growth of the transition layer. Shealy, ¶160; *Sheppard*, 6:58-62 (providing an AlN buffer layer to “provide an appropriate crystal structure transition”), 7:29-32 (“buffer nucleation and/or transition layers may be deposited by MOCVD”). The ’508 patent does not provide any description of the nucleating process, confirming that it was a well-known technique to a POSITA. Shealy, ¶160.

To the extent *Hikita-347* does not explicitly disclose providing multiple transition layers on a substrate, *Sheppard* renders this obvious. *Sheppard* discloses a GaN transistor that includes multiple transition layers on a sapphire substrate. *Sheppard*, 7:19-24. *Sheppard* discloses providing an “AlN buffer layer” and additional “strain balancing transition layer(s)” to “provide an appropriate crystal structure transition” between the substrate and the remainder of the device. *Sheppard*, 6:58-7:7. A POSITA would have been motivated and found it obvious to include multiple transition layers in *Hikita-347*’s device, as taught by *Sheppard*.
§VIII.B.1.d.i.

c. [1b]

Hikita-347 discloses [1b]. Shealy, ¶166.

Hikita-347 discloses growing an **undoped GaN layer 103** over the **buffer layer 102** (transition layer), as shown below. *Hikita-347*, [0013], [0033], [0056].



Hikita-347, Fig. 1.

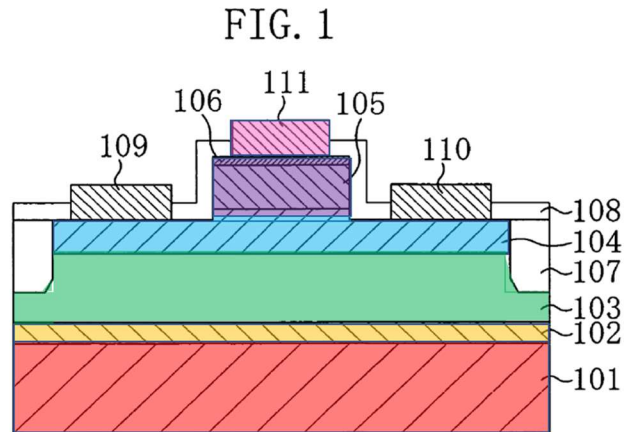
A POSITA would have understood that the **undoped GaN layer** is a III Nitride EPI layer because GaN is a III Nitride material. Shealy, ¶168. The '508 patent confirms this understanding. Ex. 1001, 3:24-25 (explaining that “[a] III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$ ”).

d. [1c]

Hikita-347 discloses [1c]. Shealy, ¶169.

Hikita-347 discloses growing an **undoped AlGaIn layer 104** (barrier layer) over the **undoped GaN layer 103** (EPI layer), as shown below. *Hikita-347*, [0013], [0033], [0056]. Like the device in the '508 patent, *Hikita-347* discloses that

the source and drain contacts 109, 110 are directly formed on the **n-type undoped AlGa_N layer 104** (barrier layer). *Hikita-347*, [0034]; Shealy, ¶170.



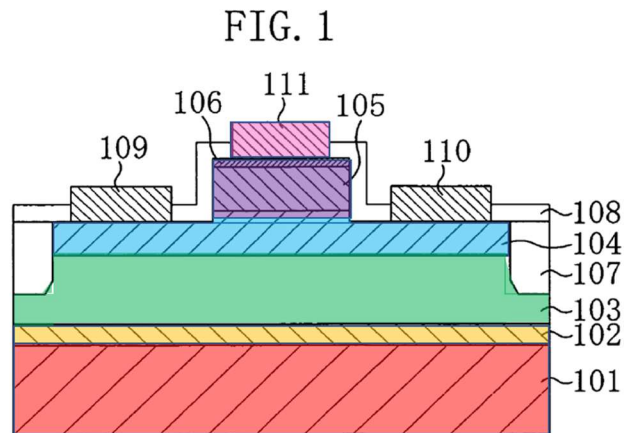
Hikita-347, Fig. 1.

A POSITA would have understood that the **undoped AlGa_N layer 104** is a III Nitride barrier layer because **AlGa_N** is a III Nitride material. Shealy, ¶171; Ex. 1001, 3:26-31 (providing an “AlGa_N barrier layer” over the EPI layer).

e. [1d]

Hikita-347 discloses [1d]. Shealy, ¶172.

Hikita-347 discloses growing a **p-type Ga_N layer 105** containing a p-type impurity over the **undoped AlGa_N layer 104** (barrier layer). *Hikita-347*, [0013], [0033], [0056].



Hikita-347, Fig. 1.

A POSITA would have understood that the p-type dopants in the **p-type GaN layer** are acceptor-type dopants. Shealy, ¶174; Ex. 1001, 6:24-28 (explaining that p-type dopants are “acceptor-rich”), 3:26-31.

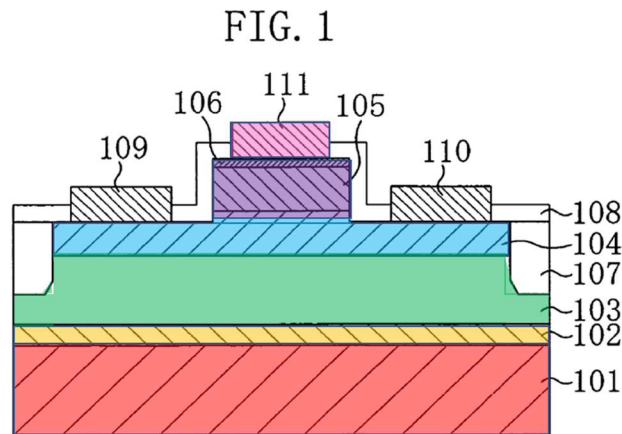
f. [1e]

Hikita-347 in view of *Beach* renders obvious [1e]. Shealy, ¶175. *Hikita-347* discloses etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact ([1e4]), and *Beach* renders obvious all steps in element [1e]. *Id.*

Hikita-347 discloses forming a **gate electrode 111** (gate contact) over the **p-type GaN layer 105**, as shown below. *Hikita-347*, [0013], [0034], [0061].

Although Figure 1 shows having a second p-type GaN layer 106 below the gate electrode 111, *Hikita-347* notes that it is “not necessary” to provide the second

p-type GaN layer 106, resulting in the gate electrode 111 formed directly over the p-type GaN layer 105. *Hikita-347*, [0040]; Shealy, ¶176.



Hikita-347, Fig. 1.

Hikita-347 discloses that, to form the p-type GaN layer 105 and gate contact 111, the portion of p-type GaN layer “located in other part than the gate region” is etched away. *Hikita-347*, [0035], [0057]. Although Figure 1 shows that the p-type GaN layer 105 extends beyond the gate contact 111, *Hikita-347* discloses in the description that the p-type GaN layer extending beyond the gate electrode is to be etched away. *Hikita-347*, [0035], [0057]; Shealy, ¶177.

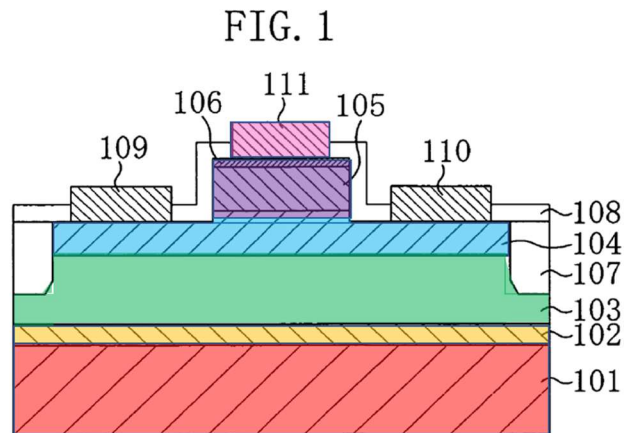
Hikita-347 does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the p-type GaN layer and gate contact layer, nor does Figure 1 show a p-GaN layer and gate electrode of the same width, but *Beach* renders this obvious. Shealy, ¶178. As explained in Ground 1, *Beach* discloses using a single mask to form a self-aligned gate and doped GaN layer with the steps

of element [1e]. §VIII.A.2.f. A POSITA would have been motivated to apply *Beach*'s single mask process to form *Hikita-347*'s device and expected success in doing so. §VIII.B.1.d.ii.

g. [1f]

Hikita-347 in view of *Sheppard* renders obvious [1f]. Shealy, ¶185. *Hikita-347* discloses depositing a dielectric layer and etching the dielectric layer to open the drain and source contact area ([1f1], [1f3]), and *Sheppard* renders obvious using a mask (contact photo resistant pattern) to open the drain and source contact area ([1f2], [1f4]). *Id.*

Hikita-347 discloses that, after etching away the p-type GaN layer, a “SiN film 108” was deposited which covers “an upper surface of the transistor,” as shown below. *Hikita-347*, [0034], [0037], [0059]. A POSITA would have understood that SiN (silicon nitride), the same dielectric material the '508 patent uses, is a material that has excellent dielectric properties and is commonly used as the dielectric material for semiconductor devices. Shealy, ¶186; Ex. 1001, 3:57-58.



Hikita-347, Fig. 1.

Hikita-347 discloses performing etching to form openings in the dielectric layer (SiN film 108) for drain and source contacts. *Hikita-347*, [0034], [0060].

Hikita-347 does not explicitly disclose using a mask (contact photo resistant pattern) to form the openings in the dielectric layer, but *Sheppard* renders this obvious. Shealy, ¶188.

Sheppard discloses using a mask pattern to form openings in a cap layer 24 for the ohmic contacts (source/drain contacts). *Sheppard* describes providing a **mask 40** and etching the cap layer to open windows for ohmic contacts (source/drain contacts) according to the mask, as shown below. Shealy, ¶189; *Sheppard*, 8:55-67. *Sheppard* explains that the etching process results in exposure of areas of the underlying barrier layer 22. Shealy, ¶189; *Sheppard*, 8:61-63. *Sheppard* also discloses that cap layer includes SiN, a dielectric material. *Sheppard*, 3:21-23.

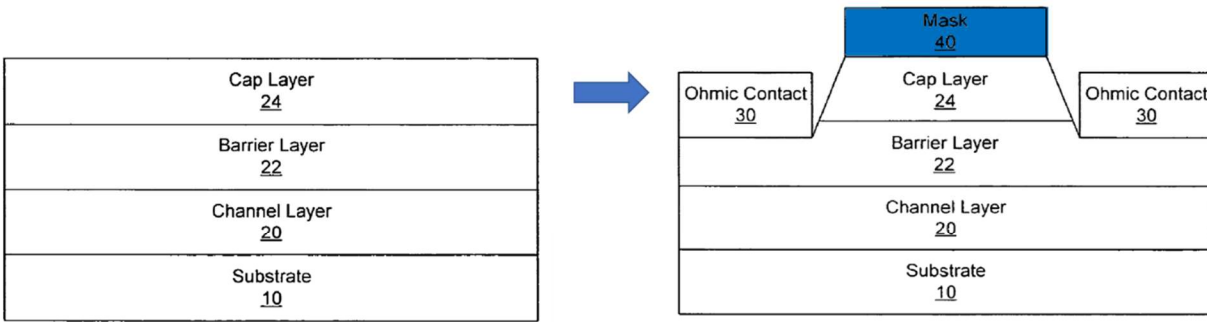


Figure 1B

Figure 1C

Sheppard, Figs. 1B, 1C.

Sheppard discloses that the mask 40 is removed after the ohmic contacts are formed, as shown in Figure 1D where the mask 40 is no longer present. Shealy, ¶190. A POSITA would have also understood that, in semiconductor manufacturing, the masks used to pattern and form the device are to be removed because the masks are only tools to construct the device and not part of the device. *Id.*; *Ghandhi*, 12. A POSITA would have been motivated to apply *Sheppard*'s drain/source area masking process to form *Hikita-347*'s device and expected success in doing so. §VIII.B.1.d.iii.

h. [1g]

Hikita-347 in view of *Beach* renders obvious [1g]. Shealy, ¶196.

Hikita-347 discloses depositing a Ti layer and an Al layer (ohmic contact metal) on the n-undoped AlGaN layer 104 to form a source electrode 109 and a

drain electrode 110 (ohmic source and drain contacts). *Hikita-347*, [0034], [0060]; Shealy, ¶197.

Hikita-347 discloses performing “heat treatment ... in an N₂ atmosphere at 650° C” to form the ohmic source and drain contacts. *Hikita-347*, [0060]. Thus, *Hikita-347* discloses performing thermal annealing to form ohmic drain and source contacts. To the extent EPC argues that *Hikita-347* does not explicitly disclose rapid thermal annealing, a POSITA would have found it obvious to perform rapid thermal annealing to form ohmic source and drain contacts in *Hikita-347*’s devices (step [1g5]). Shealy, ¶198. As explained in Ground 1, a POSITA would have been motivated to perform rapid thermal annealing to form ohmic contacts and expected to succeed in in doing so. §VIII.A.2.h.

Hikita-347 does not explicitly disclose a masking and etching process for forming the ohmic source and drain contacts, but *Beach* discloses using a masking and etching process ([1g2], [1g3], [1g4]) to form ohmic contacts as explained in Ground 1. §VIII.A.2.h; *Beach*, [0045]-[0047]. A POSITA would have been motivated to apply *Beach*’s masking process to form *Hikita-347*’s ohmic source and drain contacts and expected success in doing so. §VIII.B.1.d.iv.

3. Claim 2

Sheppard renders obvious claim 2. Shealy, ¶206.

Hikita-347 does not explicitly disclose that the EPI layer (layer 103) is comprised of InAlGa_N. *Sheppard* does. *Sheppard* discloses that the channel layer 20 (EPI layer) is an AlInGa_N material. *Sheppard*, 7:40-41. A POSITA would have understood that *Sheppard*'s channel layer 20 corresponds to the "EPI layer" because, like the EPI layer in the '508 patent, the channel layer 20 is provided under the barrier layer 22, and together they form a two-dimensional electron gas. *Sheppard*, 7:47-8:3, Fig. 3; Shealy, ¶207.

It would have been obvious to use an InAlGa_N material for the EPI layer of *Hikita-347*'s device, as disclosed by *Sheppard*. Shealy, ¶208. A POSITA would have been motivated to use InAlGa_N for the EPI layer to increase the breakdown voltage of *Hikita-347*'s transistor. *Id.* It was known that some alloys of the InAlGa_N material have higher critical electric field strengths than Ga_N, resulting in a larger breakdown voltage of the transistor. *Id.* A POSITA would have also been motivated to include an InAlGa_N for the EPI layer to construct a quantum well in *Hikita-347*'s transistor, such that the gate length of the transistor can be shortened for use in high frequency applications. *Id.*; *Ambacher*, 1 (constructing a quantum well structure using a compound with indium gallium nitride).

A POSITA would have understood that using InAlGa_N is merely an obvious design choice to form an EPI layer of *Hikita-347*'s transistor because the Group III nitride family includes combinations of Al (aluminum), In (indium), Ga (gallium)

with nitride, and a combination of Al, In, and Ga with nitride is an obvious combination from elements of the Group III nitride family. Shealy, ¶208; *Yoshida*, [0012]; *Sheu*, 6 (providing AlInGaN in each layer of a GaN-based transistor). The '508 patent does not identify a specific composition of the InAlGaN compound or state any differentiating characteristics or purpose for using the InAlGaN compound in the EPI layer. The only instance the InAlGaN material appears in the '508 patent is in a generic statement that the EPI layer 13 is made of a "III Nitride material" and "can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$." Ex. 1001, 3:23-25; *Ex parte Spangler*, Appeal No. 2018-003800, at 7-8 (PTAB Feb. 20, 2019) (informative) (because the applicants failed to identify a stated problem/solution relating to the differentiating feature or any particular purpose for the differentiating feature, the PTAB agreed that the feature would have been an obvious design choice).

A POSITA would have reasonably expected to succeed in using InAlGaN for the EPI layer of *Hikita-347*'s transistor because using InAlGaN to form an EPI layer routine, conventional, and well understood in the art. Shealy, ¶208; *Yoshida*, [0012]; *Sheu*, 6 (providing AlInGaN in each layer of a GaN-based transistor). The '508 patent does not explain how to grow InAlGaN in an EPI layer, because it was routine, conventional, and well understood in the art. Shealy, ¶208. Using

Sheppard's InAlGa_N for an EPI layer in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner. *Id.*

4. Claim 3

Hikita-347 in view of *Sheppard* renders obvious claim 3. Shealy, ¶209.

Hikita-347 discloses that the barrier layer has a larger band gap than the buffer layer in order to form a two dimensional electron gas. *Hikita-347*, [0009] (the second nitride semiconductor layer, i.e., the barrier layer, has a larger band gap energy than the first nitride semiconductor layer, i.e., the buffer layer); Shealy, ¶210.

Hikita-347 does not explicitly disclose that the barrier layer (layer 104) is comprised of InAlGa_N. However, *Sheppard* does. For example, *Sheppard* discloses that the barrier layer 22 is an AlInGa_N material. *Sheppard*, 7:52-54. *Sheppard* also discloses that the barrier layer 22 has a larger band gap than the channel layer 20 (buffer layer). *Sheppard*, 8:4-9.

It would have been obvious to use an InAlGa_N material that has a larger band gap than the buffer layer as the barrier layer of *Hikita-347*'s device, as disclosed by *Sheppard*. Shealy, ¶212. A POSITA would have been motivated to use InAlGa_N for the barrier layer to increase the device performance with reduced strain because it was known that InAlGa_N is better lattice matched with the Ga_N materials in *Hikita-347*'s transistor. *Id.*; *Liu*, 1 (InAlGa_N as a barrier layer reduces

the built-in strain and increases polarization). A POSITA would have understood that using InAlGaN is merely an obvious design choice to form a barrier layer of *Hikita-347*'s transistor because the Group III nitride family includes combinations of Al (aluminum), In (indium), Ga (gallium) with nitride, and a combination of Al, In, and Ga with nitride is an obvious combination from elements of the Group III nitride family. Shealy, ¶212; *Yoshida*, [0013]; *Sheu*, 6 (providing AlInGaN in each layer of a GaN-based transistor). The '508 patent does not identify a specific composition of the InAlGaN compound or state any differentiating characteristics or purpose for using the InAlGaN compound in the barrier layer. The only instance the InAlGaN material appears in the '508 patent is in a generic statement that the barrier layer 14 is made of a "III Nitride material" and "can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$." Ex. 1001, 3:23-25; *Ex parte Spangler*, Appeal No. 2018-003800, at 7-8. A POSITA would have reasonably expected to succeed in using InAlGaN for the barrier layer of *Hikita-347*'s transistor because using InAlGaN to form a barrier layer was routine, conventional, and well understood in the art. Shealy, ¶213; *Yoshida*, [0013]; *Sheu*, 6. The '508 patent does not explain how to grow InAlGaN in a barrier layer, because it was routine, conventional, and well understood in the art. Shealy, ¶213. Using *Sheppard*'s InAlGaN for a barrier layer in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner. *Id.*

5. Claim 4

- a. [4pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”**

[4pre] is identical to [1pre], and *Hikita-347* discloses [4pre] for the same reasons as [1pre]. §VIII.B.2.a; Shealy, ¶217.

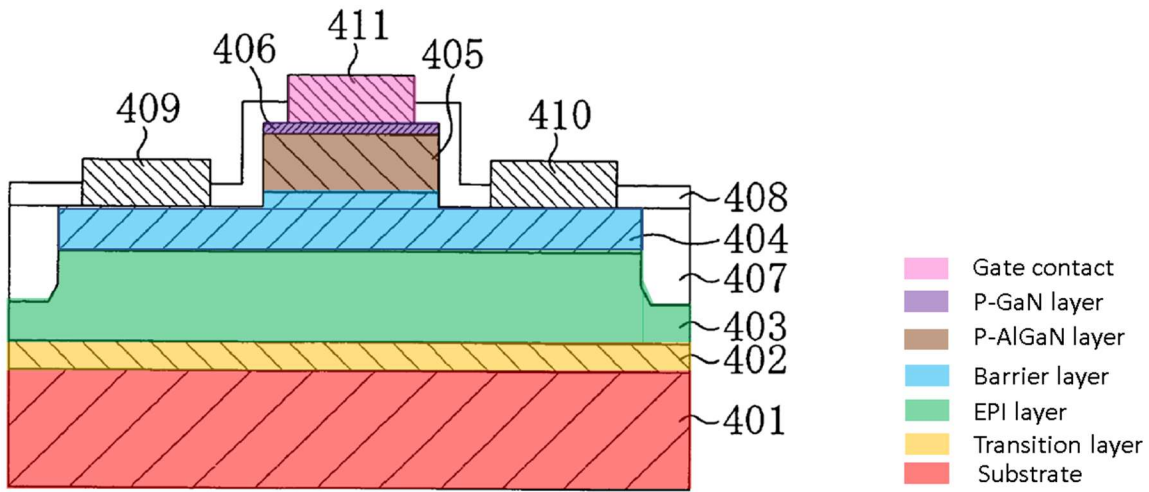
- b. [4a]: “nucleating and growing transition layers on a substrate;”**

[4a] is identical to [1a], and *Hikita-347* in view of *Sheppard* renders obvious [4a] for the same reasons as [1a]. §VIII.B.2.b.

- c. [4b]: “growing an InAlGaN EPI layer over the transistor layers;”**

Hikita-347 in view of *Sheppard* renders obvious [4b]. Shealy, ¶219. *Hikita-347* discloses growing an **undoped GaN layer 403** over the **buffer layer 402** (transition layer), as shown below, and for the same reasons discussed in claim 2, *Sheppard* renders obvious that the EPI layer is comprised of InAlGaN. *Id.*; *Hikita-347*, [0048], [0056]; §VIII.B.3.

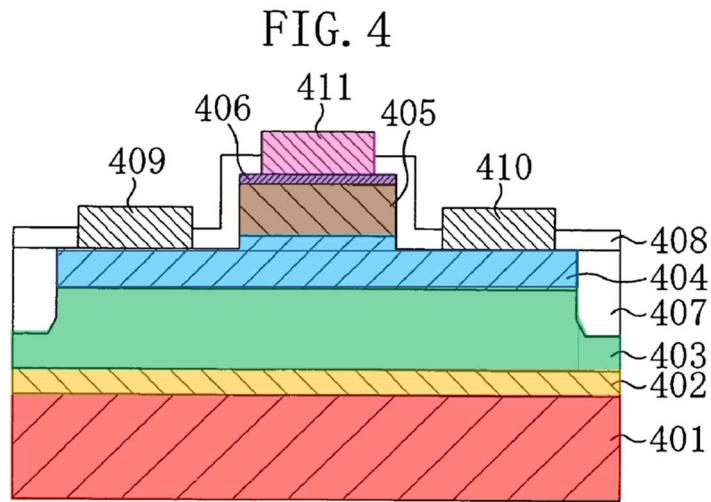
FIG. 4



Hikita-347, Fig. 4.

d. [4c]: “growing an InAlGa_N barrier layer over the InAlGa_N EPI layer;”

Hikita-347 in view of *Sheppard* renders obvious [4c]. Shealy, ¶220. As explained for [1c], *Hikita-347* discloses growing an **undoped AlGaIn layer 104** (barrier layer) over the EPI layer. *Id.*; *Hikita-347*, [0013], [0033], [0056], §VIII.B.2.d. As explained for claim 3, *Sheppard* renders obvious that the barrier layer is comprised of InAlGaIn. Shealy, ¶220; *Hikita-347*, [0048], [0056]; §VIII.B.4.

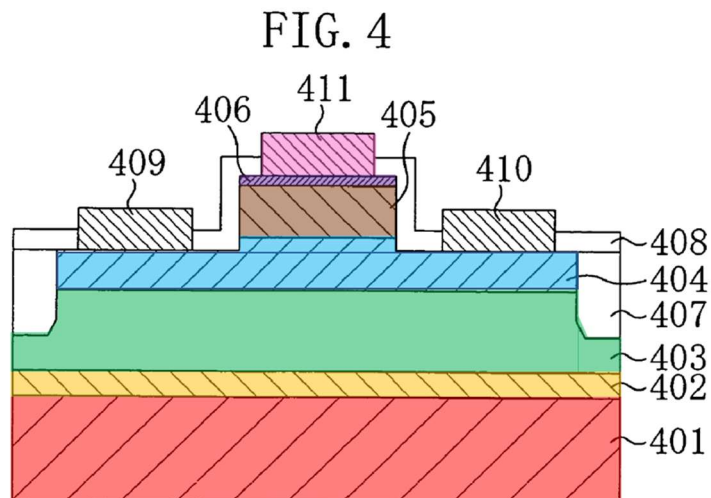


Hikita-347, Fig. 4.

- e. [4d]: “growing an InAlGa_N layer with acceptor type dopants over the InAlGa_N barrier layer;”

Hikita-347 renders obvious [4d]. Shealy, ¶221.

Hikita-347 discloses growing a first doped layer, **p-type AlGa_N layer 405**, over the barrier layer, as shown below. *Hikita-347*, [0048], [0056].



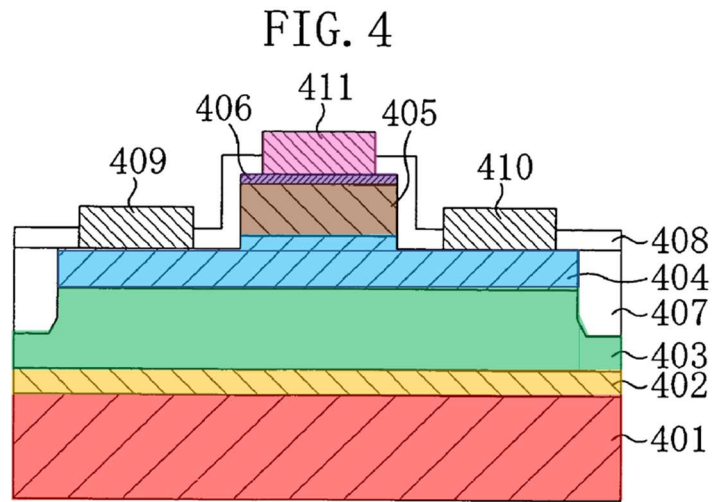
Hikita-347, Fig. 4.

It would have been obvious to use an InAlGa_N material for the first doped layer (first p-type layer over the barrier layer) of *Hikita-347*'s device. Shealy, ¶223. A POSITA would have understood that using InAlGa_N is merely an obvious design choice to form the layer over the barrier layer of *Hikita-347*'s transistor because the Group III nitride family includes combinations of Al (aluminum), In (indium), Ga (gallium) with nitride, and a combination of Al, In, and Ga with nitride is an obvious combination from elements of the Group III nitride family. *Id.*; *Sheu*, 9-10 (providing a doped AlInGa_N layer 318 over the barrier layer 310); *Mizutani*, [0028], [0031] (providing a p-type InGaAlN layer as the field generating layer under the gate). The '508 patent does not identify a specific composition of the InAlGa_N compound or state any differentiating characteristics or purpose for using the p-type InAlGa_N compound as the layer over the barrier layer. The only instance the InAlGa_N material appears in the '508 patent is in a generic statement that the EPI layer 13, barrier layer 14, and p-type gate layer 15 are made of a "III Nitride material" and "can be composed of In_xAl_yGa_{1-x-y}N, where x+y≤1." Ex. 1001, 3:23-25; *Ex parte Spangler*, Appeal No. 2018-003800, at 7-8 (because the applicants failed to identify a stated problem/solution relating to the differentiating feature or any particular purpose for the differentiating feature, the PTAB agreed that the feature would have been an obvious design choice). When an InAlGa_N layer is provided as the barrier layer underneath, it would have been obvious to a

POSITA to use the p-type InAlGaN over the InAlGaN barrier layer, because using the same material would simplify the manufacturing process and cost. Shealy, ¶223. A POSITA would have been motivated to form a p-type InAlGaN layer as the first p-type layer in *Hikita-347* because the p-type InAlGaN layer could be formed merely by switching in the p-type dopant during growth when InAlGaN of the same composition is used for the barrier layer. *Id.* And a POSITA would have had a reasonable expectation of success in doing so because using InAlGaN to form a p-type layer over the barrier layer was routine, conventional, and well understood in the art, as described in *Sheu* and *Mizutani*. *Id.*

f. [4e]: “growing a GaN layer with acceptor type dopants over the doped InAlGaN layer;”

Hikita-347 renders obvious [4e]. Shealy, ¶224. *Hikita-347* discloses growing a second doped layer, **p-type GaN layer 406**, over the **first p-type layer 405**, as shown below. *Hikita-347*, [0048], [0056]. As explained for [4d], it would have been obvious to use a p-type InAlGaN for the first p-type layer in *Hikita-347*. §VIII.B.5.e.



Hikita-347, Fig. 4.

g. [4f]:

“[4f1] depositing a gate contact layer on the doped GaN layer

[4f2] applying a gate photo resistant pattern;

[4f3] etching away the gate contact layer outside the gate region;

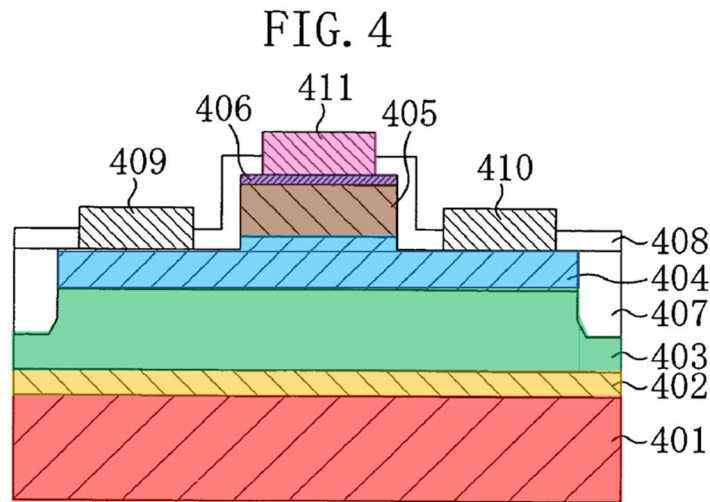
[4f4] etching away the doped GaN layer and the doped InAlGaN layer, except for portions of the doped GaN layer and the doped InAlGaN layer beneath gate contact;

[4f5] removing the gate photo resistant pattern;”

Hikita-347 in view of *Beach* renders obvious [4f]. Shealy, ¶225. *Hikita-347*

discloses etching away the first and second doped layers, except a portion of the layers beneath the gate contact ([4f4]), and *Beach* renders obvious all steps in element [4f]. *Id.*

Hikita-347 discloses forming a **gate electrode 411** (gate contact) over the **p-type GaN layer 406**, as shown below. *Hikita-347*, [0013], [0034], [0061].



Hikita-347, Fig. 4.

Hikita-347 discloses that, to form the first and second p-type layers 405 and 406 and gate contact 411, the portion of first and second p-type layers “located in other part than a gate region” is etched away. *Hikita-347*, [0057]. Although Figure 4 shows that the first and second p-type layers 405 and 406 extend beyond the gate contact 111, *Hikita-347* discloses in the description that the first and second p-type layers extending beyond the gate electrode are to be etched away. *Hikita-347*, [0057]; Shealy, ¶226. *Hikita-347* discloses the first and second p-type layers 405 and 406 being p-type AlGaN layer and p-type GaN layer respectively, and as discussed in [4d], it would have been obvious to use p-type InAlGaN for the first p-type layer.

Hikita-347 does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the first and second p-type layers and gate contact layer, but *Beach* renders this obvious. Shealy, ¶228.

As explained in Ground 1, *Beach* discloses using a single mask to form a self-aligned gate and doped GaN layer with the steps of [4f]. §VIII.A.2.f. The '508 patent admitted that it was known in the art to use a same mask to etch a first and a second doped layer. Ex. 1001, 1:65-2:3. It would have been obvious to apply *Beach*'s masking process to etch both the first and second p-type layers and gate contact layer in *Hikita-347*'s device. §VIII.A.1.d.ii.

- h. [4g]:
 - “[4g1] depositing a dielectric layer;
 - [4g2] applying a contact photo resistant pattern;
 - [4g3] etching the dielectric layer to open the drain and source contact area;
 - [4g4] removing the contact photo resistant pattern;

[4g] is identical to [1f], and *Hikita-347* in view of *Sheppard* renders obvious [4g] for the same reasons as [1f]. Shealy, ¶235; §VIII.B.2.g.

i. [4h]:

**“[4h1] depositing an Ohmic contact metal;
[4h2] applying a metal photo resistant pattern;
[4h3] etching the Ohmic contact metal;
[4h4] removing the metal photo resistant pattern; and
[4h5] performing rapid thermal annealing to form
Ohmic drain and source contacts.”**

[4h] is identical to [1g], and *Hikita-347* in view of *Beach* renders obvious [4h] for the same reasons as [1g]. Shealy, ¶238; §VIII.B.2.h.

C. Ground 3: Claim 5 Is Obvious over *Hikita-023*, *Beach*, and *Sheppard*

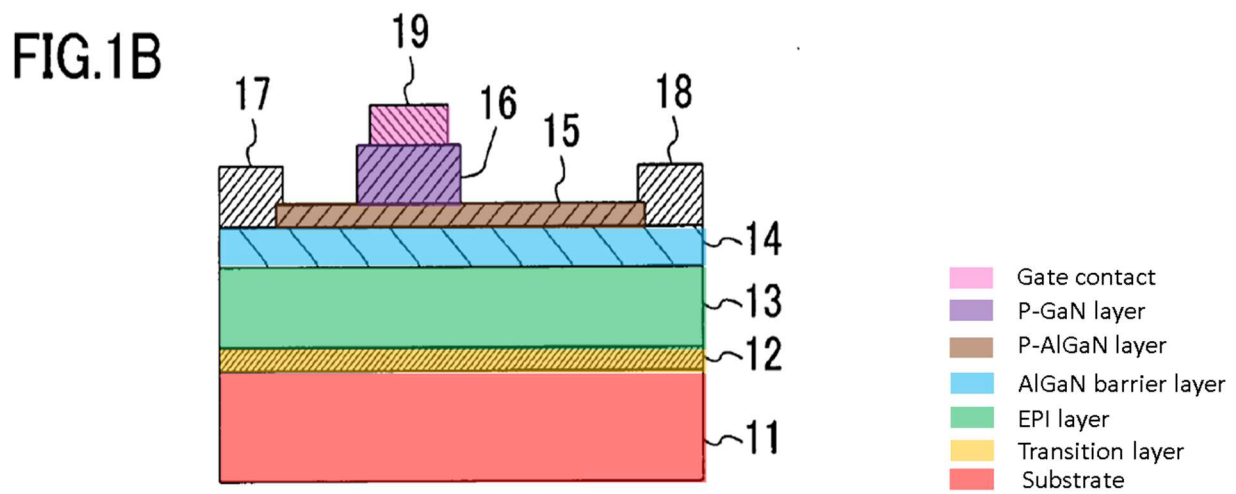
1. Overview of the Combination

Hikita-023 discloses growing various layers to form the device in claim 5 ([5a] through [5e]). *Hikita-023* does not explicitly disclose forming multiple transition layers ([5a]), using an InAlGa_N for the EPI layer ([5b]), or the masking steps ([5f], [5g], [5h]).

Sheppard renders obvious forming multiple transition layers on a substrate ([5a]), using InAlGa_N as a material for the EPI layer ([5b]), and the masking steps ([5g]) to open the drain and source contact area. And *Beach* renders obvious the masking steps to etch the gate metal and p-GaN layer ([5f]) and the masking steps to form the ohmic drain and source contacts ([5h]).

a. *Hikita-023*

Hikita-023 discloses an enhancement mode GaN transistor that includes a substrate 11, a buffer layer 12, an undoped GaN layer 13, an undoped AlGaN layer 14, a p-type AlGaN layer 15, and a p-type GaN layer 16, a gate contact 19, and source and drain contacts 17 and 18. *Hikita-023*, [0051]-[0056]. Compare:



Hikita-023, Fig. 1B.

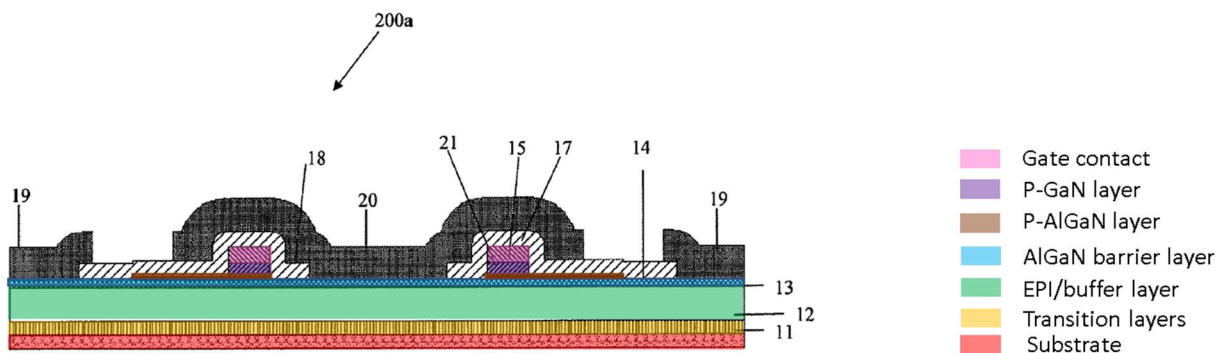


FIG. 7F

Ex. 1001, Fig. 7F.

Hikita-023 discloses that forming the GaN transistor is formed by the following steps. First, grow epitaxy layers on a substrate, including a buffer layer 12, an undoped GaN layer 13, an undoped AlGaIn layer 14, a p-type AlGaIn layer 15, and a p-type GaN layer 16. *Hikita-023*, [0051], [0076]. Second, etch away the p-type GaN layer 16 in part other than the gate region. *Hikita-023*, [0077]; Shealy, ¶90. Third, etch the p-type AlGaIn layer 15 to form regions for source and drain electrodes. *Hikita-023*, [0057], [0078]. Finally, form the contacts for the source, drain, and the gate to produce an enhancement mode GaN transistor. *Hikita-023*, [0079]-[0080]; Shealy, ¶90.

b. *Beach*

Hikita-023 does not explicitly show the use of a single mask to etch the gate material and p-type GaN layer, or the process of etching the source and drain contact using a mask. But *Beach* does, as explained in Ground 1. §§VIII.A.2.f, VIII.A.2.h.

c. *Sheppard*

Hikita-023 arguably does not explicitly disclose multiple transition layers. But *Sheppard* does, as explained in Ground 1. §VIII.A.2.b. *Hikita-023* does not explicitly show the process of forming openings in a dielectric layer for source and drain contact area. But *Sheppard* does, as explained in Ground 2. §VIII.B.1.c.

d. Motivation to Combine *Hikita-023*, *Sheppard*, and *Beach*

Like the other combinations, *Hikita-023*, *Sheppard*, and *Beach* are all directed to GaN transistors and forming such a device using a multilayered epitaxial structure. *Hikita-023*, [0051]-[0057], [0076]-[0080]; *Sheppard*, 6:45-8:54; *Beach*, [0002], [0017]-[0018]. Shealy, ¶¶253, 271. A POSITA would have been motivated to modify *Hikita-023* in view of *Sheppard* and *Beach* as explained below.

i. Motivation to Use *Sheppard*'s Multiple Transition Layers

Like the *Hikita-347* combination, both *Hikita-023* and *Sheppard* are concerned with providing a high-quality GaN transistor and both disclose a sapphire substrate. *Hikita-023*, [0051], [0076]; *Sheppard*, 7:19-23. A POSITA would have been motivated to include multiple transition layers in *Hikita-023*'s device and expected success for the same reasons. Shealy, ¶252; §§VIII.B.1.d.i, VIII.A.1.d.i.

ii. Motivation to Use *Beach*'s Single Mask Gate Process

Like the *Yoshida* combination, *Hikita-023* and *Beach* disclose a GaN device where the doped GaN layer is etched away other than the gate region. *Hikita-023*, [0077]; *Beach*, [0043]-[0048]. A POSITA would have been motivated to use

Beach's single mask process to form the gate contact and doped GaN layer and expected success for the same reasons. Shealy, ¶270; §VIII.A.1.d.ii.

iii. Motivation to Use *Sheppard*'s Drain/Source Area Masking Process

Like the *Hikita-347* combination, *Hikita-023* and *Sheppard* disclose a GaN device with source and drain contacts. *Hikita-023*, [0078]-[0079]; *Sheppard*, 3:16-27, 9:42-46. A POSITA would have been motivated to use *Sheppard*'s masking process to open the drain and source contact area and expected success for the same reasons. Shealy, ¶283; §VIII.B.1.d.iii.

iv. Motivation to Use *Beach*'s Source and Drain Masking Process

Like the *Yoshida* combination, *Hikita-023* and *Beach* disclose forming source and drain contacts using ohmic metal. *Hikita-023*, [0079]; *Beach*, [0048]-[0049]. A POSITA would have been motivated to use *Beach*'s source and drain masking process to form the source and drain contacts and expected success for the same reasons. Shealy, ¶292; §VIII.A.1.d.iii.

2. Claim 5

a. [5pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”

Hikita-023 discloses [5pre]. Shealy, ¶245.

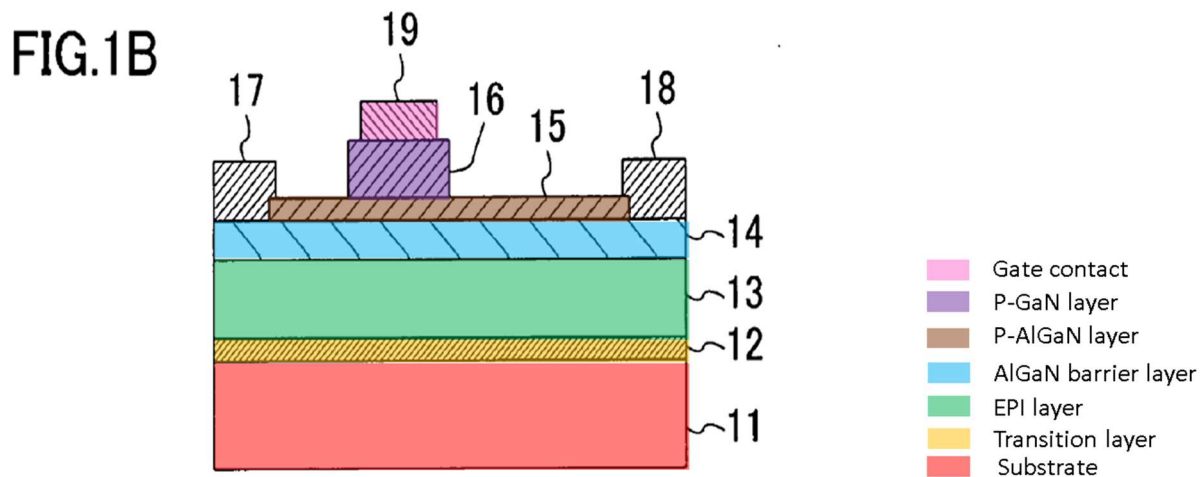
Hikita-023 discloses a “normally-off” type GaN transistor with a p-type GaN layer below the gate, constituting an enhancement mode GaN transistor.

Hikita-023, [0037], [0051], [0073]; Shealy, ¶246. *Hikita-023* discloses a method of forming such an enhancement mode GaN transistor, including growing epitaxial layers over a substrate and etching the p-type GaN layer. *Hikita-023*, [0074]-[0080].

b. [5a]: “nucleating and growing transition layers on a substrate;”

Hikita-023 in view of *Sheppard* renders obvious [5a]. Shealy, ¶247. *Hikita-023* discloses nucleating and growing a transition layer on a substrate, and *Sheppard* discloses providing multiple transition layers on the substrate. *Id.*

Hikita-023 discloses growing an **AlN buffer layer 12** over a **substrate 11** by epitaxial growth, as shown below. *Hikita-023*, [0051], [0076]; Shealy, ¶248. *Hikita-023* discloses that the **substrate 11** is a sapphire material. *Hikita-023*, [0051], [0076].



Hikita-023, Fig. 1B.

The **AlN buffer layer 12** is a transition layer because it is an intermediate layer between the **substrate 11** and the **undoped GaN layer 13**. Shealy, ¶249; Ex. 1001, 3:26-29 (describing **transition layers** located directly above the **substrate** and underneath the **undoped GaN layer**).

Hikita-023 discloses applying known a MOCVD method to grow the transition layer (AlN buffer layer 102) on the sapphire substrate. *Hikita-023*, [0076]. A POSITA would have understood that growing a transition layer on a sapphire substrate using the MOCVD method includes an initial phase of nucleation and then growth of the transition layer, as explained in Ground 2. Shealy, ¶250; §VIII.B.2.b.

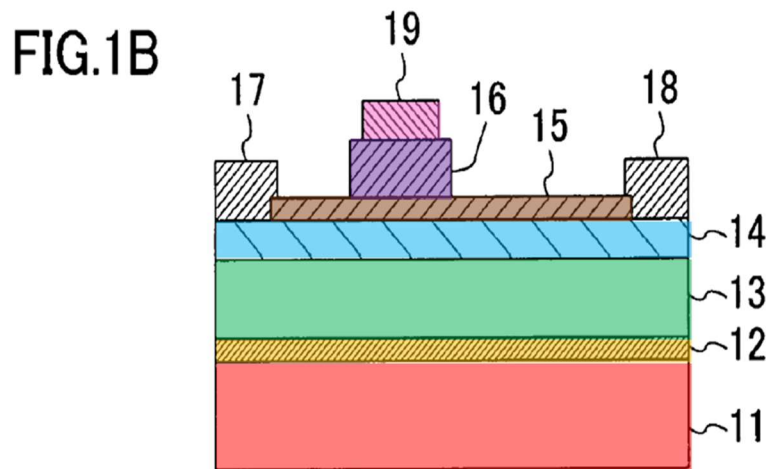
To the extent *Hikita-023* does not explicitly disclose providing multiple transition layers on a substrate, *Sheppard* discloses this. §VIII.B.2.b. A POSITA

would have been motivated and found it obvious to include multiple transition layers in *Hikita-023*'s device, as taught by *Sheppard*. §VIII.C.1.d.i.

c. [5b]: “growing an InAlGaN EPI layer over the transistor layers;”

Hikita-023 in view of *Sheppard* renders obvious [5b]. Shealy, ¶256.

Hikita-023 discloses growing an **undoped GaN layer 13** over the **buffer layer 12** (transition layer).



Hikita-023, Fig. 1B.

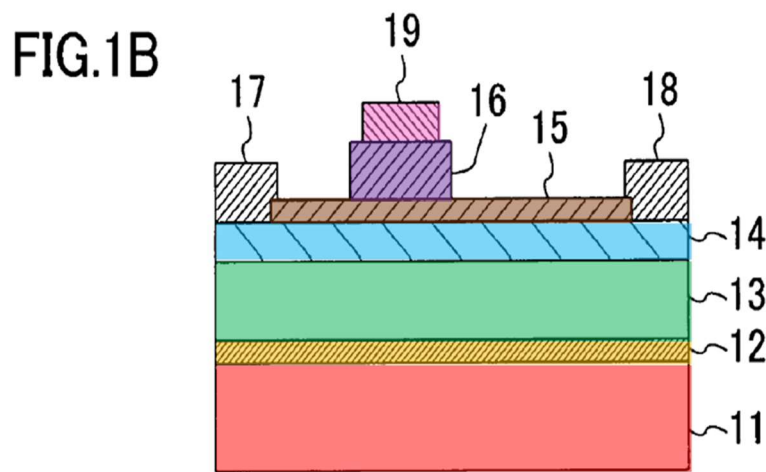
Hikita-023 does not explicitly disclose that the EPI layer (layer 13) is comprised of InAlGaN. *Sheppard* does. *Sheppard* discloses that the channel layer 20 (EPI layer) is an AlInGaN material. *Sheppard*, 7:40-41; §VIII.B.3.

It would have been obvious to use an InAlGaN material for the EPI layer of *Hikita-023*'s device, as disclosed by *Sheppard*, for the same reasons explained for *Hitkita-347* in Ground 2, claim 2. Shealy, ¶259; §VIII.B.3.

d. [5c]: “growing an AlGa_N barrier layer over the InAlGa_N EPI layer;”

Hikita-023 in view of *Sheppard* renders obvious [5c]. Shealy, ¶261.

Hikita-023 discloses growing an **undoped AlGa_N layer 14** (barrier layer) over the EPI layer, as shown below, and as explained for [5b], *Sheppard* renders obvious that the EPI layer comprises InAlGa_N. *Hikita-023*, [0051], [0076]; §VIII.C.2.c.

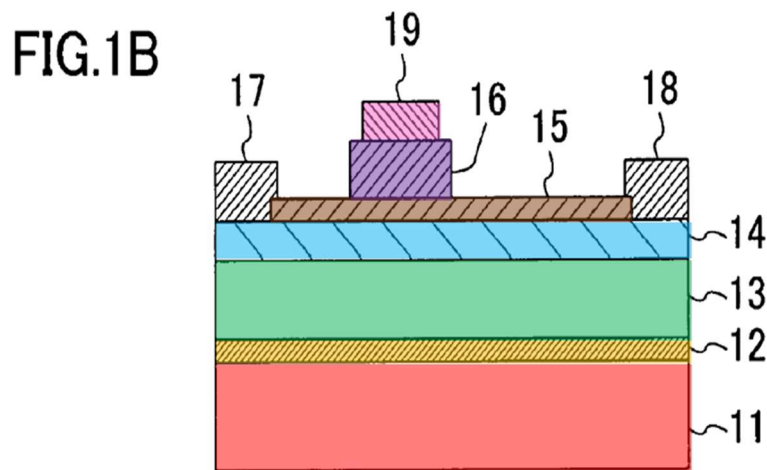


Hikita-023, Fig. 1B.

e. [5d]: “growing an AlGa_N layer with acceptor type dopants over the AlGa_N barrier layer;”

Hikita-023 discloses [5d]. Shealy, ¶262.

Hikita-023 discloses growing a first doped layer, **p-type AlGa_N layer 15**, over the AlGa_N barrier layer, as shown below. *Hikita-023*, [0051], [0076].

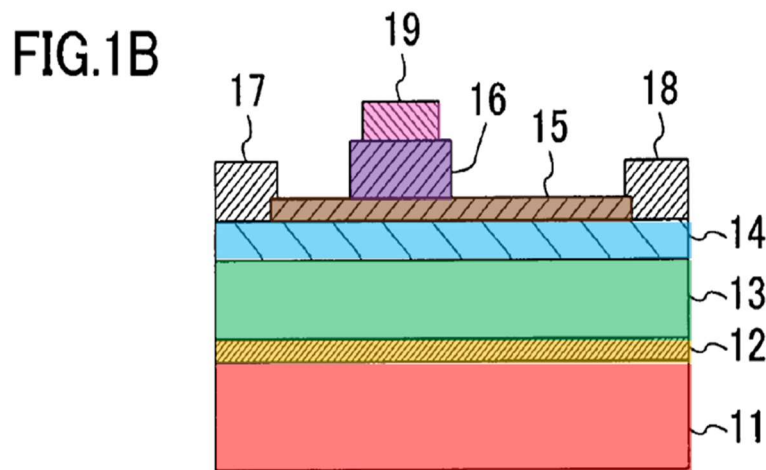


Hikita-023, Fig. 1B.

A POSITA would have understood that the p-type dopants in the **p-type AlGaN layer 15** are acceptor-type dopants. Shealy, ¶264; Ex. 1001, 6:24-28.

f. [5e]: “growing a GaN layer with acceptor type dopants over the doped AlGaN layer;”

Hikita-023 discloses [5e]. Shealy, ¶265. *Hikita-023* discloses growing a second doped layer, **p-type GaN layer 16**, over the **first p-type AlGaN layer 15**, as shown below. *Hikita-023*, [0051], [0076].



Hikita-023, Fig. 1B.

g. [5f]:

“[5f1] depositing a gate contact layer on the doped GaN layer

[5f2] applying a gate photo resistant pattern;

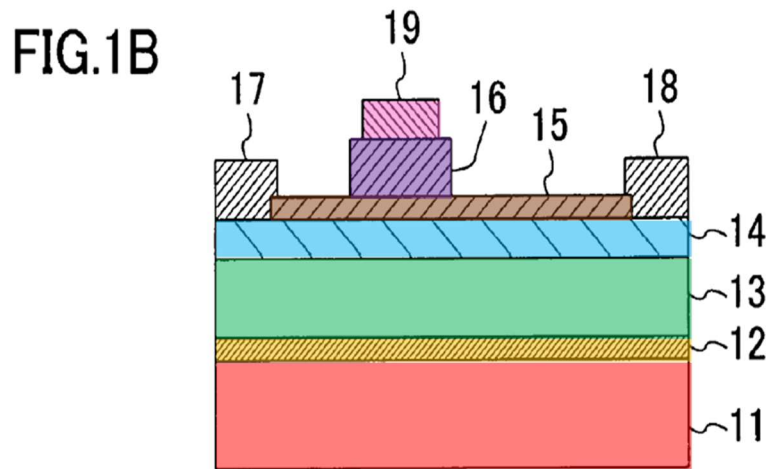
[5f3] etching away the gate contact layer outside the gate region;

[5f4] etching away the doped GaN layer, except for portions of the doped GaN layer and the doped AlGaN layer beneath gate contact;

[5f5] removing the gate photo resistant pattern;”

Hikita-023 in view of *Beach* renders obvious [5f]. Shealy, ¶266. *Hikita-023* discloses etching away the doped GaN layer, except for portions of the doped GaN layer beneath gate contact ([5f4]), and *Beach* renders obvious all steps in element [5f]. *Id.*

Hikita-023 discloses forming a **gate electrode 19** (gate contact) over the **p-type GaN layer 16**, as shown below. *Hikita-023*, [0056], [0080].



Hikita-023, Fig. 1B.

Hikita-023 discloses that, to form the p-type GaN layer 16, the portion of the p-type GaN layer “other than a gate formation region” is etched away. *Hikita-023*, [0077]. Although Figure 1B shows that the p-type GaN layer 16 extends beyond the gate contact 19, *Hikita-023* discloses in the description that the p-type GaN layer extending beyond the gate electrode is to be etched away. *Hikita-023*, [0077]; Shealy, ¶268.

Hikita-023 does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the p-type GaN layer and gate contact layer, but *Beach* renders this obvious. Shealy, ¶269. As explained in Ground 1, *Beach* discloses using a single mask to form a self-aligned gate and doped GaN layer with the steps

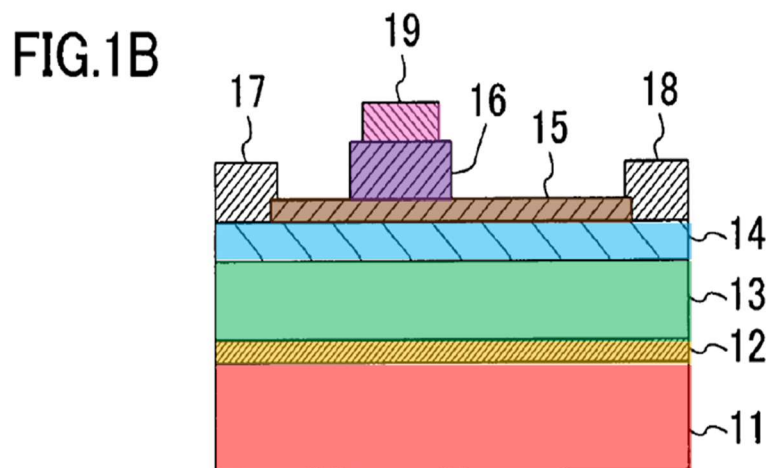
of element [5f]. §VIII.A.2.f. A POSITA would have been motivated to apply *Beach*'s single mask process to form *Hikita-023*'s device and expected success in doing so. §VIII.C.1.d.ii.

h. [5g]:

**“[5g1] applying another photo resistant pattern;
[5g2] etching the doped AlGa_N layer such that the doped AlGa_N extends outside the gate region towards the drain;
[5g3] removing the photo resistant pattern;**

Hikita-023 discloses [5g]. Shealy, ¶276.

Hikita-023 discloses etching the **doped AlGa_N layer 15** such that the doped AlGa_N extends outside the gate region towards the drain electrode 18 ([5g2]), as shown below. *Hikita-023*, [0078]; Shealy, ¶277.



Hikita-023, Fig. 1B.

Hikita-023 discloses that the etching of the doped AlGa_N layer is performed by a “lithography method.” *Hikita-023*, [0078]. A POSITA would have understood that lithography is a fundamental process in semiconductor manufacturing and involves the following steps: (1) applying a photo resistant pattern ([5g1]), (2) performing etching according to the photo resistant pattern ([5g2]), and (3) removing the photo resistant pattern ([5g3]). Shealy, ¶278; *Campbell*, 4 (describing a lithography process involving applying a photo resistant pattern, etching, and removing the photo resistant pattern); *Ghandhi*, 3-13 (same). A POSITA would have understood that a separate photo resistant pattern is applied to etch the doped AlGa_N layer 15 after etching the p-type Ga_N layer 16 and gate contact 19, because the doped AlGa_N layer 15 has a different length from that of the p-type Ga_N layer 16 and gate contact 19, requiring a separate mask for the etching of the doped AlGa_N layer 15. Shealy, ¶278; *Hikita-023*, Figs. 1A, 1B. Thus, *Hikita-023* discloses the steps in [5g]. Shealy, ¶278.

i. [5h]:

**“[5h1] depositing a dielectric layer;
[5h2] applying a contact photo resistant pattern;
[5h3] etching the dielectric layer to open the drain
and source contact area;
[5h4] removing the contact photo resistant pattern;”**

Hikita-023 in view of *Sheppard* renders obvious element [5h]. Shealy, ¶279.

Hikita-023 discloses depositing a dielectric layer, and *Sheppard* renders obvious all steps of [5h]. *Id.*

Hikita-023 discloses forming an “insulating film” over the gate electrode, having “a relative dielectric constant of 4 or lower.” *Hikita-023*, [0030], [0089].

Hikita-023 does not explicitly disclose using a mask (contact photo resistant pattern) to open the drain and source contact area in the dielectric layer, but *Sheppard* discloses steps [5h2], [5h3], [5h4] as explained above in Ground 2. Shealy, ¶281; §VIII.B.2.g. A POSITA would have been motivated to apply *Sheppard*’s drain/source area masking process to form *Hikita-023*’s device and expected success in doing so. §VIII.C.1.d.iii.

j. [5i]:

**“[5i1] depositing ana Ohmic contact metal;
[5i2] applying a fourth photo resistant pattern;
[5i3] etching the Ohmic contact metal
[5i4] removing the fourth photo resistant pattern; and
[5i5] performing rapid thermal annealing to form
Ohmic drain and source contacts.”**

Hikita-023 in view of *Beach* renders obvious element [5i]. Shealy, ¶288.

Hikita-023 discloses depositing a Ti layer and an Al layer (ohmic contact metal) to form a source electrode 17 and a drain electrode 18 (ohmic source and drain contacts). *Hikita-023*, [0079]; Shealy, ¶289.

Hikita-023 discloses performing “thermal treatment (annealing) ... at 650° C” to form the ohmic source and drain contacts. *Hikita-023*, [0079]. Thus, *Hikita-023* discloses performing thermal annealing to form ohmic drain and source contacts. To the extent EPC argues that *Hikita-023* does not explicitly disclose rapid thermal annealing, a POSITA would have found it obvious to perform rapid thermal annealing to form ohmic source and drain contacts in *Hikita-023*’s devices (step [5i5]). Shealy, ¶290. As explained in Ground 1, a POSITA would have been motivated to perform rapid thermal annealing to form ohmic contacts and expected to succeed in doing so. §VIII.A.2.h.

Hikita-023 does not explicitly disclose a masking and etching process for forming the ohmic source and drain contacts, but *Beach* discloses using a masking

and etching process ([5i2], [5i3], [5i4]) to form ohmic contacts as explained in Ground 1. §VIII.A.2.h; *Beach*, [0045]-[0047]. A POSITA would have been motivated to apply *Beach*'s masking process to form *Hikita-023*'s ohmic source and drain contacts and expected success in doing so. §VIII.C.1.d.iv.

IX. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *Fintiv* Denial Is Improper

In view of the Office's interim guidance dated June 21, 2022 ("Interim Procedures"), *Fintiv* does not apply to this case. The Interim Procedures state "the PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding," so the parallel ITC Investigation does not implicate *Fintiv*. Interim Procedures, 7.

Moreover, the *Fintiv* factors in view of the parallel district court action weigh strongly in favor of institution because the district court case has minimal investment from the Court or Parties, does not have a trial date, and has been stayed. *Efficient Power Conversion Corp. v. Innoscience (Zhuhai) Tech. Co.*, No. 2:23-cv-04026, Dkt. 26 (C.D. Cal. July 27, 2023).

B. 35 U.S.C. § 325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017) favor institution.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential).

Under *Advanced Bionics*, step 1, and *Becton, Dickinson* factors (a), (b), and (d), *Yoshida, Beach*, and *Hikita-023* were not before the Examiner in prosecution. Ex. 1002; Ex. 1001. *Hikita-347* and *Sheppard* were of record during prosecution, but there is no evidence the Examiner substantively considered or applied them. Ex. 1001, References Cited; Ex. 1002. Simply citing a reference on an information disclosure statement, with nothing more, does not favor denial of institution. *Navistar, Inc. v. Fatigue Fracture Tech., LLC*, IPR2018-00853, Paper 13 at 16-17 (P.T.A.B. Sept. 12, 2018).

Because the references cited in this Petition are not cumulative of the prosecution prior art, *Becton, Dickinson* factors (c)-(f) are inapplicable. The Examiner allowed the '508 patent without identifying the specific features or limitations that were allowable. Ex. 1002, 103-104 (reciting almost the entire claims 1, 4, and 5 in the Examiner's statement of reasons for allowance). *Yoshida, Beach*, and *Hikita-023* are not cumulative or substantially the same as the art considered during examination because *Yoshida* and *Hikita-023* disclose the structure of the device in claims 1-5, and *Beach* discloses the very single masking process the '508 patent alleged as inventive. §VIII.A.2.f.

X. MANDATORY NOTICES

A. Real Party-in-Interest

The real parties-in-interest are Innoscience (Zhuhai) Technology Company, Ltd., Innoscience America, Inc., and Innoscience (Suzhou) Technology Company, Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '508 patent is involved in:

Name	Number	Court	Filed
<i>Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Company, Ltd. et al.</i>	2:23-cv-04026	C.D. Cal.	May 24, 2023
<i>In the Matter of Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same</i>	337-TA-1366	ITC	May 26, 2023

The '508 patent is related to U.S. Patent Nos. 8,890,168; 8,823,012; 10,312,335; and 9,748,347.

C. Lead and Backup Counsel, and Service Information

Lead Counsel	Backup Counsel
Lionel Lavenue (Reg. No. 46,859) lionel.lavenue@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner LLP	Kara A. Specht (Reg. No. 69,560) kara.specht@finnegan.com Finnegan, Henderson, Farabow, Garrett, & Dunner LLP

1875 Explorer Street, Suite 800 Reston, VA 20190-6023 Tel: 571-203-2750 Fax: 202-408-4400	271 17th Street, NW, Suite 1400 Atlanta, GA 30363-6209 Tel.: 404-653-6481 Fax: 202-408-4400 Cory C. Bell (Reg. No. 75,096) cory.bell@finnegan.com Finnegan, Henderson, Farabow, Garrett, & Dunner LLP 2 Seaport Lane, 6th Floor Boston, MA 02210-2001 Tel.: 617-646-1641 Fax: 202-408-4400 Forrest A. Jones (Reg. No. 74,123) forrest.jones@finnegan.com Finnegan, Henderson, Farabow, Garrett, & Dunner LLP 901 New York Avenue, NW Washington, DC 20001 Tel.: 202-408-4019 Fax: 202-408-4400 Chen Zang (Reg. No. 81,568) chen.zang@finnegan.com Finnegan, Henderson, Farabow, Garrett, & Dunner LLP 901 New York Avenue, NW Washington, DC 20001 Tel.: 202-408-4416 Fax: 202-408-4400 Yi Yu (Reg. No. 69,397) yi.yu@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 1875 Explorer Street, Suite 800, Reston, VA 20190-6023 Tel.: 571-203-2742
--	--

	Fax: 202-408-4400 Luke H. MacDonald (Reg. No. 79,064) luke.macdonald@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 1875 Explorer Street, Suite 800, Reston, VA 20190-6023 Tel.: 571-203-2742 Fax: 202-408-4400 Carlos E. Duarte-Guevara (Reg. No. 80,559) carlos.duarte-guevara@finnegan.com Finnegan, Henderson, Farabow, Garrett, & Dunner LLP 901 New York Avenue, NW Washington, DC 20001 Tel.: 202-408-6013 Fax: 202-408-4400
--	--

D. Service Information

Please address all correspondence to lead and back-up counsel at the addresses shown above and innoscience-epc-ips@finnegan.com. Petitioner also consents to electronic service by email at the above email addresses.

XI. GROUNDS FOR STANDING

Petitioner certifies that the '508 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

XII. CONCLUSION

Petitioner requests institution of *inter partes* review and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 8, 2023

By: Lionel Lavenue/
Lionel Lavenue, Lead Counsel
Reg. No. 46,859

CLAIM APPENDIX

1. **[1pre]** A method of forming an enhancement mode GaN transistor, the method comprising:
 - [1a]** nucleating and growing transition layers on a substrate;
 - [1b]** growing an III Nitride EPI layer over the transistor layers;
 - [1c]** growing an III Nitride barrier layer over the EPI layer;
 - [1d]** growing a GaN layer with acceptor type dopants over the barrier layer;
 - [1e1]** depositing a gate contact layer on the doped GaN layer;
 - [1e2]** applying a gate photo resistant pattern;
 - [1e3]** etching away the gate contact layer outside the gate region;
 - [1e4]** etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
 - [1e5]** removing the gate photo resistant pattern;
 - [1f1]** depositing a dielectric layer;
 - [1f2]** applying a contact photo resistant pattern;
 - [1f3]** etching the dielectric layer to open the drain and source contact area;
 - [1f4]** removing the contact photo resistant pattern;
 - [1g1]** depositing an Ohmic contact metal;
 - [1g2]** applying a metal photo resistant pattern;
 - [1g3]** etching the Ohmic contact metal;

- [1g4] removing the metal photo resistant pattern; and
- [1g5] performing rapid thermal annealing to form Ohmic drain and source contacts.
2. The method of claim 1, wherein the EPI layer is comprised of InAlGaN.
 3. The method of claim 1, wherein the barrier layer is comprised of InAlGaN with a larger band gap than the buffer layer.
 4. [4pre] A method of forming an enhancement mode GaN transistor, the method comprising:
 - [4a] nucleating and growing transition layers on a substrate;
 - [4b] growing an InAlGaN EPI layer over the transistor layers;
 - [4c] growing an InAlGaN barrier layer over the InAlGaN EPI layer;
 - [4d] growing an InAlGaN layer with acceptor type dopants over the InAlGaN barrier layer;
 - [4e] growing a GaN layer with acceptor type dopants over the doped InAlGaN layer;
 - [4f1] depositing a gate contact layer on the doped GaN layer
 - [4f2] applying a gate photo resistant pattern;
 - [4f3] etching away the gate contact layer outside the gate region;

[4f4] etching away the doped GaN layer and the doped InAlGaN layer, except for portions of the doped GaN layer and the doped InAlGaN layer beneath gate contact;

[4f5] removing the gate photo resistant pattern;

[4g1] depositing a dielectric layer;

[4g2] applying a contact photo resistant pattern;

[4g3] etching the dielectric layer to open the drain and source contact area;

[4g4] removing the contact photo resistant pattern;

[4h1] depositing an Ohmic contact metal;

[4h2] applying a metal photo resistant pattern;

[4h3] etching the Ohmic contact metal;

[4h4] removing the metal photo resistant pattern; and

[4h5] performing rapid thermal annealing to form Ohmic drain and source contacts.

5. [5pre] A method of forming an enhancement mode GaN transistor, the method comprising:

[5a] nucleating and growing transition layers on a substrate;

[5b] growing an InAlGaN EPI layer over the transistor layers;

[5c] growing an AlGaN barrier layer over the InAlGaN EPI layer;

- [5d] growing an AlGa_N layer with acceptor type dopants over the AlGa_N barrier layer;
- [5e] growing a Ga_N layer with acceptor type dopants over the doped AlGa_N layer;
- [5f1] depositing a gate contact layer on the doped Ga_N layer
- [5f2] applying a gate photo resistant pattern;
- [5f3] etching away the gate contact layer outside the gate region;
- [5f4] etching away the doped Ga_N layer, except for portions of the doped Ga_N layer and the doped AlGa_N layer beneath gate contact;
- [5f5] removing the gate photo resistant pattern;
- [5g1] applying another photo resistant pattern;
- [5g2] etching the doped AlGa_N layer such that the doped AlGa_N extends outside the gate region towards the drain;
- [5g3] removing the photo resistant pattern;
- [5h1] depositing a dielectric layer;
- [5h2] applying a contact photo resistant pattern;
- [5h3] etching the dielectric layer to open the drain and source contact area;
- [5h4] removing the contact photo resistant pattern;
- [5i1] depositing an Ohmic contact metal;
- [5i2] applying a fourth photo resistant pattern;

[5i3] etching the Ohmic contact metal

[5i4] removing the fourth photo resistant pattern; and

[5i5] performing rapid thermal annealing to form Ohmic drain and source contacts.

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under § 42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,942.

Dated: September 8, 2023

By: /Lionel Lavenue/
Lionel Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), the undersigned certifies that on September 8, 2023, a copy of the foregoing Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1037 were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's Patent Center website for the '508 patent:

Dipu Doshi
Blank Rome LLP
1825 Eye Street, NW
Washington, DC 20006-5403

Date: September 8, 2023

By: /Lisa C. Hines/
Lisa C. Hines
Senior Litigation Legal Assistant
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, LLP