

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY AND

INNOSCIENCE AMERICA, INC.,

Petitioner

v.

EFFICIENT POWER CONVERSION CORPORATION,

Patent Owner

Case No. IPR2023-01383

U.S. Patent No. 8,404,508

DECLARATION OF JAMES RICHARD SHEALY, PH.D.

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I. INTRODUCTION

1. I have been retained by Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively “Innoscience”), as an independent expert for the above-identified *inter partes* review proceeding involving U.S. Patent No. 8,404,508 (“the ’508 patent”).

2. I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

3. Although I am being compensated for my time in connection with this IPR at my standard hourly consulting rate and reimbursed for reasonable out-of-pocket expenses, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

4. I have been asked to provide my opinion whether the claims of the ’508 patent would have been obvious to a person of ordinary skill in the art at the time of the earliest claimed priority date of the ’508 patent. In performing my analysis, I have been asked to assume that the priority date is April 8, 2009. My opinions are set forth below.

5. Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not intended to suggest that they are the only support for the propositions for which they are cited.

II. SUMMARY OF OPINIONS

6. This declaration considers claims 1-5 of the '508 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

7. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of April 8, 2009), it is my opinion that claims 1-5 of the '508 patent would have been obvious based on the asserted grounds discussed below.

III. QUALIFICATIONS AND BACKGROUND

8. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A.

9. I am competent to write this Declaration.

10. I have been involved in the science and engineering of high-power compound semiconductor transistors for over 40 years. I have been deeply involved in the research and design of III-V compound semiconductor devices over the course of my career. I have been a Professor at Cornell University, School of Electrical and Computer Engineering, and have been teaching and conducting research at Cornell since 1987. In 2022, I was granted emeritus status.

11. I received a B.S. degree from North Carolina State University in 1978, an M.S. from Rensselaer Polytechnic Institute in 1980, and a Ph.D. in 1983 from Cornell University. I joined the Cornell faculty in 1987 and am currently a Full Professor in the School of Electrical and Computer Engineering.

12. In 1978, I joined the technical staff of General Electric's Corporate Research and Development Center under an Edison Fellowship. While there, among other work, I developed GaAs epitaxial materials for high voltage electronics. I was the inventor of two patents on Vertical Field Effect Transistors.

13. In 1980, I transferred to General Electric's Advanced Electronics Laboratory where I developed materials and processes for the fabrication of AlGaAs LEDs as well as developing an OMVPE (also known as MOCVD) reactor and related processes for the fabrication of AlGaAs quantum well laser diodes. In 1985, I was designated Principle Staff Scientist at General Electric in recognition of my research contributions.

14. For a portion of my time at General Electric I was also concurrently working at Cornell. In 1984, my group at Cornell developed the first single quantum well red laser by Organometallic Vapor-Phase Epitaxy ("OMVPE"), a technique used for growing semiconductor crystals. The fabrication of these devices involved multi-level metallization and dielectric passivation.

15. I joined the Cornell faculty in 1987 as a Professor of Electrical and Computer Engineering (ECE) and Materials Science and Engineering (MSE).

While at Cornell I have continued my research in OMVPE, particularly as it relates to high frequency transistors, LEDs, and laser diodes. I have also researched GaN and related materials for both high-power transistors and LEDs.

16. In 1997, I was named the Director of Cornell's Optoelectronics Technology Center. In 1998, I was promoted to full professor at Cornell. I have published over 120 articles and am the inventor of over 19 patents, many of which deal with GaN-based materials and devices. Over the years, I have received numerous teaching awards for delivering quality instruction to undergraduates in Materials Science and Electrical Engineering.

17. In 1998-99, the research group that I led invented and patented a single temperature method for nucleation and growth of GaN materials on sapphire, SiC, and Si substrates. This technique has become the preferred method for growing GaN-based transistors and LED today. This nucleation method was used to grow AlN/GaN layers on silicon. By mid-1999, my research group had produced a gallium nitride-on-silicon (GaN-Si) RF transistor, a technology currently used by several GaN companies for high efficiency power convertors and RF amplifiers.

18. By the early 2000s, my research group produced the first RF integrated circuits with gallium nitride-on-silicon carbide (GaN on SiC) transistors including X Band VCOs, TR switches, frequency doublers, and internally matched power amplifiers. By 2008, my group discovered a new passivation technology (LPCVD of AlSiN, patented) for GaN-based FETs which, when applied to GaN SiC HEMTs, produced the largest power density operation (over 18 Watts/mm at 10 GHz) ever observed on submicron gated devices. These devices also delivered record power-added-efficiencies and linear gain during 10 GHz operation (PAE > 65 %, Gain > 36 dB at 60 V bias). These benchmarks remain unchallenged today.

19. In 2015, I cofounded Akoustis Technology (AKTS on the NASDAQ), a company which manufactures AlN bulk acoustic wave filters which are required for 5G communications. In 2019, I cofounded Odyssey Semiconductor, a company which is developing GaN Vertical field effect transistors for the emerging power convertor market. Odyssey Semiconductor also recently developed the fabrication techniques and built micro-LED Arrays in both AlGaInP and AlGaInN materials.

20. I have remained current in the field, as evidenced by my publications listed in my curriculum vitae.

21. I have also served as an expert in certain legal proceedings relating to GaN transistors, including materials growth, device fabrication, and packaging. A

list of cases in which I have testified at trial, hearing, or by deposition is provided in my curriculum vitae.

IV. MATERIALS CONSIDERED

22. In forming my opinions, I have reviewed the following documents and any other documents cited in this declaration:

Exhibit	Description
Ex. 1001	U.S. Patent No. 8,404,508 to Lidow et al. (“the ’508 patent”)
Ex. 1002	Prosecution History of the ’508 patent (downloaded from Public PAIR)
Ex. 1004	Japanese Patent Application Publication No. JPH11261053A to Yoshida, published September 24, 1999 (“ <i>Yoshida</i> ”), including certified English translation and certification
Ex. 1005	International Publication No. WO 2005/057624 to Beach, published June 23, 2005 (“ <i>Beach</i> ”)
Ex. 1006	U.S. Patent No. 7,238,560 to Sheppard et al., published July 3, 2007 (“ <i>Sheppard</i> ”)
Ex. 1007	U.S. Patent Application Publication No. 2006/0273347 to Hikita et al., published December 7, 2006 (“ <i>Hikita-347</i> ”)
Ex. 1008	U.S. Patent Application Publication No. 2008/0079023 to Hikita et al., published April 3, 2008 (“ <i>Hikita-023</i> ”)
Ex. 1009	U.S. Patent Application Publication No. 2007/0007547 to Beach, published January 11, 2007 (“ <i>Beach-547</i> ”)
Ex. 1010	X. Hu et al., “Enhancement mode AlGa _N /Ga _N HFET with selectively grown <i>pn</i> junction gate,” Electronics Letters, vol. 36, no. 8, April 2000, pp. 753-754 (“ <i>Hu</i> ”)
Ex. 1011	Excerpts from Sorab K. Ghandhi, “VLSI Fabrication Principles” (2d ed. 1994) (“ <i>Ghandhi</i> ”)
Ex. 1012	C. S. Suh et al., “p-GaN/AlGa _N /Ga _N Enhancement-Mode HEMTs,” 2006 64th Device Research Conference, June 2006, pp. 163-164 (“ <i>Suh</i> ”)
Ex. 1013	Japanese Patent Application Publication No. JP 2007-066979A to Iwatani et al., published March 15, 2007 (“ <i>Iwatani</i> ”), including certified English translation and certification

Exhibit	Description
Ex. 1014	S.-H. Jang et al., “High-quality GaN/Si(111) epitaxial layers grown with various Al _{0.3} Ga _{0.7} N/GaN superlattices as intermediate layer by MOCVD,” Journal of Crystal Growth, vol. 253, nos. 1-4, June 2003, pp. 64-70 (“ <i>Jang</i> ”)
Ex. 1015	E. Feltin et al., “Crack-Free Thick GaN Layers on Silicon (111) by Metalorganic Vapor Phase Epitaxy,” Physical Status Solidi A., vol. 188, no. 2, November 2001, pp. 531-535 (“ <i>Feltin</i> ”)
Ex. 1016	U.S. Patent No. 5,223,724 to Green, published June 29, 1993 (“ <i>Green</i> ”)
Ex. 1017	U.S. Patent No. 6,211,000 to Spikes et al., published April 3, 2001 (“ <i>Spikes</i> ”)
Ex. 1018	U.S. Patent No. 5,225,360 to Shim et al., published July 6, 1993 (“ <i>Shim</i> ”)
Ex. 1019	U.S. Patent Application Publication No. 2005/0133818 to Johnson et al., published June 23, 2005 (“ <i>Johnson</i> ”)
Ex. 1020	U.S. Patent Application Publication No. 2007/0228416 to Chen et al., published October 4, 2007 (“ <i>Chen</i> ”)
Ex. 1021	M. Shimizu et al., “p-Type InGa _N Cap Layer for Normally Off Operation in AlGa _N /Ga _N Heterojunction Field Effect Transistors,” Japanese Journal of Applied Physics, vol. 47, no. 4, April 2008, pp. 2817-2819 (“ <i>Shimizu</i> ”)
Ex. 1022	U.S. Patent Application Publication No. 2009/0042344 to Ye et al., published February 12, 2009 (“ <i>Ye</i> ”)
Ex. 1023	U.S. Patent No. 6,316,793 to Sheppard et al., published November 13, 2001 (“ <i>Sheppard-793</i> ”)
Ex. 1024	U.S. Patent Application Publication No. 2008/0073652 to Sugimoto et al., published March 27, 2008 (“ <i>Sugimoto</i> ”)
Ex. 1025	C.-F. Zhu et al., “Effects of Rapid Thermal Annealing on the Structural Properties of GaN Thin Films,” IEEE Transactions on Electron Devices, vol. 48, no. 6, June 2001, pp. 1225-1230 (“ <i>Zhu</i> ”)
Ex. 1026	Excerpts from Stephen A. Campbell, “The Science and Engineering of Microelectronic Fabrication” (2d ed. 1994) (“ <i>Campbell</i> ”)
Ex. 1027	A.R. Woll et al., “GaN Nucleation and Growth on Sapphire (0001): Incorporation and Interlayer Transport,” Physical Review Letters, vol. 83, no. 21, November 1999, pp. 4349-4352 (“ <i>Woll</i> ”)
Ex. 1028	J.A. Smart et al., “AlGa _N /Ga _N heterostructures on insulating AlGa _N nucleation layers,” Applied Physics Letters, vol. 75, no. 3, July 1999, pp. 388-390 (“ <i>Smart</i> ”)

Exhibit	Description
Ex. 1029	Y. Liu et al., “Demonstration of undoped quaternary AlInGa _N /Ga _N heterostructure field-effect transistor on sapphire substrate,” <i>Applied Physics Letters</i> , vol. 86, May 2005, 223510 (“ <i>Liu</i> ”)
Ex. 1030	O. Ambacher et al., “Pyroelectric properties of Al(In)Ga _N /Ga _N hetero- and quantum well structures,” <i>Journal of Physics: Condensed Matter</i> , vol. 14, March 2002, 3399-3434 (“ <i>Ambacher</i> ”)
Ex. 1031	Taiwanese Patent Application Publication No. TW200414540 A to Sheu et al., published August 1, 2004 (“ <i>Sheu</i> ”), including certified English translation and certification
Ex. 1032	Japanese Patent Application Publication No. JP 2007109830A to Mizutani et al., published April 26, 2007 (“ <i>Mizutani</i> ”), including certified English translation and certification
Ex. 1033	U.S. Patent No. 6,897,514 to Kouznetsov et al., published May 24, 2005 (“ <i>Kouznetsov</i> ”)
Ex. 1034	U.S. Patent Application Publication No. 2006/0006500 to Piner et al., published January 12, 2006 (“ <i>Piner</i> ”)
Ex. 1035	V. Kumar et al., “Field-Plated 0.25- μ m Gate-Length AlGa _N /Ga _N HEMTs With Varying Field-Plate Length,” <i>IEEE Transactions on Electron Devices</i> , vol. 53, no. 6, June 2006, pp. 1477-1480 (“ <i>Kumar</i> ”)
Ex. 1036	W. Saito et al. “Design and Demonstration of High Breakdown Voltage Ga _N High Electron Mobility Transistor (HEMT) Using Field Plate Structure for Power Electronics Applications,” <i>Japanese Journal of Applied Physics</i> , vol. 43, no. 4B, April 2004, pp. 2239-2242 (“ <i>Saito</i> ”)
Ex. 1037	U.S. Patent Application Publication No. 2006/0060895 to Hikita et al., published March 23, 2006 (“ <i>Hikita-895</i> ”)

23. I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

V. LEGAL STANDARDS

24. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel

for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

25. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

26. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

27. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-5 of the '508 patent from the perspective of a person of ordinary skill in the art at the '508 patent's earliest claimed priority date in 2009, as described in more detail below.

28. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving

unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

29. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill in the Art

30. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

31. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Claim Construction

32. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent (Ex. 1002). I understand that, like the claims and written description, the prosecution history provides

evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term's plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent's written description, the patent's prosecution history, or both.

33. I understand that claim interpretation may also be informed by “extrinsic evidence” (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a POSITA in the relevant time period.

34. I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '508 patent.

35. Based on my review of these materials and my personal knowledge and experience, I have considered the plain and ordinary meaning of each term of the '508 patent as it would have been understood by one skilled in the art at the

earliest claimed priority date of the '508 patent of April 8, 2009. I apply the plain and ordinary meaning of each claim term throughout this declaration.

C. Anticipation

36. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

37. I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

38. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;

- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

39. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is April 8, 2009. My opinions would not change if I assumed a later date of invention.

40. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

41. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that

the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

42. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;

- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

43. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of

ordinary skill in the art would have had a good reason to pursue those known options.

44. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

45. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

46. I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '508 patent.

47. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE PRIOR ART

A. Gallium Nitride (GaN) Transistors

48. Gallium Nitride (GaN) and related materials were used in semiconductor transistor devices long before the earliest claimed priority date of the '508 patent, April 8, 2009. GaN is a III Nitride (III-N) material, a class of semiconductors that combine a group III element (e.g., indium or gallium) with nitride. It was well known that GaN material exhibits a large band gap. Because of this property, GaN transistors have a higher breakdown voltage, making them attractive for high power applications. Ex. 1001, 1:22-26 (background); *Hikita*-347, [0004].

49. It was also common to form layers of different materials on a substrate to produce a GaN transistor that has high electron mobility, which is often referred to as high electron mobility transistors (HEMT) or heterojunction field effect transistors (HFET). *Hikita-347*, [0004]; Ex. 1001, 1:22-42 (background). For example, an **AlGa**N/**GaN** heterostructure was widely used to form a HEMT device before the '508 patent was filed, as shown below. *Hu*, 1.

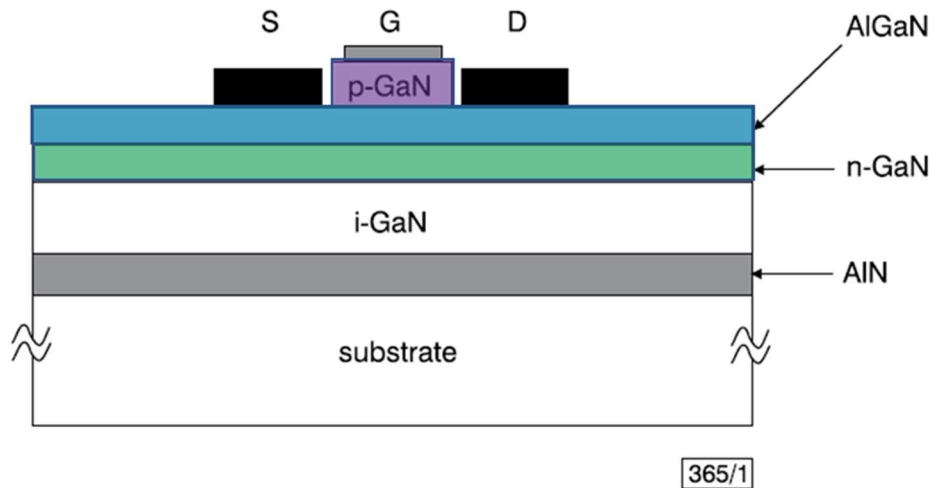


Fig. 1 Schematic diagram of structure of pn junction regrown gate HFET

Hu, Fig. 1 (annotated).

50. An enhancement mode GaN transistor refers to a GaN transistor that is normally off. *Hikita-023*, [0006]. As shown above, an enhancement mode GaN transistor can be formed by including a p-type GaN (**p-GaN**) layer under the gate, such that a drain current does not flow when no gate voltage is applied. *Hu*, Fig. 1; *Hikita-023*, [0007]-[0008]. Such enhancement mode GaN transistors were known long before the '508 patent was filed. *Hu*, 1-2. Indeed, as discussed below, the '508

patent itself admits that enhancement mode GaN transistors were conventional and known in the prior art.

B. Fabrication of GaN Transistors with Photo Masks

51. Using photo masks to control physical dimensions and patterns of structures is a fundamental step in the manufacturing of any semiconductor device. The photo mask technique was adopted to produce various semiconductor devices decades before the '508 patent was filed.

52. The conventional masking process involves three steps:

53. First, a **mask**, also called a photo resistant pattern, is formed on a semiconductor structure, as shown in *Ghandhi*, Figure 10.6(e). *Ghandhi*, 10-12; *see also Campbell*, 4. The **mask** (photo resistant pattern) may leave a certain area open on the surface. *Ghandhi*, 10; *see also Campbell*, Fig. 1.5(5).

54. Second, the structure is etched to remove parts of the material that is not covered by the mask, as shown in *Ghandhi*, Figure 10.6(f). *Ghandhi*, 12; *see also Campbell*, 4-5. The material covered by the mask is not affected by the etching process. *Ghandhi*, 12; *see also Campbell*, 4.

55. Finally, the mask is removed, and the structure is subject to the next step of processing, as shown in *Ghandhi*, Figure 10.6(g). *Ghandhi*, 12; *see also Campbell*, 4.

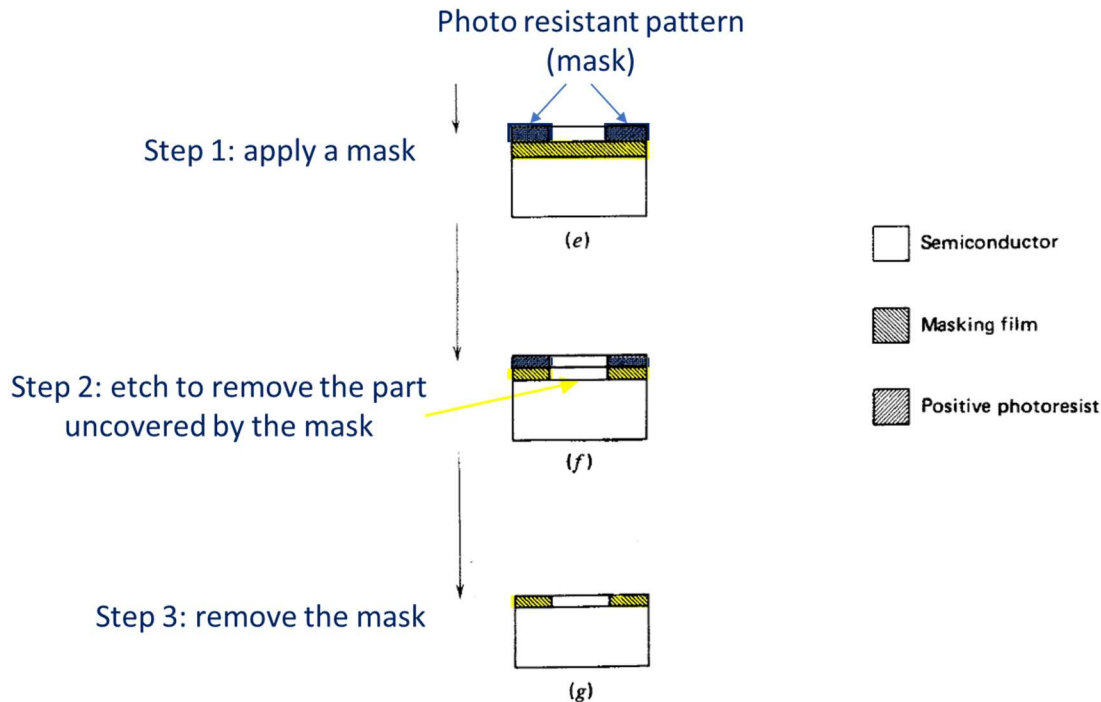


Fig. 10.6 Steps in opening a window in a masking film, using positive photoresist.

Ghandhi, Fig. 10.6 (annotated).

56. The same masking process was used to form GaN transistors years before the '508 patent. For example, masks were commonly used to form the Ohmic contact, the doped GaN layer, and the gate contact of GaN transistors. *Yoshida*, [0022]-[0023]; *Sheppard*, 8:55-63, 9:26-34; *Beach*, [0047].

C. Self-Aligned Gate and P-GaN Layer

57. In forming the GaN transistors, it is desired that the gate and p-GaN layer are self-aligned, such that the cost of applying a second mask to etch the p-GaN or gate can be avoided. GaN transistors with self-aligned gate and p-GaN layer were well known, and an example is shown below, where the gate and p-GaN

layer are perfectly aligned by using the gate as a mask to etch the p-GaN layer.

Suh, 1. See also *Iwatani*, Fig. 4.

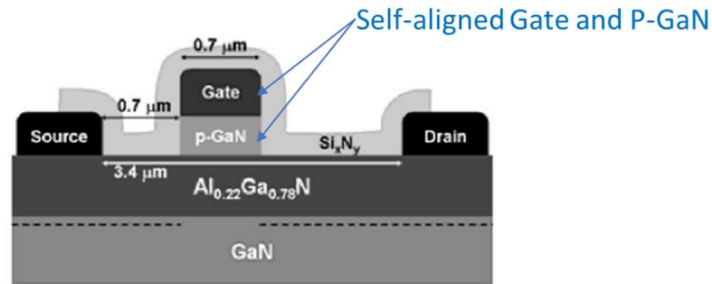
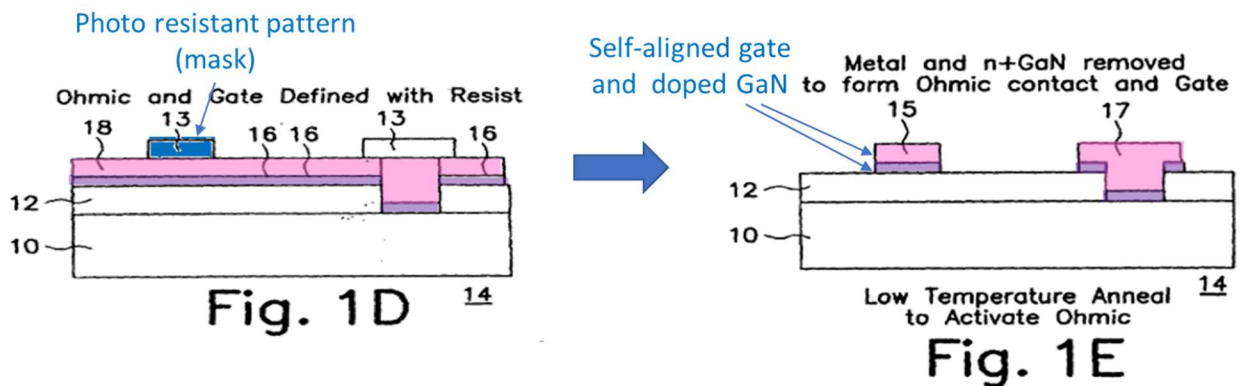


Fig. 1: Schematic cross section of the p-GaN/AlGaIn/GaN E-mode HEMT.

Suh, Fig. 1 (annotated).

58. It was also known to use a single mask to etch the gate and doped GaN material to form the self-aligned gate and doped GaN layer in GaN transistors. This figure below shows an example of a single mask applied to form self-aligned gate and doped GaN. *Beach*, [0047]. The single mask technique achieves the self-alignment between the gate and doped GaN layer and saves manufacturing cost.



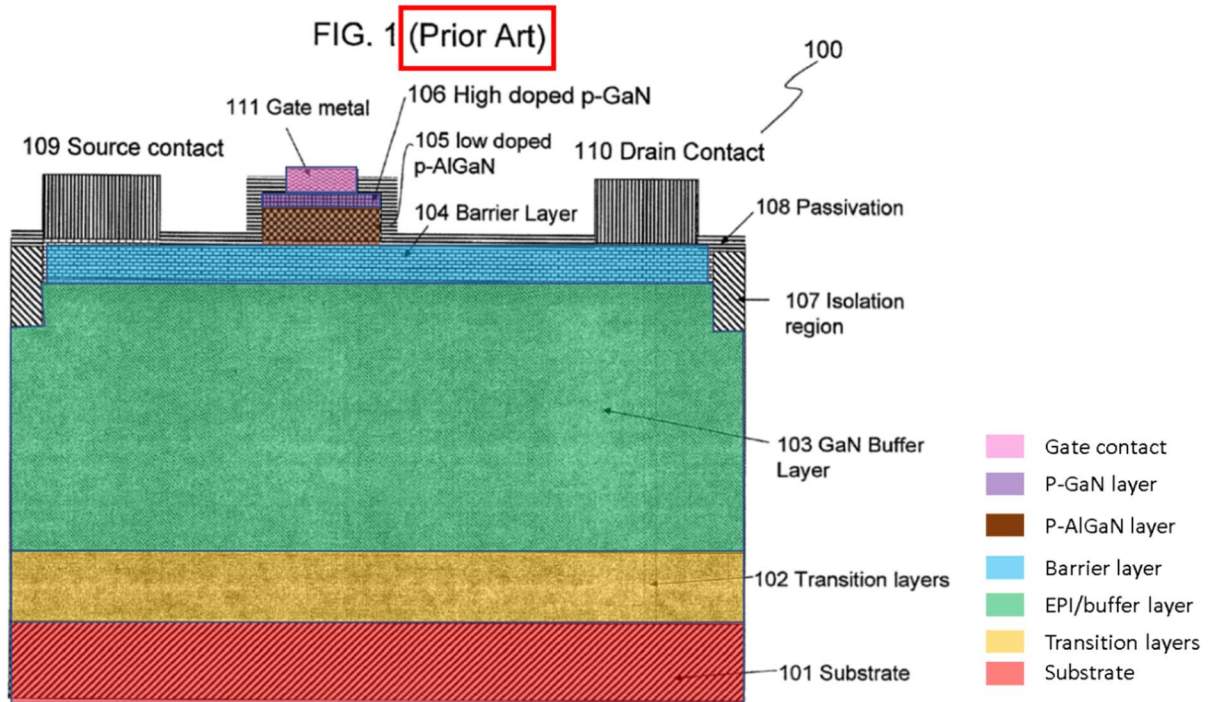
Beach, Figs. 1D, 1E (annotated).

VII. THE '508 PATENT

A. Overview of the '508 Patent

59. The '508 patent is directed to “[a]n enhancement-mode GaN transistor and a method of forming it.” Ex. 1001, Abstract.

60. The '508 patent admits that all of the various layers grown on a substrate to form an enhanced mode GaN transistor in all of its embodiments were “conventional” and known in the “prior art.” Ex. 1001, 1:32-64. This conventional transistor included conventional layers like the **substrate**, **transition layers**, **GaN buffer layer**, **AlGaN barrier layer**, and **p-type GaN layer**, the optional additional **p-type AlGaN layer** relevant to claims 4 and 5, as well as the source and drain contact and the **gate metal** formed on the device. Ex. 1001, 1:32-64. This is illustrated by the comparison of “prior art” figure 1 with embodiment in figure 2 shown below.



Ex. 1001, Fig. 1 (annotated).

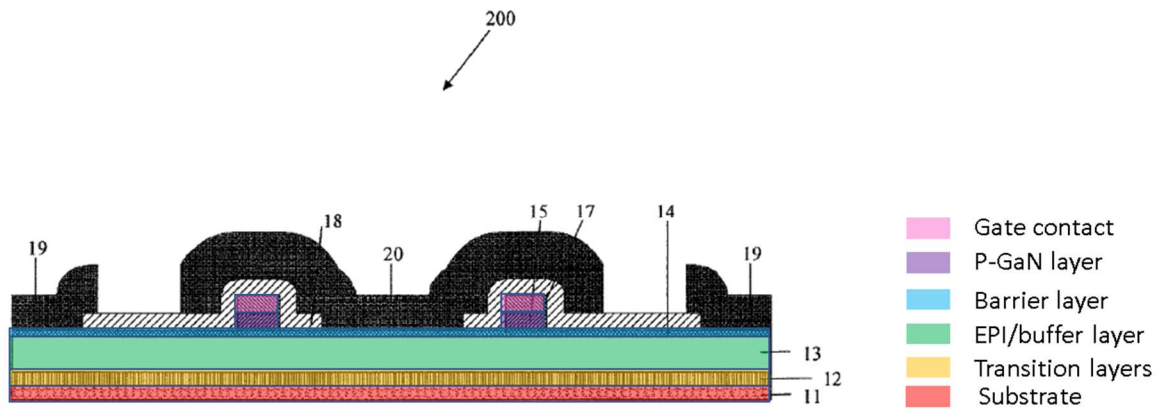
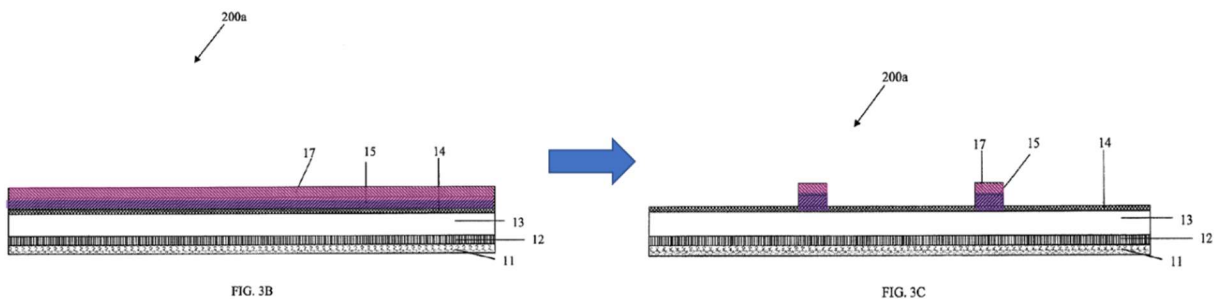


FIG. 2

Ex. 1001, Fig. 2 (annotated).

61. The '508 patent explains that, in the conventional enhancement mode GaN transistor illustrated above, the **gate metal 111** and the **p-type GaN 106** or **p-type AlGaN 105** material underneath the gate metal are defined by “two different photo masks,” where the **first mask** is used to form the **p-type GaN 106** or **p-type AlGaN 105**, and the **second mask** is used to form the **gate metal 111**. Ex. 1001, 1:53-57, 1:65-2:5, Fig. 1. The '508 patent identifies several disadvantages with the “two mask process,” such as a wider gate length, high gate charge, and increased manufacturing costs. Ex. 1001, 2:5-13.

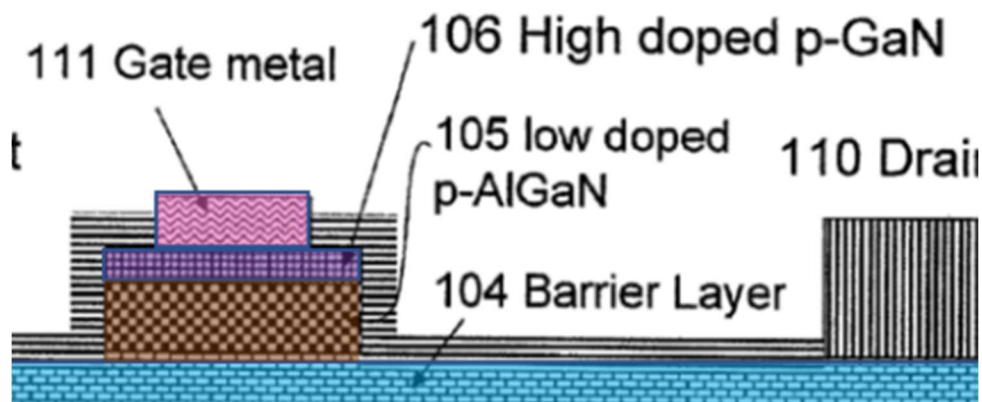
62. The '508 patent aims to solve this problem by patterning and etching the gate metal material and the p-type GaN material (and also the p-type AlGaN material in some embodiments) material “using a single photo mask.” Ex. 1001, 3:1-6. Figure 3B illustrates the structure with **gate metal 17** and **p-type GaN layer 15** before the single photo mask is applied, and Figure 3C illustrates the structure after using the single photo mask to etch the **gate metal 17** and **p-type GaN layer 15**. Ex. 1001, 3:39-50.



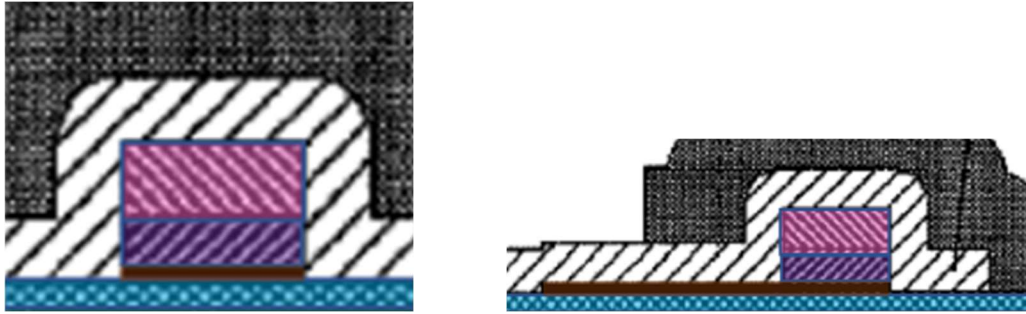
Ex. 1001, Figs. 3B and 3C (annotated).

63. The '508 patent explains that the single mask process renders the gate metal and p-type GaN material “automatically self-aligned” and “reduces manufacturing cost.” Ex. 1001, 4:6-9. The single mask process and the resultant structure of the enhancement mode GaN transistor, however, were already taught by the prior art.

64. The '508 patent also describes that, in two separate embodiments relevant to claims 4 and 5, the structure of the enhancement mode GaN transistor includes an additional layer of **p-type AlGaN material** below the p-type GaN layer. Ex. 1001, 4:25-27, 4:60-64, Figs. 4, 6. But this additional structure was also admittedly prior art by the '508 patent and was also taught by the prior art. Ex. 1001, 1:55-64, Fig. 1. This is illustrated by the comparison of “prior art” figure 1 with embodiments in figures 4 and 6 shown below.



Ex. 1001, Fig. 1. (Prior art, annotated)



Ex. 1001, Figs. 4, 6 (cropped and annotated).

65. For figures 4 and 5, relevant to claim 4, the '508 patent explains the same “single mask” process is used to etch the gate metal, p-type GaN material, and p-type AlGaN material, similarly resulting in a self-aligned gate stack “with the same advantages as the first embodiment.” Ex. 1001, 4:20-59, Figs. 5B-5C. For figures 6 and 7, relevant to claim 5, the '508 patent explains the same “single mask” process is used to etch the gate metal, p-type GaN material, with a separate mask being used to etch the p-type AlGaN material so it can extend beyond the gate region, but that the gate metal and p-type GaN are still “self-aligned.” Ex. 1001, 4:60-5:22, Figs. 7B-7D.

B. Summary of the Prosecution History of the '508 Patent

66. The application that issued as the '508 patent was filed on April 8, 2010, claiming priority to a provisional application filed on April 8, 2009. Ex. 1001, cover.

67. After the applicant elected to examine method claims of the application in response to a restriction requirement, the Examiner allowed the

claims. Ex. 1002, 101-104. The Examiner did not identify any particular limitation that renders the application allowable, and instead cited language of almost the entire claims 1, 4, and 5 in the statement of reasons for allowance. Ex. 1002, 103-104.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

68. In rendering the opinions set forth in this declaration, I have been asked to consider the '508 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the art," "skilled artisan," "POSITA," or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

69. Taking the factors described in the Legal Standards – Level of Ordinary Skill in the Art section into consideration, it is my opinion that a person of ordinary skill in the art (POSITA) would have had at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis

of device operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa.

70. Based on my educational background and experience, I was at least a person of ordinary skill in the art at the earliest priority date of the '508 patent.

IX. THE PRIOR ART

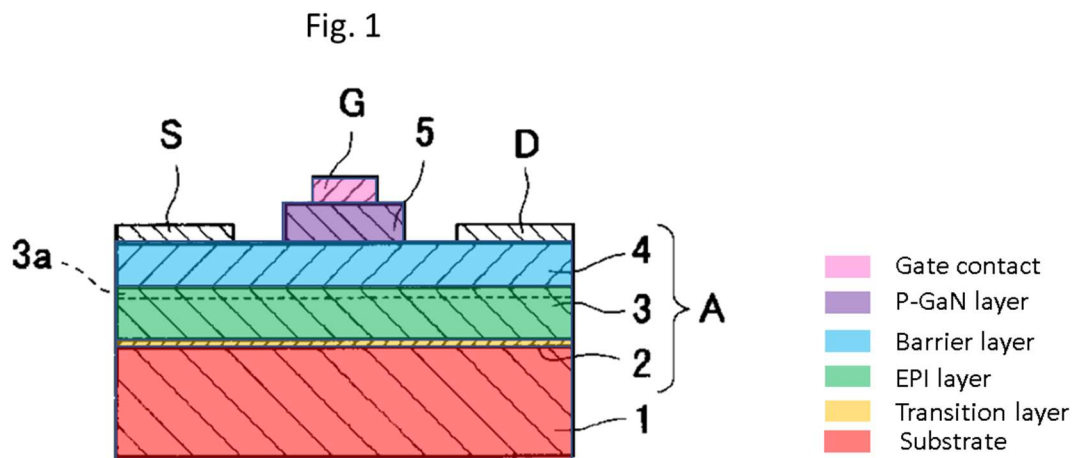
71. In forming my opinions, I found the following prior art relevant when considering whether the claims of the '508 patent would have been obvious to a person of ordinary skill in the art.

- Ex. 1004, Japanese Patent Application Publication No. JPH11261053A to Yoshida (“*Yoshida*”)
- Ex. 1005, International Publication No. WO 2005/057624 to Beach (“*Beach*”)
- Ex. 1006, U.S. Patent No. 7,238,560 to Sheppard et al. (“*Sheppard*”)
- Ex. 1007, U.S. Patent Publication No. 2006/0273347 to Hikita et al. (“*Hikita-347*”)
- Ex. 1008, U.S. Patent Publication No. 2008/0079023 to Hikita et al. (“*Hikita-023*”)

A. *Yoshida* (JPH11261053A)

72. *Yoshida* was published September 24, 1999 as Japanese Patent Application Publication No. JPH11261053A, making *Yoshida* prior art.

73. *Yoshida*, like the '508 patent, discloses a GaN high electron mobility transistor device and a method for providing such a device, and is thus analogous art to the '508 patent. *Yoshida*, [0001], [0009], [0010], [0019]-[0023]. *Yoshida* discloses an enhancement mode GaN transistor that includes a **substrate 1**, a **buffer layer 2**, an **i-type GaN layer 3**, a **n-type AlGaIn layer 4**, and a **p-type GaN layer 5**, a **gate contact**, and source and drain contacts—the same layers claimed by the '508 patent, with the sole exception being *Yoshida*'s single depicted buffer layer 2, rather than multiple transition layers. *Yoshida*, Abstract, [0010], [0013], [0015], [0021]. This is illustrated by the comparison of *Yoshida*, figure 1 with the '508 patent, figure 2 shown below.



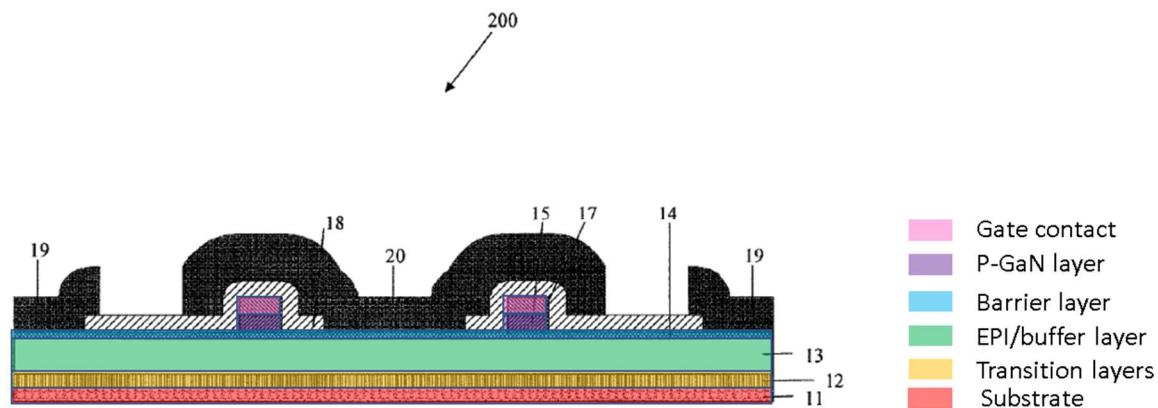


FIG. 2

Ex. 1001, Fig. 2 (annotated).

74. *Yoshida* discloses forming the GaN transistor by the following steps. First, grow epitaxy layers on a substrate, including (1) growing a buffer layer 2 over the substrate 1, (2) growing a i-type GaN layer 3 over the buffer layer 2, (3) growing a n-type AlGaN layer 4 over the i-type GaN layer 3, and (4) growing a p-GaN layer 5 over the n-type AlGaN layer 4. *Yoshida*, [0019]-[0021]. Second, etch away the p-GaN layer except where the gate is to be loaded. *Yoshida*, [0022]. Third, deposit a dielectric layer (SiO_2 film) to cover the entire surface. Fourth, apply a mask and etch the dielectric layer to open the source and drain contact area. *Yoshida*, [0022]. Fifth, deposit the source and drain electrodes on the

“exposed” n-type AlGa_N layer.¹ *Yoshida*, [0013],[0022]. Finally, remove the mask and form the gate contact above the p-GaN layer to produce an enhancement mode GaN transistor. *Yoshida*, [0023].

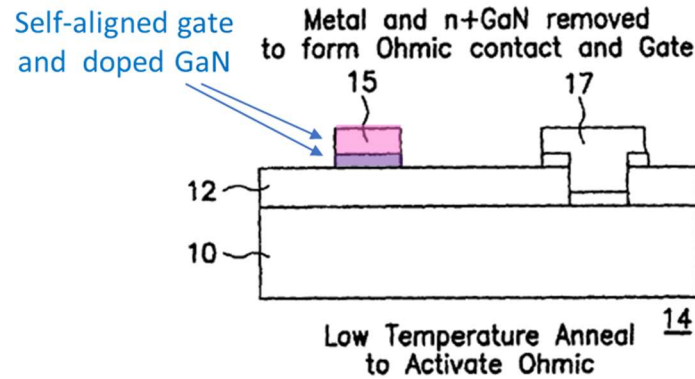
B. *Beach* (WO 2005/057624)

75. *Beach* was published June 23, 2005 as WIPO PCT publication no. WO 2005/057624, making *Beach* prior art.

76. *Beach*, like the '508 patent, discloses a GaN high electron mobility transistor device and using masks to produce such a device, and is thus analogous art to the '508 patent. *Beach*, [0004], [0024], [0040]-[0049], [0062].

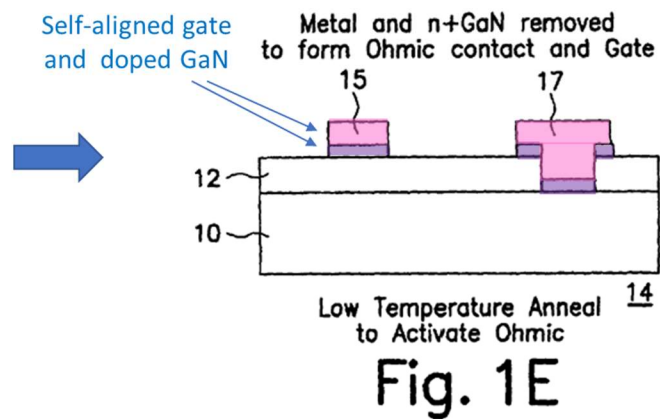
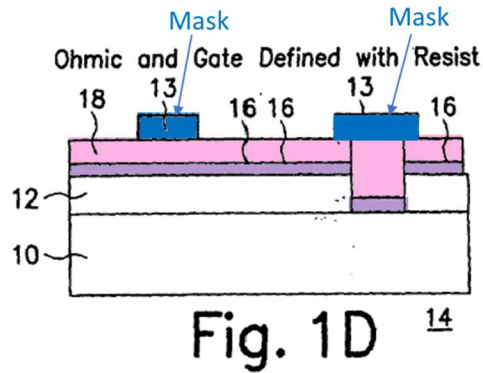
77. *Beach* discloses a GaN transistor with a **gate contact 15** self-aligned with a **doped GaN layer** underneath the gate contact, as shown by figure 1E below. *Beach*, [0047]-[0048]. The depicted GaN transistor also includes an AlGa_N barrier layer 12 and a GaN buffer layer 10 to form a high electron mobility transistor (HEMT), like the device in the '508 patent. *Beach*, [0004], [0039]-[0041].

¹ While *Yoshida* specifies “n-type AlGa_N is favorable,” it also refers to InGa_N for this layer. *Yoshida*, [0013].

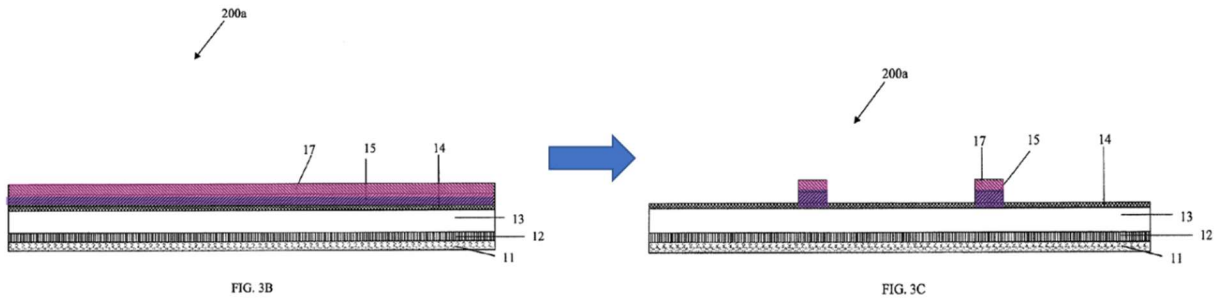


Beach, Fig. 1E (annotated).

78. *Beach* discloses forming the self-aligned gate and doped GaN layer by the following steps. First, grow **doped GaN layer 16** over layers 10 and 12. *Beach*, [0043]-[0044]. Second, deposit **Ohmic material 18** over doped GaN layer 16. *Beach*, [0045]. Third, apply a **photo resistant pattern (mask) 13**, as shown in Figure 1D below. *Beach*, [0047]. Fourth, etch the **Ohmic material 18** and **doped GaN layer 16** using the **photo resistant pattern (mask) 13**, as shown in Figure 1E. *Beach*, [0047], [0049]. Finally, remove the photo resistant pattern (mask) 13, shown in Figure 1E. *Beach*, [0049]. This is the same process claimed in the '508 patent, illustrated by the comparison of *Beach*, figures 1D, 1E with the '508 patent, figures 3B, 3C shown below.



Beach, Figs. 1D, 1E (annotated).



Ex. 1001, Figs. 3B, 3C (annotated).

79. *Beach* also discloses the claimed masking process to form the drain and source contacts. Figure 1D shows applying another **photo resistant pattern (mask) 13** to form the ohmic contact 17 (source/drain contact) then etching the **ohmic material 18** away except where protected by the **photo resistant pattern (mask) 13** to form an ohmic contact 17 (source/drain contact). *Beach*, [0047].

C. *Sheppard* (US 7,238,560)

80. *Sheppard* was published July 3, 2007 as U.S. Patent no. 7,238,560, making *Sheppard* prior art.

81. *Sheppard*, like the '508 patent, discloses a GaN high electron mobility transistor device and a method for providing such a device, and is thus analogous art to the '508 patent. *Sheppard*, 2:30-38, 8:55-9:46. *Sheppard* discloses growing various layers of materials over a substrate to form a GaN transistor, as shown below. *Sheppard*, 6:45-8:54.

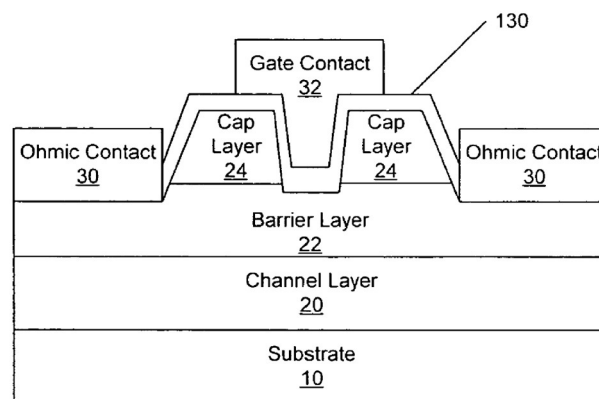


Figure 3

Sheppard, Fig. 3.

82. *Sheppard* discloses that the GaN transistor can include multiple transition layers on the substrate. *Sheppard*, 6:58-7:7, 7:25-32. *Sheppard* explains that the additional transition layers provide an appropriate crystal structure

transition between the substrate and the remainder of the device and also provide a strain balancing effect. *Sheppard*, 6:58-7:7.

83. *Sheppard* further discloses using a mask pattern to form the Ohmic contact of the GaN transistor. *Sheppard* describes providing a **mask 40** and etching the GaN cap layer to open windows for ohmic contacts (source/drain contacts) according to the mask, as shown below. *Sheppard*, 8:55-67.

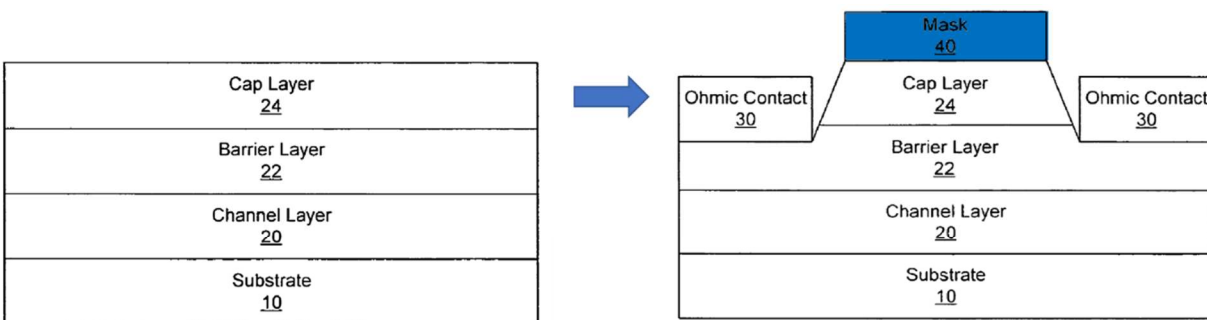


Figure 1B

Figure 1C

Sheppard, Figs. 1B, 1C (annotated).

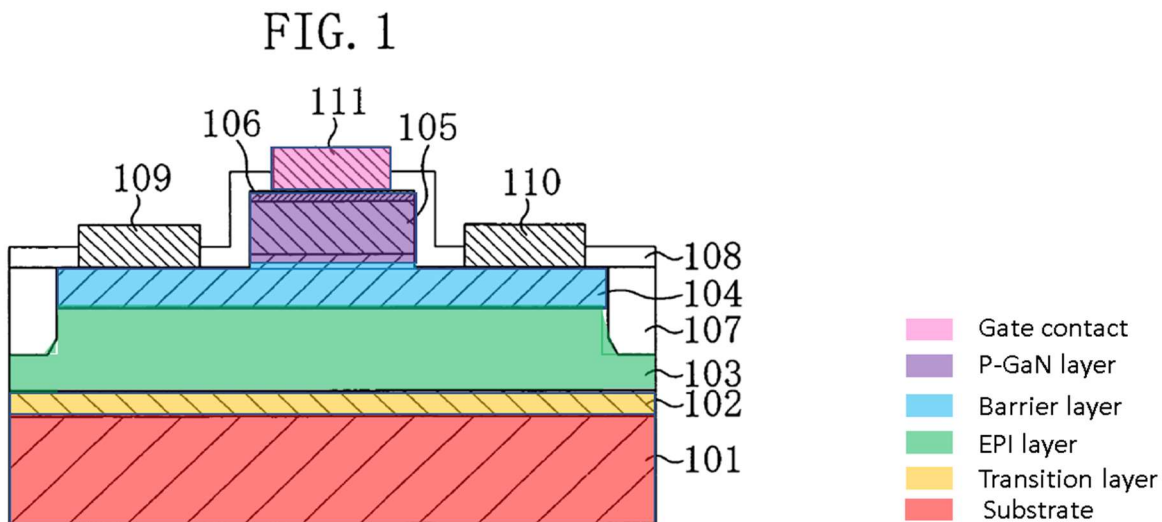
D. *Hikita-347* (US 2006/0273347)

84. *Hikita-347* was published December 7, 2006 as U.S. Patent publication no. 2006/0273347, making *Hikita-347* prior art.

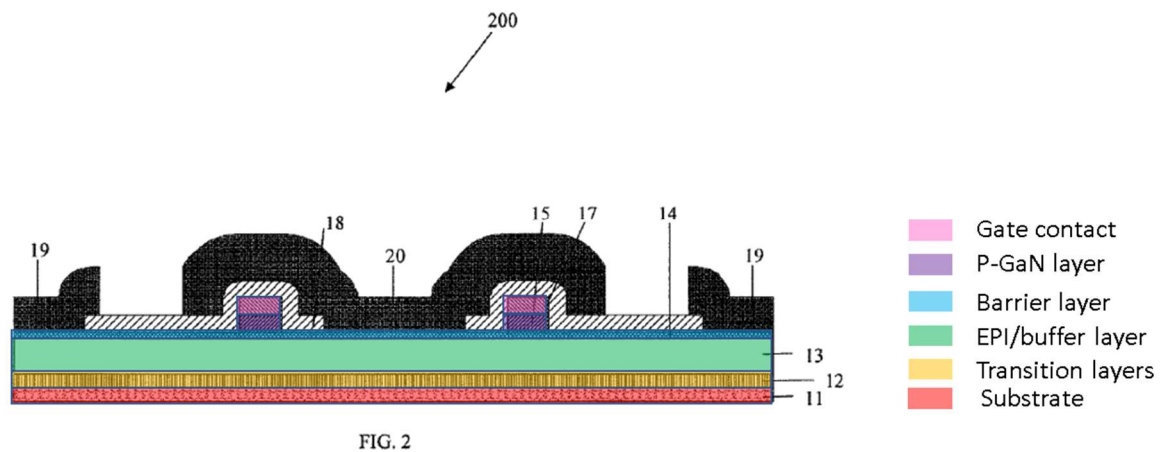
85. *Hikita-347*, like the '508 patent, discloses a GaN high electron mobility transistor device and a method for providing such a device, and is thus analogous art to the '508 patent. *Hikita-347*, [0013], [0033], [0038], [0040], [0055]-[0061]. *Hikita-347* discloses an enhancement mode GaN transistor that

includes a **substrate 101**, a **buffer layer 102**, an **undoped GaN layer 103**, an **undoped AlGaN layer 104**, and a **p-type GaN layer 105**, a **gate contact 111**, and source and drain contacts 109 and 110—the same layers claimed by the '508 patent, with the sole exception being *Hikita-347*'s single depicted buffer layer 102, rather than multiple transition layers. *Hikita-347*, Abstract, [0033]-[0035].

Although Figure 1 shows having a second p-type GaN layer 106 over the p-type GaN layer 105, *Hikita-347* notes that it is not necessary to provide the second p-type GaN layer 106. *Hikita-347*, [0040]. This is illustrated by the comparison of *Hikita-347*, figure 1 with the '508 patent, figure 2 shown below.

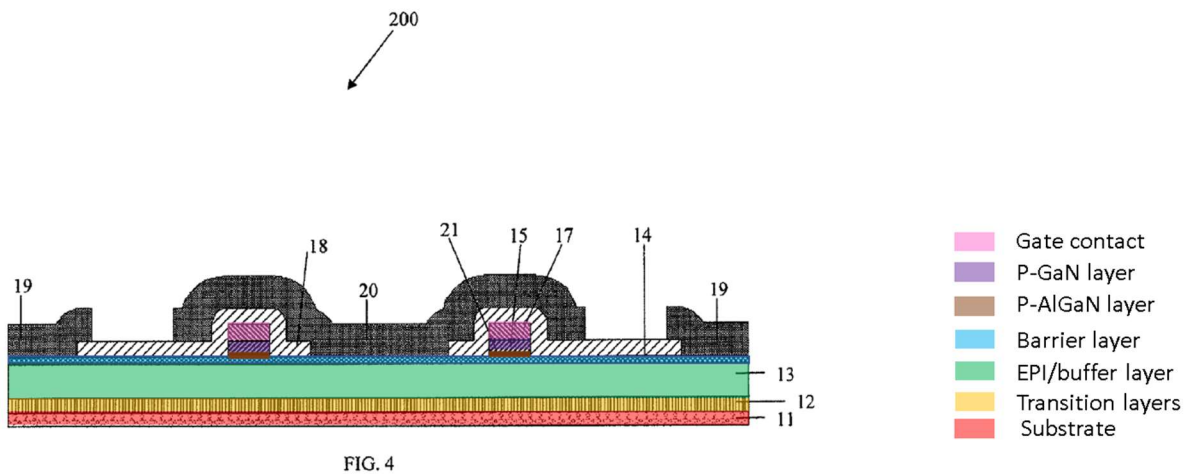
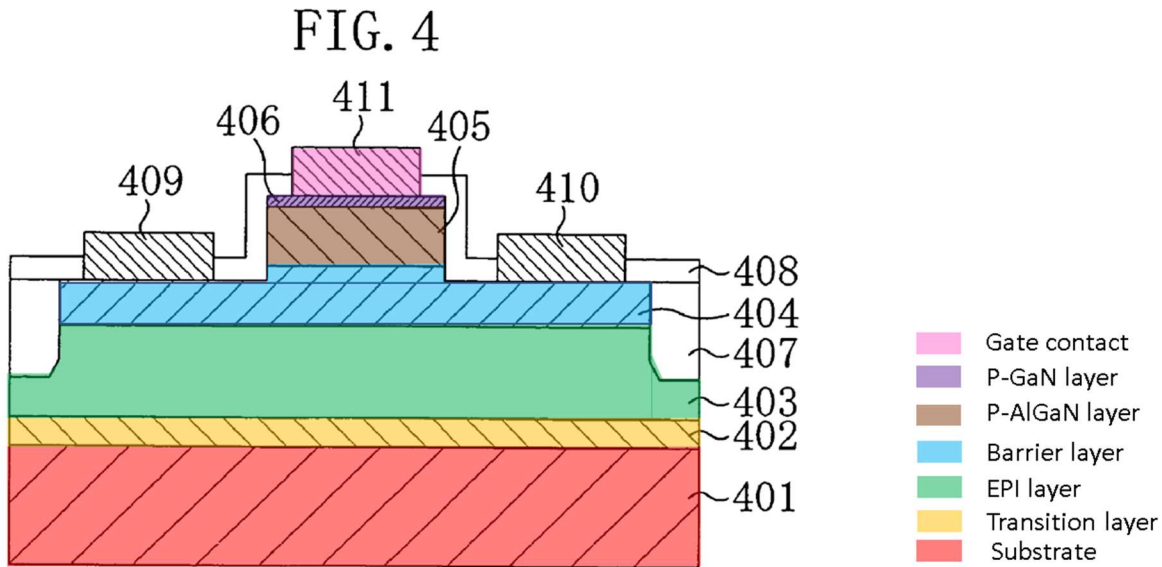


Hikita-347, Fig. 1 (annotated).



Ex. 1001, Fig. 2 (annotated).

86. *Hikita-347* also discloses an enhancement mode GaN transistor that includes a **substrate 401**, a **buffer layer 402**, an **undoped GaN layer 403**, an **undoped AlGaIn layer 404**, a **p-type AlGaIn layer 405**, and a **p-type GaN layer 406**, a **gate contact 111**, and source and drain contacts 409 and 410, the same as the embodiment in the '508 patent, figure 4, as shown below.



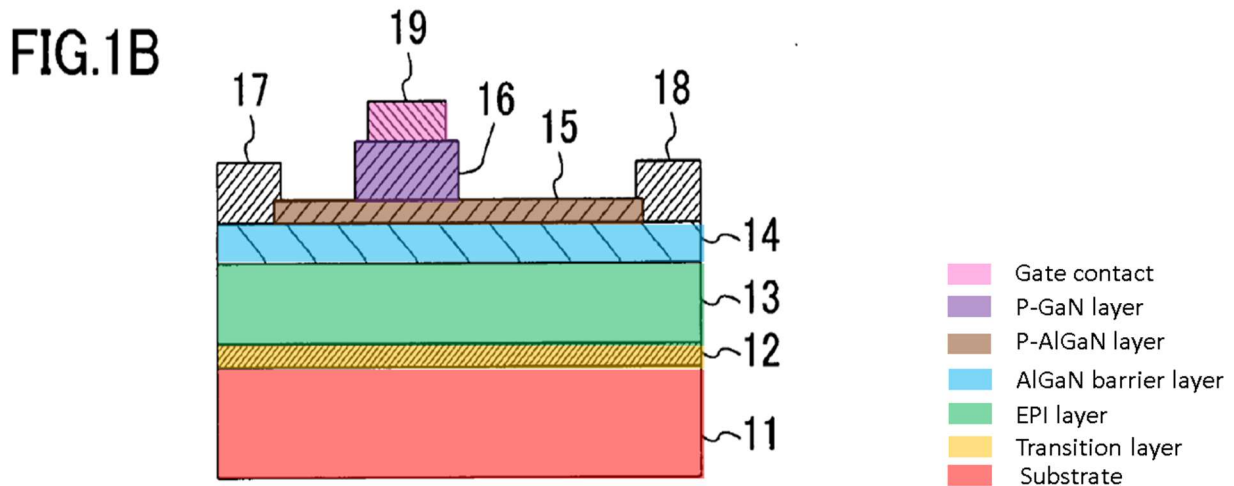
87. *Hikita-347* discloses that the GaN transistor is formed by the following steps. First, epitaxy layers are grown on a **substrate 101/401**, including growing a **buffer layer 102/402** over the substrate, growing **undoped GaN layer 103/403** over the buffer layer, growing an **undoped AlGaIn layer 104/404** over the

undoped GaN layer, and growing a **p-GaN layer 105**, or a **p-type AlGaN layer 405** and a **p-type GaN layer 406** over the undoped AlGaN layer. *Hikita-347*, [0013], [0033], [0056]. Second, the p-GaN layer 105, or p-type AlGaN layer 405 and p-type GaN layer 406 collectively, is etched away in part other than the gate region. *Hikita-347*, [0035], [0057]. Third, a dielectric layer (SiN film) 108 is formed to cover the entire surface with openings formed in the source and drain contact area and the gate area. *Hikita-347*, [0034], [0037], [0059]-[0061]. Finally, the source and drain contacts and the gate contact are formed to produce an enhancement mode GaN transistor. *Hikita-347*, [0013], [0037], [0060]-[0061].

E. *Hikita-023* (US 2008/0079023)

88. *Hikita-023* was published April 3, 2008 as U.S. Patent publication no. 2008/0079023, making *Hikita-023* prior art.

89. *Hikita-023*, like the '508 patent, discloses an enhancement mode GaN transistor that includes a **substrate 11**, a **buffer layer 12**, an **undoped GaN layer 13**, an **undoped AlGaN layer 14**, a **p-type AlGaN layer 15**, and a **p-type GaN layer 16**, a **gate contact 19**, and source and drain contacts 17 and 18, the same as the embodiment in the '508 patent, figure 7F, as shown below. *Hikita-023*, [0051]-[0056].



Hikita-023, Fig. 1B (annotated).

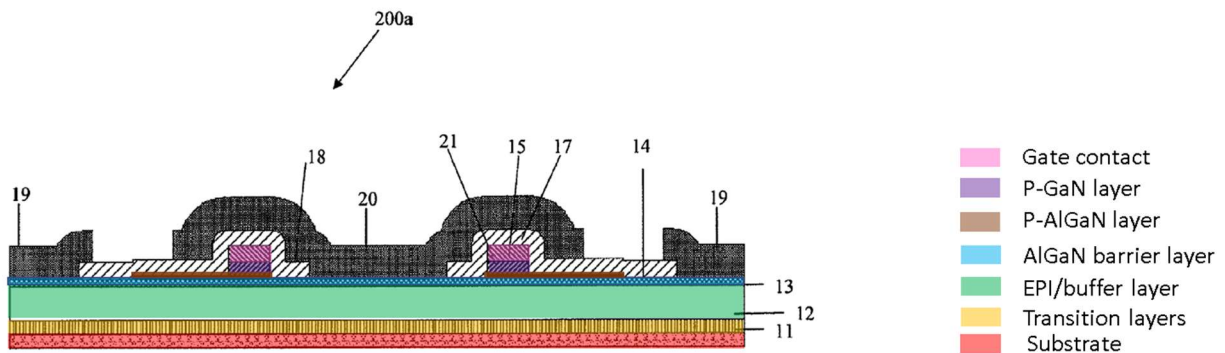


FIG. 7F

Ex. 1001, Fig. 7F (annotated).

90. *Hikita-023* discloses that forming the GaN transistor is formed by the following steps. First, grow epitaxy layers on a substrate, including (1) growing a buffer layer 12 over the substrate 11, (2) growing an undoped GaN layer 13 over the buffer layer 12, (3) growing an undoped AlGaIn layer 14 over the undoped GaN layer 13, (4) growing a p-type AlGaIn layer 15 over the undoped AlGaIn layer

14, and (5) growing a p-type GaN layer 16 over the p-AlGaN layer 15. *Hikita-023*, [0051], [0076]. Second, etch away the p-type GaN layer 16 in part other than the gate region. *Hikita-023*, [0077]. Third, etch the p-type AlGaN layer 15 to form regions for source and drain electrodes. *Hikita-023*, [0057], [0078]. Finally, form the contacts for the source, drain, and the gate to produce an enhancement mode GaN transistor. *Hikita-023*, [0079]-[0080].

X. GROUNDS OF UNPATENTABILITY

91. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my opinion that claims 1-5 of the '508 patent would have been obvious to one of ordinary skill in the art.

92. In particular, it is my opinion that claims 1-5 of the '508 patent is either anticipated or would have been rendered obvious to one of ordinary skill in the art, based on the grounds shown below:

Ground	Challenged Claims	Basis	Prior Art
1	1-3	§ 103 obviousness	<i>Yoshida, Beach, and Sheppard</i>
2	1-4	§ 103 obviousness	<i>Hikita-347, Beach, and Sheppard</i>
3	5	§ 103 obviousness	<i>Hikita-023, Beach, and Sheppard</i>

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

93. In my opinion claims 1-5 would have been obvious to one skilled in the art at the earliest priority date of the '508 patent.

A. Ground 1: Claims 1-3 Are Obvious over *Yoshida*, *Beach*, and *Sheppard*

1. Independent Claim 1

94. In my opinion, the combination of *Yoshida*, *Sheppard*, and *Beach* renders claim 1 obvious.

95. *Yoshida* discloses elements [1pre], [1b], [1c], [1d], and [1f]. *Yoshida* in view of *Sheppard* renders obvious forming multiple transition layers on a substrate ([1a]), and *Yoshida* in view of *Beach* renders obvious the masking processes in [1e] and [1g].

a. [1pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”

96. *Yoshida* discloses a method of forming an enhancement mode GaN transistor.

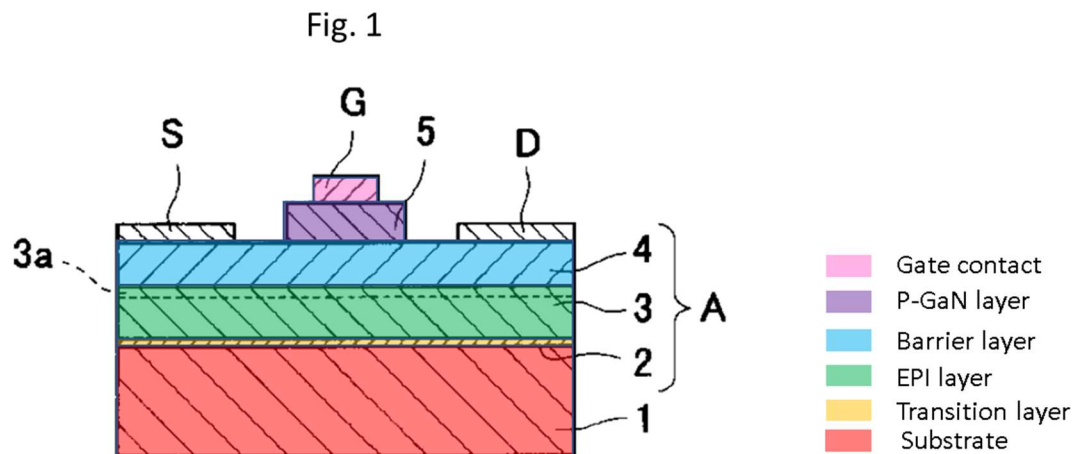
97. For example, *Yoshida* discloses a GaN high-mobility transistor that includes a p-type GaN layer below the gate, constituting a normally off enhancement mode GaN transistor. *Yoshida*, [0017], [0015], Fig. 1. *Yoshida* further discloses a method of forming such an enhancement mode GaN transistor,

including growing epitaxial layers over a substrate and etching the p-type GaN layer with dry etching. *Yoshida*, [0019]-[0023].

b. [1a] “nucleating and growing transition layers on a substrate;”

98. In my opinion, *Yoshida* in view of *Sheppard* renders obvious nucleating and growing transition layers on a substrate. *Yoshida* discloses nucleating and growing a transition layer on a substrate, and *Sheppard* discloses providing multiple transition layers on the substrate.

99. For example, *Yoshida* discloses growing a **GaN buffer layer 2** over a **substrate 1** by epitaxial growth, as shown below. *Yoshida*, [0019], [0010]. *Yoshida* discloses that the **substrate 1** is a silicon (Si) material. *Yoshida*, [0011], [0019].



Yoshida, Fig. 1 (annotated).

100. The **GaN buffer layer 2** is a transition layer because it is an intermediate layer between the **substrate 1** and the **i-type GaN layer 3**. This is

confirmed by the '508 patent which describes the **transition layers** located directly above the **substrate** and underneath the **undoped GaN layer**. Ex. 1001, 3:26-29.

101. *Yoshida* discloses applying known MOCVD and MOMBE methods to grow the transition layer (GaN buffer layer 2) on the silicon substrate. *Yoshida*, [0011], [0019]. A POSITA would have understood that growing a transition layer on a silicon substrate using the MOCVD and MOMBE methods includes an initial phase of nucleation and then growth of the transition layers. *Woll*, 1-2 (using MOMBE to nucleate and grow a thin GaN layer); *Smart*, 1 (growing a thin GaN nucleation layer). The '508 patent does not provide any description of the nucleating process, confirming that nucleating a transition layer over a silicon substrate was a well-known technique to a POSITA. *See generally*, Ex. 1001.

102. To the extent *Yoshida* does not explicitly disclose providing multiple transition layers on a substrate, *Sheppard* renders this obvious. *Sheppard* discloses a GaN transistor that includes multiple transition layers on a silicon substrate. *Sheppard*, 6:58-7:7, 7:25-32. *Sheppard* discloses providing an “AlN buffer layer” and additional “strain balancing transition layer(s)” to “provide an appropriate crystal structure transition” between the substrate and the remainder of the device. *Sheppard*, 6:58-7:7. In my opinion, a POSITA would have been motivated and found it obvious to include multiple transition layers in *Yoshida*’s device, as taught by *Sheppard*.

(a) A POSITA would have been motivated to provide multiple transition layers in *Yoshida's* device, as disclosed by *Sheppard*

103. As I explained above, *Yoshida* and *Sheppard* are both directed to a GaN transistor and forming such a device using a multilayered epitaxial structure. *Yoshida*, [0009], [0019]; *Sheppard*, 6:45-8:54; *supra*, §§IX.A, IX.C. *Sheppard* explains that providing additional transition layers on the substrate provides a benefit of strain balancing. *Sheppard*, 6:58-7:7. A POSITA would have been motivated to include multiple transition layers in *Yoshida's* device to achieve an improved strain balancing effect, as taught by *Sheppard*.

104. A POSITA would have also been motivated to include multiple transition layers in *Yoshida's* device to improve the crystalline quality of the various layers above the transition layers and reduce the crack of the materials of *Yoshida's* device. Both *Yoshida* and *Sheppard* describe using silicon as a substrate material for their GaN-based devices. *Yoshida*, [0011], [0019]; *Sheppard*, 6:48-51, 7:19-23. A POSITA would have understood that there is a large thermal mismatch between GaN and silicon, typically causing extensive cracks in the post-growth cooling down process. *Yoshida* also recognized this mismatch problem with its GaN device. *Yoshida*, [0011]. A POSITA would have recognized that having a single GaN transition layer in *Yoshida's* device does not effectively release the strain resulting from the large lattice mismatch and large thermal expansion

coefficient difference between GaN and silicon. *See, e.g., Jang*, 2 (explaining the difficulty to grow high-quality GaN devices over silicon substrates due to the mismatch of the lattice constants and thermal expansion coefficients between GaN and silicon). A POSITA would have been motivated to incorporate additional transition layers, such as the AlN buffer layer and strain balancing transition layers taught by *Sheppard*, to improve the quality and reduce cracks in the growth of GaN epitaxy over silicon. *See, e.g., Feltin*, 1-2 (using AlN and GaN transition layers to achieve high quality GaN devices); *Piner*, [0076]-[0079] (using compositionally-graded transition layers with varying composition of Aluminum (Al) to reduce crack formation in gallium nitride material).

(b) A POSITA would have reasonably expected to succeed in providing multiple transition layers in *Yoshida's* device

105. *Yoshida's* device already includes a transition layer (GaN buffer layer 2), and *Yoshida* describes a method of growing the transition layer over a silicon substrate. *Yoshida*, [0011], [0019]. Both *Yoshida* and *Sheppard* are concerned with providing a high quality GaN transistor and both use a silicon material for the substrate. *Yoshida*, [0008]-[0009], [0011]; *Sheppard*, 5:58-6:7, 6:48-51, 7:19-24. The '508 patent does not explain how to nucleate and grow transition layers over a silicon substrate, because nucleating and growing multiple transition layers to form a GaN device was routine, conventional, and well understood in the art. *See*

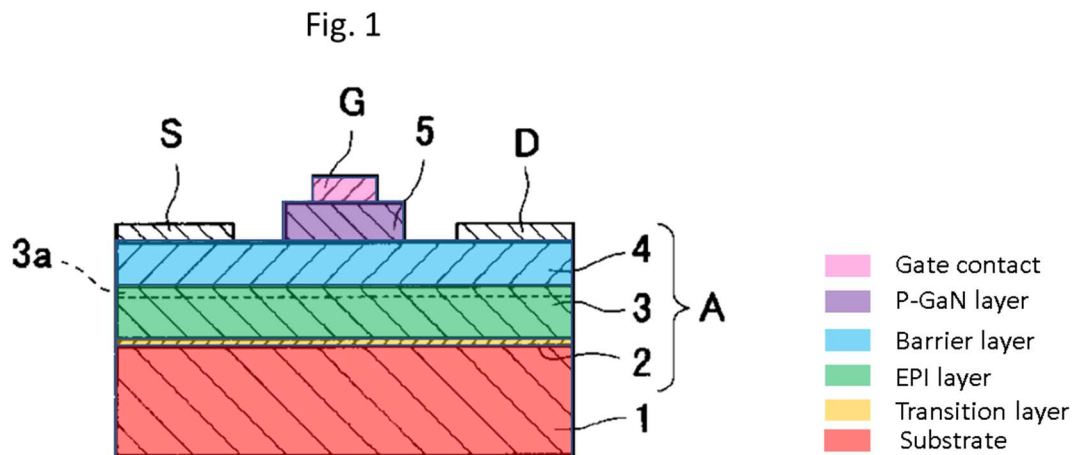
generally Ex. 1001. The '508 patent further admits that it was “conventional” to provide transition layers over a silicon substrate. Ex. 1001, 1:53-64 (background). Providing multiple transition layers in *Yoshida*’s device would have required only conventional techniques in their ordinary and expected manner, because using multiple transition layers to form a GaN transistor over a silicon substrate was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using multiple transition layers to form a GaN transistor over a silicon substrate.

c. [1b]: “growing an III Nitride EPI layer over the transistor layers;”

106. In my opinion, *Yoshida* discloses growing an III Nitride EPI layer over the transition layers.²

² The “transistor layers” in [1b] lacks an antecedent basis. It appears that “the transistor layers” refers to the “transition layers” in [1a] because the '508 patent does not describe any “transistor layers.” The '508 patent describes an III Nitride EPI layer 13 over the transition layers 12. Ex. 1001, 3:26-29, Figs. 2, 3A. I consider the “transistor layers” as the “transition layers” in [1a] in my opinions here.

107. For example, *Yoshida* discloses growing an **i-type GaN layer 3** over the **buffer layer 2** (transition layer), as shown below. *Yoshida*, [0010], [0012], [0020]. *Yoshida* further discloses that **i-type $\text{In}_x\text{Ga}_{1-x-y}\text{Al}_y\text{N}$** ($0 < x < 1$, $0 < y < 0.2$) can also be used for the semiconductor layer 3. *Yoshida*, [0012].

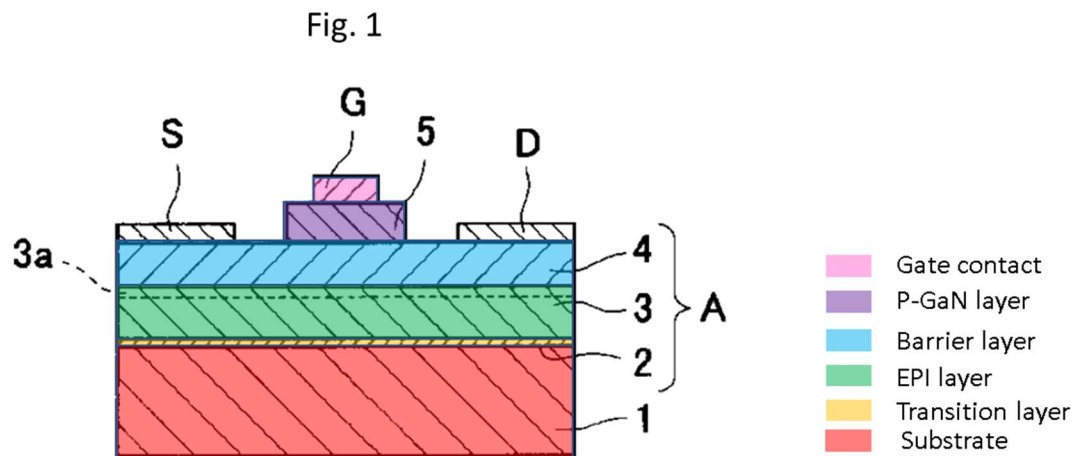


108. A POSITA would have understood that the **i-type GaN** or **i-type $\text{In}_x\text{Ga}_{1-x-y}\text{Al}_y\text{N}$ layer** is an III Nitride EPI layer because Gallium Nitride (GaN) is a III Nitride material. The '508 patent confirms this understanding. Ex. 1001, 3:24-25 (explaining that a III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$), 3:26-31 (providing an “un-doped GaN buffer material” over the transition layers).

d. [1c]: “growing an III Nitride barrier layer over the EPI layer;”

109. In my opinion, *Yoshida* discloses growing an III Nitride barrier layer over the EPI layer.

110. For example, *Yoshida* discloses growing a **n-type AlGa_{1-u}N layer 4** (barrier layer) over the **i-type Ga_{1-v}N layer 3** (EPI layer), as shown below. *Yoshida*, [0013], [0021]. Like the device in the '508 patent, *Yoshida* further discloses that the source and drain contacts are directly loaded on the **n-type AlGa_{1-u}N layer 4** (barrier layer). *Yoshida*, [0014]. *Yoshida* further discloses that **n-type In_uGa_{1-u-v}Al_vN** ($0 < u < 1$, $0 < v < 0.5$) can also be used for the semiconductor layer 4. *Yoshida*, [0013].



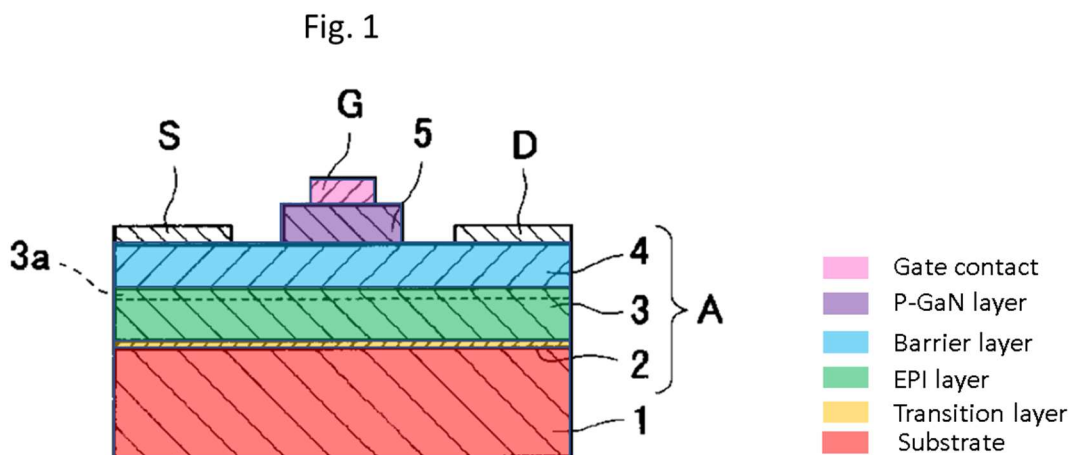
111. A POSITA would have understood that the **n-type AlGa_{1-u}N** or **n-type In_uGa_{1-u-v}Al_vN layer** is an III Nitride barrier layer because Aluminum Gallium

Nitride (**AlGaN**) is a III Nitride material. The '508 patent confirms this understanding. Ex. 1001, 3:24-25 (explaining that a III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$), 3:26-31 (providing an “AlGaN barrier layer” over the EPI layer).

e. [1d]: “growing a GaN layer with acceptor type dopants over the barrier layer;”

112. In my opinion, *Yoshida* discloses growing a GaN layer with acceptor type dopants over the barrier layer.

113. For example, *Yoshida* discloses growing a **p-type GaN layer 5** over the **n-type AlGaN layer 4** (barrier layer), as shown below. *Yoshida*, [0009], [0015], [0021]. *Yoshida* discloses that metal Mg or cyclopentadienyl magnesium are examples of a p-type dopant. *Yoshida*, [0015].



Yoshida, Fig. 1 (annotated).

114. A POSITA would have understood that the p-type dopants in the **p-type GaN layer** are acceptor type dopants. The '508 patent confirms that p-type dopants are acceptor type dopants. Ex. 1001, 6:24-28 (explaining that p-type dopants are “acceptor-rich” and can be formed by introducing magnesium impurities), 3:26-31 (providing a “p-type GaN gate layer” over the AlGaN barrier layer).

f. [1e]:

“[1e1] depositing a gate contact layer on the doped GaN layer;

[1e2] applying a gate photo resistant pattern;

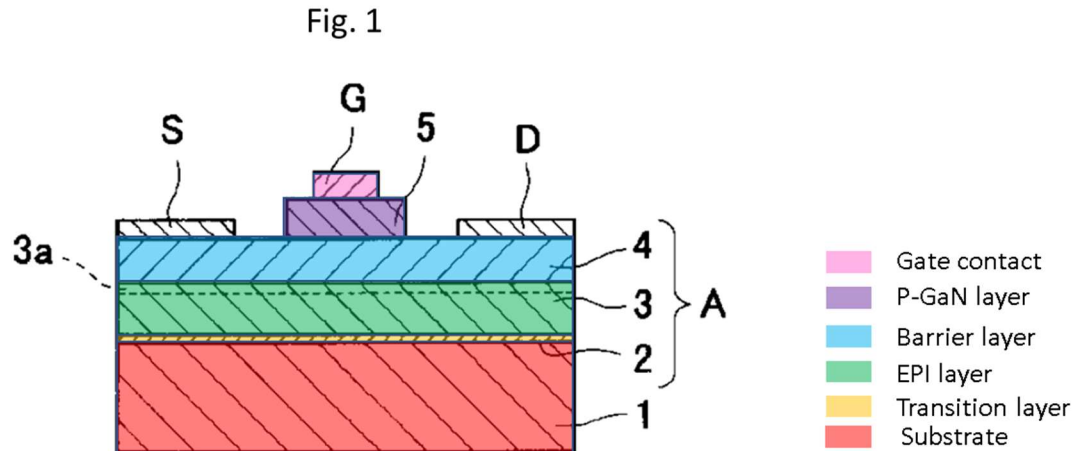
[1e3] etching away the gate contact layer outside the gate region;

[1e4] etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;

[1e5] removing the gate photo resistant pattern;”

115. In my opinion, *Yoshida* in view of *Beach* renders obvious element [1e]. *Yoshida* discloses etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact ([1e4]), and *Beach* renders obvious all steps in element [1e].

116. For example, *Yoshida* discloses forming a **gate electrode G** (gate contact) over the **p-GaN layer 5**, as shown below. *Yoshida*, [0009], [0016], [0023].

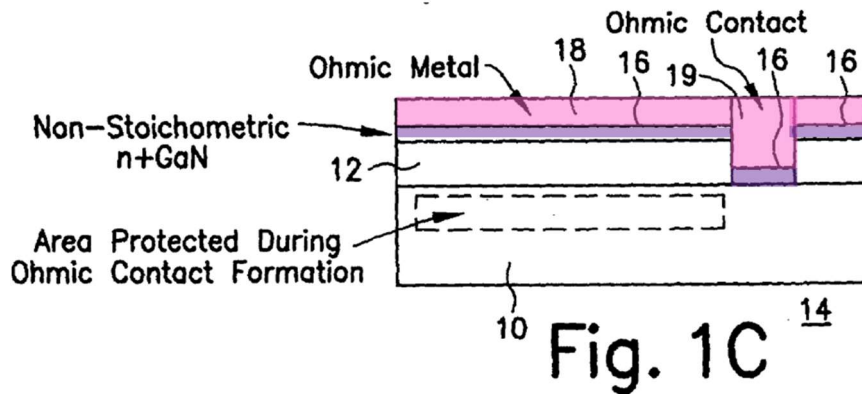


Yoshida, Fig. 1 (annotated).

117. *Yoshida* further discloses that, to form the p-GaN layer and gate contact, the p-GaN layer was etched away “except where the gate electrode was to be loaded.” *Yoshida*, [0022]. Then the gate electrode is loaded above the p-GaN layer. *Yoshida*, [0023]. Although Figure 1 shows that the p-GaN layer 5 extends beyond the gate contact, *Yoshida* discloses in the description that the p-GaN layer 5 is etched away “except where the gate electrode was to be loaded.” *Yoshida*, [0022]. Thus, *Yoshida* discloses step [1e4] “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact.”

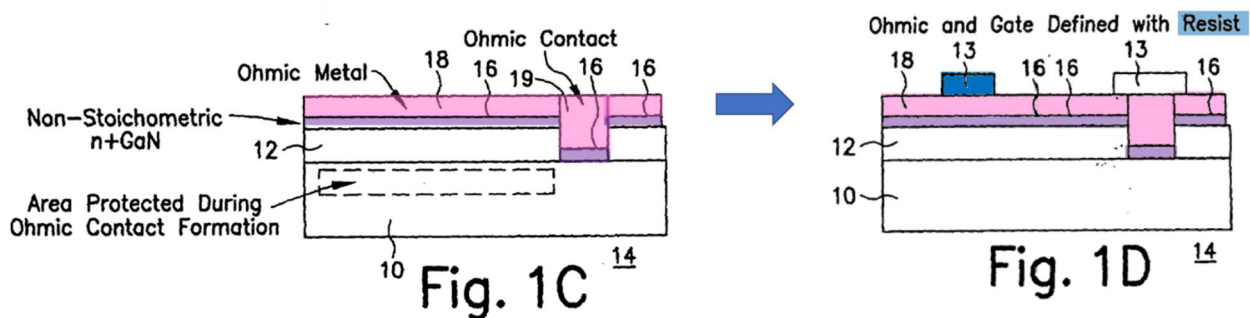
118. *Yoshida* does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the p-GaN layer and gate contact layer, nor does Figure 1 show a p-GaN layer and gate electrode of the same width, but *Beach* renders this obvious.

119. *Beach* discloses a method of forming a self-aligned gate and doped GaN layer using the steps of element [1e]. First, *Beach* discloses element [1e1], i.e., depositing an **ohmic material 18** (gate contact layer) on the **doped GaN layer 16**, as shown below. *Beach*, [0045] (“Material 18 deposited over layer 16”).



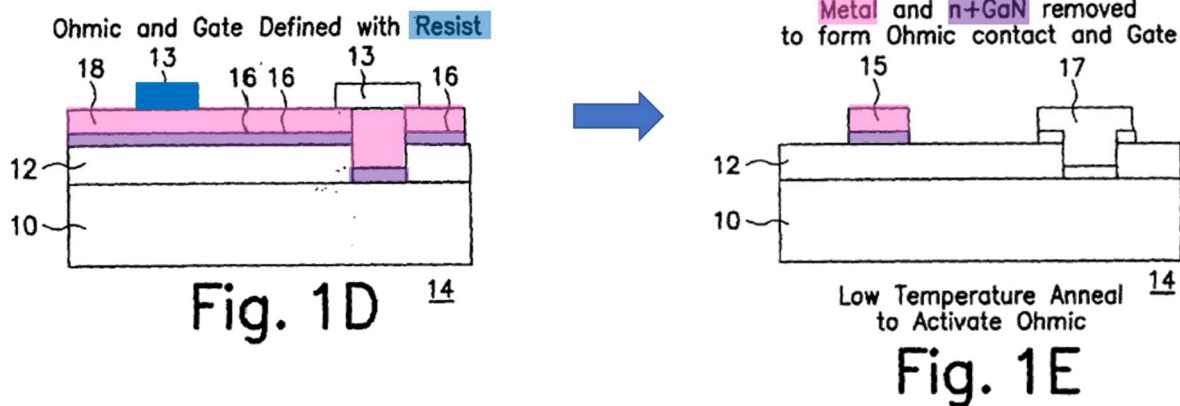
Beach, Fig. 1C (annotated).

120. Second, *Beach* discloses step [1e2], i.e., applying a **gate photo resistant pattern 13** (mask) to the structure, as shown below. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17”).



Beach, Figs. 1C, 1D (annotated).

121. Third, *Beach* discloses step [1e3], i.e., etching away the **gate contact layer** outside the gate region, and step [1e4], i.e., etching away the **doped GaN layer**, except a portion of the doped GaN layer beneath the gate contact, as shown below. *Beach*, [0047] (“After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.”).



Beach, Figs. 1D, 1E (annotated).

122. Fourth, *Beach* discloses step [1e5], i.e., removing the gate photoresistant pattern (mask). *Beach*, [0049] (“After material 18 has been removed from device 14 in regions not covered by photoresist 13, photoresist 13 is stripped off”); *see also Beach*, Fig. 1E (showing the photoresist 13 being removed).

123. Thus, *Beach* discloses all steps of element [1e] which use a single mask (gate photoresistant pattern) to form the gate contact and doped GaN layer.

In my opinion, it would have been obvious to apply *Beach*'s masking process to form *Yoshida*'s device.

(a) A POSITA would have been motivated to apply *Beach*'s masking process to form *Yoshida*'s device

124. As I explained above, *Yoshida* and *Beach* are both directed to a GaN-based semiconductor device and methods for forming such a device. *Yoshida*, [0009], [0019]-[0023]; *Beach*, [0002], [0017]-[0018]; *supra* §§IX.A, IX.B. Like *Yoshida*, *Beach* discloses a GaN device with multiple layers of III-nitride material, such as a GaN layer 10, an AlGaN layer 12, and a highly doped GaN layer 16. *Beach*, [0040]-[0043]. Like *Yoshida*'s device, *Beach*'s device has a gate contact 15 and ohmic contact 17. *Beach*, [0048]-[0049]. A POSITA would have been motivated to use the single mask process to form the gate contact and doped GaN layer, as taught by *Beach*, to improve *Yoshida*'s device and process in multiple ways.

125. First, *Beach*'s single mask process effectively achieves *Yoshida*'s objective that the doped GaN layer is to be etched away except the area where the gate contact is to be loaded. *Yoshida*, [0022]. A POSITA would have recognized that *Beach*'s single mask process automatically achieves self-alignment between the gate contact and the doped GaN layer and improves the gate's alignment in *Yoshida*'s device. Compare *Beach*, Fig. 1E with *Yoshida*, Fig. 1. A POSITA would

have appreciated that self-aligned gate and doped GaN layer is a desired feature in GaN devices and would have been motivated to implement *Beach*'s single mask process to achieve a self-aligned gate arrangement in *Yoshida*'s device. *See Beach*-547, [0043]-[0048] (describing self-aligned gates as advantageous); *Kouznetsov*, 3:42-61 (explaining that self-alignment decreases die size and cost).

126. Second, *Beach*'s single mask process to etch the gate contact and doped GaN layer simplifies *Yoshida*'s process to form the GaN device. Compared to *Yoshida*'s process which employs two separate masks and two separate steps to etch the gate contact and doped GaN layer, *Beach* uses a single mask to etch the gate and doped GaN layer which removes the additional step of applying a second mask for the gate contact. *Beach*, [0047]. A POSITA would have understood that applying an additional mask involves substantial undertaking during manufacturing and the removal of one additional mask application leads to a simplified manufacturing process and saving of manufacturing cost. A POSITA would have been motivated to use *Beach*'s single mask process to produce *Yoshida*'s device because doing so would simplify the manufacturing process and save manufacturing cost. *See Kouznetsov*, 3:55-61 (describing that uses the same photoresist mask to form the layers decreases process cost and complexity).

(b) A POSITA would have reasonably expected to succeed in applying *Beach*'s masking process to form *Yoshida*'s device

127. Applying a single mask to form the gate contact and doped GaN layer was a well-known and conventional technique when the '508 patent was filed. The '508 patent states that the etching of the gate contact and p-GaN layer using the same mask is performed by “any known technique,” because etching multiple layers of different materials using the same mask was routine, conventional, and well understood in the art. Ex. 1001, 3:45-50. Indeed, using the same mask to etch different layers of materials in semiconductor devices was known and implemented decades before the '508 patent. *Green*, 8:10-19 (etching the silicide layer and metal layer using a single mask), Figs. 6-7; *Spikes*, 4:39-5:3 (etching the metal layer, the polysilicon layer, and dielectric layer using a single mask), Figs. 1B-1C; *Shim*, 3:8-14 (etching the metal layer and silicon layer using a single mask), Figs. 2C-2D.

128. Both *Yoshida*'s and *Beach*'s devices use the same GaN material for the layer underneath the gate contact. *Yoshida*'s device could be formed using the single mask technique described by *Beach*, according to the known, routine process of masking and etching. To the extent EPC argues that the dopants applied to *Beach*'s GaN layer (n-type dopants) are not the same type of dopants as *Yoshida* (p-type dopants), a POSITA would have understood that the impurities caused by the dopants are so dilute that they do not change the etching characters of the GaN material, and as a result, a POSITA would have reasonably expected to succeed in

applying *Beach*'s masking technique to etch the p-type GaN layer in *Yoshida*'s device. A POSITA would have understood that the same etching process could be performed regardless of the type of dopants applied to the GaN material.

129. Using *Beach*'s single mask process to etch the gate contact and doped GaN layer in *Yoshida*'s device would have required only conventional techniques in their ordinary and expected manner, because using the same mask to etch different layers of materials was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach*'s single mask process to form *Yoshida*'s GaN device.

g. [1f]:

“[1f1] depositing a dielectric layer;

[1f2] applying a contact photo resistant pattern;

[1f3] etching the dielectric layer to open the drain and source contact area;

[1f4] removing the contact photo resistant pattern;”

130. In my opinion, *Yoshida* discloses all steps in element [1f].

131. First, *Yoshida* discloses that, after etching away the p-type GaN layer, “[a]n SiO₂ film was then deposited by plasma CVD to cover the entire surface.” *Yoshida*, [0022]. A POSITA would have understood that SiO₂ (Silicon dioxide) is a material that has excellent dielectric properties and is commonly used as the dielectric material for semiconductor devices. Thus, *Yoshida* discloses step [1f1], i.e., depositing a dielectric layer.

132. Second, *Yoshida* discloses “patterning [the SiO₂ film] with photoresist,” such that the portion the gate contact is “masked” and the portion to load the source and drain contacts are left “open.” *Yoshida*, [0022]. Thus, *Yoshida* discloses step [1f2], i.e., applying a contact photo resistant pattern.

133. Third, *Yoshida* discloses the layer underneath the SiO₂ film (dielectric layer) is “exposed” to “load source electrode S and drain electrode D” after applying the photoresist pattern (mask). *Yoshida*, [0022]. A POSITA would have understood that the SiO₂ film (dielectric layer) in *Yoshida*’s device is etched to leave open the drain and source contact area because (1) the SiO₂ film (dielectric layer) is initially deposited to “cover the entire surface”; and (2) after applying the mask, the portion of SiO₂ film (dielectric layer) covering the source and drain contact area are etched, such that the portion of layer underneath the SiO₂ film (dielectric layer) is exposed for loading the source and drain contacts on the exposed n-type AlGaN layer 4. *Yoshida*, [0013], [0021]-[0022]. Thus, *Yoshida* discloses step [1f3], i.e., etching the dielectric layer to open the drain and source contact area.

134. Fourth, *Yoshida* discloses “etching away the masking” after opening the source and drain contact area. *Yoshida*, [0022]. A POSITA would have also understood that, in semiconductor manufacturing, the masks used to pattern and form the device are to be removed because the masks are only tools to construct

the device and not part of the device. *Ghandhi*, 12 (describing the “final step” of the masking process is “removal of the exposed photoresist.”) Thus, *Yoshida* discloses step [1f4], i.e., removing the contact photo resistant pattern.

h. [1g]:

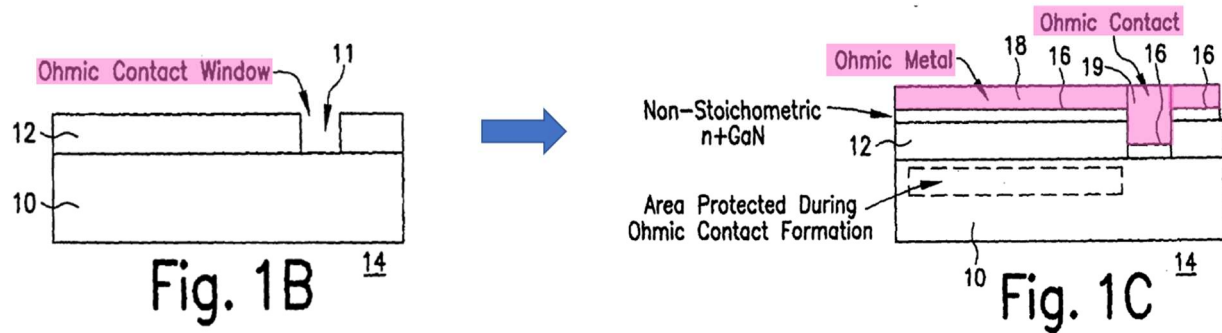
**“[1g1] depositing an Ohmic contact metal;
[1g2] applying a metal photo resistant pattern;
[1g3] etching the Ohmic contact metal;
[1g4] removing the metal photo resistant pattern; and
[1g5] performing rapid thermal annealing to form
Ohmic drain and source contacts.”**

135. In my opinion, *Yoshida* in view of *Beach* renders obvious element [1g]. *Yoshida* discloses depositing metal Al (Ohmic contact metal) on the n-type semiconductor layer 4 to load source electrode S and drain electrode D (Ohmic source and drain contacts). *Yoshida*, [0022], [0010]. Thus, *Yoshida* discloses step [1g1], i.e., depositing an Ohmic contact metal.

136. *Yoshida* does not explicitly disclose a process for forming the source and drain electrodes (Ohmic source and drain contacts), but *Beach* renders obvious using the remaining steps in [1g] to form *Yoshida*’s Ohmic source and drain contacts. *Yoshida*, [0010], [0022]; *Beach*, [0045]-[0047].

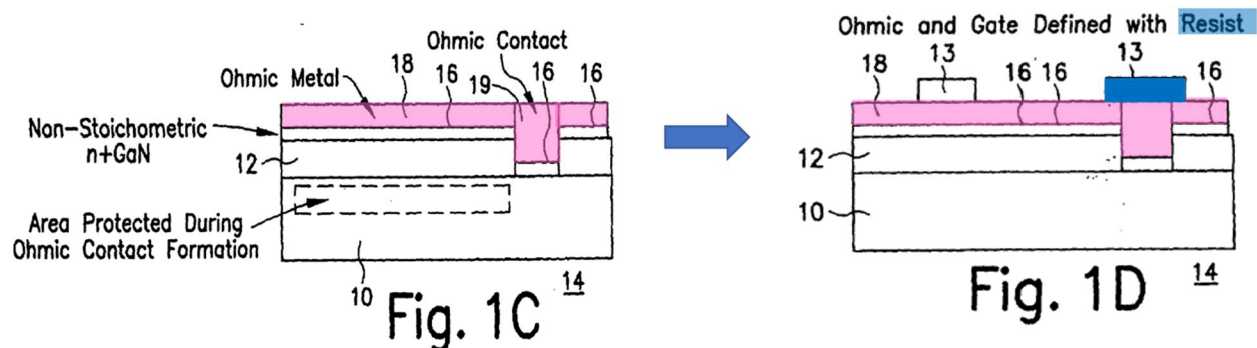
137. First, *Beach* discloses that an **Ohmic contact metal 18** is deposited in Ohmic contact window 11, as shown below. *Beach*, [0045] (“Material 18 deposited

over layer 16 and in ohmic contact window 11 [] may be an ohmic metal”). Thus, *Beach* discloses step [1g1], i.e., depositing an Ohmic contact metal.



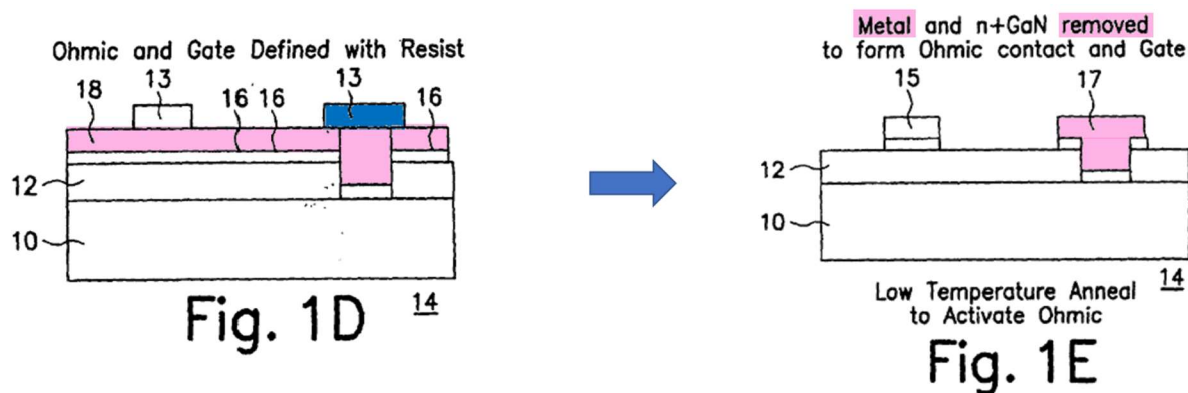
Beach, Figs. 1B, 1C (annotated).

138. Second, *Beach* discloses that a **metal photo resistant pattern 13** (mask) is applied over the **Ohmic contact metal 18**, as shown below. *Beach*, [0047] (“resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17”). Thus, *Beach* discloses step [1g2], i.e., applying a metal photo resistant pattern.



Beach, Figs. 1C, 1D (annotated).

139. Third, *Beach* discloses that the **Ohmic contact metal 18** is etched except the portion protected by **metal photo resistant pattern 13** (mask), as shown below. *Beach*, [0047] (“After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13.”). Thus, *Beach* discloses step [1g3], i.e., etching the Ohmic contact metal.



Beach, Figs. 1D, 1E (annotated).

140. Fourth, *Beach* discloses that the **metal photo resistant pattern 13** (mask) is removed, as shown in Figure 1E above. *Beach*, [0049] (“After material 18 has been removed from device 14 in regions not covered by photoresist 13, photoresist 13 is stripped off”). Thus, *Beach* discloses step [1g4], i.e., removing the metal photo resistant pattern.

141. Fifth, *Beach* discloses that thermal annealing is performed to form the source and drain contacts. *Beach*, [0049] (“The temperatures in the anneal step are below about 850°C, and preferably about 600°C. The low temperature anneal step activates ohmic contact 17 to provide a low resistance connection point between

the conduction channel formed in layer 10 and contact 17.”); *see also Beach*, [0054] (“Typically, an anneal step is performed to activate ohmic contact 26, and the presence of protective layer 22 permits the anneal to take place at a lower temperature, such as 850°C, or preferably 600 °C, for example.”), Abstract (forming device contacts with “high temperature processing”). To the extent EPC argues that *Beach* does not explicitly disclose rapid thermal annealing, a POSITA would have found that *Beach* renders it obvious to perform rapid thermal annealing to form Ohmic source and drain contacts in *Beach*’s and *Yoshida*’s devices (step [1g5]). A POSITA would have found performing rapid thermal annealing to activate ohmic contacts was routine and conventional long before the ’508 patent was filed, and would have had a reasonable expectation of success in doing so. Such technique was a conventional and commonly adopted technique in GaN semiconductor manufacturing to form a low-resistance ohmic contact in an efficient manner. *See Johnson*, [0085] (performing rapid thermal annealing to form source-drain contacts); *Hu*, 1 (performing RTA (rapid thermal annealing) at 850°C for 1 minute to form source-drain contacts); *Chen*, [0087] (performing rapid thermal annealing at 850°C for 45 seconds to form source-drain ohmic contacts); *Shimizu*, 1 (performing rapid thermal annealing at 780°C for 30 seconds to form source-drain electrodes); *Ye*, [0061] (performing RTA (rapid thermal annealing) at 500°C for 30 seconds to form source and drain ohmic contacts). A POSITA would

have been motivated to perform rapid thermal annealing instead of conventional furnace annealing to activate ohmic contacts because it was well known that rapid thermal annealing reduces thermal budget, lowers manufacturing cost, and increases production throughput of the semiconductor devices. *See Campbell*, 6 (rapid thermal processing was developed to minimize the thermal budget); *Ye*, [0061] (performing RTA (rapid thermal annealing) at 500°C for 30 seconds to form source and drain ohmic contacts); *Hu*, 1 (performing RTA (rapid thermal annealing) at 850°C for 1 minute to form source-drain contacts). A POSITA would have been motivated to perform rapid thermal annealing to activate ohmic contacts because it was known to improve the structural and electronic properties of GaN materials, as well as providing a smoother surface of the contact which improves circuit yield. *Zhu*, 5 (describing that RTA is effective in improving the structural and electronic properties of MBE-grown GaN films); *Campbell*, 9 (describing that rapid thermal processing improvise circuit yield compared to the conventional anneals). Therefore, it would have been obvious to perform rapid thermal annealing to activate the Ohmic contacts in *Beach*'s and *Yoshida*'s devices.

142. In my opinion, a POSITA would have found it obvious to apply *Beach*'s masking process to form *Yoshida*'s Ohmic source and drain contacts.

- (a) **A POSITA would have been motivated to apply *Beach*'s masking process to form *Yoshida*'s Ohmic source and drain contacts**

143. As I explained above, *Yoshida* and *Beach* are both directed to a GaN-based semiconductor device and methods for forming such a device. *Yoshida*, [0009], [0019]-[0023]; *Beach*, [0002], [0017]-[0018]; *supra* §§IX.A, IX.B. Like *Yoshida*, *Beach* discloses a GaN device with multiple layers of III-nitride material, such as a GaN layer 10, an AlGaN layer 12, and a highly doped GaN layer 16. *Beach*, [0040]-[0043]. Similar to *Yoshida*'s device, *Beach*'s device has a gate contact 15 and ohmic contact 17. *Beach*, [0048]-[0049]. A POSITA would have been motivated to use the masking process to form the Ohmic source and drain contacts, as taught by *Beach*, to improve *Yoshida*'s device and process in multiple ways.

144. First, *Beach*'s masking process was a known-technique that effectively achieved *Yoshida*'s objective to form the source and drain electrodes (Ohmic source and drain contacts). *Yoshida*, [0010], [0022]. *Yoshida* does not disclose a process for forming the source and drain electrodes (Ohmic source and drain contacts), and a POSITA would have appreciated that *Beach*'s masking process would produce the Ohmic source and drain contacts in *Yoshida*'s transistor. A POSITA would have been motivated to adopt *Beach*'s masking process to effectively form the Ohmic source and drain contacts in *Yoshida*'s transistor, such that *Yoshida*'s transistor would perform its intended functions.

145. Second, Beach's masking process is simpler compared to the other alternative process, such as the lift-off process, to form the Ohmic source and drain contacts. A POSITA would have understood that *Beach's* masking process avoids manufacturing of the vertical profile of photoresist shape used in the lift-off process, thereby saving the manufacturing cost to produce *Yoshida's* transistor. A POSITA would have been motivated to use *Beach's* masking process to produce *Yoshida's* Ohmic source and drain contacts because doing so would simplify the manufacturing process and save manufacturing cost.

146. Third, Beach's masking process allows a source and gate connected field plate to be easily formed, which reduces electrical field at the gate corner and results in higher breakdown voltage at *Yoshida's* device. *See, e.g., Kumar, 4* (describing significant improvement in breakdown voltage with the field plate); *Saito, 1* (describing that the field plate structure is effective for the high breakdown voltage HEMT design); *Hikita-895, [0046]* (describing the transistor with a field plate has an enhanced breakdown voltage). A POSITA would have appreciated that, applying Beach's masking process, a field plate can be easily formed by using a mask pattern that extends the source ohmic contact region toward the gate contact, such that a portion of the Ohmic metal between the source Ohmic contact and gate contact is not etched away. In contrast, the other alternative process, such as the lift-off process, requires a separate masking step to allow the source ohmic

contact metal to extend beyond the designated opening for source contact, and as a result, requires additional processing to provide a field plate design. *See, e.g., Kumar*, 1 (applying additional steps including patterning the gate with e-beam lithography and e-beam evaporation to form a field plate); *Saito*, 2 (forming a separate field plate electrode after forming source and drain ohmic contacts using a lift off process); *Hikita-895*, [0056]-[0057] (forming a separate field plate electrode with another liftoff process after first forming source and drain electrodes by a lift off method). Therefore, a POSITA would have been motivated to use *Beach*'s more flexible masking process to produce *Yoshida*'s Ohmic source and drain contacts to provide a field plate in *Yoshida*'s device in a simple manner.

(b) A POSITA would have reasonably expected to succeed in applying *Beach*'s masking process to form *Yoshida*'s Ohmic source and drain contacts

147. Using a mask (metal photo resist pattern) to etch Ohmic contact metal to form source and drain contacts was a well-known and conventional technique when the '508 patent was filed. The '508 patent does not explain how to apply a mask to etch Ohmic contact metal, because using a mask to pattern and etch Ohmic contact metal was routine, conventional, and well understood in the art. *See generally* Ex. 1001. Both *Yoshida*'s and *Beach*'s devices use a III Nitride material for the layer underneath the Ohmic source and drain contacts. *Yoshida*'s Ohmic source and drain contacts could be formed using the masking process described by

Beach, according to the known, routine process of masking and etching. Using *Beach*'s masking process to etch the Ohmic contact metal in *Yoshida*'s device would have required only conventional techniques in their ordinary and expected manner, because using a mask to etch an Ohmic contact metal was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach*'s masking process to form *Yoshida*'s Ohmic source and drain contacts.

2. [Claim 2] “wherein the EPI layer is comprised of InAlGaN.”

148. Claim 2 depends from claim 1. In my opinion, *Yoshida* discloses that the EPI layer is comprised of InAlGaN. As I explained in [1b], *Yoshida* discloses that the EPI layer barrier layer is comprised of i-type $\text{In}_x\text{Ga}_{1-x-y}\text{Al}_y\text{N}$ ($0 < x < 1$, $0 < y < 0.2$). *Yoshida*, [0012]; *supra*, §XI.A.1.c.

3. [Claim 3] “the barrier layer is comprised of InAlGaN with a larger band gap than the buffer layer.”

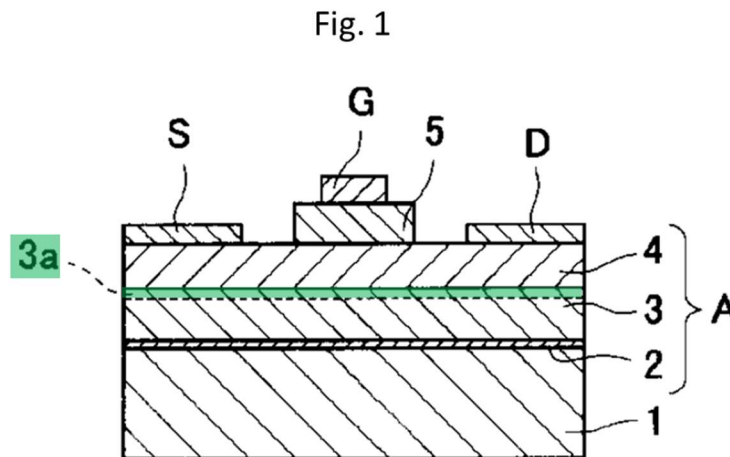
149. Claim 3 depends from claim 1. In my opinion, *Yoshida* renders it obvious that the barrier layer is comprised of InAlGaN with a larger band gap than the buffer layer.³

150. *Yoshida* discloses that the barrier layer is comprised of InAlGaN. As I explained in [1c], *Yoshida* discloses that the barrier layer is comprised of n-type $\text{In}_u\text{Ga}_{1-u-v}\text{Al}_v\text{N}$ ($0 < u < 1$, $0 < v < 0.5$). *Yoshida*, [0013]; *supra*, §XI.A.1.d.

151. *Yoshida* further discloses that the barrier layer (n-type semiconductor layer 4) and the EPI layer (i-type semiconductor layer 3) form a “two-dimensional electron gas” layer at a region near the junction of the two layers, which traps the electrons supplied from the barrier layer and allows high-speed electron mobility. *Yoshida*, [0016]-[0017], [0007]. *Yoshida* explains that a two-dimensional electron

³ The “buffer layer” in claim 3 lacks an antecedent basis. It appears that “the buffer layer” refers to the “EPI layer” in claim 1 because the ’508 patent describes the “un-doped GaN buffer material 13” as the layer below the barrier layer 14, and in claim 1 the “EPI layer” is the layer below the barrier layer. Ex. 1001, 3:26-29, Figs. 2, 3A. I consider the “buffer layer” is as the “EPI layer” in claim 1 in my opinions here.

gas layer 3a is formed “at the topmost portion of i-type semiconductor layer 3,” as shown below. *Yoshida*, [0016].



Yoshida, Fig. 1.

152. In my opinion, a POSITA would have found it obvious that *Yoshida*'s barrier layer 4 has a larger band gap than the EPI layer 3 to form the two-dimensional electron gas. A POSITA would have understood that the barrier layer 4 needs to have a larger band gap than the EPI layer 3, such that the electrons originating in the wider band gap barrier layer 4 transfer to the two-dimensional electron gas layer. See *Sheppard*, 1:33-38 (“a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity”), 8:4-6 (“The barrier layer 22 may be a Group III-nitride and has a bandgap larger than that of the channel layer 20 and a smaller electron affinity than the channel layer 20”); *Sheppard-693*, 1:47-50 (“electrons that originate in the

doped, wider-bandgap semiconductor transfer to the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering”); *Sugimoto*, [0107]-[0109] (describing that a two-dimensional electron gas is formed by providing an AlGa_N barrier layer with a wider band gap over the Ga_N buffer layer with a smaller band gap). A POSITA would have found it obvious that *Yoshida*’s barrier layer 4 has a larger band gap than the EPI layer 3 to form a two-dimensional electron gas layer in order for *Yoshida*’s high-mobility transistor (HEMT) to perform its intended functions.

B. Ground 2: Claims 1-4 Are Obvious over *Hikita-347*, *Beach*, and *Sheppard*

1. Independent Claim 1

153. In my opinion, the combination of *Hikita-347*, *Sheppard*, and *Beach* renders claim 1 obvious.

154. *Hikita-347* discloses elements [1pre], [1b], [1c], and [1d]. *Hikita-347* in view of *Sheppard* renders obvious forming multiple transition layers on a substrate ([1a]) and the masking process in [1f], and *Hikita-347* in view of *Beach* renders obvious the masking processes in [1e] and [1g].

a. [1pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”

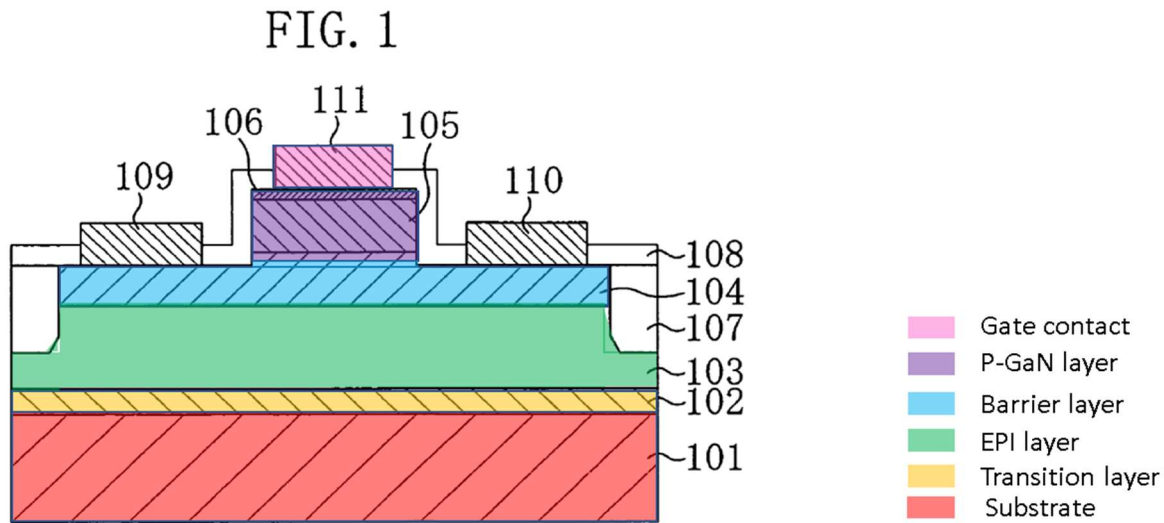
155. To the extent the preamble is limiting, *Hikita-347* discloses a method of forming an enhancement mode GaN transistor.

156. For example, *Hikita-347* discloses a “normally OFF type” GaN transistor with a p-type GaN layer below the gate, constituting an enhancement mode GaN transistor. *Hikita-347*, [0038], Fig. 1. *Hikita-347* further discloses a method of forming such an enhancement mode GaN transistor, including growing epitaxial layers over a substrate and etching the p-type GaN layer with dry etching. *Hikita-347*, [0013], [0035], [0055]-[0061].

b. [1a] “nucleating and growing transition layers on a substrate;”

157. In my opinion, *Hikita-347* in view of *Sheppard* renders obvious nucleating and growing transition layers on a substrate. *Hikita-347* discloses nucleating and growing a transition layer on a substrate, and *Sheppard* discloses providing multiple transition layers on the substrate.

158. For example, *Hikita-347* discloses growing an **AlN buffer layer 102** over a **substrate 101** by epitaxial growth, as shown below. *Hikita-347*, [0013], [0033]. *Hikita-347* discloses that the **substrate 101** is a sapphire material. *Hikita-347*, [0045], [0056].



Hikita-347, Fig. 1 (annotated).

159. The **AlN buffer layer 102** is a transition layer because it is an intermediate layer between the **substrate 101** and the **undoped GaN layer 103**. This is confirmed by the '508 patent which describes the **transition layers** located directly above the **substrate** and underneath the **undoped GaN layer**. Ex. 1001, 3:26-29.

160. *Hikita-347* discloses applying known a MOCVD method to grow the transition layer (AlN buffer layer 102) on the sapphire substrate. *Hikita-347*, [0033], [0056]. A POSITA would have understood that growing a transition layer on a sapphire substrate using the MOCVD method includes an initial phase of nucleation and then growth of the transition layer. *Sheppard*, 6:58-62 (providing an AlN buffer layer to “provide an appropriate crystal structure transition”), 7:29-32 (“buffer nucleation and/or transition layers may be deposited by MOCVD”). The

'508 patent does not provide any description of the nucleating process, confirming that nucleating a transition layer over a silicon substrate was a well-known technique to a POSITA. *See generally*, Ex. 1001.

161. To the extent *Hikita-347* does not explicitly disclose providing multiple transition layers on a substrate, *Sheppard* renders this obvious. *Sheppard* discloses a GaN transistor that includes multiple transition layers on a sapphire substrate. *Sheppard*, 7:19-24. *Sheppard* discloses providing an “AlN buffer layer” and additional “strain balancing transition layer(s)” to “provide an appropriate crystal structure transition” between the substrate and the remainder of the device. *Sheppard*, 6:58-7:7.

162. A POSITA would have been motivated and found it obvious to include multiple transition layers in *Hikita-347*'s device, as taught by *Sheppard*. Like the *Yoshida* combination, both *Hikita-347* and *Sheppard* are concerned with providing a high-quality GaN transistor and both disclose using a different material for the substrate—here Sapphire, rather than Silicon as in *Yoshida*. *Hikita-347*, [0033], [0056]; *Sheppard*, 7:19-23; *Yoshida*, [0008]-[0011], [0019]. A POSITA would have been motivated to include multiple transition layers in *Hikita-347*'s device and would have expected success for the same reasons I explained in Ground 1, which apply to GaN transistors formed using either a silicon or a sapphire substrate.

(a) A POSITA would have been motivated to provide multiple transition layers in *Hikita-347*'s device, as disclosed by *Sheppard*

163. *Hikita-347* and *Sheppard* are both directed to a GaN transistor and forming such a device using a multilayered epitaxial structure. *Hikita-347*, [0033], [0034]; *Sheppard*, 6:45-8:54. *Sheppard* explains that providing additional transition layers on the substrate provides a benefit of strain balancing. *Sheppard*, 6:58-7:7. A POSITA would have been motivated to include multiple transition layers in *Hikita-347*'s device to achieve an improved strain balancing effect, as taught by *Sheppard*. A POSITA would have also been motivated to include multiple transition layers in *Hikita-347*'s device to improve the crystalline quality of the various layers above the transition layers and reduce the crack of the materials of *Hikita-347*'s device.

164. Both *Hikita-347* and *Sheppard* describe using sapphire as a substrate material for their GaN-based devices. *Hikita-347*, [0033]; *Sheppard*, 7:19-23. A POSITA would have understood that there is a large lattice mismatch between GaN and sapphire, causing large densities of misfit dislocations to form as line defects penetrating through the epitaxial layers and as a result lowering the conductivity of the GaN transistor's channel. See, e.g., *Piner*, [0003]-[0004] (describing dislocation defects when III-nitride materials are formed on sapphire substrates). A POSITA would have recognized that having a single AlN transition

layer in *Hikita-347*'s device does not effectively reduce the line defects resulting from the large lattice mismatch coefficient difference between GaN and sapphire. A POSITA would have been motivated to incorporate additional transition layers taught by *Sheppard* to improve the quality of the GaN transistor by reducing the line defects formed during the growth of GaN epitaxy over sapphire. *See, e.g., Piner*, [0076]-[0079], [0092] (using compositionally-graded transition layers with varying composition of Aluminum (Al) over a sapphire substrate to reduce dislocation densities that negatively affect device performance).

(b) A POSITA would have reasonably expected to succeed in providing multiple transition layers in *Hikita-347*'s device

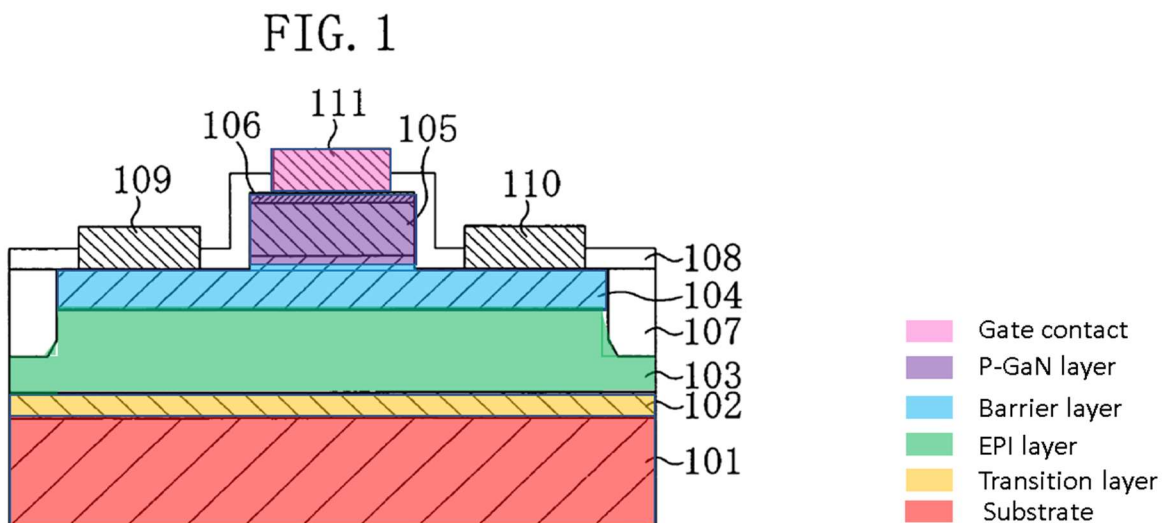
165. *Hikita-347*'s device already includes a transition layer (AlN buffer layer 102), and *Hikita-347* describes a method of growing the transition layer over a sapphire substrate. *Hikita-347*, [0033], [0056]. Both *Hikita-347* and *Sheppard* are concerned with providing a high quality GaN transistor and both disclose using a sapphire material for the substrate. *Hikita-347*, [0033], [0056]; *Sheppard*, 7:19-24. The '508 patent does not explain how to nucleate and grow transition layers over a substrate, because nucleating and growing multiple transition layers to form a GaN device was routine, conventional, and well understood in the art. *See generally* Ex. 1001. The '508 patent further admits that it was "conventional" to provide transition layers over a sapphire substrate. Ex. 1001, 1:53-64 (background).

Providing multiple transition layers in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner, because using multiple transition layers to form a GaN transistor over a sapphire substrate was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using multiple transition layers to form a GaN transistor over a sapphire substrate.

c. [1b]: “growing an III Nitride EPI layer over the transistor layers;”

166. In my opinion, *Hikita-347* discloses growing an III Nitride EPI layer over the transition layers.

167. For example, *Hikita-347* discloses growing an **undoped GaN layer 103** over the **buffer layer 102** (transition layer), as shown below. *Hikita-347*, [0013], [0033], [0056].



Hikita-347, Fig. 1 (annotated).

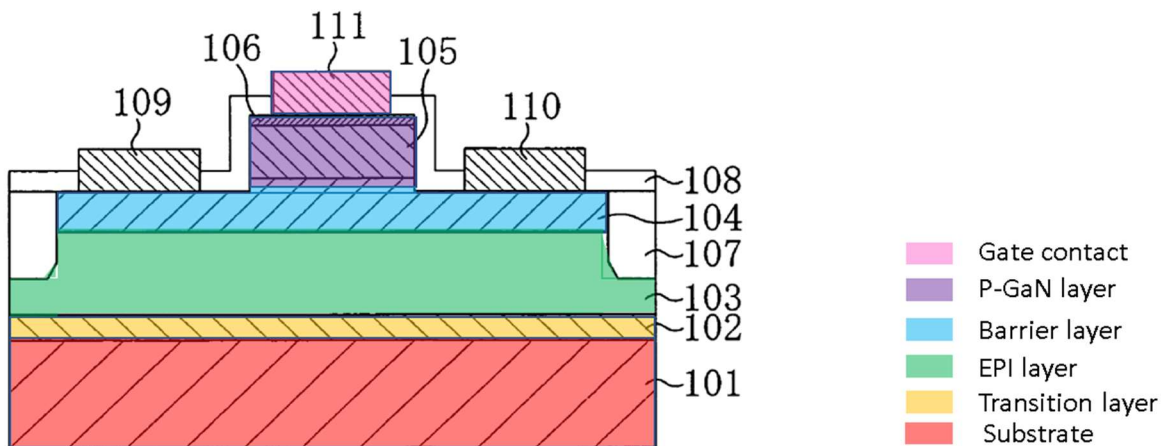
168. A POSITA would have understood that the **undoped GaN layer** is an III Nitride EPI layer because Gallium Nitride (GaN) is a III Nitride material. The '508 patent confirms this understanding. Ex. 1001, 3:24-25 (explaining that a III Nitride material can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$), 3:26-31 (providing an “un-doped GaN buffer material” over the transition layers).

d. [1c]: “growing an III Nitride barrier layer over the EPI layer;”

169. In my opinion, *Hikita-347* discloses growing an III Nitride barrier layer over the EPI layer.

170. For example, *Hikita-347* discloses growing an **undoped AlGaN layer 104** (barrier layer) over the **undoped GaN layer 103** (EPI layer), as shown below. *Hikita-347*, [0013], [0033], [0056]. Like the device in the '508 patent, *Hikita-347* further discloses that the source and drain contacts 109, 110 are directly formed on the **n-type undoped AlGaN layer 104** (barrier layer). *Hikita-347*, [0034].

FIG. 1



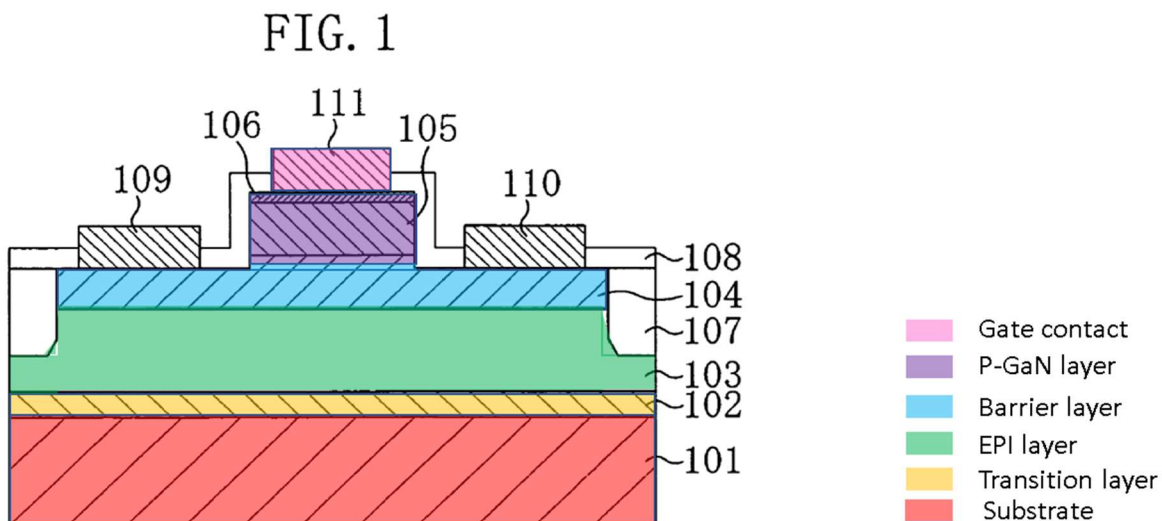
Hikita-347, Fig. 1 (annotated).

171. A POSITA would have understood that the **undoped AlGa_N layer 104** is an III Nitride barrier layer because Aluminum Gallium Nitride (**AlGa_N**) is a III Nitride material. The '508 patent confirms this understanding. Ex. 1001, 3:26-31 (providing an “AlGa_N barrier layer” over the EPI layer).

e. [1d]: “growing a GaN layer with acceptor type dopants over the barrier layer;”

172. In my opinion, *Hikita-347* discloses growing a GaN layer with acceptor type dopants over the barrier layer.

173. For example, *Hikita-347* discloses growing a **p-type GaN layer 105** containing a p-type impurity over the **undoped AlGa_N layer 104** (barrier layer), as shown below. *Hikita-347*, [0013], [0033], [0056].



Hikita-347, Fig. 1 (annotated).

174. A POSITA would have understood that the p-type dopants in the **p-type GaN layer** are acceptor type dopants. The '508 patent confirms that p-type dopants are acceptor type dopants. Ex. 1001, 6:24-28 (explaining that p-type dopants are “acceptor-rich”), 3:26-31 (providing a “p-type GaN gate layer” over the AlGaN barrier layer).

f. [1e]:

“[1e1] depositing a gate contact layer on the doped GaN layer;

[1e2] applying a gate photo resistant pattern;

[1e3] etching away the gate contact layer outside the gate region;

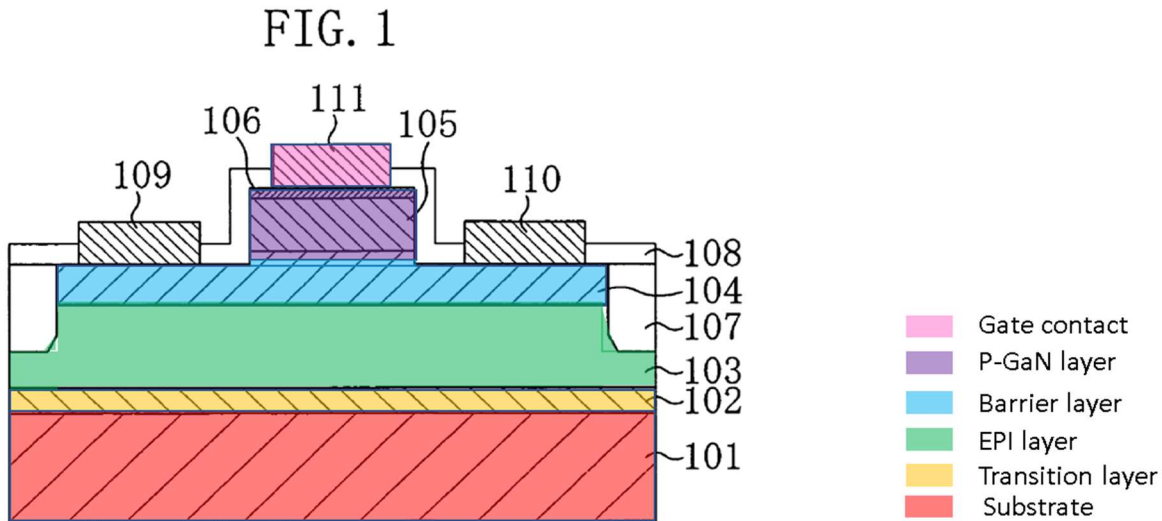
[1e4] etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;

[1e5] removing the gate photo resistant pattern;”

175. In my opinion, *Hikita-347* in view of *Beach* renders obvious element [1e]. *Hikita-347* discloses etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact ([1e4]), and *Beach* renders obvious all steps in element [1e].

176. *Hikita-347* discloses forming a **gate electrode 111** (gate contact) over the **p-type GaN layer 105**, as shown below. *Hikita-347*, [0013], [0034], [0061]. Although Figure 1 shows having a second p-type GaN layer 106 below the gate electrode 111, *Hikita-347* notes that it is “not necessary” to provide the second p-

type GaN layer 106, resulting in the gate electrode 111 formed directly over the p-type GaN layer 105. *Hikita-347*, [0040].



Hikita-347, Fig. 1 (annotated).

177. *Hikita-347* further discloses that, to form the p-type GaN layer 105 and gate contact 111, the portion of p-type GaN layer “located in other part than a gate region” is etched away. *Hikita-347*, [0035], [0057]. Although Figure 1 shows that the p-type GaN layer 105 extends beyond the gate contact 111, *Hikita-347* discloses in the description that the p-type GaN layer extending beyond the gate electrode is to be etched away. *Hikita-347*, [0035], [0057]. Thus, *Hikita-347* discloses step [1e4] “etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact.”

178. *Hikita-347* does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the p-type GaN layer and gate contact layer, nor

does Figure 1 show a p-GaN layer and gate electrode of the same width, but *Beach* renders this obvious.

179. As I explained in Ground 1, *Beach* discloses using a single mask to form a self-aligned gate and doped GaN layer with the steps of element [1e]. *Supra*, §XI.A.1.f. Like the *Yoshida* combination, *Hikita-347* and *Beach* disclose a GaN device where the doped GaN layer is etched away except the gate region. *Hikita-347*, [0035], [0057]; *Beach*, [0043]-[0048]; *Yoshida*, [0022]. In my opinion, a POSITA would have been motivated to apply *Beach*'s masking process to form the p-type GaN layer and gate contact layer in *Hikita-347*'s device and would have expected success for the same reasons I explained in Ground 1. *Supra*, §XI.A.1.f.

(a) A POSITA would have been motivated to apply *Beach*'s masking process to form *Hikita-347*'s device

180. *Hikita-347* and *Beach* are both directed to a GaN-based semiconductor device and methods for forming such a device. *Hikita-347*, [0013], [0033], [0038], [0040], [0055]-[0061]; *Beach*, [0002], [0017]-[0018]. Like *Hikita-347*, *Beach* discloses a GaN device with multiple layers of III-nitride material, such as a GaN layer 10, an AlGaN layer 12, and a highly doped GaN layer 16. *Beach*, [0040]-[0043]. Like *Hikita-347*'s device, *Beach*'s device has a gate contact 15 and ohmic contact 17. *Beach*, [0048]-[0049]. A POSITA would have been motivated to use the single mask process to form the gate contact and doped GaN

layer, as taught by *Beach*, to improve *Hikita-347*'s device and process in multiple ways.

181. First, *Beach*'s single mask process effectively achieves *Hikita-347*'s objective that the doped GaN layer is to be etched away except the gate region. *Hikita-347*, [0035], [0057]. A POSITA would have recognized that *Beach*'s single mask process automatically achieves self-alignment between the gate contact and the doped GaN layer and improves the gate's alignment in *Hikita-347*'s device. *See Beach*, Fig. 1E; *Hikita-347*, Fig. 1. A POSITA would have appreciated that self-aligned gate and doped GaN layer is a desired feature in GaN devices and would have been motivated to implement *Beach*'s single mask process to achieve a self-aligned gate arrangement in *Hikita-347*'s device. *See Beach-547*, [0043]-[0048] (describing self-aligned gates as advantageous); *Kouznetsov*, 3:42-61 (explaining that self-alignment decreases die size and cost).

182. Second, *Beach*'s single mask process to etch the gate contact and doped GaN layer simplifies *Hikita-347*'s process to form the GaN device. Compared to *Hikita-347*'s process which employs two separate masks and two separate steps to etch the gate contact and doped GaN layer, *Beach* uses a single mask to etch the gate and doped GaN layer which removes the additional step of applying a second mask for the gate contact. *Beach*, [0047]. A POSITA would have understood that applying an additional mask involves substantial undertaking

during manufacturing and the removal of one additional mask application leads to a simplified manufacturing process and saving of manufacturing cost. A POSITA would have been motivated to use *Beach*'s single mask process to produce *Hikita-347*'s device because doing so would simplify the manufacturing process and save manufacturing cost. *See Kouznetsov*, 3:55-61 (describing that uses the same photoresist mask to form the layers decreases process cost and complexity).

(b) A POSITA would have reasonably expected to succeed in applying *Beach*'s masking process to form *Hikita-347*'s device

183. Applying a single mask to form the gate contact and doped GaN layer was a well-known and conventional technique when the '508 patent was filed. The '508 patent states that the etching of the gate contact and p-GaN layer using the same mask is performed by "any known technique," because etching multiple layers of different materials using the same mask was routine, conventional, and well understood in the art. *Ex. 1001*, 3:45-50. Indeed, using the same mask to etch different layers of materials in semiconductor devices was known and implemented decades before the '508 patent. *Green*, 8:10-19 (etching the silicide layer and metal layer using a single mask), Figs. 6-7; *Spikes*, 4:39-5:3 (etching the metal layer, the polysilicon layer, and dielectric layer using a single mask), Figs. 1B-1C; *Shim*, 3:8-14 (etching the metal layer and silicon layer using a single mask), Figs. 2C-2D.

184. Both *Hikita-347*'s and *Beach*'s devices use the same GaN material for the layer underneath the gate contact. To the extent EPC argues that the dopants applied to *Beach*'s GaN layer (n-type dopants) are not the same type of dopants as *Hikita-347* (p-type dopants), a POSITA would have understood that the impurities caused by the dopants are so dilute that they do not change the etching characters of the GaN material, and as a result, a POSITA would have reasonably expected to succeed in applying *Beach*'s masking technique to etch the p-type GaN layer in *Hikita-347*'s device. *Hikita-347*'s device could be formed using the single mask technique described by *Beach*, according to the known, routine process of masking and etching. Using *Beach*'s single mask process to etch the gate contact and doped GaN layer in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner, because using the same mask to etch different layers of materials was routine, conventional, and well understood in

the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach*'s single mask process to form *Hikita-347*'s GaN device.

g. [1f]:

“[1f1] depositing a dielectric layer;

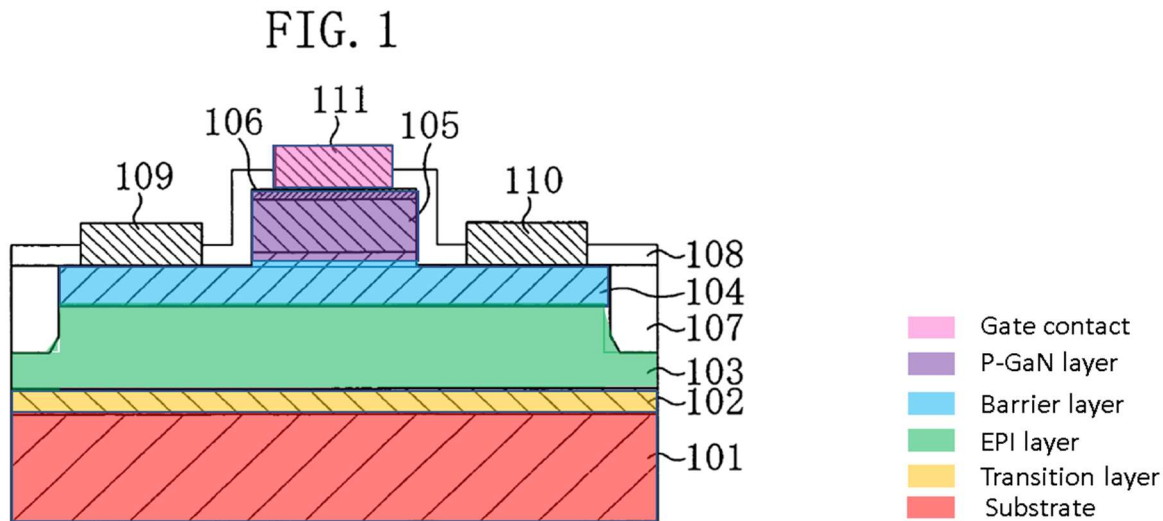
[1f2] applying a contact photo resistant pattern;

[1f3] etching the dielectric layer to open the drain and source contact area;

[1f4] removing the contact photo resistant pattern;”

185. In my opinion, *Hikita-347* in view of *Sheppard* renders obvious element [1f]. *Hikita-347* discloses depositing a dielectric layer and etching the dielectric layer to open the drain and source contact area ([1f1], [1f3]), and *Sheppard* renders obvious using a mask (contact photo resistant pattern) to open the drain and source contact area ([1f2], [1f4]).

186. *Hikita-347* discloses that, after etching away the p-type GaN layer, a “SiN film 108” was deposited which covers “an upper surface of the transistor,” as shown below. *Hikita-347*, [0034], [0037], [0059]. A POSITA would have understood that SiN (Silicon nitride), the same dielectric material as the '508 patent uses, is a material that has excellent dielectric properties and is commonly used as the dielectric material for semiconductor devices. Ex. 1001, 3:57-58. Thus, *Hikita-347* discloses step [1f1], i.e., depositing a dielectric layer.



Hikita-347, Fig. 1 (annotated).

187. *Hikita-347* further discloses performing etching to form openings in the dielectric layer (SiN film 108) for drain and source contacts. *Hikita-347*, [0034], [0060]. Thus, *Hikita-347* discloses step [1f3], i.e., etching the dielectric layer to open the drain and source contact area.

188. *Hikita-347* does not explicitly disclose using a mask (contact photo resistant pattern) to form the openings in the dielectric layer, but *Sheppard* renders this obvious.

189. *Sheppard* discloses using a mask pattern to form openings in a cap layer 24 for the Ohmic contacts (source/drain contacts). *Sheppard* describes providing a **mask 40** and etching the cap layer to open windows for ohmic contacts (source/drain contacts) according to the mask, as shown below. *Sheppard*, 8:55-67. *Sheppard* explains that the etching process results in exposure of areas of the

underlying barrier layer 22. *Sheppard*, 8:61-63. *Sheppard* also discloses that cap layer includes SiN, a dielectric material. *Sheppard*, 3:21-23. Thus, *Sheppard* discloses step [1f2], i.e., applying a contact photo resistant pattern.

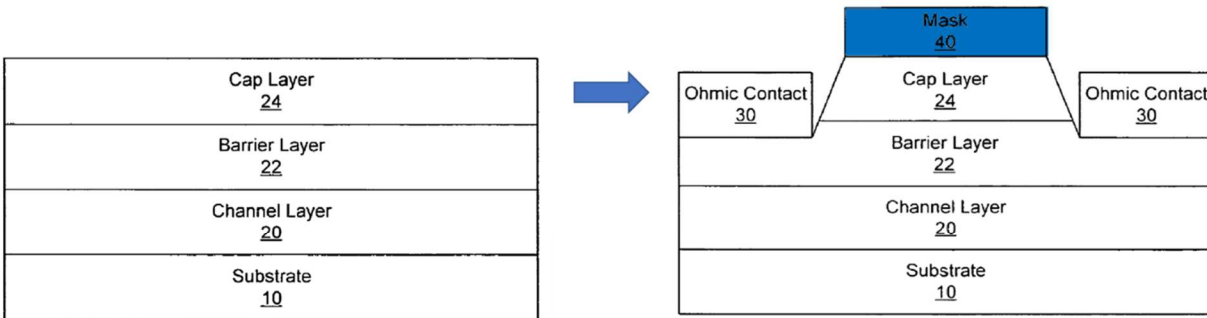


Figure 1B

Figure 1C

Sheppard, Figs. 1B, 1C (annotated).

190. *Sheppard* discloses that the mask 40 is removed after the Ohmic contacts are formed, as shown in Figure 1D where the mask 40 is no longer present. A POSITA would have also understood that, in semiconductor manufacturing, the masks used to pattern and form the device are to be removed because the masks are only tools to construct the device and not part of the device. *Ghandhi*, 12. Thus, *Sheppard* discloses step [1f4], i.e., removing the contact photo resistant pattern.

191. Thus, *Sheppard* discloses applying a mask (contact photo resistant pattern) to form openings in the dielectric layer and removing the mask afterwards.

In my opinion, it would have been obvious to apply *Sheppard*'s masking process to open the drain and source contact area in *Hikita-347*'s dielectric layer.

(a) A POSITA would have been motivated to apply *Sheppard*'s masking process to open drain and source contact area in *Hikita-347*'s device

192. *Hikita-347* and *Sheppard* are both directed to a GaN transistor with source and drain contacts and methods of forming such a device. *Hikita-347*, [0033]-[0035], [0055]-[0061]; *Sheppard*, 6:45-8:54. Like *Hikita-347*, *Sheppard* discloses a GaN device with source and drain contacts. *Sheppard*, 3:16-27, 9:42-46. A POSITA would have been motivated to use the masking process to open the drain and source contact area, as taught by *Sheppard*, to improve *Hikita-347*'s device and process in multiple ways.

193. First, *Sheppard*'s masking process effectively achieves *Hikita-347*'s objective to open the drain and source contact area in the dielectric layer. *Hikita-347*, [0034], [0060]. *Hikita-347* does not disclose how to perform etching of the dielectric layer to open the drain and source contact area, and a POSITA would have appreciated that *Sheppard*'s masking process would allow etching of the dielectric layer to open the drain and source contact area. A POSITA would have been motivated to adopt *Sheppard*'s masking process to effectively open the drain and source contact area in *Hikita-347*'s dielectric layer, such that the drain and

source contacts are formed for *Hikita-347*'s transistor to perform its intended functions.

194. Second, *Sheppard*'s masking process enables the drain and source contact area to be formed at the desired locations. A POSITA would have understood that *Sheppard*'s masking process allows control of the etching such that only the dielectric layer at desired areas is etched and leaving the other part of the dielectric layer intact. A POSITA would have understood that such precision and control is essential for manufacturing of any semiconductor device to ensure the device operates as intended. A POSITA would have been motivated to adopt *Sheppard*'s masking process to open the drain and source contact area at desired locations and leave the remaining part of the dielectric layer intact, such that *Hikita-347*'s transistor operates as intended.

(b) A POSITA would have reasonably expected to succeed in applying *Sheppard*'s masking process to open drain and source contact area in *Hikita-347*'s device

195. Using a mask to form openings in a dielectric layer of a semiconductor device was a well-known and conventional technique when the '508 patent was filed. *See Yoshida*, [0022]. The '508 patent does not explain how to apply a mask to etch the dielectric layer, because using a mask to pattern and etch a dielectric layer was routine, conventional, and well understood in the art.

See generally Ex. 1001. Both *Hikita-347*'s and *Sheppard*'s devices use a SiN material in the layer where etching is performed to open the source and drain contact area. *Hikita-347*, [0034], [0060]; *Sheppard*, 8:37-39 (the cap layer includes a SiN layer), 9:15-25 (including SiN and/or SiO₂ portions in the cap layer). *Hikita-347*'s drain and source contact area could be opened using the masking process described by *Sheppard*, according to the known, routine process of masking and etching. Using *Sheppard*'s masking process to etch the dielectric layer in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner, because using a mask to etch a dielectric material was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Sheppard*'s masking process to open drain and source contact area in *Hikita-347*'s device.

h. [1g]:

**“[1g1] depositing an Ohmic contact metal;
[1g2] applying a metal photo resistant pattern;
[1g3] etching the Ohmic contact metal;
[1g4] removing the metal photo resistant pattern; and
[1g5] performing rapid thermal annealing to form
Ohmic drain and source contacts.”**

196. In my opinion, *Hikita-347* in view of *Beach* renders obvious element [1g].

197. *Hikita-347* discloses depositing a Ti layer and an Al layer (Ohmic contact metal) on the n-undoped AlGaN layer 104 to form a source electrode 109 and a drain electrode 110 (Ohmic source and drain contacts). *Hikita-347*, [0034], [0060]. Thus, *Hikita-347* discloses step [1g1], i.e., depositing an Ohmic contact metal.

198. *Hikita-347* further discloses performing “heat treatment ... in an N₂ atmosphere at 650° C” to form the Ohmic source and drain contacts. *Hikita-347*, [0060]. Thus, *Hikita-347* disclose performing thermal annealing to form Ohmic drain and source contacts. To the extent EPC argues that *Hikita-347* does not explicitly disclose rapid thermal annealing, a POSITA would have found it obvious to perform rapid thermal annealing to form Ohmic source and drain contacts in *Hikita-347*’s devices (step [1g5]). A POSITA would have found performing rapid thermal annealing to activate ohmic contacts was routine and conventional long before the ’508 patent was filed, and would have had a reasonable expectation of success in doing so. Such technique was a conventional and commonly adopted technique in GaN semiconductor manufacturing to form a low-resistance ohmic contact in an efficient manner. *See Johnson*, [0085]; *Hu*, 1; *Chen*, [0087]; *Shimizu*, 1; *Ye*, [0061]. A POSITA would have been motivated to perform rapid thermal annealing instead of conventional furnace annealing to activate ohmic contacts because it was well known that rapid thermal annealing reduces thermal budget,

lowers manufacturing cost, and increases production throughput of the semiconductor devices. *See Campbell*, 6; *Ye*, [0061]; *Hu*, 1. A POSITA would have been motivated to perform rapid thermal annealing to activate ohmic contacts because it was known to improve the structural and optoelectronic properties of GaN materials, as well as providing a smoother surface of the contact which improves circuit yield. *Zhu*, 5; *Campbell*, 9. Therefore, it would have been obvious to perform rapid thermal annealing to activate the Ohmic contacts in *Hikita-347*'s devices.

199. *Hikita-347* does not explicitly disclose a masking and etching process for forming the Ohmic source and drain contacts, but *Beach* discloses using a masking and etching process ([1g2], [1g3], [1g4]) to form Ohmic contacts as explained in Ground 1. *Supra*, §XI.A.1.h; *Beach*, [0045]-[0047].

200. In my opinion, it would have been obvious to use *Beach*'s masking and etching process to form *Hikita-347*'s Ohmic source and drain contacts. Like the *Yoshida* combination, *Hikita-347* and *Beach* disclose forming source and drain contacts using ohmic metal. *Hikita-347*, [0034], [0060]; *Beach*, [0048]-[0049]; *Yoshida*, [0010], [0022]. A POSITA would have been motivated to apply *Beach*'s source and drain masking process to form the source and drain contacts in *Hikita-347*'s device and would have expected success for the same reasons I explained in Ground 1. *Supra*, §XI.A.1.h.

(a) A POSITA would have been motivated to apply *Beach*'s masking process to form *Hikita-347*'s Ohmic source and drain contacts

201. *Hikita-347* and *Beach* are both directed to a GaN-based semiconductor device and methods for forming such a device. *Hikita-347*, [0033]-[0035], [0055]-[0061]; *Beach*, [0002], [0017]-[0018]. Like *Hikita-347*, *Beach* discloses a GaN device with multiple layers of III-nitride material, such as a GaN layer 10, an AlGaN layer 12, and a highly doped GaN layer 16. *Beach*, [0040]-[0043]. Similar to *Hikita-347*'s device, *Beach*'s device has a gate contact 15 and ohmic contact 17. *Beach*, [0048]-[0049]. A POSITA would have been motivated to use the masking process to form the Ohmic source and drain contacts, as taught by *Beach*, to improve *Hikita-347*'s device and process in multiple ways.

202. First, *Beach*'s masking process effectively achieves *Hikita-347*'s objective to form the source and drain electrodes (Ohmic source and drain contacts) at the openings in the dielectric layer. *Hikita-347*, [0034], [0060]. *Hikita-347* does not disclose how the source and drain electrodes (Ohmic source and drain contacts) are formed at the openings, and a POSITA would have appreciated that *Beach*'s masking process would produce the Ohmic source and drain contacts in *Hikita-347*'s transistor. A POSITA would have been motivated to adopt *Beach*'s masking process to effectively form the Ohmic source and drain contacts in *Hikita-*

347's transistor, such that *Hikita-347*'s transistor would perform its intended functions.

203. Second, *Beach*'s masking process is simpler compared to the other alternative process, such as the lift-off process, to form the Ohmic source and drain contacts. A POSITA would have understood that *Beach*'s masking process avoids manufacturing of the vertical profile of photoresist shape used in the lift-off process, thereby saving the manufacturing cost to produce *Hikita-347*'s transistor. A POSITA would have been motivated to use *Beach*'s masking process to produce *Hikita-347*'s Ohmic source and drain contacts because doing so would simplify the manufacturing process and save manufacturing cost.

204. Third, *Beach*'s masking process allows a source and gate connected field plate to be easily formed, which reduces electrical field at the gate corner and results in higher breakdown voltage at *Hikita-347*'s device. *See, e.g., Kumar*, 4 (describing significant improvement in breakdown voltage with the field plate); *Saito*, 1 (describing that the field plate structure is effective for the high breakdown voltage HEMT design); *Hikita-895*, [0046] (describing the transistor with a field plate has an enhanced breakdown voltage). A POSITA would have appreciated that, applying *Beach*'s masking process, a field plate can be easily formed by using a mask pattern that extends over the gate contact, such that a portion of the Ohmic metal between the source Ohmic contact and gate contact is not etched away. In

contrast, the other alternative process, such as the lift-off process, requires a separate masking step to allow the source Ohmic contact metal to extend beyond the designated opening for source contact, and as a result, requires additional processing to provide a field plate design. *See, e.g., Kumar*, 1 (applying additional steps including patterning the gate with e-beam lithography and e-beam evaporation to form the field plate); *Saito*, 2 (forming a separate field plate electrode after forming source and drain ohmic contacts using a lift off process); *Hikita-895*, [0056]-[0057] (forming a separate field plate electrode with another liftoff process after first forming source and drain electrodes by a lift off method). Therefore, a POSITA would have been motivated to use *Beach*'s masking process to produce *Hikita-347*'s Ohmic source and drain contacts to provide a field plate in *Hikita-347*'s device in a simple manner.

(b) A POSITA would have reasonably expected to succeed in applying *Beach*'s masking process to form *Hikita-347*'s Ohmic source and drain contacts

205. Using a mask (metal photo resist pattern) to pattern and etch Ohmic contact metal to form source and drain contacts was a well-known and conventional technique when the '508 patent was filed. The '508 patent does not explain how to apply a mask to etch Ohmic contact metal, because using a mask to pattern and etch Ohmic contact metal was routine, conventional, and well understood in the art. *See generally* Ex. 1001. Both *Hikita-347*'s and *Beach*'s

devices use a III Nitride material for the layer underneath the Ohmic source and drain contacts. *Hikita-347*'s Ohmic source and drain contacts could be formed using the masking process described by *Beach*, according to the known, routine process of masking and etching. Using *Beach*'s masking process to etch the Ohmic contact metal in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner, because using a mask to etch an Ohmic contact metal was routine, conventional, and well understood in the art. Both *Yoshida*'s and *Beach*'s devices use ohmic contact metal to form source and drain contacts which could be etched with the same techniques. *Yoshida*, [0022], [0010] (metal Al); *Beach*, [0045] ("ohmic metal"). Thus, a POSITA would have reasonably expected to succeed in using *Beach*'s masking process to form *Hikita-347*'s Ohmic source and drain contacts.

2. [Claim 2] "wherein the EPI layer is comprised of InAlGaN."

206. Claim 2 depends from claim 1. In my opinion, *Sheppard* renders obvious that the EPI layer is comprised of InAlGaN.

207. *Hikita-347* does not explicitly disclose that the EPI layer (layer 103) is comprised of InAlGaN. However, *Sheppard* does. For example, *Sheppard* discloses that the channel layer 20 (EPI layer) is an AlInGaN material. *Sheppard*, 7:40-41. A POSITA would have understood that *Sheppard*'s channel layer 20 corresponds to the "EPI layer" because, like the EPI layer in the '508 patent, the

channel layer 20 is provided under the barrier layer 22, and together they form a two-dimensional electron gas. *Sheppard*, 7:47-8:3, Fig. 3.

208. It would have been obvious to use an InAlGa_N material for the EPI layer of *Hikita-347*'s device, as disclosed by *Sheppard*. A POSITA would have been motivated to use InAlGa_N for the EPI layer to increase the breakdown voltage of *Hikita-347*'s transistor. It was known that some alloys of the InAlGa_N material have higher critical electric field strengths in comparing with that of Ga_N, resulting in a larger breakdown voltage of the transistor. A POSITA would have also been motivated to include an InAlGa_N for the EPI layer to construct a quantum well in *Hikita-347*'s transistor, such that the gate length of the transistor can be shortened for use in high frequency applications. *Ambacher*, 1 (constructing a quantum well structure using a compound with Indium Gallium Nitride). A POSITA would have further understood that using InAlGa_N is merely an obvious design choice to form an EPI layer of *Hikita-347*'s transistor because the Group III nitride family includes combinations of Al (Aluminum), In (Indium), Ga (Gallium) with Nitride, and a combination of Al, In, and Ga with Nitride is an obvious combination from elements of the Group III nitride family. *See Yoshida*, [0012]; *Sheu*, 6 (providing AlInGa_N in each layer of a Ga_N-based transistor). The '508 patent does not identify a specific composition of the InAlGa_N compound or state any differentiating characteristics or purpose for using the InAlGa_N compound in

the EPI layer. The only instance the InAlGa_N material appears in the '508 patent is in a generic statement that the EPI layer 13 is made of a "III Nitride material" and "can be composed of In_xAl_yGa_{1-x-y}N, where $x+y \leq 1$." Ex. 1001, 3:23-25. A POSITA would have reasonably expected to succeed in using InAlGa_N for the EPI layer of *Hikita-347*'s transistor because using InAlGa_N to form an EPI layer routine, conventional, and well understood in the art. *See Yoshida*, [0012]; *Sheu*, 6 (providing AlInGa_N in each layer of a Ga_N-based transistor). The '508 patent does not explain how to grow InAlGa_N in an EPI layer, because growing InAlGa_N in an EPI layer was routine, conventional, and well understood in the art. *See generally* Ex. 1001. Using *Sheppard*'s InAlGa_N for an EPI layer in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner. Thus, a POSITA would have reasonably expected to succeed in using *Sheppard*'s InAlGa_N for an EPI layer in *Hikita-347*'s device.

3. [Claim 3] "the barrier layer is comprised of InAlGa_N with a larger band gap than the buffer layer."

209. Claim 3 depends from claim 1. In my opinion, *Hikita-347* in view of *Sheppard* renders it obvious that the barrier layer is comprised of InAlGa_N with a larger band gap than the buffer layer.

210. *Hikita-347* discloses that the barrier layer has a larger band gap than the buffer layer in order to form a two dimensional electron gas. *Hikita-347*, [0009]

(the second nitride semiconductor layer, i.e., the barrier layer, has a larger band gap energy than the first nitride semiconductor layer, i.e., the buffer layer);

211. *Hikita-347* does not explicitly disclose that the barrier layer (layer 104) is comprised of InAlGaN. However, *Sheppard* does. For example, *Sheppard* discloses that the barrier layer 22 is an AlInGaN material. *Sheppard*, 7:52-54. *Sheppard* also discloses that the barrier layer 22 has a larger band gap than the channel layer 20 (buffer layer). *Sheppard*, 8:4-9.

212. In my opinion, it would have been obvious to use an InAlGaN material that has a larger band gap than the buffer layer as the barrier layer of *Hikita-347*'s device, as disclosed by *Sheppard*. A POSITA would have been motivated to use InAlGaN for the barrier layer to increase the device performance with reduced strain because it was known that InAlGaN is better lattice matched with the GaN materials in *Hikita-347*'s transistor. *Liu*, 1 (InAlGaN as a barrier layer reduces the built-in strain and increases polarization). A POSITA would have further understood that using InAlGaN is merely an obvious design choice to form a barrier layer of *Hikita-347*'s transistor because the Group III nitride family includes a combination of Al (Aluminum), In (Indium), Ga (Gallium) with Nitride, and a combination of Al, In, and Ga with Nitride is an obvious combination from elements of the Group III nitride family. *See Yoshida*, [0013]; *Sheu*, 6 (providing AlInGaN in each layer of a GaN-based transistor). The '508 patent does not

identify a specific composition of the InAlGaN compound or state any differentiating characteristics or purpose for using the InAlGaN compound in the barrier layer. The only instance the InAlGaN material appears in the '508 patent is in a generic statement that the barrier layer 14 is made of a "III Nitride material" and "can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$." Ex. 1001, 3:23-25.

213. A POSITA would have reasonably expected to succeed in using InAlGaN for the barrier layer of *Hikita-347*'s transistor because using InAlGaN to form a barrier layer was routine, conventional, and well understood in the art. *See Yoshida*, [0013]; *Sheu*, 6. The '508 patent does not explain how to grow InAlGaN in a barrier layer, because growing InAlGaN in a barrier layer was routine, conventional, and well understood in the art. *See generally* Ex. 1001. Using *Sheppard*'s InAlGaN for a barrier layer in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner. Thus, a POSITA would have reasonably expected to succeed in using *Sheppard*'s InAlGaN for a barrier layer in *Hikita-347*'s device.

4. Independent Claim 4

214. In my opinion, the combination of *Hikita-347*, *Sheppard*, and *Beach* renders claim 4 obvious.

215. As I explain below, *Hikita-347* discloses growing various layers to form the device in claim 4 ([4a] through [4e]). *Hikita-347* does not explicitly

disclose forming multiple transition layers ([4a]), using an InAlGa_N for the EPI layer, the barrier layer, and first p-type layer ([4b]-[4d]), or the masking steps ([4f], [4g], [4h]) to etch the metal and p-type GaN-based layers, open the drain and source contact area, and form the Ohmic drain and source contacts.

216. A POSITA would have found it obvious to form a p-type InAlGa_N layer as the first p-type layer in *Hikita-347* ([4d]) as the InAlGa_N p-type layer could be formed merely by switching in the p-type dopant during growth when InAlGa_N of the same composition is used for the barrier layer. *Sheppard* renders obvious forming multiple transition layers on a substrate ([4a]), using InAlGa_N as a material for the EPI layer and barrier layer ([4b], [4c]), and the masking steps ([4g]) to open the drain and source contact area. And *Beach* renders obvious the masking steps to etch the gate metal and p-type GaN-based layers ([4f]) and the masking steps to form the Ohmic drain and source contacts ([4h]).

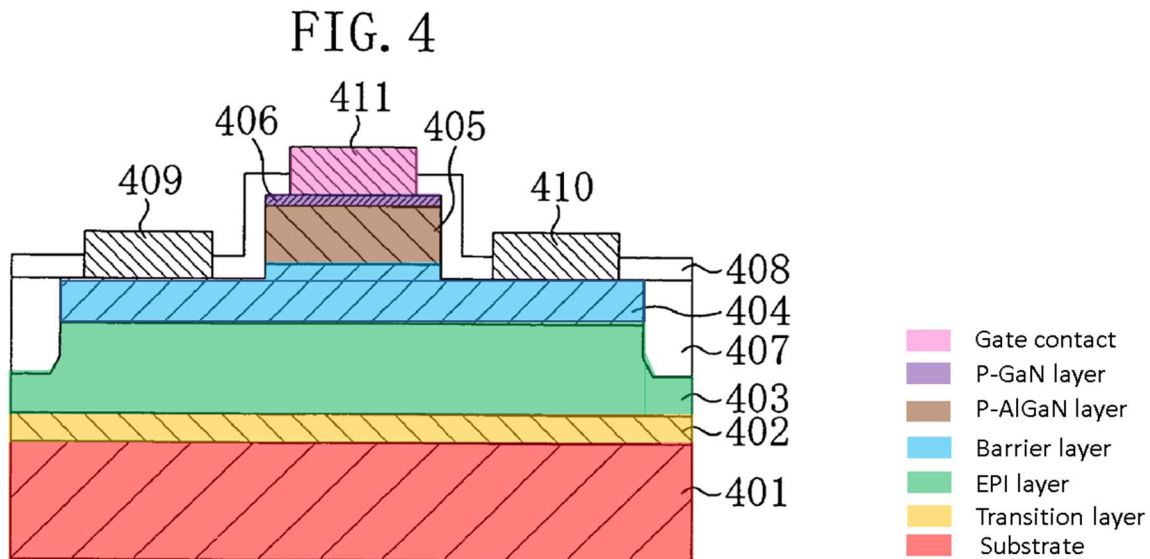
a. [4pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”

217. As I discussed above for [1pre], *Hikita-347* discloses this limitation. *Supra*, §XI.B.1.a.

b. [4a]: “nucleating and growing transition layers on a substrate;”

218. As I discussed above for [1a], *Hikita-347* in view of *Sheppard* renders obvious this limitation. *Hikita-347* discloses nucleating and growing an **AlN**

buffer layer 402 (transition layer) over a **substrate 401**, as shown below, and for the same reasons I discussed above in [1a], *Sheppard* renders obvious providing multiple transition layers on the substrate. *Hikita-347*, [0048], [0056]; *supra*, §XI.B.1.b.



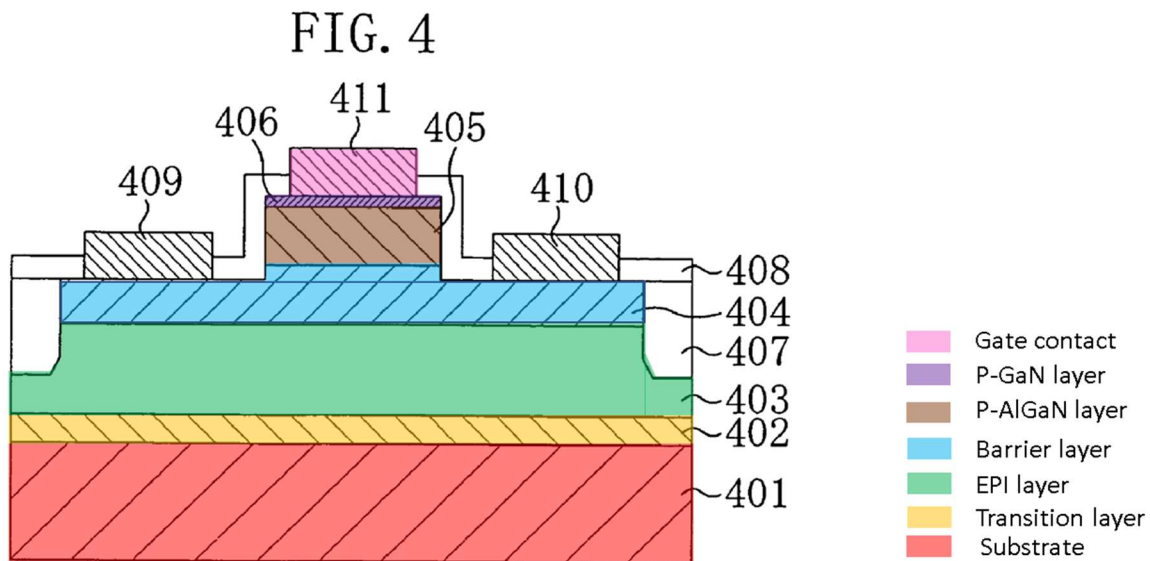
Hikita-347, Fig. 4 (annotated).

c. [4b]: “growing an InAlGaN EPI layer over the transistor layers;”

219. In my opinion, *Hikita-347* in view of *Sheppard* renders obvious this limitation.⁴ *Hikita-347* discloses growing an **undoped GaN layer 403** over the

⁴ The “transistor layers” in [4b] lacks an antecedent basis. It appears that “the transistor layers” refers to the “transition layers” in [4a] because the ’508 patent

buffer layer 402 (transition layer), as shown below, and for the same reasons I discussed in claim 2, *Sheppard* renders obvious that the EPI layer is comprised of InAlGa_N. *Hikita-347*, [0048], [0056]; *supra*, §XI.B.2. Thus, *Hikita-347* in view of *Sheppard* renders obvious growing an InAlGa_N EPI layer over the transition layers.

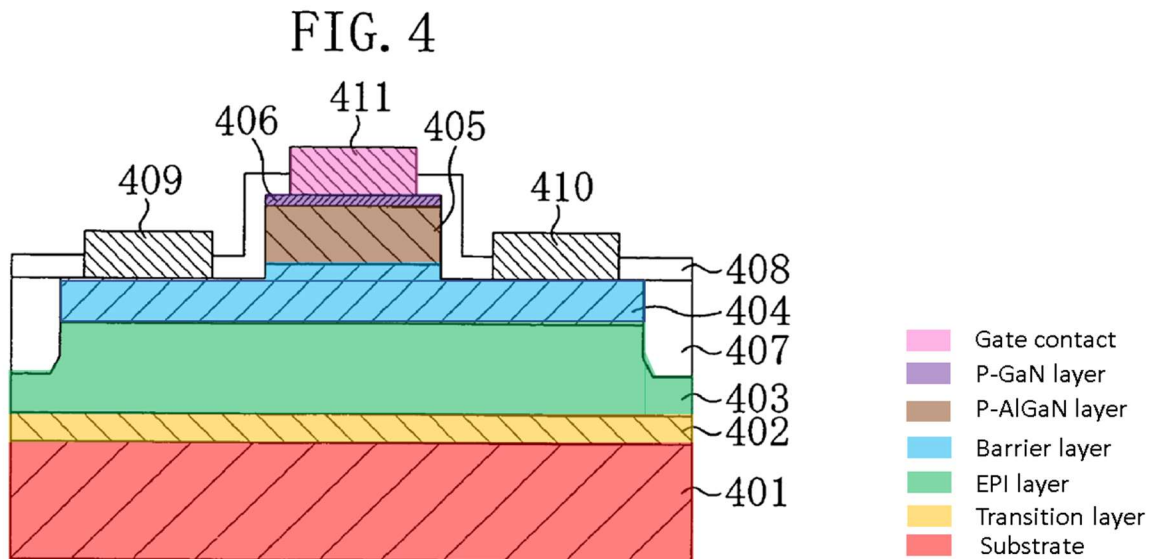


Hikita-347, Fig. 4 (annotated).

does not describe any “transistor layers.” The ’508 patent describes an III Nitride EPI layer 13 over the transition layers 12. Ex. 1001, 4:28-36, Figs. 4, 5A. I consider the “transistor layers” as the “transition layers” in [4a] in my opinions here.

d. [4c]: “growing an InAlGaN barrier layer over the InAlGaN EPI layer;”

220. In my opinion, *Hikita-347* in view of *Sheppard* renders obvious this limitation. As I discussed above for [1c], *Hikita-347* discloses growing an **undoped AlGaN layer 404** (barrier layer) over the EPI layer, as shown below, and for the same reasons I discussed in claim 3, *Sheppard* renders obvious that the barrier layer is comprised of InAlGaN. *Hikita-347*, [0048], [0056]; *supra*, §§XI.B.1.d, XI.B.3. Thus, *Hikita-347* in view of *Sheppard* renders obvious growing an InAlGaN barrier layer over the InAlGaN EPI layer.

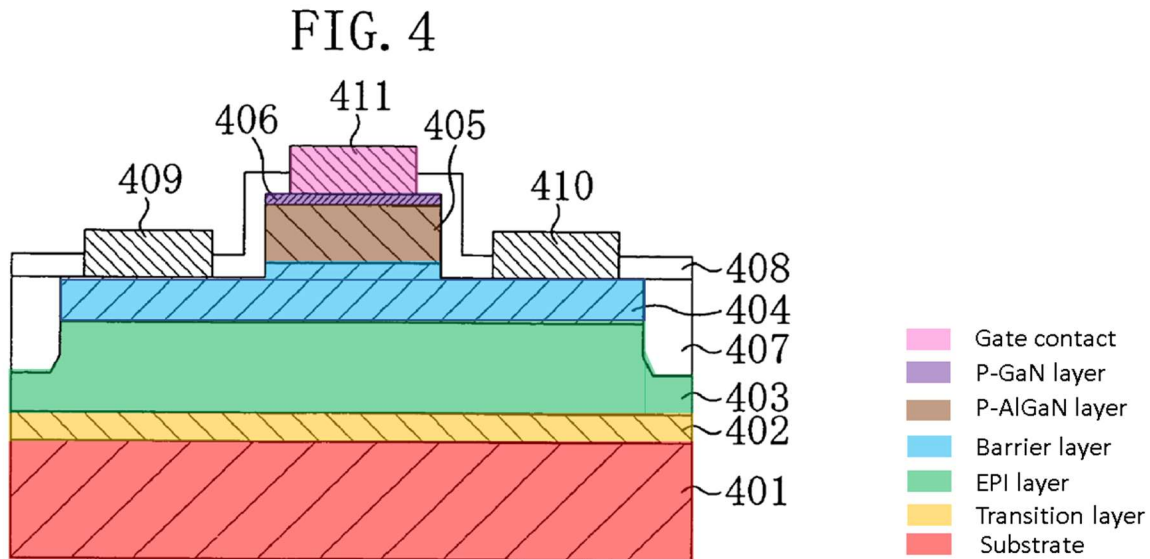


Hikita-347, Fig. 4 (annotated).

e. [4d]: “growing an InAlGaN layer with acceptor type dopants over the InAlGaN barrier layer;”

221. In my opinion, *Hikita-347* renders obvious this limitation.

222. For example, *Hikita-347* discloses growing a first doped layer, **p-type AlGa_N layer 405**, over the barrier layer, as shown below. *Hikita-347*, [0048], [0056].

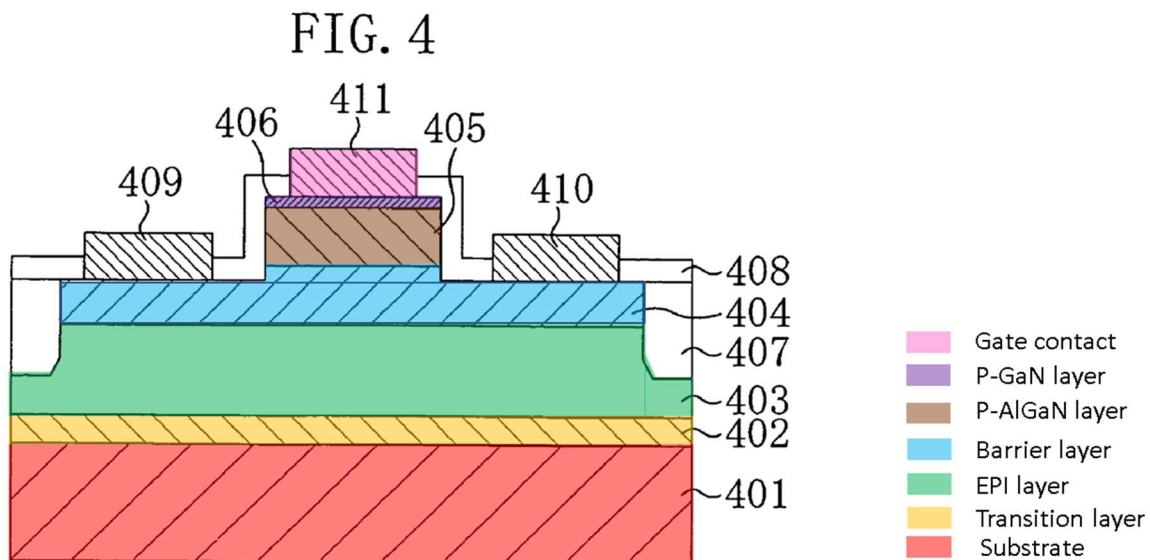


223. In my opinion, it would have been obvious to use an InAlGa_N material for the first doped layer (first p-type layer over the barrier layer) of *Hikita-347*'s device. A POSITA would have understood that using InAlGa_N is merely an obvious design choice to form the layer over the barrier layer of *Hikita-347*'s transistor because the Group III nitride family includes combination of Al (Aluminum), In (Indium), Ga (Gallium) with Nitride, and a combination of Al, In, and Ga with Nitride is an obvious combination from elements of the Group III nitride family. See *Sheu*, 9-10 (providing a doped AlInGa_N layer 318 over the

barrier layer 310); *Mizutani*, [0028], [0031] (providing a p-type InGaAlN layer as the field generating layer under the gate). The '508 patent does not identify a specific composition of the InAlGa_N compound or state any differentiating characteristics or purpose for using the p-type InAlGa_N compound as the layer over the barrier layer. The only instance the InAlGa_N material appears in the '508 patent is in a generic statement that the EPI layer 13, barrier layer 14, and p-type gate layer 15 are made of a "III Nitride material" and "can be composed of In_xAl_yGa_{1-x-y}N, where x+y≤1." Ex. 1001, 3:23-25. When an InAlGa_N layer is provided as the barrier layer underneath, it would have been obvious to a POSITA to use the p-type InAlGa_N over the InAlGa_N barrier layer, because using the same material would simplify the manufacturing process and cost. A POSITA would have been motivated to form a p-type InAlGa_N layer as the first p-type layer in *Hikita-347* because the p-type InAlGa_N layer could be formed merely by switching in the p-type dopant during growth when InAlGa_N of the same composition is used for the barrier layer. And a POSITA would have had a reasonable expectation of success in doing so because using InAlGa_N to form a p-type layer over the barrier layer was routine, conventional, and well understood in the art, as described in *Sheu* and *Mizutani*.

f. [4e]: “growing a GaN layer with acceptor type dopants over the doped InAlGaN layer;”

224. In my opinion, *Hikita-347* renders obvious this limitation. *Hikita-347* discloses growing a second doped layer, **p-type GaN layer 406**, over the **first p-type layer 405**, as shown below. *Hikita-347*, [0048], [0056]. As I discussed in [4d], it would have been obvious to use a p-type InAlGaN for the first p-type layer in *Hikita-347*.



Hikita-347, Fig. 4 (annotated).

g. [4f]:

“[4f1] depositing a gate contact layer on the doped GaN layer

[4f2] applying a gate photo resistant pattern;

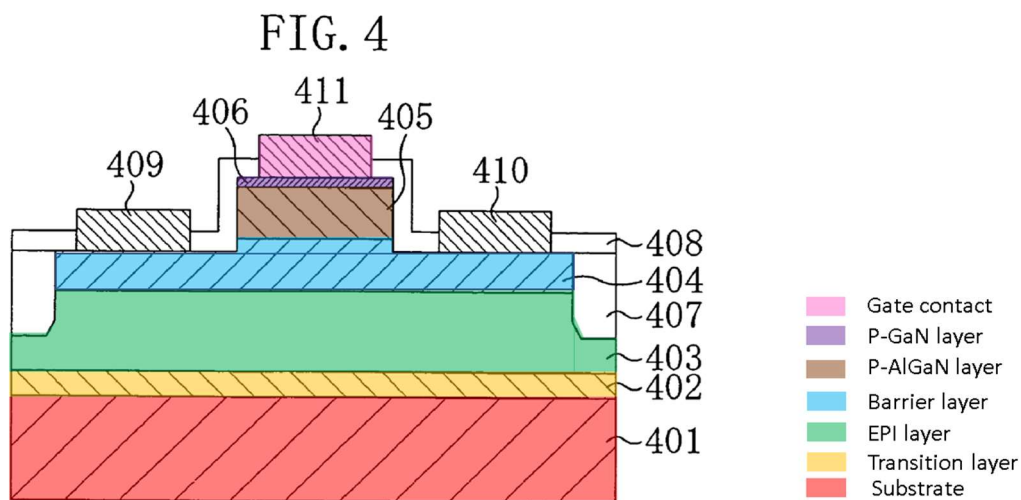
[4f3] etching away the gate contact layer outside the gate region;

[4f4] etching away the doped GaN layer and the doped InAlGaN layer, except for portions of the doped GaN layer and the doped InAlGaN layer beneath gate contact;

[4f5] removing the gate photo resistant pattern;”

225. In my opinion, *Hikita-347* in view of *Beach* renders obvious element [4f]. *Hikita-347* discloses etching away the first and second doped layers, except a portion of the layers beneath the gate contact ([4f4]), and *Beach* renders obvious all steps in element [4f].

226. *Hikita-347* discloses forming a **gate electrode 411** (gate contact) over the **p-type GaN layer 406**, as shown below. *Hikita-347*, [0013], [0034], [0061].



Hikita-347, Fig. 4 (annotated).

227. *Hikita-347* further discloses that, to form the first and second p-type layers 405 and 406 and gate contact 411, the portion of first and second p-type layers “located in other part than a gate region” is etched away. *Hikita-347*, [0057]. Although Figure 4 shows that the first and second p-type layers 405 and 406 extend beyond the gate contact 111, *Hikita-347* discloses in the description that the first and second p-type layers extending beyond the gate electrode are to be etched away. *Hikita-347*, [0057]. *Hikita-347* discloses the first and second p-type layers 405 and 406 being p-type AlGa_N layer and p-type Ga_N layer respectively, and as I discussed in [4d], it would have been obvious to use p-type InAlGa_N for the first p-type layer. Thus, *Hikita-347* renders obvious step [4f4] “etching away the doped Ga_N layer and the doped InAlGa_N layer, except for portions of the doped Ga_N layer and the doped InAlGa_N layer beneath gate contact.”

228. *Hikita-347* does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the first and second p-type layers and gate contact layer, but *Beach* renders this obvious.

229. As I explained in Ground 1, *Beach* discloses using a single mask to form a self-aligned gate and doped Ga_N layer with the steps of element [4f]. *Supra*, §XI.A.1.f. The ’508 patent admitted that it was known in the art to use a same mask to etch a first and a second doped layers. Ex. 1001, 1:65-2:3. *Hikita-347* discloses that both p-type layers are etched away in part other than the gate

region. *Hikita-347*, [0057]. A POSITA would have been motivated to use *Beach*'s single mask process to form the gate contact and p-type GaN layer(s) in *Hikita-347*'s device and would have expected success for the same reasons I explained in [1e]. *Supra*, §XI.B.1.f.

(a) A POSITA would have been motivated to apply *Beach*'s masking process to form *Hikita-347*'s device

230. *Hikita-347* and *Beach* are both directed to a GaN-based semiconductor device and methods for forming such a device. *Hikita-347*, [0013], [0033], [0038], [0040], [0055]-[0061]; *Beach*, [0002], [0017]-[0018]. Like *Hikita-347*, *Beach* discloses a GaN device with multiple layers of III-nitride material, such as a GaN layer 10, an AlGaN layer 12, and a highly doped GaN layer 16. *Beach*, [0040]-[0043]. Like *Hikita-347*'s device, *Beach*'s device has a gate contact 15 and ohmic contact 17. *Beach*, [0048]-[0049]. A POSITA would have been motivated to use the single mask process to form *Hikita-347*'s gate contact and first and second doped layers, as taught by *Beach*, to improve *Hikita-347*'s device and process in multiple ways.

231. First, *Beach*'s single mask process effectively achieves *Hikita-347*'s objective that the first and second doped layers are to be etched away except the gate region. *Hikita-347*, [0057]. A POSITA would have recognized that *Beach*'s single mask process automatically achieves self-alignment between the gate

contact and the first and second doped layers and improves the gate's alignment in *Hikita-347*'s device. See *Beach*, Fig. 1E; *Hikita-347*, Fig. 4. A POSITA would have appreciated that self-aligned gate and doped layers is a desired feature in GaN devices and would have been motivated to implement *Beach*'s single mask process to achieve a self-aligned gate arrangement in *Hikita-347*'s device. See *Beach-547*, [0043]-[0048] (describing self-aligned gates as advantageous); *Kouznetsov*, 3:42-61 (explaining that self-alignment decreases die size and cost).

232. Second, *Beach*'s single mask process to etch the gate contact and doped GaN layers simplifies *Hikita-347*'s process to form the GaN device. Compared to *Hikita-347*'s process which employs two separate masks and two separate steps to etch the gate contact and doped GaN layers, *Beach* uses a single mask to etch the gate and doped GaN layer which removes the additional step of applying a second mask for the gate contact. *Beach*, [0047]. A POSITA would have understood that applying an additional mask involves substantial undertaking during manufacturing and the removal of one additional mask application leads to a simplified manufacturing process and saving of manufacturing cost. A POSITA would have been motivated to use *Beach*'s single mask process to produce *Hikita-347*'s device because doing so would simplify the manufacturing process and save manufacturing cost. See *Kouznetsov*, 3:55-61 (describing that uses the same photoresist mask to form the layers decreases process cost and complexity).

(b) A POSITA would have reasonably expected to succeed in applying *Beach*'s masking process to form *Hikita-347*'s device

233. Applying a single mask to form the gate contact and doped GaN layers was a well-known and conventional technique when the '508 patent was filed. The '508 patent does not explain how to perform etching of the gate contact and p-GaN layers using the same mask, because etching multiple layers of different materials using the same mask was routine, conventional, and well understood in the art. Ex. 1001, 4:41-44. Indeed, using the same mask to etch different layers of materials in semiconductor devices was known and implemented decades before the '508 patent. *Green*, 8:10-19 (etching the silicide layer and metal layer using a single mask), Figs. 6-7; *Spikes*, 4:39-5:3 (etching the metal layer, the polysilicon layer, and dielectric layer using a single mask), Figs. 1B-1C; *Shim*, 3:8-14 (etching the metal layer and silicon layer using a single mask), Figs. 2C-2D.

234. Both *Hikita-347*'s and *Beach*'s devices use the same GaN material for the layer underneath the gate contact. To the extent EPC argues that the dopants applied to *Beach*'s GaN layer (n-type dopants) are not the same type of dopants as *Hikita-347* (p-type dopants), a POSITA would have understood that the impurities caused by the dopants are so dilute that they do not change the etching characters of the GaN material, and as a result, a POSITA would have reasonably expected to

succeed in applying *Beach*'s masking technique to etch the p-type GaN-based layers in *Hikita-347*'s device. *Hikita-347*'s device could be formed using the single mask technique described by *Beach*, according to the known, routine process of masking and etching. The '508 patent also admits that it was known in the art to use a same mask to etch a first and a second doped layers. Ex. 1001, 1:65-2:3. Using *Beach*'s single mask process to etch the gate contact and doped GaN-based layers in *Hikita-347*'s device would have required only conventional techniques in their ordinary and expected manner, because using the same mask to etch multiple layers of materials was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach*'s single mask process to form *Hikita-347*'s GaN device.

h. [4g]:

- “[4g1] depositing a dielectric layer;**
- [4g2] applying a contact photo resistant pattern;**
- [4g3] etching the dielectric layer to open the drain and source contact area;**
- [4g4] removing the contact photo resistant pattern;**

235. In my opinion, *Hikita-347* in view of *Sheppard* renders obvious [4g]. *Hikita-347* discloses depositing a dielectric layer and etching the dielectric layer to open the drain and source contact area ([4g1], [4g3]), and *Sheppard* renders obvious using a mask (contact photo resistant pattern) to open the drain and source contact area ([4g2], [4g4]).

236. *Hikita-347* discloses that, after etching away the p-type GaN layer, depositing a “SiN film 408” (dielectric layer) and performing etching to form “openings” in the SiN film 408 for drain and source contacts, as shown below. *Hikita-347*, [0059], [0061]. Thus, *Hikita-347* discloses steps [4g1] and [4g3], i.e., depositing a dielectric layer and etching the dielectric layer to open the drain and source contact area.

237. *Hikita-347* does not explicitly disclose using a mask (contact photo resistant pattern) to form the openings in the dielectric layer, but as I discussed above in [1f] *Sheppard* renders this obvious. *Supra*, §XI.B.1.g.

i. [4h]:

**“[4h1] depositing an Ohmic contact metal;
[4h2] applying a metal photo resistant pattern;
[4h3] etching the Ohmic contact metal;
[4h4] removing the metal photo resistant pattern; and
[4h5] performing rapid thermal annealing to form
Ohmic drain and source contacts.”**

238. In my opinion, *Hikita-347* in view of *Beach* renders obvious element [4h].

239. For example, *Hikita-347* discloses depositing a Ti layer and an Al layer (Ohmic contact metal) on the n-undoped AlGaIn layer 404 to form a source electrode 409 and a drain electrode 410 (Ohmic source and drain contacts). *Hikita-*

347, [0060]. Thus, *Hikita-347* discloses step [4h1], i.e., depositing an Ohmic contact metal.

240. *Hikita-347* further discloses performing “heat treatment ... in an N₂ atmosphere at 650° C” to form the Ohmic source and drain contacts. *Hikita-347*, [0060]. Thus, *Hikita-347* disclose performing thermal annealing to form Ohmic drain and source contacts. As I discussed above in [1g], a POSITA would have found it obvious to perform rapid thermal annealing to form Ohmic source and drain contacts in *Hikita-347*’s devices (step [4h5]). *Supra*, §XI.B.1.h.

241. *Hikita-347* does not explicitly disclose a masking and etching process for forming the Ohmic source and drain contacts, but *Beach* renders obvious using a masking and etching process ([4h2], [4h3], [4h4]) to form Ohmic contacts as I explained above in [1g]. *Supra*, §XI.B.1.h.

C. Ground 3: Claim 5 Is Obvious over *Hikita-023*, *Beach*, and *Sheppard*

1. Independent Claim 5

242. In my opinion, the combination of *Hikita-023*, *Sheppard*, and *Beach* renders claim 5 obvious.

243. As I explain below, *Hikita-023* discloses growing various layers to form the device in claim 5 ([5a] through [5e]). *Hikita-023* does not explicitly disclose forming multiple transition layers ([5a]), using an InAlGa_N for the EPI layer ([5b]), or the masking steps ([5f], [5g], [5h]) to etch the metal and p-type

GaN-based layers, open the drain and source contact area, and form the Ohmic drain and source contacts.

244. *Sheppard* renders obvious forming multiple transition layers on a substrate ([5a]), using InAlGaN as a material for the EPI layer ([5b]), and the masking steps ([5g]) to open the drain and source contact area. And *Beach* renders obvious the masking steps to etch the gate metal and p-GaN layer ([5f]) and the masking steps to form the Ohmic drain and source contacts ([5h]).

a. [5pre]: “A method of forming an enhancement mode GaN transistor, the method comprising:”

245. In my opinion, *Hikita-023* discloses a method of forming an enhancement mode GaN transistor.

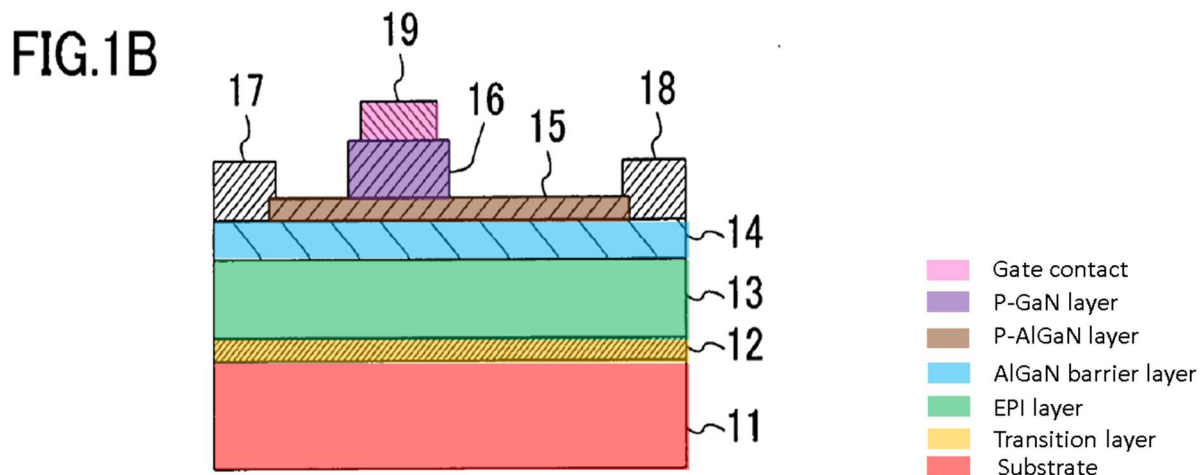
246. *Hikita-023* discloses a “normally-off” type GaN transistor with a p-type GaN layer below the gate, constituting an enhancement mode GaN transistor. *Hikita-023*, [0037], [0051], [0073]. *Hikita-023* further discloses a method of forming such an enhancement mode GaN transistor, including growing epitaxial layers over a substrate and etching the p-type GaN layer with dry etching. *Hikita-023*, [0074]-[0080].

b. [5a]: “nucleating and growing transition layers on a substrate;”

247. In my opinion, *Hikita-023* in view of *Sheppard* renders obvious nucleating and growing transition layers on a substrate. *Hikita-023* discloses

nucleating and growing a transition layer on a substrate, and *Sheppard* discloses providing multiple transition layers on the substrate.

248. For example, *Hikita-023* discloses growing an **AlN buffer layer 12** over a **substrate 11** by epitaxial growth, as shown below. *Hikita-023*, [0051], [0076]. *Hikita-023* discloses that the **substrate 11** is a sapphire material. *Hikita-023*, [0051], [0076].



Hikita-023, Fig. 1B (annotated).

249. The **AlN buffer layer 12** is a transition layer because it is an intermediate layer between the **substrate 11** and the **undoped GaN layer 13**. This is confirmed by the '508 patent which describes the **transition layers** located directly above the **substrate** and underneath the **undoped GaN layer**. Ex. 1001, 3:26-29.

250. *Hikita-023* discloses applying known a MOCVD method to grow the transition layer (AlN buffer layer 102) on the sapphire substrate. *Hikita-023*, [0076]. A POSITA would have understood that growing a transition layer on a sapphire substrate using the MOCVD method includes an initial phase of nucleation and then growth of the transition layer. *Sheppard*, 6:58-62 (providing an AlN buffer layer to “provide an appropriate crystal structure transition”), 7:29-32 (“buffer nucleation and/or transition layers may be deposited by MOCVD”). The ’508 patent does not provide any description of the nucleating process, confirming that nucleating a transition layer over a silicon substrate was a well-known technique to a POSITA. *See generally*, Ex. 1001.

251. To the extent *Hikita-023* does not explicitly disclose providing multiple transition layers on a substrate, *Sheppard* renders this obvious. *Sheppard* discloses a GaN transistor that includes multiple transition layers on a sapphire substrate. *Sheppard*, 7:19-24. *Sheppard* discloses providing an “AlN buffer layer” and additional “strain balancing transition layer(s)” to “provide an appropriate crystal structure transition” between the substrate and the remainder of the device. *Sheppard*, 6:58-7:7.

252. In my opinion, a POSITA would have been motivated and found it obvious to include multiple transition layers in *Hikita-023*’s device, as taught by *Sheppard*. Like the *Hikita-347* combination, both *Hikita-023* and *Sheppard* are

concerned with providing a high-quality GaN transistor and both disclose a sapphire substrate. *Hikita-023*, [0051], [0076]; *Sheppard*, 7:19-23; *Hikita-347*, [0033], [0056]. A POSITA would have been motivated to include multiple transition layers in *Hikita-347*'s device and would have expected success for the same reasons I explained in Ground 2.

(a) A POSITA would have been motivated to provide multiple transition layers in *Hikita-023*'s device, as disclosed by *Sheppard*

253. *Hikita-023* and *Sheppard* are both directed to a GaN transistor and forming such a device using a multilayered epitaxial structure. *Hikita-023*, [0051], [0076]; *Sheppard*, 6:45-8:54. *Sheppard* explains that providing additional transition layers on the substrate provides a benefit of strain balancing. *Sheppard*, 6:58-7:7. A POSITA would have been motivated to include multiple transition layers in *Hikita-023*'s device to achieve an improved strain balancing effect, as taught by *Sheppard*. A POSITA would have also been motivated to include multiple transition layers in *Hikita-023*'s device to improve the crystalline quality of the various layers above the transition layers of *Hikita-023*'s device.

254. Both *Hikita-023* and *Sheppard* describe using sapphire as a substrate material for their GaN-based devices. *Hikita-023*, [0051]; *Sheppard*, 7:19-23. A POSITA would have understood that there is a large lattice mismatch between GaN and sapphire, causing large densities of misfit dislocations to form as line

defects penetrating through the epitaxial layers and as a result lowering the conductivity of the GaN transistor's channel. *See, e.g., Piner*, [0003]-[0004] (describing dislocation defects when III-nitride materials are formed on sapphire substrates). A POSITA would have recognized that having a single AlN transition layer in *Hikita-023*'s device does not effectively reduce the line defects resulting from the large lattice mismatch between GaN and sapphire. A POSITA would have been motivated to incorporate additional transition layers taught by *Sheppard* to improve the quality of the GaN transistor by reducing the line defects formed during the growth of GaN epitaxy over sapphire. *See, e.g., Piner*, [0076]-[0079], [0092] (using compositionally-graded transition layers with varying composition of Aluminum (Al) over a sapphire substrate to reduce dislocation densities that negatively affect device performance).

(b) A POSITA would have reasonably expected to succeed in providing multiple transition layers in *Hikita-023*'s device

255. *Hikita-023*'s device already includes a transition layer (AlN buffer layer 12), and *Hikita-023* describes a method of growing the transition layer over a sapphire substrate. *Hikita-023*, [0051], [0076]. Both *Hikita-023* and *Sheppard* are concerned with providing a high quality GaN transistor and both disclose using a sapphire material for the substrate. *Hikita-023*, [0051], [0076]; *Sheppard*, 7:19-24. The '508 patent does not explain how to nucleate and grow transition layers over a

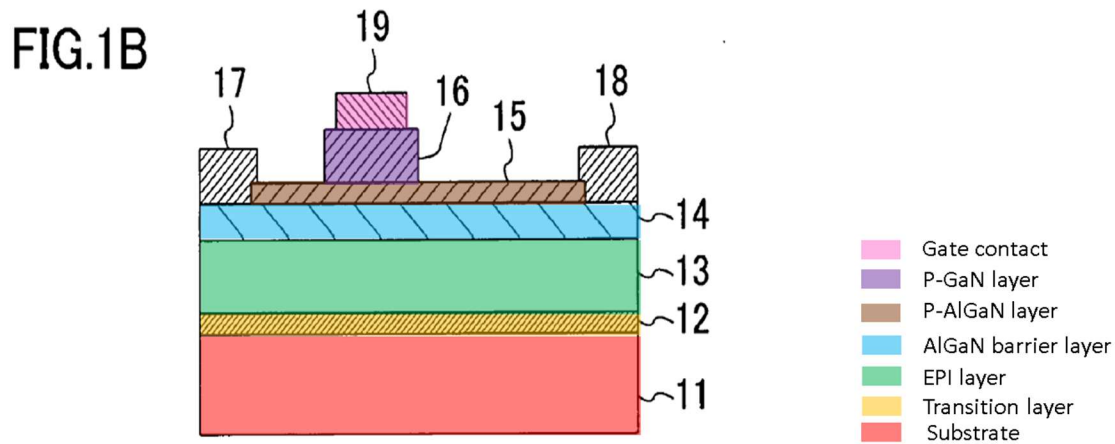
substrate, because nucleating and growing multiple transition layers to form a GaN device was routine, conventional, and well understood in the art. *See generally* Ex. 1001. The '508 patent further admits that it was “conventional” to provide transition layers over a sapphire substrate. Ex. 1001, 1:53-64 (background). Providing multiple transition layers in *Hikita-023*’s device would have required only conventional techniques in their ordinary and expected manner, because using multiple transition layers to form a GaN transistor over a sapphire substrate was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using multiple transition layers to form a GaN transistor over a sapphire substrate.

c. [5b]: “growing an InAlGaN EPI layer over the transistor layers;”

256. In my opinion, *Hikita-023* in view of *Sheppard* renders obvious growing an InAlGaN EPI layer over the transition layers.⁵

⁵ The “transistor layers” in [5b] lacks an antecedent basis. It appears that “the transistor layers” refers to the “transition layers” in [5a] because the '508 patent does not describe any “transistor layers.” The '508 patent describes an III Nitride EPI layer 13 over the transition layers 12. Ex. 1001, 3:26-29, Fig. 2. I consider the “transistor layers” as the “transition layers” in [5a] in my opinions here.

257. For example, *Hikita-023* discloses growing an **undoped GaN layer 13** over the **buffer layer 12** (transition layer), as shown below.



Hikita-023, Fig. 1B (annotated).

258. *Hikita-023* does not explicitly disclose that the EPI layer (layer 13) is comprised of InAlGaIn. However, *Sheppard* does. For example, *Sheppard* discloses that the channel layer 20 (EPI layer) is an AlInGaIn material. *Sheppard*, 7:40-41. A POSITA would have understood that *Sheppard*'s channel layer 20 corresponds to the "EPI layer" because, like the EPI layer in the '508 patent, the channel layer 20 is provided under the barrier layer 22, and together they form a two-dimensional electron gas. *Sheppard*, 7:47-8:3, Fig. 3.

259. It would have been obvious to use an InAlGaIn material for the EPI layer of *Hikita-023*'s device, as disclosed by *Sheppard*. A POSITA would have been motivated to use InAlGaIn for the EPI layer to increase the breakdown voltage of *Hikita-023*'s transistor. It was known that some alloys of the InAlGaIn

material have higher critical field in comparing with that of GaN, resulting in a larger breakdown voltage of the transistor. A POSITA would have also been motivated to include an InAlGaN for the EPI layer to construct a quantum well in *Hikita-023*'s transistor, such that the gate length of the transistor can be shortened for use in high frequency applications. *Ambacher*, 1 (constructing a quantum well structure using a compound with Indium Gallium Nitride). A POSITA would have further understood that using InAlGaN is merely an obvious design choice to form an EPI layer of *Hikita-023*'s transistor because the Group III nitride family includes combinations of Al (Aluminum), In (Indium), Ga (Gallium) with Nitride, and a combination of Al, In, and Ga with Nitride is an obvious combination from elements of the Group III nitride family. *See Yoshida*, [0012]; *Sheu*, 6 (providing AlInGaN in each layer of a GaN-based transistor). The '508 patent does not identify a specific composition of the InAlGaN compound or state any differentiating characteristics or purpose for using the InAlGaN compound in the EPI layer. The only instance the InAlGaN material appears in the '508 patent is in a generic statement that the EPI layer 13 is made of a "III Nitride material" and "can be composed of $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $x+y \leq 1$." Ex. 1001, 3:23-25.

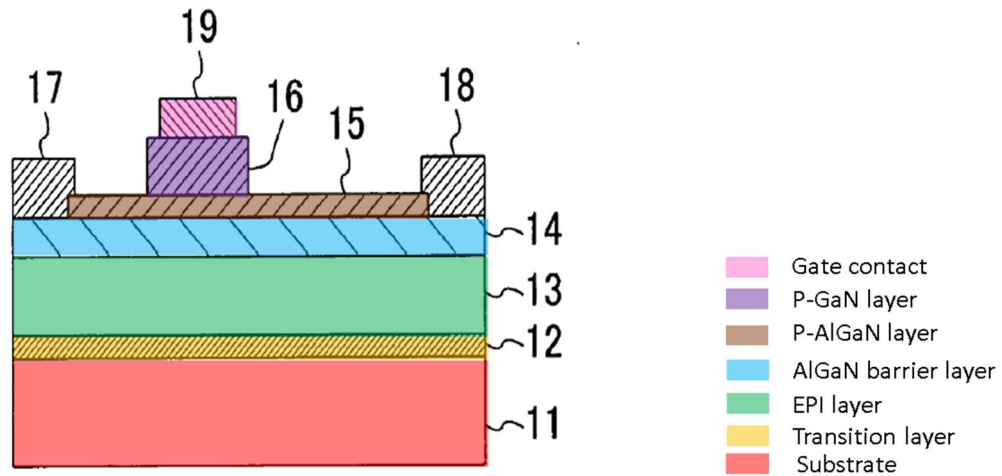
260. A POSITA would have reasonably expected to succeed in using InAlGaN for the EPI layer of *Hikita-023*'s transistor because using InAlGaN to form an EPI layer routine, conventional, and well understood in the art. *See*

Yoshida, [0012]; *Sheu*, 6 (providing AlInGaN in each layer of a GaN-based transistor). The '508 patent does not explain how to grow InAlGaN in an EPI layer, because growing InAlGaN in an EPI layer was routine, conventional, and well understood in the art. *See generally* Ex. 1001. Using *Sheppard's* InAlGaN for an EPI layer in *Hikita-023's* device would have required only conventional techniques in their ordinary and expected manner. Thus, a POSITA would have reasonably expected to succeed in using *Sheppard's* InAlGaN for an EPI layer in *Hikita-023's* device.

d. [5c]: “growing an AlGaN barrier layer over the InAlGaN EPI layer;”

261. In my opinion, *Hikita-023* in view of *Sheppard* renders obvious this limitation. *Hikita-023* discloses growing an **undoped AlGaN layer 14** (barrier layer) over the EPI layer, as shown below, and as discussed above in [5b], *Sheppard* renders obvious that the EPI layer is comprised of InAlGaN. *Hikita-023*, [0051], [0076].

FIG.1B



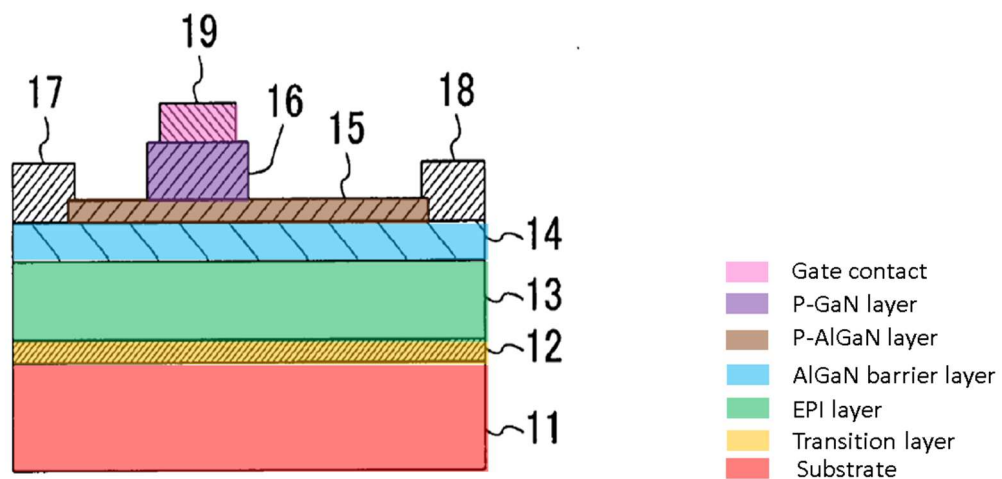
Hikita-023, Fig. 1B (annotated).

- e. [5d]: “growing an AlGaN layer with acceptor type dopants over the AlGaN barrier layer;”

262. In my opinion, *Hikita-023* discloses growing an AlGaN layer with acceptor type dopants over the AlGaN barrier layer.

263. *Hikita-023* discloses growing a first doped layer, **p-type AlGaN layer 15**, over the AlGaN barrier layer, as shown below. *Hikita-023*, [0051], [0076].

FIG.1B

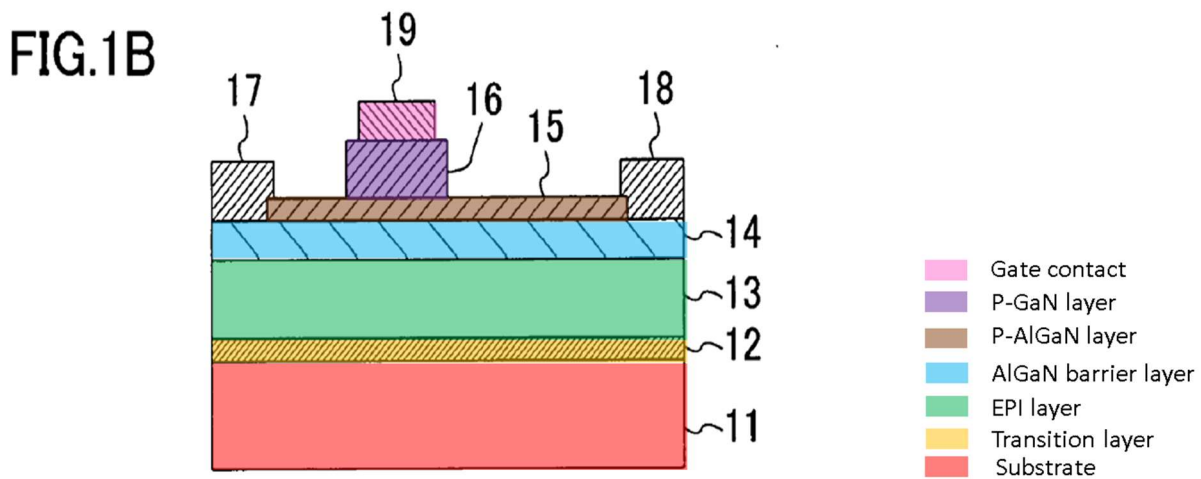


Hikita-023, Fig. 1B (annotated).

264. A POSITA would have understood that the p-type dopants in the **p-type AlGa_N layer 15** are acceptor type dopants. The '508 patent confirms that p-type dopants are acceptor type dopants. Ex. 1001, 6:24-28 (explaining that p-type dopants are “acceptor-rich”).

f. [5e]: “growing a GaN layer with acceptor type dopants over the doped AlGa_N layer;”

265. In my opinion, *Hikita-023* discloses growing a GaN layer with acceptor type dopants over the doped AlGa_N layer. For example, *Hikita-023* discloses growing a second doped layer, **p-type Ga_N layer 16**, over the **first p-type AlGa_N layer 15**, as shown below. *Hikita-023*, [0051], [0076].



Hikita-023, Fig. 1B (annotated).

g. [5f]:

“[5f1] depositing a gate contact layer on the doped GaN layer

[5f2] applying a gate photo resistant pattern;

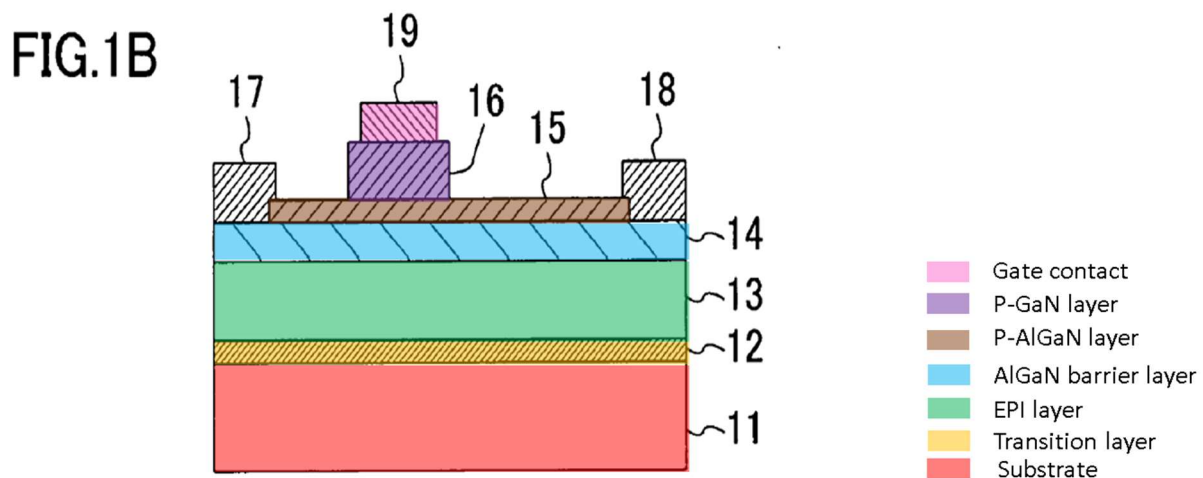
[5f3] etching away the gate contact layer outside the gate region;

[5f4] etching away the doped GaN layer, except for portions of the doped GaN layer and the doped AlGaN layer beneath gate contact;

[5f5] removing the gate photo resistant pattern;”

266. In my opinion, *Hikita-023* in view of *Beach* renders obvious element [5f]. *Hikita-023* discloses etching away the doped GaN layer, except for portions of the doped GaN layer beneath gate contact ([5f4]), and *Beach* renders obvious all steps in element [5f].

267. *Hikita-023* discloses forming a **gate electrode 19** (gate contact) over the **p-type GaN layer 16**, as shown below. *Hikita-023*, [0056], [0080].



Hikita-023, Fig. 1B (annotated).

268. *Hikita-023* further discloses that, to form the p-type GaN layer 16, the portion of the p-type GaN layer “other than a gate formation region” is etched away. *Hikita-023*, [0077]. Although Figure 1B shows that the p-type GaN layer 16 extends beyond the gate contact 19, *Hikita-023* discloses in the description that the p-type GaN layer extending beyond the gate electrode is to be etched away. *Hikita-023*, [0077].

269. *Hikita-023* does not explicitly disclose using a single mask (gate photo resistant pattern) to etch the p-type GaN layer and gate contact layer, but *Beach* renders this obvious.

270. As I explained in Ground 1, *Beach* discloses using a single mask to form a self-aligned gate and doped GaN layer with the steps of element [5f]. *Supra*, §XI.A.1.f. Like the *Yoshida* combination, *Hikita-023* and *Beach* disclose a GaN device where the doped GaN layer is etched away other than the gate region. *Hikita-023*, [0077]; *Beach*, [0043]-[0048]; *Yoshida*, [0022]. In my opinion, a POSITA would have been motivated to use *Beach*’s single mask process to form the gate contact and doped GaN layer in *Hikita-023*’s device and would have expected success for the same reasons as in Ground 1. *Supra*, §XI.A.1.f.

- (a) **A POSITA would have been motivated to apply *Beach*’s masking process to form *Hikita-023*’s device**

271. *Hikita-023* and *Beach* are both directed to a GaN-based semiconductor device and methods for forming such a device. *Hikita-023*, [0051]-[0057]; *Beach*, [0002], [0017]-[0018]. Like *Hikita-023*, *Beach* discloses a GaN device with multiple layers of III-nitride material, such as a GaN layer 10, an AlGaN layer 12, and a highly doped GaN layer 16. *Beach*, [0040]-[0043]. Like *Hikita-023*'s device, *Beach*'s device has a gate contact 15 and ohmic contact 17. *Beach*, [0048]-[0049]. A POSITA would have been motivated to use the single mask process to form the gate contact and doped GaN layer, as taught by *Beach*, to improve *Hikita-023*'s device and process in multiple ways.

272. First, *Beach*'s single mask process effectively achieves *Hikita-023*'s objective that the doped GaN layer is to be etched away except the gate region. *Hikita-023*, [0077]. A POSITA would have recognized that *Beach*'s single mask process automatically achieves self-alignment between the gate contact and the doped GaN layer and improves the gate's alignment in *Hikita-023*'s device. See *Beach*, Fig. 1E; *Hikita-023*, Fig. 1B. A POSITA would have appreciated that self-aligned gate and doped GaN layer is a desired feature in GaN devices and would have been motivated to implement *Beach*'s single mask process to achieve a self-aligned gate arrangement in *Hikita-023*'s device. See *Beach-547*, [0043]-[0048] (describing self-aligned gates as advantageous); *Kouznetsov*, 3:42-61 (explaining that self-alignment decreases die size and cost).

273. Second, *Beach*'s single mask process to etch the gate contact and doped GaN layer simplifies *Hikita-023*'s process to form the doped GaN layer. Compared to *Hikita-023*'s process which employs two separate masks and two separate steps to etch the gate contact and doped GaN layer, *Beach* uses a single mask to etch the gate and doped GaN layer which removes the additional step of applying a second mask for the gate contact. *Beach*, [0047]. A POSITA would have understood that applying an additional mask involves substantial undertaking during manufacturing and the removal of one additional mask application leads to a simplified manufacturing process and saving of manufacturing cost. A POSITA would have been motivated to use *Beach*'s single mask process to produce *Hikita-023*'s device because doing so would simplify the manufacturing process and save manufacturing cost. *See Kouznetsov*, 3:55-61 (describing that uses the same photoresist mask to form the layers decreases process cost and complexity).

(b) A POSITA would have reasonably expected to succeed in applying *Beach*'s masking process to form *Hikita-023*'s device

274. Applying a single mask to form the gate contact and doped GaN layer was a well-known and conventional technique when the '508 patent was filed. The '508 patent states that the etching of the gate contact and p-GaN layer using the same mask is performed by "any known technique," because etching multiple layers of different materials using the same mask was routine, conventional, and

well understood in the art. Ex. 1001, 3:45-50. Indeed, using the same mask to etch different layers of materials in semiconductor devices was known and implemented decades before the '508 patent. *Green*, 8:10-19 (etching the silicide layer and metal layer using a single mask), Figs. 6-7; *Spikes*, 4:39-5:3 (etching the metal layer, the polysilicon layer, and dielectric layer using a single mask), Figs. 1B-1C; *Shim*, 3:8-14 (etching the metal layer and silicon layer using a single mask), Figs. 2C-2D.

275. Both *Hikita-023*'s and *Beach*'s devices use the same GaN material for the layer underneath the gate contact. To the extent EPC argues that the dopants applied to *Beach*'s GaN layer (n-type dopants) are not the same type of dopants as *Hikita-023* (p-type dopants), a POSITA would have understood that the impurities caused by the dopants are so dilute that they do not change the etching characters of the GaN material, and as a result, a POSITA would have reasonably expected to succeed in applying *Beach*'s masking technique to etch the p-type GaN layer in *Hikita-023*'s device. *Hikita-023*'s device could be formed using the single mask technique described by *Beach*, according to the known, routine process of masking and etching. Using *Beach*'s single mask process to etch the gate contact and doped GaN layer in *Hikita-023*'s device would have required only conventional techniques in their ordinary and expected manner, because using the same mask to etch different layers of materials was routine, conventional, and well understood in

the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach*'s single mask process to form *Hikita-023*'s GaN device.

h. [5g]:

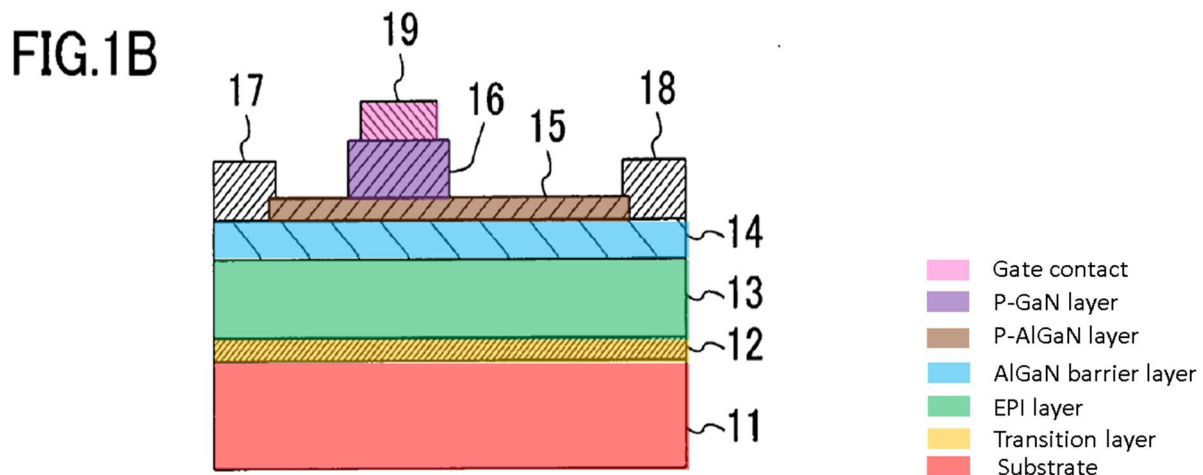
“[5g1] applying another photo resistant pattern;

[5g2] etching the doped AlGaN layer such that the doped AlGaN extends outside the gate region towards the drain;

[5g3] removing the photo resistant pattern;

276. In my opinion, *Hikita-023* discloses element [5g].

277. *Hikita-023* discloses etching the doped AlGaN layer 15 such that the doped AlGaN extends outside the gate region towards the drain 18 ([5g2]), as shown below. *Hikita-023*, [0078].



Hikita-023, Fig. 1B (annotated).

278. *Hikita-023* further discloses that the etching of the doped AlGaN layer is performed by a “lithography method.” *Hikita-023*, [0078]. A POSITA would

have understood that lithography is a fundamental process in semiconductor manufacturing and involves the following steps: (1) applying a photo resistant pattern ([5g1]), (2) performing etching according to the photo resistant pattern ([5g2]), and (3) removing the photo resistant pattern ([5g3]). *See Campbell*, 4 (describing a lithography process involving applying a photo resistant pattern, etching the exposed material, and removing the photo resistant pattern); *Ghandhi*, 3-13 (describing lithographic processes involving applying a photoresist, etching the underlying material, and removing the photoresist). A POSITA would have understood that a separate photo resistant pattern is applied to etch the doped AlGa_N layer 15 after etching the p-type Ga_N layer 16 and gate contact 19, because the doped AlGa_N layer 15 has a different length from that of the p-type Ga_N layer 16 and gate contact 19, requiring a separate mask for the etching of the doped AlGa_N layer 15. *Hikita-023*, Figs. 1A, 1B. Thus, *Hikita-023* disclose the steps in [5g].

i. [5h]:

“[5h1] depositing a dielectric layer;
[5h2] applying a contact photo resistant pattern;
[5h3] etching the dielectric layer to open the drain
and source contact area;
[5h4] removing the contact photo resistant pattern;”

279. In my opinion, *Hikita-023* in view of *Sheppard* renders obvious element [5h]. *Hikita-023* discloses depositing a dielectric layer, and *Sheppard* renders obvious all steps of [5h].

280. *Hikita-023* discloses forming an “insulating film” over the gate electrode, having “a relative dielectric constant of 4 or lower.” *Hikita-023*, [0030]; *see also Hikita-023*, [0089]. Thus, *Hikita-023* discloses depositing a dielectric layer ([5h1]).

281. *Hikita-023* does not explicitly disclose using a mask (contact photo resistant pattern) to open the drain and source contact area in the dielectric layer, and *Sheppard* renders this obvious.

282. *Sheppard* discloses using a mask pattern to form openings in a cap layer 24 for the Ohmic contacts (source/drain contacts). *Sheppard* describes providing a **mask 40** and etching the cap layer to open windows for ohmic contacts (source/drain contacts) according to the mask, as shown below. *Sheppard*, 8:55-67. *Sheppard* also discloses that cap layer includes SiN, a dielectric material. *Sheppard*, 3:21-23. *Sheppard* explains that the etching process results in exposure

of areas of the underlying barrier layer 22. *Sheppard*, 8:61-63. *Sheppard* discloses that the mask 40 is removed after the Ohmic contacts are formed. *Sheppard*, Fig. 1D. Thus, *Sheppard* discloses steps [5h2], [5h3], [5h4].

283. In my opinion, it would have been obvious to apply *Sheppard*'s masking process to etch the dielectric layer to open the drain and source contact area in *Hikita-023*'s device. Like the *Hikita-347* combination, *Hikita-023* and *Sheppard* disclose a GaN device with source and drain contacts. *Hikita-023*, [0078]-[0079]; *Sheppard*, 3:16-27, 9:42-46. A POSITA would have been motivated to use *Sheppard*'s masking process to open the drain and source contact area in *Hikita-023*'s device and would have expected success for the same reasons as in Ground 2, [4f]. *Supra*, §XI.B.1.g.

(a) A POSITA would have been motivated to apply *Sheppard*'s masking process to open drain and source contact area in *Hikita-023*'s device

284. *Hikita-023* and *Sheppard* are both directed to a GaN transistor with source and drain contacts and methods of forming such a device. *Hikita-023*, [0051], [0056], [0074]; *Sheppard*, 6:45-8:54. Like *Hikita-023*, *Sheppard* discloses a GaN device with source and drain contacts. *Sheppard*, 3:16-27, 9:42-46. A POSITA would have been motivated to use the masking process to open the drain and source contact area in a dielectric layer, as taught by *Sheppard*, to improve *Hikita-023*'s device and process in multiple ways.

285. First, *Sheppard's* masking process allows opening the drain and source contact area in the dielectric layer such that the drain and source contacts can be formed. A POSITA would have appreciated that *Sheppard's* masking process would allow etching of the dielectric layer to open the drain and source contact area. A POSITA would have been motivated to adopt *Sheppard's* masking process to effectively open the drain and source contact area in *Hikita-023's* dielectric layer, such that the drain and source contacts are formed for *Hikita-023's* transistor to perform its intended functions. A POSITA would have also understood that depositing a dielectric layer over the gate electrode and surface of the structure, as taught by *Hikita-023*, provides protection to the gate electrode and underlying layers during a subsequent anneal of the Ohmic drain and source contacts and would have been motivated to apply the dielectric layer prior to forming the Ohmic drain and source contacts.

286. Second, *Sheppard's* masking process enables the drain and source contact area to be formed at the desired locations. A POSITA would have understood that *Sheppard's* masking process allows control of the etching such that only the dielectric layer at desired areas is etched and leaving the other part of the dielectric layer intact. A POSITA would have understood that such precision and control is essential for manufacturing of any semiconductor device to ensure the device operates as intended. A POSITA would have been motivated to adopt

Sheppard's masking process to open the drain and source contact area at desired locations and leave the remaining part of the dielectric layer intact, such that *Hikita-023's* transistor operates as intended.

(b) A POSITA would have reasonably expected to succeed in applying *Sheppard's* masking process to open drain and source contact area in *Hikita-023's* device

287. Using a mask to form openings in a dielectric layer of a semiconductor device was a well-known and conventional technique when the '508 patent was filed. *See Yoshida*, [0022]. The '508 patent does not explain how to apply a mask to etch the dielectric layer, because using a mask to pattern and etch a dielectric layer was routine, conventional, and well understood in the art. *See generally* Ex. 1001. *Hikita-023's* drain and source contact area could be opened using the masking process described by *Sheppard*, according to the known, routine process of masking and etching. Using *Sheppard's* masking process to etch the dielectric layer in *Hikita-023's* device would have required only conventional techniques in their ordinary and expected manner, because using a mask to etch a dielectric material was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Sheppard's* masking process to open drain and source contact area in *Hikita-023's* device.

j. [5i]:

**“[5i1] depositing an Ohmic contact metal;
[5i2] applying a fourth photo resistant pattern;
[5i3] etching the Ohmic contact metal
[5i4] removing the fourth photo resistant pattern; and
[5i5] performing rapid thermal annealing to form
Ohmic drain and source contacts.”**

288. In my opinion, *Hikita-023* in view of *Beach* renders obvious element [5i].

289. *Hikita-023* discloses depositing a Ti layer and an Al layer (Ohmic contact metal) to form a source electrode 17 and a drain electrode 18 (Ohmic source and drain contacts). *Hikita-023*, [0079]; Thus, *Hikita-023* discloses step [1g1], i.e., depositing an Ohmic contact metal.

290. *Hikita-023* further discloses performing “thermal treatment (annealing)... at 650° C” to form the Ohmic source and drain contacts. *Hikita-023*, [0079]. Thus, *Hikita-023* disclose performing thermal annealing to form Ohmic drain and source contacts. To the extent EPC argues that *Hikita-023* does not explicitly disclose rapid thermal annealing, a POSITA would have found it obvious to perform rapid thermal annealing to form Ohmic source and drain contacts in *Hikita-023*’s devices (step [5i5]). A POSITA would have found performing rapid thermal annealing to activate ohmic contacts was routine and conventional long before the ’508 patent was filed, and would have had a reasonable expectation of

success in doing so. Such technique was a conventional and commonly adopted technique in GaN semiconductor manufacturing to form a low-resistance ohmic contact in an efficient manner. *See Johnson*, [0085]; *Hu*, 1; *Chen*, [0087]; *Shimizu*, 1; *Ye*, [0061]. A POSITA would have been motivated to perform rapid thermal annealing instead of conventional furnace annealing to activate ohmic contacts because it was well known that rapid thermal annealing reduces thermal budget, lowers manufacturing cost, and increases production throughput of the semiconductor devices. *See Campbell*, 6; *Ye*, [0061]; *Hu*, 1. A POSITA would have been motivated to perform rapid thermal annealing to activate ohmic contacts because it was known to improve the structural and optoelectronic properties of GaN materials, as well as providing a smoother surface of the contact which improves circuit yield. *Zhu*, 5; *Campbell*, 9. Therefore, it would have been obvious to perform rapid thermal annealing to activate the Ohmic contacts in *Hikita-023*'s devices.

291. *Hikita-023* does not explicitly disclose a masking and etching process for forming the Ohmic source and drain contacts, but *Beach* discloses using a masking and etching process ([5i2], [5i3], [5i4]) to form Ohmic contacts as explained in Ground 1. *Supra*, §XI.A.1.h; *Beach*, [0045]-[0047].

292. In my opinion, it would have been obvious to use *Beach*'s masking and etching process to form *Hikita-023*'s Ohmic source and drain contacts. Like

the *Yoshida* combination, *Hikita-023* and *Beach* disclose forming source and drain contacts using ohmic metal. *Hikita-023*, [0079]; *Beach*, [0048]-[0049]; *Yoshida*, [0010], [0022]. A POSITA would have been motivated to use *Beach*'s source and drain masking process to form the source and drain contacts in *Hikita-023*'s device and would have expected success for the same reasons as in Ground 1, [1g]. *Supra*, §XI.A.1.h.

(a) A POSITA would have been motivated to apply *Beach*'s masking process to form *Hikita-023*'s Ohmic source and drain contacts

293. *Hikita-023* and *Beach* are both directed to a GaN-based semiconductor device and methods for forming such a device. *Hikita-023*, [0051]-[0057]; *Beach*, [0002], [0017]-[0018]. Like *Hikita-023*, *Beach* discloses a GaN device with multiple layers of III-nitride material, such as a GaN layer 10, an AlGaN layer 12, and a highly doped GaN layer 16. *Beach*, [0040]-[0043]. Similar to *Hikita-023*'s device, *Beach*'s device has a gate contact 15 and ohmic contact 17. *Beach*, [0048]-[0049]. A POSITA would have been motivated to use the masking process to form the Ohmic source and drain contacts, as taught by *Beach*, to improve *Hikita-023*'s device and process in multiple ways.

294. First, *Beach*'s masking process is simpler than the lift-off process, to form the Ohmic source and drain contacts. A POSITA would have understood that *Beach*'s masking process avoids manufacturing of the vertical profile of

photoresist shape used in the lift-off process, thereby saving the manufacturing cost to produce *Hikita-023*'s transistor. A POSITA would have been motivated to use *Beach*'s masking process to produce *Hikita-023*'s Ohmic source and drain contacts because doing so would simplify the manufacturing process and save manufacturing cost.

295. Second, *Beach*'s masking process allows a source and gate connected field plate to be easily formed, which reduces electrical field at the gate corner and results in higher breakdown voltage at *Hikita-023*'s device. A POSITA would have appreciated that, applying *Beach*'s masking process, a field plate can be easily formed by using a mask pattern that extends over the gate contact, such that a portion of the Ohmic metal between the source Ohmic contact and gate contact is not etched away. In contrast, the lift-off process requires a separate masking step to allow the source ohmic contact metal to extend beyond the designated opening for source contact, and as a result, requires additional processing to provide a field plate design. Therefore, a POSITA would have been motivated to use *Beach*'s masking process to produce *Hikita-023*'s Ohmic source and drain contacts to provide a field plate in *Hikita-023*'s device in a simple manner.

- (b) A POSITA would have reasonably expected to succeed in applying *Beach*'s masking process to form *Hikita-023*'s Ohmic source and drain contacts**

296. Using a mask (metal photo resist pattern) to pattern and etch Ohmic contact metal to form source and drain contacts was a well-known and conventional technique when the '508 patent was filed. The '508 patent does not explain how to apply a mask to etch Ohmic contact metal, because using a mask to pattern and etch Ohmic contact metal was routine, conventional, and well understood in the art. *See generally* Ex. 1001. Both *Hikita-023*'s and *Beach*'s devices use a III Nitride material for the layer underneath the Ohmic source and drain contacts. *Hikita-023*'s Ohmic source and drain contacts could be formed using the masking process described by *Beach*, according to the known, routine process of masking and etching. Using *Beach*'s masking process to etch the Ohmic contact metal in *Hikita-023*'s device would have required only conventional techniques in their ordinary and expected manner, because using a mask to etch an Ohmic contact metal was routine, conventional, and well understood in the art. Thus, a POSITA would have reasonably expected to succeed in using *Beach*'s masking process to form *Hikita-023*'s Ohmic source and drain contacts.

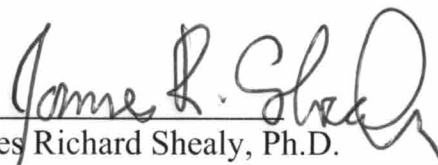
XII. CONCLUSION

297. For the reasons set forth above, in my opinion, a person of ordinary skill in the art would have found claims 1-5 of the '508 patent obvious.

298. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

299. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 8, 2023

By: 
James Richard Shealy, Ph.D.

APPENDIX A

James R. Shealy
School of Electrical and Computer Engineering
301 Phillips Hall
Cornell University
Ithaca NY, 14853

Biography

B.S. – 1978 (North Carolina State); M.S. – 1980 (Rensselaer Polytechnic); Ph.D. – 1983 (Cornell University)

In 1978, Shealy joined the technical staff of General Electric's Corporate Research & Development Center under an Edison Fellowship, where he developed GaAs epitaxial materials for high voltage electronics, and composite dielectrics for device fabrication by MOCVD. From this work, Shealy received two patents based on GaAs vertical field effect transistors. In 1980, Shealy transferred to General Electric's Advanced Electronics Laboratory where he developed the materials and a process for the fabrication of AlGaAs Light Emitting Diodes (LEDs). Shealy then developed an MOCVD reactor and process for the fabrication of AlGaAs quantum well laser diodes which resulted in the highest power, lowest threshold devices realized at that time. A novel and patented gas purification technique was developed and applied to the MOCVD process. Con-currently with the General Electric employment, Shealy worked at Cornell, and in 1984, Shealy's group at Cornell developed the first single quantum well red laser by MOCVD (emitting over 1 watt of power at 650 nm). In 1985, Shealy was designated a Principle Staff Scientist in General Electric in recognition of his research contributions.

After a decade with General Electric, Shealy joined the Cornell faculty in 1987. He continued the MOCVD related materials research which included the preparation of epitaxial structures for LEDs, laser diodes and high frequency transistors, all using GaAs or InP based materials. Also during this time, he developed a direct write process for laser stimulated epitaxial growth of quantum dots. In 1994, Shealy began research on GaN and related materials for both LEDs and high power transistors. This work resulted in a new nucleation technique for GaN materials on substrates including sapphire, SiC and Si. Shealy's group then produced the first operational GaN microwave transistor on a Si substrate. In 1997, Shealy became the Director of Cornell's Optoelectronics Technology Center, a joint research program with UCSB focusing on compound semiconductor optoelectronic devices. With a decade of funding (from the Office of Naval Research and DARPA), which includes a MURI program which Shealy was PI, several bench marks on GaN transistor performance were achieved, and several patents were issued on key aspects of the technology. In 1999, Shealy's group at Cornell realized the first operational GaN microwave transistors on Silicon substrates, a technology that is currently entering production in dozens of companies worldwide. In parallel, work progressed on realizing defect free GaN materials on micro-machined Si (also patented) which led to the development of operational pyramidal pn junction diodes in GaN. These structures are under investigation for realizing high efficiency surface emitting UV LEDs.

In 1998, Shealy was promoted to Full Professor at Cornell and he is a member of the graduate faculty of Electrical and Computer Engineering and Materials Science. He has received multiple awards for excellence in under-graduate teaching and has developed new courses in semiconductor materials and nanofabrication. While at Cornell, he has also consulted for dozens of US companies (including GE, GM, Motorola, Raytheon, NGC, Cree, RFMD, Honeywell, Welch Allyn) on the subject of compound semiconductor materials and devices. Shealy has published in excess of 250 Journal articles and is the inventor of over 15 patents, roughly half of which, involve GaN-based materials and devices. Shealy's work also includes the development of new dielectric passivation materials for GaN transistors which has resulted in unprecedented power performance for submicron-gated GaN transistors. This level of performance still represents the state-of-the-art in the present day. Shealy's publications have received over 10,000 citations by colleagues around the world working in semiconductor electronics.

In 2002, Shealy was co-founder and technical advisor to RF Nitro Communications which developed high performance GaN-based electronics. RF Nitro became the Charlotte division of RF Micro-Devices, a US company which merged into Qorvo in 2015. In 2009, Shealy co-founded two other companies, one involved in the manufacture of GaAs-based MMICs and the other taking advantage of new intellectual property in pursuit of high power GaN electronics. In 2015, Shealy co-founded Akoustis Technologies (publicly traded on the NASDAQ) which has developed next generation Bulk Acoustic Wave (BAW) filters using AlN single crystal materials for use in the 5G mobile communications cellular market. Akoustis is currently manufacturing these devices in their MEMs fabrication facility in upstate New York. In 2019, Shealy co-founded Odyssey Semiconductor which is developing vertical GaN field effect transistors for high voltage, power switching applications.

EXPERT WITNESS EXPERIENCE:

Since 2007, Shealy has engaged in expert witness related consulting in technical field of Gallium Nitride electronics and optoelectronics. A list of engagements follow. Note that the parties name appears in **boldface** for the side which Shealy represented.

- ITC in 2007-2009, Investigation No. 337-TA-640,"Certain LEDs, Laser Diodes and Products Containing Same," **Rothschild** vs. Sony, Toshiba, Sharp, etc. Albert Jacobs LLP.,US Patent 5,252,499.
- US District Court, Southern District of New York in 2008-2009, 05_CIV-5939 (WGY), "**Rothschild** vs. Cree, Inc.," Albert Jacobs LLP., US Patent 5,252,499.
- US District Court, Southern District of New York in 2010, 05_CIV-5939 (WGY), "**Rothschild** vs. Cree, Inc.," Troutman Sanders LLP., US Patent 5,252,499.

- US District Court, District of Massachusetts in 2010-2011, Civil Action No. 11-10133-WGY, "**Rothschild** vs. Cree, Inc.," Troutman Sanders LLP., US Patents 4,904,618 and 5,252,499.
- District Court Dusseldorf in 2011-2012, Civil Action No. 11-10133-WGY, "**Rothschild** vs. OSRAM.," Lang & Rahman Rechtsanwälte, US Patent 5,252,499.
- ITC in 2012, Investigation No. 337-TA-802,"Certain LEDs, Laser Diodes and Products Containing Same," **LG** vs. OSRAM, Finnegan, Henderson, Farabow, Garrett & Dunner LLP.,US Patent 7,928,465.
- US PTO in 2014-2015, Inter Partes Review of U.S. Patent 6,692,251, **Ultradent** vs. Kerr Corporation, Stoel Rivers LLP.
- US District Court, District of Delaware in 2013-present, Civil No. 1:12-cv-923-GMS, "**Schubert** vs. OSRAM," Troutman Sanders LLP., US Patent 6,294,475.
- US PTO in 2013-2014, Inter Partes Review of U.S. Patent 6,294,475, "**Schubert** vs. OSRAM", Troutman Sanders LLP.
- ITC in 2015, Investigation No. 337-TA-947,"Certain Light Emitting Diode Products and Components Thereof," **CREE** vs. Feit Electric Co. & Unity Opto Technology, Quinn Emanuel Urquhart & Sullivan, LLP., US Patent 8,766,298 B2.
- ITC in 2018, Investigation No. 337-TA-1081,"Certain Light Emitting Diode Products and Components Thereof," Phillips Lighting vs. **Lowes**, Hunton & Williams, LLP., US Patent 7,038,399, US Patent 7,256,554, US Patent 7,262,559.
- US PTO in 2018, Inter Partes Review of U.S. Patent 7,524,087, U.S. Patent 7,652,297, U.S. Patent 7,256,486, U.S. Patent 6,949,771, U.S. Patent 7,919,787 Document Security Systems, Inc, vs. **Nichia Corporation**, Shearman & Sterling LLP.
- US PTO in 2020, Inter Partes Review of U.S. Patent 6,879,040, Document Security Systems, Inc, vs. **Nichia Corporation**, Shearman & Sterling LLP.
- US District Court, Central District of California, Western Div. in 2017-2018, U.S. Patent No. 8,344,417, U.S. Patent No. 8,592,862, U.S. Patent No. 8,928,034, U.S. Patent No. 8,937,335, MACOM Technology vs. **Infineon**, Baker Botts, LLP.
- US District Court in 2019-present, U.S. Patent No. 6,465,961, **CAO Lighting** vs. various lighting companies , Barnes & Thornburg, LLP.
- US District Court, District of Delaware in 2023, U.S. Patent No. 6,465,961, **CAO Lighting** vs. General Electric, OSRAM and LEDVANCE LLC., Barnes & Thornburg, LLP.

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“Hydrodynamic simulation of surface traps in the AlGa_N/Ga_N HEMT”, Brannick, A; Zakhleniuk, NA; Ridley, BK; Eastman, LF; **Shealy, JR**; Schaff, WJ. *Workshop on Recent Advances on Low Dimensional Structures and Devices*, 07-09, April, 2008.

“Influence of Field Plate on the Transient Operation of the AlGa_N/Ga_N HEMT”, Brannick, A; Zakhleniuk, NA; Ridley, BK; **Shealy, JR**; Schaff, WJ; Eastman, LF. *IEEE Electron Device Letters*, **30** (5):436-438 2009

“Frequency dispersion in capacitance-voltage characteristics of AlGa_N/Ga_N heterostructures”, **Shealy, JR**; Brown, RJ, *Applied Physics Letters*, **92** (3): Art No. 032101 2008

“Methodology for small-signal model extraction of AlGa_NHEMT’s”, **Shealy, JR**; Wang, JL; Brown, R. *IEEE Transactions on Electron Devices* **55** (7):1603-1613- 2008

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“Influence of Si₃N₄ passivation on surface trapping in SiC metal-semiconductor field-effect transistors”, Cha, HY; Choi, YC; Thompson, RM; Kaper, V; **Shealy, JR**; Eastman, LF; Spencer, MG. *Journal of Electronic Materials* **33** (8):908-911 2004

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