US 20070007547A1

(19) United States

(12) Patent Application Publication

Beach

(10) Pub. No.: US 2007/0007547 A1

(43) Pub. Date: Jan. 11, 2007

(54) III-NITRIDE ENHANCEMENT MODE DEVICES

(76) Inventor: **Robert Beach**, Altadena, CA (US)

Correspondence Address:
OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403

(21) Appl. No.: **11/481,771**

(22) Filed: **Jul. 6, 2006**

Related U.S. Application Data

(60) Provisional application No. 60/696,985, filed on Jul. 6, 2005.

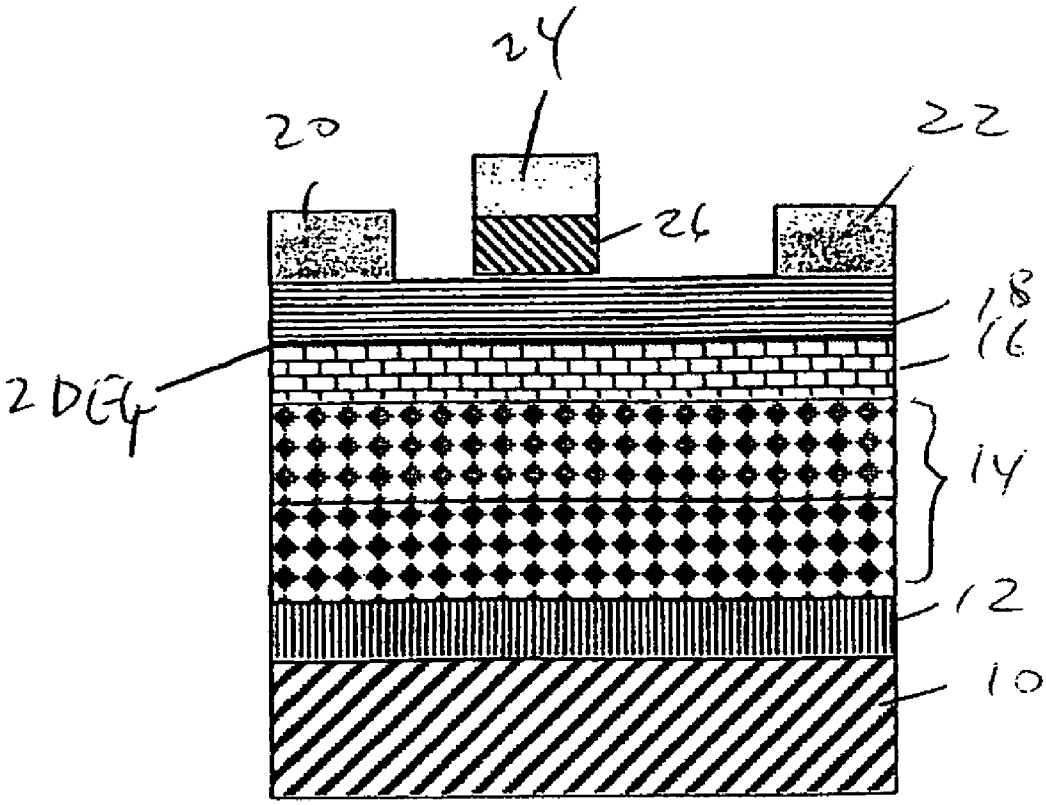
Publication Classification

(51) **Int. Cl.**
H01L 29/739 (2006.01)
H01L 31/00 (2006.01)

(52) **U.S. Cl.** **257/201**; 257/192; 257/194

(57) **ABSTRACT**

A III-nitride power semiconductor device that includes a gate barrier under the gate thereof, and a method for fabricating the device.



INNOSCIENCE EXHIBIT 1009

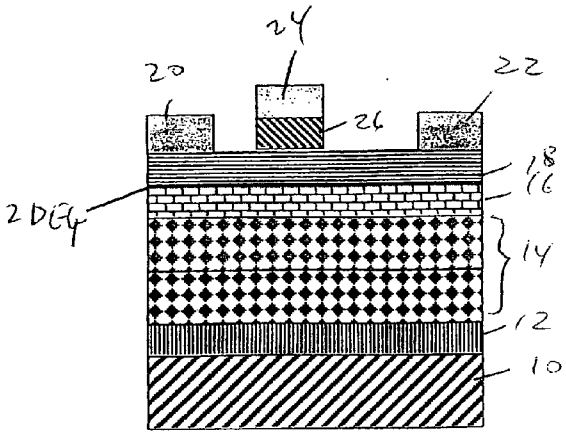


Fig. 1

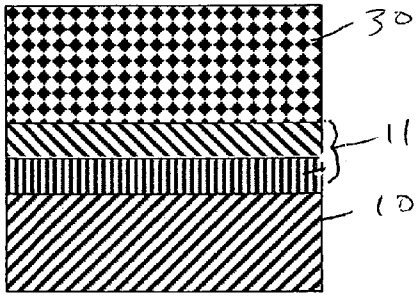


Fig. 2A

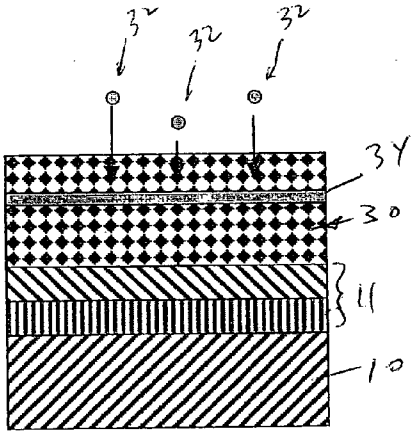


Fig. 2B

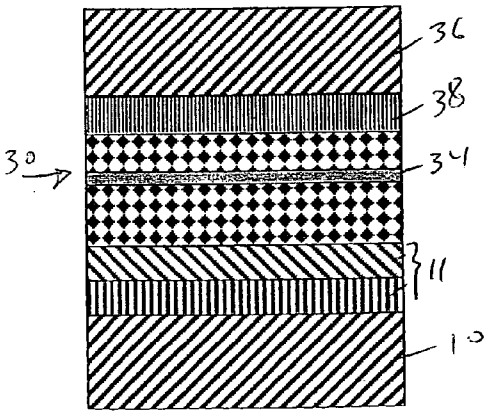


Fig. 2C

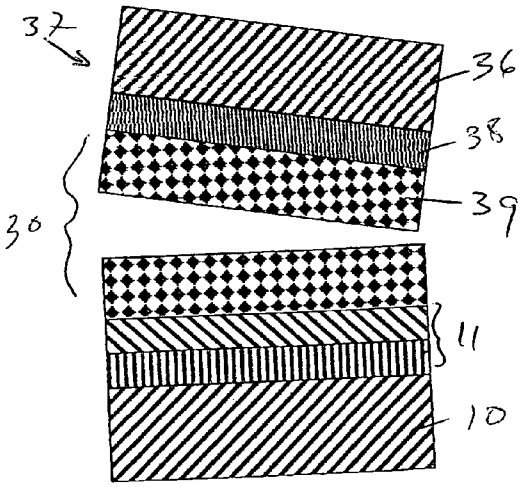


Fig. 2D

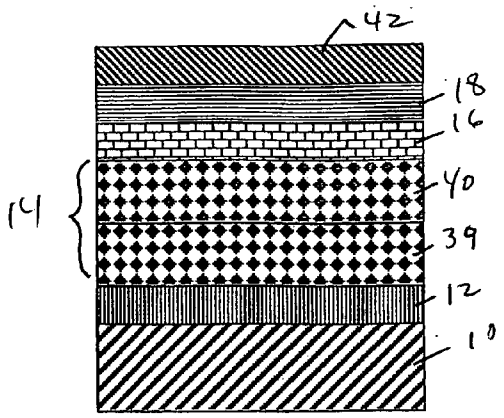


Fig. 2E

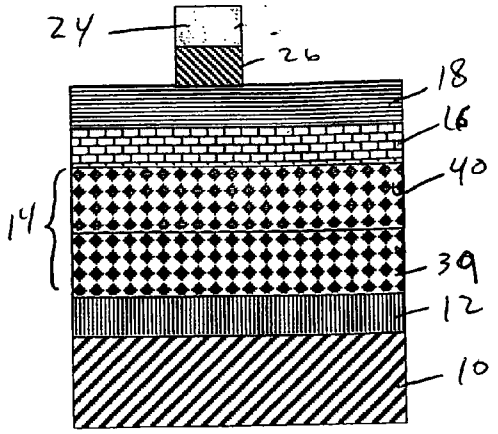


Fig. 2F

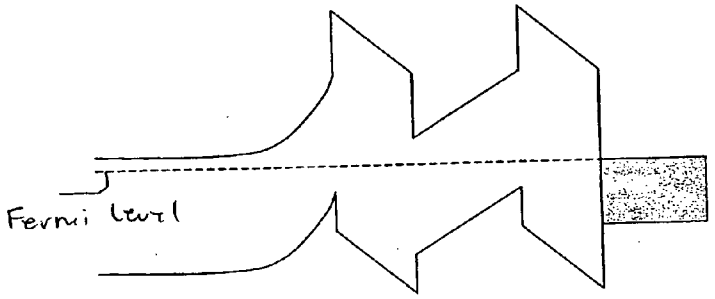


Fig. 3A

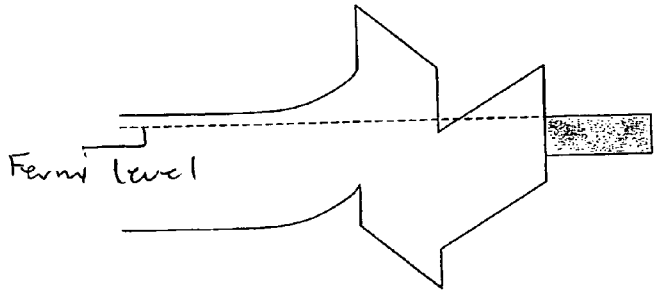


Fig. 3B

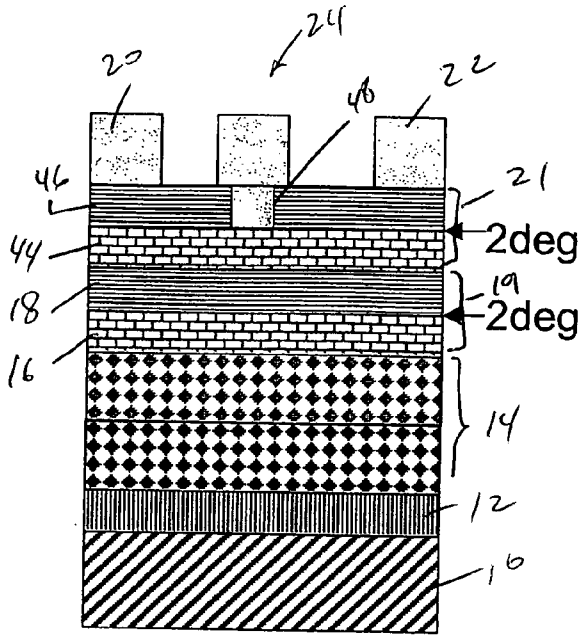
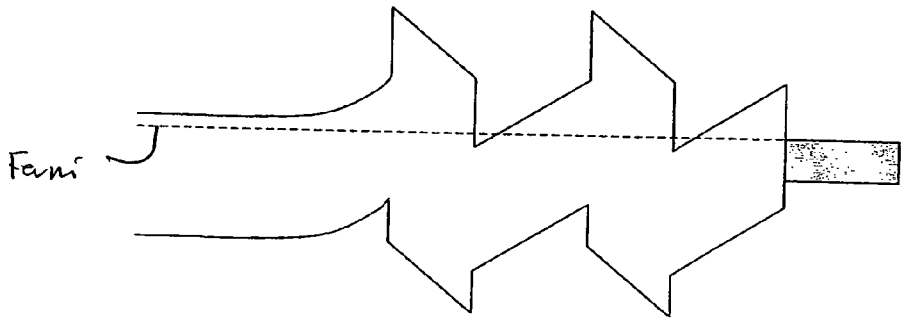
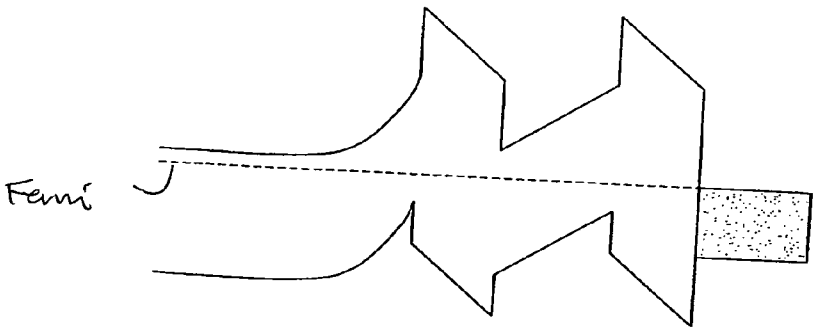


Fig. 4



Under Ohmic

Fig. 5A



Under Gate

Fig. 5B

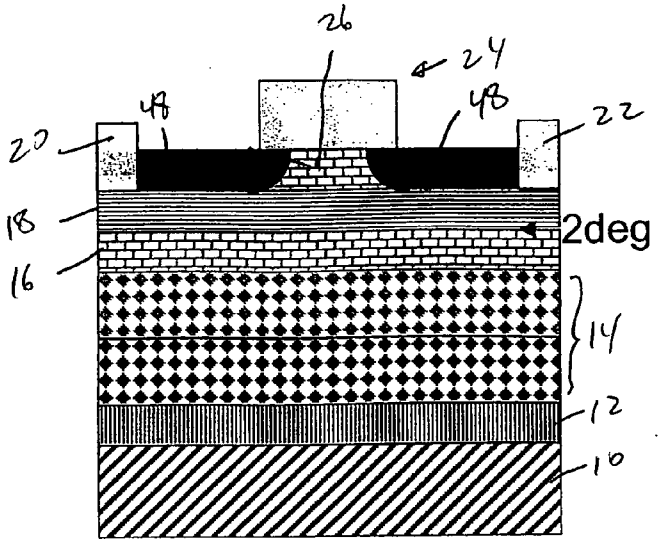
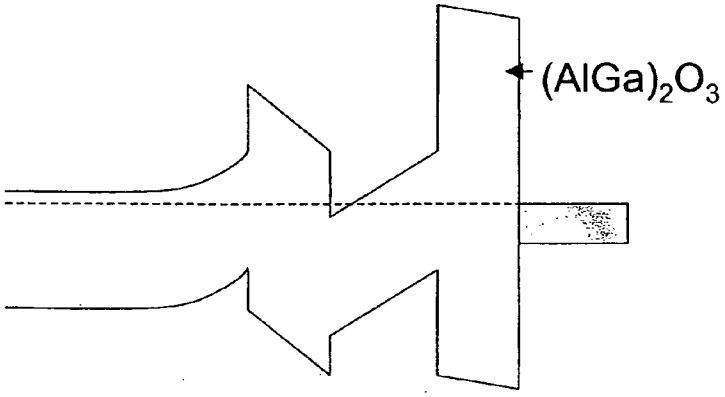
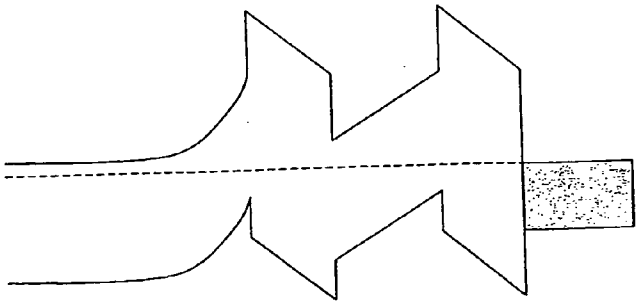


Fig. 6



Under Ohmic

Fig. 7A



Under Gate

Fig. 7B

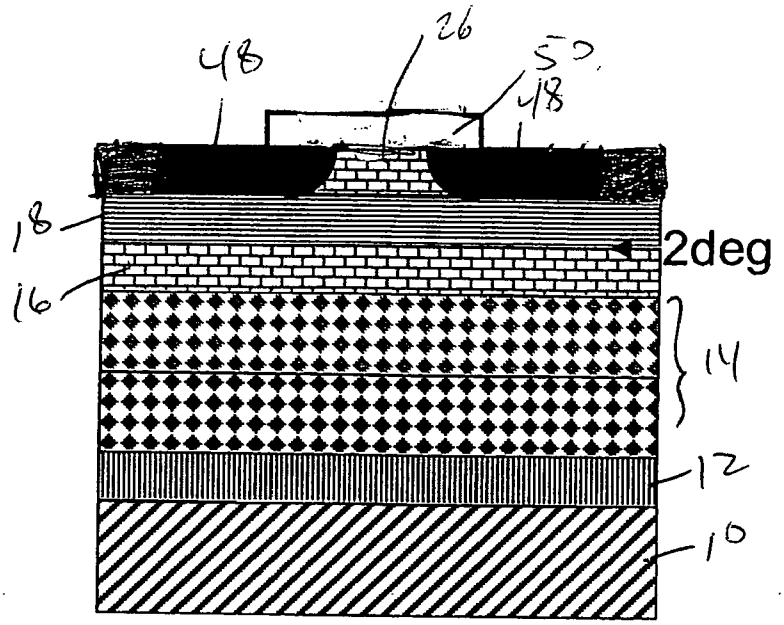

48
26
50
48
18
2deg
16
14
12
10

Fig. 8

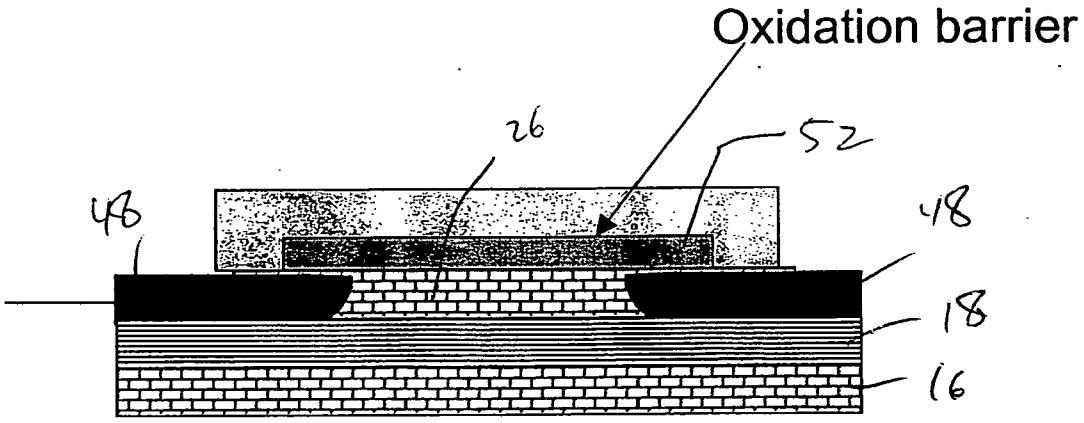

Oxidation barrier
26
52
48
48
18
16

Fig. 9

III-NITRIDE ENHANCEMENT MODE DEVICES

RELATED APPLICATION

[0001] This application is based on and claims the benefit of U.S. Provisional Application Ser. No. 60/696,985, filed on Jul. 6, 2005, entitled ACHIEVE ENHANCEMENT MODE DEVICES IN GaN, to which a claim of priority is hereby made and the disclosure of which is incorporated by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to power semiconductor devices and more particularly to III-nitride power semiconductor devices.

BACKGROUND OF THE INVENTION

[0003] A high electron mobility transistor (HEMT) is an example of a conventional power semiconductor device. A HEMT may be fabricated using a III-nitride semiconductor, which, when referred to herein, means a semiconductor alloy from the AlInGaN system such as GaN, AlGaN, InGaN, or the like.

[0004] A HEMT according to the conventionally known art includes a first III-nitride semiconductor body, which may be composed of, for example, undoped GaN, and a second III-Nitride semiconductor body, which may be composed of, for example, AlGaN, disposed over first III-nitride semiconductor body. As is well known, the heterojunction of first III-nitride semiconductor body and second III-nitride semiconductor body results in the formation of a conductive region usually referred to as a two dimensional electron gas (2DEG).

[0005] A typical HEMT further includes at least two power electrodes. The current is conducted through the 2DEG between the two power electrodes.

[0006] A HEMT may also include a gate arrangement which can be operated to disable and enable the 2DEG as desired, thereby turning the device ON or OFF. As a result, a HEMT can be operated like a field effect transistor. Indeed, such a device is sometimes referred to as a heterojunction field effect transistor (HFET).

[0007] Due to their low loss, high current carrying and high breakdown voltage capabilities III-nitride-based heterojunction power semiconductor devices are suitable for power applications. However, many III-nitride semiconductor devices are normally ON, which means that a bias to the gate is required to render the device OFF. Normally ON devices are less desirable for power application because: a) such devices are operated less efficiently that normally ON devices; b) the drive circuitry for normally ON device are more complicated and thus more expensive.

[0008] It is thus desirable to have a normally OFF III-nitride power semiconductor device.

SUMMARY OF THE INVENTION

[0009] It is an object of the present invention to provide a normally off III-nitride power semiconductor device and a method for the fabrication thereof.

[0010] According to an aspect of the present invention, nitrogen polar III-nitride semiconductor (e.g. nitrogen polar GaN) is used to fabricate a semiconductor device.

[0011] A power semiconductor device according to the preferred embodiment of the present invention includes preferably a substrate, a nitrogen polar active heterojunction having a two dimensional electron gas that includes a first III-nitride semiconductor body having one band gap, and a second III-nitride semiconductor body having another band gap over said first III-nitride semiconductor body, a gate arrangement coupled to at least said second III-nitride semiconductor body, a gate barrier interposed between said gate arrangement and said second III-nitride semiconductor body to interrupt said two dimensional electron gas when said gate is not biased, and a first power electrode and a second power electrode coupled to said at least second III-nitride semiconductor body.

[0012] In the preferred embodiment of the present invention, the gate barrier is composed of an alloy from the AlInGaN system. For example, the gate barrier may be composed of AlGaN.

[0013] In an embodiment of the present invention, the gate barrier may be spaced from each power electrode by an insulation spacer. The insulation spacers may be an oxide. For example, the insulation spacers may be composed of (AlGa)2O3.

[0014] In another embodiment of the present invention, the semiconductor device may include multiple active III-nitride heterojunctions, each including a 2DEG. At least one of the active heterojunctions can include a recess in which the gate arrangement is received.

[0015] A device according to the present invention is preferably fabricated by growing a III-nitride semiconductor body, which is preferably GaN, implanting hydrogen ions into a region in said III-nitride semiconductor body, separating said semiconductor body along said region to obtain an nitrogen polar III-nitride semiconductor body, and fabricating a III-nitride semiconductor device over said nitrogen polar semiconductor body.

[0016] According to an aspect of the present invention, the method allows for obtaining a nitrogen polar III-nitride body, e.g. nitrogen polar GaN, which in turn allows for the fabrication of enhancement type (normally OFF) devices.

[0017] The method may further include bonding a substrate to said III-nitride semiconductor body.

[0018] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. **1** schematically shows a cross-sectional view of a device according to the first embodiment of the present invention.

[0020] FIGS. **2**A-**2**F schematically show a method of fabricating a device according to the present invention.

[0021] FIG. **3**A shows a band diagram resulting from the addition of a gate barrier according to the present invention.

[0022] FIG. 3B shows a band diagram illustrating the results obtained from the addition of a gate barrier under the gate arrangement.

[0023] FIG. 4 schematically illustrates a cross-sectional view of a device according to the second embodiment of the present invention.

[0024] FIG. 5A shows the band diagram under the power electrodes of the second embodiment.

[0025] FIG. 5B shows the band diagram under the gate arrangement of the second embodiment.

[0026] FIG. 6 schematically illustrates a cross-sectional view of a device according to the third embodiment of the present invention.

[0027] FIG. 7A shows the band diagram under the power electrodes of the third embodiment.

[0028] FIG. 7B shows the band diagram under the gate arrangement of the third embodiment.

[0029] FIG. 8 schematically illustrates a step in the fabrication of the third embodiment.

[0030] FIG. 9 schematically illustrates a variation of the third embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0031] Referring to FIG. 1, a semiconductor device according to the first embodiment of the present invention includes substrate **10**, bonding layer **12**, first III-nitride buffer body **14**, first III-nitride semiconductor body **16**, second III-nitride semiconductor body **18**, first power electrode **20** and a second power electrode **22** electrically coupled to second III-nitride semiconductor body **18**, and a gate arrangement **24**.

[0032] According to an aspect of the present invention a gate barrier **26** is disposed under gate arrangement **24** and over second III-nitride semiconductor body **18**. Gate barrier **26** is an alloy from the AlInGaN, and may be preferably AlGaN

[0033] According to another aspect of the present invention, buffer layer **14** is a nitrogen polar III-nitride semiconductor material, for example, nitrogen polar GaN. As a result the entire stack formed on buffer layer **14** is nitrogen polar. First III-nitride semiconductor **16** and second III-nitride semiconductor **18** are different alloys from the AlInGaN system each having a band gap different from the other. Preferably, first III-nitride semiconductor body **16** is AlGaN, while second III-nitride semiconductor body **18** is GaN. Note that 2DEG is formed at the heterojunction of first III-nitride semiconductor body **16** and second III-nitride semiconductor body **18**, as is well known. Power electrodes **20**, **22** are thus electrically coupled to the 2DEG for current conduction. The device illustrated by FIG. **1** is a normally OFF device. That is, due to the presence of gate barrier **26**, the 2DEG is interrupted. Note that gate arrangement **24** includes a gate electrode (not specifically illustrated) which, when biased, restores the 2DEG to allow for conduction. Thus, when no bias is applied to the gate electrode the device remains off. Gate electrode may be coupled to the heterojunction of first III-nitride semiconductor **16**, and second III-nitride semiconductor **18** through a schottky contact with gate barrier **26**, or may be coupled through a gate insulator, e.g. Si3N4, SiO2 or the like without deviating from the scope and the spirit of the present invention.

[0034] According to an aspect of the present invention smart cut technology is used to fabricate a device according to the present invention.

[0035] A power semiconductor device according to the present invention is fabricated by first growing a transition layer **11** (e.g., AlN) on a suitable substrate **10** (e.g., Si), and then growing a buffer material **30** on transition layer **12**, as illustrated by FIG. **2**A.

[0036] Substrate **10** is preferably silicon, but may be a SiC, sapphire, or a GaN substrate without deviating from the scope and spirit of the present invention.

[0037] Transition layer **11** may be preferably composed of one AlN, which is graded to have different aluminum concentration along the thickness thereof, or a stack of AlN layers of varying aluminum content as is well known. Buffer material **30** is preferably GaN

[0038] As illustrated by FIG. **2**B, after the buffer material **30** is grown, hydrogen atoms **32** are implanted therein at a desired depth to form an implant region **34**. The hydrogen atom act to break the bonds between Galium and Nitrogen so that it can be easily separated.

[0039] Referring next to FIG. **2**C, a silicon material is bonded to the top surface of GaN layer **30** through, for example, silicon dioxide bonding layer **38**. GaN layer **30** is split along implant site **34**, and the top layer thereof is removed by removing silicon wafer **36**. Specifically, an annealing strip is applied which causes GaN layer **30** to split, the top portion thereof to be removed as silicon wafer **36** is removed. Note that top portion **37** includes a nitrogen polar GaN body **39**

[0040] Next, top portion **37** is flipped, and another layer of GaN **40** is grown on nitrogen polar GaN **39** using, for example, molecular beam epitaxy (MBE), whereby buffer layer **14** is formed. Thereafter, first III-nitride semiconductor body **16** (e.g. AlGaN) is grown on buffer layer **14**, second III-nitride semiconductor body **18** (e.g. GaN) is grown on first III-nitride semiconductor body **16**, and gate barrier material **42** is formed on second III-nitride semiconductor body **18**, as illustrated in FIG. **2**E. Materials for the gate arrangement are then deposited on gate barrier material **42** and the stack is patterned and etched to obtain gate arrangement **24** over gate barrier **26**, as illustrated in FIG. **2**F. Power electrodes **20**, **22** are then formed to obtain a device according to the first embodiment as illustrated in FIG. **1**. Note that the method as described results in a self-aligned gate arrangement.

[0041] Also note that although smart cutting is a preferred method, other method can be used to obtain nitrogen polar GaN. For example, a substrate can be selected on which nitrogen polar buffer GaN is grown prior to the fabrication of the devices.

[0042] Referring to FIG. **3**A, under the gate, gate barrier **26** (e.g. AlGaN) causes the bands to rise away from the structure. This added potential pulls the conduction band above the fermi level, turning off the device. However, after the removal of the gate barrier layer, the conduction band will lie below the fermi level resulting in accumulation and

a high mobility 2DEG, as illustrated by FIG. **3**B. Thus, leaving a portion of the gate barrier material under the gate arrangement as described results in the interruption of the 2DEG, which can be then restored upon application of an appropriate bias. As a result, an enhancement mode III-nitride device can be obtained according to the concept described herein.

[**0043**] A device according to the first embodiment is advantageous because:

[**0044**] it is an enhancement mode device;

[**0045**] it includes self-aligned gates;

[**0046**] its insulating back plane eliminates vertical breakdown voltage issues;

[**0047**] it does not require a thick epitaxial layer of GaN on a Si substrate;

[**0048**] its thin GaN buffer reduces parasitic leakage through the buffer under gate.

[**0049**] Referring next to FIG. **4**, a power semiconductor device according to the second embodiment includes third III-nitride semiconductor body **44**, which may be the same material as first III-nitride semiconductor body **16** (e.g., AlGaN), and fourth III-nitride semiconductor body **46**, which may be the same material as second III-nitride semiconductor body **18** (e.g., GaN). Note that fourth III-nitride semiconductor body **46** includes recess **48** to interrupt the 2DEG at the heterojunction of third **44** and fourth **46** III-nitride semiconductor bodies. Gate arrangement **24** is received in recess **48**. Although FIG. **4** shows two active III-nitride heterojunctions **19**, **21**, each including a 2DEG, a device according to the second embodiment can include multiple active III-nitride heterojunctions for increased conduction. Further note that in this embodiment layer **44** acts as a gate barrier as well as being part of an active heterojunction.

[**0050**] Note that FIG. **5**A graphically illustrates the band diagram relating to the condition of the bands under power electrodes **20**, **22**, while FIG. **5**B graphically illustrates a band diagram to illustrate the condition under gate arrangement **24** of a device according to the second embodiment.

[**0051**] A device according to the second embodiment is fabricated according to the steps illustrated in FIGS. **2**A-**2**F, except that third **44** and fourth **46** III-nitride semiconductor bodies are formed, and fourth III-nitride semiconductor body is recessed prior to forming the gate arrangement and power electrodes **20**, **22**.

[**0052**] A device according to the second embodiment is advantageous because:

[**0053**] it is an enhancement mode device;

[**0054**] it includes self-aligned gates;

[**0055**] its insulating back plane eliminates vertical breakdown voltage issues;

[**0056**] it does not require a thick epitaxial layer of GaN on a Si substrate;

[**0057**] its thin GaN buffer reduces parasitic leakage through the buffer under gate;

[**0058**] it can be fabricated using well known techniques because selective etch for GaN over AlGaN is known;

[**0059**] the fabrication thereof may allow for possible oxidation of AlGaN.

[**0060**] Referring next to FIG. **6**, a device according to the third embodiment includes gate barrier **26** on second III-nitride semiconductor **18** and under gate arrangement **24**, which is spaced from a respective power electrode on either side thereof by an oxide body **48**, for example, $(AlGa)_2O_3$.

[**0061**] FIG. **7**A illustrates the band diagram relating to the conditions under the power electrodes in the third embodiment, while FIG. **7**B illustrates a band diagram relating to the conditions under gate arrangement **24**.

[**0062**] Note that a device according to the third embodiment is fabricated according to the same steps illustrated by FIGS. **2**A-**2**B, except that a barrier material **42** is appropriately oxidized before gate arrangement is fabricated.

[**0063**] Oxide bodies **48** can be formed by masking a portion that is not to be oxidized with an appropriate mask, and then oxidizing the unmasked portions. Thus, as illustrated by FIG. **8**, a mask **50** is applied and the unmasked portions are oxidized. A suitable mask material can be Si_3N_4. Another suitable mask can be formed with silicon, which after oxidation, turns into SiO_2 **52**. SiO_2 **52** can then be used as a gate insulator.

[**0064**] The following advantages are apparent from the disclosed subject matter:

[**0065**] nitrogen polar material opens additional pathways for achieving enhancement mode III-nitride devices;

[**0066**] multiple heterojunctions can be used to produce or prevent 2DEG depending on the number of layers;

[**0067**] the use of smart cut technology allows for the production of GaN material on Si substrates without requiring a thick epitaxial GaN on silicon;

[**0068**] wafer bonding eliminates the vertical break down voltage;

[**0069**] wafer bonding reduces GaN buffer thickness and the corresponding leakage path, and also reduces constraints on buffer resistivity, thus eliminating the need for C or Fe coping and corresponding trapping issues;

[**0070**] nitrogen polar material reduces the complexity of smart cut by eliminating the second flip in bonding flow.

[**0071**] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A power semiconductor device comprising:

a substrate;

a nitrogen polar active heterojunction having a two dimensional electron gas that includes a first III-nitride semiconductor body having one band gap, and a second III-nitride semiconductor body having another band gap over said first III-nitride semiconductor body;

a gate arrangement coupled to at least said second III-nitride semiconductor body;

a gate barrier interposed between said gate arrangement and said second III-nitride semiconductor body to interrupt said two dimensional electron gas when said gate is not biased; and

a first power electrode and a second power electrode coupled to said at least second III-nitride semiconductor body.

2. The power semiconductor device of claim 1, further comprising a III-nitride buffer layer and a bonding layer between said III-nitride buffer layer and said substrate.

3. The power semiconductor device of claim 2, wherein said substrate is comprised of silicon and said bonding layer is comprised of silicon dioxide.

4. The power semiconductor device of claim 3, wherein said buffer layer is comprised of GaN.

5. The power semiconductor device of claim 1, wherein said gate barrier is comprised of an alloy of InAlGaN.

6. The power semiconductor device of claim 1, wherein said gate barrier is comprised of AlGaN.

7. The power semiconductor device of claim 1, wherein said gate barrier is spaced from each power electrode by a respective oxide body.

8. The power semiconductor device of claim 7, wherein said barrier is comprised of an alloy of AlInGaN and said oxide body is comprised (AlGa)2O3.

9. The power semiconductor device of claim 7, wherein said barrier is comprised of AlGaN and said oxide body is comprised (AlGa)2O3.

10. The power semiconductor device of claim 1, further comprising a second active III-nitride heterojunction formed over said first active III-nitride heterojunction, the second active III-nitride heterojunction including a third III-nitride semiconductor body, and a fourth III-nitride semiconductor body, the third and the fourth III-nitride semiconductor bodies having different band gaps and forming a two dimensional electron gas.

11. The power semiconductor device of claim 10, wherein said fourth III-nitride semiconductor body includes a recess therein to receive said gate arrangement.

12. A method of producing a semiconductor device, comprising:

growing a III-nitride semiconductor body;

implanting hydrogen ions into a region in said III-nitride semiconductor body;

separating said semiconductor body along said region to obtain an nitrogen polar III-nitride semiconductor body; and

fabricating a III-nitride semiconductor device over said nitrogen polar semiconductor body.

13. The method of claim 12, further comprising bonding a substrate to said III-nitride semiconductor body.

14. The method of claim 12, wherein said III-nitride semiconductor body is comprised of GaN.

15. The method of claim 12, wherein said III-nitride semiconductor device includes a gate arrangement and a gate barrier under said gate arrangement.

16. The method of claim 15, wherein said gate barrier is an alloy from the AlInGaN system.

17. The method of claim 16, wherein said gate barrier is comprised of AlGaN.

18. The method of claim 12, wherein said III-nitride semiconductor device includes a gate arrangement, a first power electrode, a second power electrode, a gate barrier under said gate arrangement, an insulation spacer disposed between each said power electrode and said gate barrier

19. The method of claim 18, wherein said gate barrier is comprised of an alloy from the AlInGaN system.

20. The method of claim 18, wherein said gate barrier is comprised of AlGaN.

21. The method of claim 18, wherein said insulation spacers are comprised of (AlGa)2O3.

22. The method of claim 12, wherein said III-nitride semiconductor device comprises at least one III-nitride active heterojunction.

23. The method of claim 12, wherein said III-nitride semiconductor device comprises at least one III-nitride active heterojunction having a recess to receive said gate arrangement.

* * * * *