

p-Type InGaN Cap Layer for Normally Off Operation in AlGaIn/GaN Heterojunction Field Effect Transistors

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The normally off operation of AlGaIn/GaN heterojunction field effect transistor (HFET) devices with a p-type InGaN cap layer under a gate electrode was demonstrated. The threshold gate voltage V_{Gth} was 0.5 V, and the maximum transconductance g_m was about 120 mS/mm. The maximum drain current I_{Dmax} was more than 210 mA/mm. RF characteristics were also measured, and it was found that f_T is 2.1 GHz and f_{max} is 6.4 GHz when the gate length is 2 μm .
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KEYWORDS: AlGaIn/GaN heterojunction field effect transistor, p-InGaN cap layer, normally off operation

1. Introduction

An AlGaIn/GaN heterojunction field effect transistor (HFET) is a promising electron device offering potential for high-power high-voltage switching applications, because GaN-based materials have superior characteristics, such as wide bandgap energy, high breakdown electric strength, high saturation electron drift velocity and strong spontaneous and piezoelectric polarization. The carrier mobility of the two-dimensional electron gas (2DEG) channel formed at the AlGaIn/GaN heterointerface is 1200–2000 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, and the sheet resistance of the 2DEG channel is 350–600 Ω . Thus, by optimizing the design of the GaN-based HFET, a high-voltage low-loss switching operation can be expected. However, switching devices in power electronic applications must operate in a normally off mode, i.e., the enhancement mode.

To achieve a normally off operation, several methods have been proposed and demonstrated. One of the methods is employing a thin AlGaIn barrier layer or recess gate.^{1–5} The sheet carrier density of the channel under the gate is reduced when the AlGaIn barrier used is thin, and the threshold gate voltage V_{Gth} increases and a nearly normally off operation is achieved. Another method is encapsulating the AlGaIn barrier with a p-type GaN layer at the gate. A negative spatial charge is induced at the interface between the AlGaIn barrier and GaN cap layers by piezoelectric polarization. The p-doping and negative spatial charge reduce the sheet carrier density of the channel under the gate. Tsuyokuchi *et al.* achieved a normally off operation with a V_{Gth} of 0.05 V using a p-GaN cap layer.⁶ However, the transconductance g_m , which is an important parameter of the device, was low. We consider that the growth temperature of the p-GaN cap layer is high and that the Mg diffusion into the AlGaIn/GaN heterointerface is marked.

On the other hand, when the AlGaIn/GaN heterostructure has an InGaN cap layer on its surface, we can expect more large negative spatial charges induced at the interface between the AlGaIn barrier and InGaN cap layers by piezoelectric polarization because the lattice constant of InGaN is larger than that of GaN. Also, the growth temperature of InGaN is low, p-InGaN can be activated more easily than p-GaN, and the effect of Mg doping can be

reduced. In addition, the etching rate of InGaN obtained by argon or chlorine plasma etching is higher than that of the GaN layer, and InGaN can be removed almost selectively.

Thus, in this study, we examined the effect of an InGaN cap layer, optimized a wafer structure by p-doping and obtained a normally off operation.

2. Experimental Procedure

The wafer structures used in this study were grown on a sapphire (0001) *c*-face substrate by metal-organic chemical vapor deposition (MOCVD; Taiyo Nippon Sanso SR4000sr). First, we compared the effects of the GaN and InGaN cap layers on the AlGaIn/GaN heterostructure. The first wafer structure, sample A, consisted of a 2- μm -thick nondoped GaN layer, a 15-nm-thick nondoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer, and a 5-nm-thick GaN cap layer. The second wafer structure, sample B, consisted of a 2- μm -thick nondoped GaN layer, a 15-nm-thick nondoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer, and a 5-nm-thick $\text{In}_{0.04}\text{Ga}_{0.96}\text{N}$ cap layer. We determined the difference in sheet resistance between the two as-grown samples. Sample A had a sheet resistance of 530–630 Ω . Sample B had a sheet resistance of 720–890 Ω .

We also fabricated HFETs using these wafer samples and compared DC operating characteristics, as shown in Figs. 1 and 2. The Ti/Al/Ni/Au source and drain electrodes on the AlGaIn surface were evaporated by electron beam evaporation. The electrodes were annealed by rapid thermal annealing (RTA) at 780 °C for 30 s. The Ni/Au gate electrode on the GaN or InGaN cap layer was evaporated by electron beam evaporation. The source–gate distance L_{SG} , gate length L_{G} , and drain–gate distance L_{DG} were 2, 2, and 4 μm , respectively. V_{G} was varied from –2 to 0 V in 1 V steps. The maximum drain current of the HFET with the GaN cap layer was 157 mA/mm when $V_{\text{G}} = 0 \text{ V}$ and $V_{\text{DS}} = 10 \text{ V}$, as shown in Fig. 1. On the other hand, the maximum drain current of the HFET with the InGaN cap layer was 105 mA/mm, as shown in Fig. 2. Thus, the transconductance of the HFET with the GaN cap layer in Fig. 1 was higher than that of the HFET with the InGaN cap layer in Fig. 2. A difference in threshold gate voltage was also observed, and the threshold voltage of the HFET with the InGaN cap layer was higher than that of the HFET with the GaN cap layer. We considered that the negative spatial charge caused by the piezoelectric effect at the interface between the AlGaIn barrier and InGaN cap layers in sample B is larger than that

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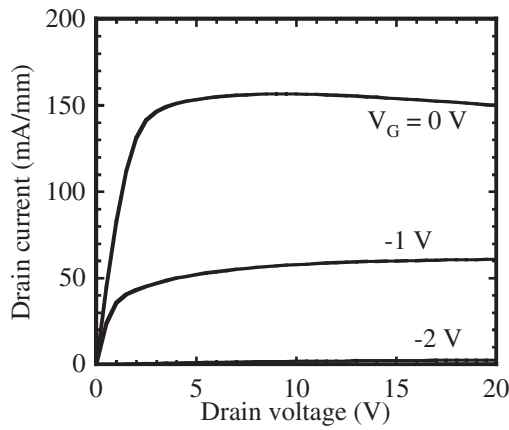


Fig. 1. Drain current I_D as function of drain voltage V_{DS} of fabricated HFET with GaN cap layer.

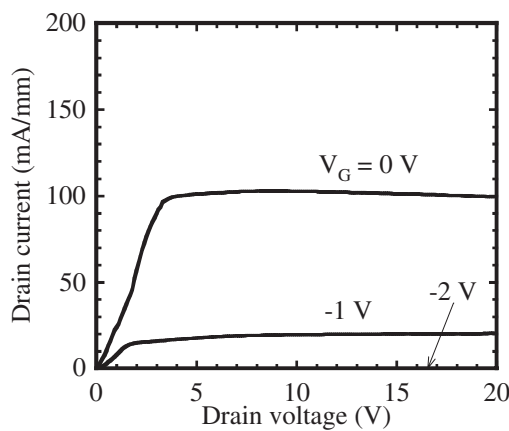


Fig. 2. Drain current I_D as function of drain voltage V_{DS} of fabricated HFET with InGaN cap layer.

at the interface between the AlGaIn barrier and GaN cap layers in sample A. Thus, the sheet carrier density of sample B was considered lower than that of sample A.

Next, in order to reduce the sheet carrier density of the AlGaIn/GaN heterojunction channel completely, we decreased the Al composition of the AlGaIn barrier layer, increased the In composition, and performed Mg doping in the InGaIn cap layer. The grown wafer, sample C, consisted of a 2- μm -thick nondoped GaN layer, a 15-nm-thick nondoped $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ barrier layer, and a 10-nm-thick p- $\text{In}_{0.17}\text{Ga}_{0.83}\text{N}$ cap layer. The doping density of the InGaIn cap layer was estimated to be about $4 \times 10^{18} \text{ cm}^{-3}$. The sheet resistance of the as-grown wafer was about 15000–100000 Ω , and we confirmed that the 2DEG at the AlGaIn/GaN heterointerface is almost completely depleted owing to the presence of the p-type InGaIn cap layer.

Using sample C, we fabricated an HFET and measured its operating characteristics. Figure 3 shows the schematic diagram of the fabricated HFET. Except under the gate, the p-InGaIn cap layer was removed by reactive ion beam etching (RIBE) with argon plasma. The etching rate of the p-type InGaIn cap layer was several times higher than that of the AlGaIn barrier layer, and the p-type InGaIn cap layer was almost selectively removed by RIBE. The photoresist of the gate pattern was used as the argon-plasma etching mask, and

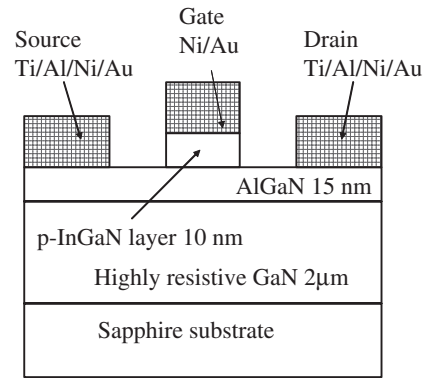


Fig. 3. Schematic diagram of fabricated HFET structure with p-InGaIn cap layer.

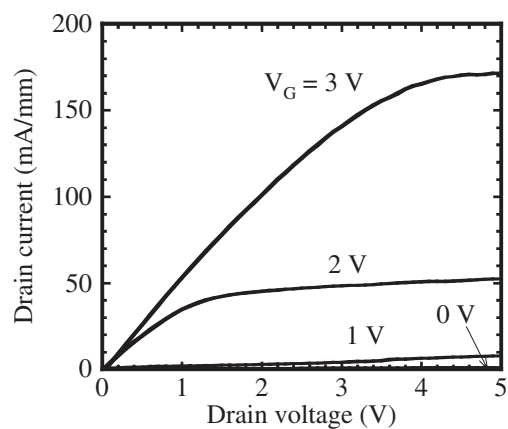


Fig. 4. Drain current I_D as function of drain voltage V_{DS} of HFET with p-InGaIn cap layer.

the alignment precision between the etching mask and the gate electrode was less than 0.5 μm . The sheet resistance after the etching of the p-type InGaIn cap layer was measured to be about 800 Ω . The Ti/Al/Ni/Au source and drain electrodes were employed. We performed transmission line model (TLM) measurements to obtain the contact resistance of the ohmic electrodes, and a low contact resistance of $9.5 \times 10^{-6} \Omega \text{ cm}^2$ was obtained. We did not observe the degradation of the ohmic characteristics due to the plasma etching by RIBE. The Ni/Au gate electrode on the p-type InGaIn cap layer was evaporated by electron beam evaporation.

Figure 4 shows the drain current characteristics as functions of the drain voltage of the fabricated device with the p-type InGaIn cap layer under the gate electrode. The source–gate distance L_{SG} , gate length L_G , and drain–gate distance L_{DG} were 2, 2, and 7 μm , respectively. V_G was varied from -1 to 3 V in +1 V steps. When $V_G = 0 \text{ V}$, a good pinch-off characteristic was obtained. The maximum drain current was 172 mA/mm when $V_G = 3 \text{ V}$ and $V_{DS} = 5 \text{ V}$.

Figure 5 shows the drain current I_D and transconductance g_m as functions of the gate voltage V_G when V_{DS} is 5 V in the case of the fabricated FET with the p-type InGaIn cap layer under the gate electrode. The gate voltage was varied from 5 to -1 V during the measurement, and a thermal effect or

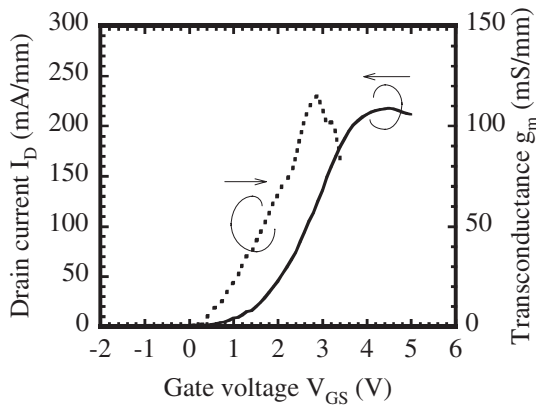


Fig. 5. Drain current I_D and transconductance g_m characteristics of HFET with p-InGaN cap layer under gate electrode.

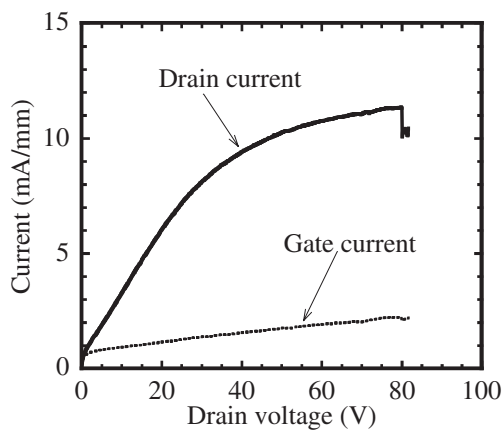


Fig. 6. Drain current I_D and gate current I_G as functions of drain voltage V_{DS} of HFET with p-InGaN cap layer when gate voltage V_G is 0 V.

drain current collapse was observed. Thus, the drain current in Fig. 5 is slightly smaller than that in Fig. 4. The threshold gate voltage V_{Gth} was found to be 0.5 V. The maximum transconductance was about 120 mS/mm. The maximum drain current I_{Dmax} shown in Fig. 5 was about 210 mA/mm.

For the future application of the fabricated HFET as the switching device, the drain breakdown characteristic is important. We show the drain and gate currents as functions of the drain voltage when the gate voltage $V_G = 0$ V in Fig. 6. The breakdown voltage of the fabricated HFET with the p-InGaN cap layer was more than 80 V. An increase in drain current at a high drain voltage was observed. These breakdown voltage characteristics are considered to be improved by employing the field plate structure connected to the gate or source electrode.

The rf characteristics of the fabricated HFET with the p-InGaN cap layer were measured and are shown in Fig. 7.

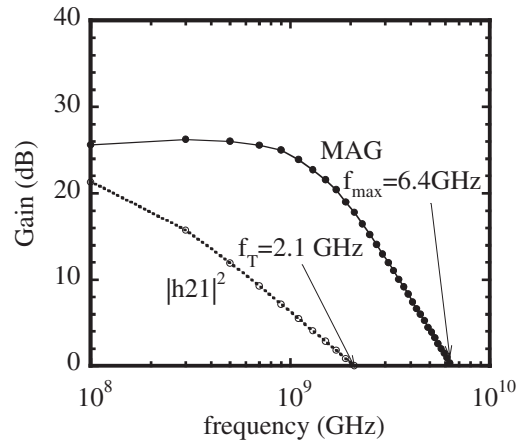


Fig. 7. RF characteristics of fabricated HFET with p-InGaN cap layer. The gate length L_G is 2 μ m.

The source–gate distance L_{SG} , gate length L_G , and drain–gate distance L_{DG} were 2, 2, and 2 μ m, respectively. The transient frequency, f_T was 2.1 GHz, and the maximum oscillation frequency f_{max} for a maximum available gain was 6.4 GHz. These rf characteristics indicate the possibility of high-speed switching using the normally off AlGaIn/GaN HFET with the p-type InGaIn cap layer.

3. Conclusions

We succeeded in obtaining normally off AlGaIn/GaN HFET devices using a p-type InGaIn cap layer under a gate electrode. The threshold gate voltage V_{Gth} was 0.5 V, and the maximum transconductance g_m was about 120 mS/mm. The maximum drain current I_{Dmax} was more than 210 mA/mm. We also measured the rf characteristics of the fabricated HFET of 2 μ m gate length with the p-type InGaIn cap layer and found that f_T is 2.1 GHz and f_{max} is 6.4 GHz. These results indicate that the p-type InGaIn cap layer on the AlGaIn barrier layer at the gate is an effective structure for obtaining a normally off operation.

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