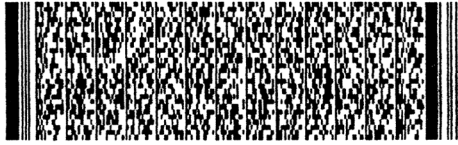


Filing Date: 92 1 23	IPC
Application Number: 92101440	H01L29/772, 21/8232

(The above columns are filled in by our office)		Invention Patent Specification	200414540
I. Invention Title	Chinese	場效電晶體結構及其製程	
	English	Field effect transistor and method of fabricating the same	
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	Representative (Chinese)	1.鄭朝元	
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I. This case has applied

for a patent to the
country (region)

Filing Date

Reference Number

Claiming the priority of
Article 24, paragraph 1
of the Patent LawII. ☐ Claiming the priority of Article 25, Paragraph 1 of the Patent Law:

Application Number:

Date:

III. Claiming that this case is within the period specified in the first ☐ or ☐ second proviso to Article 20, Paragraph 1 of the Patent Law

Date:

IV. ☐ The relevant microorganisms have been deposited abroad:

Depository Country:

Depository Institution:

Deposit Date:

Deposit Number:

☐ The relevant microorganisms have been deposited domestically (Depository institution designated by our office):

Depository Institution:

Deposit Date:

Deposit Number:

☐ For those who are skilled in the art, the microorganisms are readily available, without being deposited.

V. Description (1)

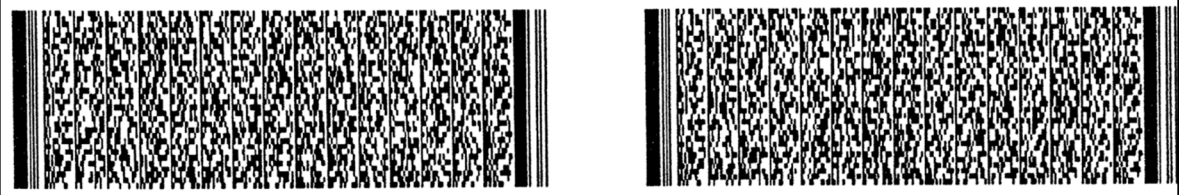
Technical Field

The present invention relates to a field effect transistor (FET), in particular to a field effect transistor with a GaN-based gate insulating layer.

Prior Art

With the advent of the digital era, all electronics companies have devoted great efforts to this flood of digital reforms, with the semiconductor industry stepping from early original equipment manufacturing to current research and development being the most significant. The integrated circuits manufactured in the semiconductor industry can be roughly divided into two types: a digital circuit layout and an analog circuit layout. The most common electronic element in the digital integrated circuit layout is a field effect transistor (FET), which can be widely applied to a micro-processor, a logical device, a memory, or other integrated circuit elements. Furthermore, due to the different fields of application of the field effect transistor, its substrates also vary in material. For a common integrated circuit, a silicon substrate is generally used, but for high-speed computing or high operating power integrated circuits, a semiconductor compound substrate with gallium nitride (GaN), gallium arsenide (GaAs) or indium phosphate (InP) as a main material is used.

FIG. 1 shows a structural schematic diagram of a conventional field effect transistor employing a gallium nitride substrate. Referring to FIG. 1, the conventional field effect transistor is mainly composed of a gallium nitride substrate 100, a GaN-based semiconductor layer 102, a source 104, a drain 106 and a gate 108, wherein the GaN-based semiconductor layer 102 is provided on the gallium nitride substrate 100, while the GaN-based semiconductor layer 102 is generally formed on the gallium nitride substrate 100 by means of epitaxy, and the material of the GaN-based semiconductor layer 102 is $\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $1 \geq x \geq 0$. Furthermore, the source 104, the drain 106 and the gate 108 are provided

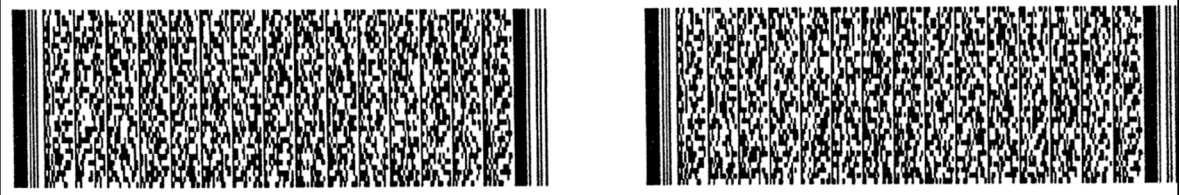


V. Description (2)

on the GaN-based semiconductor layer 102, and the source 104 and the drain 106 are located on both sides of the gate 108, respectively.

FIG. 2 shows a structural schematic diagram of a conventional field effect transistor for high-power operation. Referring to both FIG. 1 and FIG. 2, in the field effect transistor shown in FIG. 1, since the gate 108 is directly located on the GaN-based semiconductor layer 102, the gate leakage current of the element cannot be effectively suppressed under high temperature and high-power operation, thereby influencing the characteristics of the element. For the requirements of high temperature resistance and high operating power of the element, if a gate insulating layer 110 (shown in FIG. 2) can be provided between the gate 108 and the GaN-based semiconductor layer 102, it is expected that the breakdown voltage of the element will be significantly increased, thereby reducing the gate leakage current of the element. However, in the conventional field effect transistor, for the gate insulating layer 110, insulating materials such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4) and gallium oxide (Ga_2O_3) are directly used. After actual production, the gate insulating layers 110 of these insulating materials are found to have poor lattice matching with the GaN-based semiconductor layer 102, so the operating characteristics of the element cannot be accurately evaluated. Due to the lack of high-quality insulating layers in III-V group materials, it is quite difficult to fabricate a metal-insulating layer-semiconductor field effect transistor (MISFET) with stable electrical characteristics.

In order to improve the problem that the insulating layer mentioned above is not proper, the practice of using a semi-insulating homogeneous material to replace the insulating layer on a GaAs substrate has been proposed. This practice attempts to improve the lattice matching characteristics between the gate insulating layer and the substrate, so that the metal-insulating layer-semiconductor field effect transistor (MISFET) has good electrical



V. Description (3)

characteristics. Since a low-temperature growth process is employed for forming gallium arsenide, the insulating layer formed by the low-temperature process between the gate and the substrate still needs to undergo high-temperature heat treatment (post annealing) to have good insulation characteristics. However, the gallium arsenide substrate will be partially damaged in the high-temperature process and the steps of the high-temperature process are relatively complicated, which is not only time-consuming but also costly.

Summary

Therefore, a purpose of the present invention is to provide a field effect transistor, which can reduce the gate leakage current of an element by improving the lattice matching degree between the gate insulating layer and the GaN-based semiconductor layer.

Another purpose of the present invention is to provide a field effect transistor, which has low manufacturing cost and simple process steps.

Yet another purpose of the present invention is to provide a field effect transistor that is resistant to high temperatures and suitable for high-power operation.

To achieve the above purposes, the present invention provides a field effect transistor, mainly composed of a gallium nitride substrate, a GaN-based semiconductor layer, a GaN-based gate insulating layer, a source/drain and a gate. The GaN-based semiconductor layer is located on the gallium nitride substrate. The GaN-based gate insulating layer is provided on the GaN-based semiconductor layer, and the GaN-based gate insulating layer is an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$. The source/drain is provided on the GaN-based semiconductor layer and located next to the GaN-based gate insulating layer, and the gate is then provided on the GaN-based gate insulating layer.

According to an exemplary embodiment of the present invention, there is, for example,



V. Description (4)

a dopant in the GaN-based gate insulating layer to enhance the resistance value of the GaN-based gate insulating layer, and this dopant is metal such as carbon, magnesium, iron, or a combination of these materials or grows at low temperatures (300°C to 900°C).

According to an exemplary embodiment of the present invention, the GaN-based semiconductor layer is, for example, an $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, where $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $a < x$.

According to an exemplary embodiment of the present invention, the field effect transistor is, for example, a modulation doped FET (MODFET). Therefore, the GaN-based semiconductor layer in this embodiment is, for example, composed of a buffer layer, a channel layer, a gap layer and a barrier layer. The buffer layer and the channel layer are each, for example, an undoped $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, and $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $x > a$. The gap layer, for example, is an undoped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$. The barrier layer, for example, is a silicon doped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

As mentioned above, in the field effect transistor in this embodiment, an isolation layer is, for example, provided between the buffer layer and the channel layer. The material of this isolation layer is, for example, an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer that is carbon, magnesium and iron doped or grows at low temperature (300 to 900°C), and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

In the present invention, a GaN-based material is employed as the gate insulating layer, which has good lattice matching characteristics with the GaN-based semiconductor layer, and has good insulation characteristics after being doped with appropriate dopants (metals such as carbon, magnesium and iron). Therefore, the field effect transistor of the present invention has superior electrical characteristics.

In order to make the above and other purposes, features and advantages of the present invention more obvious and easier to understand, an exemplary embodiment is given, and



V. Description (5)

in conjunction with the accompanying drawings, a detailed explanation is given as follows:

Detailed Description

FIG. 3 shows a structural schematic diagram of a field effect transistor according to a first exemplary embodiment of the present invention. Referring to FIG. 3, a field effect transistor in this embodiment is mainly composed of a gallium nitride substrate 200, a GaN-based semiconductor layer 202, a GaN-based gate insulating layer 210, a source 204, a drain 206 and a gate 208. The GaN-based semiconductor layer 202 is located on the gallium nitride substrate 200, and its material is, for example, $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$, where $a \geq 0$, $b \geq 0$, $1 \geq a+b$. The GaN-based gate insulating layer 210 is provided on the GaN-based semiconductor layer 202, and the material of the GaN-based gate insulating layer 210 is $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$, $x > a$. Furthermore, the gate 208 is then provided on the GaN-based gate insulating layer 210, while the source 204 and the drain 206 are located on the GaN-based semiconductor layers 202 on both sides of the gate 208.

In this embodiment, there is, for example, a dopant in the GaN-based gate insulating layer 210 to enhance the resistance value of the GaN-based gate insulating layer 210, and this dopant is metal such as carbon, magnesium, iron or a combination of these materials, and these dopants (such as carbon, iron and magnesium) are, for example, doped in the epitaxy process. Furthermore, the resistance value of the GaN-based gate insulating layer 210 mentioned above is, for example, between 10⁹ ohms and 10¹² ohms/ $\square$.

In this embodiment, since the GaN-based gate insulating layer 210 is provided on the GaN-based semiconductor layer 202, and the two layers are of similar materials, the lattice matching characteristics are very good. In other words, the interface characteristics between the GaN-based gate insulating layer 210 and the GaN-based semiconductor layer 202 are good, so there will be no depression of the element characteristics due to too much



V. Description (6)

difference in material characteristics between the two layers. Furthermore, the GaN-based gate insulating layer 210 in this embodiment is fabricated, for example, using a low-temperature process. The GaN-based gate insulating layer 210 can be generated in a low-temperature state (300°C to 900°C), and an excellent insulation effect can be achieved without the need for high-temperature heat treatment (post annealing) after epitaxy.

From the above, it can be seen that the GaN-based gate insulating layer 210 has good insulation characteristics after low-temperature epitaxial growth, which is quite simple to fabricate. Moreover, the high resistance characteristics of the GaN-based gate insulating layer 210 will make the field effect transistor have the operating characteristics of high temperature resistance and high power.

Although the above-mentioned GaN-based gate insulating layer 210 is illustrated in terms of fabrication with taking the low-temperature epitaxy process as an example, the present invention is not limited to employing the low-temperature epitaxy process to achieve this. In the present invention, the epitaxial growth of the GaN-based gate insulating layer 210 can also be performed in other temperature states to directly generate the GaN-based gate insulating layer 210 with good insulation characteristics.

FIG. 4 shows a diagram of a relationship between reverse bias voltage and gate leakage current in the field effect transistor of FIGS. 1 and 3. Referring to FIG. 4, curve A is a relationship between the reverse bias voltage and the gate leakage current of a conventional gallium nitride field effect transistor without the gate insulating layer, while curve B is a relationship between the reverse bias voltage and the gate leakage current of the gallium nitride field effect transistor with a GaN-based gate insulating layer of high resistance value in this embodiment. From the FIG. 4, it can be clearly seen that by comparison between the gate leakage current of the conventional gallium nitride field effect transistor and the gate



V. Description (7)

leakage current of the gallium nitride field effect transistor in this embodiment, the difference therebetween exceeds 1000 times. Based on the conventional experience of fabricating the field effect transistor, it can be predicted that such excellent insulation characteristics will inevitably meet the needs of high-temperature and high-power operation of the element.

In addition to being applied to the structure shown in FIG. 3, the GaN-based gate insulating layer of the present invention can be applied to other elements that apply a GaN-based epitaxial material layer, such as elements including the modulation doped field effect transistor (MODFET) or a high electron mobility transistor (HEMT) of other architectures. It will be illustrated below only for the application level of the modulation doped field effect transistors (MODFET).

FIG. 5 shows a structural schematic diagram of a field effect transistor according to a second exemplary embodiment of the present invention. Referring to FIG. 5, a modulation doped field effect transistor (MODFET) is mainly composed of a gallium nitride substrate 300, a GaN-based semiconductor layer 302, a GaN-based gate insulating layer 318, a source 312, a drain 314 and a gate 316. The GaN-based semiconductor layer 302 is located on the gallium nitride substrate 300. The GaN-based gate insulating layer 318 is provided on the GaN-based semiconductor layer 302, and the material of the GaN-based gate insulating layer 318 is $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$, $x > a$. Furthermore, the gate 316 is then provided on the GaN-based gate insulating layer 318, while the source 312 and the drain 314 are located on the GaN-based semiconductor layers 302 on both sides of the gate 318.

Also referring to FIG. 5, in the architecture of the modulation doped field effect transistor, the GaN-based semiconductor layer 302 is composed of, for example, a buffer



V. Description (8)

layer 304, a channel layer 306, a gap layer 308 and a barrier layer 310. The buffer layer 304 and the channel layer 306 are each, for example, an undoped $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, and $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $x > a$. The gap layer 308, for example, is an undoped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$; while the barrier layer 310, for example, is a silicon doped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

Similar to the previous embodiment, the GaN-based gate insulating layer 318 in this embodiment may also have a dopant to enhance the resistance value of the GaN-based gate insulating layer 318 (about 109 ohms to 1012 ohms/ $\square$), such as metal such as carbon, magnesium, iron or a combination of these materials, and these dopants (metals such as carbon, iron, and magnesium) are, for example, doped in the epitaxy process.

FIG. 6 shows a structural schematic diagram of a field effect transistor according to a third exemplary embodiment of the present invention. Referring to both FIG. 5 and FIG. 6, this embodiment is similar to FIG. 5, except that an isolation layer 305 is provided between the buffer layer 304 and the channel layer 306 in this embodiment, and the material of the isolation layer 305 is, for example, $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ like that of the gate insulating layer 318, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

The above disclosed field effect transistor device architecture mainly aims to enhance the gate collapse characteristics of the device itself, thereby achieving the purpose of high-power operation. In addition, the GaN-based insulating layer mentioned above can also be used as an insulating buffer layer between a semiconductor epitaxial layer and the substrate, which can effectively eliminate the side-gating effect or the back-gating effect, and output conductance is substantially reduced, which is more conducive to high-frequency operation.

Although the present invention has been disclosed as above in multiple exemplary



V. Description (9)

embodiments, it is not intended to limit the present invention. Anyone skilled in this art may make some modifications and embellishments within the spirit and scope of the present invention. Therefore, the scope of protection of the present invention shall be subject to the scope defined in the attached claims.



Brief Description of The Drawings

FIG. 1 shows a structural schematic diagram of a conventional field effect transistor employing a gallium nitride substrate;

FIG. 2 shows a structural schematic diagram of a conventional field effect transistor for high-power operation;

FIG. 3 shows a structural schematic diagram of a field effect transistor according to a first exemplary embodiment of the present invention;

FIG. 4 shows a diagram of a relationship between reverse bias voltage and gate leakage current in the field effect transistor of FIGS. 1 and 3;

FIG. 5 shows a structural schematic diagram of a field effect transistor according to a second exemplary embodiment of the present invention; and

FIG. 6 shows a structural schematic diagram of a field effect transistor according to a third exemplary embodiment of the present invention.

Reference Numerals

- 100: Gallium nitride substrate
- 102: GaN-based semiconductor layer
- 104: Source
- 106: Drain
- 108: Gate
- 110: Gate insulating layer
- 200: Gallium nitride substrate
- 202: GaN-based semiconductor layer
- 204: Source
- 206: Drain



Brief Description of The Drawings

208: Gate
210: GaN-based gate insulating layer
300: Gallium nitride substrate
302: GaN-based semiconductor layer
304: Buffer layer
305: Isolation layer
306: Channel layer
308: Gap layer
310: Barrier layer
312: Source
314: Drain
316: Gate
318: GaN-based gate insulating layer



IV. Abstract (Chinese) (TITLE: 場效電晶體結構及其製程)

一種場效電晶體結構，主要係由氮化鎵基材、氮化鎵基礎(GaN-based)半導體層、氮化鎵基礎閘極絕緣層、源極/汲極以及閘極所構成。其中，氮化鎵基礎半導體層係位於氮化鎵基材上；氮化鎵基礎(GaN-based)閘極絕緣層係配置於氮化鎵基礎半導體層上，且氮化鎵基礎閘極絕緣層為一 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；源極/汲極係配置於氮化鎵基礎半導體層上，且位於氮化鎵基礎閘極絕緣層旁；而閘極則配置於氮化鎵基礎閘極絕緣層上。上述之氮化鎵基礎(GaN-based)閘極絕緣層在製作上不需經過磊晶後的高溫熱處理，製程更形簡單，且使得場效電晶體能夠達到高耐溫與高功率操作的目的。

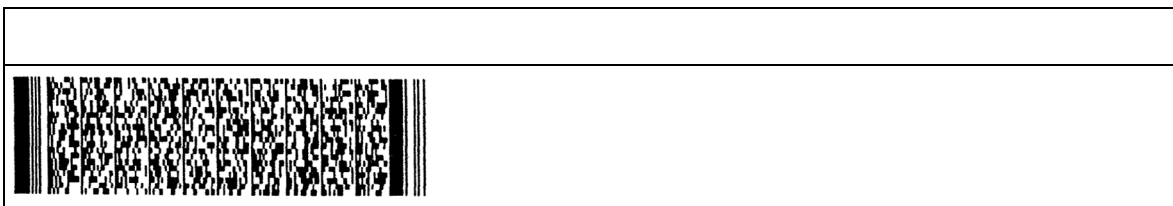
V. (I) Representative drawing: FIG. 6

(II). Brief description of component representative symbols of representative drawings:
 300: Gallium nitride substrate 302: GaN-based semiconductor layer 304: Buffer layer 305: Isolation layer 306: Channel layer 308: Gap layer 310: Barrier layer 312: Source 314: Drain 316: Gate 318: GaN-based gate insulating layer

VI. Abstract (English) (TITLE: Field effect transistor and method of fabricating the same)

A field effect transistor is provided, mainly composed of a gallium nitride substrate, a GaN-based semiconductor layer, a GaN-based gate insulating layer, a source/drain and a gate. The GaN-based semiconductor layer is located on the gallium nitride substrate. The GaN-based gate insulating layer is provided on the GaN-based semiconductor layer, and the GaN-based gate insulating layer is an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$. The source/drain is provided on the GaN-based semiconductor layer and located next to the GaN-based gate insulating layer, and the gate is provided on the GaN-based gate insulating layer. The GaN-based gate insulating layer mentioned above does not require high-temperature heat treatment after epitaxy, so that the process is simpler and the field effect transistor is enabled to achieve the purposes of high temperature resistance and high-power operation.

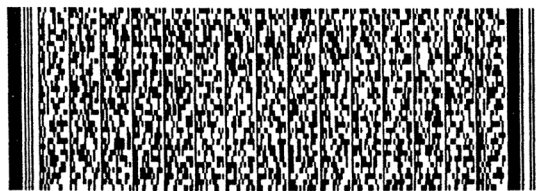
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VI. CLAIMS

What is claimed is:

1. A field effect transistor, comprising:
 - a gallium nitride substrate;
 - a GaN-based semiconductor layer, located on the gallium nitride substrate;
 - a GaN-based gate insulating layer, provided on the GaN-based conductive layer, and the nitride based gate insulating layer is an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$;
 - a source/drain, provided on the GaN-based semiconductor layer, and located next to the GaN -based gate insulating layer; and
 - a gate, provided on the GaN-based gate insulating layer.
2. The field effect transistor according to claim 1, wherein the GaN-based semiconductor layer is an $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, where $a \geq 0$, $b \geq 0$, $1 \geq a+b$.
3. The field effect transistor according to claim 1, wherein the GaN-based semiconductor layer comprises:
 - a buffer layer, located on the gallium nitride substrate;
 - a channel layer, located on the buffer layer;
 - a gap layer, located on the channel layer; and
 - a barrier layer, located on the gap layer and between the GaN-based gate insulating layer and the source/drain.
4. The field effect transistor according to claim 3, wherein the buffer layer and the channel layer are each an undoped $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, and $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $x > a$.
5. The field effect transistor according to claim 3, wherein the gap layer is an undoped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.
6. The field effect transistor according to claim 3, wherein the barrier layer is a silicon doped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.



VI. CLAIMS

7. The field effect transistor according to claim 1, wherein the GaN-based semiconductor layer comprises:

- a buffer layer, located on the gallium nitride substrate;
- an isolation layer, located on the buffer layer;
- a channel layer, located on the isolation layer;
- a gap layer, located on the channel layer; and
- a barrier layer, located on the gap layer and between the GaN-based gate insulating layer and the source/drain.

8. The field effect transistor according to claim 7, wherein the buffer layer and the channel layer are each an undoped $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, and $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $x > a$.

9. The field effect transistor according to claim 7, wherein the isolation layer is an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

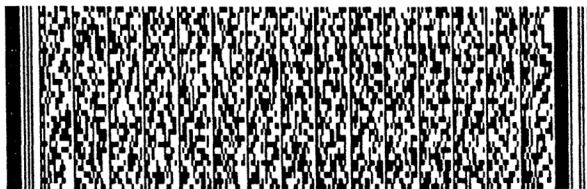
10. The field effect transistor according to claim 7, wherein the gap layer is an undoped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

11. The field effect transistor according to claim 7, wherein the barrier layer is a silicon doped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

12. The field effect transistor according to claim 1, wherein the GaN-based gate insulating layer has a dopant, and the dopant comprises one of carbon, magnesium, iron and a combination thereof.

13. A field effect transistor, comprising:

- a gallium nitride substrate;
- a buffer layer, located on the gallium nitride substrate;



VI. CLAIMS

a channel layer, located on the buffer layer, wherein the buffer layer and the channel layer are each an undoped $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ layer, and $a \geq 0$, $b \geq 0$, $1 \geq a+b$;

a gap layer, located on the channel layer, wherein the gap layer is an undoped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$; and

a barrier layer, located on the gap layer, wherein the barrier layer is a silicon doped $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, and $x \geq 0$, $y \geq 0$, $1 \geq x+y$;

a GaN-based gate insulating layer, provided on the GaN-based semiconductor layer, wherein the GaN-based gate insulating layer is an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$, $x > a$;

a source/drain, provided on the GaN-based semiconductor layer, and located next to the GaN-based gate insulating layer; and

a gate, provided on the GaN-based gate insulating layer.

14. The field effect transistor according to claim 13, further comprising an isolation layer, the isolation layer being provided between the buffer layer and the channel layer.

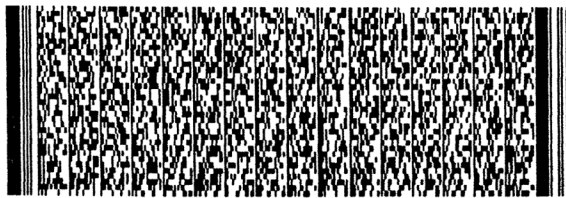
15. The field effect transistor according to claim 14, wherein the isolation layer is an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$.

16. The field effect transistor according to claim 13, wherein the GaN-based gate insulating layer has a dopant, and the dopant comprises one of carbon, magnesium, iron and a combination thereof.

17. A process for a field effect transistor, comprising the following steps:

forming a GaN-based semiconductor layer on a gallium nitride substrate;

forming a GaN-based gate insulating layer on the GaN-based semiconductor layer, wherein the GaN-based gate insulating layer is an $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer, where $x \geq 0$, $y \geq 0$, $1 \geq x+y$;



VI. CLAIMS

forming a source/drain on the GaN-based semiconductor layer next to the GaN-based gate insulating layer; and

forming a gate on the GaN-based gate insulating layer.

18. The process for the field effect transistor according to claim 17, wherein the forming the GaN-based semiconductor layer comprises:

forming a buffer layer on the gallium nitride substrate;

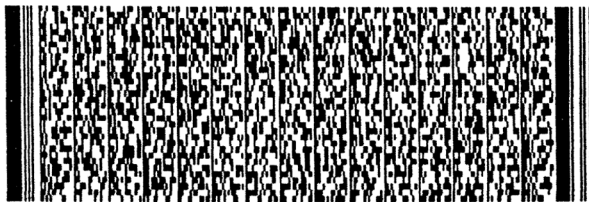
forming a channel layer on the buffer layer;

forming a gap layer on the channel layer; and

forming a barrier layer on the gap layer and between the GaN-based gate insulating layer and the source/drain.

19. The process for the field effect transistor according to claim 18, further comprising forming an isolation layer between the buffer layer and the channel layer.

20. The process for the field effect transistor according to claim 19, wherein the method for forming the GaN-based gate insulating layer and the isolation layer comprises a low-temperature growth method, and the process temperature of the low-temperature growth method is between 300°C and 900°C.



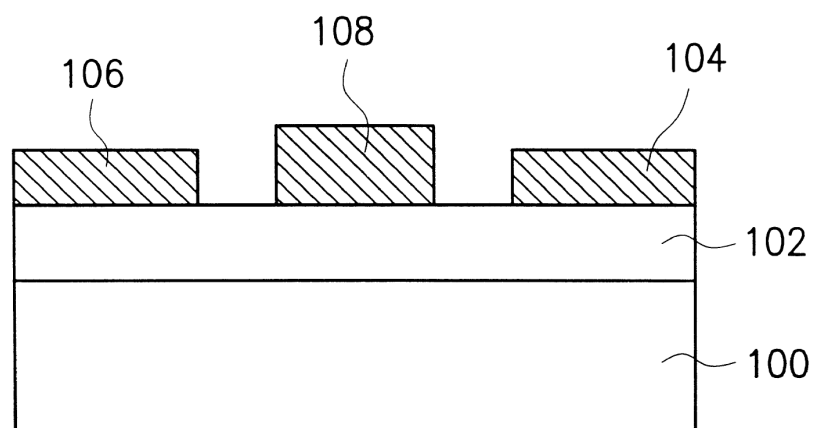


FIG. 1

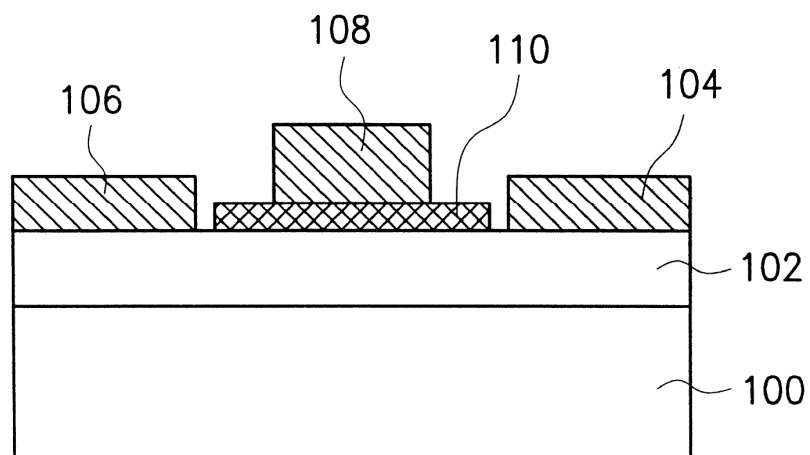


FIG. 2

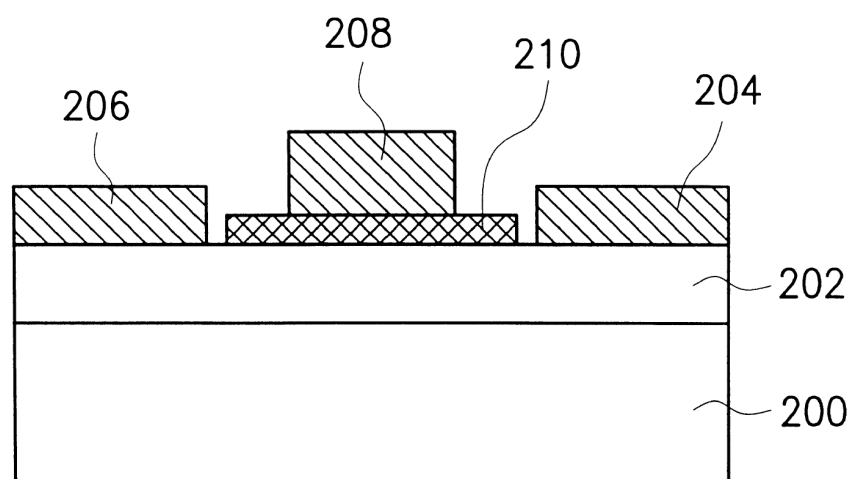


FIG. 3

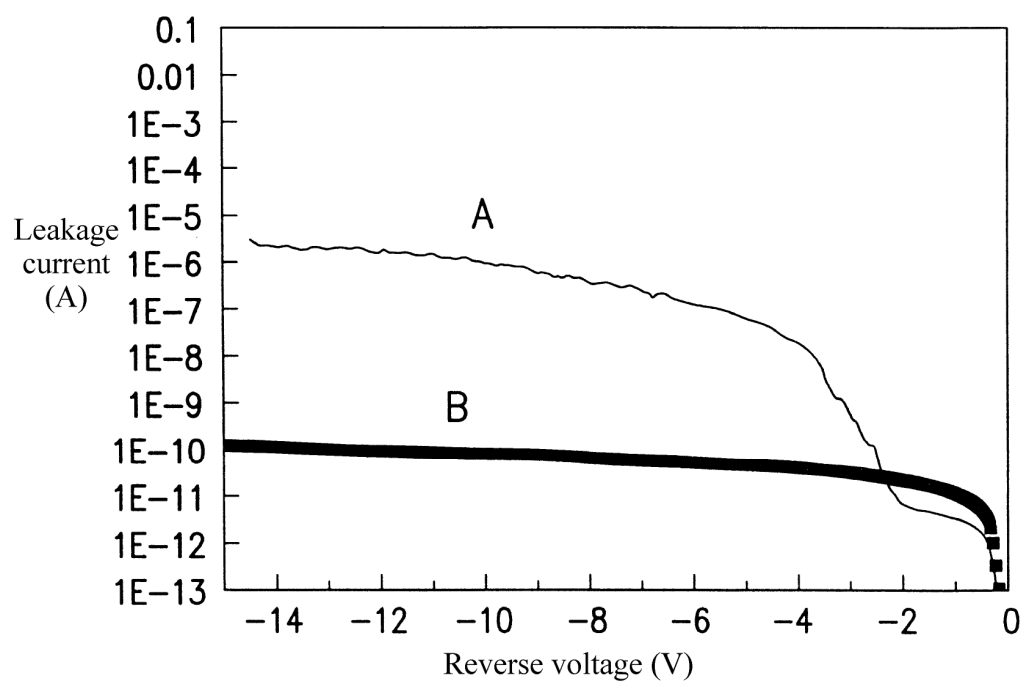


FIG. 4

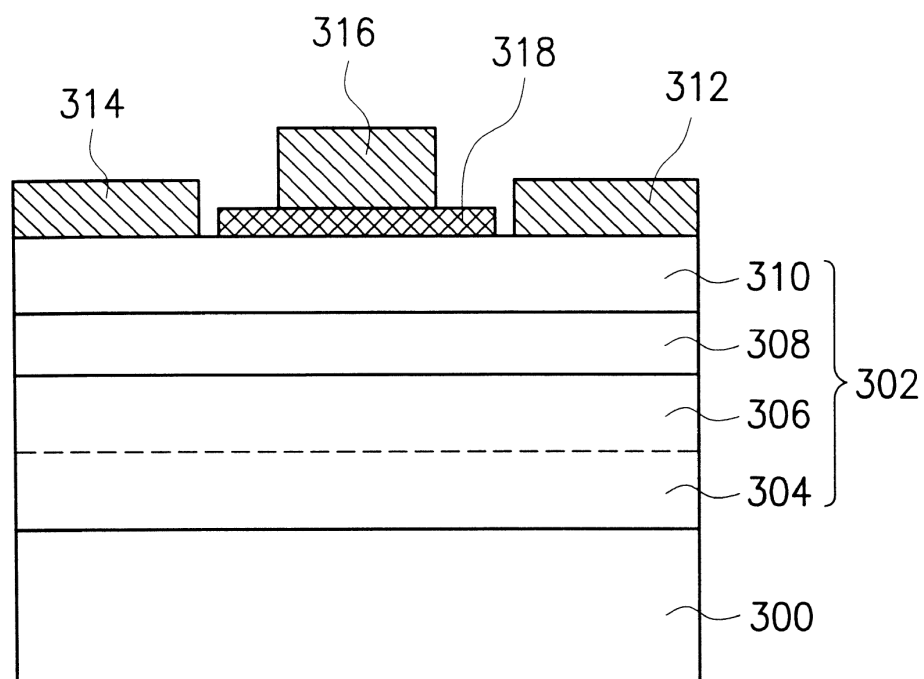


FIG. 5

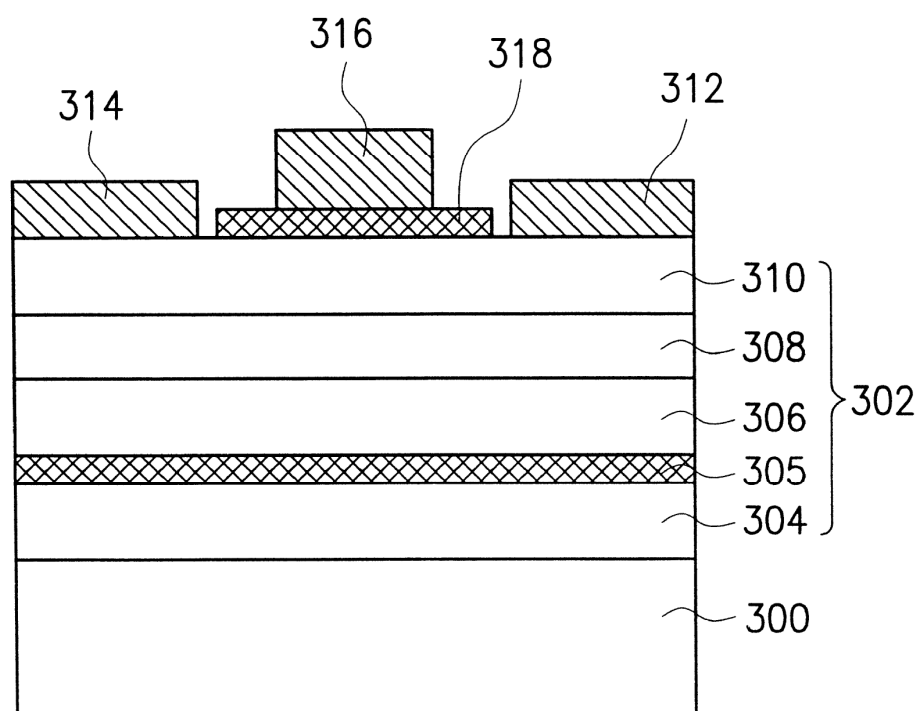


FIG. 6

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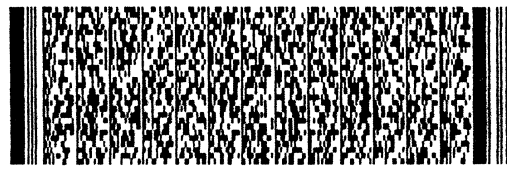
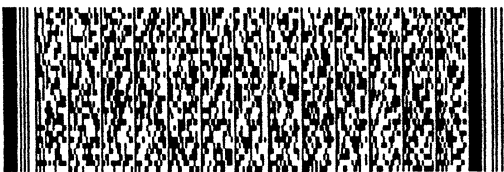
申請日期：92 1 23	IPC分類
申請案號：92101440	H01L29/772, 21/8232

(以上各欄由本局填註)

發明專利說明書

200114540

一、 發明名稱	中 文	場效電晶體結構及其製程
	英 文	Field effect transistor and method of fabricating the same
二、 發明人 (共2人)	姓 名 (中文)	1. 許進恭 2. 賴韋志
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	國 籍 (中英文)	1. 中華民國 TW
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	代表人 (中文)	1. 鄭朝元
	代表人 (英文)	1. Chao-yuan Cheng



一、本案已向

國家(地區)申請專利	申請日期	案號	主張專利法第二十四條第一項優先權
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二、☐主張專利法第二十五條之一第一項優先權：

申請案號：

日期：

三、主張本案係符合專利法第二十條第一項☐第一款但書或☐第二款但書規定之期間

日期：

四、☐有關微生物已寄存於國外：

寄存國家：

寄存機構：

寄存日期：

寄存號碼：

☐有關微生物已寄存於國內(本局所指定之寄存機構)：

寄存機構：

寄存日期：

寄存號碼：

☐熟習該項技術者易於獲得，不須寄存。



五、發明說明 (1)

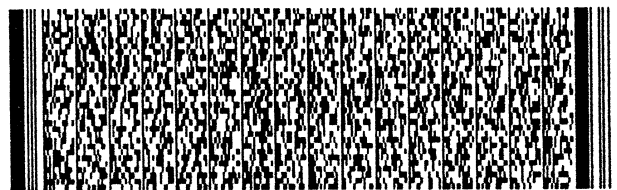
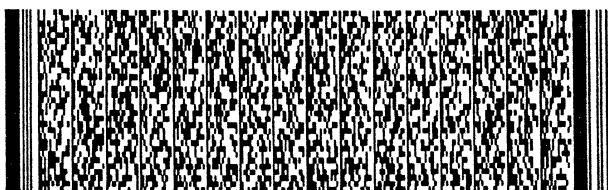
發明所屬之技術領域

本發明是有關於一種場效電晶體結構(Field Effect Transistor, FET)，且特別是有關於一種具有氮化鎵基礎閘極絕緣層(GaN-based Gate insulating layer)之場效電晶體結構。

先前技術

數位時代來臨，各電子業者皆針對此波數位化改革投注莫大心力，其中又以半導體產業由早期代工至目前邁向研發的腳步最為顯著。對於半導體產業中所製造的積體電路可略分為數位電路佈局與類比電路佈局兩大型態，而數位積體電路佈局中最常見的電子元件即屬場效電晶體(FET)，其可廣泛地應用於微處理器(micro-processor)、邏輯元件(logical device)、記憶體(memory)，或其他積體電路元件中。此外，由於場效電晶體所應用的領域不同，故其基材的材料亦相異，一般的積體電路通常是使用矽基材，但針對高速運算或高操作功率之積體電路則採用以氮化鎵(GaN)、砷化鎵(GaAs)或是磷化銦(InP)為主要材料的半導體化合物基材。

第1圖繪示為習知採用氮化鎵基材之場效電晶體的結構示意圖。請參照第1圖，習知的場效電晶體主要係由氮化鎵基材100、氮化鎵基礎(GaN-based)半導體層102、源極104、汲極106，以及閘極108所構成。其中，氮化鎵基礎半導體層102配置於氮化鎵基材100上，而氮化鎵基礎半導體層102通常係藉由磊晶的方式形成於氮化鎵基材100，

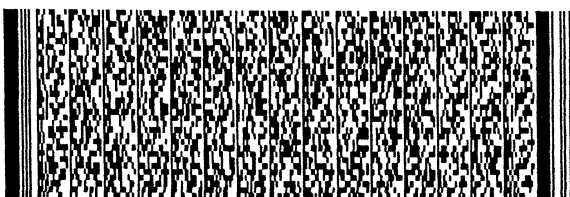


五、發明說明 (2)

且氮化鎵基礎半導體層102之材質為 $\text{Al}_x\text{Ga}_{1-x}\text{N}$ ，其中 $1 \geq x \geq 0$ 。此外，源極104、汲極106，以及閘極108係配置於氮化鎵基礎半導體層102上，且源極104、汲極106分別位於閘極108的兩側。

第2圖繪示為習知高功率操作之場效電晶體的結構示意圖。請同時參照第1圖與第2圖，第1圖所繪示之場效電晶體結構中，由於閘極108係直接位於氮化鎵基礎半導體層102上，故在高溫、高功率操作的情況下，元件的閘極漏電流並無法有效的抑制，進而影響其特性。針對元件耐高溫與高操作功率的需求而言，若能在閘極108與氮化鎵基礎半導體層102之間配置一閘極絕緣層110（繪示於第2圖），預期將可大幅提昇元件的崩潰電壓，進而降低其閘極漏電流。然而，習知的場效電晶體結構中，閘極絕緣層110係直接使用二氧化矽(SiO_2)、氮化矽(Si_3N_4)、氧化鎵(Ga_2O_3)等絕緣材質，這些絕緣材質之閘極絕緣層110在實際生產之後發現其與氮化鎵基礎半導體層102之間的晶格匹配度不佳，故元件的操作特性便無法準確的評估。正由於III-V族材料中缺乏品質良好的絕緣層，故要製作出電氣特性穩定之金屬-絕緣層-半導體場效電晶體(MISFET)相當困難。

為了改善上述絕緣層不適當的問題，一種在砷化鎵基材(GaAs substrate)上使用半絕緣同質材料取代絕緣層的做法已被提出，此作法試圖提高閘極絕緣層與基材之間的晶格匹配特性，以使得金屬-絕緣層-半導體場效電晶體



五、發明說明 (3)

(MISFET) 具有良好的電氣特性。由於形成砷化鎵係採用低溫成長的製程，故在閘極與基材之間以低溫製程形成的絕緣層仍須經過高溫熱處理(post annealing)，才會具有良好的絕緣特性，但因為高溫製程中仍會對砷化鎵基材造成部份的破壞，且高溫製程的步驟較為繁雜，不僅耗時且增加成本。

發明內容

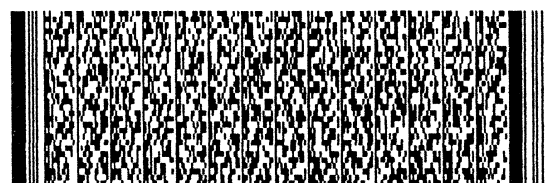
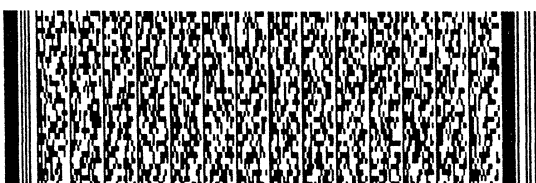
因此，本發明的目的就是在提供一種場效電晶體結構，其可藉由改善閘極絕緣層與氮化鎵基礎半導體層之間晶格匹配程度，以降低元件之閘極漏電流。

本發明的另一目的就是在提供一種場效電晶體結構，其製造成本低廉且製程步驟簡易。

本發明的另再一目的就是在提供一種耐高溫且適於高功率操作之場效電晶體結構。

為達上述目的，本發明提供一種場效電晶體結構，主要係由氮化鎵基材、氮化鎵基礎半導體層、氮化鎵基礎閘極絕緣層、源極/汲極以及閘極所構成。其中，氮化鎵基礎半導體層係位於氮化鎵基材上；氮化鎵基礎閘極絕緣層係配置於氮化鎵基礎半導體層上，且氮化鎵基礎閘極絕緣層為一 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；源極/汲極係配置於氮化鎵基礎半導體層上，且位於氮化鎵基礎閘極絕緣層旁；而閘極則配置於氮化鎵基礎閘極絕緣層上。

依照本發明的較佳實施例所述，氮化鎵基礎閘極絕緣



五、發明說明 (4)

層中例如具有一摻質，以增進氮化鎵基礎閘極絕緣層的電阻值，且此摻質例如為碳、鎂、鐵等金屬或是這些材質之組合或以低溫成長（攝氏300至900度）。

依照本發明的較佳實施例所述，氮化鎵基礎半導體層例如為一 $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ 層，其中 $a \geq 0$ ， $b \geq 0$ ， $1 \geq a+b$ ， $a < x$ 。

依照本發明的較佳實施例所述，場效電晶體例如為調製摻雜場效電晶體 (Modulation Doped FET, MODFET)，因此本實施例中的氮化鎵基礎半導體層例如是由緩衝層、通道層、間隙層以及阻障層所構成。其中，緩衝層與通道層例如為一未摻雜之 $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ 層，且 $a \geq 0$ ， $b \geq 0$ ， $1 \geq a+b$ ， $x > a$ ；間隙層例如為一未摻雜之 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；阻障層例如為一矽摻雜的 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ 。

承上述，本實施例之場效電晶體結構中，在緩衝層與通道層之間例如配置有一隔絕層，此隔絕層之材質例如為一碳、鎂、鐵摻雜的或低溫成長的（攝氏300至900度） $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ 。

本發明因採用氮化鎵基礎材質 (GaN-based material) 作為閘極絕緣層，其與氮化鎵基礎半導體層之間具有良好的晶格匹配特性，且在摻雜適當的摻質（碳、鎂、鐵等金屬）之後具有良好的絕緣特性，故本發明之場效電晶體具有優越的電器特性。

為讓本發明之上述和其他目的、特徵、和優點能更明



五、發明說明 (5)

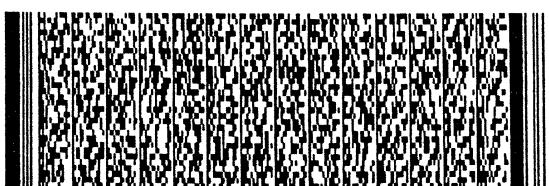
顯易懂，下文特舉一較佳實施例，並配合所附圖式，作詳細說明如下：

實施方式

第3圖繪示為依照本發明第一較佳實施例場效電晶體之結構示意圖。請參照第3圖，本實施例之場效電晶體結構主要係由氮化鎵基材200、氮化鎵基礎半導體層202、氮化鎵基礎閘極絕緣層210、源極204、汲極206以及閘極208所構成。其中，氮化鎵基礎半導體層202係位於氮化鎵基材200上，其材質例如為 $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ ，其中 $a \geq 0$ ， $b \geq 0$ ， $1 \geq a+b$ 。氮化鎵基礎閘極絕緣層210係配置於氮化鎵基礎半導體層202上，且氮化鎵基礎閘極絕緣層210之材質 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ ，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ， $x > a$ 。此外，閘極208則配置於氮化鎵基礎閘極絕緣層210上，而源極204與汲極206係位於閘極208兩側之氮化鎵基礎半導體層202上。

本實施例中，氮化鎵基礎閘極絕緣層210中例如具有一摻質，以增進氮化鎵基礎閘極絕緣層210的電阻值，且此摻質例如為碳、鎂、鐵等金屬或是這些材質之組合，而這些摻質（碳、鐵及鎂等金屬）例如係於磊晶過程中進行摻雜。此外，上述之氮化鎵基礎閘極絕緣層210的電阻值例如係介於 10^9 至 10^{12} 歐姆/ $\square$ 之間。

本實施例中，由於氮化鎵基礎閘極絕緣層210係配置於氮化鎵基礎半導體層202上，二者為相似之材料，故晶格匹配特性十分良好。換言之，氮化鎵基礎閘極絕緣層



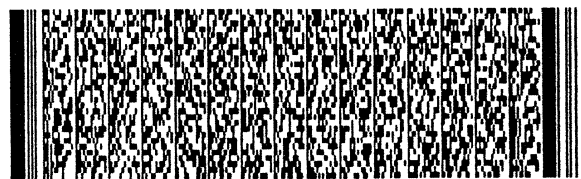
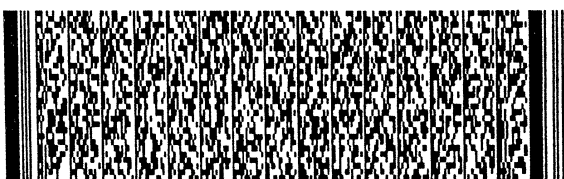
五、發明說明 (6)

210 與氮化鎵基礎半導體層202之間的介面特性良好，所以不會因二者之間的材料特性差異太大而導致元件特性低落。此外，本實施例之氮化鎵基礎閘極絕緣層210在製作上例如係採用低溫製程，氮化鎵基礎閘極絕緣層210可於低溫狀態（攝氏300至900度）生成，且毋需再經由磊晶後之高溫熱處理(post annealing)製程即可獲得絕佳的絕緣效果。

由上述可知，氮化鎵基礎閘極絕緣層210在低溫磊晶成長之後便具有良好的絕緣特性，在製作上相當簡單，且氮化鎵基礎閘極絕緣層210的高電阻特性將使得場效電晶體具有耐溫與高功率之操作特性。

上述之氮化鎵基礎閘極絕緣層210在製作上雖以低溫磊晶製程為例進行說明，但並非限定本發明必須採用低溫磊晶製程才能夠達成，本發明亦可於其他溫度狀態下進行氮化鎵基礎閘極絕緣層210的磊晶成長，以直接生成具有良好絕緣特性之氮化鎵基礎閘極絕緣層210。

第4圖繪示為第1圖與第3圖之場效電晶體中，反向偏(reverse bias)壓與閘極漏電流之間的關係圖。請參照第4圖，曲線A為習知不具閘極絕緣層之氮化鎵場效電晶體，其反向偏(reverse bias)壓(reverse voltage)與閘極漏電流之間的關係，而曲線B則為本實施例中具有高阻值之氮化鎵基礎閘極絕緣層之氮化鎵場效電晶體，其反向偏壓與閘極漏電流之間的關係。由第4圖可清楚得知，習知之氮化鎵場效電晶體的閘極漏電流與本實施例之氮化鎵場效



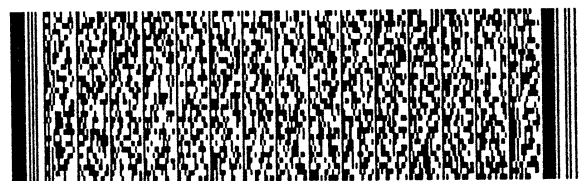
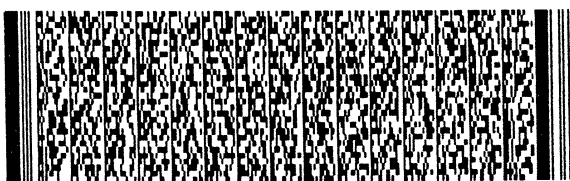
五、發明說明 (7)

電晶體的閘極漏電流相較，二者之間的閘極漏電流差值超過1000倍。以習知製作場效電晶體之經驗可以預測，如此優異之絕緣特性必然可以滿足元件高溫與高功率操作之需求。

本發明之氮化鎵基礎閘極絕緣層除了應用於第3圖所繪示的結構之外，亦可應用於其他應用氮化鎵基礎磊晶材料層的元件上，例如調製摻雜場效電晶體(MODFET)或其他架構之高電子移動率電晶體(High Electron Mobility Transistor, HEMT)等元件，以下僅針對調製摻雜場效電晶體(MODFET)的應用層面進行說明。

第5圖繪示為依照本發明第二較佳實施例場效電晶體之結構示意圖。請參照第5圖，調製摻雜場效電晶體(MODFET)主要係由氮化鎵基材300、氮化鎵基礎半導體層302、氮化鎵基礎閘極絕緣層318、源極312、汲極314以及閘極316所構成。其中，氮化鎵基礎半導體層302係位於氮化鎵基材300上。氮化鎵基礎閘極絕緣層318係配置於氮化鎵基礎半導體層302上，且氮化鎵基礎閘極絕緣層318之材質 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ ，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ， $x > a$ 。此外，閘極316則配置於氮化鎵基礎閘極絕緣層318上，而源極312與汲極314係位於閘極316兩側之氮化鎵基礎半導體層302上。

同樣請參照第5圖，在調製摻雜場效電晶體的架構中，氮化鎵基礎半導體層302例如是由緩衝層304、通道層306、間隙層308以及阻障層310所構成。其中，緩衝層304



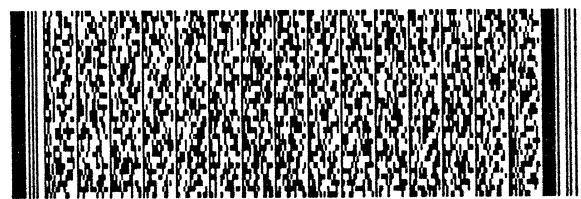
五、發明說明 (8)

與通道層306例如為一未摻雜之 $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ 層，且 $a \geq 0$ ， $b \geq 0$ ， $1 \geq a+b$ ， $x > a$ ；間隙層308例如為一未摻雜之 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；而阻障層310例如為一矽摻雜的 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ 。

與前一實施例相似，本實施例之氮化鎵基礎閘極絕緣層318中亦可具有一摻質，以增進氮化鎵基礎閘極絕緣層318的電阻值（約為 10^9 至 10^{12} 歐姆/ $\square$ 之間），此摻質例如為碳、鎂、鐵等金屬或是這些材質之組合，而這些摻質（碳、鐵及鎂等金屬）例如係於磊晶過程中進行摻雜。

第6圖繪示為依照本發明第三較佳實施例場效電晶體之結構示意圖。請同時參照第5圖第6圖，本實施例與第5圖相似，惟其差異之處在於本實施例在緩衝層304與通道層306之間配置有一隔絕層305，而此隔絕層305之材質例如與閘極絕緣層318同為 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ ，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ 。

上述所揭露之場效電晶體元件架構，主要在於加強元件本身的閘極崩潰特性，進而達到高功率操作之目的。另外，吾人更可利用上述之氮化鎵基礎絕緣層(GaN-based insulating layer)作為半導體磊晶層與基材間的絕緣緩衝層，這將可有效地消除邊閘極效應(side-gating effect)或背閘極效應(back-gating effect)，且實質地降低輸出電導(output conductance)，進而更有利於高頻操作。



五、發明說明 (9)

雖然本發明已以多個較佳實施例揭露如上，然其並非用以限定本發明，任何熟習此技藝者，在不脫離本發明之精神和範圍內，當可作些許之更動與潤飾，因此本發明之保護範圍當視後附之申請專利範圍所界定者為準。



圖式簡單說明

第1圖繪示為習知採用氮化鎵基材之場效電晶體的結構示意圖；

第2圖繪示為習知高功率操作之場效電晶體的結構示意圖；

第3圖繪示為依照本發明第一較佳實施例場效電晶體之結構示意圖；

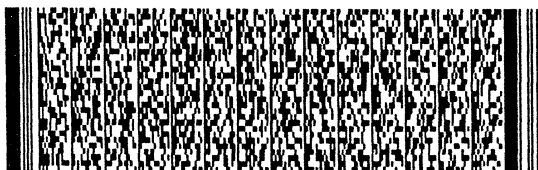
第4圖繪示為第1圖與第3圖之場效電晶體中，反向偏壓與閘極漏電流之間的關係圖；

第5圖繪示為依照本發明第二較佳實施例場效電晶體之結構示意圖；以及

第6圖繪示為依照本發明第三較佳實施例場效電晶體之結構示意圖。

圖式標示說明

- 100：氮化鎵基材
- 102：氮化鎵基礎半導體層
- 104：源極
- 106：汲極
- 108：閘極
- 110：閘極絕緣層
- 200：氮化鎵基材
- 202：氮化鎵基礎半導體層
- 204：源極
- 206：汲極



圖式簡單說明

- 208 : 閘極
- 210 : 氮化鎵基礎閘極絕緣層
- 300 : 氮化鎵基材
- 302 : 氮化鎵基礎半導體層
- 304 : 緩衝層
- 305 : 隔絕層
- 306 : 通道層
- 308 : 間隙層
- 310 : 阻障層
- 312 : 源極
- 314 : 汲極
- 316 : 閘極
- 318 : 氮化鎵基礎閘極絕緣層



四、中文發明摘要 (發明名稱：場效電晶體結構及其製程)

一種場效電晶體結構，主要係由氮化鎵基材、氮化鎵基礎(GaN-based)半導體層、氮化鎵基礎閘極絕緣層、源極/汲極以及閘極所構成。其中，氮化鎵基礎半導體層係位於氮化鎵基材上；氮化鎵基礎(GaN-based)閘極絕緣層係配置於氮化鎵基礎半導體層上，且氮化鎵基礎閘極絕緣層為 $-Al_xIn_yGa_{1-x-y}N$ 層，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；源極/汲極係配置於氮化鎵基礎半導體層上，且位於氮化鎵基礎閘極絕緣層旁；而閘極則配置於氮化鎵基礎閘極絕緣層上。上述之氮化鎵基礎(GaN-based)閘極絕緣層在製作上不需經過磊晶後的高溫熱處理，製程更形簡單，且使得場效電晶體能夠達到高耐溫與高功率操作的目的。

伍、(一)、本案代表圖為：第____6____圖

(二)、本案代表圖之元件代表符號簡單說明：

300：氮化鎵基材 302：氮化鎵基礎半導體層

陸、英文發明摘要 (發明名稱：Field effect transistor and method of fabricating the same)

A field effect transistor comprising a GaN-based substrate, a GaN-based semiconductor layer, a GaN-based gate insulating layer, a source/drain and a gate is provided. The GaN-based semiconductor layer is disposed on the GaN-based substrate; the GaN-based gate insulating layer is disposed on the GaN-based semiconductor layer, and the material of the GaN-based gate insulating

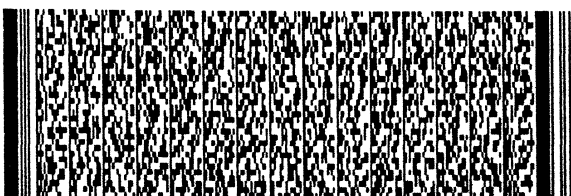


四、中文發明摘要 (發明名稱：場效電晶體結構及其製程)

304：緩衝層 305：隔絕層(blocking layer)
 306：通道層 308：間隙層(spacer) 310：阻障層
 (barrier layer) 312：源極 314：汲極 316：
 閘極 318：氮化鎵基礎閘極絕緣層

陸、英文發明摘要 (發明名稱：Field effect transistor and method of fabricating the same)

layer is $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$, wherein $x \geq 0$, $y \geq 0$, $1 \geq x+y$; the source/drain is disposed on the GaN-based semiconductor layer and adjacent to the GaN-based gate insulating layer; and the gate is disposed on the GaN-based gate insulating layer. The process to fabricating the GaN-based gate insulating layer is simple and easy because a high temperature thermal treatment is abbreviated. In addition, in



四、中文發明摘要 (發明名稱：場效電晶體結構及其製程)

陸、英文發明摘要 (發明名稱：Field effect transistor and method of fabricating the same)

the condition of high temperature and high power operating the FET will still work.



六、申請專利範圍

1. 一種場效電晶體結構，包括：

一氮化鎵基材；

一氮化鎵基礎半導體層，位於該氮化鎵基材上；

一氮化鎵基礎閘極絕緣層，配置於該氮化鎵基礎半導體層上，且該氮化鎵基礎閘極絕緣層為一 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；

一源極/汲極，配置於該氮化鎵基礎半導體層上，且位於該氮化鎵基礎閘極絕緣層旁；以及

一閘極，配置於該氮化鎵基礎閘極絕緣層上。

2. 如申請專利範圍第1項所述之場效電晶體結構，其中該氮化鎵基礎半導體層為一 $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ 層，其中 $a \geq 0$ ， $b \geq 0$ ， $1 \geq a+b$ 。

3. 如申請專利範圍第1項所述之場效電晶體結構，其中該氮化鎵基礎半導體層包括：

一緩衝層，位於該氮化鎵基材上；

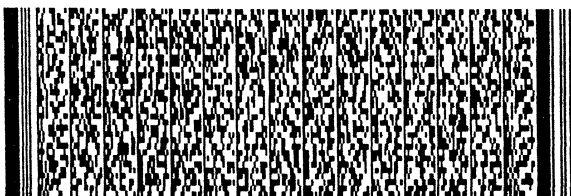
一通道層，位於該緩衝層上；

一間隙層，位於該通道層上；以及

一阻障層，位於該間隙層上以及該氮化鎵基礎閘極絕緣層、該源極/汲極之間。

4. 如申請專利範圍第3項所述之場效電晶體結構，其中該緩衝層與該通道層為一未摻雜之 $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ 層，且 $a \geq 0$ ， $b \geq 0$ ， $1 \geq a+b$ ， $x > a$ 。

5. 如申請專利範圍第3項所述之場效電晶體結構，其中該間隙層為一未摻雜之 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， y



六、申請專利範圍

≥ 0 , $1 \geq x+y$ 。

6. 如申請專利範圍第3項所述之場效電晶體結構，其中該阻障層為一矽摻雜的 $Al_xIn_yGa_{1-x-y}N$ 層，且 $x \geq 0$, $y \geq 0$, $1 \geq x+y$ 。

7. 如申請專利範圍第1項所述之場效電晶體結構，其中該氮化鎵基礎半導體層包括：

一緩衝層，位於該氮化鎵基材上；

一隔絕層，位於該緩衝層上；

一通道層，位於該隔絕層上；

一間隙層，位於該通道層上；以及

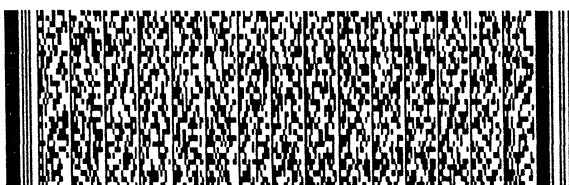
一阻障層，位於該間隙層上以及該氮化鎵基礎閘極絕緣層、該源極/汲極之間。

8. 如申請專利範圍第7項所述之場效電晶體結構，其中該緩衝層與該通道層為一未摻雜之 $Al_aIn_bGa_{1-a-b}N$ 層，且 $a \geq 0$, $b \geq 0$, $1 \geq a+b$, $x > a$ 。

9. 如申請專利範圍第7項所述之場效電晶體結構，其中該隔絕層為一 $Al_xIn_yGa_{1-x-y}N$ 層，其中 $x \geq 0$, $y \geq 0$, $1 \geq x+y$ 。

10. 如申請專利範圍第7項所述之場效電晶體結構，其中該間隙層為一未摻雜之 $Al_xIn_yGa_{1-x-y}N$ 層，且 $x \geq 0$, $y \geq 0$, $1 \geq x+y$ 。

11. 如申請專利範圍第7項所述之場效電晶體結構，其中該阻障層為一矽摻雜的 $Al_xIn_yGa_{1-x-y}N$ 層，且 $x \geq 0$, $y \geq 0$, $1 \geq x+y$ 。



六、申請專利範圍

12. 如申請專利範圍第1項所述之場效電晶體結構，其中該氮化鎵基礎閘極絕緣層中具有一摻質，且該摻質包括碳、鎂、鐵及該等組合其中之一。

13. 一種場效電晶體結構，包括：

一氮化鎵基材；

一緩衝層，位於該氮化鎵基材上；

一通道層，位於該緩衝層上，其中該緩衝層與該通道層為一未摻雜之 $\text{Al}_a\text{In}_b\text{Ga}_{1-a-b}\text{N}$ 層，且 $a \geq 0$ ， $b \geq 0$ ， $1 \geq a+b$ ；

一間隙層，位於該通道層上，其中該間隙層為一未摻雜之 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；以及

一阻障層，位於該間隙層上，其中該阻障層為一摻雜的 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，且 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；

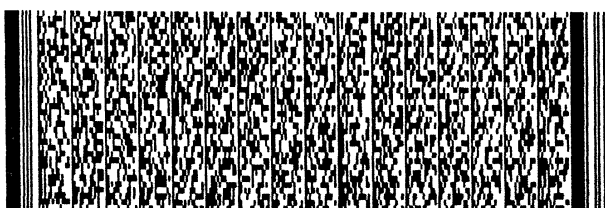
一氮化鎵基礎閘極絕緣層，配置於該氮化鎵基礎半導體層上，且該氮化鎵基礎閘極絕緣層為一 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ， $x > a$ ；

一源極/汲極，配置於該氮化鎵基礎半導體層上，且位於該氮化鎵基礎閘極絕緣層旁；以及

一閘極，配置於該氮化鎵基礎閘極絕緣層上。

14. 如申請專利範圍第13項所述之場效電晶體結構，更包括一隔絕層，該隔絕層配置於該緩衝層與該通道層之間。

15. 如申請專利範圍第14項所述之場效電晶體結構，其中該隔絕層為一 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，其中 $x \geq 0$ ， $y \geq 0$ ，



六、申請專利範圍

$$1 \geq x+y。$$

16. 如申請專利範圍第13項所述之場效電晶體結構，其中該氮化鎵基礎閘極絕緣層中具有一摻質，且該摻質包括碳、鎂、鐵及該等組合其中之一。

17. 一種場效電晶體製程，包括下列步驟：

於一氮化鎵基材上形成一氮化鎵基礎半導體層；

於該氮化鎵基礎半導體層上形成一氮化鎵基礎閘極絕緣層，其中該氮化鎵基礎閘極絕緣層為一 $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ 層，其中 $x \geq 0$ ， $y \geq 0$ ， $1 \geq x+y$ ；

於該氮化鎵基礎閘極絕緣層旁之該氮化鎵基礎半導體層上形成一源極/汲極；以及

於該氮化鎵基礎閘極絕緣層上形成一閘極。

18. 如申請專利範圍第17項所述之場效電晶體製程，其中該氮化鎵基礎半導體層的形成包括：

於該氮化鎵基材上形成一緩衝層；

於該緩衝層上形成一通道層；

於該通道層上形成一間隙層；以及

於該間隙層上以及該氮化鎵基礎閘極絕緣層、該源極/汲極之間形成一阻障層。

19. 如申請專利範圍第18項所述之場效電晶體製程，更包括形成一隔絕層於該緩衝層與該通道層之間。

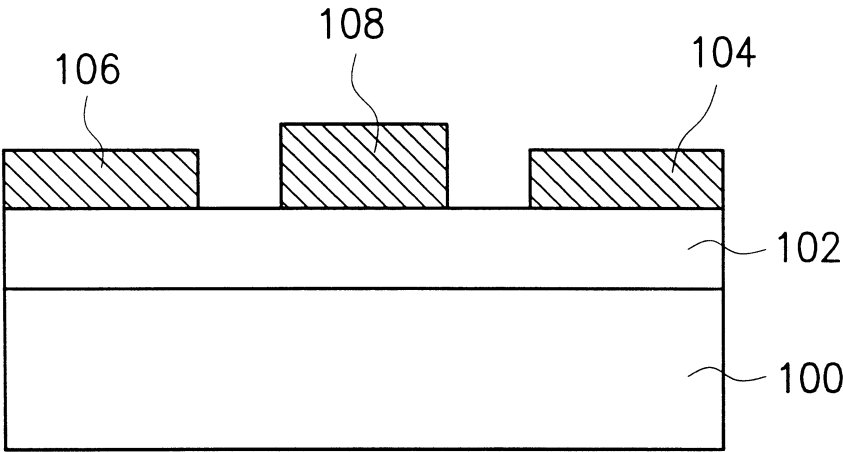
20. 如申請專利範圍第19項所述之場效電晶體製程，其中該氮化鎵基礎閘極絕緣層與該隔絕層之形成方法包括低溫成長法，而該低溫成長法的製程溫度係介於攝氏300



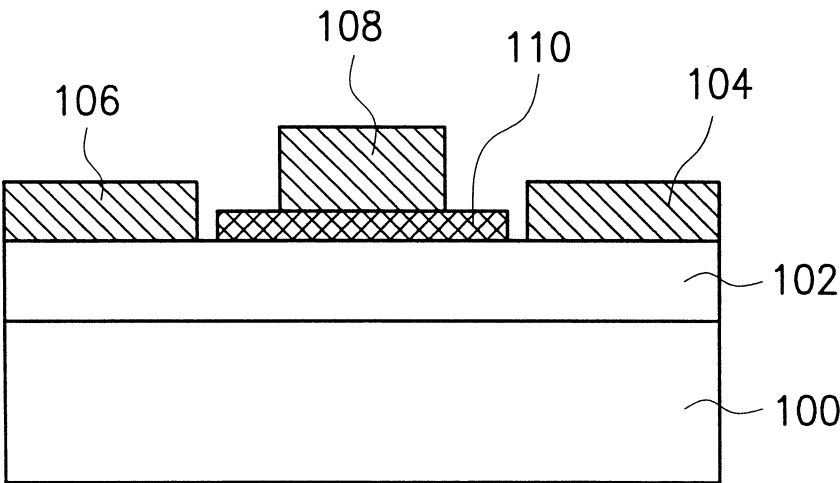
六、申請專利範圍
至900 度。



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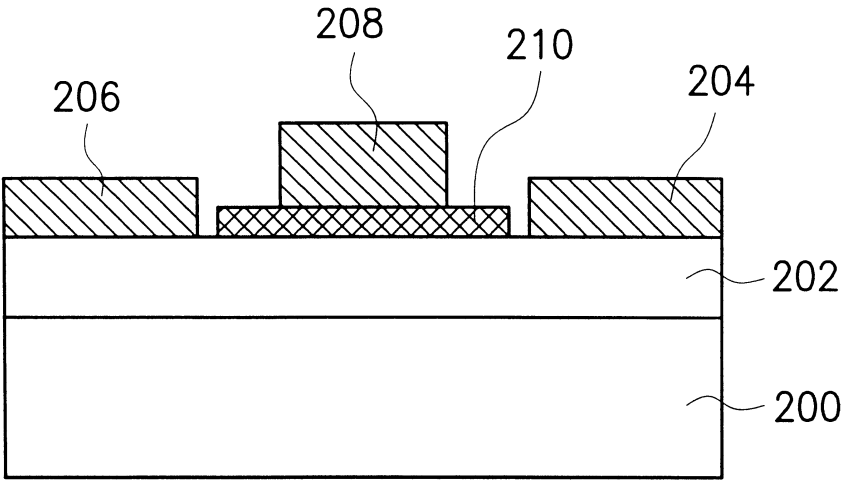


第 1 圖

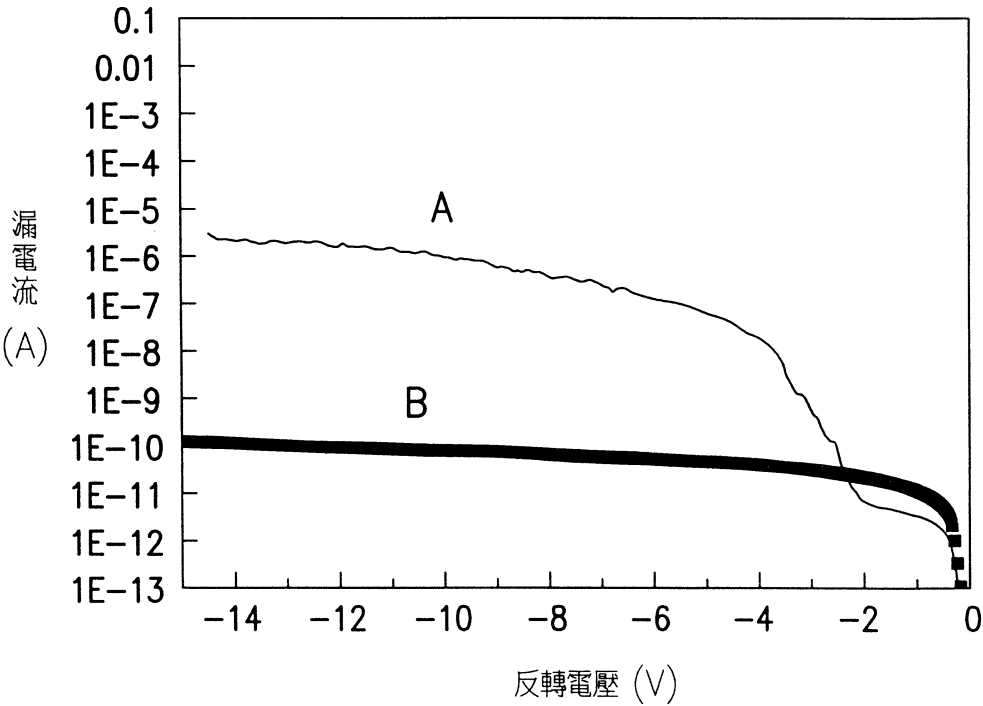


第 2 圖

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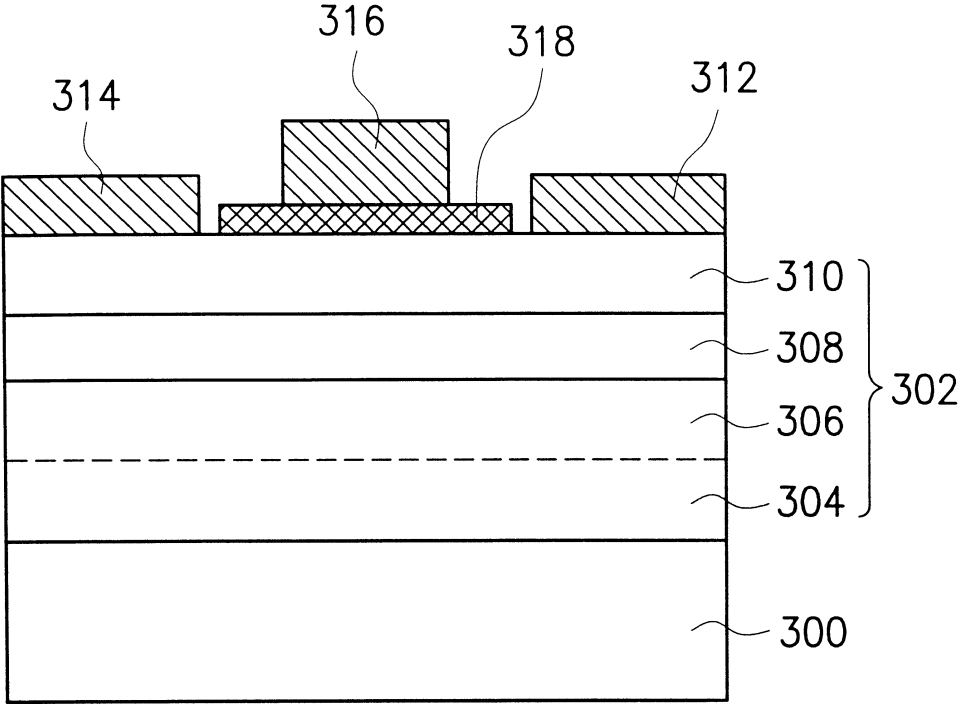


第 3 圖

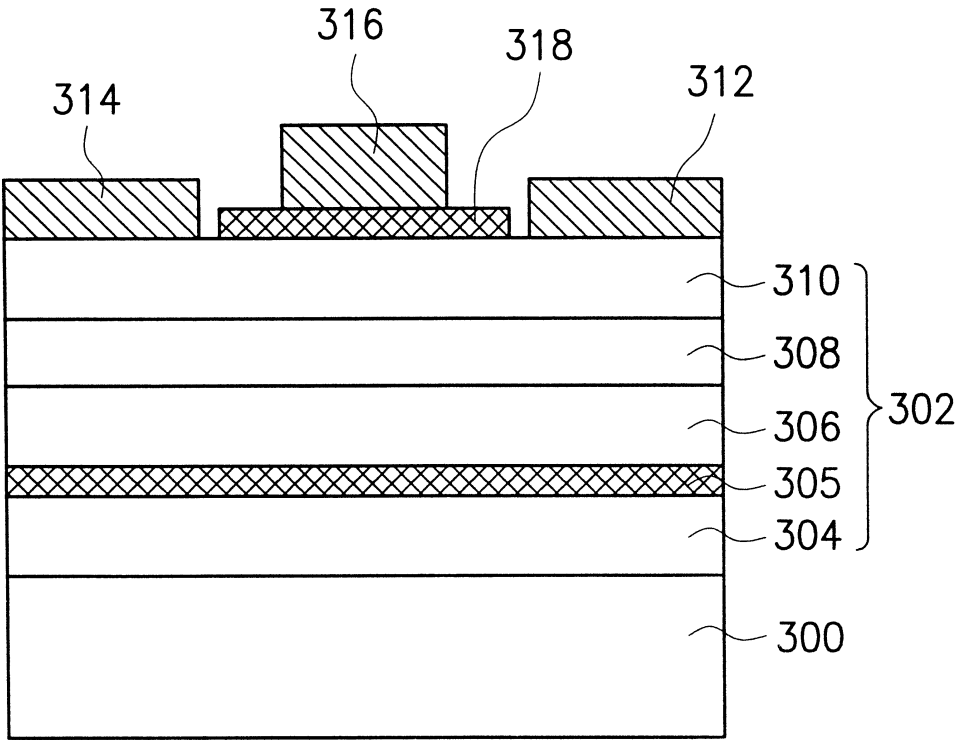


第 4 圖

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第 5 圖

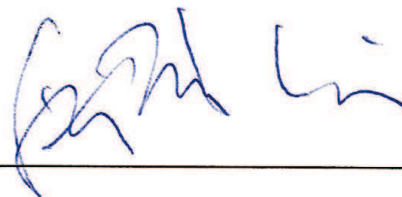


第 6 圖

I, Xin Min Liu, declare as follows:

1. I am over 21 years of age and competent to make this declaration.
2. I am a native speaker of Chinese.
3. I am fluent in English.
4. I have over 30 years of experience translating Chinese into English.
5. I have translated the attached patent document “TW200414540A” from Chinese into English.
6. I certify that the translation of the document “TW200414540A” is, to the best of my knowledge, a true and accurate translation from Chinese to English.
7. In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.
8. I declare under penalty of perjury that all statements made herein are true and accurate to the best of my knowledge and belief, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: _____



July 19, 2023