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Field-Plated 0.25- μm Gate-Length AlGaIn/GaN HEMTs With Varying Field-Plate Length

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Abstract—Metal–organic chemical vapor deposition-grown field-plated 0.25- μm gate-length AlGaIn/GaN high-electron mobility transistors (HEMTs) with field-plate lengths of 0.5, 0.8, and 1.1 μm have been fabricated on 6H-SiC substrates. These 0.25- μm gate-length devices exhibited maximum drain current density of more than 1.4 A/mm and peak extrinsic transconductance of 437 mS/mm. No dependence of dc I – V as well as transfer characteristics on field-plate length was observed. With increase of field-plate length, degradation in the value of unity current gain frequency f_T and maximum frequency of oscillation f_{max} was observed, but there is significant improvement in breakdown voltage and power densities. Also, at 18 GHz, a continuous-wave output power density of 9.1 W/mm with power added efficiency of 23.7% was obtained for device with field-plate length of 1.1 μm , yielding the highest reported power performance of AlGaIn/GaN HEMTs at 18 GHz.

Index Terms—AlGaIn/GaN high-electron mobility transistors (HEMTs), field plate, transconductance.

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I. INTRODUCTION

AlGaIn/GaN high-electron mobility transistors (HEMTs) are excellent candidates for high-power and high-frequency applications at room temperature as well as elevated temperatures due to their superior material properties [1]–[5]. As a result of improved material growth and processing technologies, microwave power densities have been demonstrated in GaN HEMTs that are five to ten times greater than that of corresponding GaAs-based devices. These higher power densities will result in simplifying the design and fabrication of monolithic microwave integrated circuits (MMICs). Although GaN HEMTs using field plates have demonstrated power densities as high as 32 W/mm at 4 GHz, yet to date, there have been only few reports of these devices up to and beyond X band [6]–[12]. In this brief, we present the effect of field-plate length on 0.25- μm gate-length devices. A record power performance of AlGaIn/GaN HEMTs on 6H-SiC substrates at 18 GHz is presented. A continuous-wave (CW) output power density of 9.1 W/mm with a gain of 5.8 dB and power added efficiency (PAE) of 23.7% was achieved.

II. DEVICE REALIZATION

The AlGaIn HEMT structure used in the present study was grown on 6H-SiC substrates by metal–organic chemical vapor deposition (MOCVD). The epilayer consists of an AlN buffer, a 1.5- μm undoped GaN, and a 20-nm $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}$ barrier layer. Average sheet resistance across the as-grown wafer was 380 Ω/sq as measured by Leighton measurements. Device fabrication started with mesa isolation using Cl_2/Ar plasma in an inductively coupled plasma-reactive ion etch (ICP-RIE) system. The mesa height is typically about 120 nm. Next, ohmic contacts were formed by rapid thermal annealing of evaporated Ti/Al/Mo/Au (15 nm/60 nm/35 nm/50 nm) at 850 $^\circ\text{C}$ for 30 s in N_2 ambient. A pretreatment of the ohmic contact area using SiCl_4 plasma in an RIE system was performed prior to Ti/Al/Mo/Au metalization [13]. Using on-wafer transfer length measurement (TLM) patterns, the ohmic contact resistance was measured to be $\sim 0.15 \Omega \cdot \text{mm}$. The source–drain spacing for these devices was 2.7 μm . Next, silicon nitride was deposited at a substrate temperature of 300 $^\circ\text{C}$ using silane and ammonia precursors in a plasma-enhanced chemical vapor deposition (PECVD) system. Then, 0.25- μm gate footprints were patterned using e-beam lithography and etched through the silicon nitride film using CHF_3 plasma in an RIE system. The distance between the edge of the gate footprint and source contact was 0.8 μm . Finally, Ni/Au (300/2500 Å) gamma gates with different side-lobe lengths on the drain side were deposited by e-beam evaporation. Three field-plate lengths L_{FP} were designed: 0.5, 0.8, and 1.1 μm . The devices had a total gate width of 100 μm . The schematic of the device structure is shown in Fig. 1.

III. RESULTS AND DISCUSSIONS

On-wafer dc measurements were performed using an HP4145B semiconductor parameter analyzer. Fig. 2 shows typical drain current–voltage (I_D – V_{DS}) characteristics for 0.25- μm gate-length devices with field-plate lengths of 0.5 and 1.1 μm . The gates were biased from -5 to 2 V in a step of 1 V. The maximum current densities $I_{D,\text{max}}$ for both devices were nearly identical at just more than 1.4 A/mm at a gate bias of 2 V and a drain bias of 10 V. For both devices, the saturation current I_{dss} was ~ 1.05 A/mm. The devices pinched-off completely at $V_{\text{gs}} = -5$ V. The knee voltage is less than 4.0 V, showing the excellent nature of the ohmic contacts. The dc transfer

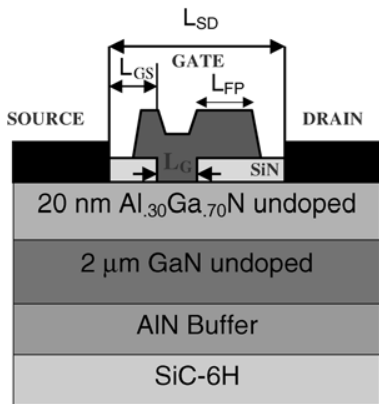


Fig. 1. Schematic of field-plated AlGaIn/GaN HEMT structure.

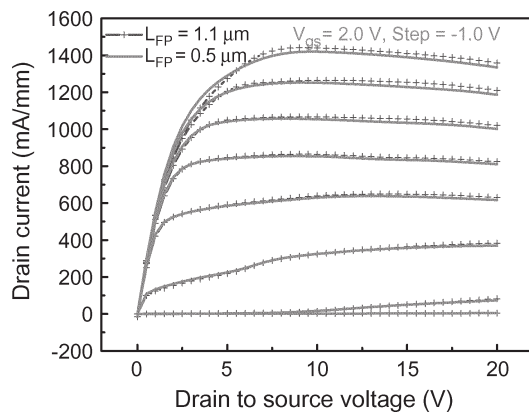


Fig. 2. Drain current-voltage (I_D - V_{DS}) characteristics of a $0.25 \mu\text{m} \times 100 \mu\text{m}$ AlGaIn/GaN HEMT with $L_{FP} = 0.5$ and $1.1 \mu\text{m}$. The gate bias was swept from -5 to 2 V in a step of 1 V.

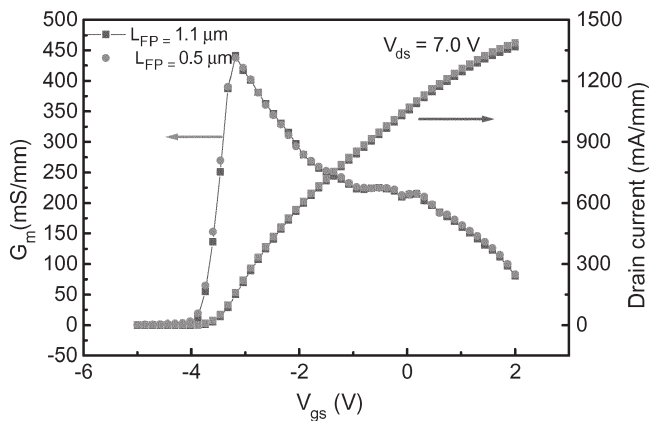


Fig. 3. Transfer characteristics of the $0.25 \mu\text{m} \times 100 \mu\text{m}$ AlGaIn/GaN HEMT with $L_{FP} = 0.5$ and $1.1 \mu\text{m}$. The drain bias was 7.0 V.

characteristics at a drain voltage of 8 V are shown in Fig. 3. A peak extrinsic transconductance g_m of 437 mS/mm was measured at $V_{gs} = -3.4$ V. The high value of g_m is attributed to the thin AlGaIn barrier layer and the low contact resistance. By defining the threshold voltage V_{th} as the gate bias intercept of the extrapolation of drain current at the point of peak g_m , V_{th} was determined to be -4.0 V. These results show that the dc I - V as well as transfer characteristics

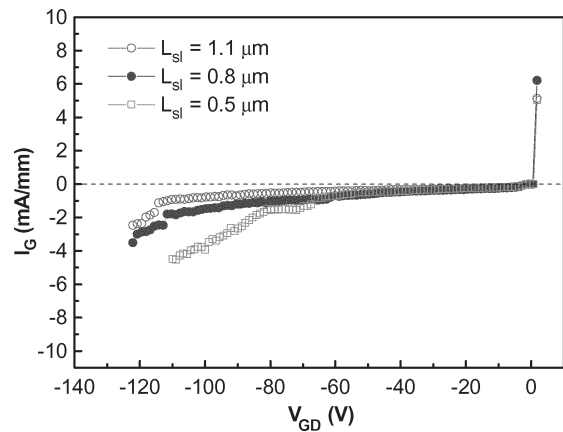


Fig. 4. Gate-drain diode characteristic of the field-plated AlGaIn/GaN HEMT with varying field-plate length.

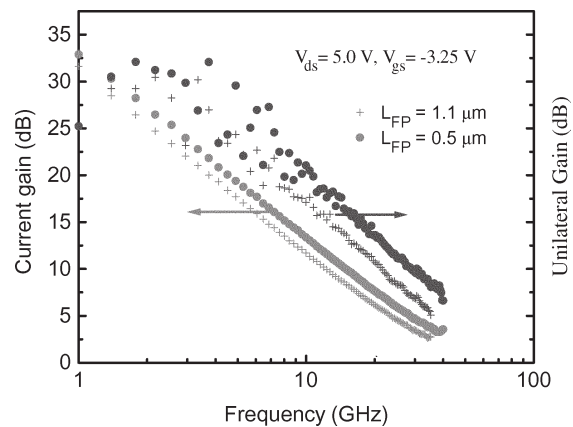


Fig. 5. Short-circuit current gain $|h_{21}|$ and unilateral power gain of a $0.25 \mu\text{m} \times 100 \mu\text{m}$ AlGaIn/GaN HEMT with $L_{FP} = 0.5$ and $1.1 \mu\text{m}$. The device was biased at $V_{ds} = 5$ V and $V_{gs} = -3.25$ V.

are practically independent on the length of field plate. Also, these results are in agreement with previously reported results on 1 - μm gate-length field-plated AlGaIn/GaN HEMTs [7]. The effect of field-plate length on the gate-to-drain diode I - V characteristics is shown in Fig. 4. The off-state gate-to-drain breakdown voltage measured at a gate current density of 1 mA/mm increased from 68 to 110 V as the field-plate length increased from 0.5 to $1.1 \mu\text{m}$. This improvement in breakdown voltage is due to the depletion layer formed under the field-plate electrode resulting in the reduction of the electric field strength at the gate edge toward drain.

On-wafer radio frequency (RF) measurements were carried out using a Cascade Microtech Probe and an HP8510B network analyzer in the 1 – 40 GHz range. Fig. 5 shows the short-circuit current gain $|h_{21}|$ and Mason's unilateral power gain U_G derived from on-wafer S -parameter measurements as a function of frequency for the devices with field-plate length of 0.5 and $1.1 \mu\text{m}$. The values of unity current gain cutoff frequency f_T and maximum frequency of oscillation f_{max} were determined by extrapolation of the $|h_{21}|$ and U_G data at -20 dB/dec, respectively. With the increase of field-plate length from 0.5 to $1.1 \mu\text{m}$, the value of f_T decreased from 50 to 41 GHz, whereas the value of f_{max} decreased from 81 to 63 GHz. This is attributed to an increase in the additional feedback capacitance. The devices were biased at a drain bias of 5 V and a gate bias

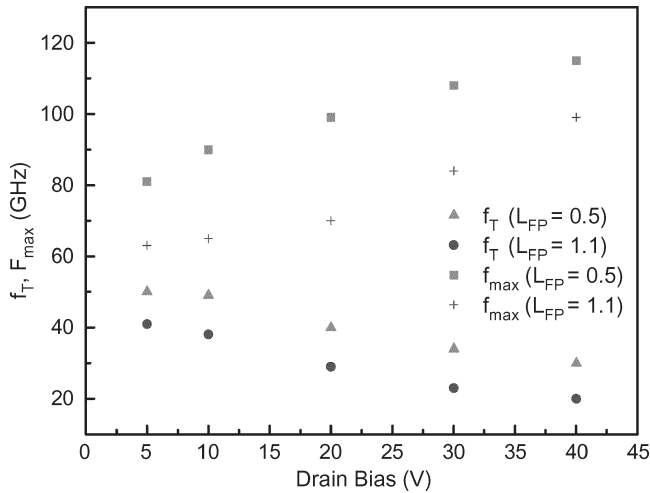


Fig. 6. Variation of f_T and $f_{\max}$ as a function of drain bias of a $0.25 \mu\text{m} \times 100 \mu\text{m}$ AlGaIn/GaN HEMT with $L_{\text{FP}} = 0.5$ and $1.1 \mu\text{m}$.

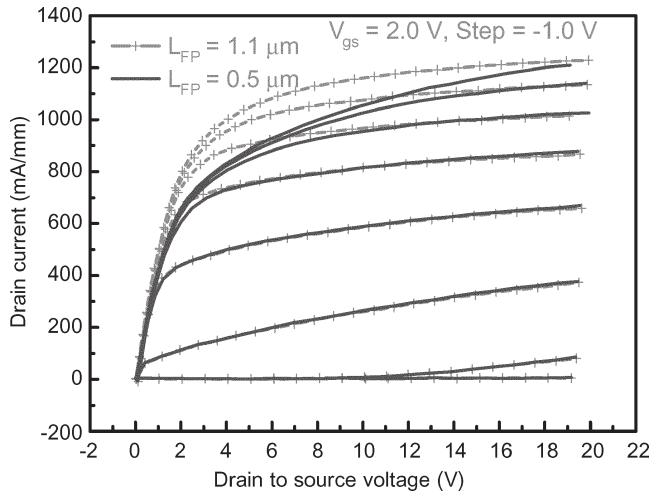


Fig. 7. Pulsed I - V characteristics of the $0.25 \mu\text{m} \times 100 \mu\text{m}$ AlGaIn/GaN HEMT with $L_{\text{FP}} = 0.5$ and $1.1 \mu\text{m}$

of -3.25 V to achieve the peak value of f_T . The variation of f_T and $f_{\max}$ with drain bias is shown in Fig. 6. With the increase in drain bias, there is decrease in the value of f_T , whereas the value of $f_{\max}$ increases. This enhancement in the value of $f_{\max}$ is due to the decrease of gate-drain capacitance induced by the increase of the gate-drain depletion region width. Pulsed current-voltage (I - V) measurements were performed using OptoAccent's Diva D265 to characterize the dc-to-RF dispersion in HEMTs. The dynamic (pulsed I - V) characteristics are measured by pulsing both the drain-source voltage and gate-source voltage synchronously away from the bias point (which was $V_{\text{gs}} = -5 \text{ V}$ and $V_{\text{ds}} = 20 \text{ V}$) to the point where the current is measured. The reason for this bias point was to consider drain lag effect. For these measurements, pulse width and duty cycle were 200 ns and 0.04% , respectively. The results of these measurements are shown in Fig. 7. There is significant improvement in the pulsed I - V characteristics as the length of the field plate increased. This improvement in dispersion is attributed to the mitigation of the electric field at the gate edge resulting in lower electron injection into surface traps and/or better modulation of the surface traps in

TABLE I
SUMMARY OF THE RESULTS OF THE FIELD-PLATED AlGaIn/GaN HEMTs
WITH VARYING FIELD-PLATE LENGTH

$L_{\text{FP}}(\mu\text{m})$	$G_{\text{m,ext}}$ (mS/mm)	I_{Dmax} (mA/mm)	f_T (GHz)	$f_{\max}$ (GHz)	BV_{GD} (V)	Power (W/mm) @ 18 GHz
0.5	437	1.42	50	81	68	5.4
0.8	435	1.42	44	74	78	6.4
1.1	437	1.44	41	63	110	7.3

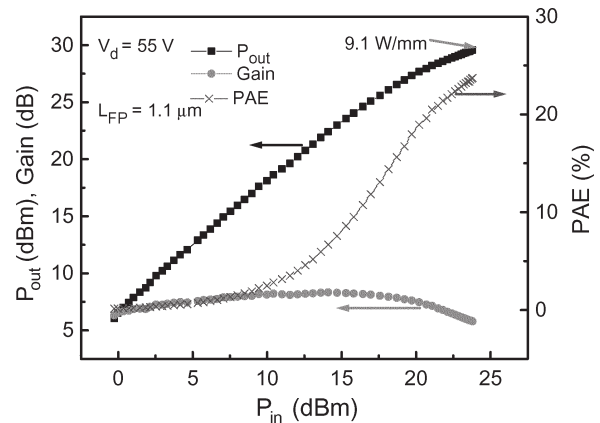


Fig. 8. Large-signal performance of the $0.25 \mu\text{m} \times 100 \mu\text{m}$ with $L_{\text{FP}} = 1.1 \mu\text{m}$ at 18 GHz . The device was biased with $V_{\text{ds}} = 55 \text{ V}$ and $V_{\text{gs}} = -2.9 \text{ V}$.

the gate-drain access region [11]. Large-signal CW measurements at 18 GHz were performed using a Focus Microwave automatic load pull system. The data were taken on-wafer at room temperature without any thermal management. The improvement observed in the pulsed I - V characteristics with increase of L_{FP} was reflected in the power performance of the devices. At a drain bias of 40 V , power densities of 5.4 , 6.4 , and 7.3 W/mm were measured for devices with L_{FP} of 0.5 , 0.8 , and $1.1 \mu\text{m}$, respectively. These results are summarized in Table I. The large-signal performance of the device with L_{FP} of $1.1 \mu\text{m}$ at a drain bias of 55 V is shown in Fig. 8. The device has an output power of 29.57 dBm , corresponding to 9.1 W/mm , with an associated gain of 5.8 dB and PAE of 23.7% . The expected linear power can be deduced from the pulsed I - V characteristics and is given by $P = I_{\text{max}} \times 2 \times (V_{\text{bias}} - V_{\text{knee}})/8$. At a drain bias of 55 V , the expected linear power is 15.4 W/mm , corresponding to saturated power of 24.6 W/mm . The lower value of the measured power and PAE is believed to be the result of the imperfect load match. The load impedance was $Z_l = 108.31 + j156.03$, corresponding to a shunt resistance of 331.1Ω . Utilizing the pulsed I - V characteristics and load-line impedance, the maximum linear power is estimated to be 27.96 dBm , corresponding to 6.26 W/mm . The saturated power density was then estimated to be about 10 W/mm . This value is in close agreement with the measured power performance of the device. To the best of the authors' knowledge, 9.1 W/mm is the highest power density reported at 18 GHz for GaN-based HEMTs. These results demonstrate the exceptional potential of these devices for high-power applications beyond X band. It is worth mentioning that these devices did not degrade while performing power sweeps even at a drain bias of 55 V . Also, further improvements in gain can be achieved by making recessed and shorter gate-length devices.

IV. SUMMARY

In summary, we have presented the results on the performance of 0.25- μm gate-length AlGaIn/GaN HEMTs with varying field-plate length. These devices exhibited high current densities of more than 1.4 A/mm and peak extrinsic transconductances of more than 430 mS/mm. DC I - V as well as transfer characteristics were essentially independent of the length of the field plate, but there was significant improvement in breakdown voltage as the length of the field plate increased. With increase in field-plate length, degradation in the values of f_T and f_{max} was observed, but there was significant improvement in power densities. Also, at 18 GHz, a CW output power density of 9.1 W/mm with PAE of 23.7% was obtained for device with a field-plate length of 1.1 μm , yielding the highest reported power performance of AlGaIn/GaN HEMTs at 18 GHz.

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A Novel Voltage-Mode CMOS Quaternary Logic Design

Ricardo Cunha G. da Silva, Henri Boudinov, and Luigi Carro

Abstract—This brief presents a novel kind of voltage-mode CMOS design that uses multiple threshold voltage transistors and three power supply lines to implement quaternary logic gates, showing lower power dissipation and using less area than the present voltage-mode quaternary circuits. Inverter, NMN, and NMAX gates are simulated with the Spice tool using TSMC 0.18- μm technology. The proposed logic circuits overcome the limitations of previous implementations used for multiple-valued logic circuits, such as static power consumption and noise vulnerability.

Index Terms—Inverter, multiple-valued logic (MVL) circuits, NMAX, NMN, voltage-mode quaternary CMOS design.

I. INTRODUCTION

The interest in electronic circuits that employ more than two discrete levels of signal has recently increased [1]. To go beyond regular CMOS, several researchers have tried to compact more information in a single gate or wire. This has been successfully accomplished in Flash memories, for example, where a single memory bit can hold different logic values. Regarding combinational circuits, most of the efforts have been targeted for the use of multiple-valued logic (MVL) circuits [2]–[4]. Several kinds of MVL circuits have been developed in the past decades, starting from early works on three-valued designs. MVL circuits have been implemented in bipolar technology such as integrated injection logic (I^2L) [5], emitter-coupled logic (ECL) [6], and charge-coupled devices (CCDs) [7] in CMOS technology and using quantum devices [8]. Among the suggested MVL designs concerning the standard IC fabrication process, the most promising was the current-mode CMOS [1]. Several prototype chips of current-mode CMOS circuits have been fabricated, showing somewhat better performances compared with the corresponding binary circuits [9]–[12]. However, some disadvantages are inherent to current-mode CMOS technology, the most critical ones being static power dissipation and variations on the output impedance. To overcome these limitations, some works regarding voltage-mode MVL have been recently published [13]–[15]. In [16], a low-power quaternary adder is presented as a promising way to solve the static power problem using some features of current-mode and voltage-mode combination, but it does not present other basic gates.

To deal with the static power dissipation problem and still maintain the logic compaction allowed by MVL gates, this brief proposes a novel quaternary voltage-mode CMOS logic using transistors with different threshold voltages (V_t) and three levels of power supply. We present inverter, NMAX, and NMN logic gates.

Spice simulations have been done to confirm the functionality and performance of the proposed voltage-mode CMOS quaternary logic as compared with previous voltage-mode quaternary circuits.

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