UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01383
U.S. Patent No. 8,404,508

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I. INTRODUCTION

In accordance with 37 C.F.R. § 42.107, Patent Owner Efficient Power Conversion Corporation ("EPC" or "Patent Owner") submits this preliminary response to the Petition (the "Petition" or "Pet.") filed by Petitioner Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. ("Petitioner") for *Inter Partes* Review of claims 1-5 of U.S. Patent No. 8,404,508 (the "'508 patent"). Patent Owner respectfully requests that the Board deny the Petition for at least the reasons set forth below.

First, Petitioner fails to establish that the asserted prior art teaches both a "gate photo resistant pattern" and a "metal photo resistant pattern" (or "fourth photo resistant pattern). The '508 patent describes and claims a separate and distinct "gate photo resistant pattern" and "metal photo resistant pattern." Petitioner admits that each of the asserted primary references (*Yoshida*, *Hikita-347*, *Hikita-023*) fails to disclose these two photo resistant patterns, instead relying on *Beach*. But Petitioner points to a single photo resist pattern in *Beach* as allegedly teaching both the claimed "gate photo resistant pattern" and a "metal photo resistant pattern." Because the claims require separate patterns that are used at different times in the claimed processes, Petitioner's challenges are deficient.

Second, Petitioner has not established that a person of ordinary skill in the art ("POSA") would have been motivated to combine the asserted primary

references (*Yoshida, Hikita-347, Hikita-023*) with *Beach* to result in the claimed methods of forming an enhancement mode GaN transistor. The '508 patent describes and claims processes for forming transistors in which a gate structure is formed before source and drain contacts are formed. These "gate first" processes are substantially different than the asserted primary references, which all form a gate structure after source and drain contacts are formed. These "gate first" processes are also substantially different than the crucial *Beach* reference, which simultaneously forms a gate structure and ohmic contacts (which Petitioner equates to the source and drain contacts). Petitioner has provided no motivation as to why a POSA would combine a "gate last" process with a simultaneous gate/ohmic formation process to result in a "gate first" process, as disclosed and claimed by the '508 patent.

Accordingly, Petitioner has not established that there is a reasonable likelihood that at least one of the challenged claims of the '508 patent is unpatentable, and the Petition should be denied.

II. BACKGROUND

A. The '508 Patent

The '508 patent describes and claims a method for making an enhancement-mode GaN HEMT (high electron mobility transistor) device using a single photo mask to form a gate structure, applying a photoresist pattern to pattern and etch

areas in a dielectric layer within which the source and drain contacts will be deposited, and applying a photoresist pattern to pattern and etch metal to form the source and drain contacts. The process results in an enhancement-mode GaN HEMT with a self-aligned gate structure. *See* '508 patent at 4:55-59.

The single mask self-alignment of the gate described in the '508 patent prevents misalignment between the gate metal and the GaN gate material. The '508 patent discloses a method for forming a GaN HEMT device in which the "gate metal 17 and the p-type GaN material 15 are patterned and etched using a single photo mask and are thus self-aligned." *Id.* at 4:55-59. The resulting HEMT performs better than those previously known in the art (particularly with respect to undesirable gate leakage) and can be manufactured less expensively due to the single photo mask process. *See id.* at 4:7-19.

As illustrated in the below Figures 3A-3C from the '508 patent, after epitaxial growth, shown in Fig. 3A, a gate metal 17 (for example, TiN) is deposited atop the p-type GaN layer 15. '508 patent at 3:26-44. Then, using photolithography, a gate photo-resist pattern is formed on the epitaxial wafer surface. *Id.* at 3:45-56. Then the gate metal 17 is then etched. *Id.* Subsequently, the p-type GaN gate layer 15 is etched using the same photo-resist pattern used to form the gate metal contact 17, resulting in the device of Fig. 3C. *Id.* Because the

two etching processes are formed with a single photo mask, the resulting gate structure is self-aligned.

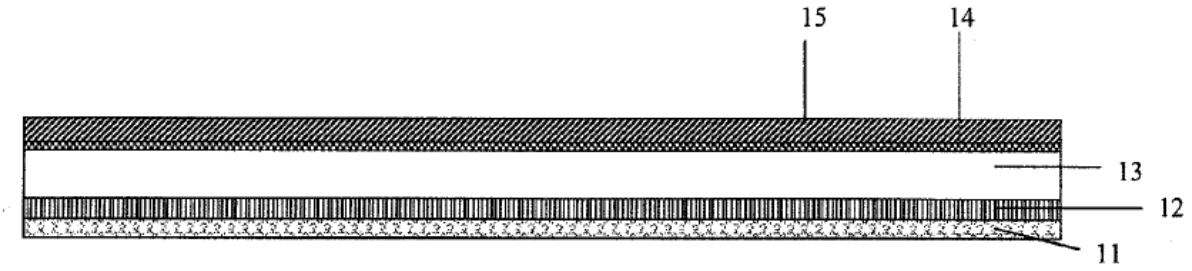


FIG. 3A

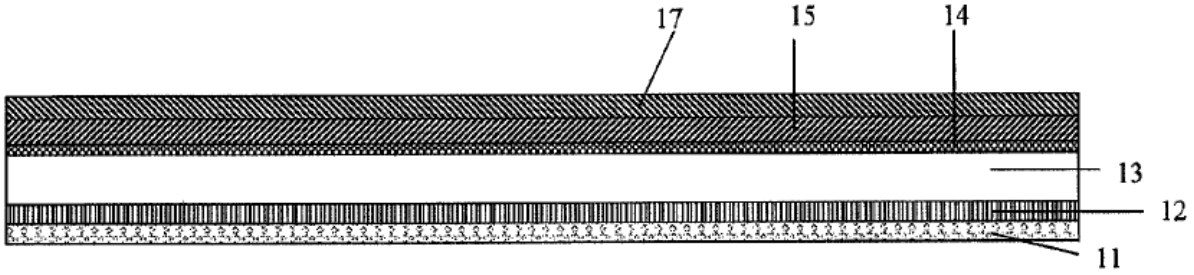


FIG. 3B

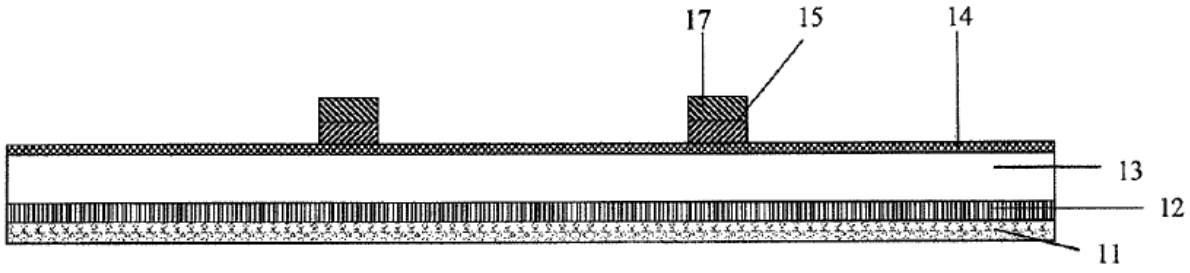


FIG. 3C

'508 Patent Figs. 3A-3C.

The gate structure of the '508 patent is formed before the source and drain contacts. That is, the '508 patent is directed to a "gate first" process. For example, as depicted in Fig. 3C, before source and drain contacts are formed, a single photo mask is used to pattern and etch the gate metal 17 and the p-type GaN gate layer 15. '508 patent at Fig. 3C, 3:45-47.

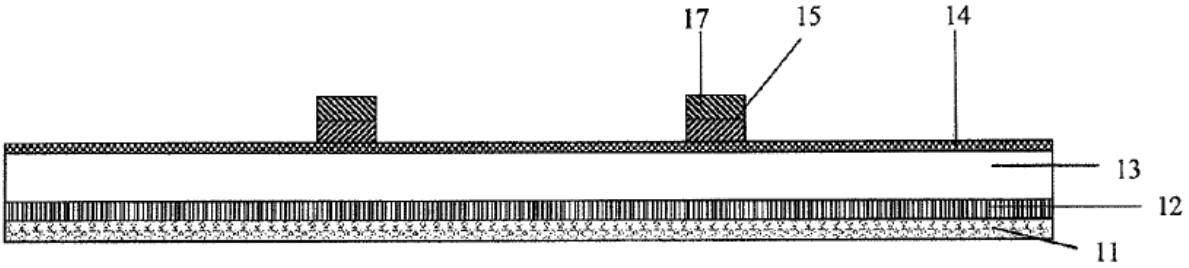


FIG. 3C

Subsequently, dielectric material 18 is deposited. After deposition of the dielectric material 18, a contact photo mask is used to pattern and etch the dielectric material 18, followed by a photoresist strip. The source and drain (20 and 19, respectively) are ultimately formed in the openings left by etching the dielectric material. '508 patent at Figs. 3D, 3E, 3:57-67.

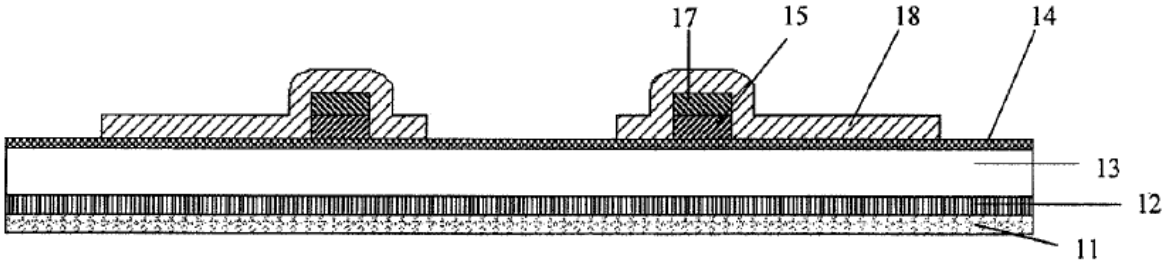


FIG. 3D

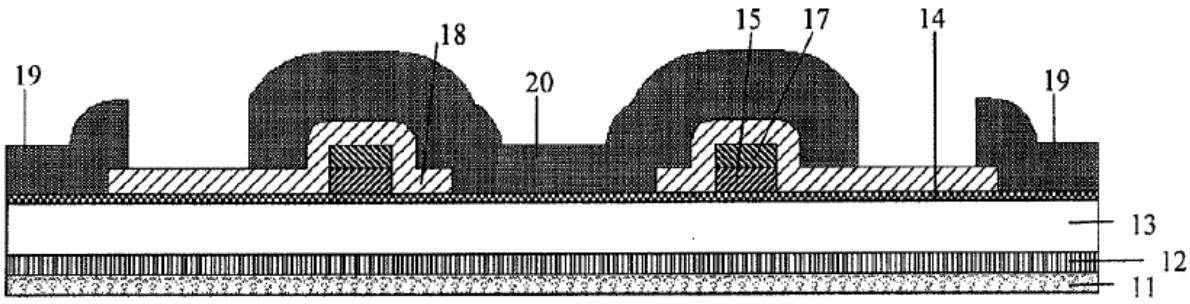


FIG. 3E

The claims are consistent with this description of a "gate first" process. For example, claim 1 requires "applying a gate photo resistant pattern," "etching away the gate contact layer outside the gate region," "etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact," and "removing the gate photo resistant pattern." These claimed steps result in a gate structure.

Claim 1 also requires "depositing a dielectric layer," "applying a contact photo resistant pattern," and "etching the dielectric to open the drain and source contact area." Because the claimed dielectric layer is etched to open the drain and source contact area, a POSA would understand that the dielectric layer must be deposited before forming the source and drain contacts. A POSA would also understand these claimed requirements to mean that the claimed gate structure was formed before the claimed source and drain contacts, because the claims do not specify that the dielectric layer is etched to form an opening for the gate structure. And if the dielectric layer was deposited before forming the gate structure, such an

opening in the dielectric layer would be necessary in order to result in an operating transistor.

Other embodiments, including the embodiments to which independent claims 4 and 5 are directed, have similar recitations that a POSA would understand describe a "gate first" process. *See* '508 patent at Figs. 5C, 5D, 5E, 7C, 7D, 7E, 7F, 4:41-54, 5:4-15.

B. Grounds of challenge

Petitioner challenges the patentability of the claims of the '508 patent on three grounds:

Ground 1: Claims 1-3 are challenged as being obvious over *Yoshida, Beach* and *Sheppard*.

Ground 2: Claims 1-4 are challenged as being obvious over *Hikita347, Beach* and *Sheppard*.

Ground 3: Claim 5 is challenged as being obvious over *Hikita023, Beach* and *Sheppard*.

III. CLAIM CONSTRUCTION

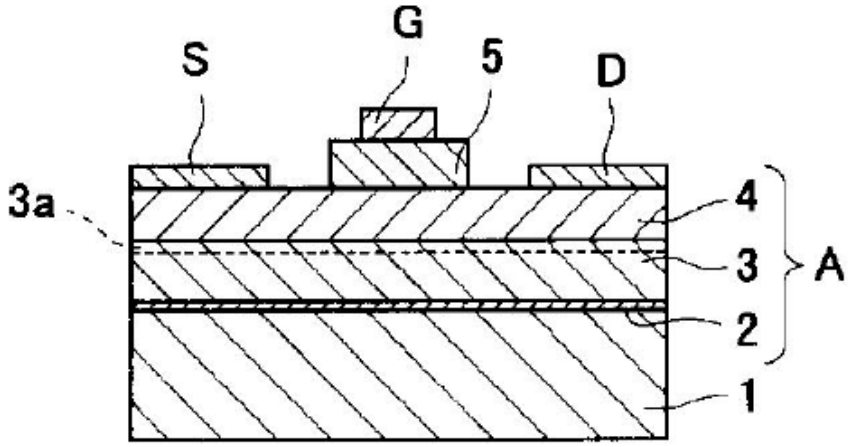
Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Without waiving its right to submit proposed claim

constructions in a Patent Owner Response, Patent Owner submits that the Board need not engage in any pre-institution claim construction.

IV. Overview of Selected References Relied Upon by Petitioner

A. Yoshida

Yoshida discloses an enhancement mode GaN HEMT, with a p-GaN layer under the gate contact:



Ex. 1004, Fig. 1.

The enhancement mode GaN HEMT of *Yoshida* is made by a process in which the gate structure is formed *after* forming the source and drain contacts (e.g., a "gate-last" process), as opposed to the "gate-first" process of the '508 patent. Specifically, as described in the Petition and in the '508 patent, Yoshida discloses the following process:

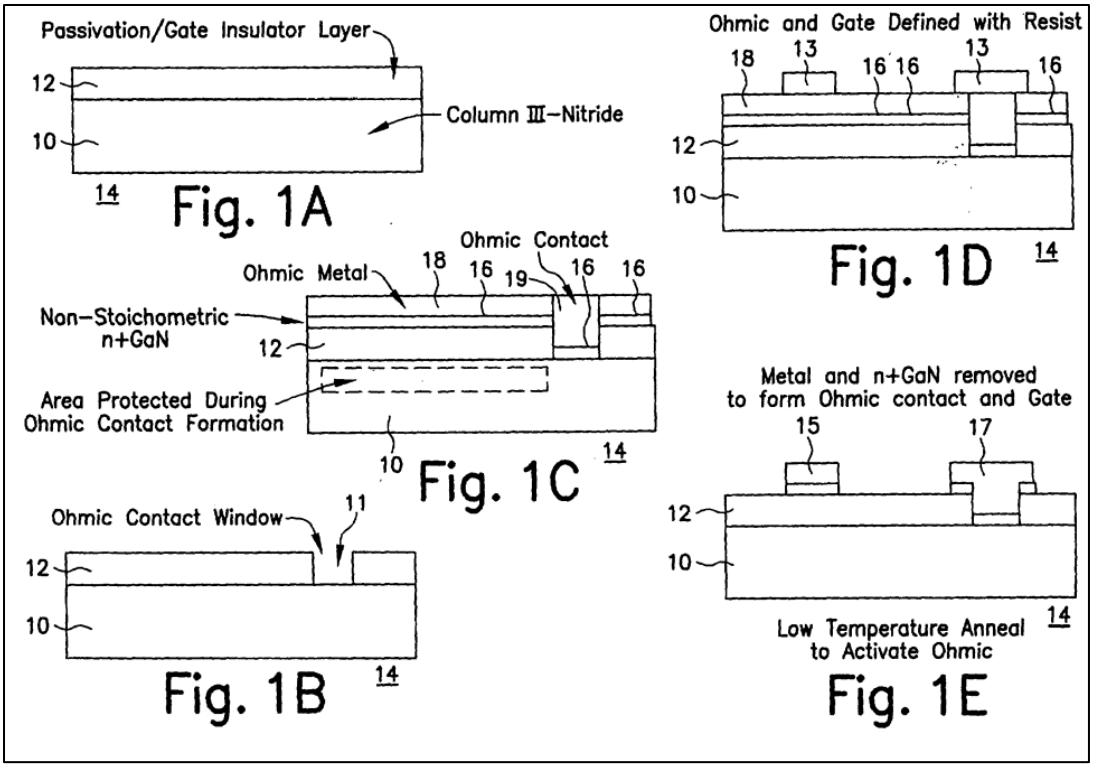
1. grow layers 2-5 over the substrate 1;

2. etch away the p-GaN layer 5 except where the gate electrode is to be loaded;
3. deposit a dielectric layer (SiO_2) to cover the entire surface, including the p-GaN layer 5;
4. apply photo resist/mask, open areas in the dielectric layer for the source S and drain D electrodes;
5. deposit Al in the openings to form the source S and drain D electrodes on the AlGaN barrier layer;
6. remove the mask and open the SiO_2 film over the gate p-GaN material 5, leaving the source S and drain D electrodes masked.
7. deposit Au in the opening to form the gate electrode G and form the gate contact above the p-GaN layer to produce an enhancement mode GaN transistor.

Petition at 14-15, citing *Yoshida* at [0013], [0021]-[0023].

B. Beach

The Beach process differs significantly from the "gate-first" process of the '508 patent and the "gate-last" process of *Yoshida*, described above. This process is shown in Figures 1A-1E below.



Ex. 1005 at Figs. 1A-1E.

First, as shown in Figure 1A, a III-nitride layer 10 and a gate insulator layer 12 are formed on a substrate. Ex. 1005 at [0039] and [0040].

Second, as shown in Figure 1B, "an ohmic contact window 11 is opened in layer 12 to provide access to layer 10 for the deposition of an ohmic contact." *See id* at [0042]. The gate insulator layer 12 serves as the insulator layer in the depletion mode MISFET of Beach.

Third, as shown in Figure 1C, non-diffusive protective layer 16, is formed over the device 14 of Figure 1B. *See id.* at [0043]. After the deposition of the material layer 16 atop the III-nitride layer 10 and the gate insulator layer 12 and

within the ohmic contact window 11, an ohmic metal material layer 18 is deposited. *See id* at [0045].

Fourth, as shown in Figure 1D, "resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17." *See id.* at [0047]. After the photoresist layer 13 has been deposited, an etching takes place, removing the portions of the ohmic metal layer 18 and material layer 16 except within the areas protected by the photoresist layer 13. *See id.* Notably, as is evident from this description, *Beach* teaches a single etching step to finalize the formation of the gate 15 and ohmic contact 17, such as source and drain contacts, all at the same time.

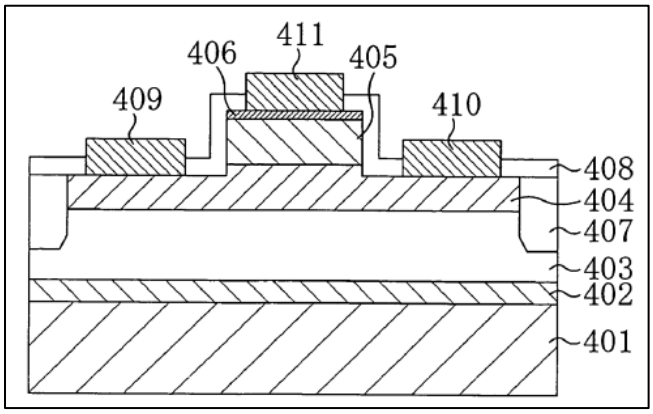
Last, "the photoresist layer 13 is stripped off and the resultant structure is subjected to a low temperature anneal step," *Id.* at [0049].

Figure 1E shows the results of this final etching step. There now exists a defined gate contact 15 and an ohmic contact 17, **both formed in a single step**.

C. Hikita-347

Hikita-347 discloses an enhancement-mode GaN transistor for use in consumer-electronic products. Ex. 1007 at [0001] and [0011]. *Hikita-347's* enhancement-mode GaN transistor includes a substrate 401, an AlN buffer layer 402, an undoped GaN layer 403, an undoped AlGaN layer 404, and a p-type AlGaN layer 405, a heavily doped p-type GaN layer 406, a gate electrode 411,

source electrode 409, and drain electrode 410. Id. at [0048]. An exemplary embodiment of *Hikita-347* is presented in the following figure:

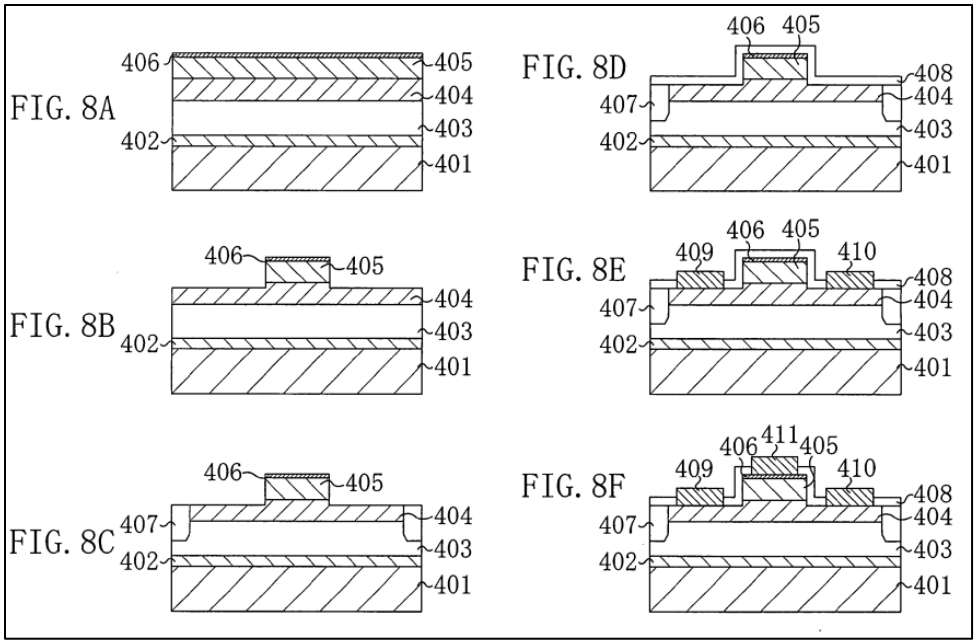


Ex. 1007 at Fig. 4.

Notably, *Hikita-347* corresponds to the enhancement mode device identified in Fig. 1 of the '508 patent as "Prior Art". Compare Fig. 4 of *Hikita-347* with Fig. 1 of the '508 patent.

Hikita-347 also discloses an additional transistor structure that only has a single p-type layer 105, the equivalent to 405 above, rather than two doped p-type GaN layers 405 and 406 as shown in Figure 4 above. *See* Ex. 1007 at [0040] (explaining that "it is not necessary that the heavily doped p-type GaN layer 106 is provided").

Hikita-347 also describes the process to form the GaN transistors of Figure 4. *See* Ex. 1007 at [0055]-[0061]. This process is shown in Figures 8A-8F below.



Ex. 1007 at Figs. 8A-8F.

First, as shown in Figure 8A, an AlN buffer layer 402, an undoped GaN layer 403, an undoped AlGaN layer 404, a p-type AlGaN layer 405, and an optional heavily doped p-type GaN layer 406 are formed on a sapphire substrate. *See* Ex. 1007 at [0040] and [0056].

Second, as shown in Figure 8B, the heavily doped p-type GaN layer 406, the p-type AlGaN layer 405 and an upper portion of the undoped AlGaN layer 404 are etched. *See* Ex. 1007 at [0035], [0057].

Third, as shown in Figure 8C, an isolation region 407 is formed by implanting boron into parts of the undoped AlGaN layer 404 and undoped GaN layer 403, blocking the remaining regions of the device with photoresist, as in Figure 8C. *See* Ex. 1007 at [0058].

Fourth, as shown in Figure 8D a SiN film 408 is formed to cover the upper surface of the wafer. *See* Ex. 1007 at [0059].

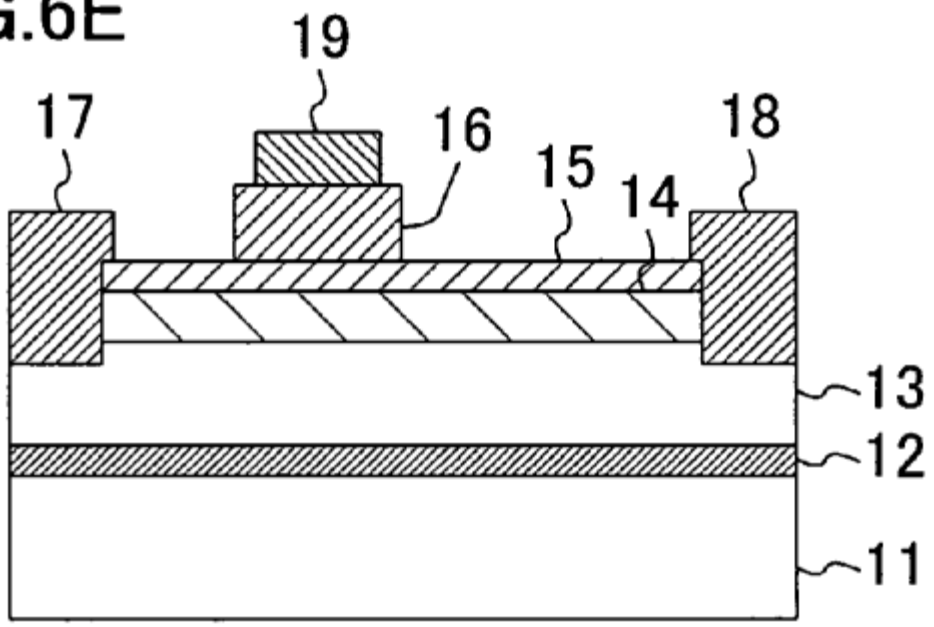
Fifth, as shown in Figure 8E, openings are formed in the SiN film 408. Then, a source electrode 409 and a drain electrode 410 are formed within these openings, followed by a heat treatment in an N_2 atmosphere at 650° C. *See* Ex. 1007 at [0060].

Last, after the source and drain contacts have been fully formed as shown in Figure 8F, an opening is created in the upper surface of SiN film 408 above the p-type semiconductor layers 405 and 406. A gate electrode 411 is formed in the opening. *See* Ex. 1007 at [0061]. Thus, *Hikita-347* is another example of a "gate last" process.

D. Hikita-023

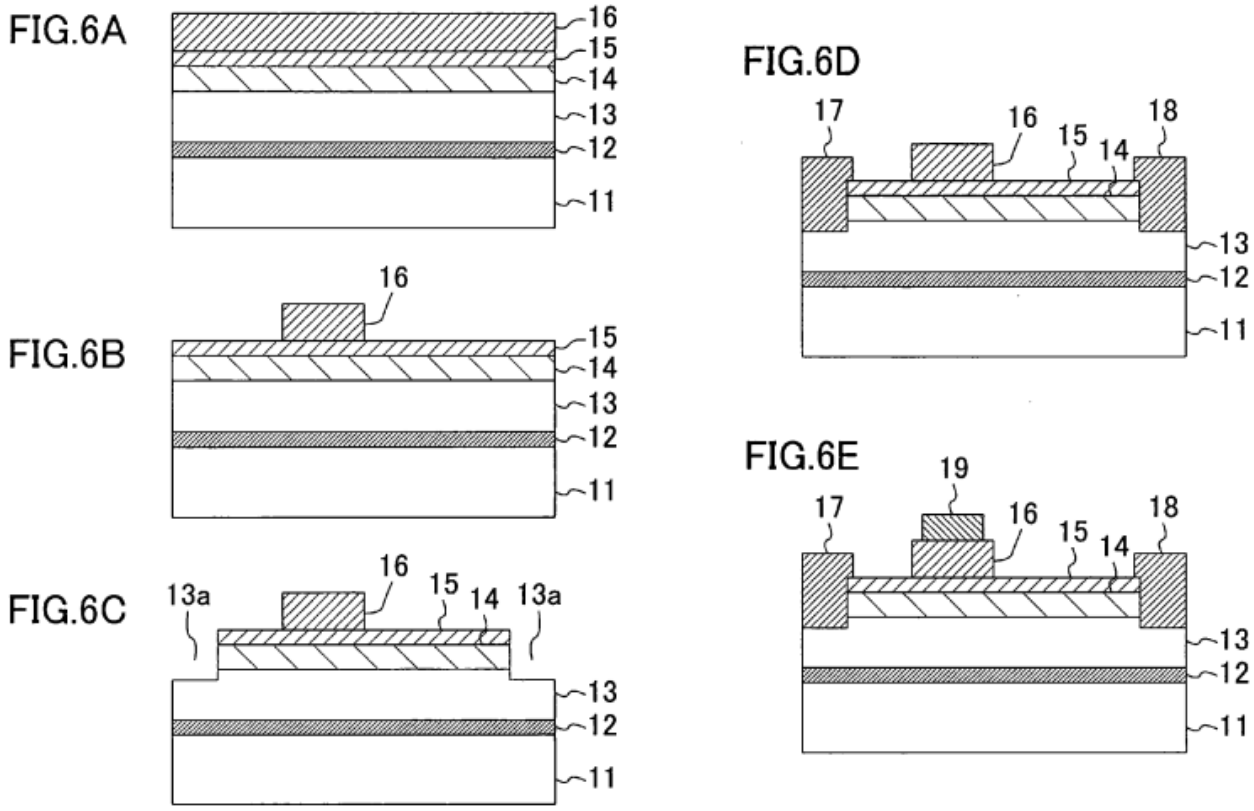
Hikita-023 discloses an enhancement-mode GaN transistor for use in consumer-electronic products. Ex. 1008 at [0014] and [0037]. *Hikita-023's* enhancement-mode GaN transistor includes a substrate 11, a buffer layer 12, a channel layer 13, an undoped GaN barrier layer 14, a p-type AlGaN layer 15, and a p-type GaN layer 16, source electrode 17, and drain electrode 18, and a gate electrode 19. *Id*. at [0076]-[0080]. An exemplary embodiment of *Hikita-023* is presented in the following figure:

FIG.6E



Ex. 1008 at Fig. 6E.

Hikita-023 also describes the process to form the GaN transistors of Figure 4. *See Hikita-023* at [0055]-[0061]. This process is shown in Figures 8A-8F below.



Ex. 1008 at Figs. 6A-8E.

First, as shown in Figure 6A, a buffer layer 12, a channel layer 13, an undoped GaN barrier layer 14, a p-type AlGaN layer 15, and a p-type GaN layer 16, are formed on a substrate 11. *See* Ex. 1008 at [0076].

Second, as shown in Figure 6B, the p-type GaN layer 16 is etched. *See id.* at [0077].

Third, as shown in Fig. 6C, the "p-type AlGaN layer 15, the barrier layer 14, and the upper portion of the channel layer 13 are selectively removed to form recesses 13a serving as source and drain electrode formation regions in the epitaxial layer." *Id.* at [0078].

Fourth, as shown in Figure 6D, the source electrode 17 and drain electrode 18 are formed by a liftoff method. *See Id.* at [0079].

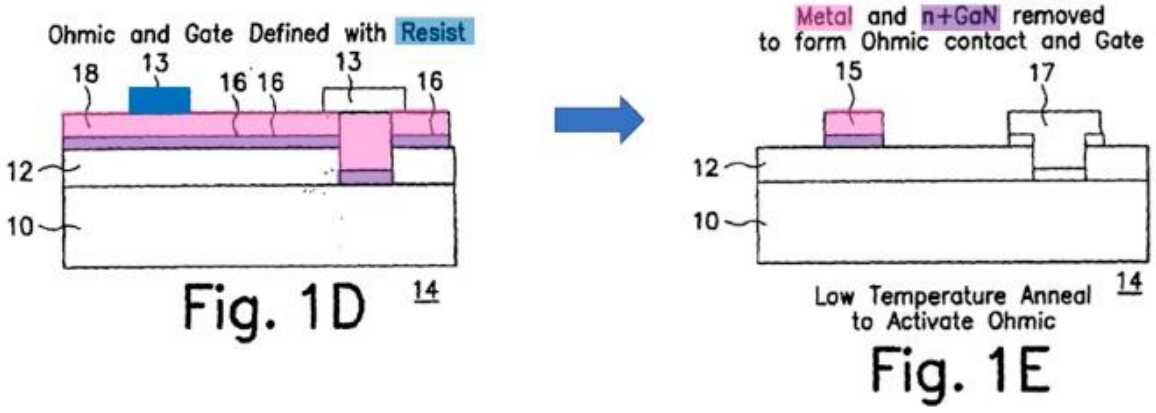
Lastly, **after** the source and drain contacts have been fully formed as shown in Figure 6D, as shown in Figure 6E, the gate electrode 19 is formed on the p-type GaN layer 16 by a liftoff method. *See* Ex. 1008 at [0080]. Thus, *Hikita-023* is another example of a "gate last" process.

V. The Board Should Deny Institution of Ground 1

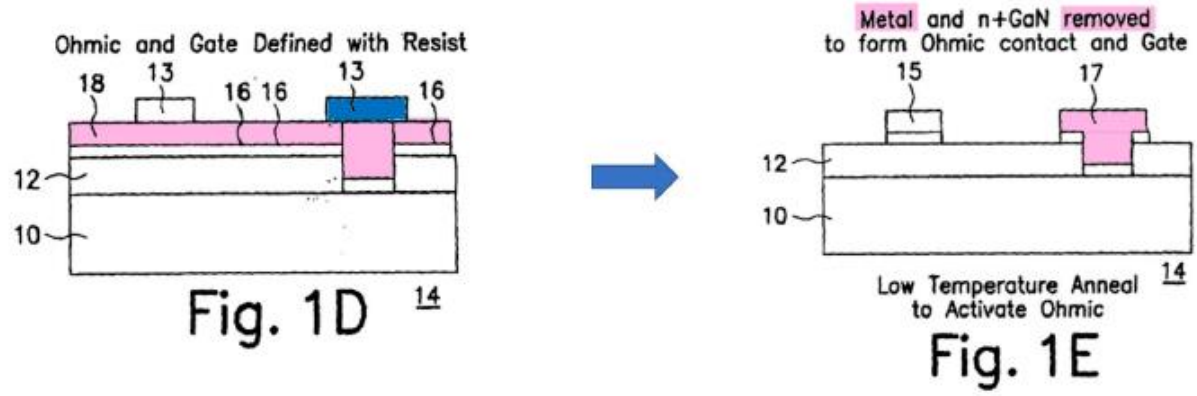
A. Petitioner has not established that *Yoshida*, alone or in combination with *Beach* and *Sheppard*, does teaches both a "gate photo resistant pattern" and a "metal photo resistant pattern" as required by claim 1

Petitioner concedes that *Yoshida* does not disclose the claimed "applying a gate photo resistant pattern" and the claimed "applying a metal photo resistant pattern." *See* Petition at 30-33 and 35-39, respectively. Instead, Petitioner alleges that *Beach* discloses these steps, and that it renders obvious the claimed elements missing from *Yoshida*. *See id.* Petitioner is incorrect.

In *Beach*, the Petitioner points to the same photoresist 13 as the evidence for both the "gate photo resistant pattern" and "metal photo resistant pattern." Petition at 32-33 and 36-37. Specifically, Petitioner has provided the following annotated figures which make clear that it is referring to a single element of Beach (photoresist 13), as both the alleged "gate photo resistant pattern" and "metal photo resistant pattern":



Petition at 33.



Petition at 37.

Furthermore, Petitioner alleges the following:

Second, *Beach* discloses step [1e2], i.e., applying a gate photo resistant pattern 13 (mask) to the structure, as shown below. *Beach*, [0047] ("resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17").

Third, *Beach* discloses step [1e3], i.e., etching away the gate contact layer outside the gate region, and step [1e4], i.e., etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact, as shown below. *Beach*, [0047] ("After the deposition of photoresist layer 13, material 18 is removed, as by etching, except

> where protected by photoresist 13. The removal, or etching process, also eliminates protective layer 16 under patterned photoresist 13.").

Petition at 32-33.

> First, *Beach* discloses that an ohmic contact metal 18 is deposited in ohmic contact window 11. *Beach*, [0045] ("Material 18 deposited over layer 16 and in ohmic contact window 11 … may be an ohmic metal").
>
> Second, *Beach* discloses that a metal photo resistant pattern 13 (mask) is applied over the ohmic contact metal 18. *Beach*, [0047] ("resist material 13 is deposited in a pattern to permit the formation of a gate 15 and ohmic contact 17.").
>
> Third, *Beach* discloses that the ohmic contact metal 18 is etched except the portion protected by the mask. *Beach*, [0047] ("After the deposition of photoresist layer 13, material 18 is removed, as by etching, except where protected by photoresist 13.").

Petition at 36-37.

Thus, Petitioner improperly conflates the use of a single photoresist (13) in *Beach* with the use of a "gate photo resistant pattern" and "metal photo resistant pattern," which are distinctly claimed in the '508 patent and correspond to separate photo resistant patterns that are used at different times in the claimed process. For example, the claimed "gate photo resistant pattern" is used to form a gate structure using a single mask. *See* '508 patent at 3:45-50, claim 1. Separately, the claimed "metal photo resistant pattern," a different pattern than the "gate photo resistant pattern," is used as part of the process to form the claimed source and drain contacts, which occurs at a different time than using the "gate photo resistant pattern" to form a gate structure. *See* '508 patent at 3:64-67, claim 1. A single

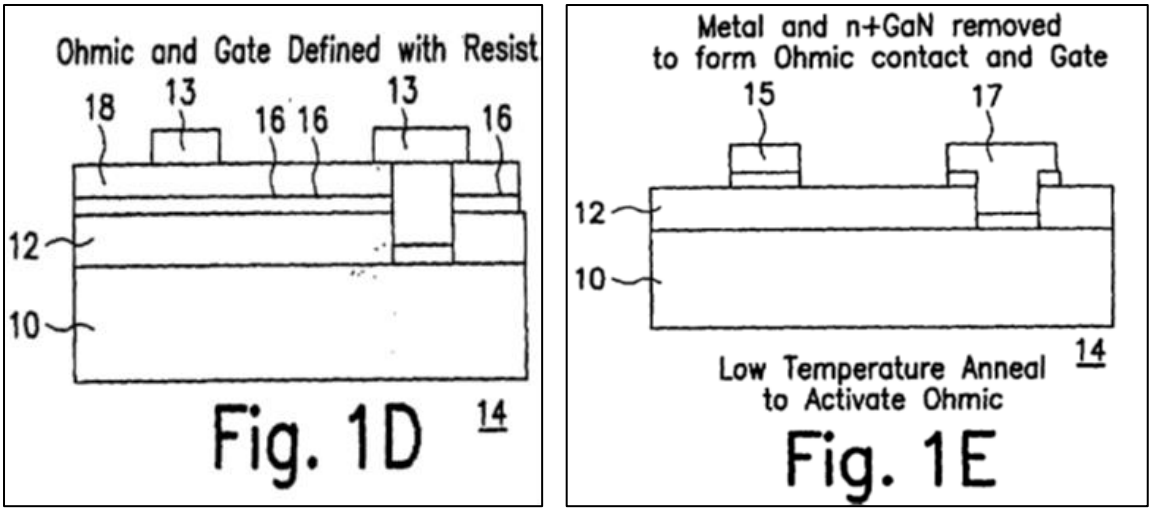
photoresist pattern that is used to simultaneously form a gate and ohmic contacts (which Petitioner equates to the source and drain contacts), such as Beach's photoresist 13, cannot correspond to the separately claimed "gate photo resistant pattern" and "metal photo resistant pattern."

Therefore, for at least the reasons above, Petitioner has not established that *Yoshida*, alone or in combination with *Beach* or *Sheppard* render obvious the claimed "applying a gate photo resistant pattern" and "applying a metal photo resistant pattern" as recited in claim 1 of the '508 patent.

Accordingly, the Board should deny institution of Ground 1.

B. A POSA would not be motivated to combine *Yoshida* and *Beach*

A POSA would not have found it obvious to combine the teachings of *Yoshida* with *Beach* to result in the claimed method, absent hindsight. *Beach's* teaching of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teachings of *Yoshida*. *Beach's* simultaneous contact formation process of *Beach* is shown in the figures below.



Ex. 1005, Figs. 1D and 1E.

As seen in these figures, *Beach* discloses a transistor that has a III-N (typically GaN) channel layer (10), and a gate insulator (12). *Beach* forms openings in the gate insulator (12) and deposits a protective layer 16. *See* Ex. 1005 at [0042]-[0043], [0048]. Then, *Beach* deposits a metal layer (18) and forms a photoresist pattern (13) on the metal layer. *See id.* at [0046]-[0047]. These steps result in the device as depicted above in *Beach* Figure 1D.

Subsequently, *Beach* forms the gate and ohmic contacts by etching the metal layer at the same time. *See id.* at [0048]. Notably, *Beach* forms both the gate and ohmic contacts from the same metal material layer 18. *See id.*

Conversely, *Yoshida* forms the drain and source contacts *before* the formation of a gate electrode. *See* Ex. 1004 at [0021]-[0023]. As such, *Yoshida* discloses a "gate-last" process, in which the gate is fabricated after the source and drain contacts have been fabricated. Both the simultaneous gate/ohmic contact

formation of *Beach* and the "gate last" process of *Yoshida* are dramatically different from the "gate first" process of the '508 patent. Petitioner has provided no motivation as to why a POSA would combine a "gate last" process, like *Yoshida*, with the simultaneous gate/ohmic formation process of *Beach* to result in a "gate first" process, as disclosed and claimed by the '508 patent. *Personal Web Technologies v. Apple*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) ([Petitioner] conten[ds] that a person of ordinary skill in the art reading [two references] would have understood that the combination of [them] would have allowed for the selective access features of [one reference] to be used with [the other reference's] content-dependent identifies feature. But that reasoning seems to say no more than that a skilled artisan, once presented with two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.) (quotations omitted).

Therefore, for at least the reasons discussed above, the Board should deny institution of Ground 1.

VI. The Board Should Deny Institution of Ground 2

A. *Hikita-347*, alone or in combination with *Beach* and *Sheppard*, does not teach both a "gate photo resistant pattern" and a "metal photo resistant pattern" as required by claims 1 and 4

Petitioner concedes that *Hikita-347* does not disclose the claimed "applying a gate photo resistant pattern" and the claimed "applying a metal photo resistant pattern." *See* Petition at 56-58 and 60-61, respectively. Instead, Petitioner alleges that *Beach* discloses these steps, and that it renders obvious the claimed elements missing from *Hikita-347*. *See id.* Petitioner is incorrect.

Just as it has done in Ground 1, Petitioner points to the same photo resist pattern (13) as the evidence for both the "gate photo resistant pattern" and "metal photo resistant pattern." Petition at 61.

Thus, similar to Ground 1, Petitioner improperly conflates the use of a single photoresist (13) in *Beach* with the use of a "gate photo resistant pattern" and "metal photo resistant pattern," which are distinctly claimed in the '508 patent and correspond to separate photo resistant patterns that are used at different times in the claimed process. For example, the claimed "gate photo resistant pattern" is used to form a gate structure using a single mask. *See* '508 patent at 3:45-50, 4:41-44, claims 1 and 4. Separately, the claimed "metal photo resistant pattern," a different pattern than the "gate photo resistant pattern," is used as part of the process to form the claimed source and drain contacts, which occurs at a different time than using the "gate photo resistant pattern" to form a gate structure. *See* '508 patent at 3:64-67, 4:49-52, claims 1 and 4. A single photoresist pattern that is used to simultaneously form a gate and ohmic contacts (which Petitioner equates to the

source and drain contacts), such as Beach's photoresist 13, cannot correspond to the separately claimed "gate photo resistant pattern" and "metal photo resistant pattern."

Therefore, for at least the reasons above and for those provided above in conjunction with Ground 1, Petitioner has not established that *Hikita-347,* alone or in combination with *Beach* or *Sheppard* render obvious the claimed "applying a gate photo resistant pattern" and "applying a metal photo resistant pattern" as recited in claims 1 and 4 of the '508 patent.

Accordingly, the Board should deny institution of ground 2.

B. A POSA would not be motivated to combine *Hikita-347* and *Beach*

A POSA would not have found it obvious to combine the teachings of *Hikita-347* with *Beach* to result in the claimed method, absent hindsight. *Beach's* teaching of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teachings of *Hikita-347*.

Conversely, *Hikita-347* forms the drain and source contacts *before* the formation of a gate electrode. *See* Ex. 1007 at [0059]-[0061] and Figures 8D-8F. As such, *Hikita-347* discloses a "gate-last" process, in which the gate is fabricated after the source and drain contacts have been fabricated. Both the simultaneous gate/ohmic contact formation of *Beach* and the "gate last" process of *Hikita-347* are dramatically different from the "gate first" process of the '508 patent.

Petitioner has provided no motivation as to why a POSA would combine a "gate last" process, like *Hikita-347*, with the simultaneous gate/ohmic formation process of *Beach* to result in a "gate first" process, as disclosed and claimed by the '508 patent. *Personal Web Technologies v. Apple*, 848 F.3d at 993-94.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 2.

VII. The Board Should Deny Institution of Ground 3

A. *Hikita-023*, alone or in combination with *Beach* and *Sheppard*, does not teach both a "gate photo resistant pattern" and a "fourth photo resistant pattern" as required by claim 5

Petitioner concedes that *Hikita-023* does not disclose the claimed "applying a gate photo resistant pattern" and the claimed "applying a fourth photo resistant pattern." *See* Petition at 84-86 and 89-90, respectively. Instead, Petitioner alleges that *Beach* discloses these steps, and that it renders obvious the claimed elements missing from *Hikita-023*. *See id.* Petitioner is incorrect.

Just as it has done in Grounds 1 and 2, Petitioner points to the same photo resist pattern (13) in *Beach* as the evidence for both the "gate photo resistant pattern" and "fourth photo resistant pattern." Petition at 84-86 and 89-90.

Thus, similar to Grounds 1 and 2, Petitioner improperly conflates the use of a single photoresist (13) in *Beach* with the use of a "gate photo resistant pattern" and "fourth photo resistant pattern," which are distinctly claimed in the '508 patent

and correspond to separate photo resistant patterns that are used at different times in the claimed process. For example, the claimed "gate photo resistant pattern" is used to form a gate structure using a single mask. *See* '508 patent at 5:4-8, claim 5. Separately, the claimed "fourth photo resistant pattern," a different pattern than the "gate photo resistant pattern," is used as part of the process to form the claimed source and drain contacts, which occurs at a different time than using the "gate photo resistant pattern" to form a gate structure. *See* '508 patent at 3:64-67, 4:49-52, 5:13-15, claim 5. A single photoresist pattern that is used to simultaneously form a gate and ohmic contacts (which Petitioner equates to the source and drain contacts), such as Beach's photoresist 13, cannot correspond to the separately claimed "gate photo resistant pattern" and "fourth photo resistant pattern."

Therefore, for at least the reasons above and for those provided above in conjunction with Grounds 1 and 2, Petitioner has not established that *Hikita-023*, alone or in combination with *Beach* or *Sheppard* render obvious the claimed "applying a gate photo resistant pattern" and "applying a fourth photo resistant pattern" as recited in claim 5 of the '508 patent.

Accordingly, the Board should deny institution of Ground 3.

B. A POSA would not be motivated to combine *Hikita-023* and *Beach*

A POSA would not have found it obvious to combine the teachings of *Hikita-023* with *Beach* to result in the claimed method, absent hindsight.

Beach's teaching of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teachings of *Hikita-023*.

Conversely, *Hikita-023* forms the drain and source contacts *before* the formation of a gate electrode. *See* Ex. 1008 at [0075]-[0080], Figs. 6A-6E. As such, *Hikita-023* discloses a "gate-last" process, in which the gate is fabricated after the source and drain contacts have been fabricated. Both the simultaneous gate/ohmic contact formation of *Beach* and the "gate last" process of *Hikita-023* are dramatically different from the "gate first" process of the '508 patent. Petitioner has provided no motivation as to why a POSA would combine a "gate last" process, like *Hikita-023*, with the simultaneous gate/ohmic formation process of *Beach* to result in a "gate first" process, as disclosed and claimed by the '508 patent. *Personal Web Technologies v. Apple*, 848 F.3d at 993-94.

Therefore, for at least the reasons discussed above, the Board should deny institution of ground 3.

VIII. RESERVATION OF RIGHTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut any such arguments in its Patent Owner Response if IPR is instituted. Similarly, Patent Owner does not concede any underlying contentions in the Petition and reserves the right to rebut any such contention later. Further, Patent

Owner is not limited to the arguments presented in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented herein.

IX. CONCLUSION

For the foregoing reasons, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

Dated: December 21, 2023

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER's PRELIMINARY RESPONSE complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word count tool in Microsoft Word, the brief contains 4843 words, excluding the parts of the document that are exempted by 37 C.F.R. § 42.24(a).

Dated: December 21, 2023

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** is being served on counsel of record by filing this document through the Patent Review Processing System, with a copy served via electronic mail to the following email address, as authorized in the Petition:

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