

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before the Honorable Clark S. Cheney
Chief Administrative Law Judge**

In the Matter of

**CERTAIN SEMICONDUCTOR DEVICES,
AND METHODS OF MANUFACTURING
SAME AND PRODUCTS CONTAINING
THE SAME**

Investigation No. 337-TA-1366

COMPLAINANT’S OPENING CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Complainant Efficient Power Conversion Corporation's ("EPC") four asserted patents¹ are all directed to novel gallium nitride (GaN) semiconductor high-electron mobility transistors (HEMTs) that exhibit superior functionalities.

Generally, GaN HEMTs are comprised of a gate, source, and a drain as depicted in Figure 1 below.² Depending upon the voltage applied at the gate, the gate controls whether electric current flows between the source and the drain in the buffer layer region. The gate has a metal contact connecting to the voltage source and semi-insulating nitride gate material underneath it, resting above the barrier layer.

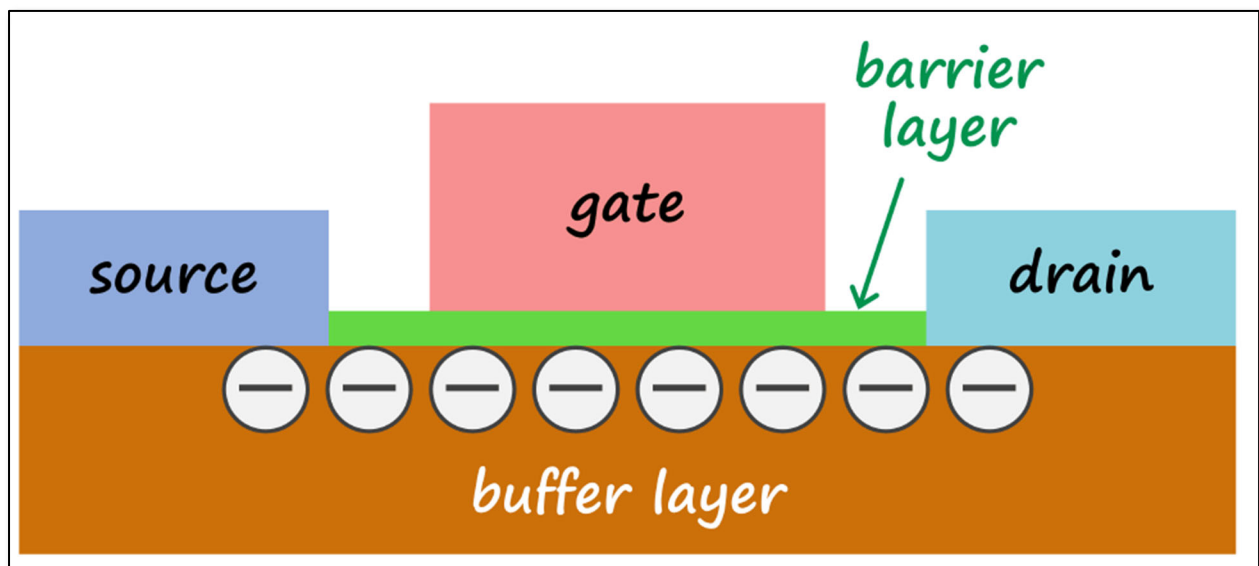


Figure 1 Basic GaN HEMT Structure

¹ The four asserted patents include U.S. Patent No. 8,350,294 ("the '294 patent"), U.S. Patent No. 8,404,508 ("the '508 patent"), U.S. Patent No. 9,748,347 ("the '347 patent"), and U.S. Patent No. 10,312,335 ("the '335 patent") (collectively, the "Asserted Patents").

² The figure is a modified version of Figure 1.7(b) from Complaint Exhibit 45, which is a textbook by, among others, Dr. Alex Lidow who is a co-founder of Complainant and a co-inventor of the Asserted Patents. The textbook provides a good overview of GaN transistors.

The '294 patent describes EPC's novel compensated GaN gate that reduces gate leakage current, a problem associated with prior HEMTs.

The '508, '335, and '347 patents are directed to self-aligned GaN gates, including configurations with symmetrical ledges and side surfaces that extend horizontally towards the source and the drain, that further serve to reduce gate leakage current and create better performing GaN HEMTs.

* * * * *

Complainant's proffered constructions are grounded in the intrinsic evidence and the well-established understanding of those skilled in the art. Conversely, Respondents import limitations from the specification into the claims to narrow the claims beyond their plain meaning so to avoid infringement. In other respects, Respondents also misconstrue structural claim limitations as product-by-process claims in contravention of well-settled Federal Circuit authority.

II. LAW OF CLAIM CONSTRUCTION

The words of a claim "are generally given their ordinary and customary meaning . . . [which is] the meaning that the term would have to a person of ordinary skill in the art ["POSA"] in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (citations omitted). The POSA "is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.* at 1313. Indeed, claims are to be read in view of the specification, which is "the single best guide to the meaning of disputed terms." *Id.* at 1315.

Words in a claim must be given their ordinary and customary meaning unless the intrinsic evidence mandates that an alternative construction apply. The only exceptions to giving the

words in a claim their ordinary and customary meaning are: (1) when the applicant acts as their own lexicographer; and (2) when the applicant disavows or disclaims the full scope of a claim term in the specification. “Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question.” *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001).

Although the construction that “stays true to the claim language and most naturally aligns with the patent’s description of the invention” will be the correct construction,” *Phillips*, 415 F.3d at 1316, it is improper to import limitations from the specification into the claims. *Id.* at 1323. “Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim.” *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (“[A] particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment.”).

The rule against importation applies not only to restrictions that would serve to narrow the scope of a claim, but also applies to the order of steps in a claimed method. The Federal Circuit has enacted a two-part test for determining whether the steps of a method claim must be limited to a certain order: (1) examination of “the claim language to determine if, as a matter of logic or grammar, they must be performed in the order written”; and (2) examination of “the rest of the specification to determine whether it directly or implicitly requires such a narrow construction.” *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369-70 (Fed. Cir. 2003). If neither apply, “the sequence in which such steps are written is not a requirement.” *Id.* at 1370.

And although such steps may be ordered in described embodiments, it is improper to import that order from those embodiments into the claims:

The number of embodiments disclosed in the specification is not determinative of the meaning of disputed claim terms. Nor are claims ordinarily limited in scope to the preferred embodiment. These principles apply with equal force where the limitation to be imported from the specification is an order of method steps, rather than a limitation on a specific claim term.

Id.

III. CLAIM CONSTRUCTION OF ASSERTED PATENTS

A. “a compensated GaN layer”

This term appears in claim 1 of the '294 patent. It should be construed as follows:

“a semiconductor GaN gate material in which one type of dopant, impurity, or imperfection (for example, donor) partially cancels the electrical effects of the other type of dopant, impurity, or imperfection (for example, acceptor)”

EPC’s construction applies the plain meaning to a POSA of “GaN layer” and “compensated” consistent with the *Phillips* standard. 415 F.3d at 1312-13. Respondents’ incorrect construction—“a doped GaN layer formed with a step to passivate its impurities”—fails to recognize that a POSA would understand the claimed “GaN layer” to be a GaN *gate* material. Moreover, Respondents improperly seek to have the limitation construed as a product-by-process limitation, contending that “compensated” refers to a process. As discussed below, however, a POSA would understand the term “compensated” in the context of the claim to be referring to and connoting a specific structure and electrical characteristics in the claimed “GaN layer,” not a process to create a GaN layer.

1. “GaN Layer” Refers to GaN Gate Material

A POSA would understand the plain meaning of the term “compensated GaN layer” in view of both the claim and the specification to be referring to a “compensated GaN gate

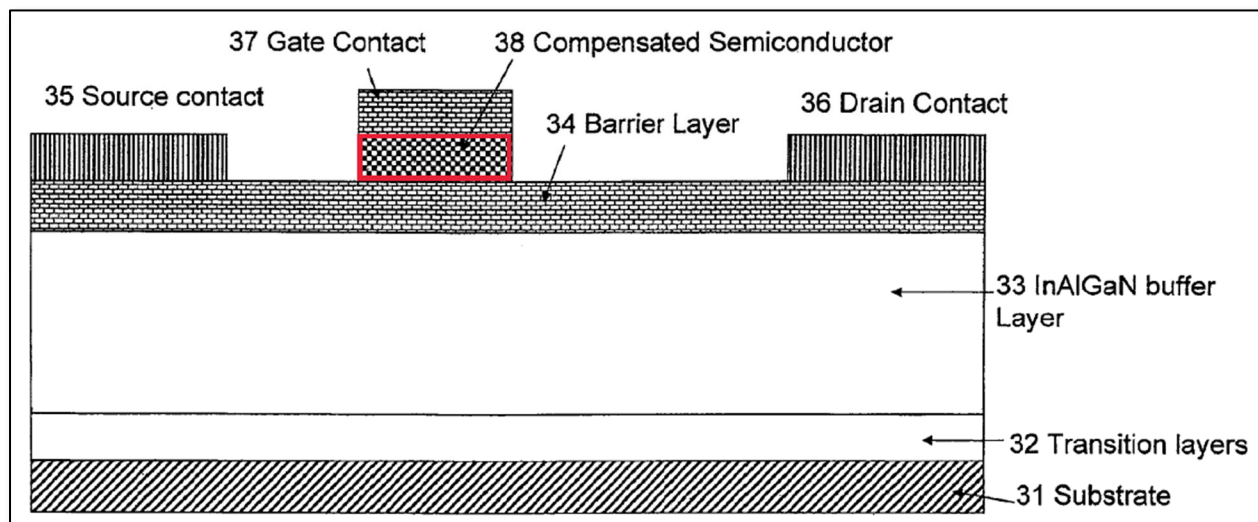
material.” No claim term should be construed in a vacuum, out of context with the other words in a claim. *Phillips*, 415 F.3d at 1314 (“[T]he claims themselves provide substantial guidance as to the meaning of particular claim terms.”); *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1347 (Fed. Cir. 2008) (“[T]his court does not interpret claim terms in a vacuum, devoid of the context of the claim as a whole.”); *ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) (“While certain terms may be at the center of the claim construction debate, the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms.”).

Claim 1 of the ’294 patent describes a transistor where the “compensated GaN layer” is formed “above the barrier layer” and that “a gate contact” is formed “above the compensated GaN layer.” A POSA would understand from the placement of the “compensated GaN layer” between the barrier and the gate contact that the “GaN layer” is a GaN gate material.

The POSA’s interpretation based on the claim language itself is confirmed by the specification. “[T]he specification is always highly relevant to the claim construction analysis . . . [and] it is the single best guide to the meaning of a disputed term.” *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Here, the entirety of the specification refers solely to a compensated GaN gate material. The ’294 patent is titled “Compensated **Gate** MISFET and Method for Fabricating Same.” The specification details the problems with prior art GaN transistors having unfavorable **gate** leakage (*see* ’294 patent at 1:55-2:6) and identifies a solution to that problem by creating a compensated **gate** “with low **gate** leakage.” *Id.* at 2:13-14 (emphasis added).

The figures and Summary of Invention further confirm the POSA’s understanding of the meaning of “compensated GaN layer” based on the claim itself. Indeed, in describing Figure 2,

the specification explains that “a compensated semiconductor layer 38 is formed over the barrier layer 34 and under the *gate* contact 37.” *Id.* at 3:7-9 (emphasis added). Figure 2 (excerpted below with the compensated GaN layer annotated in red) has the same structure as recited in claim 1.



A POSA would understand that the layer between the gate contact and the barrier layer—in Figure 2 just as in claim 1—refers to a GaN gate material. Indeed, the Summary of Invention explains that the claimed inventions are directed to using a material “below the gate contact and above the barrier layer” to “reduce[]” “gate leakage.” *Id.* at 2:14-16; *see also id.* at 3:18-21 (“using a compensated semiconductor layer 38 leads to low *gate* leakage during device operation”) (emphasis added). A POSA would understand that it is the gate material between these layers that contributes to reducing gate leakage, not some other type of GaN layer. Moreover, the specification provides a method of making the device depicted in Figure 2 (a transistor) and recites the step of “etch[ing] away the compensated semiconductor layer 38, except the portion beneath the gate contact layer 37.” *See id.* at 3:35-38. A POSA reading the claim in light of the specification would have understood the ’294 patent to be describing the

manufacturing of a gate stack, where the gate material is beneath the gate contact, and serves the purpose of turning the transistor on or off.

In short, the intrinsic evidence confirms that a POSA would have understood the term “compensated GaN layer” as used in claim 1 to be referring to a compensated GaN gate material, which is the only structure described in the intrinsic evidence as providing the advantages to the claimed transistor over the prior art and which the applicant identified as being at the heart of the claimed inventions.

2. Compensated Describes a Semiconductor with Modified Electrical Characteristics

A POSA would have understood the term “compensated” to have its plain and ordinary meaning in the art. Declaration of Dr. Eric Fred Schubert in Support of Complainant’s Opening Claim Construction Brief (“Schubert Decl.”). The IEEE dictionary defines “compensated semiconductor” as “[a] semiconductor in which one type of impurity or imperfection (for example, donor) partially cancels the electric effects of the other type of impurity or imperfection (for example, acceptor).” *See* Schubert Decl., ¶ 37 (citing IEEE Dictionary). EPC’s construction is the same as the IEEE’s dictionary but includes the term “dopant,” a form of impurity in the GaN semiconductor crystal structure, consistent with the specification’s explanation that the compensated GaN gate material has a “high doping level.” *See* ’294 patent at 3:16-17; *see also* Schubert Decl., ¶ 38 (citing IEEE Dictionary defining “dopant” as an “impurity”).

The description of “compensated” in the specification of the ’294 patent is consistent with the plain and ordinary meaning of “compensated.” For example, the specification explains that the compensated GaN gate material includes a p-type impurity (e.g., Mg, Zn, Be, Cd, or Ca) that imparts an electric effect (i.e., conductivity), and a second impurity, e.g., hydrogen, that partially cancels the electric effect of the p-type impurity by rendering it semi-insulating. ’294

patent at 3:10-13, 3:43-45. The specification explains further that by having the electrical effect of the p-type impurity cancelled out by another impurity, the p-type gate material is differentiated from the prior art by having modified electrical characteristics—specifically, by being more resistive than the conductive structures found in the prior art. *See id.* at 3:46-49 (“the compensated semiconductor layer 38 is a highly compensated semi-insulating material, while in GaN transistor 100 of the prior art, layer 105 is a conductive p-type material.”). A more resistive p-type GaN gate material has improved functional characteristics compared to the prior art, including “low gate leakage during device operation,” *id.* at 3:16-19, reduced gate capacitance, and the ability to act as an enhancement mode device (where the transistor is activated only when a positive voltage is applied to the gate contact). Indeed, nowhere does the ’294 patent refer to a compensated GaN material anywhere other than in connection with the compensated GaN gate. In fact, a POSA reading the ’294 patent – beginning with its title – would have understood the compensated GaN as part of the gate structure to be the novel feature that distinguished the claimed transistor from the prior art by reducing gate leakage.

Because the term “compensated” has a plain meaning in the art and because the intrinsic evidence describes a “compensated GaN layer” consistent with the plain meaning of the term, EPC’s plain-meaning construction should be adopted.

3. Respondents’ Construction Should be Rejected

Respondents’ construction of “compensated GaN layer” as “a doped GaN layer formed with a step to passivate its impurities” is incorrect for several reasons.

First, Respondents’ construction does not apply the plain and ordinary meaning of “compensated GaN layer” to a POSA as “compensated *GaN gate material*.” As discussed above, the claimed structure is not referring to any GaN layer, but rather a gate material. Thus,

Respondents' non-construction renders the term impermissibly broader than its plain meaning in view of the intrinsic evidence.

Second, Respondents' failure to construe GaN layer consistent with the intrinsic evidence by limiting the GaN layer to the gate material would encompass transistor designs in which the compensated GaN layer does not serve as gate semiconductor material and does not reduce the gate leakage current, as taught in the '294 patent. Schubert Decl., ¶ 45 (citing the '294 patent at 2:15-16). For example, a transistor with a compensated GaN layer that is separate from the gate structure and in contact with the source and the drain would fall under Respondents' expansive construction. In such a transistor, the gate structure would consist only of the metal, and as a result, the compensated GaN layer would not prevent gate leakage, as taught by the '294 patent. Respondents' reading of the claim term in isolation is therefore incorrect.

But even if there was an equal choice between Respondents' broad construction and EPC's narrower construction, which there is not for the reasons discussed above, the proper choice would be the narrower construction proposed by EPC. *See Takeda Pharm. Co. v. Zydus Pharms. USA, Inc.*, 743 F.3d 1359, 1365 (Fed. Cir. 2014) ("We long ago established that '[w]here there is an equal choice between a broader and a narrower meaning of a claim, and there is an enabling disclosure that indicates that the applicant is at least entitled to a claim having the narrower meaning, we consider the notice function of the claim to be best served by adopting the narrower meaning.'") (quoting *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996)).

Third, "compensated GaN layer" is not a product-by-process limitation. Indeed, nothing in the claim defines the "compensated GaN layer" in terms of the processes used to compensate. The purpose of the product-by-process "doctrine is to prevent foreclosing inventors 'from the

benefits of the patent system simply because a product is difficult to describe in words, or its structure is insufficiently understood.” *In re Biogen* 335 F. Supp. 3d 688, 712 (D.N.J. 2018) (quoting *SmithKline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312 (Fed. Cir. 2006)), *rev'd and remanded sub nom. Biogen MA Inc. v. EMD Serono, Inc.*, 976 F.3d 1326 (Fed. Cir. 2020). In this case, claim 1 of the '294 patent is not directed to a product that the inventors were unable to describe in words or where the product's structure was not sufficiently understood. *Id.* As discussed above, the IEEE dictionary itself underscores that the term is well understood in the field and a POSA would have readily understood that the term “compensated GaN” layer refers to a GaN layer having certain structural and electric characteristics, not a GaN layer made according to a particular process.

Respondents have made the same argument in the context of their IPR directed to the '294 patent. Respondents argued in their petition that “while the claim uses ‘compensated as an adjective, that adjective derives from a past-tense verb” and that “[t]he past-tense form of ‘compensated’ suggests that the step of compensating had occurred.” Declaration of Dipu A. Doshi in Support of Complainant’s Opening Claim Construction Brief (“Doshi Decl.”), Exhibit A (Petition for *Inter Partes Review*, IPR2023-01381, at 14). Even if Respondents were correct that the term “compensated” derives from a past-tense verb, that does not transform the term “compensated” into a process term. Indeed, in *In re Garnero*, the predecessor court to the Federal Circuit recognized that past-tense verbs such as “‘intermixed,’ ‘ground in place,’ ‘press fitted,’ ‘etched,’ and ‘welded’ all . . . at one time or another have been separately held capable of construction as structural, rather than process, limitations.” 412 F.2d 276, 279 (C.C.P.A. 1969); *see also 3M Innovative Prop. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (“‘[S]uperimposed’ . . . neither transforms claim 1 into a product-by-process claim nor

even limits the scope of the claim to a serial method of manufacture; it describes only the structural relationship between the embossing patterns.”); *Hazani v. U.S. Int’l Trade Comm’n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997) (“chemically engraved” not a process term). As discussed above, “compensated GaN layer” is not merely “capable of construction as [a] structural, rather than a process, limitation,” *In re Garnero*, 412 F.2d at 279, a POSA would understand the term to be a structural term.

But even if the Court believes that “compensated” can be interpreted as both a structural limitation (as EPC proposes) and as a process limitation (as Respondents propose), the term still would not be a product-by-process limitation. “[W]ords of limitation that can connote with equal force a structural characteristic of the product or a process of manufacture are commonly and *by default* interpreted in their structural sense, unless the patentee has demonstrated otherwise.” *In re Nordt Dev. Co.*, 881 F.3d 1371, 1375 (Fed. Cir. 2018) (emphasis added). Here, the patentee has clearly demonstrated that “compensated” is to be interpreted in its structural sense as allowing for modified electric characteristics in a GaN gate material that were otherwise possible in a material that was not compensated. *See Hazani*, 126 F.3d at 1479 (“chemically engraved” limitation not a product-by-process limitation because the limitation, “read in context, describes the product more by its structure than by the process used to obtain it”).

**B. “etching away the doped GaN layer,
except a portion of the doped GaN layer beneath the gate contact”**

This term appears in claim 1 of the ’508 patent. It should be construed as follows:

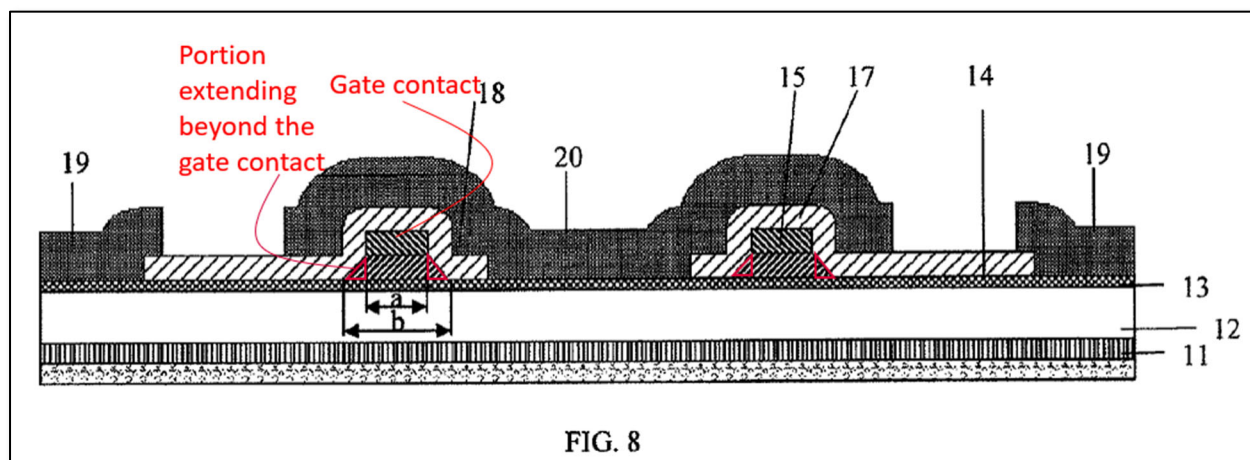
“etching away the doped GaN layer without etching beneath the gate contact”

EPC’s construction is consistent with the Staff’s proposed construction and applies the plain and ordinary meaning of the term as identifying a region to avoid while etching (i.e., except a portion

. . . beneath the gate contact”). Respondents’ incorrect construction—“etching away the doped GaN layer in *all regions* extending outside the gate contact” (emphasis added)—would improperly transform the negative limitation as defining an area to avoid into an affirmative requirement not contemplated by the intrinsic evidence.

Nothing in the intrinsic evidence requires that the doped GaN gate material be etched in “all regions extending outside the gate contact.” All that is required is that the area under the gate contact not be etched. Respondents’ construction cannot be correct as it would read out numerous embodiments described in the ’508 patent. The ’508 patent relates to methods of forming an enhancement mode transistor with a single photo mask, which allows for self-alignment of a gate contact and gate material and also reduces the costs associated with manufacturing. ’508 patent at 4:6-9. Claim 1 is directed to “[a] method of forming an enhancement mode GaN transistor” that involves numerous steps, including the etching step in dispute. Etching is a tool that is used along with the single photo masking to create the various structures in the transistor, including the gate contact and gate material. Claim 1 recites that the gate contact and gate material are each etched. But claim 1 does not include any limitations on the shape of the various transistor structures to be achieved through the claimed etching. Figure

8 is an embodiment describing a trapezoidal structure for the gate material, as depicted below.³



As shown by this figure, Respondents’ construction of the disputed term as requiring “etching away the doped GaN layer in *all regions extending outside* the gate contact” would impermissibly read out this embodiment as well as those depicted in Figures 9-12 as it would result in etching of a portion of the gate material corresponding to the inventive “ledges” and “side surfaces,” which are limitations of other asserted claims, but also are within the scope of claim 1 of the ’508 patent and thus are embodiments of this claim. Claim constructions that exclude preferred embodiments are “rarely, if ever, correct and would require highly persuasive evidentiary support.” *Vitronics*, 90 F.3d at 1583. There is nothing in the intrinsic evidence that supports Respondents’ construction excluding a preferred embodiment.

C. ’508 Patent, Claim 1

Claim 1 of the ’508 patent is a method that requires four distinct steps. Claim 1 provides, in relevant part:

A method of forming an enhancement mode GaN transistor, the method comprising: . . .

³ This embodiment shows an example of “side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer. This limitation is discussed below in Section III.E.

applying a gate photo resistant pattern;
etching away the gate contact layer outside the gate region;
etching away the doped GaN layer, except a portion of the
doped GaN layer beneath the gate contact;
removing the gate photo resistant pattern;

EPC does not believe any construction of these process steps is required beyond recognizing that each of these steps defines a discrete process step. *See, e.g., Kyocera Senco Indus. Tools Inc. v. Int’l Trade Comm’n*, 22 F.4th 1369, 1382 (Fed. Cir. 2022) (“presumption” that elements listed separately in claim are distinct elements).

The constructions proposed by Respondents improperly seek to impute an order into these process steps. Respondents’ proposed construction also violates basic claim construction principles by seeking to import the “gate photo resistant pattern” limitation into each of the defined etching steps and therefore adds restrictions neither contemplated by the claim itself nor mandated by any other intrinsic evidence.

1. Respondents’ Proposed Ordering of Claim 1 Is Contrary to Federal Circuit Authority

The Federal Circuit has held that a court should not assume the steps in a method claim must be performed in the sequential order in which they are listed “[u]nless the steps . . . actually recite an order.” *Interactive Gift Exp., Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342 (Fed. Cir. 2001). A sequential order may be imputed into a method claim however, where “as a matter of logic or grammar, . . . the steps [must] be performed in the order written, or the specification directly or implicitly requires’ an order of steps.” *Mformation Techs., Inc. v. Rsch. In Motion Ltd.*, 764 F.3d 1392, 1398 (Fed. Cir. 2014) (internal citations omitted). An order is not required simply because it is described in an embodiment. Imposing a restriction of order into a claim based on an order described in an embodiment violates the rule against importing restrictions

from the specification into the claims. *See CH₂O, Inc. v. Meras Eng'g, Inc.*, No. LA CV13-08418 JAK, 2015 WL 12743876, at *9 (C.D. Cal. Dec. 29, 2015) (“[U]sing the example in the written description to require a specific sequence of steps would improperly import limitations from the specification on the claims.”); *Bd. of Regents of the Univ. of Tex. Sys. V. BenQ Am. Corp.*, No. A-05-CA-181-SS, 2006 WL 6112210, at *15 (W.D. Tex. July 14, 2006) (declining to limit the claim as requiring that the “inputting step be fully completed before the matching step begins” based on such disclosure in “the only embodiment disclosed in the specification”); *see also Altiris*, 318 F.3d at 1371 (no order imputed to claimed method based on order of steps in preferred embodiment where the intrinsic evidence was devoid of “any statement that this order is important” or “disclaimer of any other order or steps,” or “any prosecution history indicating a surrender of any other order of steps”).

In this case, only two of the steps, the first and fourth recited limitations, are required in the order recited because, as a matter of logic, a photo resistant pattern must be applied before the photo resistant pattern is removed. Other than that, neither the logic nor grammar of the claim dictates that the method steps be performed in the recited order. Respondents’ construction seeks to impute an order into the claimed method based on the described embodiments. For example, the specification, in describing Figure 3C, explains a process of using a single photo mask whereby the photo mask is used to apply a photo resistant pattern (photoresist) and etch the gate contact and gate material, and then the photo resistant pattern (photoresist) is removed. ’508 patent at 3:45-50. But nothing in the intrinsic evidence reflects any statement that this particular order is important, any disclaimer of any other order or steps, or any surrender of any other order of steps. Respondents’ construction, which limits the claimed

steps to the order written in the claims, improperly imports limitations from the specification into the claim.

Respondents' construction conflates a single photo mask with a single photoresist, but that is not what the patent describes. The '508 describes a single photo mask that is used to form a gate structure that has a gate material under a gate contact. *See, e.g.*, the '508 patent at 3:1-6, 3:45-47, 4:6-9, 4:41-44, 4:55-59 (describing patterning and etching of gate metal material and doped GaN material). One embodiment includes using a single photo mask to pattern a photoresist from the single photo mask and etching both the GaN gate material and gate contact and then removing the photoresist. The claim, however, is not limited to this embodiment, and, as discussed above, there should be no presumption that steps in a method claim must occur in the order recited. As Dr. Schubert explains, it is possible to use a single photo mask to pattern a photoresist, etch one of the underlying materials, remove the photoresist, and use the etched underlying material as a mask for etching a second underlying material. Schubert Decl., ¶¶ 67, 76 (Steps 2-6). The above steps fall within the claimed process. Respondents' attempt to import limitations from the specification should be rejected.

2. Respondents Improperly Import the “Photo Resistant Pattern” Limitation into Both Etching Steps

As discussed above, the only order that is imputed to the claimed method is one dictated by logic. Logically, a photo resistant pattern must first be applied before it is removed; a photo resist pattern must first be applied before the first layer (the gate contact) is etched; and the gate contact must be etched before the gate material is etched. Beyond the logical order inherent in the claimed technology, no other can be imputed without violating the rule against importing limitations from the specification into the claims. *Phillips*, 415 F.3d at 1323 (“[A]lthough the

specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.”).

Claim 1 of the '508 patent requires only that a photo resistant pattern be applied and removed. The claim does not place any limits on when the photo resistant pattern is to be used after etching the gate metal contact. As explained by Dr. Schubert (at ¶¶ 67, 76), a POSA would have known that, in an exemplary embodiment, once the metal gate is formed using the single photo mask and its corresponding photo resistant pattern, the photo resistant pattern can be removed and the edges defining the newly formed gate metal contact can serve to guide the further etching of the GaN gate material. Thus, the photo resistant pattern may be used to etch the gate metal only or, alternatively, it can also be used to further etch the GaN gate material underneath that gate metal contact. Logic dictates that the photo resistant pattern must be applied before the gate contact is etched. But to the extent Respondents are asserting that the photo resistant pattern must remain present throughout both etching steps and not removed until the final etching step, that conclusion is not dictated by the claim itself or the specification.

Indeed, had the applicant wanted the photo resistant pattern to be “used” (as Respondents propose) as part of both etching steps in the context of claim 1 of the '508 patent and not removed until after those etching steps are performed, the applicant knew how to express this order of steps based on the description of embodiments in the specification itself. For example, the specification describes that after “a gate metal 17 is deposited,” “[s]ubsequently, a single photo mask is used to pattern and etch the gate metal 17 and the p-type GaN gate layer 15, resulting in the structure shown in FIG. 3C. The gate metal 17 and the p-type GaN gate layer are etched by any known technique . . . followed by a photoresist strip.” '508 patent at 3:39-50. But, that recitation of order is absent from claim 1.

Because the applicant chose not to limit the scope of claim 1 to the described embodiments, it would be improper to read the claims as being limited to those embodiments, as Respondents’ construction would require. *Phillips*, 415 F.3d at 1323; *see also CH₂O*, 2015 WL 12743876, at *9 (“[U]sing the example in the written description to require a specific sequence of steps would improperly import limitations from the specification on the claims.”); *BenQ Am.*, 2006 WL 6112210, at *15 (declining to limit the claim as requiring that the “inputting step be fully completed before the matching step begins” based on such disclosure “in the only embodiment disclosed in the specification”). All that is required by the claim is that a photo resistant pattern be applied and removed and that two layers be etched. The specification does not **require** the “use” of the claimed photo resistant pattern as part of any of the claimed etching steps. Respondents’ attempt to import such a restriction into the claim violates clear Federal Circuit standards and must be rejected.

D. “wherein the pair of horizontal ledges of the p-type gate material are self-aligned” / “a pair of self-aligned ledges”

These terms appear in claims 2 and 5 of the ’335 patent. They should be construed as follows:

Term	Construction
“wherein the pair of horizontal ledges of the p-type gate material are self-aligned” ’335 patent, claim 2	“wherein the process of creating the pair of ledges involves forming the p-type gate material and the gate metal using a single photo mask” Not a product-by-process limitation
“a pair of self-aligned ledges” ’335 patent, claim 5	“a pair of ledges created with a process that involves forming the p-type gate material and the gate metal using a single photo mask” Not a product-by-process limitation

EPC’s construction applies the plain meaning of the term “self-aligned” to a POSA in view of the intrinsic evidence—specifically, as a process that involves use of a single photo mask. Respondents do not appear to dispute this point. Rather, they contend only that the limitation at issue is a product-by-process limitation. But, as discussed below, the term “self-aligned ledges” refers to a structure that is created by a certain process (i.e., a single photo mask), the limitation is not a product-by-process limitation. And, Respondents cannot meet their burden to show that the process of self-alignment can be ignored as part of an invalidity analysis.

1. “Self-Aligned” Refers to a Process that Uses a Single Photo Mask

A POSA would understand the term “self-aligned” as used in claims 2 and 5 of the ’335 patent to be referring to a process that utilizes a single photo mask to create the claimed ledges. As Dr. Schubert explains, the ’335 patent, like all Asserted Patents, is directed to GaN transistors that are manufactured using photo masking and etching technology to define the features of the claimed transistors, including, for example, the gate metal, p-type GaN material, and related ledges and side surfaces. Schubert Decl. at ¶ 34. For two features to be self-aligned to each other, only one photo mask can be used. As Dr. Schubert explains, when a single photo mask is used to define the patterns of the gate metal and the p-type gate material at the same time, the centers of the two features are aligned with one another. *Id.* at ¶¶ 75-76. Accordingly, the p-type gate material is self-aligned with the gate metal and vice versa. When more than one photo mask is used, however, the same alignment between the centers of the two features may not be achievable because the process of applying the second photo mask typically leads to deviations in alignment between the material etched using the first photo mask and the second photo mask. *Id.* at ¶ 77. This problem is eliminated through self-alignment.

EPC's construction therefore applies the POSA's understanding of the term "self-aligned" in the context of the claims and the other intrinsic evidence. Respondents have chosen not to propose a construction for the term "self-aligned" and have not previously articulated why EPC's proposed construction does not align with the plain meaning of the term to a POSA in view of the intrinsic evidence. EPC respectfully submits, however, that because the term itself, standing alone, does not have a plain and ordinary meaning, it is important for the term to be construed in the way a POSA would understand the term in view of the intrinsic evidence. *See Phillips*, 415 F.3d at 1313.

2. "Self-Aligned Ledges" Is Not a Product-by-Process Limitation

Respondents incorrectly contend that the claimed "self-aligned ledges" term is a product-by-process limitation. Respondents' strategy in doing so is clear—they seek to ease their burden on invalidity by ignoring the self-alignment process entirely, relying on the general rule that the validity of a product-by-process claim focuses "on the product and not the process of making it." *Greenliant Sys., Inc. v. Xicor LLC*, 692 F.3d 1261, 1268 (Fed. Cir. 2012). EPC disagrees that Respondents can prove invalidity without considering self-alignment in the prior art because self-alignment, as used in claims 2 and 5 of the '335 patent, connotes a specific structure to the claimed GaN transistor and imparts structural and functional differences onto the claimed GaN transistor.

EPC does not dispute that the term "self-aligned ledges" refers to a product made by a process; EPC's construction confirms as much. But whether the term refers to a product made by a process does not end the inquiry into whether the "self-aligned ledges" term is a "product-

by-process” limitation.⁴ A “product-by-process” claim is one in which the product is defined, at least in part, in terms of the method or process by which it is made. *Bonito Boats, Inc. v. Thunder Craft Boats, Inc.*, 489 U.S. 141, 158 n. *2 (1989) (citing D. Chisum, *Patents* § 8.05, p. 8–67 (1988)). The mere reference to a process in a product claim, however, does not render that claim a “product-by-process” claim. Instead, “if the process limitation connotes specific structure and may be considered a structural limitation,” then the so-called process limitation is considered structural. *In re Nordt*, 881 F.3d at 1374. This is because “words of limitation that can connote with equal force a structural characteristic of the product or a process of manufacture are commonly and by default interpreted in their structural sense, unless the patentee has demonstrated otherwise.” *Id.* at 1375. Moreover, even if a particular limitation, on its face, is a product-by-process limitation, that process limitation is not made irrelevant “if the process by which [the claimed] product is made imparts ‘structural and functional differences’ distinguishing the claimed product from the prior art.” *Greenliant*, 692 F.3d at 1268 (recognizing this as the “exception to th[e] general rule that the process by which the product is made is irrelevant” to an invalidity analysis) (citing *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1370 (Fed. Cir. 2009)).

⁴ Whether the “self-aligned ledges” term is a product-by-process limitation allowing Respondents to avoid the alleged process entirely as part of its invalidity analysis is an issue that should be resolved at the claim construction stage. *See, e.g., Pacira Pharms. Inc. v. eVenus Pharms. Labs., Inc.*, Nos. 22-00718 & 21-19829, 2023 WL 3841559, at *9 (D.N.J. June 6, 2023) (“Whether a term is a product-by-process limitation is part of the Court’s analysis at the claim construction stage.”). EPC respectfully submits that whether Respondents have met their burden to show that the claimed process is not entitled to patentable weight should be resolved now because the issue is part-and-parcel to Respondents’ contention that the disputed limitation is a product-by-process limitation.

In assessing whether a process imparts structural or functional differences to the claimed product such that the process is entitled to patentable weight, the specification, the prosecution history, and any extrinsic evidence may be considered. *See Amgen*, 580 F.3d at 1365-67; *Purdue Pharma L.P. v. Epic Pharma, LLC*, 811 F.3d 1345, 1353-54 (Fed. Cir. 2016). Respondents, as the parties asserting invalidity, bear the burden of proving that the claimed process limitation does not impart structural or functional characteristics on the claimed product that differentiate the claimed product from the prior art. *See, e.g., Cubist Pharms., Inc. v. Hospira, Inc.*, 75 F. Supp. 3d 641, 668 (D. Del. 2014) (“The party asserting anticipation bears the burden of proving that the process limitations do not result in an invention distinguishable from the prior art.”) (citing *Amgen*, 580 F.3d at 1370), *aff’d*, 805 F.3d 1112 (Fed. Cir. 2015).

As discussed below, the term “self-aligned” connotes specific structure to the claimed GaN transistor. And even if the term, on its face, refers to a product created by a process, the process imparts structural and functional differences that differentiate the claimed GaN transistor over the prior art and is therefore entitled to patentable weight. Accordingly, the term “self-aligned ledges” is not a product-by-process limitation, and Respondents cannot meet their burden to show otherwise.

i. “Self-Aligned Ledges” Connotes Specific Structure to the Claimed GaN Transistor

The term “self-aligned” ledges is not a product-by-process limitation because while the term may refer to a process, “intrinsic evidence demonstrates that the term connotes specific structure” onto the claimed GaN transistors. *Pacira*, 2023 WL 3841559, at *9. *Pacira* is instructive in confirming that the term “self-aligned” connotes specific structure onto the claimed GaN transistors and therefore is not a product-by-process limitation. In *Pacira*, the parties disputed whether the term “prepared by a commercial process” as it related to the preparation of

bupivacaine, a numbing agent, encapsulated in multivesicular liposomes (MVLs) to facilitate drug delivery into the body was a product-by-process limitation. 2023 WL 3841559, at *1, *9. The court found that the term connoted specific structure based on disclosure in the specification that, due to the claimed commercial process, the resulting drug product exhibited increased stability, contained less lipid degradation products, and exhibited increased encapsulation. *Id.* at *9. The court also agreed with the patentee’s expert, who opined that the “prepared by a commercial process” term “informs a POSA about the structural properties of the claimed composition.” *Id.* at *10 (internal quotations omitted). In short, both the intrinsic and extrinsic evidence in *Pacira* confirmed that the claimed process imparted structural characteristics onto the claimed composition, resulting in a better product compared to products not prepared by such commercial processes.

Like in *Pacira*, the specification here discloses the structural characteristics imparted by the process on the claimed product. The specification explains that the “primary benefit” of self-alignment is that it “enable[s] the creation of a p-type gate with a minimum critical dimension (“CD”)” and allows ledges to be created “that are symmetric to the gate metal disposed on the p-type gate material.” ’335 patent at 3:65–4:3. As Dr. Schubert explains, a feature’s CD is the smallest possible size of the feature on a wafer. Schubert Decl. at ¶ 79. Using a single photo mask achieves smaller CDs as compared to processes that use multiple photo masks because processes that utilize multiple photo masks inherently involve small deviations in alignment. *Id.* As a result, the smallest dimensions achievable through processes that rely on multiple photo masks are never as small as those achieved through single photo masking and are typically out of alignment, which can result in asymmetrical secondary structures. *Id.* Self-alignment has a distinct structural impact on GaN transistors that differentiate the claimed transistors from the

prior art. By permitting smaller dimensions of integral features such as the gate contact, p-type gate material, and related ledges, self-alignment directly allows GaN transistors to be created with increased efficiency. *Id.* at ¶ 80.

Other than being able to build more transistors into a given area, a smaller transistor has less gate capacitance, which means it can switch faster and less energy is spent in switching. *Id.* Moreover, self-alignment allows a transistor designer to have more flexibility over the features incorporated into that transistor (such as symmetry with respect to p-type gate ledges or sloped or stepped side p-type GaN layer side surfaces) to modulate the electronic properties of the transistor such as leakage current. *Id.* at ¶ 86. A single photo mask therefore permits smaller, better, more efficient GaN transistors to be created than were otherwise possible with prior art, multiple photo masking processes. *Id.* at ¶ 86-87.

Nothing in the intrinsic evidence suggests that the “patentee has demonstrated” that the term “self-aligned” should be interpreted as a mere “process of manufacture.” *In re Nordt*, 881 F.3d at 1374. Thus, although the term “self-aligned” refers to a process, because it also refers to a “structural characteristic” of the claimed product and a POSA would understand the process as imparting structural characteristics onto the claimed GaN transistor, the term must be “interpreted in [its] structural sense.” *Id.* at 1374-1375 (finding the term “injection molded” is not product-by-process limitation because, although the application refers to the term as a process of manufacture, the term connotes structure to claimed knee braces).⁵ Accordingly, the term “self-aligned ledges” is not a product-by-process limitation.

⁵ See also *First Quality Tissue, LLC v. Irving Consumers Prods. Ltd.*, No. 19-cv-428, 2020 WL 3542321, at *3-4 (finding the term “through air dried tissue” was not a product-by-process limitation because it “connotes specific structure”—namely characteristic patterns—on the resulting tissues although it “is certainly a process”); *In re Garnero*, 412 F.2d at 279 (holding

ii. The Process of Self-Alignment Imparts Structural and Functional Differences onto the Claimed GaN Transistors as Compared to the Prior Art

Even assuming that the term “self-aligned ledges” is a product-by-process limitation, Respondents cannot ignore the process limitation in their invalidity arguments because “self-alignment” “imparts ‘structural and functional differences’ distinguishing the claimed product from the prior art.” *Greenliant*, 692 F.3d at 1268. And Respondents cannot satisfy their burden to show otherwise. Indeed, as explained above, both the intrinsic and extrinsic evidence show that the term “self-aligned,” which refers to a process in which a single photo mask is used, imparts both structural *and* functional characteristics onto the claimed GaN transistor to differentiate the claimed transistor from prior art transistors that do not utilize self-alignment.

Self-alignment is a feature that differentiates the claimed transistor from prior art as none of the prior art before the Examiner disclosed self-aligned ledges of a p-type GaN gate material in a GaN transistor that also utilized elongated side surfaces. Moreover, the lack of any such prior art resulted in the issuance of claim 2 of the '335 patent, which depends from claim 1 and adds as its only additional limitation that the ledges are self-aligned, which confirms the patentability of the feature over the prior art.

The “exception to the general rule that the process by which the product is made is irrelevant,” *Greenliant*, 692 F.3d at 1268, is clearly applicable here. Accordingly, the term “self-

that “interbonded one to another by interfusion” connotes structure to a claimed composite and should therefore be considered in the determination of patentability although the term could be construed as both a process and structural limitation); *Hazani*, 126 F.3d at 1479 (“chemically engraved” not a process term); *Genentech, Inc. v. Amgen Inc.*, No. 17-1407-CFC, 2019 WL 2502932, at *8-10 (D. Del. June 17, 2019) (“humanized antibody” not a product-by-process limitation because “humanized” connotes structure to the claimed antibodies).

aligned” is entitled to patentable weight, and Respondents cannot ignore it as irrelevant in attempting to satisfy their burden to prove invalidity by clear and convincing evidence.

E. Side Surface Terms

These terms appear in claims 1 and 5 of the ’335 patent and claim 1 of the ’347 patent.

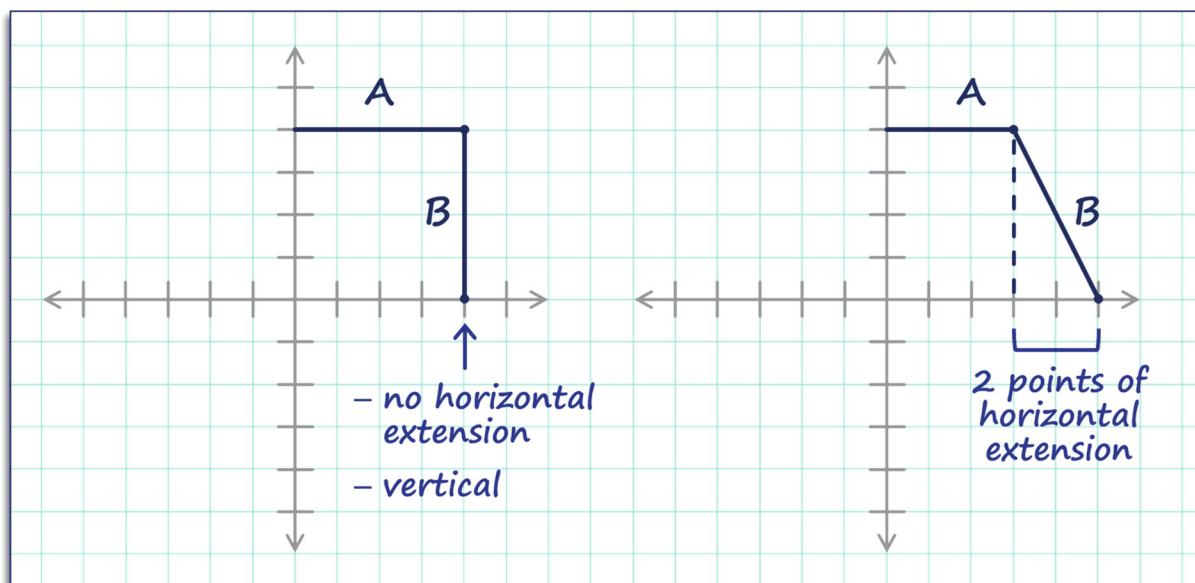
They should be construed as follows:

Term	Construction
“side surfaces extending horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer” ’335 patent, claim 1 “side surfaces that extend horizontally towards the source contact and drain contact, respectively, and contacting the barrier layer” ’335 patent, claim 5	“p-type gate material having side surfaces extending horizontally such that the bottom of the material, which contacts the barrier layer, is wider than the top of the material”
“forming side surfaces of the p-type gate material that extend horizontally towards the source and drain contacts, respectively, and contact the barrier layer” ’347 patent, claim 1	“forming side surfaces of the p-type gate semiconductor material such that the bottom of the material, which contacts the barrier layer, is wider than the top of the material”

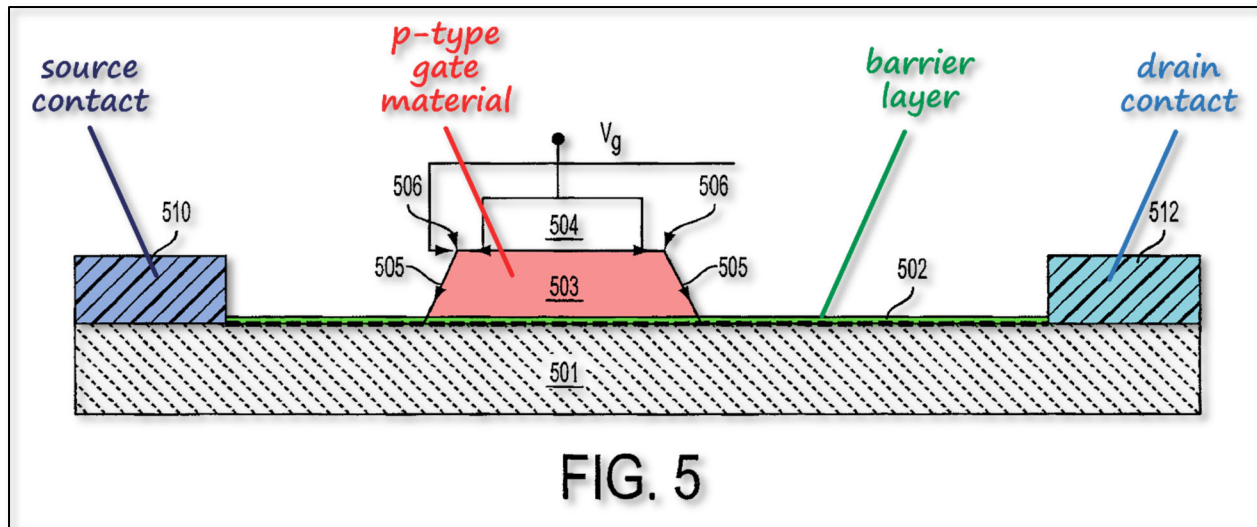
EPC’s construction, with which the Staff agrees, applies the plain meaning of the term “extending horizontally” as defining the side surfaces of the p-type gate material in relation to the barrier layer. Respondents’ construction deviates significantly from plain meaning by requiring three additional limitations neither mandated by the claims nor the rest of the intrinsic evidence: (1) the base of the p-type gate material must be “more than 10% wider than the top of the material,” (2) the side surfaces must be “sloped,” and (3) the sloped portion of those side surfaces must “contact the barrier layer.” This construction must be rejected because it

improperly imports limitations into the claims that would narrow the scope of the claims beyond their plain meaning without any proper directive from the intrinsic evidence.

Put simply, to extend something horizontally means to lengthen or elongate something in the lateral direction. As a result, the endpoint is farther out on a hypothetical x axis than the origin. The figures below depict the difference between a line that does not extend horizontally and one that does. On the left, line B is vertical, having no units of horizontal extension. On the right, line B has two units of horizontal extension.



This concept is easily transposed onto the “side surfaces” that comprise the p-type gate material, which is itself a polygonal structure consisting of a top and a bottom along with the two “side surfaces.” Figure 5 of the ’335 patent, shown below with annotations, depicts an embodiment of this structure.



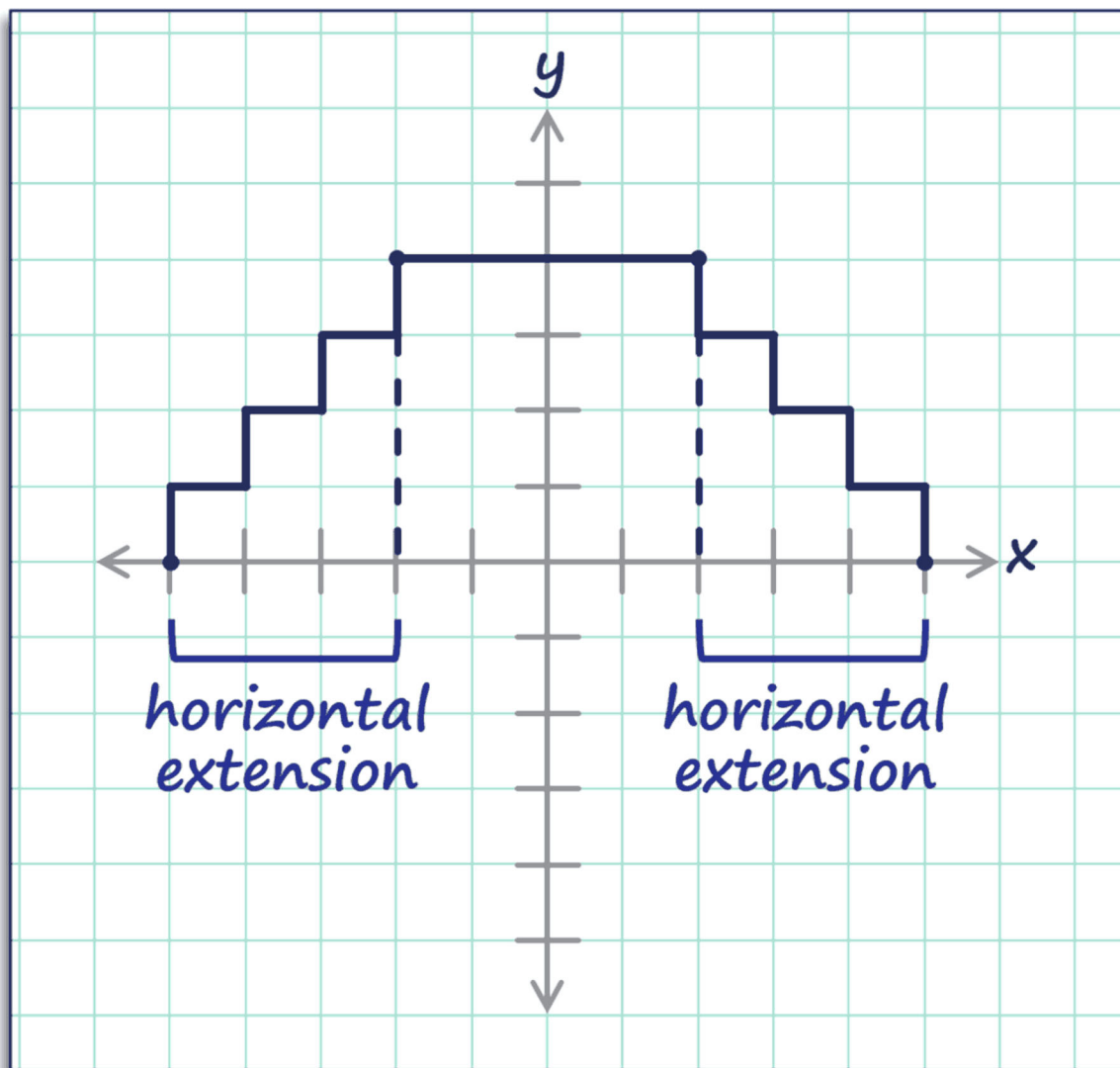
As depicted in this figure, the p-type gate material (503) sits atop the barrier layer (502). Due to the side surfaces of the p-type gate material (505) “extending horizontally towards the source and the drain contacts” (510 and 512, respectively), the result is that the polygonal structure that is the p-type gate material has a bottom that is wider than the top. And, because the bottom of the p-type gate material is formed atop the barrier layer (*see* ’335 patent at claim 1 (requiring “depositing a p-type gate material on the barrier layer”), it is the bottom of the p-type gate material, including where the bottom intersects the “side surfaces,” that naturally must “contact the barrier layer.”

The intrinsic evidence fails to mandate the additional restrictions Respondents’ proposed construction would seek to import into the claims. **First**, the only intrinsic support for Respondents’ proposed construction that the bottom of the p-type gate material must be “more than 10% wider than the top of the material” comes from one embodiment (the fourth) described in the specification. (*See* ’508 patent at 5:23-28.) The claims at issue do not recite any numerical degree of horizontal extension for the claimed side surfaces or threshold values for the p-type gate material width compared to the top. And no such values are **required** by any

intrinsic evidence. Simply put, there is no intrinsic evidence **defining** the horizontal extension of the side surfaces to have a minimum threshold value or unequivocally disavowing from the scope of the claims p-type gate materials where the side surfaces extend horizontally towards the source and drain contacts but where the bottom of those materials is less than 10% wider than the top. *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015) (“The standards for finding lexicography and disavowal are exacting.” (quotations omitted)). Accordingly, Respondents’ proposed additional restriction that the bottom of the p-type gate material must be “more than 10% wider than the top of the material” improperly seeks to import a limitation from the specification into the claim, *Phillips*, 415 F.3d at 1323, and should therefore be rejected.

Second, there is no intrinsic support for Respondents’ proposed additional restriction that the claimed side surfaces must be “sloped.” A sloped side surface is only one example of the type of side surface structure subsumed within the plain meaning of “side surfaces extending horizontally to the source and drain contacts.” For example, side surfaces can be stepped towards the source and drain contacts, not sloped,⁶ as shown in the figure below.

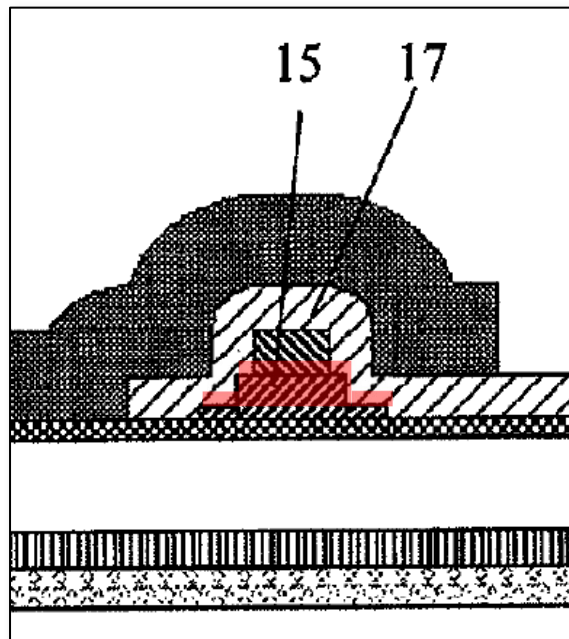
⁶ Although a stepped side surface from the top of the p-type gate material to the bottom can be understood as having a slope (defined by the equation $\text{slope} = \text{rise}/\text{run}$), the individual components of the stepped side surface do not have slopes. The horizontal component has a slope of zero because the numerator in the above-referenced equation is zero. The vertical component has no slope or has a slope that is undefined because the denominator in the above-referenced equation is zero,



This structure, like the sloped structure depicted in the figures of the '335 and '347 patents, exhibits horizontal extension thereby resulting in a p-type gate material having a bottom that is wider than the top.

The figures of the '335 and '347 patent certainly depict sloped, not stepped, side surfaces. But to exclude stepped structures from the scope of the claims would be to limit the claims to the embodiments and thereby import limitations from the specification into the claims in violation of well-settled Federal Circuit precedent. *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d

870, 875 (Fed. Cir. 2004); *see also Liebel-Flarsheim Co. v. Medrad Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004). In addition, limiting the claimed side surfaces to those that are “sloped” would read out embodiments from the ’508 patent, which the ’335 and ’347 patents incorporate by reference. As depicted below, Figure 12 of the ’508 patent depicts a p-type gate material (15, annotated in red) where the bottom is wider than the top but where the side surfaces are stepped, not sloped.



Accordingly, Respondents’ proposal to limit the scope of the claims only to “sloped” side surfaces must be rejected.

Third, there is no intrinsic support for Respondents’ additional restriction that the sloped portion of the claimed “side surfaces” must contact the barrier layer. As discussed above, the claimed “side surfaces” need not be sloped, but can alternatively be stepped towards the source and drain contacts. In such a configuration—even if the stepped side surface overall could be considered sloped—the portion of the side surface that contacts the barrier layer can be entirely vertical (i.e., have no slope), as shown in Figure 12 of the ’508 patent above. Accordingly,

Respondents’ proposal to limit the nature of the claimed barrier layer contact only to the portion of the side surface that is “sloped” must be rejected.

**F. “etching the gate metal and the p-type gate material” /
“etching the gate metal to form a pair of ledges”**

These terms appear in claim 1 of the ’347 patent. They should be construed as follows:

Term	Construction
“etching the gate metal and the p-type gate material”	“etching the gate metal and etching the p-type gate material”
“etching the gate metal to form a pair of ledges”	“performing a process during which gate metal is removed and two ledges are created”

Claim 1 of the ’347 patent is directed to a “method for manufacturing an enhancement-mode GaN transistor, the method comprising,” among other steps, the following three steps:

“forming a photoresist over the gate metal,”

“etching the gate metal and the p-type gate material” to form “side surfaces” (referred to herein as the side-surfaces etching step), and

“etching the gate metal to form a pair of ledges” (referred to herein as the “ledges-etching step”).

EPC’s proposed constructions apply the plain meaning of the term “etching.” By contrast, Respondents again violate basic claim construction principles by importing limitations from the specification into the claims.

First, Respondents improperly import a photoresist “use” step into both etching steps. The claim, however, requires only that the photoresist be formed over the gate metal. Logically, the photoresist must be formed before the gate metal is etched. But as with the photo resistant pattern of claim 1 of the ’508 patent, nothing in claim 1 of the ’347 patent or the intrinsic evidence requires that the photoresist also be used to etch the p-type gate material. Like claim 1 of the ’508 patent directed to application of a photo resistant pattern, claim 1 of the ’347 patent does not specify any limits on when the photoresist is to be used, how it is to be used—in

connection with the etching of the gate metal, the p-type gate material, or both—or when the photoresist should be removed.

To the extent the applicant wanted to require that the photoresist be used as part of both the etching of the gate metal and p-type gate material (as Respondents propose), the applicant knew how to express this requirement as evidenced by the description of embodiments in the specification. For example, the specification describes that “a photoresist 605 is deposited and the gate metal 604 is then etched. The p-type gate material 603 is also etched in a manner that results in the gate structure depicted in FIG. 6B.” ’347 patent at 4:17-20. As reflected in Figure 6B, the photoresist remains present during both the gate metal and p-type gate material etching steps in this embodiment.

But because the applicant chose not to limit the scope of claim 1 by requiring that the photoresist be used in connection with both the side surfaces- and ledges-etching steps, as the applicant described in the embodiments, it would be improper to read the claims as being limited to those embodiments. *Phillips*, 415 F.3d at 1323; *CH₂O*, 2015 WL 12743876, at *9; *BenQ Am*, 2006 WL 6112210 at *15. All that is required is that a photoresist be formed over the gate metal, and that two layers be etched. The specification does not *require* the “use” of the claimed photoresist as part of any of the claimed etching steps. Respondents’ attempt to import such a restriction into the claim violates clear Federal Circuit standards and must be rejected.

Second, Respondents improperly impute an order into the two listed etching steps. Respondents contend that the ledges-etching step occurs only after the side surfaces-etching step. As with claim 1 of the ’508 patent, no order can be imputed into the claimed process limitations other than those dictated by logic or grammar. Similar to claim 1 of the ’508 patent, logic does not dictate that the side-surfaces etching step must occur before the ledges-etching step as

Respondents' proposed construction would require. Indeed, nothing in the claim suggests that either etching step must occur before, during, or after the other.

Had the applicant wanted to impute an order to these etching steps, the applicant knew how to do so based on embodiments described in the specification. Indeed, the specification describes one step of etching the gate metal and p-type gate material to achieve side surfaces and then a "second etching step [that] results in the formation of the ledges 506 of the p-type gate material." *Id.* at 4:23-25. But because the applicant chose not to limit the claimed etching steps to the order described in the embodiments, it would be improper to read that order from the specification into the claim. *Phillips*, 415 F.3d at 1323; *CH₂O*, 2015 WL 12743876, at *9; *BenQ Am*, 2006 WL 6112210 at *14. All that is required is that the gate metal and p-type gate material be etched to form side surfaces and that the gate metal be etched to form ledges. Neither the claim nor the specification ***requires*** that one etching step occur before, during, or after the other. Respondents' attempt to impute an order to the etching steps violates clear Federal Circuit standards and must be rejected.

IV. CONCLUSION

For the reasons stated above, the Court should adopt Complainant's proposed constructions.

WORD COUNT CERTIFICATION

Pursuant to Ground Rules 1.6 and 7.2, I hereby certify that the foregoing Complainant's Opening Claim Construction Brief complies with the word count limitation of Ground Rule 7.2. The brief contains 9,692 words, excluding those portions exempted by Ground Rule 1.6, as calculated by the word count indicated by the word-processing system used to prepare this brief.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing ***Complainant's Opening Claim Construction Brief*** was served upon the following as indicated below on September 22, 2023:

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