

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner

Case IPR2023-01383
U.S. Patent No. 8,404,508

**PATENT OWNER'S SUR-REPLY TO PETITIONER'S REPLY TO
PATENT OWNER'S PRELIMINARY RESPONSE**

I. THE INTRINSIC EVIDENCE REQUIRES A GATE FIRST PROCESS

Despite abundant intrinsic evidence to the contrary, Petitioner argues that the intrinsic evidence of the ‘508 patent does not require the gate structure to be formed before the source and drain. Petitioner is wrong. Both the claims and specification support Patent Owner’s view that the gate structure is formed first.

A. The claims require a gate first process

In analyzing the claims, Petitioner classifies five steps as the so-called gate structure steps, and five steps as the so-called ohmic contact steps. Reply at 2-3. Petitioner then posits that these two sets of steps are independent and self-contained, “and thus logically the gate structure could be formed before, after, or simultaneously with the ohmic source and drain contacts.” Reply at 3. Petitioner makes two critical errors in its analysis.

First, Petitioner does not account for the claimed dielectric layer steps: depositing a dielectric layer; applying a contact photo resistant pattern; etching the dielectric layer to open the drain and source contact area; and removing the contact photo resistant pattern. ‘508 patent at 7:5-9. These steps clearly must occur before the so-called ohmic contact steps. Claim 1 specifies that the dielectric layer is etched to open the drain and source contact area. A POSA would understand that the drain and source contact area is where the drain and source contacts are formed. Therefore, the ohmic contact steps, which culminate with performing

rapid thermal annealing to form Ohmic drain and source contacts, logically must be performed after the dielectric layer steps. *See Mformation Techs., Inc. v. Rsch. In Motion Ltd.*, 764 F. 3d 1392, 1398 (Fed. Cir. 2014).

With this unassailable fact in mind, if the claims require the gate structure to be formed before the dielectric layer, then the gate structure is necessarily formed before the source and drain contacts. Petitioner's second critical error establishes exactly that. Specifically, Petitioner omitted the step of "growing a GaN layer with acceptor type dopants over the barrier layer" from its characterization of the so-called gate structure steps. That GaN layer is part of the gate structure ('508 patent at 3:45-50), and any analysis as to whether the claims are directed to a "gate first" process that does not consider the step of "growing a GaN layer..." is faulty.

The claimed GaN layer is **grown** over the barrier layer. That is, it is part of the epitaxial growth process for the transistor. *See* '508 patent at 3:26-29, 39-41; 6:61-65. A POSA would understand that the epitaxial growth process of the '508 patent occurs before depositing insulation and metal contacts on the surface of the transistor wafer, such as the dielectric layer and ohmic contacts.

Claim 1 then clearly recites that the gate contact layer is deposited on the GaN layer, resulting in a gate contact layer on top of the doped GaN layer, before the dielectric layer has been deposited. Logically, the gate structure would next be formed from the gate contact layer and underlying doped GaN layer using the

applying, etching, and removing steps noted by Petitioner as part of the gate structure steps. And that gate structure would have to be formed before depositing the dielectric layer. Otherwise, the goal of ‘508 patent –creating a self-aligned gate structure which avoids the disadvantages of the prior art (including the desire for reduced cell pitch and manufacturing costs)– would be frustrated, due to the need to engage in additional patterning and etching steps to *somehow* create an opening in the dielectric layer (which has been deposited on top of an incomplete gate structure) to allow the self-aligned gate structure to *somehow* be formed in a way that results in an operational “enhancement mode GaN transistor.”

Accordingly, because claim 1 requires the gate structure to be formed before the dielectric layer is deposited (which in turn occurs before the source and drain are formed), the claim is directed to a “gate first” process.

B. The specification requires a gate first process

The specification also requires a “gate first” process. Like the claims, the specification indicates that p-type material layer 15, from which a portion of the gate structure is formed, is part of the epitaxial structure (and hence, *grown* on top of another layer) depicted in Fig. 3A. *See* ‘508 patent at Fig. 3A, 3:39-40. Thus, it is incontrovertible that the process of forming the gate begins before the process of forming the source and drain contacts.

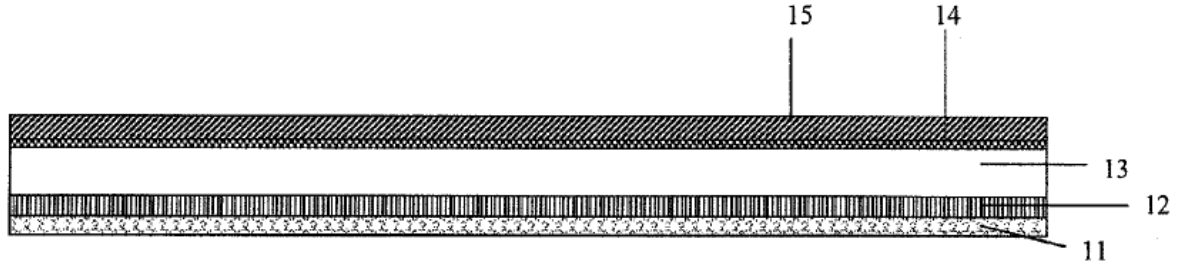


FIG. 3A

After the p-type material layer 15 is grown, a gate metal 17 is deposited or grown atop the p-type material layer 15. '508 patent at 39-41; Fig. 3B.

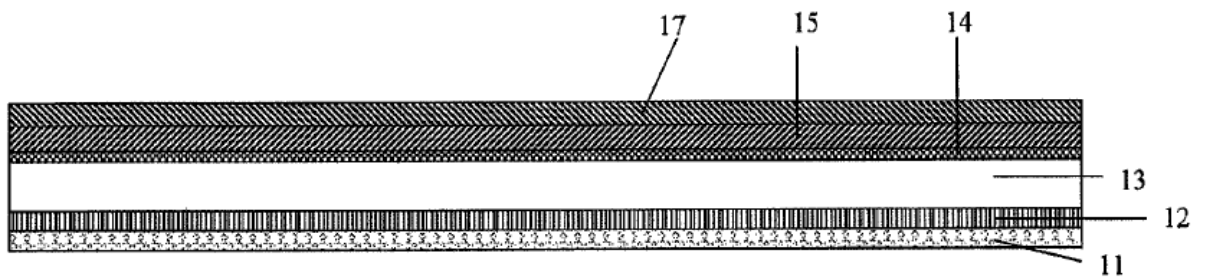


FIG. 3B

Thereafter, as depicted in Fig. 3C and the detailed description (*see* '508 patent at 3:45-56), a self-aligned gate structure is formed.

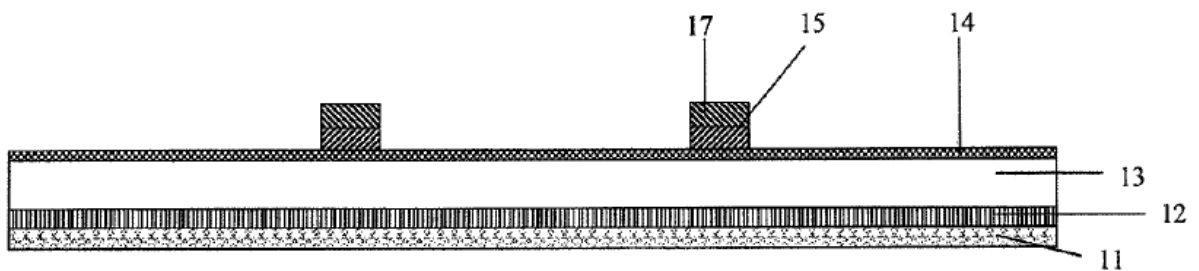


FIG. 3C

Subsequently, dielectric material 18 is deposited. After deposition of the dielectric material 18, a contact photo mask is used to pattern and etch the dielectric material 18, followed by a photoresist strip. The source and drain (20 and 19, respectively) are ultimately formed in the openings left by etching the dielectric material. '508 patent at Figs. 3D, 3E, 3:57-67.

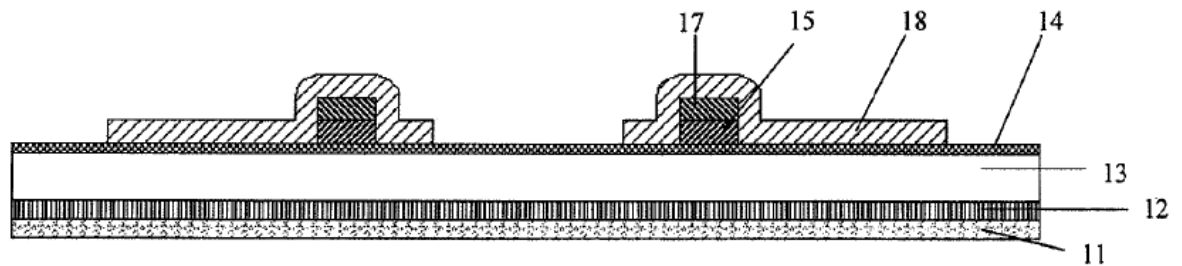


FIG. 3D

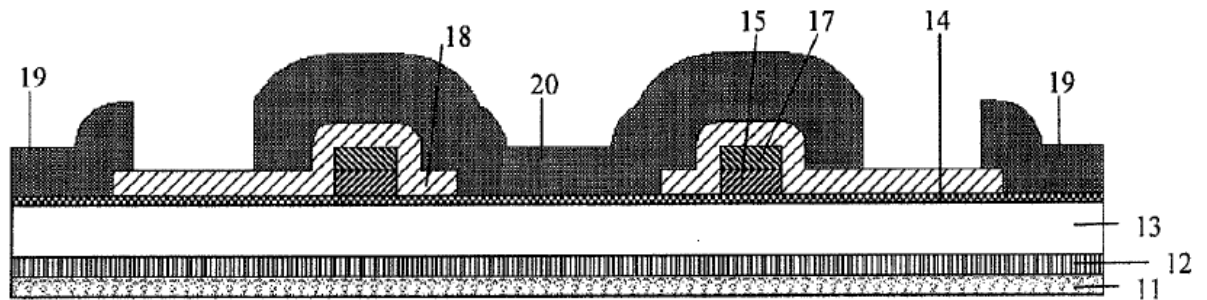


FIG. 3E

The specification does not show, nor does Petitioner explain how, an operational enhancement mode GaN transistor can be made at all, let alone without undue experimentation, if the dielectric layer (which indisputably and logically must be deposited before the source and drain contacts are formed) were to be deposited after the p-type material layer 15 is grown but before the gate structure is

completed. *See Kimberly-Clark Worldwide v. First Quality Baby Products*, 2011 WL 196509 (E.D. Wis. 2011) (finding that logic requires three steps of a method of making refastenable training pants to be performed in the order that they are recited when a party could not show that it was possible to perform the steps out of order). The reality is, it cannot. The logical conclusion is that the specification requires a “gate first” process.

II. PATENT OWNER’S ITC POSITION IS NOT INCONSISTENT

Petitioner argues that Patent Owner’s positions in a parallel ITC investigation are not consistent with the positions Patent Owner takes here. Specifically, Petitioner urges that in the parallel ITC investigation, Patent Owner insists that four of Petitioner’s so-called gate structure steps do not need to be performed in the order listed. Reply at 7-8. That is a misleading oversimplification of Patent Owner’s position in that case.

In the ITC investigation, Patent Owner stresses that a sequential order may be imputed into a method claim, where as a matter of logic, the steps must be performed in the order written. Ex. 1039 at 14. Applying that concept to claim 1 of the ‘508 patent, Patent Owner argues that two of the four identified gate structure steps, the first and fourth recited limitations, are required in the recited order. *Id.* at 15. And other than that, neither the logic nor grammar of the claim

necessitates that the so-called gate structure steps be performed in the recited order.
Id.

That position is wholly consistent with the position Patent Owner takes here. As detailed above in section I, the logic of claim 1 dictates that the gate structure must be formed before the source and drain contacts. Petitioner cannot deny that the claimed dielectric layer must be deposited before the source and drain contacts. And the requirement (explained above in section I) that the doped GaN layer must be grown before the dielectric layer is deposited logically means that the gate structure is formed before the dielectric layer is deposited. As such, per the logic of claim 1, the gate structure must be formed before the source and drain contacts.

Moreover, Petitioner does not explain how an operational enhancement mode GaN transistor can be made if the dielectric layer (which indisputably and logically must be deposited before the source and drain contacts are formed) were to be deposited after the p-type material layer 15 is grown but before the gate structure is completed. Conversely, faced with a similar issue of explaining why certain claim steps are not required to be performed in the recited order, Patent Owner explained (backed up with expert testimony) that it is possible to use a single photo mask to pattern a photoresist, etch one of the underlying materials, remove the photoresist, and use the etched underlying material as a mask for etching a second underlying material. Ex. 1039 at 16. Petitioner's failure in this

regard dooms its position. *See Kimberly-Clark Worldwide v. First Quality Baby Products*, 2011 WL 196509.

III. CONCLUSION

For the foregoing reasons and those submitted in Patent Owner's Preliminary Response, Petitioner's challenge is deficient and no *inter partes* review should be instituted.

Dated: January 23, 2024

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the foregoing
PATENT OWNER'S SUR-REPLY TO PETITIONER'S REPLY TO
PATENT OWNER'S PRELIMINARY RESPONSE is being served on counsel
of record by filing this document through the Patent Review Processing System,
with a copy served via electronic mail to the following email address, as authorized
in the Petition:

Innoscence-EPC-IPRs@finnegan.com

Dated: January 23, 2024

Respectfully submitted,

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