

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE (ZHUHAI) TECHNOLOGY COMPANY, LTD.,
AND
INNOSCIENCE AMERICA, INC.
Petitioner,

v.

EFFICIENT POWER CONVERSION CORPORATION,
Patent Owner.

IPR2023-01383
Patent 8,404,508 B2

Before JON B. TORNQUIST, JEFFREY W. ABRAHAM, and
KIMBERLY McGRAW, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Innoscence (Zhuhai) Technology Company, Ltd. and Innoscience America, Inc., (collectively “Petitioner”) filed a petition for an *inter partes* review (Paper 1 (“Pet.”)) challenging claims 1–5 of U.S. Patent No. 8,404,508 B2 (Ex. 1001 (“the ’508 Patent”)). Efficient Power Conversion Corporation (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). After receiving authorization from the Board, Petitioner filed a Reply to the Preliminary Response (Paper 8 (“Reply”)), and Patent Owner filed a Sur-reply (Paper 10 (“Sur-reply”)).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, we determine that Petitioner has sufficiently shown a reasonable likelihood that it would prevail with respect to at least one claim of the ’508 patent. Accordingly, we institute an *inter partes* review of all challenged claims of the ’508 patent on all grounds asserted in the Petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (stating that a decision to institute is “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

B. Related Matters

The parties identify two matters involving the '508 patent: *Efficient Power Conversion Corporation v. Innoscience (Zhuhai) Technology Co., Ltd*, 2:23-cv-04026-AB-AS (C.D. Cal. May 24, 2023) and *Certain Semiconductor Devices, and Methods of Manufacturing Same and Products Containing the Same*, Inv. No. 337-TA-1366 (USITC May 26, 2023). Pet. 92; Paper 5 (Patent Owner's Mandatory Notices), 2.

C. The '508 Patent (Ex. 1001)

The '508 patent, titled "Enhancement Mode GaN HEMT Device and Method for Fabricating the Same," which issued March 26, 2013 and claims priority to a provisional application filed on April 8, 2009, relates to the field of enhancement mode gallium nitride (GaN) high electron mobility transistor (HEMT) devices and methods of forming such devices. *See* Ex. 1001, codes (45), (54), (57), 2:14–18. The '508 patent explains that "GaN semiconductor devices are increasingly desirable because of their ability to switch at high frequency, to carry large current, and to support high voltages." Ex. 1001, 1:22–24.

Figure 2 of the '508 patent, with color annotations and the labels on the right side provided by Petitioner, is reproduced below. Pet. 8; Ex. 1001, Fig. 2.

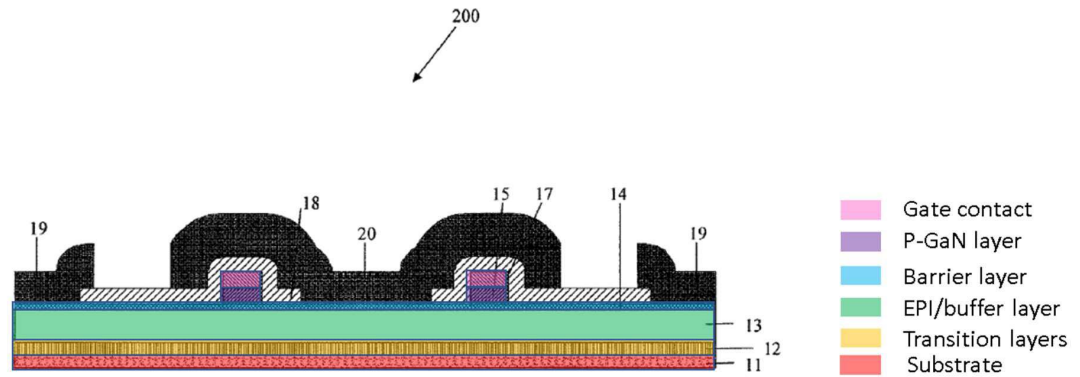


FIG. 2

Figure 2 above illustrates a first embodiment of an enhancement mode GaN HEMT device having silicon substrate 11, transition layers 12, undoped GaN buffer material 13, AlGaN barrier material 14, p-type GaN gate layer 15 (purple), gate metal (pink), dielectric material 18, drain ohmic contact 19, and source ohmic contact 20. Ex. 1001, 2:25–27, 3:10–25.

The process for forming the device according to the first embodiment is schematically illustrated in Figures 3B–3E, shown below, with Petitioner's color annotations added to Figures 3B and 3C. Ex. 1001, 2:28–30; Pet. 9–10.

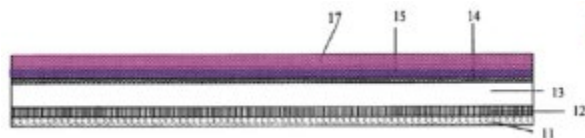


FIG. 3B

Figure 3B above shows gate metal 17 (pink) deposited on an EPI structure having p-type GaN gate layer 15 (purple). Ex. 1001, 3:26–29, 3:39–40.

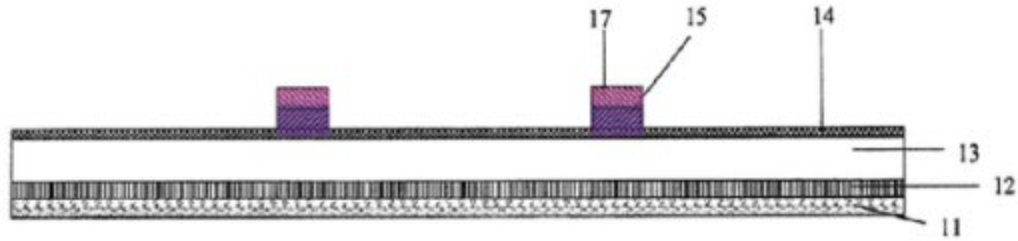


FIG. 3C

Figure 3C above shows the structure resulting from a single photo mask used to pattern and etch gate metal 17 (pink) and p-type GaN gate layer 15 (purple). Ex. 1001, 3:45–47.

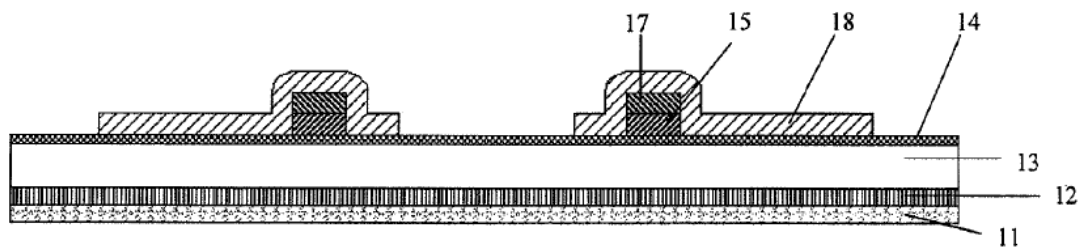


FIG. 3D

The '508 patent states that the structure shown in Figure 3D above is formed by depositing dielectric material 18 and then, after deposition of the material, a contact photo mask is used to pattern and etch the dielectric material 18, followed by a photoresist strip. Ex. 1001, 3:57–61.

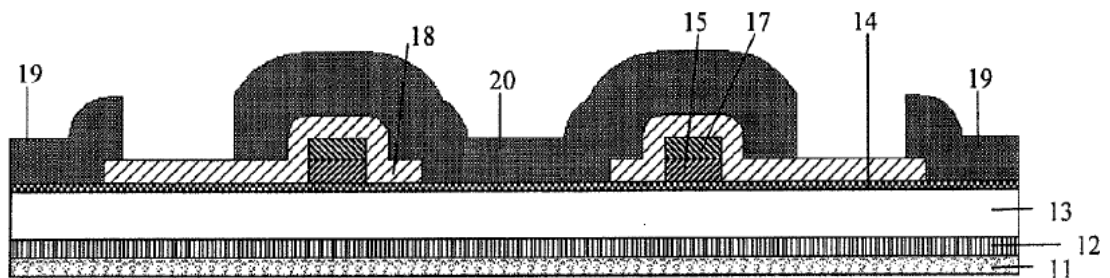


FIG. 3E

The '508 patent states, referring to Figure 3E above, ohmic contact metal is deposited, after which, a metal mask is used to pattern and etch the

ohmic contact metal, resulting in drain ohmic contact 19 and source ohmic contact 20. Ex. 1001, 3:62–67. Rapid thermal anneal is performed to form ohmic contacts to AlGaN/GaN 2DEG. *Id.* at 3:67–4:2.

D. Illustrative Claims

Petitioner challenges claims 1–5 of the '508 patent. Claims 1, 4, and 5 are independent and are reproduced below.

Claim 1: [1pre] A method of forming an enhancement mode GaN transistor, the method comprising:

- [1a] nucleating and growing transition layers on a substrate;
- [1b] growing an III Nitride EPI layer over the transistor layers;
- [1c] growing an III Nitride barrier layer over the EPI layer;
- [1d] growing a GaN layer with acceptor type dopants over the barrier layer;
- [1e]:
 - [1e1] depositing a gate contact layer on the doped GaN layer;
 - [1e2] applying a *gate photo resistant pattern*;
 - [1e3] etching away the gate contact layer outside the gate region;
 - [1e4] etching away the doped GaN layer, except a portion of the doped GaN layer beneath the gate contact;
 - [1e5] removing the gate photo resistant pattern;
- [1f]:
 - [1f1] *depositing a dielectric layer*;
 - [1f2] applying a contact photo resistant pattern;
 - [1f3] *etching the dielectric layer to open the drain and source contact area*;
 - [1f4] removing the contact photo resistant pattern;
- [1g]:
 - [1g1] depositing an Ohmic contact metal;
 - [1g2] applying a *metal photo resistant pattern*;

- [1g3] etching the Ohmic contact metal;
- [1g4] removing the metal photo resistant pattern; and
- [1g5] performing rapid thermal annealing to form Ohmic drain and source contacts.

Ex. 1001, 6:59–7:15 (labels and formatting added to correspond with Petitioner’s designation of claim limitations (*see, e.g.,* Pet. 25–35; Claim Appendix)) (emphasis added).

Claim 4: [4pre] A method of forming an enhancement mode GaN transistor, the method comprising:

- [4a] nucleating and growing transition layers on a substrate;
- [4b] growing an InAlGaNEPI layer over the transistor layers;
- [4c] growing an InAlGaN barrier layer over the InAlGaNEPI layer;
- [4d] growing an InAlGaN layer with acceptor type dopants over the InAlGaN barrier layer;
- [4e] growing a GaN layer with acceptor type dopants over the doped InAlGaN layer;
- [4f]:
 - [4f1] depositing a gate contact layer on the doped GaN layer
 - [4f2] *applying a gate photo resistant pattern;*
 - [4f3] etching away the gate contact layer outside the gate region;
 - [4f4] etching away the doped GaN layer and the doped InAlGaN layer, except for portions of the doped GaN layer and the doped InAlGaN layer beneath gate contact;
 - [4f5] removing the gate photo resistant pattern;
- [4g]:
 - [4g1] depositing a dielectric layer;
 - [4g2] applying a contact photo resistant pattern;
 - [4g3] etching the dielectric layer to open the drain and source contact area;
 - [4g4] removing the contact photo resistant pattern;

[4h]:

- [4h1] depositing an Ohmic contact metal;
- [4h2] *applying a metal photo resistant pattern;*
- [4h3] etching the Ohmic contact metal;
- [4h4] removing the metal photo resistant pattern; and
- [4h5] performing rapid thermal annealing to form Ohmic drain and source contacts.

Ex. 1001, 7:21–8:7 (labels and formatting added to correspond with Petitioner’s designation of claim limitations (*see, e.g.,* Pet. 66–74; Claim Appendix)) (emphasis added).

Claim 5: [5pre] A method of forming an enhancement mode GaN transistor, the method comprising:

- [5a] nucleating and growing transition layers on a substrate;
- [5b] growing an InAlGaNEPI layer over the transistor layers;
- [5c] growing an AlGaNEPI barrier layer over the InAlGaNEPI layer;
- [5d] growing an AlGaNEPI layer with acceptor type dopants over the AlGaNEPI barrier layer;
- [5e] growing a GaN layer with acceptor type dopants over the doped AlGaNEPI layer;
- [5f]:
 - [5f1] depositing a gate contact layer on the doped GaN layer
 - [5f2] *applying a gate photo resistant pattern;*
 - [5f3] etching away the gate contact layer outside the gate region;
 - [5f4] etching away the doped GaN layer, except for portions of the doped GaN layer and the doped AlGaNEPI layer beneath gate contact;
 - [5f5] removing the gate photo resistant pattern;
- [5g]:
 - [5g1] applying another photo resistant pattern;

[5g2] etching the doped AlGa_N layer such that the doped AlGa_N extends outside the gate region towards the drain;

[5g3] removing the photo resistant pattern;

[5h]:

[5h1] depositing a dielectric layer;

[5h2] applying a contact photo resistant pattern;

[5h3] *etching the dielectric layer to open the drain and source contact area;*

[5h4] removing the contact photo resistant pattern;

[5i]:

[5i1] depositing an Ohmic contact metal;

[5i2] applying a *fourth photo resistant pattern;*

[5i3] etching the Ohmic contact metal

[5i4] removing the fourth photo resistant pattern; and

[5i5] performing rapid thermal annealing to form Ohmic drain and source contacts.

Ex. 1001, 8:8–39 (labels and formatting added to correspond with Petitioner’s designation of claim limitations (*see, e.g.,* Pet. 78–89; Claim Appendix)) (emphasis added).

E. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–5 are unpatentable based on the following challenges:

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1–3	103	Yoshida, ² Beach, ³ Sheppard ⁴
1–4	103	Hikita-347, ⁵ Beach, Sheppard
5	103	Hikita-023 ⁶ , Beach, Sheppard

Petitioner relies on the declaration of James Richard Shealy, Ph.D. (Ex. 1003).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have had a “at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (Sept. 16, 2011), includes revisions to Section 103 that became effective on March 16, 2013. Because the challenged claims issued from an application filed before March 16, 2013, we apply the pre-AIA law to the challenges. *See* Ex. 1001, code (30).

² JP H11-261053, published Sept. 24, 1999 (Ex. 1004, pp. 8–11 (original language), pp. 1–7 (certified English translation), p. 12 (certification “Yoshida”)). All references are to the English translation portion of Ex. 1004.

³ US 2007/0057624, published June 23, 2005 (Ex. 1005, “Beach”).

⁴ US 7,238,560, issued July 3, 2007 (Ex. 1006, “Sheppard”).

⁵ US Pub. App. No. 2006/0273347, published Dec. 7, 2006 (Ex. 1007, “Hikita-347”).

⁶ US Pub. App. No. 2008/0079023, published Apr. 3, 2008 (Ex. 1008, “Hikita-023”).

operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa.”

Pet. 11 (citing Ex 1003 ¶ 69). Patent Owner does not challenge Petitioner’s definition or offer its own. *See generally*, Prelim. Resp.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner’s proposal regarding the level of ordinary skill in the art. Based on our review of the ’508 patent and the prior art of record, we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the ’508 patent and the prior art.

B. Claim Construction

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). In this context, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (citations omitted) (en banc).

The claims of the ’508 patent are directed to methods of forming an enhancement mode GaN transistor. As a general rule, unless the steps of a method claim actually recite an order, the steps are not ordinarily construed to require one. *Mformation Techs., Inc. v. Research in Motion Ltd.*, 764 F.3d 1392, 1398 (Fed. Cir. 2014). However, a claim requires an ordering of steps when the claim language, as a matter of logic or grammar, requires that the steps be performed in the order written, or the specification directly or implicitly requires an order of steps. *Id.*; *see also Function Media, LLC v. Google, Inc.*, 708 F.3d 1310, 1320 (Fed. Cir. 2013) (concluding that a claim

that recites “processing” an “electronic advertisement” necessarily indicates that “the creation of the ad must happen before the processing begins”).

Although the parties state no claim construction is required (Pet. 10; Prelim. Resp. 8), the parties dispute whether the claims require that a gate structure be formed before the source and drain contacts.

For example, Patent Owner asserts that the challenged claims require that the gate structure be formed before the source and drain contacts because the claims require the dielectric layer to be deposited before forming the source and drain contacts, and if the dielectric layer were deposited before forming the gate, an opening in the dielectric layer would be necessary to result in an operating transistor. Prelim. Resp. 6–7. Petitioner asserts that the gate structure steps and ohmic contact steps are “independent and self-contained” and that the gate structure could be formed before, after, or simultaneously with the ohmic source and drain contacts. Reply 3.

At this stage of the proceeding, based on the present record, we determine that the claims require that the dielectric layer steps of [1f] must occur before the ohmic contact steps of [1g] but that the claims do not require that the gate structure be formed before the source and drain contacts.

Step [1f] recites depositing a dielectric layer; applying a contact photo resistant pattern; etching the dielectric layer to open the drain and source contact area; and removing the contact photo resistant pattern. Ex. 1001, 7:5–9. Thus, it appears that the drain and source contact area recited in step [1f3] is the area where the drain and source contacts are formed. The ohmic contact steps of [1g] are directed to forming the drain and source contacts. As a matter of logic, the drain source contact area must be opened before the drain and source contacts are formed. As such, the dielectric layer steps of

[1f]—which require etching a layer to open the drain and source contact area and removal of the contact photo resistant pattern—must be performed before the ohmic contact steps of [1g] to form the Ohmic drain and source contacts are performed. Petitioner does not dispute this construction. *See* Reply 1–9 (disputing whether the gate must be formed before the source and drain, but not disputing that the dielectric layer [1f1] must be deposited before forming the source and drain contacts [1g]).

The claims, however, do not appear to contain any language that requires that the gate structure be formed before the drain and source are formed. A review of the claim language shows that the gate structure and the ohmic contacts are separate components, and there does not to be any apparent order requirement set forth in the claims.

Patent Owner points to the claimed dielectric layer steps to support its contention that the claims require that the gate be formed before the source and drain. *See* Prelim. Resp. 6; Sur-reply 1–2. As noted above, we agree that the dielectric layer steps of [1f] must be performed before the source and drain are formed as set forth in the steps of [1g]. However, based on the record before us, we do not see any limitations in the claim that *require* the gate structure steps of [1e] be performed in any order in relation to the dielectric layer steps.

Patent Owner contends that because the claims do not specify that the dielectric layer is etched to form an opening for the gate structure, a POSITA would understand the claims to require that the claimed gate structure was formed before the claimed source and drain contacts. Prelim. Resp. 6. Patent Owner asserts that if the dielectric layer were formed before the gate structure, an opening in the dielectric layer would be necessary to result in an operating transistor. *Id.* at 6–7. Patent Owner also argues that

because the claims state that the gate contact layer is deposited on the GaN layer, the gate structure must be formed before depositing the dielectric layer. Sur-reply 2. Patent Owner contends that unless the gate layer is deposited before the dielectric layer, the goals of the '508 patent (e.g., reducing cell pitch and manufacturing costs) would be frustrated if additional patterning and etching steps were required to open the dielectric layer to allow the self-aligned gate structure to *somehow* be formed in a way that results in an operational enhancement mode GaN transistor. *Id.* at 3.

Patent Owner also asserts that the Specification requires a gate first process because the Specification shows the p-type layer (which forms part of the gate structure) is grown on top of the epitaxial structure and therefore “it is incontrovertible that the process of forming the gate begins before the process of forming the source and drain contacts.” Sur-reply 3; *see also id.* at 3–5 (citing, *inter alia*, Ex. 1001, Figs. 3A–3D). Patent Owner asserts that the Specification does not show how to form a functional transistor without undue experimentation if the dielectric layer is deposited after the p-type material is grown but before the gate structure is completed. *Id.* at 5–6.

Patent Owner’s arguments are not persuasive at this stage of the proceeding, based on the present record. The Specification does not expressly *require* that the gate structure be formed before the source and drain. Although the Specification does describe some gate-first embodiments, we are not inclined to limit the claims to certain embodiments disclosed in the Specification, based on the present record. *Phillips*, 415 F.3d at 1323; *see* Reply, 3–4. In addition, Patent Owner does not sufficiently address Petitioner’s argument that the claims are open-ended because they use the word “comprising,” and therefore the claims do not exclude any additional steps such as forming an opening for the gate

structure in the dielectric layer. *See* Pet. Reply at 3–4. The open-ended nature of the claims as written casts doubt on Patent Owner’s argument that the doped GaN layer must be grown before the dielectric layer is deposited, or that the gate layer must be deposited before the source and drain contacts layer.

As such, based on the present record and for purposes of this Decision, we determine the claims do not require that a gate structure be formed before the source and drain contacts. The parties are invited to further address this issue at trial if they choose. For the purposes of this decision, no additional express claim construction is required. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating that only “those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy”).

C. Overview of Asserted Prior Art

1. Yoshida (*Ex. 1004*)

Yoshida discloses novel GaN-based HEMT structures that can operate under the application of high voltages and at higher speeds. *Ex. 1004* ¶¶ 1, 8. Yoshida depicts the basic structure of its claimed invention in Figure 1, reproduced below.

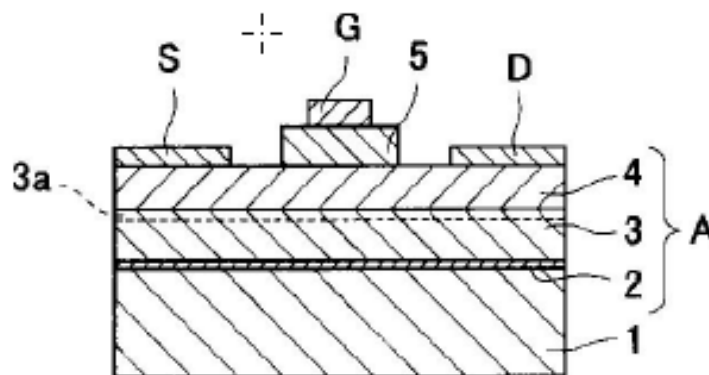


Figure 1 of Yoshida shows a cross-sectional view of a transistor having a stacked structure comprising buffer layer 2, i-type semiconductor layer 3, and n-type semiconductor layer 4 formed on semi-insulating substrate 1.

Ex. 1004 ¶ 10. Figure 1 also shows gate electrode G on p-type semiconductor layer 5⁷, as well as source electrode S and drain electrode D, all formed on n-type semiconductor layer 4. Ex. 1004 ¶ 10.

Yoshida discloses methods for fabricating the structure shown in Figure 1, including deposition and etching conditions. Ex. 1004 ¶¶ 19–23. In particular, Yoshida discloses the deposition of a GaN buffer layer 2 on semi-insulating substrate 1, followed by deposition of i-type GaN layer 3, n-type AlGaIn layer 4, and p-type GaN layer 5. *Id.* ¶¶ 20–21, 25. A dry etching process is used to etch away p-type GaN layer 5, except where the gate electrode is to be loaded, to expose underlying layer 4. *Id.* ¶ 22. “An SiO₂ film was then deposited by plasma CVD to cover the entire surface, and after patterning with photoresist, the area including the part where the gate electrode was to be loaded was masked, [leaving] the portion where the source and drain electrodes were to be loaded open.” *Id.* (bracketed material in English translation). Metal Al is then deposited on the exposed layer 4 to load source electrode S and drain electrode D. *Id.* Lastly, “after etching away the masking and opening the SiO₂ film beneath it, the source electrode S and drain electrode G locations were masked with SiO₂ film, Au was deposited in the opening portions, and gate electrodes G were loaded above the p-type GaN layer 5 to fabricate the HEMT shown in Fig. 1.” *Id.* ¶ 23.

⁷ Yoshida’s identification of the p-type GaN layer as element “6” instead of element “5” in paragraph 21 appears to be a typographical error. *Compare* Ex. 1004 ¶ 21 *with* Ex. 1004 ¶ 25, Figure 1.

2. *Beach (Ex. 1005)*

Beach is a PCT Publication titled “III-Nitride Device Passivation and Method” that published June 23, 2005. Ex. 1005, code (12), (43), (54).

Beach is directed to forming an “ohmic contact on a semiconductor device in the III-nitride material system using a non-stoichiometric, highly doped GaN layer deposited before the ohmic contact is deposited.” *Id.* ¶ 17. The highly doped GaN layer forms a very low resistive contact with the ohmic material used for the ohmic contact due to a tunneling effect at the interface between the highly doped GaN layer and the ohmic contact material. *Id.* The presence of the highly doped GaN layer permits the ohmic contact to be formed with little or no damage to the semiconductor surface device. *Id.*

3. *Sheppard (Ex. 1006)*

Sheppard is a US patent issued July 3, 2007 titled “Methods of Fabricating Nitride-based transistors with a Cap Layer and a Recessed Gate.” Ex. 1006, code (12), (45), (54). Sheppard states that its invention relates to, *inter alia*, methods of fabricating high electron mobility transistors (HEMTs), including forming a channel layer, forming a barrier layer on the channel layer, forming a cap layer on the barrier layer, and forming a gate recess in the cap layer that extends to the barrier layer. *Id.* at 2:30–35. The barrier, channel, and cap layers with the gate recess are annealed and then a gate contact is formed in the annealed gate recess. *Id.* at 2:35–38. Sheppard further states that annealing the gate recess prior to forming a gate contact, such as a Schottky contact, may reduce gate leakage. *Id.* at code (57).

4. *Hikita-347 (Ex. 1007)*

Hikita-347 is a US Patent Publication titled “Field-Effect Transistor and Method for Fabricating the Same,” that published on December 7, 2006. Ex. 1007, code (12), (43), (54). Hikita-347 states that one object of the invention is “to provide a field-effect transistor of normally OFF type nitride semiconductor, which is applicable to a power transistor and allows a sufficient large current density, and a method for fabricating the field-effect transistor.” *Id.* ¶ 8. The transistor comprises a substrate, a first, second, and third nitride semiconductor layer, a gate electrode formed on or above the third nitride semiconductor layer, and source and drain electrodes formed on or above the second nitride semiconductor layer so as to be located on both sides of the gate electrode, when viewed from the top. *Id.* ¶ 9.

5. *Hikita-023 (Ex. 1008)*

Hikita-023 is a US Patent Publication titled “Nitride Semiconductor Device and Method for Fabricating the Same,” that published on April 3, 2008. Ex. 1007, code (12), (43), (54). Hikita-023 states that one object of the invention is to prevent the current collapse caused in normally-off type nitride semiconductor devices applicable to power transistors. *Id.* ¶ 14. Hikita-023 discloses a nitride semiconductor device having a substrate, a first, second, and third nitride semiconductor layer, a gate electrode formed on the third nitride semiconductor layer, and source and drain electrodes formed in the regions located on both sides of the gate electrode, and the third nitride semiconductor layer has a thickness greater in a portion below the gate electrode than in a portion below the side of the gate electrode. *Id.* ¶ 16.

*D. Alleged Obviousness of Claims 1–3
over Yoshida, Beach, and Sheppard*

Petitioner contends that independent claim 1 and dependent claims 2–3 of the '508 patent are unpatentable as obvious over Yoshida, Beach, and Sheppard. Pet. 13–42.

1. Claim 1

a) Preamble and Steps [1a]–[1d]

Petitioner asserts that Yoshida teaches a method of forming an enhancement mode transistor and the nucleating/growing steps recited in claim elements [1a]–[1d]. Pet. 25–30. Petitioner also asserts that to the extent Yoshida does not explicitly disclose providing *multiple* transition layers as recited in step [1a], Sheppard's disclosure of a transistor with multiple transition layer renders this obvious. Pet. 27.

Patent Owner does not dispute Petitioner's assertions. We have reviewed Petitioner's arguments and evidence and determine Petitioner has shown sufficiently that Yoshida discloses the preamble and the limitations recited in steps [1b]–[1d] and that Yoshida in combination with Sheppard teaches the limitations of step [1].⁸

⁸ Because we determine Petitioner sufficiently shows that Yoshida discloses the material recited in the preamble, we need not determine whether the preamble is limiting.

b) Steps [1e]–[1g]

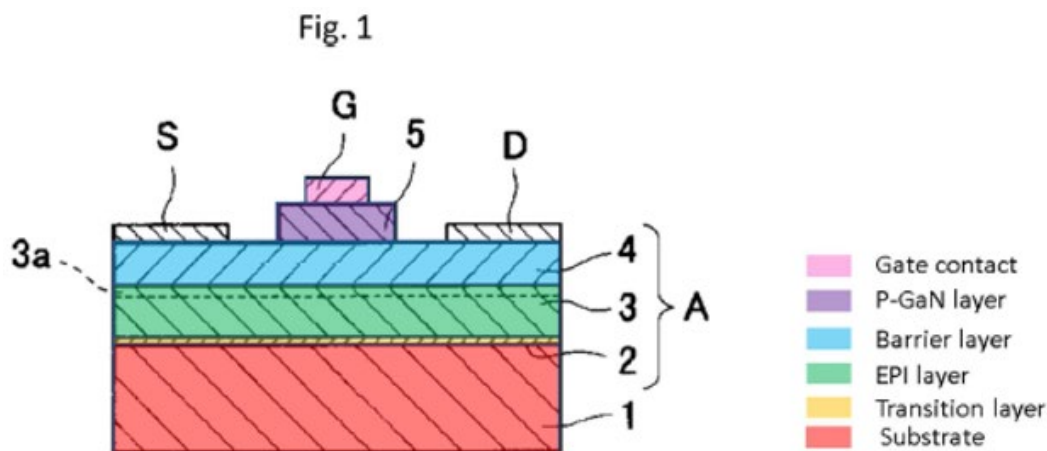
In general, steps [1e]–[1g] require:

- depositing a gate contact layer on the doped GaN layer, applying a particular pattern (i.e., a “*gate photo resist pattern*”), etching the gate contact layer, etching an underlying layer, and removing the gate photoresist pattern (steps [1e1]–[1e5] (“the gate structure steps”⁹));
- depositing a dielectric layer, applying a particular pattern (i.e., a “*contact photo resistant pattern*”), *etching the dielectric layer to open drain and source contact areas*, and removing the contact photo resist pattern (steps [1f1]–[1f4]) (“the dielectric layer steps”)); and
- depositing an Ohmic contact metal, applying a particular pattern (i.e., a “*metal photo resistant pattern*”), etching the Ohmic contact metal, removing the metal photo resistant pattern, and performing rapid thermal annealing to form Ohmic drain and source contacts (steps [1g1]–[1g5] (“the “ohmic contact steps”¹⁰)).

Petitioner asserts that Yoshida in view of Beach renders obvious these limitations. Yoshida’s Figure 1, with color annotations and labels on the right provided by Petitioner, is reproduced below.

⁹ Petitioner refers to claim elements [1e1]–[1e5] as the “gate structure steps” and contends a “single mask” is used to etch both the gate contact layer and an underlying layer. *See, e.g.,* Reply Br. 2.

¹⁰ Petitioner refers to claim elements [1g1]–[1g5] as the “ohmic structure steps.” *See* Reply Br. 2–3.

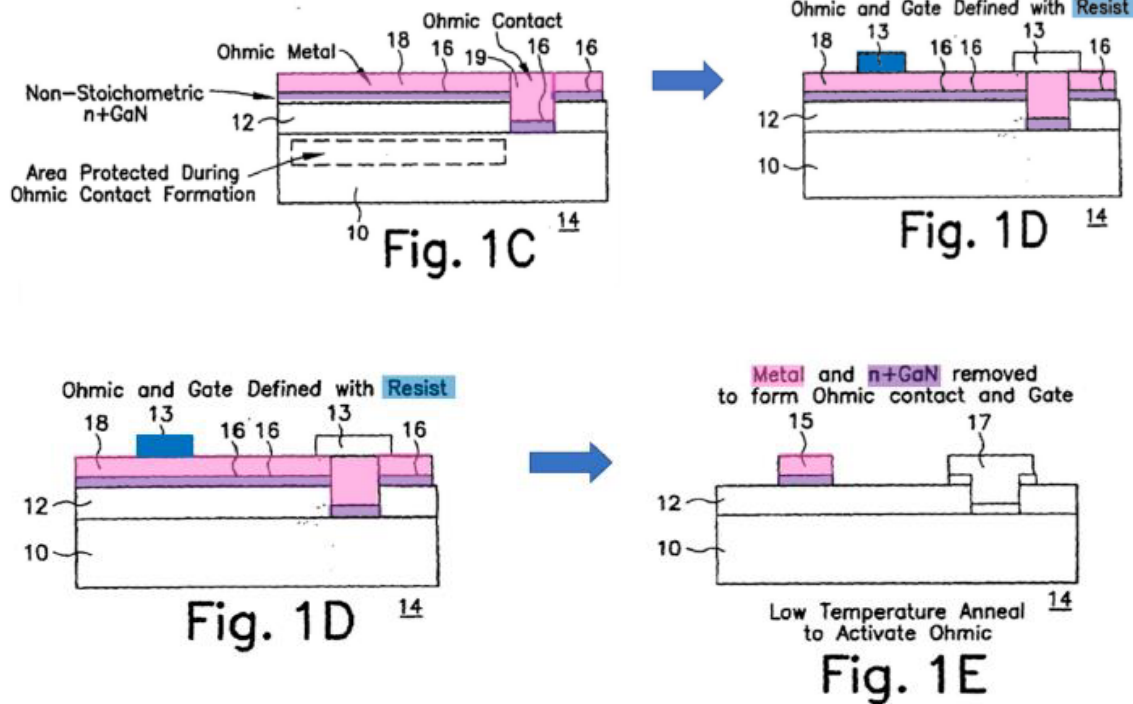


Annotated Figure 1 of Yoshida shows a cross-sectional view of a transistor. *See* Pet. 14; Ex. 1004 ¶ 19.

With respect to the gate structure steps of [1e], Petitioner asserts that Yoshida teaches forming gate electrode G (gate contact) over p-GaN layer 5 (doped GaN layer) as required by step [1e1]. Pet. 30–31 (citing Ex. 1004 ¶¶ 9, 16, 23). In particular, Petitioner contends that Yoshida discloses etching away the p-GaN layer “except where the gate electrode was to be loaded” and then loading the gate electrode above the GaN layer. Pet. 31 (citing Ex. 1004 ¶¶ 22–23).

Petitioner acknowledges that Yoshida does not use a single mask (i.e., the “gate photo resistant pattern” of [1e2]) to etch both layers or show that p-GaN layer and gate electrode have the same width. *See* Pet. 30–31 (citing Ex. 1004 ¶¶ 22, Fig. 1). Petitioner, however, asserts that it would have been obvious for a POSITA to have used Beach’s single mask to etch both the doped GaN layer (purple) and the gate contact layer (pink). *See* Pet. 31–32.

Beach’s Figures 1C, 1D, and 1E, are reproduced below with Petitioner’s annotations added. Pet. 31–33.



Beach Figures 1C (top right), 1D (top right and bottom left), and 1E (bottom right) with color coding added by Petitioner, are a series of cross-sectional views of a III-nitride device illustrating a series of steps in a process for forming the III-nitride device. Pet. 32–33; Ex. 1005 ¶¶ 40–49.

Petitioner asserts that Beach discloses a method of forming a self-aligned gate and doped GaN layer using the steps of [1e], including, depositing a gate contact layer (ohmic material 18-pink) on doped GaN layer 16 (purple). Pet. 31–32. Petitioner asserts Beach discloses step [1e2], applying gate photo resistant pattern 13 (blue) to the structure (Pet. 32 (citing Ex. 1005 ¶ 47, Fig. 1D)), then step [1e3], etching away gate contact layer (layer 18 – pink) outside the gate region and step [1e4], and etching away the doped GaN layer (layer 16 – purple), except a portion of the doped GaN layer (purple) beneath the gate contact (pink). Pet. 33 (citing Ex. 1005 ¶ 47).

Petitioner contends that using Beach's single mask process to etch both the gate contact layer (pink) and the doped GaN layer (purple), instead of Yoshida's process which requires separate masks to etch each of the two layers to form the gate, is simpler, reduces costs, and improves the gate's alignment. Pet. 21–22 (citing Ex. 1003 ¶ 126; Ex. 1005 ¶ 47).

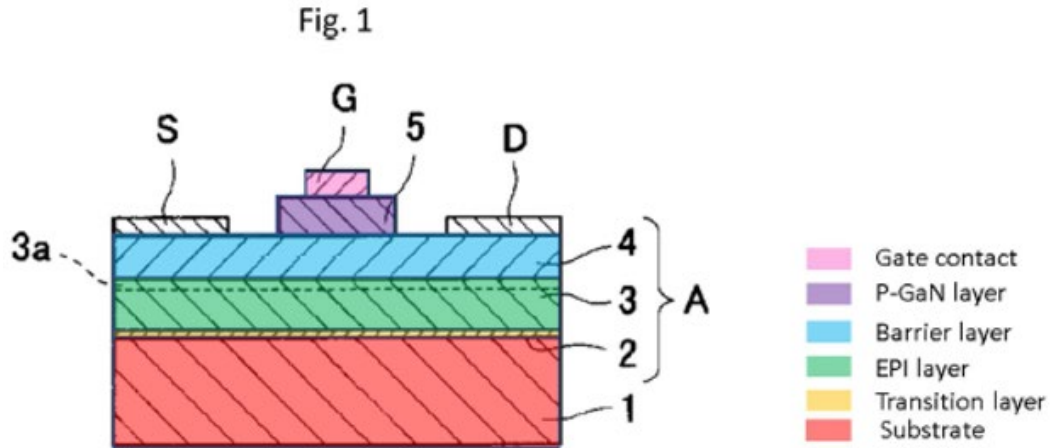
With respect to step [1f], Petitioner relies on the teachings of Yoshida. Pet. 34–35. In particular, Petitioner asserts that Yoshida discloses:

- after etching away the p-type GaN layer (purple layer 5¹¹), depositing an SiO₂ film (a dielectric layer) to cover the entire surface (Pet. 34; Ex. 1004 ¶ 22) (step [1f1]);
- patterning with a photoresist to mask the part where the gate electrode is to be loaded but leaving the portion where the source and drain electrodes are to be loaded (Pet. 34; Ex. 1004 ¶ 22) (step [1f2]); and
- etching away the masking and opening the SiO₂ film to etch the dielectric layer to open the drain and source contact area and remove the contact photoresistant pattern (Pet. 34–35; Ex. 1004 ¶¶ 22–23) (steps [1f3]–[1f4]).

See id.

Yoshida's Figure 1, with color annotations and labels on the right provided by Petitioner, is again reproduced below for reader convenience.

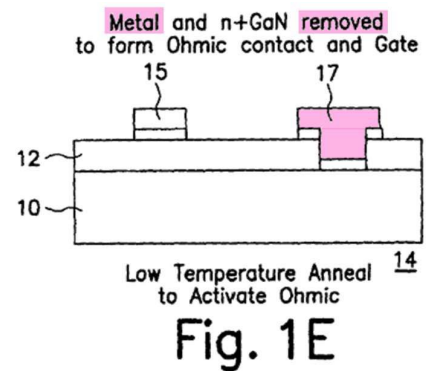
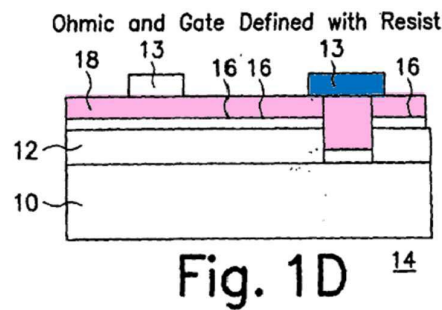
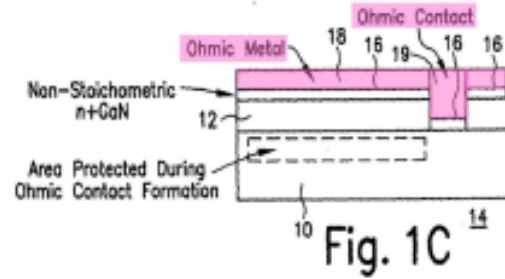
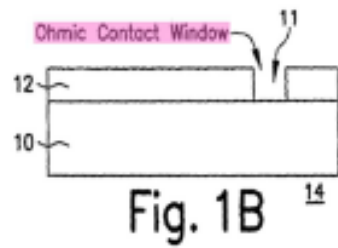
¹¹ Although Petitioner does not include the color labels when discussing Yoshida's asserted disclosure of steps 1[1f], the Board includes the color labels for clarity. *See* Pet. 26 (providing color annotations to identify the layers of Yoshida Figure 1).



Annotated Figure 1 of Yoshida shows a cross-sectional view of a transistor. *See* Pet. 14; Ex. 1004 ¶ 19.

With respect to the ohmic contact steps of [1g], Petitioner asserts Yoshida discloses step [1g1] by disclosing the deposition of metal Al (an ohmic contact metal) on n-type semiconductor layer 4 (blue). Pet. 35 (citing Ex. 1004 ¶¶ 10, 22; Ex. 1003 ¶ 135). Petitioner admits that Yoshida does not teach steps [1g2]–[1g5], which require applying a metal photo resistant pattern, etching the ohmic contact metal, removing the metal photo resistant pattern, and performing rapid thermal annealing to form Ohmic drain and source contacts, but contends that Beach renders obvious use of these steps to form Yoshida’s ohmic source and drain contacts. Pet. 36–39.

In particular, Petitioner points to Beach Figures 1B, 1C, 1D and 1E. Pet. 36–37. Beach’s Figures 1B–1E, with Petitioner’s annotations (which differ from the annotations shown above) are reproduced below.



Beach Figures 1B (top left), 1C (top right), 1D (bottom left), and 1E (bottom right) with color coding added by Petitioner, are a series of cross-sectional views of a III-nitride device illustrating a series of steps in a process for forming the III-nitride device. Pet. 32–33; Ex. 1005 ¶¶ 40–49.

Petitioner asserts that Beach teaches

- depositing an Ohmic contact metal (ohmic material 18 – pink) in ohmic contact window 11 ([1g1]); (Pet. 36 (citing Ex. 1005 ¶ 45, Figs. 1B, 1C));
- applying a *metal photoresistant pattern* (resist material 13 – blue) over ohmic contact metal 18 ([1g2]); (Pet. 36 (citing Ex. 1005 ¶ 47, Figs. 1C, 1D));
- etching away the ohmic contact metal 18 (pink) except the portion protected by the mask/photoresist layer 13 ([1g3]); (Pet. 37 (citing Ex. 1005 ¶ 47, Figs. 1D, 1E));
- removing the metal photoresistant pattern; ([1g4]); (Pet. 37 (citing Ex. 1005 ¶ 49)); and
- performing rapid thermal annealing to form Ohmic drain and source contacts ([1g5]); (Pet. 38 (citing Ex. 1007 ¶¶ 49, 54)).

Petitioner contends that a POSITA would have been motivated to use Beach's source and drain masking process to form the ohmic source and drain contacts of Yoshida because (1) Beach's masking process was a well-known technique that is suitable for Yoshida and (2) Beach's masking process is simpler compared to alternative "lift-off" processes and would reduce costs. Pet. 23. Petitioner also asserts that (3) Beach's masking process allows a POSITA to use the mask to extend the source ohmic contact region toward the gate contact, allowing a source and gate connected field plate to be easily formed, which reduces electrical field at the gate corner and results in higher breakdown voltage. Pet. 24. Petitioner explains that, in contrast, the lift-off process would require a separate masking step to allow the ohmic contact metal to extend beyond the designated opening, which would require additional processing to provide a field plate design. *Id.*

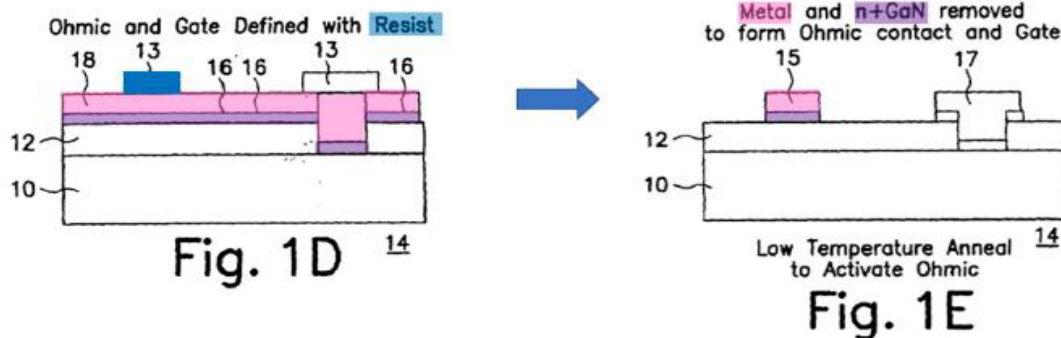
Patent Owner presents a number of arguments in response. Prelim. Resp. 1–22. We have reviewed the parties' arguments and evidence and determine that Petitioner sufficiently shows a reasonable likelihood that claim 1 would have been obvious over Yoshida, Beach, and Sheppard, notwithstanding Patent Owner's arguments to the contrary, which we now address.

Patent Owner first asserts that Petitioner improperly relies on Beach's use of a single photo resist (i.e., photoresist 13 (blue)) to satisfy steps involving both the "*gate photo resistant pattern*" recited in steps [1e] and the "*metal photo resistant pattern*" recited in claim steps [1g]. Prelim. Resp. 1, 17–20. Patent Owner asserts that by doing so, Petitioner improperly conflates the two steps, which are distinctly claimed and correspond to

separate photo resist patterns that are used at different times in the claimed process. *Id.* at 1, 19–20.

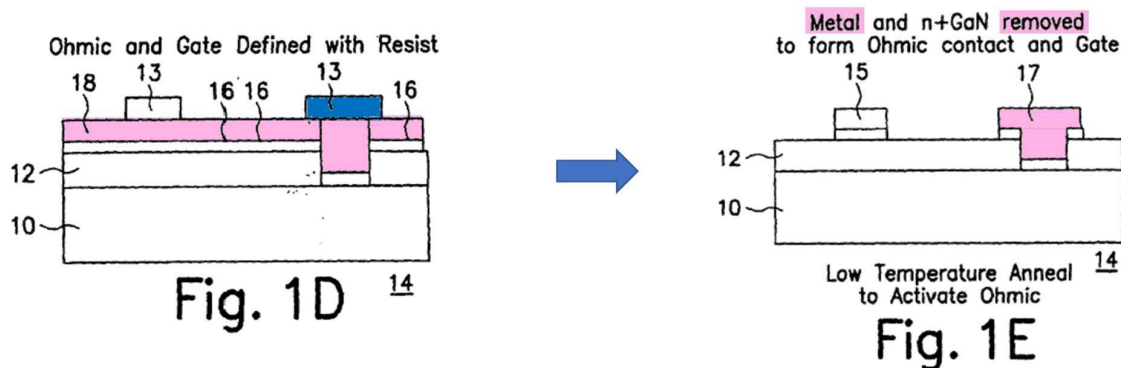
We disagree with Patent Owner based on the present record. As noted above, at this stage of the proceeding, we determine that the claims do not *require* that the application of the gate contact photo resistant layer must occur at a different time than the application of the metal photo resistant pattern.

Additionally, at this stage of the proceeding, we disagree with Patent Owner’s argument that Beach’s “single photo resist pattern” cannot satisfy both the claimed “gate photo resistant pattern” and a “metal photo resistant pattern.” Prelim. Resp. 1. It appears from the present record that Beach’s resist material 13, depending on where it is applied, can be used as both as a “gate photo resistant pattern” as well as a “metal photo resistant pattern.” For example, as shown in Petitioner’s annotated Figures 1D and 1E of Beach below, Beach’s resist layer 13 (blue) acts as a “gate photo resistant pattern” when used to etch layers 18 (pink) and 16 (purple) to form gate 15.



Beach Figures 1D (left) and 1E (right) are a series of cross-sectional views of a III-nitride device with Petitioner’s highlighting added to illustrate use of resist layer 13 (blue) to form gate 15. Pet. 33.

Similarly, as shown in Petitioner’s annotated Figures 1D and 1E below, Beach’s resist layer 13 (blue) acts as a “metal photo resistant pattern” when used to etch ohmic contact metal 18, which has been deposited in ohmic contact window 11 and forms Ohmic contact 17.



Beach Figures 1D (left) and 1E (right) are a series of cross-sectional views of a III-nitride device with Petitioner’s highlighting added to illustrate use of resist layer 13 (blue) to form Ohmic contact 17. Pet. 37.

Although Beach deposits resist 13 in a single step, the resist is applied in different locations with varying types of layers underneath. Thus, depending on where resist layer 13 is applied, resist layer 13 appears to function as a different type of pattern, (i.e., as either as a gate photo resistant pattern or a metal photo resistant pattern). Again, as noted above, based on the present record, claim 1 does not require that the gate photo resistant pattern and the metal photo resistant pattern be applied at different times.

Patent Owner, however, also argues that a POSITA would not have found it obvious combine Yoshida and Beach because, *inter alia*, Beach’s teachings of simultaneously forming the gate contact and ohmic contacts is inconsistent and contrary to the teaching of Yoshida. Prelim. Resp. 20–22. Patent Owner asserts that Beach forms the gate and ohmic contacts by etching metal layer 18 at the same time because Beach forms both the gate and ohmic contacts from the same metal material. *Id.* at 21 (citing Ex. 1005

¶¶ 46–47). Patent Owner asserts that, in contrast, Yoshida forms the drain and source contacts before forming the gate electrode. *Id.* Patent Owner contends that Yoshida’s “gate last” process is dramatically different from Beach’s “simultaneous gate/ohmic contact formation” process, which is also dramatically different from the “gate first” process of the ’508 patent. *Id.* at 21–22.

We recognize that Yoshida’s “gate-last” process—in which the gate contact is formed after the source and drain contacts are formed—differs from Beach’s process—which appears to form the gate contact at the same time as the ohmic (source/drain). We also acknowledge Patent Owner’s arguments that these two methods are inconsistent and contrary to each other. Prelim. Resp. 20–22. However, Petitioner has provided evidence and argument, supported by declaration testimony, that it would have been obvious to combine Yoshida and Beach to arrive at the subject matter of claim 1.

For example, Petitioner asserts that a POSITA would have been motivated to use Beach’s resist pattern 13 as a single gate photo resistant pattern to etch away both Yoshida’s gate contact layer and doped GaN layer in order to remove the second mask step to decrease costs and simplify the manufacturing process, as well as improve gate alignment. Pet. 21 (citing, *inter alia*, Ex. 1003 ¶¶ 125–126). Petitioner has also provided evidence and arguments, supported by declaration testimony, that a POSITA would have been motivated to use Beach’s resist pattern 13 as a metal photo resistant pattern to etch away Yoshida’s metal Al (ohmic contact metal) deposited on layer 4. Pet. 35 (citing Ex. 1004 ¶¶ 10, 22; Ex. 1003 ¶ 135). These contentions are sufficient, for purposes of institution, to show that a POSITA would have had reason to combine Yoshida and Beach in the manner

asserted by Petitioner. Additionally, Petitioner has also provided evidence and arguments, supported by declaration testimony, that a POSITA would have had a reasonable expectation of success in combining the teachings of the prior art to arrive at the claimed invention. Pet. 20. We have considered all of Patent Owner's arguments to the contrary, and determine they raise issues best resolved on a full record.

For all of the foregoing reasons, we determine that Petitioner has sufficiently shown that Yoshida, Beach, and Sheppard teach or suggest all of the limitations of claim 1 and that a person of ordinary skill in the art would have had reason to combine the teachings of the asserted art. Accordingly, we determine that Petitioner has demonstrated a reasonable likelihood of showing that claim 1 would have been obvious over Yoshida, Beach, and Sheppard.

Because we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one of the claims challenged in the Petition, we institute *inter partes* review of all claims and all challenges raised in the petition. Nevertheless, in order to further guide the parties after institution, we provide the following observations.

2. *Claims 2–3*

Claims 2 and 3 depend from claim 1. Petitioner asserts that Yoshida discloses the limitations recited in these dependent claims. Pet. 39–50.

Patent Owner does not address Petitioner's arguments with respect to these dependent claims, apart from its arguments related to independent claim 1, addressed above. We have reviewed Petitioner's arguments and evidence and determine Petitioner has shown sufficiently that Yoshida teaches the limitations recited in these claims. As such, Petitioner

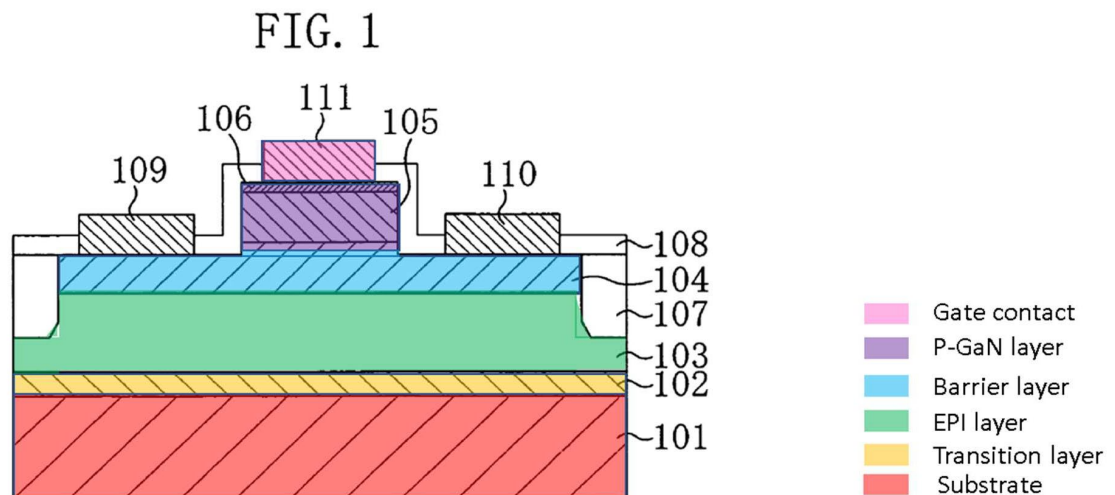
demonstrates a reasonable likelihood that claims 2–3 would have been obvious over Yoshida, Beach, and Sheppard.

E. Alleged Obviousness of Claims 1–4 over Hikita-347, Beach, and Sheppard (Ground 2)

Petitioner asserts that claims 1–4 would have been obvious over Hikita-347, Beach, and Sheppard. Pet. 42–74. Patent Owner opposes. Prelim. Resp. 22–25.

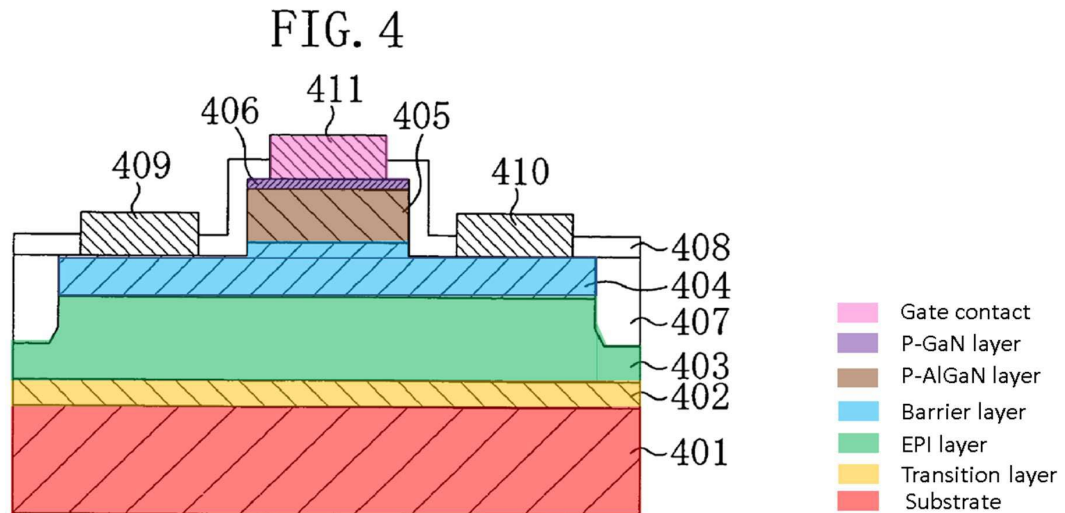
1. Claim 1

Hikita-347 Figures 1 and 4, with Petitioner’s color annotations added, are reproduced below. The transistors shown in Figure 1 and Figure 4 differ in that Figure 4 has a p-type AlGaN layer (layer 405-purple) whereas Figure 1 has p-type GaN layer (layer 105-purple). Ex. 1007 ¶ 49; Pet. 45. Also, Hikita-423 states that layer 106 (dark purple) of Figure 1 is preferable, but not necessary. Ex. 1007 ¶ 40.



Hikita-347 Figure 1 above, with Petitioner’s color annotations added, depicts a GaN transistor according to a first embodiment having substrate layer 101, buffer layer 102, undoped GaN layer 103, undoped AlGaN layer 104, p-type GaN layer 105 (purple), a heavily doped p-type GaN layer 106 (dark purple), isolation region 107, SiN film 108, source electrode 109, drain

electrode 110, and gate electrode 111 (pink). Pet. 43–44; Ex. 1007 ¶¶ 16, 33–39, Fig. 1.



Hikita-347 Figure 4, with Petitioner’s color annotations added, above depicts a GaN transistor according to a second embodiment having substrate layer 401, buffer layer 402, undoped GaN layer 403, undoped AlGaIn layer 404, p-type AlGaIn layer 405, a heavily doped p-type GaN layer 406, isolation region 407, SiN film 408, source electrode 409, drain electrode 410, and gate electrode 411. Ex. 1007 ¶¶ 19, 47–48, Fig. 4.

Petitioner asserts that Hikita-347 discloses forming the transistors shown in the above Figures by:

- Growing, on substrate 101/401, (1) layers 102/402, (2) layers 103/403, (3) layers 104/404, and either (4) a p-GaN layer 105 (purple) or a p-type AlGaIn layer 405 and a p-type layer 406¹². Pet. 45–46 (citing Ex. 1007 ¶¶ 13, 33, 56);
- Etching away either layer 105 or layers 405/406 “in other part than the gate region” (Ex. 1007 ¶¶ 35, 57);

¹² Petitioner further asserts that to the extent Hikita-347 does not explicitly disclose providing multiple transition layers on the substrate, Sheppard renders this obvious. Pet. 53.

- Forming a dielectric layer (SiN film) 108/408 to cover the entire surface with openings formed in the source and drain contact area and gate area (Ex. 1007 ¶¶ 34, 37, 59–61); and
- Forming source and drain contacts and gate contact to produce an enhancement mode GaN transistor (Ex. 1007 ¶¶ 13, 37, 60–67)

Pet. 45–46 (citing Ex. 1003 ¶ 87).

Petitioner contends that Hikita-347 teaches making the structure of Figure 1 using most of the steps recited in claim 1 (i.e., claim steps [1a]–[1d]) and relies on the combination of Hikita-347 and Beach for teaching claim steps [1e] and [1g] and on Hikita-347 and Sheppard for step [1f]. *See* Pet. 42–61. Petitioner also states Hikita-347 does not disclose forming the multiple layers required by claim element [1a] but asserts Sheppard teaches these layers. Pet. 51–54. More specifically, Petitioner asserts Hikita-347 teaches growing the layers required by steps [1a]–[1d] including growing the p-type GaN layer (purple) of step [1d]. *See* Pet. 52–56.

Petitioner asserts that the combination of Hikita-347 and Sheppard teaches the dielectric layer structure steps of [1f]. Petitioner asserts Hikita-347 discloses:

- after etching away the p-type GaN layer (purple), depositing SiN film 108 (a dielectric layer) to cover an upper surface of the transistor (Pet. 58; Ex. 1007 ¶¶ 34, 67, 59) (step [1f1]).

Petitioner asserts that although Hikita-347 discloses etching to form openings in the dielectric layer 108 for drain and source contacts, that Hikita-347 does not explicitly disclose using a mask (contact photo resistant pattern) to form the openings. Pet. 59. For this, Petitioner asserts that Sheppard discloses:

- using a mask pattern (mask 40) to form openings in cap layer 24 for the source/drain contacts, an etching process that exposes areas of underlying barrier 2, and removing mask 40 after the

ohmic contacts are formed. Pet. 59–60 (citing Ex. 1006 8:55–67, Figs. 1B, 1C, 1D).

With respect to the gate structure steps of 1[e], Petitioner states that Hikita-347 does not teach claim steps [1e2]–[1e5], which require use of a *single mask* (gate photo resistant pattern) to etch both p-GaN layer 105 and the gate contact 111. See Pet. 56–57. Petitioner, contends however, similar to its arguments for ground 1, that a POSITA would have used Beach’s single mask to etch Hikita-347’s p-GaN layer (purple) and gate (pink), thereby removing Hikita-347’s additional second mask step, in order to simplify the manufacturing process and reduce costs. Pet. 48–49, 57–58 (citing, *inter alia*, Ex. 1003 ¶¶ 179, 229).

With respect to the ohmic contact steps of [1g], Petitioner states Hikita-347 discloses step [1g1] by disclosing the deposition of a Ti layer and an Al layer (ohmic contact metal) on n-undoped AlGaIn layer 104 to form source electrode 109 and drain electrode 110 (Pet. 60–61 (citing Ex. 1007 ¶¶ 34, 60)) and performing the rapid thermal annealing to form ohmic drain and source contacts of step [1g5] (Pet. 61 (citing Ex. 1007 ¶ 60)).

Petitioner admits that Hikita-357 does not teach claim steps [1g2]–[1g4], which require applying a metal photo resistant pattern, etching the ohmic contact metal, and removing the metal photo resistant pattern, but contends that “Beach discloses using a masking and etching process ([1g2], [1g3], [1g4]) to form ohmic contacts as explained in Ground 1.” Pet. 61.

Patent Owner argues that, similar to ground 1, Petitioner improperly conflates the use of single photoresist (13) in Beach, with the use of both the “gate photo resistant pattern” and “metal photo resistant pattern” that are used in different steps in the claimed process. Prelim. Resp. 23. Again, Patent Owner asserts that Beach’s single photoresist pattern 13, which is

used to simultaneously form both a gate as well as ohmic contacts cannot correspond to the separately claimed “gate photo resistant pattern” and “metal photo resistant pattern.” *Id.* at 23–24.

We have reviewed the parties’ evidence and arguments and determine Petitioner has shown sufficiently that claim 1 would have been unpatentable over the asserted art, notwithstanding Patent Owner’s arguments to the contrary. Patent Owner’s arguments, which are similar to those set forth with respect to ground 1, raise issues best resolved on a full record. As such, Petitioner sufficiently demonstrates a reasonable likelihood that claim 1 would have been obvious over Hikita-347, Beach, and Sheppard.

2. *Claims 2–3*

Claims 2–3 depend from claim 1. Petitioner asserts that Sheppard teaches the limitations recited in these claims and articulates a reason a POSITA would have been motivated to combine Sheppard with Hikita-347 and Beach. Pet. 61–65. Patent Owner does not address Petitioner’s arguments with respect to these dependent claims, apart from its arguments related to independent claim 1, addressed above.

We have reviewed Petitioner’s arguments and evidence and determine Petitioner has shown sufficiently that Sheppard teaches the limitations recited in these claims and that a person of ordinary skill in the art would have had reason to combine the teachings of the asserted art. As such, Petitioner demonstrates a reasonable likelihood that claims 2–3 would have been obvious over Hikita-347, Beach, and Sheppard.

3. *Claim 4*

There is much overlap between the limitations of independent claim 4 and those of independent claim 1. *Compare* Ex. 1001, 6:59–7:15 (claim 1) *with id.* at 7:21–8:7 (claim 4). For example, claim element [1e] is similar to

claim element [4f], except that claim element [4f4] further requires a doped InAlGaN layer as indicated in italics below:

[4f]:

- [4f1] depositing a gate contact layer on the doped GaN layer;
- [4f2] applying a gate photo resistant pattern;
- [4f3] etching away the gate contact layer outside the gate region;
- [4f4] etching away the doped GaN layer *and the doped InAlGaN layer*, except a portion of the doped GaN layer *and the doped InAlGaN layer* beneath the gate contact;
- [4f5] removing the gate photo resistant pattern;

Ex. 1001, 7:31–37.

Step [4g] is identical to step [1f] and step [4h] is identical to step [1g].
See Pet. 73–74.

Petitioner relies on its assertions regarding claim 1 for similar limitations found in claim 4. *See* Pet. 66–74. Petitioner relies on Hikita-347 for disclosing the additional limitations relating to the InAlGaN layers. *See* Pet. 71–73. Patent Owner asserts claim 4 is patentable for the same reasons as claim 1. Prelim. Resp. 22–24.

We have reviewed the parties’ evidence and arguments and determine Petitioner has shown sufficiently that claim 4 would have been unpatentable over Hikita-347, Beach, and Sheppard, notwithstanding Patent Owner’s arguments to the contrary. Patent Owner’s arguments, which are similar to those set forth with respect to ground 1, raise issues that are best resolved on a full record. As such, Petitioner sufficiently demonstrates a reasonable likelihood that claim 4 would have been obvious over Hikita-347, Beach, and Sheppard.

F. Alleged Obviousness of Claim 5 over Hikita-023, Beach, and Sheppard (Ground 3)

Petitioner asserts that claim 5 is unpatentable over Hikita-023, Beach, and Sheppard. Pet. 74–90. Patent Owner opposes. Prelim Resp. 25–27.

Claim 5 is directed to a method of forming an enhancement mode GaN transistor, that requires, in general:

- growing various layers (steps [5a]–[5e]), including a doped AlGa_N layer (step [5d]) and a doped Ga_N layer (step [5e]);
- depositing a gate contact layer on the doped Ga_N layer, applying a particular pattern (i.e., a “*gate photo resist pattern*”), etching the gate contact layer, etching an underlying layer, and removing the gate photoresist pattern (steps [5f1]–[5f5]);
- applying another photo resistant pattern, etching the doped AlGa_N layer, and removing the photo resistant pattern (steps [5g1]–[5g3]);
- depositing a dielectric layer, applying a particular pattern (i.e., a “*contact photo resistant pattern*”), etching the dielectric layer to open drain and source contact areas, and removing the contact photo resist pattern (steps [5h1]–[5h4]); and
- depositing an Ohmic contact metal, applying a particular pattern (i.e., a “*fourth photo resistant pattern*”), etching the Ohmic contact metal, removing the fourth photo resistant pattern, and performing rapid thermal annealing to form Ohmic drain and source contacts (steps [5i1]–[5i5]).

Petitioner relies on the combined teachings of Hikita-023, Beach, and Sheppard for teaching the steps of claim 5. Pet. 78–90.

For example, Petitioner asserts that Hikita-023 teaches many of the limitations of claim 5, but concedes that Hikita-023 does not disclose the claimed “applying a gate photo resistant pattern” of step [5f] and the claimed “applying a fourth photo resistant pattern” of step [5i]. See Pet. 84–86, 89–90. Similar to the arguments presented for grounds 1 and 2, Petitioner relies on Beach’s use of the single resist pattern (13) as teaching two different

patterns, namely the “gate photo resistant pattern” of step [5f] and the “fourth photo resistant pattern” of step [5i]. Pet. 84–86, 89–90. With respect to step [5h], which is similar to steps [1f] and [4f], Petitioner states “Hikita-023 discloses depositing a dielectric layer, and *Sheppard* renders obvious all steps of [5h].” Pet. 88.

Patent Owner asserts that, similar to grounds 1 and 2, Petitioner improperly conflates the use of Beach’s single photoresist with use of a “gate photo resist pattern” and “fourth photo resistant” pattern, which are distinctly claimed in the ’508 patent and correspond to separate photo resist patterns that are used at different times in the claimed process. Prelim. Resp. 25–26.

We have reviewed the parties’ evidence and arguments and determine Petitioner has shown sufficiently that claim 5 would have been unpatentable over Hikita-023, Beach, and Sheppard, notwithstanding Patent Owner’s arguments to the contrary. Patent Owner’s arguments, which are similar to those set forth with respect to grounds 1 and 2, raise issues that are best resolved on a full record. As such, Petitioner demonstrates a reasonable likelihood that claim 5 would have been obvious over Hikita-023, Beach, and Sheppard.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one challenged claim of the ’508 patent. Thus, we institute an *inter partes* review on all challenged claims and on all grounds presented.

IV. ORDER

In consideration of the foregoing, it is hereby:

IPR2023-01383

Patent 8,404,508 B2

ORDERED that an *inter partes* review is instituted on each of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this decision.

IPR2023-01383
Patent 8,404,508 B2
FOR PETITIONER:

Lionel Lavenue
Kara Specht
Cory Bell
Forrest Jones
Chen Zang
Yi Yu
Luke MacDonald
Carlos Duarte-Guevara
FINNEGAN, HENDERSON, FARABOW, GARRETT, & DUNNER LLP
lionel.lavenue@finnegan.com
kara.specht@finnegan.com
cory.bell@finnegan.com
forrest.jones@finnegan.com
chen.zang@finnegan.com
yi.yu@finnegan.com
luke.macdonald@finnegan.com
carlos.duarte-guevara@finnegan.com

FOR PATENT OWNER:

Walter Davis
Dipu Doshi
Mark Thronson
Stephen Soffen
Ameya Paradkar
Jonathan England
BLANK ROME LLP
walter.davis@blankrome.com
dipu.doshi@blankrome.com
mthronson@blankrome.com
ssoffen@blankrome.com
aparadkar@blankrome.com
jwengland@blankrome.com